# 3.3V, 2.5V, 1:9 LVCMOS Clock Fanout Buffer

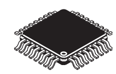
# MPC9447

PRODUCT DISCONTINUATION NOTICE - LAST TIME BUY EXPIRES SEPTEMBER 7, 2016

DATA SHEET

The Freescale Semiconductor, Inc. MPC9447 is a 3.3 V or 2.5 V compatible, 1:9 clock fanout buffer targeted for high performance clock tree applications. With output frequencies up to 350 MHz and output skews less than 150 ps, the device meets the needs of most demanding clock applications.

**LOW VOLTAGE**
**3.3 V/2.5 V LVCMOS 1:9**
**CLOCK FANOUT BUFFER**



**AC SUFFIX**
**32-LEAD LQFP PACKAGE**
**Pb-FREE PACKAGE**
**CASE 873A-03**

### Features

- 9 LVCMOS Compatible Clock Outputs
- 2 Selectable, LVCMOS Compatible Inputs
- Maximum Clock Frequency of 350 MHz
- Maximum Clock Skew of 150 ps
- Synchronous Output Stop in Logic Low State Eliminates Output Runt Pulses
- High-Impedance Output Control
- 3.3 V or 2.5 V Power Supply
- Drives up to 18 Series Terminated Clock Lines
- Ambient Temperature Range -40°C to +85°C
- 32-Lead LQFP Packaging, Pb-free
- Supports Clock Distribution in Networking, Telecommunications, and Computer Applications
- Pin and Function Compatible to MPC947
- For drop in replacement use 83947AYILN

### Functional Description

MPC9447 is specifically designed to distribute LVCMOS compatible clock signals up to a frequency of 350 MHz. Each output provides a precise copy of the input signal with a near zero skew. The outputs buffers support driving of 50 Ω terminated transmission lines on the incident edge. Each is capable of driving either one parallel terminated or two series terminated transmission lines.

Two selectable independent LVCMOS compatible clock inputs are available, providing support of redundant clock source systems. The MPC9447 $\overline{\text{CLK\_STOP}}$ control is synchronous to the falling edge of the input clock. It allows the start and stop of the output clock signal only in a logic low state, and thus, eliminates potential output runt pulses. Applying the OE control will force the outputs into high-impedance mode.

All inputs have an internal pull-up or pull-down resistor preventing unused and open inputs from floating. The device supports a 2.5 V or 3.3 V power supply and an ambient temperature range of -40°C to +85°C. The MPC9447 is pin and function compatible but performance-enhanced to the MPC947.

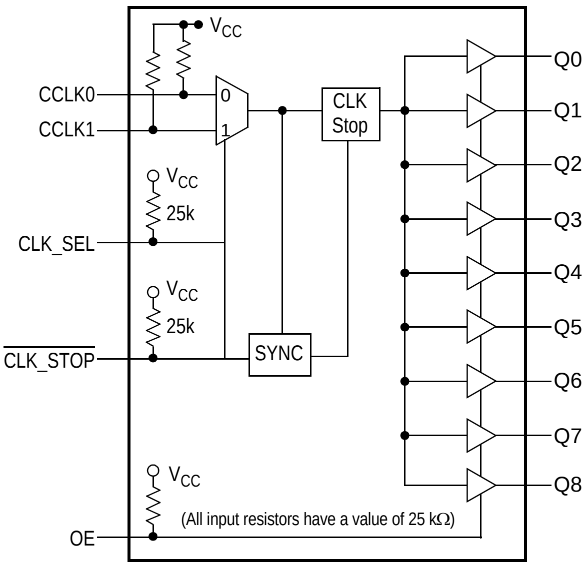



**Figure 1. Logic Diagram**

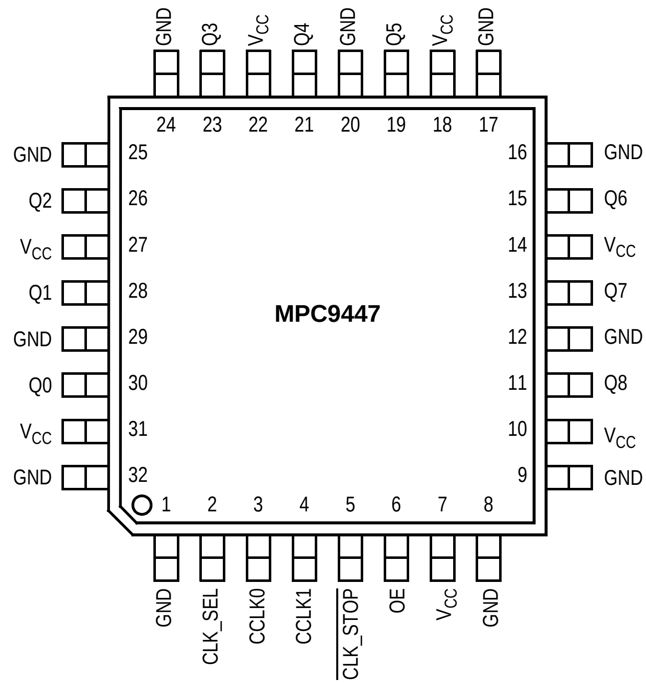



**Figure 2. 32-Lead Pinout** (Top View)

### Table 1. Function Table

| Control | Default | 0 | 1 |
|---|---|---|---|
| CLK_SEL | 1 | CLK0 input selected | CLK1 input selected |
| OE | 1 | Outputs disabled (high-impedance state)(1) | Outputs enabled |
| $\overline{\text{CLK\_STOP}}$ | 1 | Outputs synchronously stopped in logic low state | Outputs active |

1. OE = 0 will high-impedance tristate all outputs independent on $\overline{\text{CLK\_STOP}}$.

### Table 2. Pin Configurations

| Pin | I/O | Type | Function |
|---|---|---|---|
| CCLK0 | Input | LVCMOS | Clock Signal Input |
| CCLK1 | Input | LVCMOS | Alternative Clock Signal Input |
| CLK_SEL | Input | LVCMOS | Clock Input Select |
| $\overline{\text{CLK\_STOP}}$ | Input | LVCMOS | Clock Output Enable/Disable |
| OE | Input | LVCMOS | Output Enable/Disable (high-impedance tristate) |
| Q0–8 | Output | LVCMOS | Clock Outputs |
| GND | Supply | Ground | Negative Power Supply (GND) |
| $V_{CC}$ | Supply | $V_{CC}$ | Positive power supply for I/O and core. All $V_{CC}$ pins must be connected to the positive power supply for correct operation |

**Table 3. General Specifications**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{TT}$ | Output Termination Voltage | | $V_{CC} \div 2$ | | V | |
| MM | ESD Protection (Machine model) | 200 | | | V | |
| HBM | ESD Protection (Human body model) | 2000 | | | V | |
| LU | Latch-up Immunity | 200 | | | mA | |
| $C_{PD}$ | Power Dissipation Capacitance | | 10 | | pF | Per output |
| $C_{IN}$ | Input Capacitance | | 4.0 | | pF | Inputs |

**Table 4. Absolute Maximum Ratings**[1]

| Symbol | Characteristics | Min | Max | Unit | Condition |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | –0.3 | 3.9 | V | |
| $V_{IN}$ | DC Input Voltage | –0.3 | $V_{CC}$ + 0.3 | V | |
| $V_{OUT}$ | DC Output Voltage | –0.3 | $V_{CC}$ + 0.3 | V | |
| $I_{IN}$ | DC Input Current | | ±20 | mA | |
| $I_{OUT}$ | DC Output Current | | ±50 | mA | |
| $T_S$ | Storage temperature | –65 | 125 | °C | |

1. Absolute maximum continuous ratings are those maximum values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation at absolute-maximum-rated conditions is not implied.

**Table 5. DC Characteristics** ($V_{CC}$ = 3.3 V ± 5%, $T_A$ = -40°C to +85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 2.0 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | –0.3 | | 0.8 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 2.4 | | | V | $I_{OH}$ = –24 mA[1] |
| $V_{OL}$ | Output Low Voltage | | | 0.55<br>0.30 | V<br>V | $I_{OL}$ = 24 mA<br>$I_{OL}$ = 12 mA |
| $Z_{OUT}$ | Output Impedance | | 17 | | Ω | |
| $I_{IN}$ | Input Current[2] | | | ±300 | μA | $V_{IN} = V_{CC}$ or GND |
| $I_{CCQ}$ | Maximum Quiescent Supply Current[3] | | | 2.0 | mA | All $V_{CC}$ Pins |

1. The MPC9447 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives up to two 50 Ω series terminated transmission lines (for $V_{CC}$ = 3.3 V).
2. Inputs have pull-down or pull-up resistors affecting the input current.
3. $I_{CCQ}$ is the DC current consumption of the device with all outputs open and the input in its default state or open.

**Table 6. AC Characteristics** ($V_{CC}$ = 3.3 V ± 5%, $T_A$ = -40°C to +85°C)**(1)**

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency | 0 | | 350 | MHz | |
| $f_{max}$ | Output Frequency | 0 | | 350 | MHz | |
| $f_{P,REF}$ | Reference Input Pulse Width | 1.4 | | | ns | |
| $t_r$, $t_f$ | CCLK0, CCLK1 Input Rise/Fall Time | | | 1.0(2) | ns | 0.8 to 2.0 V |
| $t_{PLH/HL}$ | Propagation Delay CCLK0 or CCLK1 to any Q | 1.3 | | 3.3 | ns | |
| $t_{PLZ, HZ}$ | Output Disable Time | | | 11 | ns | |
| $t_{PZL, ZH}$ | Output Enable Time | | | 11 | ns | |
| $t_S$ | Setup Time CCLK0 or CCLK1 to $\overline{\text{CLK\_STOP}}$(3) | 0.0 | | | ns | |
| $t_H$ | Hold Time CCLK0 or CCLK1 to $\overline{\text{CLK\_STOP}}$(3) | 1.0 | | | ns | |
| $t_{sk(O)}$ | Output-to-Output Skew | | | 150 | ps | |
| $t_{sk(PP)}$ | Device-to-Device Skew | | | 2.0 | ns | |
| $t_{SK(P)}$<br>$DC_Q$ | Output Pulse Skew(4)<br>Output Duty Cycle $f_Q$<170 MHz | <br>45 | <br>50 | 300<br>55 | ps<br>% | <br>$DC_{REF}$ = 50% |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.1 | | 1.0 | ns | 0.55 to 2.4 V |
| $t_{JIT}$ | Buffer Additive Phase Jitter, RMS | | 0.03 | | ps | 156.25MHz,<br>Integration Range:<br>12kHz - 20MHz |

1. AC characteristics apply for parallel output termination of 50 Ω to $V_{TT}$.
2. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
3. Setup and hold times are referenced to the falling edge of the selected clock signal input.
4. Output pulse skew is the absolute difference of the propagation delay times: | $t_{PLH}$ – $t_{PHL}$ |.

**Table 7. DC Characteristics** ($V_{CC}$ = 2.5 V ± 5%, $T_A$ = -40°C to +85°C)

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage | 1.7 | | $V_{CC}$ + 0.3 | V | LVCMOS |
| $V_{IL}$ | Input Low Voltage | –0.3 | | 0.7 | V | LVCMOS |
| $V_{OH}$ | Output High Voltage | 1.8 | | | V | $I_{OH}$ = –15 mA(1) |
| $V_{OL}$ | Output Low Voltage | | | 0.6 | V | $I_{OL}$ = 15 mA |
| $Z_{OUT}$ | Output Impedance | | 19 | | Ω | |
| $I_{IN}$ | Input Current(2) | | | ±300 | μA | $V_{IN}$ = $V_{CC}$ or GND |
| $I_{CCQ}$ | Maximum Quiescent Supply Current(3) | | | 2.0 | mA | All $V_{CC}$ Pins |

1. The MPC9447 is capable of driving 50 Ω transmission lines on the incident edge. Each output drives one 50 Ω parallel terminated transmission line to a termination voltage of $V_{TT}$. Alternatively, the device drives one 50 Ω series terminated transmission lines per output ($V_{CC}$ = 2.5 V).
2. Inputs have pull-down or pull-up resistors affecting the input current.
3. $I_{CCQ}$ is the DC current consumption of the device with all outputs open and the input in its default state or open.

**Table 8. AC Characteristics** ($V_{CC}$ = 2.5 V ± 5%, $T_A$ = -40°C to +85°C)[1]

| Symbol | Characteristics | Min | Typ | Max | Unit | Condition |
|---|---|---|---|---|---|---|
| $f_{ref}$ | Input Frequency | 0 | | 350 | MHz | |
| $f_{max}$ | Output Frequency | 0 | | 350 | MHz | |
| $f_{P,REF}$ | Reference Input Pulse Width | 1.4 | | | ns | |
| $t_r$, $t_f$ | CCLK0, CCLK1 Input Rise/Fall Time | | | 1.0[2] | ns | 0.7 to 1.7 V |
| $t_{PLH/HL}$ | Propagation Delay CCLK0 or CCLK1 to any Q | 1.7 | | 4.4 | ns | |
| $t_{PLZ, HZ}$ | Output Disable Time | | | 11 | ns | |
| $t_{PZL, ZH}$ | Output Enable Time | | | 11 | ns | |
| $t_S$ | Setup Time CCLK0 or CCLK1 to $\overline{\text{CLK\_STOP}}$[3] | 0.0 | | | ns | |
| $t_H$ | Hold Time CCLK0 or CCLK1 to $\overline{\text{CLK\_STOP}}$[3] | 1.0 | | | ns | |
| $t_{sk(O)}$ | Output-to-Output Skew | | | 150 | ps | |
| $t_{sk(PP)}$ | Device-to-Device Skew | | | 2.7 | ns | |
| $t_{SK(P)}$<br>$DC_Q$ | Ouput Pulse Skew[4]<br>Output Duty Cycle $f_Q$<350 MHz | <br>45 | <br>50 | 200<br>55 | ps<br>% | <br>$DC_{REF}$ = 50% |
| $t_r$, $t_f$ | Output Rise/Fall Time | 0.1 | | 1.0 | ns | 0.6 to 1.8 V |
| $t_{JIT}$ | Buffer Additive Phase Jitter, RMS | | 0.03 | | ps | 156.25MHz,<br>Integration Range:<br>12kHz - 20MHz |

1. AC characteristics apply for parallel output termination of 50 Ω to $V_{TT}$.
2. Violation of the 1.0 ns maximum input rise and fall time limit will affect the device propagation delay, device-to-device skew, reference input pulse width, output duty cycle and maximum frequency specifications.
3. Setup and hold times are referenced to the falling edge of the selected clock signal input.
4. Output pulse skew is the absolute difference of the propagation delay times: | $t_{PLH}$ – $t_{PHL}$ |.

## APPLICATION INFORMATION

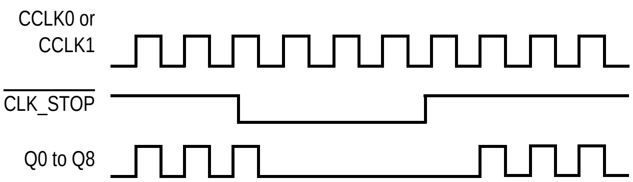



**Figure 3. Output Clock Stop (CLK_STOP) Timing Diagram**

### Driving Transmission Lines

The MPC9447 clock driver was designed to drive high-speed signals in a terminated transmission line environment. To provide the optimum flexibility to the user, the output drivers were designed to exhibit the lowest impedance possible. With an output impedance of 17 Ω ($V_{CC}$ = 3.3 V), the outputs can drive either parallel or series terminated transmission lines. For more information on transmission lines, the reader is referred to Freescale application note AN1091. In most high performance clock networks, point-to-point distribution of signals is the method of choice. In a point-to-point scheme, either series terminated or parallel terminated transmission lines can be used. The parallel technique terminates the signal at the end of the line with a 50 Ω resistance to $V_{CC}$÷2.

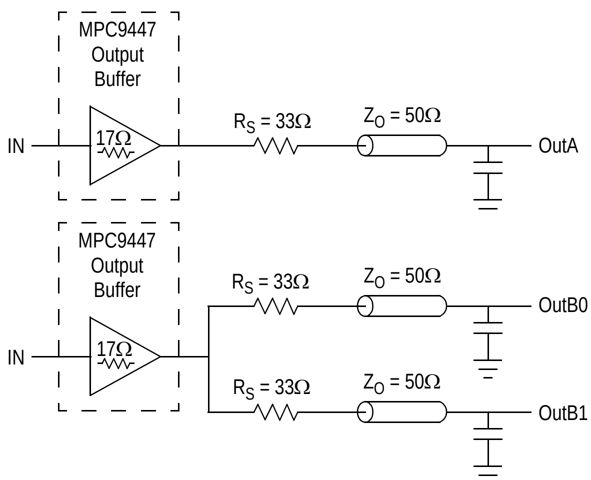



**Figure 4. Single versus Dual Transmission Lines**

This technique draws a fairly high level of DC current, and thus, only a single terminated line can be driven by each output of the MPC9447 clock driver. For the series terminated case, however, there is no DC current draw; thus, the outputs can drive multiple series terminated lines. Figure 4 illustrates an output driving a single series terminated line versus two series terminated lines in parallel. When taken to its extreme, the fanout of the MPC9447 clock driver is effectively doubled due to its capability to drive multiple lines at $V_{CC}$ = 3.3 V.

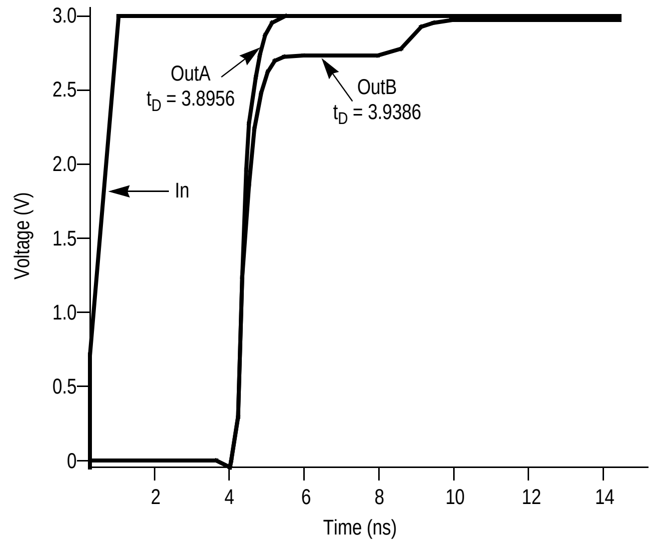


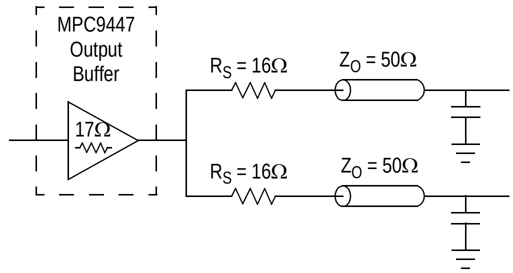

**Figure 5. Single versus Dual Line Termination Waveforms**

The waveform plots in Figure 5 show the simulation results of an output driving a single line versus two lines. In both cases, the drive capability of the MPC9447 output buffer is more than sufficient to drive 50 Ω transmission lines on the incident edge. Note from the delay measurements in the simulation,s a delta of only 43 ps exists between the two differently loaded outputs. This suggests that the dual line driving need not be used exclusively to maintain the tight output-to-output skew of the MPC9447. The output waveform in Figure 5 shows a step in the waveform; this step is caused by the impedance mismatch seen looking into the driver. The parallel combination of the 33 Ω series resistor, plus the output impedance, does not match the parallel combination of the line impedances. The voltage wave launched down the two lines will equal:

$$V_L = V_S (Z_0 \div (R_S + R_0 + Z_0))$$
$$Z_0 = 50\ \Omega \ ||\ 50\ \Omega$$
$$R_S = 33\ \Omega \ ||\ 33\ \Omega$$
$$R_0 = 17\ \Omega$$
$$V_L = 3.0 (25 \div (16.5+17+25)$$
$$= 1.28 \text{ V}$$

At the load end, the voltage will double, due to the near unity reflection coefficient, to 2.5 V. It will then increment towards the quiescent 3.0 V in steps separated by one round trip delay (in this case 4.0 ns).

Since this step is well above the threshold region, it will not cause any false clock triggering; however, designers may be uncomfortable with unwanted reflections on the line. To better match the impedances when driving multiple lines, the situation in Figure 6 should be used. In this case, the series terminating resistors are reduced such that when the parallel combination is added to the output buffer impedance, the line impedance is perfectly matched.




$$17\Omega + 16\Omega \,||\, 16\Omega = 50\Omega \,||\, 50\Omega$$
$$25\Omega = 25\Omega$$

**Figure 6. Optimized Dual Line Termination**

**The Following Figures Illustrate the Measurement Reference for the MPC9447 Clock Driver Circuit**

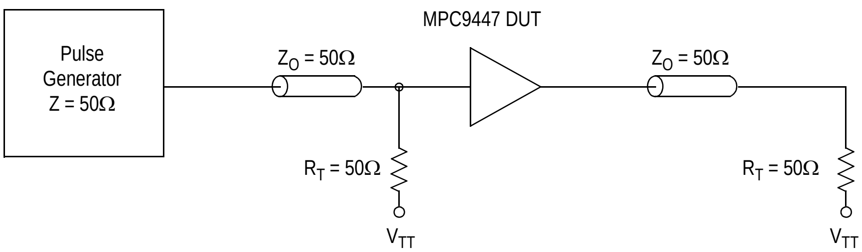



**Figure 7. CCLK MPC9447 AC Test Reference for $V_{CC}$ = 3.3 V and $V_{CC}$ = 2.5 V**

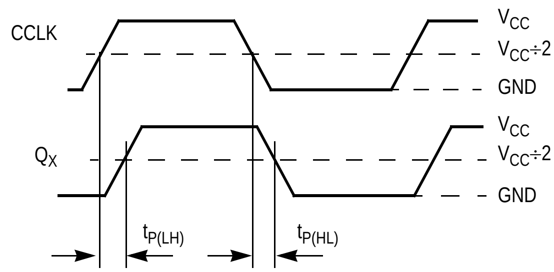
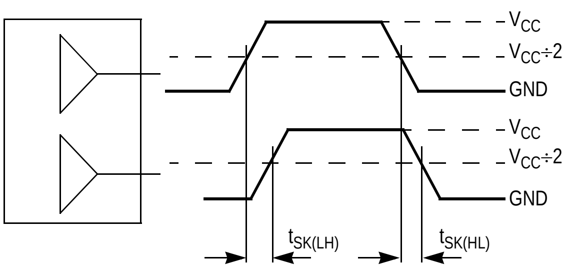
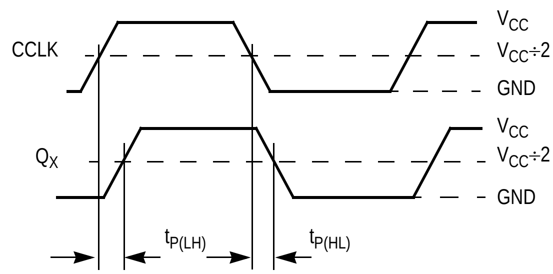



**Figure 8. Propagation Delay ($t_{PD}$) Test Reference**



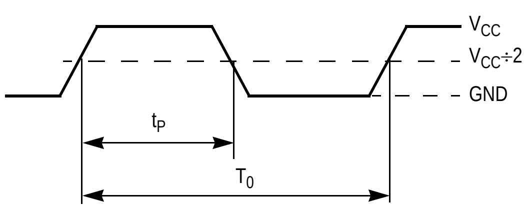

The pin-to-pin skew is defined as the worst case difference in propagation delay between any similar delay path within a single device.

**Figure 9. Output-to-Output Skew $t_{SK(LH, HL)}$**




$t_{SK(P)} = | t_{PLH} - t_{PHL} |$

**Figure 10. Output Pulse Skew ($t_{SK(P)}$) Test Reference**




*DC = (tP ? T0 x 100%)*

The time from the output controlled edge to the non-controlled edge, divided by the time between output controlled edges, expressed as a percentage.

**Figure 11. Output Duty Cycle (DC)**

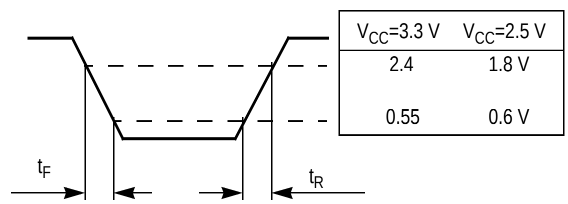
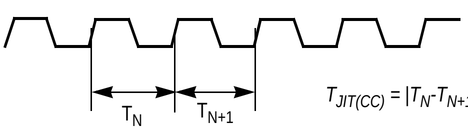



**Figure 12. Output Transition Time Test Reference**




$T_{JIT(CC)} = |T_N - T_{N+1}|$

The variation in cycle time of a signal between adjacent cycles, over a random sample of adjacent cycle pairs.

**Figure 13. Cycle-to-Cycle Jitter**

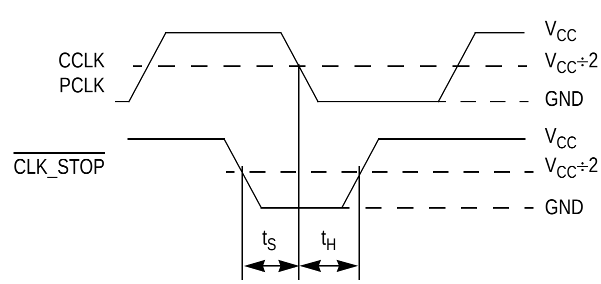
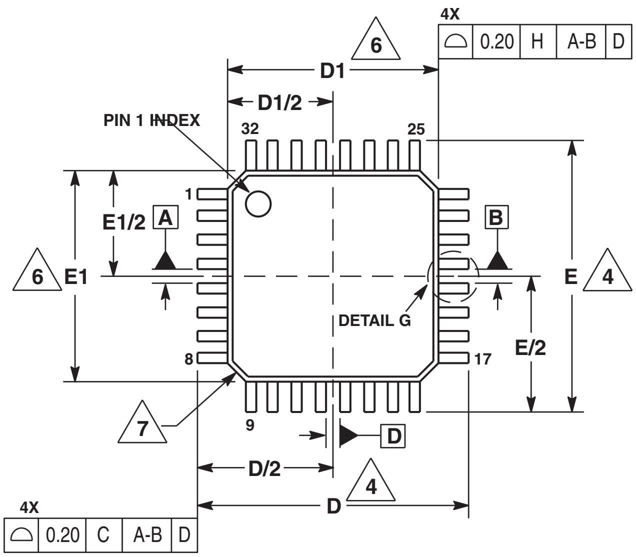
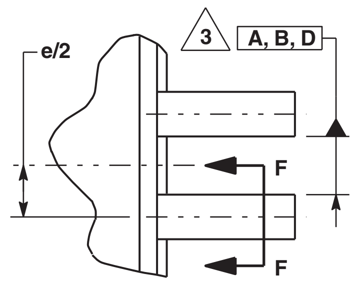



**Figure 14. Setup and Hold Time ($t_S$, $t_H$) Test Reference**

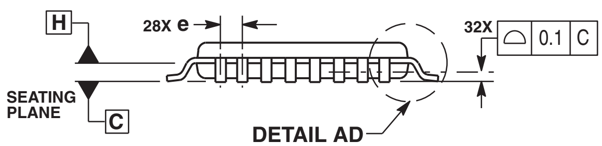
## PACKAGE DIMENSIONS

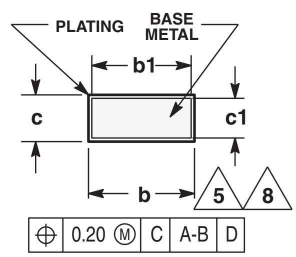



DETAIL G

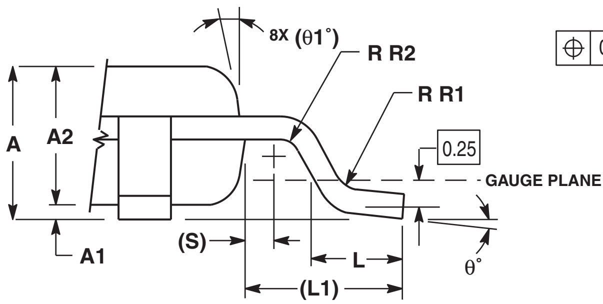
NOTES:
1. DIMENSIONS ARE IN MILLIMETERS.
2. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994.
3. DATUMS A, B, AND D TO BE DETERMINED AT DATUM PLANE H.
4. DIMENSIONS D AND E TO BE DETERMINED AT SEATING PLANE C.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED THE MAXIMUM b DIMENSION BY MORE THAN 0.08-mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD OR PROTRUSION: 0.07-mm.
6. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD PROTRUSION. ALLOWABLE PROTRUSION IS 0.25-mm PER SIDE. D1 AND E1 ARE MAXIMUM PLASTIC BODY SIZE DIMENSIONS INCLUDING MOLD MISMATCH.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1-mm AND 0.25-mm FROM THE LEAD TIP.




SECTION F-F

| DIM | MILLIMETERS MIN | MAX |
|---|---|---|
| A | 1.40 | 1.60 |
| A1 | 0.05 | 0.15 |
| A2 | 1.35 | 1.45 |
| b | 0.30 | 0.45 |
| b1 | 0.30 | 0.40 |
| c | 0.09 | 0.20 |
| c1 | 0.09 | 0.16 |
| D | 9.00 BSC | |
| D1 | 7.00 BSC | |
| e | 0.80 BSC | |
| E | 9.00 BSC | |
| E1 | 7.00 BSC | |
| L | 0.50 | 0.70 |
| L1 | 1.00 REF | |
| q | 0° | 7° |
| q1 | 12 REF | |
| R1 | 0.08 | 0.20 |
| R2 | 0.08 | --- |
| S | 0.20 REF | |




DETAIL AD

**CASE 873A-03**
**ISSUE B**
**32-LEAD LQFP PACKAGE**

**REVISION HISTORY SHEET**

| Rev | Table | Page | Description of Change | Date |
|---|---|---|---|---|
| 7 | <br><br><br>T6, T8 | 1<br>2<br><br>4, 5<br>6 | Functional Description - corrected pin name CLK_STOP to $\overline{\text{CLK\_STOP}}$.<br>Logic Diagram (fig 1) - corrected pin name CLK_STOP to $\overline{\text{CLK\_STOP}}$ and deleted bar from pin 1, 2, 3, 4, 6, 9, 11, 20, 25.<br>AC Characteristics table - corrected pin name CLK_STOP to $\overline{\text{CLK\_STOP}}$.<br>Figure 3 Diagram and Title - corrected pin name CLK_STOP to $\overline{\text{CLK\_STOP}}$. | 9/12/11 |
| 8 | | 1 | Removed leaded part information | 11/16/12 |
| 8 | | 1 | NRND – Not Recommend for New Designs | 12/21/12 |
| 9 | | 1 | Removed NRND and updated data sheet format | 3/18/15 |
| 9 | | 1 | Product Discontinuation Notice - Last time buy expires September 7, 2016.<br>PDN N-16-02 | 3/15/16 |

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