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April 1st, 2010 Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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SILICON POWER MOS FET NE552R679A

3.0 V OPERATION SILICON RF POWER LDMOS FET FOR 460 MHz 0.6 W TRANSMISSION AMPLIFIERS

DESCRIPTION

The NE552R679A is an N-channel silicon power laterally diffused MOS FET specially designed as the transmission power amplifier for 3.0 V FRS (Family Radio Service). Dies are manufactured using our NEWMOS2 technology (our WSi gate laterally diffused MOS FET) and housed in a surface mount package. This device can deliver 28.0 dBm output power with 60% power added efficiency at 460 MHz under the 3.0 V supply voltage.

FEATURES

High output power
 Pout = 28.0 dBm TYP. (VDs = 3.0 V, IDset = 300 mA, f = 460 MHz, Pin = 15 dBm)
 High power added efficiency
 η_{add} = 60% TYP. (VDs = 3.0 V, IDset = 300 mA, f = 460 MHz, Pin = 15 dBm)
 High linear gain
 GL = 20 dB TYP. (VDs = 3.0 V, IDset = 300 mA, f = 460 MHz, Pin = 5 dBm)

Surface mount package : 5.7 × 5.7 × 1.1 mm MAX.

Single supply : VDS = 2.8 to 6.0 V

APPLICATION

• Family Radio Service : 3.0 V Handsets

ORDERING INFORMATION

Part Number	Package	Marking	Supplying Form
NE552R679A-T1	79A	AU	12 mm wide embossed tapingGate pin face the perforation side of the tapeQty 1 kpcs/reel
NE552R679A-T1A			12 mm wide embossed tapingGate pin face the perforation side of the tapeQty 5 kpcs/reel

Remark To order evaluation samples, contact your nearby sales office.

Part number for sample order: NE552R679A

Caution Observe precautions when handling because these devices are sensitive to electrostatic discharge.

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ABSOLUTE MAXIMUM RATINGS ($T_A = +25$ °C)

Parameter	Symbol	Ratings	Unit
Drain to Source Voltage	VDS	15.0	V
Gate to Source Voltage	Vgs	5.0	V
Drain Current	lσ	350	mA
Drain Current (Pulse Test)	ID Note	600	mA
Total Power Dissipation	Ptot	10	W
Channel Temperature	Tch	125	°C
Storage Temperature	Tstg	-55 to +125	°C

Note Duty Cycle 50%, $T_{on} \le 1 \text{ s}$

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Drain to Source Voltage	VDS		2.8	3.0	6.0	V
Gate to Source Voltage	Vgs		0	2.0	3.0	V
Drain Current	lσ			300	500	mA
Input Power	Pin	f = 460 MHz, V _{DS} = 3.0 V	14	15	20	dBm

ELECTRICAL CHARACTERISTICS

(TA = +25°C, unless otherwise specified, using NEC standard test fixture)

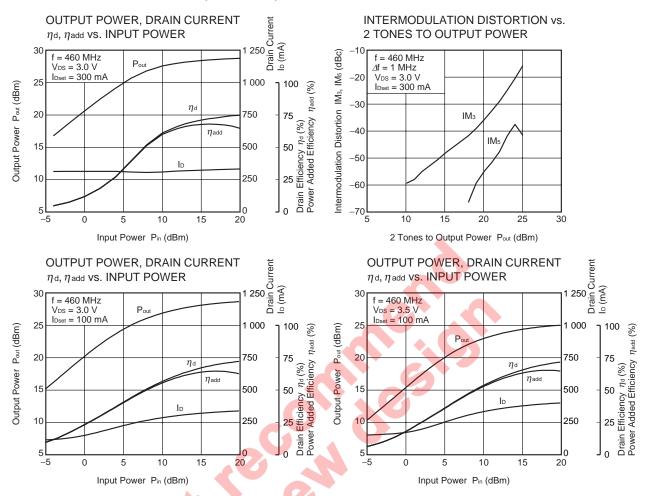
Parameter	Symbol	Test Conditions	MIN.	TYP.	MAX.	Unit
Gate to Source Leak Current	lgss	Vgs = 5.0 V	_	-	100	nA
Drain to Source Leakage Current (Zero Gate Voltage Drain Current)	loss	V _{DS} = 8.0 V	ı	ı	100	nA
Gate Threshold Voltage	Vth	V _{DS} = 3.5 V, I _D = 1 mA	1.0	1.4	1.9	V
Thermal Resistance	Rth	Channel to Case	-	-	10	°C/W
Transconductance	Gm	V _{DS} = 3.0 V, I _D = 300 mA	-	0.6	-	S
Drain to Source Breakdown Voltage	BVDSS	$loss = 10 \mu A$	15	18	-	٧
Output Power	Pout	f = 460 MHz, V _{DS} = 3.0 V,	26.0	28.0	-	dBm
Drain Current	ΙD	P _{in} = 15 dBm,	_	320	_	mA
Power Added Efficiency	η add	I _{Dset} = 300 mA (RF OFF), Note1	55	60	-	%
Linear Gain Note2	GL		ı	20	-	dB

Note 1. DC performance is 100% testing. RF performance is testing several samples per wafer. Wafer rejection criteria for standard devices is 1 reject for several samples.

2. Pin = 5 dBm



TYPICAL CHARACTERISTICS (TA = +25°C)



Remark The graphs indicate nominal characteristics.

S-PARAMETERS

S-parameters/Noise parameters are provided on the NEC Compound Semiconductor Devices Web site in a form (S2P) that enables direct import to a microwave circuit simulator without keyboard input.

Click here to download S-parameters.

[RF and Microwave] \rightarrow [Device Parameters]

URL http://www.csd-nec.com/

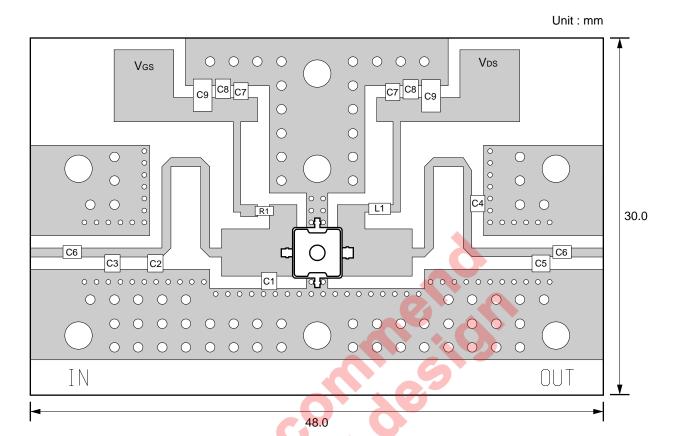
LARGE SIGNAL IMPEDANCE (VDS = 3.0 V, ID = 300 mA, f = 460 MHz)

f (MHz)	$Z_{in}\left(\Omega\right)$	Z OL (Ω) Note		
460	7.47 +j18.24	4.82 +j5.04		

Note ZoL is the conjugate of optimum load impedance at given voltage, idling current, input power and frequency.



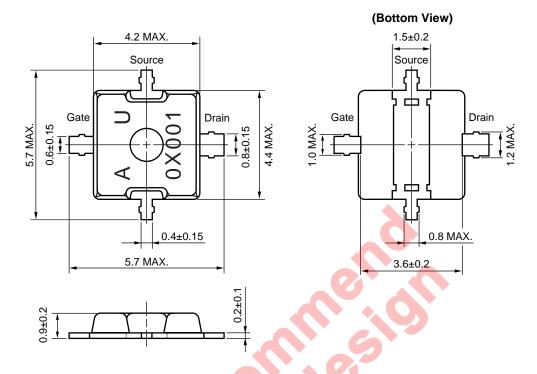
★ EVALUATION BOARD FOR 460 MHz



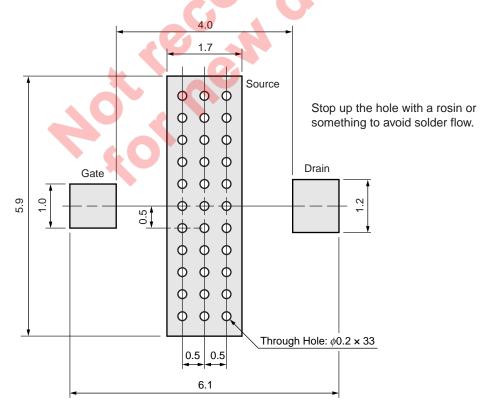
Symbol	Value	Comment
C1	9.1 pF	
C2	12 pF	
C3	20 pF	
C4	3.3 pF	
C5	13 pF	
C6	22 pF	
C7	1 000 pF	
C8	0.33 μF	
C9	3.3 μ F - 16V	
R1	1 000 Ω	
L1	22 nH	_
Circuit Board	$t = 0.4$ mm, ε $r = 4.5$	R4775

★ PACKAGE DIMENSIONS

79A (UNIT: mm)



79A PACKAGE RECOMMENDED P.C.B. LAYOUT (UNIT: mm)





RECOMMENDED SOLDERING CONDITIONS

This product should be soldered and mounted under the following recommended conditions. For soldering methods and conditions other than those recommended below, contact your nearby sales office.

Soldering Method	Soldering Conditions	Condition Symbol	
Infrared Reflow	Peak temperature (package surface temperature) Time at peak temperature Time at temperature of 220°C or higher Preheating time at 120 to 180°C Maximum number of reflow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 60 seconds or less : 120±30 seconds : 3 times : 0.2%(Wt.) or below	IR260
VPS	Peak temperature (package surface temperature) Time at temperature of 200°C or higher Preheating time at 120 to 150°C Maximum number of reflow processes Maximum chlorine content of rosin flux (% mass)	: 215°C or below : 25 to 40 seconds : 30 to 60 seconds : 3 times : 0.2%(Wt.) or below	VP215
Wave Soldering	Peak temperature (molten solder temperature) Time at peak temperature Preheating temperature (package surface temperature) Maximum number of flow processes Maximum chlorine content of rosin flux (% mass)	: 260°C or below : 10 seconds or less : 120°C or below : 1 time : 0.2%(Wt.) or below	WS260
Partial Heating	Peak temperature (pin temperature) Soldering time (per pin of device) Maximum chlorine content of rosin flux (% mass)	: 350°C or below : 3 seconds or less : 0.2%(Wt.) or below	HS350-P3

Caution Do not use different soldering methods together (except for partial heating).

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M8E 00.4-0110



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UF28100M MW6S010GNR1 MW6S010GNR1 DU2820S SD2943W SD2932BW SD2941-10W MRF24301HR5 ARF469AG
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AFT09MP055NR1 DU2860U MHT1803A D2081UK.F