# R1LP0408D Series

## 4Mb Advanced LPSRAM (512-kword × 8-bit)

R10DS0274EJ0200
Rev.2.00
2019.10.29

## Description

The R1LP0408D Series is a family of 4-Mbit static RAMs organized 512-kword × 8-bit, fabricated by Renesas's high-performance CMOS and TFT technologies. The R1LP0408D Series has realized higher density, higher performance and low power consumption. The R1LP0408D Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 32-pin SOP and 32-pin TSOP.

## Features

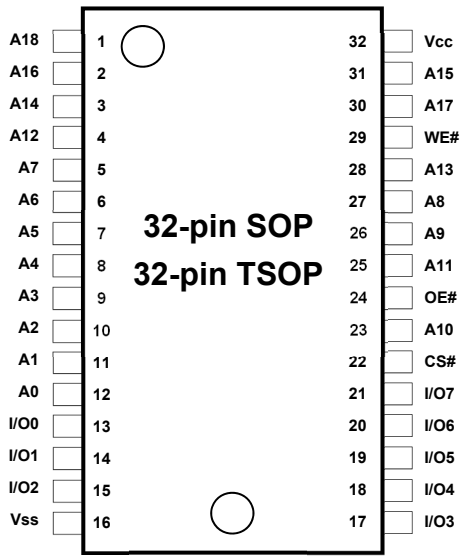
- Single 5V supply: 4.5V to 5.5V
- Access time: 55ns (max.)
- Power dissipation:
  — Standby: 4µW (typ.)
- Equal access and cycle times
- Common data input and output
  — Three state output
- Directly TTL compatible
  — All inputs and outputs
- Battery backup operation

## Ordering Information

| Orderable part name | Access time | Temperature range | Package | Shipping container |
|---|---|---|---|---|
| R1LP0408DSP-5SI#B* | 55 ns | -40 ~ +85°C | 525-mil 32-pin plastic SOP | Tube (Magazine) |
| R1LP0408DSP-5SI#S* | | | | Embossed tape |
| R1LP0408DSB-5SI#B* | | | 400-mil 32-pin plastic TSOP (II) | Tray |
| R1LP0408DSB-5SI#S* | | | | Embossed tape |

Note 1. * = Revision code for Assembly site change, etc. (* = 0, 1, etc.)

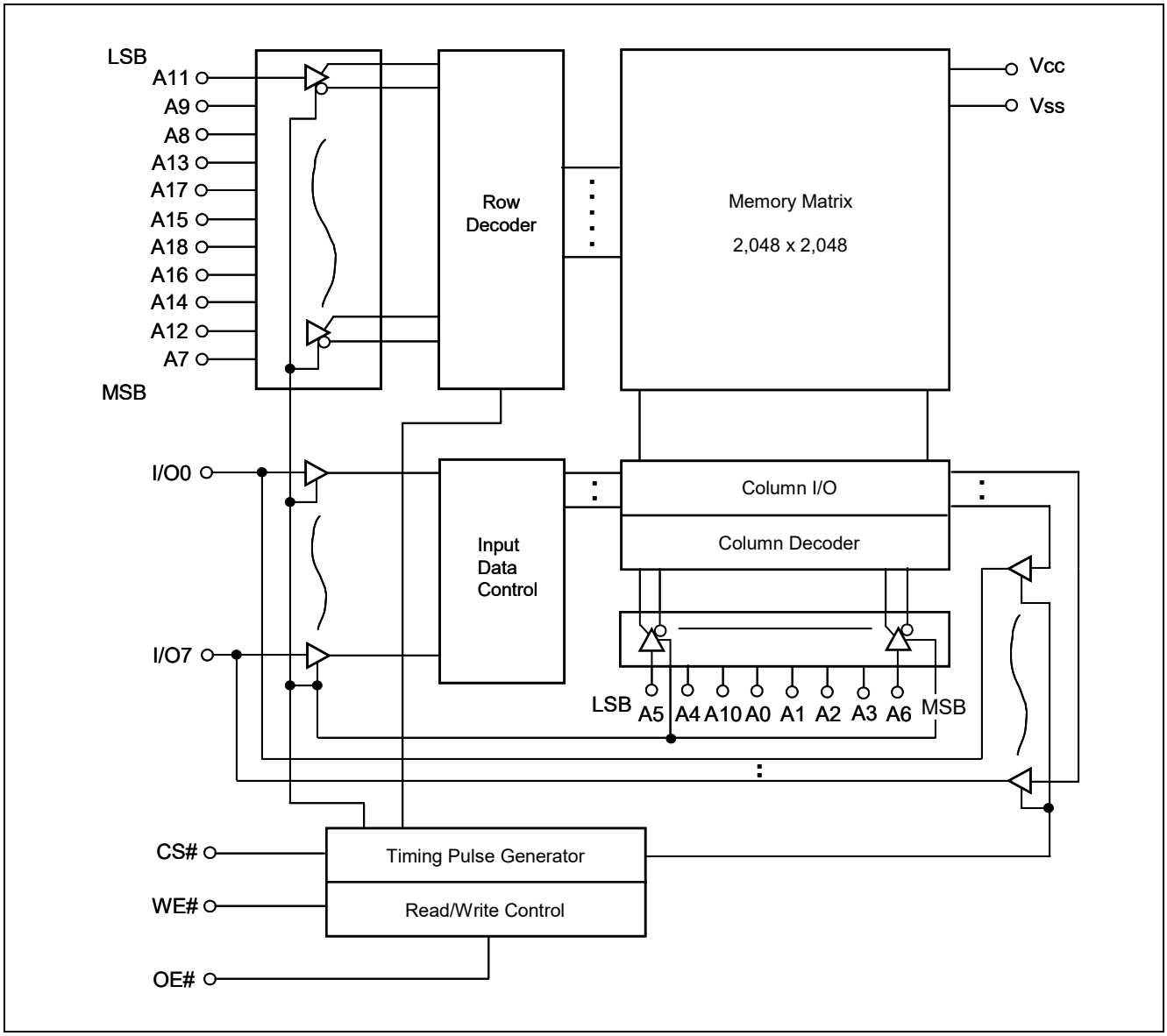
## Pin Arrangement




## Pin Description

| Pin name | Function |
|---|---|
| Vcc | Power supply |
| Vss | Ground |
| A0 to A18 | Address input |
| I/O0 to I/O7 | Data input/output |
| CS# | Chip select |
| WE# | Write enable |
| OE# | Output enable |

## Block Diagram



## Operation Table

| WE# | CS# | OE# | Mode | Vcc current | I/O0 to I/O7 | Ref. cycle |
|---|---|---|---|---|---|---|
| × | H | × | Not selected | $I_{SB}$, $I_{SB1}$ | High-Z | — |
| H | L | H | Output disable | Icc | High-Z | — |
| H | L | L | Read | Icc | Dout | Read cycle |
| L | L | H | Write | Icc | Din | Write cycle (1) |
| L | L | L | Write | Icc | Din | Write cycle (2) |

Note 1. H: $V_{IH}$ L:$V_{IL}$ ×: $V_{IH}$ or $V_{IL}$

## Absolute Maximum Ratings

| Parameter | Symbol | Value | unit |
|---|---|---|---|
| Power supply voltage relative to Vss | Vcc | -0.5 to +7.0 | V |
| Terminal voltage on any pin relative to Vss | $V_T$ | -0.5[*1] to Vcc+0.3[*2] | V |
| Power dissipation | $P_T$ | 0.7 | W |
| Operation temperature | Topr | -40 to +85 | °C |
| Storage temperature range | Tstg | -65 to 150 | °C |
| Storage temperature range under bias | Tbias | -40 to +85 | °C |

Note 1. -3.0V for pulse ≤ 30ns (full width at half maximum)
2. Maximum voltage is +7.0V.

## DC Operating Conditions

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Note |
|---|---|---|---|---|---|---|
| Supply voltage | Vcc | 4.5 | 5.0 | 5.5 | V | |
| | Vss | 0 | 0 | 0 | V | |
| Input high voltage | $V_{IH}$ | 2.2 | — | Vcc+0.3 | V | |
| Input low voltage | $V_{IL}$ | -0.3 | — | 0.8 | V | 1 |
| Ambient temperature range | Ta | -40 | — | +85 | °C | |

Note 1. -3.0V for pulse ≤ 30ns (full width at half maximum)

## DC Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test conditions |
|---|---|---|---|---|---|---|
| Input leakage current | $\lvert I_{LI} \rvert$ | — | — | 1 | µA | Vin = Vss to Vcc |
| Output leakage current | $\lvert I_{LO} \rvert$ | — | — | 1 | µA | CS# =$V_{IH}$ or OE# =$V_{IH}$, VI/O =Vss to Vcc |
| Operating current | Icc | — | 5*1 | 10 | mA | CS# =$V_{IL}$, Others = $V_{IH}$/$V_{IL}$, II/O = 0mA |
| Average operating current | $I_{CC1}$ | — | 15*1 | 25 | mA | Min. cycle, duty =100%, II/O = 0mA, CS# =$V_{IL}$, Others = $V_{IH}$/$V_{IL}$ |
| | $I_{CC2}$ | — | 3*1 | 5 | mA | Cycle =1µs, duty =100%, II/O = 0mA, CS# ≤ 0.2V, $V_{IH}$ ≥ Vcc-0.2V, $V_{IL}$ ≤ 0.2V |
| Standby current | $I_{SB}$ | — | 0.1*1 | 0.5 | mA | CS# =$V_{IH}$, Others = Vss to Vcc |
| Standby current | $I_{SB1}$ | — | 0.8*1 | 2.5 | µA | ~+25°C; Vin = Vss to Vcc, CS# ≥ Vcc-0.2V |
| | | — | 1*2 | 3 | µA | ~+40°C |
| | | — | — | 8 | µA | ~+70°C |
| | | — | — | 10 | µA | ~+85°C |
| Output high voltage | $V_{OH}$ | 2.4 | — | — | V | $I_{OH}$ = -1mA |
| | $V_{OH2}$ | Vcc-0.5 | — | — | V | $I_{OH}$ = -0.1mA |
| Output low voltage | $V_{OL}$ | — | — | 0.4 | V | $I_{OL}$ = 2.1mA |

Note 1. Typical parameter indicates the value for the center of distribution at 5.0V (Ta=25ºC), and not 100% tested.
2. Typical parameter indicates the value for the center of distribution at 5.0V (Ta=40ºC), and not 100% tested.

## Capacitance

(Vcc = 4.5V ~ 5.5V, f = 1MHz, Ta = -40 ~ +85°C)

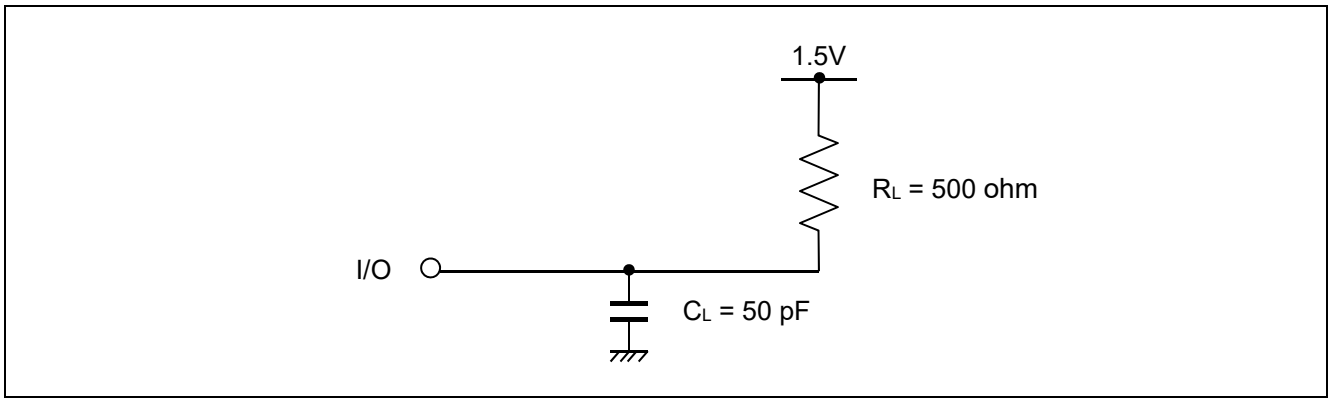
| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test conditions | Note |
|---|---|---|---|---|---|---|---|
| Input capacitance | C in | — | — | 8 | pF | Vin =0V | 1 |
| Input / output capacitance | $C_{I/O}$ | — | — | 10 | pF | VI/O =0V | 1 |

Note 1. This parameter is sampled and not 100% tested.

## AC Characteristics

Test Conditions (Vcc = 4.5V ~ 5.5V, Ta = -40 ~ +85°C)

- Input pulse levels: VIL = 0.4V, VIH = 2.4V
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.5V
- Output load: See figures (Including scope and jig)



### Read Cycle

| Parameter | Symbol | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Read cycle time | $t_{RC}$ | 55 | — | ns | |
| Address access time | $t_{AA}$ | — | 55 | ns | |
| Chip select access time | $t_{ACS}$ | — | 55 | ns | |
| Output enable to output valid | $t_{OE}$ | — | 25 | ns | |
| Chip select to output in low-Z | $t_{CLZ}$ | 10 | — | ns | 2 |
| Output enable to output in low-Z | $t_{OLZ}$ | 5 | — | ns | 2 |
| Chip deselect to output in high-Z | $t_{CHZ}$ | 0 | 20 | ns | 1,2 |
| Output disable to output in high-Z | $t_{OHZ}$ | 0 | 20 | ns | 1,2 |
| Output hold from address change | $t_{OH}$ | 10 | — | ns | |

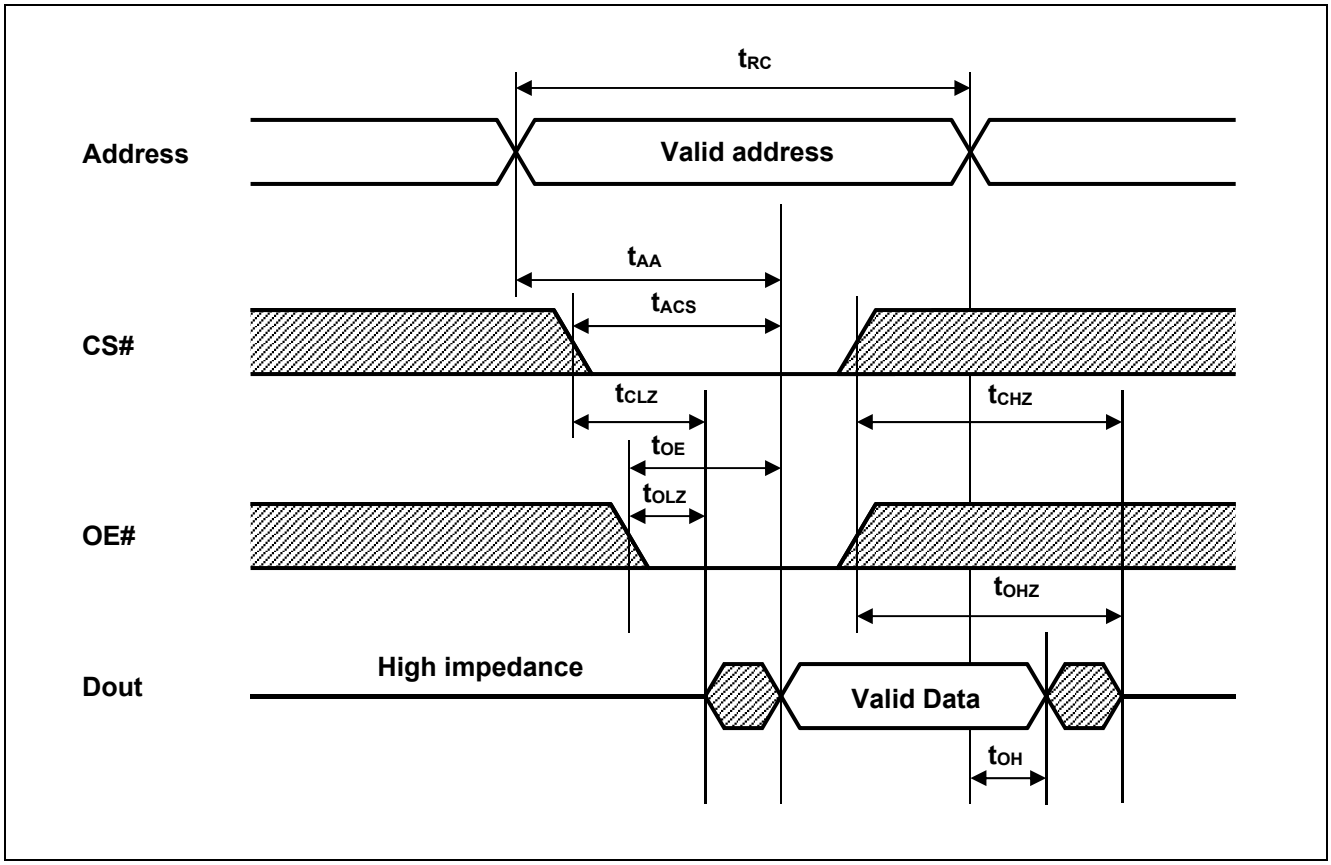
### Write Cycle

| Parameter | Symbol | Min. | Max. | Unit | Note |
|---|---|---|---|---|---|
| Write cycle time | $t_{WC}$ | 55 | — | ns | |
| Chip select to end of write | $t_{CW}$ | 50 | — | ns | 4 |
| Address setup time | $t_{AS}$ | 0 | — | ns | 5 |
| Address valid to end of write | $t_{AW}$ | 50 | — | ns | |
| Write pulse width | $t_{WP}$ | 40 | — | ns | 3,12 |
| Write recovery time | $t_{WR}$ | 0 | — | ns | 6 |
| Write to output in high-Z | $t_{WHZ}$ | 0 | 20 | ns | 1,2,7 |
| Data to write time overlap | $t_{DW}$ | 25 | — | ns | |
| Data hold from write time | $t_{DH}$ | 0 | — | ns | |
| Output enable from end of write | $t_{OW}$ | 5 | — | ns | 2 |
| Output disable to output in high-Z | $t_{OHZ}$ | 0 | 20 | ns | 1,2,7 |

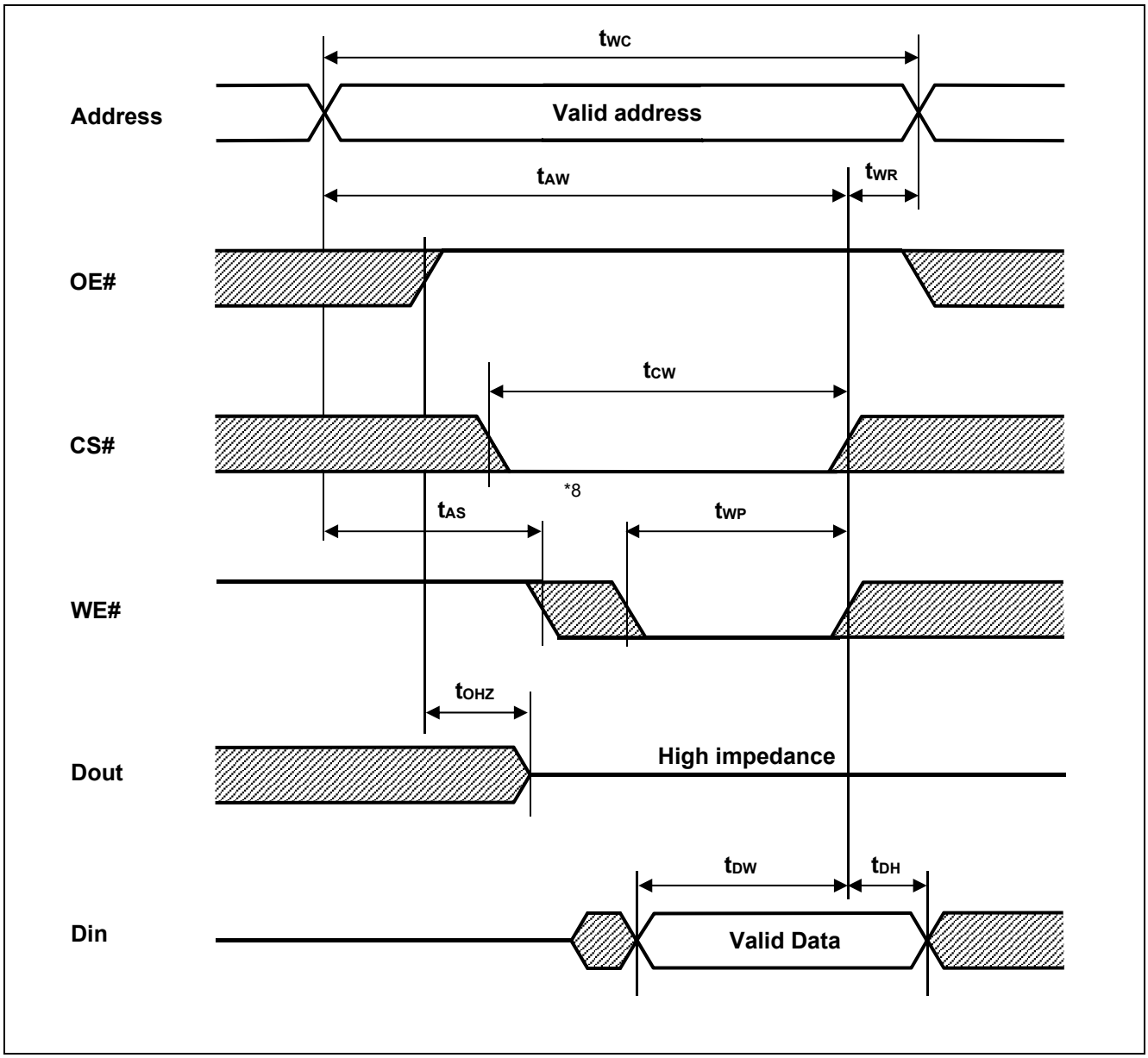
Note
1. $t_{CHZ}$, $t_{OHZ}$ and $t_{WHZ}$ are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.
2. This parameter is sampled and not 100% tested.
3. A write occurs during the overlap ($t_{WP}$) of a low CS# and a low WE#.
   A write begins at the later transition of CS# going low or WE# going low.
   A write ends at the earlier transition of CS# going high or WE# going high.
   $t_{WP}$ is measured from the beginning of write to the end of write.
4. $t_{CW}$ is measured from CS# going low to end of write.
5. $t_{AS}$ is measured the address valid to the beginning of write.
6. $t_{WR}$ is measured from the earlier of WE# or CS# going high to the end of write cycle.
7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
8. If the CS# low transition occurs simultaneously with the WE# low transition or after the WE# transition, the output remain in a high impedance state.
9. Dout is the same phase of the write data of this write cycle.
10. Dout is the read data of next address.
11. If CS# is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
12. In the write cycle with OE# low fixed, $t_{WP}$ must satisfy the following equation to avoid a problem of data bus contention.
    $t_{WP} \geq t_{DW}$ min + $t_{WHZ}$ max

## Timing Waveforms

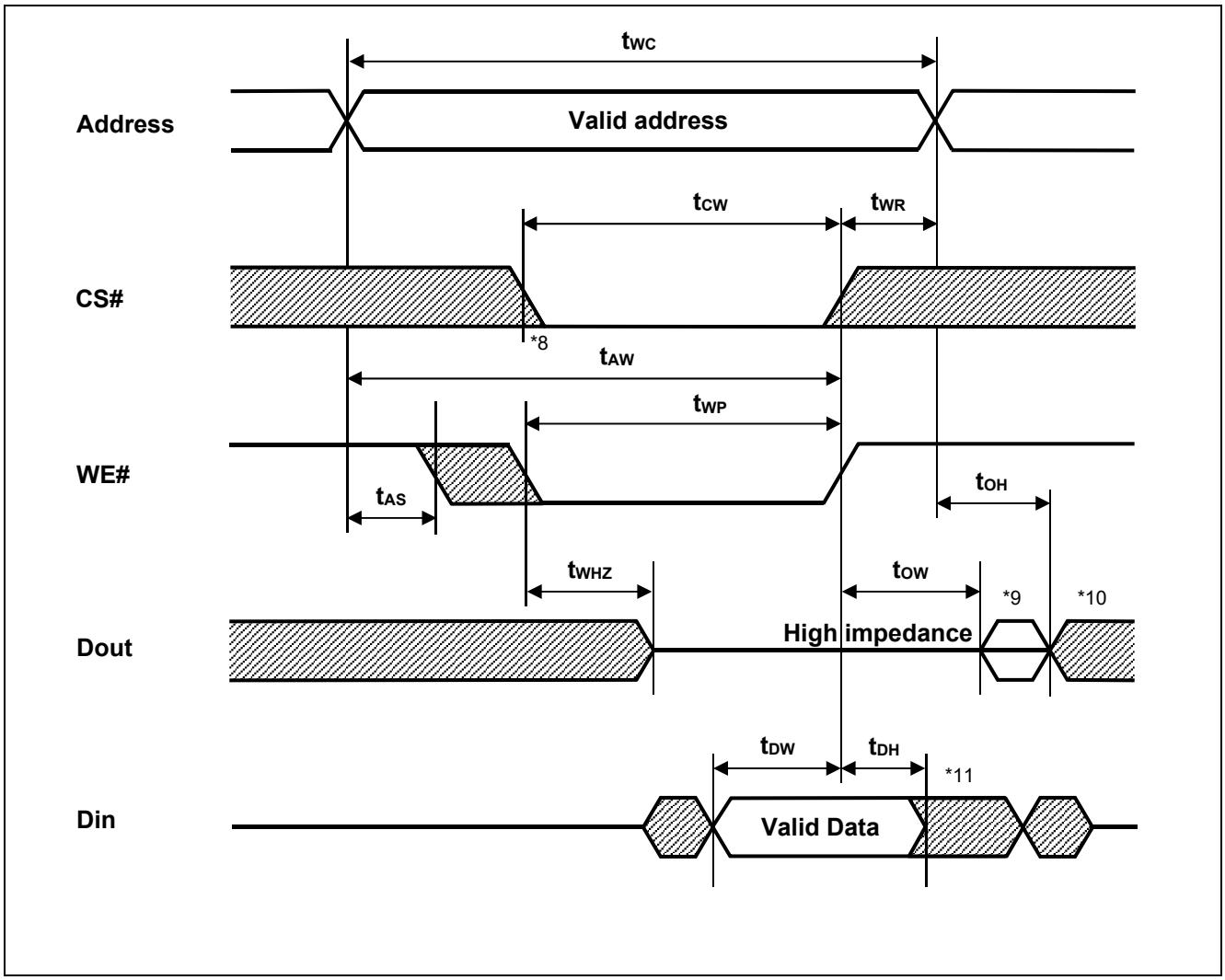
### Read Cycle (WE# = $V_{IH}$ )



**Write Cycle (1) (OE# CLOCK)**



**Write Cycle (2) (OE# Low Fixed)**



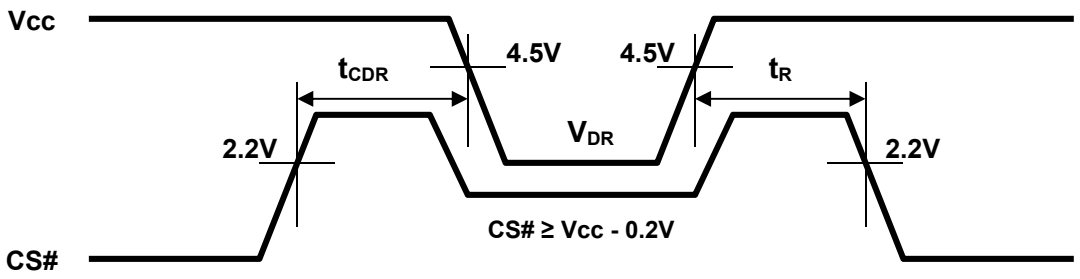
## Low Vcc Data Retention Characteristics

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Test conditions[*3] | |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ for data retention | $V_{DR}$ | 2.0 | — | 5.5 | V | Vin ≥ 0V, CS# ≥ Vcc-0.2V | |
| Data retention current | $I_{CCDR}$ | — | 0.8[*1] | 2.5 | µA | ~+25°C | Vcc=3.0V, Vin ≥ 0V, CS# ≥ Vcc-0.2V |
| | | — | 1[*2] | 3 | µA | ~+40°C | |
| | | — | — | 8 | µA | ~+70°C | |
| | | — | — | 10 | µA | ~+85°C | |
| Chip deselect time to data retention | $t_{CDR}$ | 0 | — | — | ns | See retention waveform. | |
| Operation recovery time | $t_R$ | 5 | — | — | ms | | |

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=25ºC), and not 100% tested.
2. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=40ºC), and not 100% tested.
3. CS# controls address buffer, WE# buffer, OE# buffer and Din buffer. If data retention mode, Vin levels (address, WE#, OE#, I/O) can be in the high impedance state.

### Low Vcc Data Retention Timing Waveforms

**CS# Controlled**



| Revision History | R1LP0408D Series Data Sheet |
|---|---|

| Rev. | Date | Description | |
|---|---|---|---|
| | | Page | Summary |
| 1.00 | 2017.1.27 | — | First Edition issued |
| 2.00 | 2019.10.29 | p.1 | Revised orderable part name information. |
| | | | |
| | | | |

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)


### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/


### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

# X-ON Electronics

Largest Supplier of Electrical and Electronic Components

***Click to view similar products for*** SRAM ***category:***

***Click to view products by*** Renesas ***manufacturer:***

Other Similar products are found below :

CY6116A-35DMB CY7C1049GN-10VXI CY7C1461KV33-133AXI GS8161Z36DD-200I GS88237CB-200I RMLV0408EGSB-4S2#AA0 IS64WV3216BLL-15CTLA3 IS66WVE4M16ECLL-70BLI PCF8570P K6F2008V2E-LF70000 K6T4008C1B-GB70 CY7C1353S-100AXC AS6C8016-55BIN AS7C164A-15PCN 515712X IS62WV51216EBLL-45BLI IS63WV1288DBLL-10HLI IS66WVE2M16ECLL-70BLI IS66WVE4M16EALL-70BLI IS61WV102416DBLL-10TLI CY7C1381KV33-100AXC CY7C1460KV25-200BZI CY7C1373KV33-100AXC CY7C1381KVE33-133AXI CY7C4121KV13-600FCXC GS882Z18CD-150I IS66WVC2M16ECLL-7010BLI 7140LA35PDG CY7C1380KV33-250AXC AS6C8016-55BINTR CY7C1370KV33-250AXC CY7C1370KVE33-167AXI 7140LA100PDG AS7C34096B-10TIN AS6C8016-55TIN IS62WV25616EALL-55TLI GS8128418B-167IV CY7C1460KV25-200BZXI CY7C1460KV25-167BZXI CY7C1315KV18-333BZXC CY7C1370KV25-200AXC 71421LA55JI8 CY62158G30-45ZSXI CY62157G30-45ZSXI RMLV3216AGSD-5S2#AA0 CY62187G30-55BAXI CY62157G30-45ZXI IS61VVPS102436B-200B3LI IS66WVC2M16EALL-7010BLI IS66WVE4M16EALL-70BLI-TR