RENESAS

R1LP0408D Series

4Mb Advanced LPSRAM (512-kword × 8-bit)

R10DS0274EJ0100 Rev.1.00 2017.1.27

Description

The R1LP0408D Series is a family of 4-Mbit static RAMs organized 512-kword × 8-bit, fabricated by Renesas's high-performance CMOS and TFT technologies. The R1LP0408D Series has realized higher density, higher performance and low power consumption. The R1LP0408D Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 32-pin SOP and 32-pin TSOP.

Features

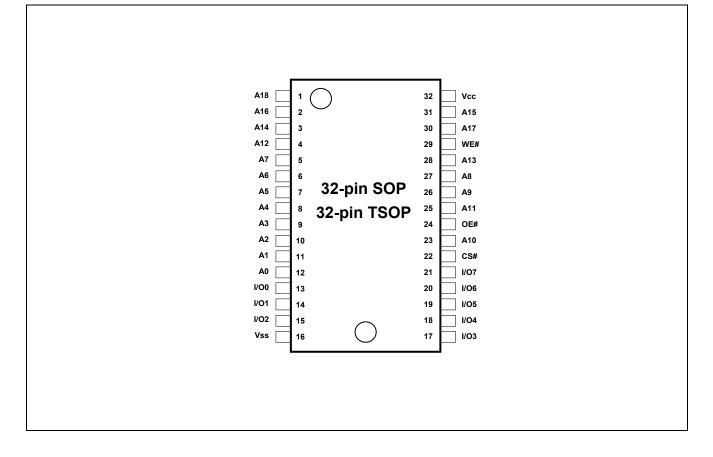
- Single 5V supply: 4.5V to 5.5V
- Access time: 55ns (max.)
- Power dissipation:
 Standby: 4µW (typ.)
- Equal access and cycle times
- Common data input and output — Three state output
- Directly TTL compatible — All inputs and outputs
- Battery backup operation

Ordering Information

Orderable part name	Access time	Temperature range	Package	Shipping container
R1LP0408DSP-5SI#B0			525-mil 32-pin	Tube (Magazine)
R1LP0408DSP-5SI#S0	FF ma	40	plastic SOP	Embossed tape
R1LP0408DSB-5SI#B1	55 ns	-40 ~ +85°C	400-mil 32-pin	Tray
R1LP0408DSB-5SI#S1			plastic TSOP (II)	Embossed tape



Pin Arrangement

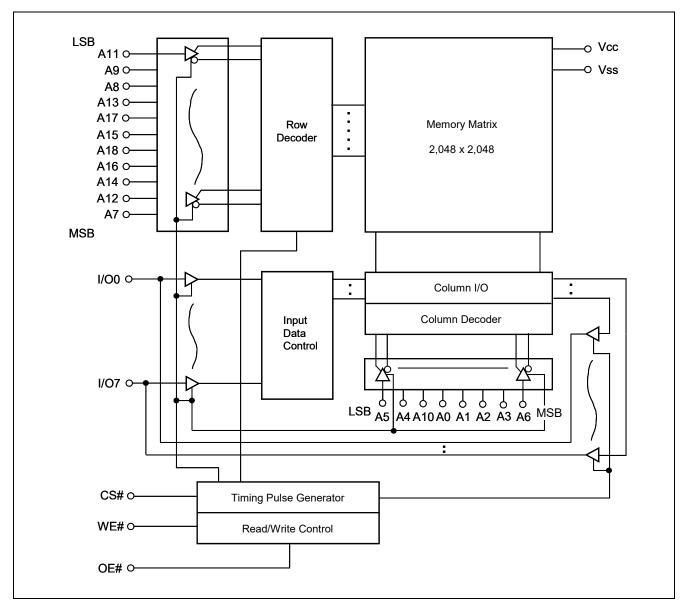


Pin Description

Pin name	Function	
Vcc	Power supply	
Vss	Ground	
A0 to A18	Address input	
I/O0 to I/O7	Data input/output	
CS#	Chip select	
WE#	Write enable	
OE#	Output enable	



Block Diagram





Operation Table

WE#	CS#	OE#	Mode	Vcc current	I/O0 to I/O7	Ref. cycle
×	Н	×	Not selected	I _{SB} , I _{SB1}	High-Z	—
Н	L	Н	Output disable	lcc	High-Z	—
Н	L	L	Read	lcc	Dout	Read cycle
L	L	Н	Write	lcc	Din	Write cycle (1)
L	L	L	Write	lcc	Din	Write cycle (2)

Note 1. H: V_{IH} L:V_{IL} ×: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to Vss	Vcc	-0.5 to +7.0	V
Terminal voltage on any pin relative to Vss	VT	-0.5 ^{*1} to Vcc+0.3 ^{*2}	V
Power dissipation	PT	0.7	W
Operation temperature	Topr	-40 to +85	°C
Storage temperature range	Tstg	-65 to 150	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Note 1. -3.0V for pulse \leq 30ns (full width at half maximum)

2. Maximum voltage is +7.0V.



DC Operating Conditions

Parameter	Symbol	Min.	Тур.	Max.	Unit	Note
Supply voltage	Vcc	4.5	5.0	5.5	V	
	Vss	0	0	0	V	
Input high voltage	VIH	2.2	_	Vcc+0.3	V	
Input low voltage	VIL	-0.3	_	0.8	V	1
Ambient temperature range	Та	-40	_	+85	°C	

Note 1. -3.0V for pulse \leq 30ns (full width at half maximum)

DC Characteristics

Parameter	Symbol	Min.	Тур.	Max.	Unit		Test conditions	
Input leakage current	u	_	-	1	μA	Vin = Vss	s to Vcc	
Output leakage current	Ilo	_	_	1	μA	CS# =V _{IH} or OE# =V _{IH} , VI/O =Vss to Vcc		
Operating current	lcc	_	5 ^{*1}	10	mA	CS# =V _{IL} , Others = V _{IH} /V _{IL} , II/O = 0mA		
Average operating current	Icc1	_	15 ^{*1}	25	mA	Min. cycle, duty =100%, II/O = 0m CS# =V _{IL} , Others = V_{IH}/V_{IL}		
	Icc2	_	3 ^{*1}	5	mA	Cycle =1µs, duty =100%, II/O = 0 CS# ≤ 0.2V, VIH ≥ Vcc-0.2V, VIL ≤ 0.2V		
Standby current	Isb	_	0.1 ^{*1}	0.5	mA	CS# =V _{IH} , Others = Vss to Vcc		
Standby current		_	0.8 ^{*1}	2.5	μA	~+25°C		
		_	1 ^{*2}	3	μA	~+40°C	Vin = Vss to Vcc,	
	I _{SB1}	_	_	8	μΑ	~+70°C	CS# ≥ Vcc-0.2V	
		_	_	10	μA	~+85°C		
Output high voltage	V _{OH}	2.4	—	—	V	I _{он} = -1m	A	
	Vон2	Vcc-0.5	—	—	V	I _{OH} = -0.1mA		
Output low voltage	Vol	—	—	0.4	V	$I_{OL} = 2.1 \text{mA}$		

Note 1. Typical parameter indicates the value for the center of distribution at 5.0V (Ta=25°C), and not 100% tested.
 2. Typical parameter indicates the value for the center of distribution at 5.0V (Ta=40°C), and not 100% tested.

Capacitance

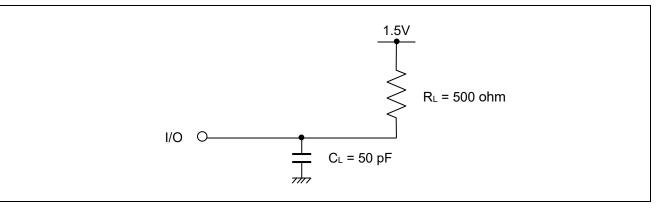
			(Vcc = 4)	4.5V ~ t	5.5V, f =	= 1MHz, Ta = -40) ~ +85°C)
Parameter	Symbol	Min.	Тур.	Max.	Unit	Test conditions	Note
Input capacitance	C in	I	—	8	pF	Vin =0V	1
Input / output capacitance	C 1/O	_	_	10	pF	VI/O =0V	1

Note 1. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (Vcc = $4.5V \sim 5.5V$, Ta = $-40 \sim +85^{\circ}C$)

- Input pulse levels: VIL = 0.4V, VIH = 2.4V
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.5V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Read cycle time	t _{RC}	55	-	ns	
Address access time	t _{AA}	I	55	ns	
Chip select access time	t _{ACS}	I	55	ns	
Output enable to output valid	toe	-	25	ns	
Chip select to output in low-Z	t _{CLZ}	10	_	ns	2
Output enable to output in low-Z	tolz	5	_	ns	2
Chip deselect to output in high-Z	t _{снz}	0	20	ns	1,2
Output disable to output in high-Z	tонz	0	20	ns	1,2
Output hold from address change	t _{он}	10	_	ns	

Write Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Write cycle time	t _{WC}	55	_	ns	
Chip select to end of write	t _{CW}	50	_	ns	4
Address setup time	t _{AS}	0	_	ns	5
Address valid to end of write	t _{AW}	50	_	ns	
Write pulse width	twp	40	_	ns	3,12
Write recovery time	t _{wR}	0	_	ns	6
Write to output in high-Z	t _{wнz}	0	20	ns	1,2,7
Data to write time overlap	t _{DW}	25	_	ns	
Data hold from write time	t _{DH}	0	_	ns	
Output enable from end of write	tow	5	_	ns	2
Output disable to output in high-Z	tонz	0	20	ns	1,2,7

Note 1. t_{CHZ}, t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

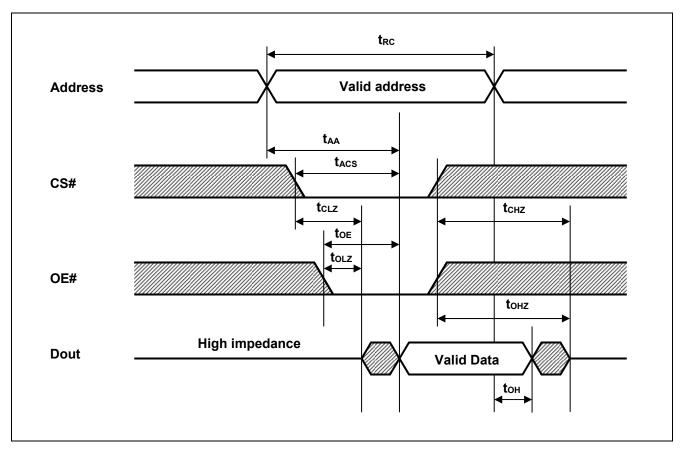
- 2. This parameter is sampled and not 100% tested.
- A write occurs during the overlap (twp) of a low CS# and a low WE#.
 A write begins at the later transition of CS# going low or WE# going low.
 A write ends at the earlier transition of CS# going high or WE# going high.
 twp is measured from the beginning of write to the end of write.
- 4. t_{CW} is measured from CS# going low to end of write.
- 5. t_{AS} is measured the address valid to the beginning of write.
- 6. t_{WR} is measured from the earlier of WE# or CS# going high to the end of write cycle.
- 7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.
- 8. If the CS# low transition occurs simultaneously with the WE# low transition or after the WE# transition, the output remain in a high impedance state.
- 9. Dout is the same phase of the write data of this write cycle.
- 10. Dout is the read data of next address.
- 11. If CS# is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.
- 12. In the write cycle with OE# low fixed, twp must satisfy the following equation to avoid a problem of data bus contention.

 $t_{WP} \ge t_{DW} \min + t_{WHZ} \max$



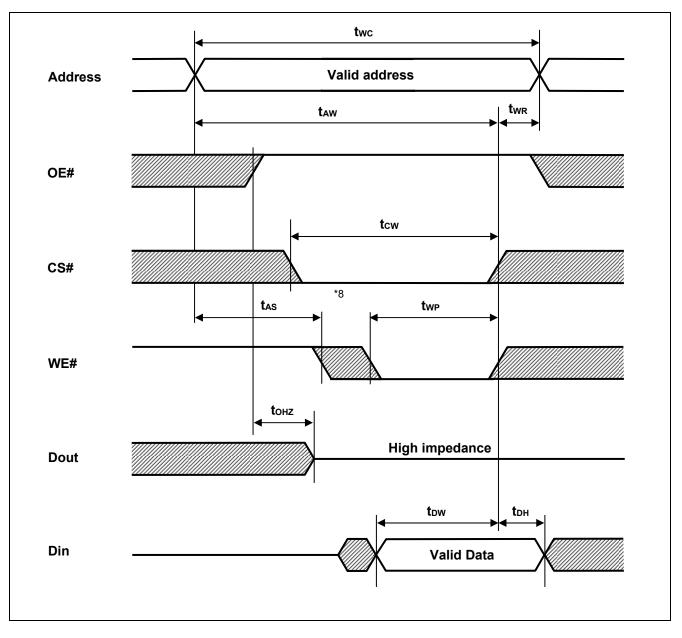
Timing Waveforms

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Read Cycle (WE# = VIH )
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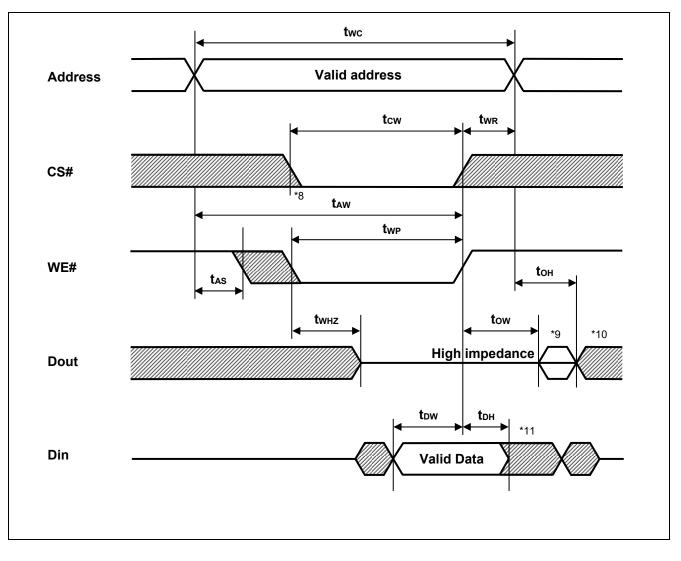


Write Cycle (1) (OE# CLOCK)





Write Cycle (2) (OE# Low Fixed)





Low Vcc Data Retention Characteristics	Low Vcc	Data Rete	ention Cha	racteristics
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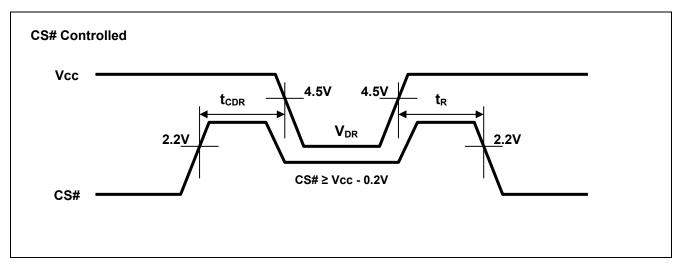
Parameter	Symbol	Min.	Тур.	Max.	Unit		Test conditions ^{*3}
V _{CC} for data retention	V _{DR}	2.0	_	5.5	V	Vin ≥ 0V, CS# ≥ Vco	c-0.2V
Data retention current		_	0.8 ^{*1}	2.5	μA	~+25°C	
		-	1 ^{*2}	3	μA	~+40°C	Vcc=3.0V, Vin ≥ 0V,
	ICCDR	_	_	8	μA	~+70°C	CS# ≥ Vcc-0.2V
		_	_	10	μA	~+85°C	
Chip deselect time to data retention	t _{CDR}	0	_	_	ns	See roton	tion waveform
Operation recovery time	t _R	5	_	_	ms	See retention waveform.	

Note 1. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=25°C), and not 100% tested.

2. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=40°C), and not 100% tested.

3. CS# controls address buffer, WE# buffer, OE# buffer and Din buffer. If data retention mode, Vin levels (address, WE#, OE#, I/O) can be in the high impedance state.







Revision History	R1LP0408D Series Data Sheet
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		Description	
Rev.	Date	Page	Summary
1.00	2017.1.27	-	First Edition issued

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