

True Low Power Platform (as low as 66 μ A/MHz, and 0.60 μ A for RTC + LVD), 1.6 V to 5.5 V operation, 16 to 512 Kbyte Flash, 44 DMIPS at 32 MHz, for General Purpose Applications

1. OUTLINE

1.1 Features

Ultra-Low Power Consumption Technology

- V_{DD} = single power supply voltage of 1.6 to 5.5 V which can operate a 1.8 V device at a low voltage
- HALT mode
- STOP mode
- SNOOZE mode

RL78 CPU Core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time: Can be changed from high speed (0.03125 μ s: @ 32 MHz operation with high-speed on-chip oscillator) to ultra-low speed (30.5 μ s: @ 32.768 kHz operation with subsystem clock)
- Multiply/divide/multiply & accumulate instructions are supported.
- Address space: 1 MB
- General-purpose registers: (8-bit register \times 8) \times 4 banks
- On-chip RAM: 2.5 to 48 KB

Code Flash Memory

- Code flash memory: 16 to 512 KB
- Block size: 1 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debug function
- Self-programming (with boot swap function/flash shield window function)

Data Flash Memory

- Data flash memory: 4 KB and 8 KB
- Back ground operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (TYP.)
- Voltage of rewrites: V_{DD} = 1.8 to 5.5 V

High-speed On-chip Oscillator

- Select from 64 MHz, 48 MHz, 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy: $\pm 1.0\%$ (V_{DD} = 1.8 to 5.5 V, T_A = -20 to +85°C)

Operating Ambient Temperature

- T_A = -40 to +85°C (A: Consumer applications, D: Industrial applications)
- T_A = -40 to +105°C (G: Industrial applications)

Power Management and Reset Function

- On-chip power-on-reset (POR) circuit
- On-chip voltage detector (LVD) (Select interrupt and reset from 14 levels)

Data Transfer Controller (DTC)

- Transfer modes: Normal transfer mode, repeat transfer mode, block transfer mode
- Activation sources: Activated by interrupt sources.
- Chain transfer function

Event Link Controller (ELC)

- Event signals of 19 to 26 types can be linked to the specified peripheral function.

Serial Interfaces

- CSI: 3 to 8 channels
- UART/UART (LIN-bus supported): 3 or 4 channels
- I²C/simplified I²C: 3 to 8 channels

Timer

- 16-bit timer: 8 to 12 channels
(Timer Array Unit (TAU): 4 to 8 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)
- 12-bit interval timer: 1 channel
- Real-time clock: 1 channel (calendar for 99 years, alarm function, and clock correction function)
- Watchdog timer: 1 channel (operable with the dedicated low-speed on-chip oscillator)

A/D Converter

- 8/10-bit resolution A/D converter (V_{DD} = 1.6 to 5.5 V)
- Analog input: 8 to 20 channels
- Internal reference voltage (1.45 V) and temperature sensor

D/A Converter

- 8-bit resolution D/A converter (V_{DD} = 1.6 to 5.5 V)
- Analog output: None or up to two channels
- Output voltage: 0 V to V_{DD}
- Real-time output function

Comparator

- None or up to two channels
- Operating modes: Comparator high-speed mode, comparator low-speed mode, window mode
- The external reference voltage or internal reference voltage can be selected as the reference voltage.

I/O Port

- I/O port: 26 to 92 (N-ch open drain I/O [withstand voltage of 6 V]: 2 to 4, N-ch open drain I/O [V_{DD} withstand voltage/EV_{DD} withstand voltage]: 10 to 28)
- Can be set to N-ch open drain, TTL input buffer, and on-chip pull-up resistor
- Different potential interface: Can connect to a 1.8/2.5/3 V device
- On-chip key interrupt function
- On-chip clock output/buzzer output controller

Others

- On-chip BCD (binary-coded decimal) correction circuit

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

○ ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G14			
			30 pins	32 pins	36 pins	40 pins
192 KB	8 KB	20 KB	—	—	—	R5F104EH
128 KB	8 KB	16 KB	R5F104AG	R5F104BG	R5F104CG	R5F104EG
96 KB	8 KB	12 KB	R5F104AF	R5F104BF	R5F104CF	R5F104EF
64 KB	4 KB	5.5 KB Note	R5F104AE	R5F104BE	R5F104CE	R5F104EE
48 KB	4 KB	5.5 KB Note	R5F104AD	R5F104BD	R5F104CD	R5F104ED
32 KB	4 KB	4 KB	R5F104AC	R5F104BC	R5F104CC	R5F104EC
16 KB	4 KB	2.5 KB	R5F104AA	R5F104BA	R5F104CA	R5F104EA

Flash ROM	Data flash	RAM	RL78/G14			
			44 pins	48 pins	52 pins	64 pins
512 KB	8 KB	48 KB Note	—	R5F104GL	—	R5F104LL
384 KB	8 KB	32 KB	—	R5F104GK	—	R5F104LK
256 KB	8 KB	24 KB Note	R5F104FJ	R5F104GJ	R5F104JJ	R5F104LJ
192 KB	8 KB	20 KB	R5F104FH	R5F104GH	R5F104JH	R5F104LH
128 KB	8 KB	16 KB	R5F104FG	R5F104GG	R5F104JG	R5F104LG
96 KB	8 KB	12 KB	R5F104FF	R5F104GF	R5F104JF	R5F104LF
64 KB	4 KB	5.5 KB Note	R5F104FE	R5F104GE	R5F104JE	R5F104LE
48 KB	4 KB	5.5 KB Note	R5F104FD	R5F104GD	R5F104JD	R5F104LD
32 KB	4 KB	4 KB	R5F104FC	R5F104GC	R5F104JC	R5F104LC
16 KB	4 KB	2.5 KB	R5F104FA	R5F104GA	—	—

Flash ROM	Data flash	RAM	RL78/G14	
			80 pins	100 pins
512 KB	8 KB	48 KB Note	R5F104ML	R5F104PL
384 KB	8 KB	32 KB	R5F104MK	R5F104PK
256 KB	8 KB	24 KB Note	R5F104MJ	R5F104PJ
192 KB	8 KB	20 KB	R5F104MH	R5F104PH
128 KB	8 KB	16 KB	R5F104MG	R5F104PG
96 KB	8 KB	12 KB	R5F104MF	R5F104PF

The flash library uses RAM in self-programming and rewriting of the data flash memory.

The target products and start address of the RAM areas used by the flash library are shown below.

R5F104xD (x = A to C, E to G, J, L): Start address FE900H

R5F104xE (x = A to C, E to G, J, L): Start address FE900H

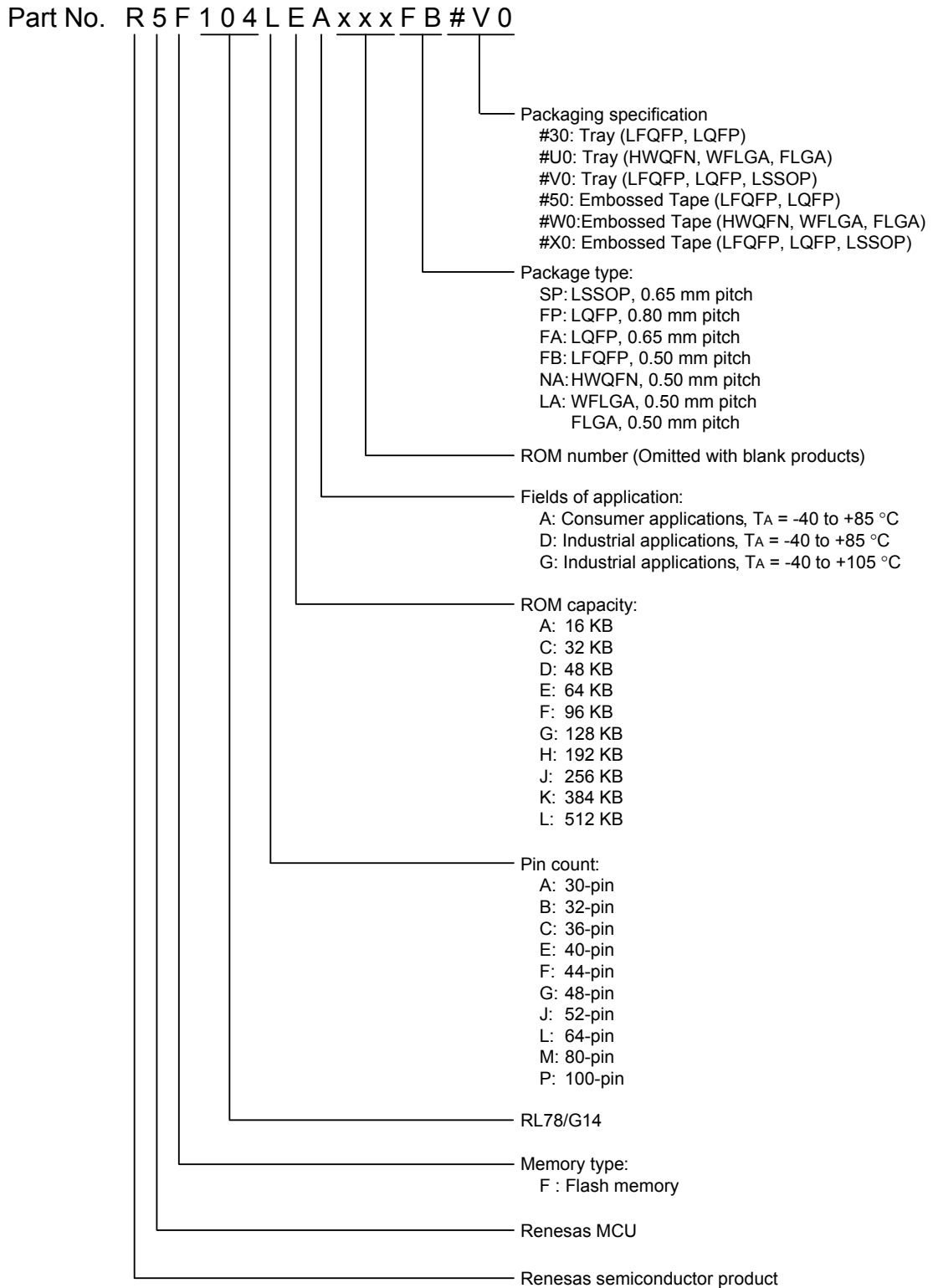
R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H

R5F104xL (x = G, L, M, P): Start address F3F00H

For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

1.2 Ordering Information

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14



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Pin count	Package	Fields of Application Note	Ordering Part Number
30 pins	30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)	A	R5F104AAASP#V0, R5F104ACASP#V0, R5F104ADASP#V0, R5F104AEASP#V0, R5F104AFASP#V0, R5F104AGASP#V0 R5F104AAASP#X0, R5F104ACASP#X0, R5F104ADASP#X0, R5F104AEASP#X0, R5F104AFASP#X0, R5F104AGASP#X0
		D	R5F104AADSP#V0, R5F104ACDSP#V0, R5F104ADDSP#V0, R5F104AEDSP#V0, R5F104AFDSP#V0, R5F104AGDSP#V0 R5F104AADSP#X0, R5F104ACDSP#X0, R5F104ADDSP#X0, R5F104AEDSP#X0, R5F104AFDSP#X0, R5F104AGDSP#X0
		G	R5F104AAGSP#V0, R5F104ACGSP#V0, R5F104ADGSP#V0, R5F104AEGSP#V0, R5F104AFGSP#V0, R5F104AGGSP#V0 R5F104AAGSP#X0, R5F104ACGSP#X0, R5F104ADGSP#X0, R5F104AEGSP#X0, R5F104AFGSP#X0, R5F104AGGSP#X0
32 pins	32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)	A	R5F104BAANA#U0, R5F104BCANA#U0, R5F104BDANA#U0, R5F104BEANA#U0, R5F104BFANA#U0, R5F104BGANA#U0 R5F104BAANA#W0, R5F104BCANA#W0, R5F104BDANA#W0, R5F104BEANA#W0, R5F104BFANA#W0, R5F104BGANA#W0
		D	R5F104BADNA#U0, R5F104BCDNA#U0, R5F104BDDNA#U0, R5F104BEDNA#U0, R5F104BFDNA#U0, R5F104BGDNA#U0 R5F104BADNA#W0, R5F104BCDNA#W0, R5F104BDDNA#W0, R5F104BEDNA#W0, R5F104BFDNA#W0, R5F104BGDNA#W0
		G	R5F104BAGNA#U0, R5F104BCGNA#U0, R5F104BDGNA#U0, R5F104BEGNA#U0, R5F104BFGNA#U0, R5F104BGGNA#U0 R5F104BAGNA#W0, R5F104BCGNA#W0, R5F104BDGNA#W0, R5F104BEGNA#W0, R5F104BFGNA#W0, R5F104BGGNA#W0
	32-pin plastic LQFP (7 × 7, 0.8 mm pitch)	A	R5F104BAAFP#V0, R5F104BCAFP#V0, R5F104BDAFP#V0, R5F104BEAFP#V0, R5F104BFAFP#V0, R5F104BGAFP#V0 R5F104BAAFP#X0, R5F104BCAFP#X0, R5F104BDAFP#X0, R5F104BEAFP#X0, R5F104BFAFP#X0, R5F104BGAFP#X0
		D	R5F104BADFP#V0, R5F104BCDFP#V0, R5F104BDDFP#V0, R5F104BEDFP#V0, R5F104BDFP#V0, R5F104BGDFP#V0 R5F104BADFP#X0, R5F104BCDFP#X0, R5F104BDDFP#X0, R5F104BEDFP#X0, R5F104BDFP#X0, R5F104BGDFP#X0
		G	R5F104BAGFP#V0, R5F104BCGFP#V0, R5F104BDGFP#V0, R5F104BEGFP#V0, R5F104BFGFP#V0, R5F104BGGFP#V0 R5F104BAGFP#X0, R5F104BCGFP#X0, R5F104BDGFP#X0, R5F104BEGFP#X0, R5F104BFGFP#X0, R5F104BGGFP#X0
36 pins	36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)	A	R5F104CAALA#U0, R5F104CCALA#U0, R5F104CDALA#U0, R5F104CEALA#U0, R5F104CFALA#U0, R5F104CGALA#U0 R5F104CAALA#W0, R5F104CCALA#W0, R5F104CDALA#W0, R5F104CEALA#W0, R5F104CFALA#W0, R5F104CGALA#W0
		G	R5F104CAGLA#U0, R5F104CCGLA#U0, R5F104CDGLA#U0, R5F104CEGLA#U0, R5F104CFGLA#U0, R5F104CGGLA#U0 R5F104CAGLA#W0, R5F104CCGLA#W0, R5F104CDGLA#W0, R5F104CEGLA#W0, R5F104CFGLA#W0, R5F104CGGLA#W0

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

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Pin count	Package	Fields of Application Note	Ordering Part Number
40 pins	40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)	A	R5F104EAANA#U0, R5F104ECANA#U0, R5F104EDANA#U0, R5F104EEANA#U0, R5F104EFANA#U0, R5F104EGANA#U0, R5F104EHANA#U0 R5F104EAANA#W0, R5F104ECANA#W0, R5F104EDANA#W0, R5F104EEANA#W0, R5F104EFANA#W0, R5F104EGANA#W0, R5F104EHANA#W0
		D	R5F104EADNA#U0, R5F104ECDNA#U0, R5F104EDDNA#U0, R5F104EEDNA#U0, R5F104EFDNA#U0, R5F104EGDNA#U0, R5F104EHDNA#U0 R5F104EADNA#W0, R5F104ECDNA#W0, R5F104EDDNA#W0, R5F104EEDNA#W0, R5F104EFDNA#W0, R5F104EGDNA#W0, R5F104EHDNA#W0
		G	R5F104EAGNA#U0, R5F104ECGNA#U0, R5F104EDGNA#U0, R5F104EEGNA#U0, R5F104EFGNA#U0, R5F104EGGNA#U0, R5F104EHGNA#U0 R5F104EAGNA#W0, R5F104ECGNA#W0, R5F104EDGNA#W0, R5F104EEGNA#W0, R5F104EFGNA#W0, R5F104EGGNA#W0, R5F104EHGNA#W0
44 pins	44-pin plastic LQFP (10 × 10, 0.8 mm pitch)	A	R5F104FAAFP#V0, R5F104FCAFP#V0, R5F104FDAFP#V0, R5F104FEAFP#V0, R5F104FFAFP#V0, R5F104FGAFP#V0, R5F104FHAFP#V0, R5F104FJAFP#V0 R5F104FAAFP#X0, R5F104FCAFP#X0, R5F104FDAFP#X0, R5F104FEAFP#X0, R5F104FFAFP#X0, R5F104FGAFP#X0, R5F104FHAFP#X0, R5F104FJAFP#X0
		D	R5F104FADFP#V0, R5F104FCDFP#V0, R5F104FDDFP#V0, R5F104FEDFP#V0, R5F104FFDFP#V0, R5F104FGDFP#V0, R5F104FHDFP#V0, R5F104JDFP#V0 R5F104FADFP#X0, R5F104FCDFP#X0, R5F104FDDFP#X0, R5F104FEDFP#X0, R5F104FFDFP#X0, R5F104FGDFP#X0, R5F104FHDFP#X0, R5F104JDFP#X0
		G	R5F104FAGFP#V0, R5F104FCGFP#V0, R5F104FDGFP#V0, R5F104FEGFP#V0, R5F104FFGFP#V0, R5F104FGGFP#V0, R5F104FHGFP#V0, R5F104FJGFP#V0 R5F104FAGFP#X0, R5F104FCGFP#X0, R5F104FDGFP#X0, R5F104FEGFP#X0, R5F104FFGFP#X0, R5F104FGGFP#X0, R5F104FHGFP#X0, R5F104FJGFP#X0

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

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Pin count	Package	Fields of Application <small>Note</small>	Ordering Part Number	
48 pins	48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)	A	R5F104GAAFB#V0, R5F104GCAFB#V0, R5F104GDAFB#V0, R5F104GEAFB#V0, R5F104GFAFB#V0, R5F104GGAFB#V0, R5F104GHAFB#V0, R5F104GJAFB#V0 R5F104GAAFB#X0, R5F104GCAFB#X0, R5F104GDAFB#X0, R5F104GEAFB#X0, R5F104GFAFB#X0, R5F104GGAFB#X0, R5F104GHAFB#X0, R5F104GJAFB#X0 R5F104GKAFB#30, R5F104GLAFB#30 R5F104GKAFB#50, R5F104GLAFB#50	
		D	R5F104GADFB#V0, R5F104GCDFB#V0, R5F104GDDFB#V0, R5F104GEDFB#V0, R5F104GDFB#V0, R5F104GGDFB#V0, R5F104GHDFB#V0, R5F104GJDFB#V0 R5F104GADFB#X0, R5F104GCDFB#X0, R5F104GDDFB#X0, R5F104GEDFB#X0, R5F104GDFB#X0, R5F104GGDFB#X0, R5F104GHDFB#X0, R5F104GJDFB#X0	
		G	R5F104GAGFB#V0, R5F104GCGFB#V0, R5F104GDGFB#V0, R5F104GEGFB#V0, R5F104GFGFB#V0, R5F104GGGFB#V0, R5F104CHGFB#V0, R5F104GJGFB#V0 R5F104GAGFB#X0, R5F104GCGFB#X0, R5F104GDGFB#X0, R5F104GEGFB#X0, R5F104GFGFB#X0, R5F104GGGFB#X0, R5F104CHGFB#X0, R5F104GJGFB#X0 R5F104GKGF#30, R5F104GLGF#30 R5F104GKGF#50, R5F104GLGF#50	
	48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)	A	R5F104GAANA#U0, R5F104GCANA#U0, R5F104GDANA#U0, R5F104GEANA#U0, R5F104GFANA#U0, R5F104GGANA#U0, R5F104GHANA#U0, R5F104GJANA#U0 R5F104GAANA#W0, R5F104GCANA#W0, R5F104GDANA#W0, R5F104GEANA#W0, R5F104GFANA#W0, R5F104GGANA#W0, R5F104GHANA#W0, R5F104GJANA#W0 R5F104GKANA#U0, R5F104GLANA#U0 R5F104GKANA#W0, R5F104GLANA#W0	
		D	R5F104GADNA#U0, R5F104GCDNA#U0, R5F104GDDNA#U0, R5F104GEDNA#U0, R5F104GFDNA#U0, R5F104GGDNA#U0, R5F104GHDNA#U0, R5F104GJDNA#U0 R5F104GADNA#W0, R5F104GCDNA#W0, R5F104GDDNA#W0, R5F104GEDNA#W0, R5F104GFDNA#W0, R5F104GGDNA#W0, R5F104GHDNA#W0, R5F104GJDNA#W0	
		G	R5F104GAGNA#U0, R5F104GCGNA#U0, R5F104GDGNA#U0, R5F104GEGNA#U0, R5F104GFGNA#U0, R5F104GGGNA#U0, R5F104GHGNA#U0, R5F104GJGNA#U0 R5F104GAGNA#W0, R5F104GCGNA#W0, R5F104GDGNA#W0, R5F104GEGNA#W0, R5F104GFGNA#W0, R5F104GGGNA#W0, R5F104GHGNA#W0, R5F104GJGNA#W0 R5F104GKGNA#U0, R5F104GLGNA#U0 R5F104GKGNA#W0, R5F104GLGNA#W0	
	52 pins	52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)	A	R5F104JCAFA#V0, R5F104JDAFA#V0, R5F104JEFA#V0, R5F104JFAFA#V0, R5F104JGAFA#V0, R5F104JHFA#V0, R5F104JJAFA#V0 R5F104JCAFA#X0, R5F104JDAFA#X0, R5F104JEFA#X0, R5F104JFAFA#X0, R5F104JGAFA#X0, R5F104JHFA#X0, R5F104JJAFA#X0
			D	R5F104JCDFA#V0, R5F104JDDFA#V0, R5F104JEDFA#V0, R5F104JFDFA#V0, R5F104JGDFA#V0, R5F104JHDFA#V0, R5F104JJFA#V0 R5F104JCDFA#X0, R5F104JDDFA#X0, R5F104JEDFA#X0, R5F104JFDFA#X0, R5F104JGDFA#X0, R5F104JHDFA#X0, R5F104JJFA#X0
			G	R5F104JCGFA#V0, R5F104JDGFA#V0, R5F104JEGFA#V0, R5F104JFGFA#V0, R5F104JGGFA#V0, R5F104JHGFA#V0, R5F104JJGFA#V0 R5F104JCGFA#X0, R5F104JDGFA#X0, R5F104JEGFA#X0, R5F104JFGFA#X0, R5F104JGGFA#X0, R5F104JHGFA#X0, R5F104JJGFA#X0

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14**.

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Pin count	Package	Fields of Application Note	Ordering Part Number
64 pins	64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)	A	R5F104LCAFA#V0, R5F104LDAFA#V0, R5F104LEAFA#V0, R5F104LFAFA#V0, R5F104LGFA#V0, R5F104LHFAFA#V0, R5F104LJAFA#V0 R5F104LCAFA#X0, R5F104LDAFA#X0, R5F104LEAFA#X0, R5F104LFAFA#X0, R5F104LGFA#X0, R5F104LHFAFA#X0, R5F104LJAFA#X0 R5F104LKAFA#30, R5F104LLAFA#30 R5F104LKAFA#50, R5F104LLAFA#50
		D	R5F104LCDFA#V0, R5F104LDDFA#V0, R5F104LEDFA#V0, R5F104LFDFA#V0, R5F104LGDFFA#V0, R5F104LHDFFA#V0, R5F104LJDFFA#V0 R5F104LCDFA#X0, R5F104LDDFA#X0, R5F104LEDFA#X0, R5F104LFDFA#X0, R5F104LGDFFA#X0, R5F104LHDFFA#X0, R5F104LJDFFA#X0
		G	R5F104LCGFA#V0, R5F104LDGFA#V0, R5F104LEGFA#V0, R5F104LFGFA#V0, R5F104LGGFA#V0, R5F104LHGFA#V0, R5F104LJGFA#V0 R5F104LCGFA#X0, R5F104LDGFA#X0, R5F104LEGFA#X0, R5F104LFGFA#X0, R5F104LGGFA#X0, R5F104LHGFA#X0, R5F104LJGFA#X0 R5F104LKGFA#30, R5F104LLGFA#30 R5F104LKGFA#50, R5F104LLGFA#50
	64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)	A	R5F104LCAFB#V0, R5F104LDAFB#V0, R5F104LEAFB#V0, R5F104LFAFB#V0, R5F104LGAFB#V0, R5F104LHAFB#V0, R5F104LJAFB#V0 R5F104LCAFB#X0, R5F104LDAFB#X0, R5F104LEAFB#X0, R5F104LFAFB#X0, R5F104LGAFB#X0, R5F104LHAFB#X0, R5F104LJAFB#X0 R5F104LKAFB#30, R5F104LLAFB#30 R5F104LKAFB#50, R5F104LLAFB#50
		D	R5F104LCDFB#V0, R5F104LDDFB#V0, R5F104LEDFB#V0, R5F104LDFB#V0, R5F104LGDFB#V0, R5F104LHDFB#V0, R5F104LJDFB#V0 R5F104LCDFB#X0, R5F104LDDFB#X0, R5F104LEDFB#X0, R5F104LDFB#X0, R5F104LGDFB#X0, R5F104LHDFB#X0, R5F104LJDFB#X0
		G	R5F104LCGFB#V0, R5F104LDGFB#V0, R5F104LEGFB#V0, R5F104LFGFB#V0, R5F104LGGFB#V0, R5F104LHGFB#V0, R5F104LJGFB#V0 R5F104LCGFB#X0, R5F104LDGFB#X0, R5F104LEGFB#X0, R5F104LFGFB#X0, R5F104LGGFB#X0, R5F104LHGFB#X0, R5F104LJGFB#X0 R5F104LKGFB#30, R5F104LLGFB#30 R5F104LKGFB#50, R5F104LLGFB#50
	64-pin plastic FLGA (5 × 5 mm, 0.5 mm pitch)	A	R5F104LCALA#U0, R5F104LDALA#U0, R5F104LEALA#U0, R5F104LFALA#U0, R5F104LGALA#U0, R5F104LHALA#U0, R5F104LJALA#U0 R5F104LCALA#W0, R5F104LDALA#W0, R5F104LEALA#W0, R5F104LFALA#W0, R5F104LGALA#W0, R5F104LHALA#W0, R5F104LJALA#W0 R5F104LKALA#U0, R5F104LLALA#U0 R5F104LKALA#W0, R5F104LLALA#W0
		G	R5F104LCGLA#U0, R5F104LDGLA#U0, R5F104LEGLA#U0, R5F104LFGLA#U0, R5F104LGGLA#U0, R5F104LHGLA#U0, R5F104LJGLA#U0, R5F104LKGLA#U0, R5F104LLGLA#U0 R5F104LCGLA#W0, R5F104LDGLA#W0, R5F104LEGLA#W0, R5F104LFGLA#W0, R5F104LGGLA#W0, R5F104LHGLA#W0, R5F104LJGLA#W0, R5F104LKGLA#W0, R5F104LLGLA#W0
	64-pin plastic LQFP (14 × 14 mm, 0.8 mm pitch)	A	R5F104LCAFP#V0, R5F104LDAFP#V0, R5F104LEAFP#V0, R5F104LFAFP#V0, R5F104LGAFP#V0, R5F104LHAFP#V0, R5F104LJAFP#V0 R5F104LCAFP#X0, R5F104LDAFP#X0, R5F104LEAFP#X0, R5F104LFAFP#X0, R5F104LGAFP#X0, R5F104LHAFP#X0, R5F104LJAFP#X0
D		R5F104LCDFP#V0, R5F104LDDFP#V0, R5F104LEDFP#V0, R5F104LDFFP#V0, R5F104LGDFP#V0, R5F104LHDFP#V0, R5F104LJDFP#V0 R5F104LCDFP#X0, R5F104LDDFP#X0, R5F104LEDFP#X0, R5F104LDFFP#X0, R5F104LGDFP#X0, R5F104LHDFP#X0, R5F104LJDFP#X0	
G		R5F104LCGFP#V0, R5F104LDGFP#V0, R5F104LEGFP#V0, R5F104LFGFP#V0, R5F104LGGFP#V0, R5F104LHGFP#V0, R5F104LJGFP#V0 R5F104LCGFP#X0, R5F104LDGFP#X0, R5F104LEGFP#X0, R5F104LFGFP#X0, R5F104LGGFP#X0, R5F104LHGFP#X0, R5F104LJGFP#X0	

Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14.**

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

(5/5)

Pin count	Package	Fields of Application Note	Ordering Part Number	
80 pins	80-pin plastic LQFP (12 × 12 mm, 0.5 mm pitch)	A	R5F104MFAFB#V0, R5F104MGAFB#V0, R5F104MHAFB#V0, R5F104MJAFB#V0 R5F104MFAFB#X0, R5F104MGAFB#X0, R5F104MHAFB#X0, R5F104MJAFB#X0 R5F104MKAFB#30, R5F104MLAFB#30 R5F104MKAFB#50, R5F104MLAFB#50	
		D	R5F104MDFB#V0, R5F104MGDFB#V0, R5F104MHDFB#V0, R5F104MJDFB#V0 R5F104MDFB#X0, R5F104MGDFB#X0, R5F104MHDFB#X0, R5F104MJDFB#X0	
		G	R5F104MFGFB#V0, R5F104MGGFB#V0, R5F104MHGFB#V0, R5F104MJGFB#V0 R5F104MFGFB#X0, R5F104MGGFB#X0, R5F104MHGFB#X0, R5F104MJGFB#X0 R5F104MKGFB#30, R5F104MLGFB#30 R5F104MKGFB#X0, R5F104MLGFB#50	
	80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)	A	R5F104MFafa#V0, R5F104MGafa#V0, R5F104MHafa#V0, R5F104MJafa#V0 R5F104MFafa#X0, R5F104MGafa#X0, R5F104MHafa#X0, R5F104MJafa#X0 R5F104MKafa#30, R5F104MLafa#30 R5F104MKafa#50, R5F104MLafa#50	
		D	R5F104MFDfa#V0, R5F104MGdfa#V0, R5F104MHdfa#V0, R5F104MJdfa#V0 R5F104MFDfa#X0, R5F104MGdfa#X0, R5F104MHdfa#X0, R5F104MJdfa#X0	
		G	R5F104MFGfa#V0, R5F104MGgfa#V0, R5F104MHgfa#V0, R5F104MJgfa#V0 R5F104MFGfa#X0, R5F104MGgfa#X0, R5F104MHgfa#X0, R5F104MJgfa#X0 R5F104MKGfa#30, R5F104MLgfa#30 R5F104MKGfa#50, R5F104MLgfa#50	
	100 pins	100-pin plastic LQFP (14 × 14 mm, 0.5 mm pitch)	A	R5F104PFAFB#V0, R5F104PGAFA#V0, R5F104PHAFA#V0, R5F104PJAFB#V0 R5F104PFAFB#X0, R5F104PGAFA#X0, R5F104PHAFA#X0, R5F104PJAFB#X0 R5F104PKAFB#30, R5F104PLAFB#30 R5F104PKAFB#50, R5F104PLAFB#50
			D	R5F104PFDfb#V0, R5F104PGDFB#V0, R5F104PHDFB#V0, R5F104PJDFB#V0 R5F104PFDfb#X0, R5F104PGDFB#X0, R5F104PHDFB#X0, R5F104PJDFB#X0
			G	R5F104PFGFB#V0, R5F104PGGFB#V0, R5F104PHGFB#V0, R5F104PJGFB#V0 R5F104PFGFB#X0, R5F104PGGFB#X0, R5F104PHGFB#X0, R5F104PJGFB#X0 R5F104PKGFB#30, R5F104PLGFB#30 R5F104PKGFB#50, R5F104PLGFB#50
100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch)		A	R5F104PFAfa#V0, R5F104PGAfa#V0, R5F104PHAfa#V0, R5F104PJafa#V0 R5F104PFAfa#X0, R5F104PGAfa#X0, R5F104PHAfa#X0, R5F104PJafa#X0 R5F104PKafa#30, R5F104PLafa#30 R5F104PKafa#50, R5F104PLafa#50	
		D	R5F104PFDfa#V0, R5F104PGdfa#V0, R5F104PHdfa#V0, R5F104PJdfa#V0 R5F104PFDfa#X0, R5F104PGdfa#X0, R5F104PHdfa#X0, R5F104PJdfa#X0	
		G	R5F104PFGfa#V0, R5F104PGgfa#V0, R5F104PHgfa#V0, R5F104PJgfa#V0 R5F104PFGfa#X0, R5F104PGgfa#X0, R5F104PHgfa#X0, R5F104PJgfa#X0 R5F104PKgfa#30, R5F104PLgfa#30 R5F104PKgfa#50, R5F104PLgfa#50	

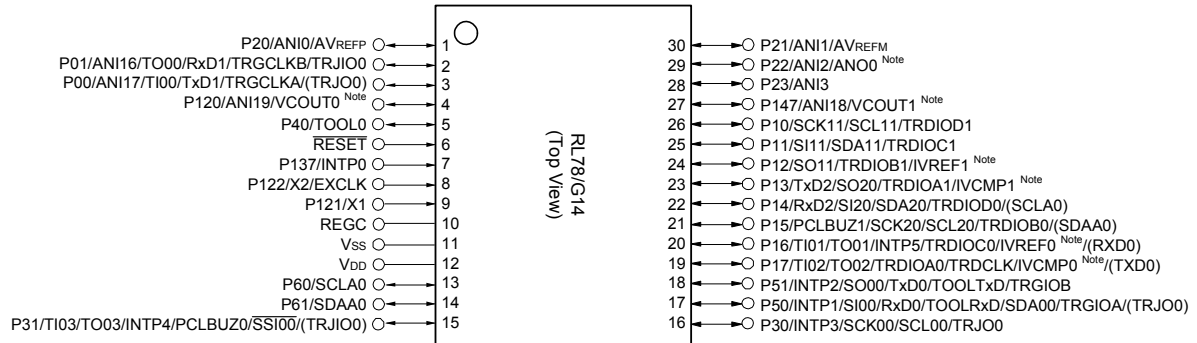
Note For the fields of application, refer to **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14.**

Caution The ordering part numbers represent the numbers at the time of publication. For the latest ordering part numbers, refer to the target product page of the Renesas Electronics website.

1.3 Pin Configuration (Top View)

1.3.1 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

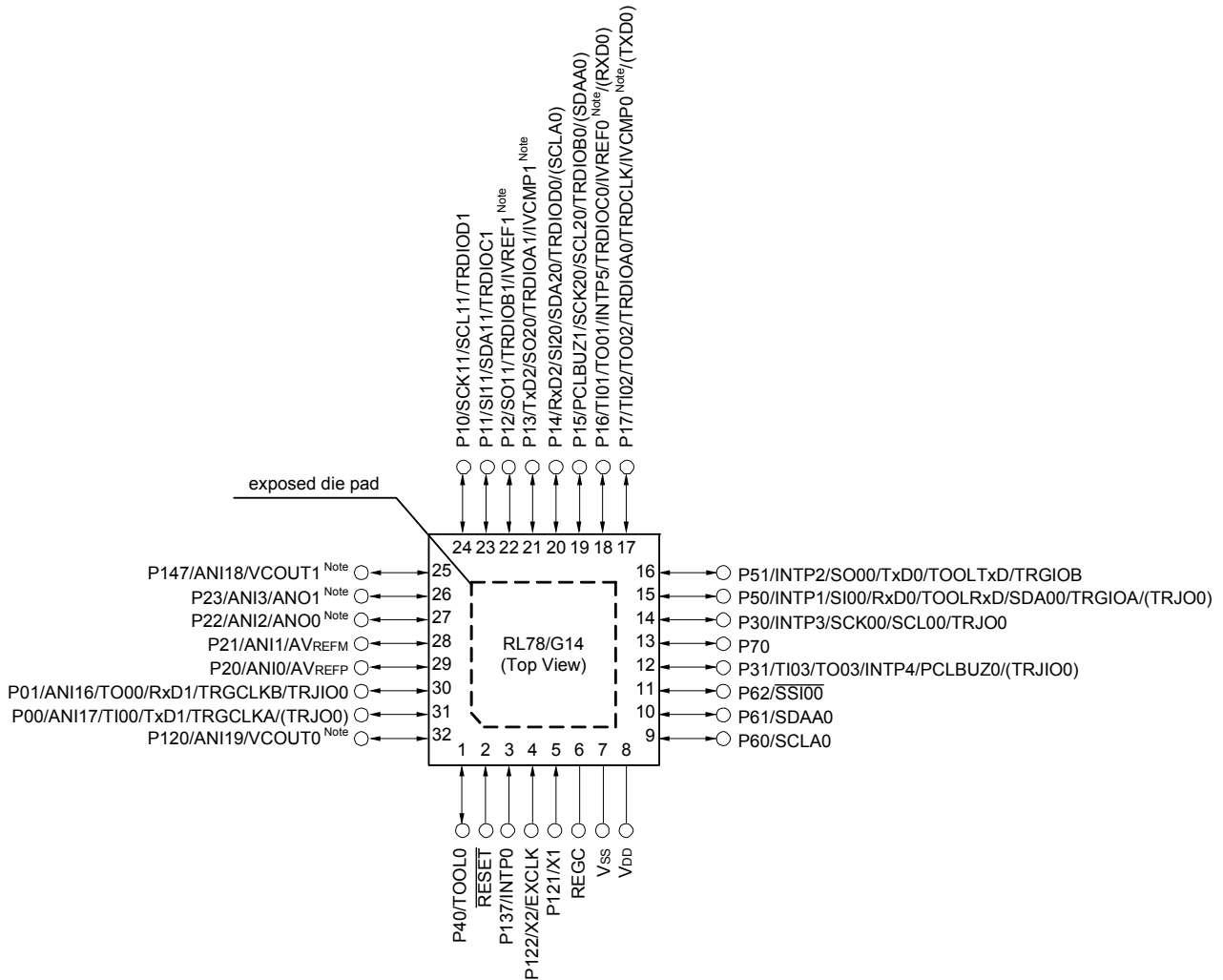
Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.2 32-pin products

- 32-pin plastic HWQFN (5 × 5 mm, 0.5 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

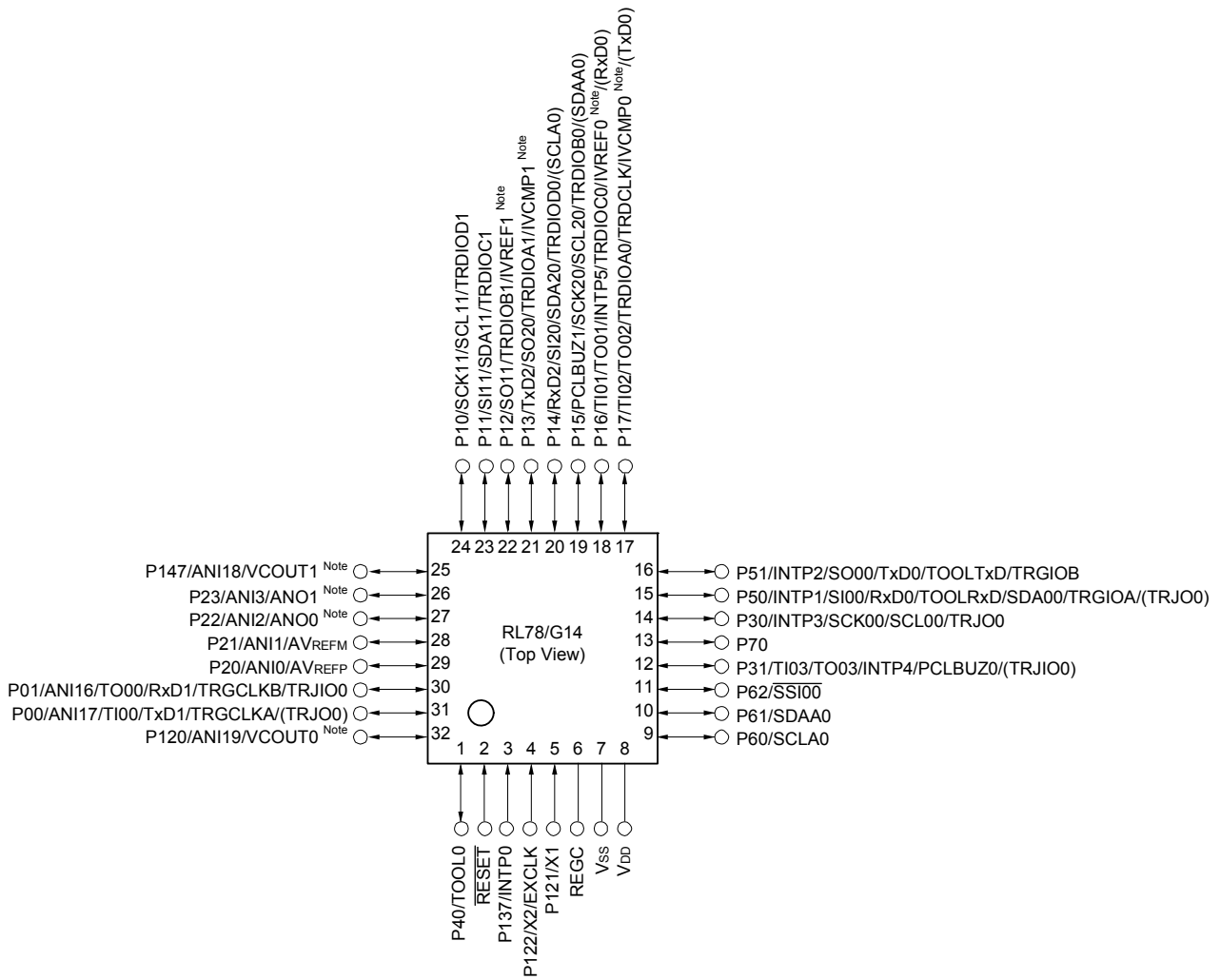
Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

Remark 3. It is recommended to connect an exposed die pad to V_{SS}.

- 32-pin plastic LQFP (7 × 7 mm, 0.8 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

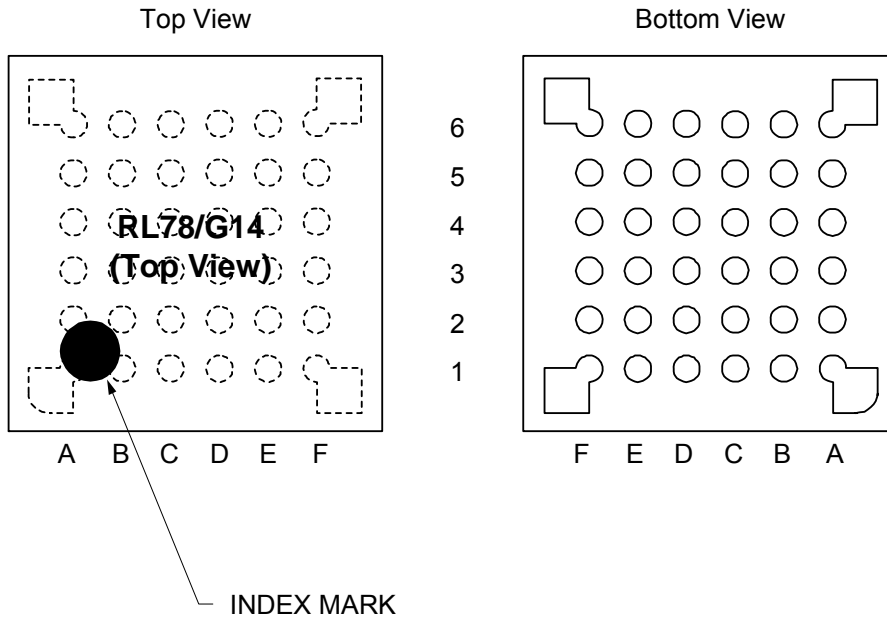
Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.3 36-pin products

- 36-pin plastic WFLGA (4 × 4 mm, 0.5 mm pitch)



	A	B	C	D	E	F	
6	P60/SCLA0	V _{DD}	P121/X1	P122/X2/EXCLK	P137/INTP0	P40/TOOL0	6
5	P62/ $\overline{\text{SSI00}}$	P61/SDAA0	V _{SS}	REGC	$\overline{\text{RESET}}$	P120/ANI19/ VCOUT0 Note	5
4	P72/SO21	P71/SI21/ SDA21	P14/RxD2/SI20/ SDA20/TRDIOD0/ (SCLA0)	P31/TI03/TO03/ INTP4/PCLBUZ0/ (TRJIO0)	P00/TI00/TxD1/ TRGCLKA/ (TRJO0)	P01/TO00/ RxD1/TRGCLKB/ TRJIO0	4
3	P50/INTP1/ SI00/RxD0/ TOOLRxD/ SDA00/TRGIOA/ (TRJO0)	P70/SCK21/ SCL21	P15/PCLBUZ1/ SCK20/SCL20/ TRDIOB0/ (SDAA0)	P22/ANI2/ ANO0 Note	P20/ANI0/ AVREFP	P21/ANI1/ AVREFM	3
2	P30/INTP3/ SCK00/SCL00/ TRJO0	P16/TI01/TO01/ INTP5/TRDIOC0/ IVREF0 Note/ (RXD0)	P12/SO11/ TRDIOB1/ IVREF1 Note	P11/SI11/ SDA11/ TRDIOC1	P24/ANI4	P23/ANI3/ ANO1 Note	2
1	P51/INTP2/ SO00/TxD0/ TOOLTxD/ TRGIOB	P17/TI02/TO02/ TRDIOA0/ TRDCLK/ IVCMP0 Note/ (TXD0)	P13/TxD2/ SO20/TRDIOA1/ IVCMP1 Note	P10/SCK11/ SCL11/ TRDIOD1	P147/ANI18/ VCOUT1 Note	P25/ANI5	1
	A	B	C	D	E	F	

Note Mounted on the 96 KB or more code flash memory products.

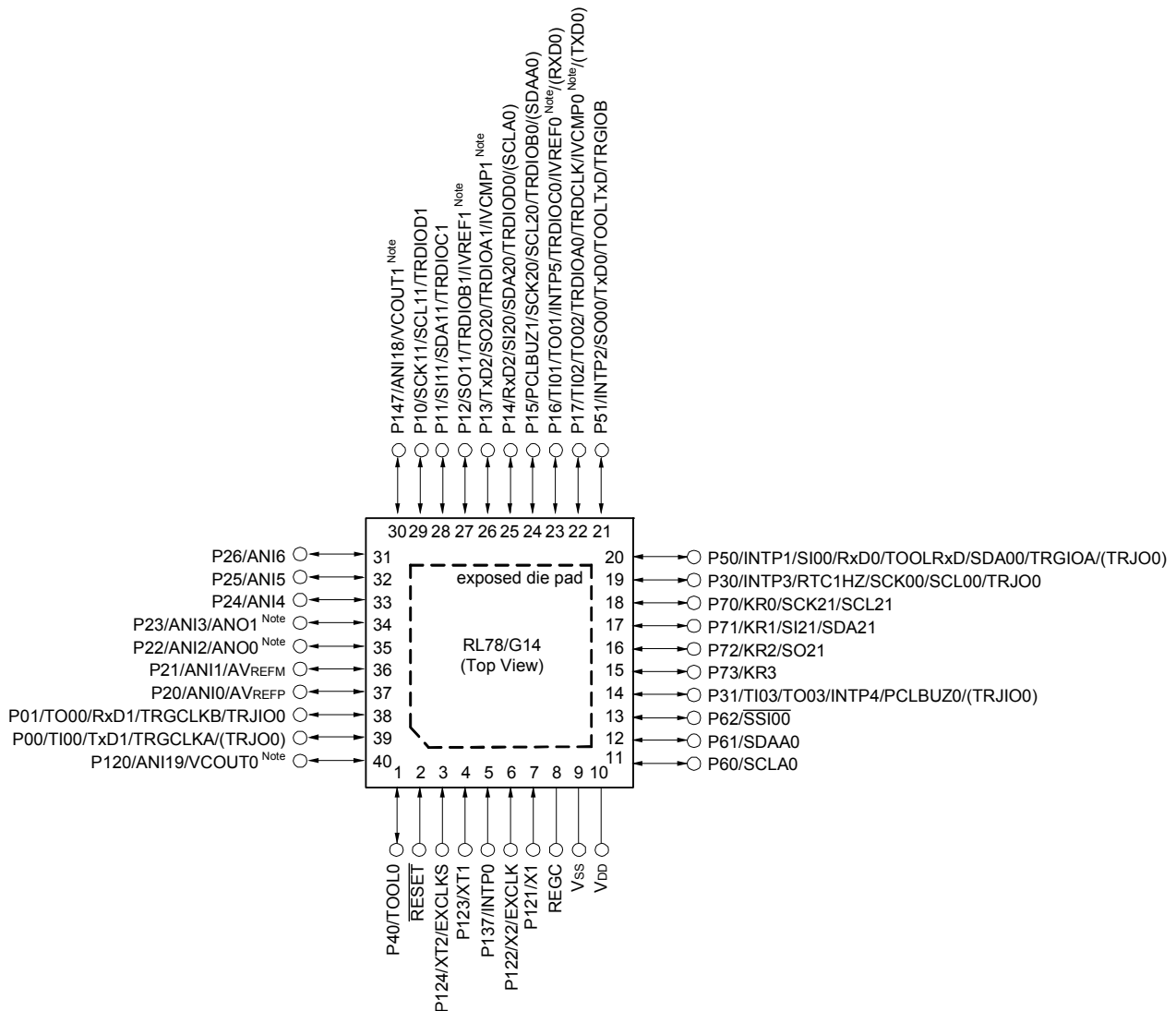
Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.4 40-pin products

- 40-pin plastic HWQFN (6 × 6 mm, 0.5 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

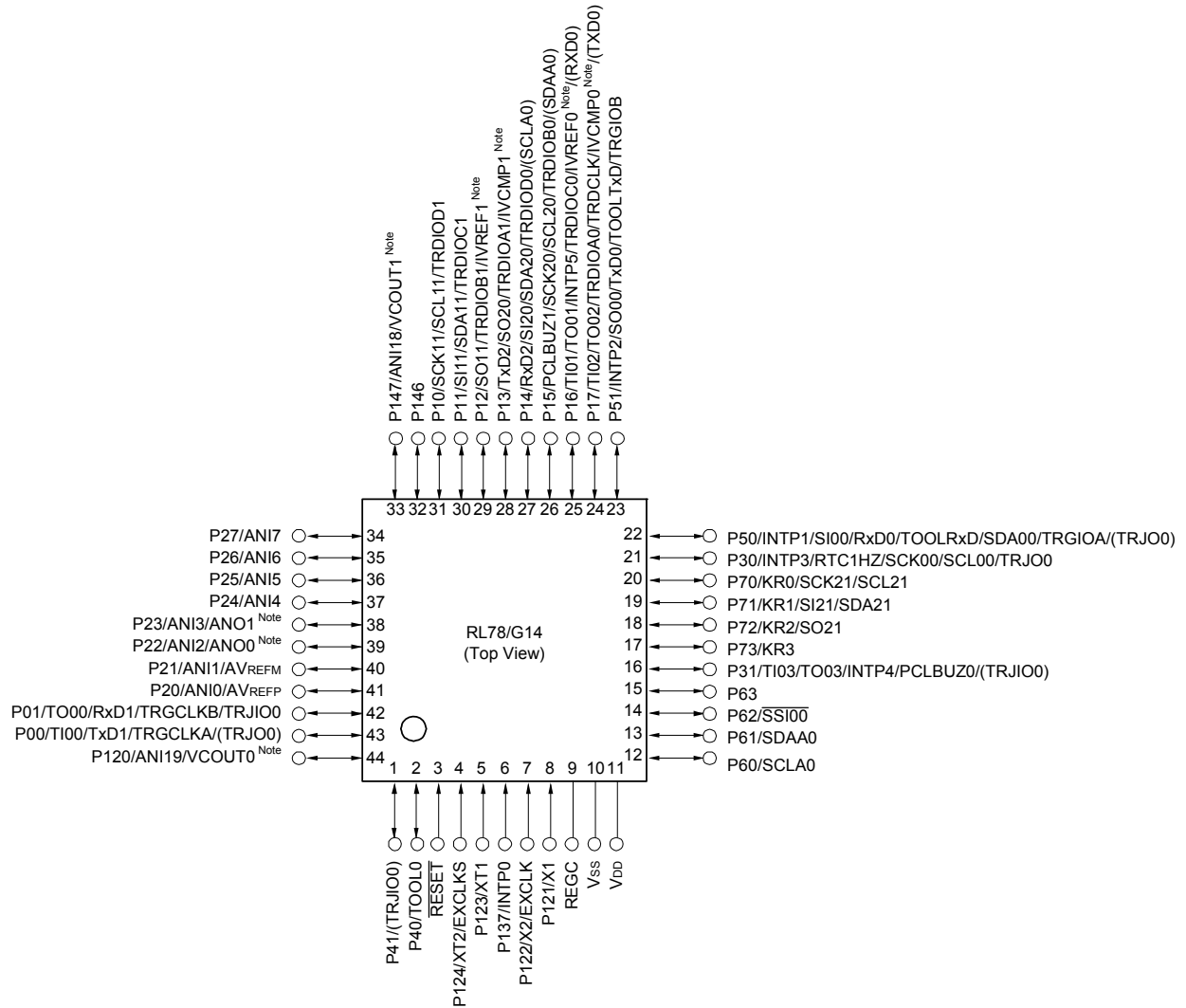
Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

Remark 3. It is recommended to connect an exposed die pad to V_{SS}.

1.3.5 44-pin products

- 44-pin plastic LQFP (10 × 10 mm, 0.8 mm pitch)



Note Mounted on the 96 KB or more code flash memory products.

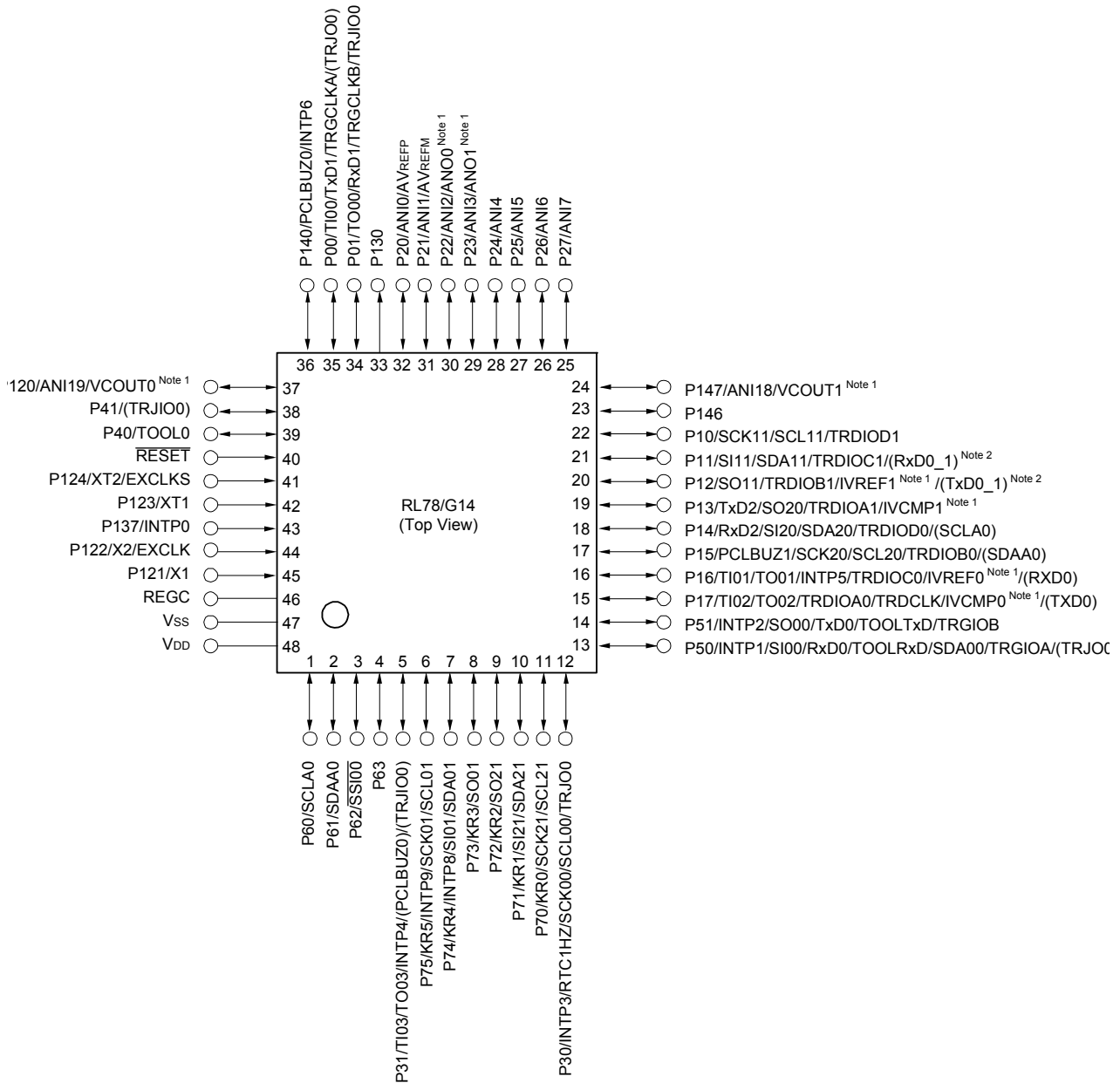
Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.6 48-pin products

- 48-pin plastic LFQFP (7 × 7 mm, 0.5 mm pitch)



Note 1. Mounted on the 96 KB or more code flash memory products.

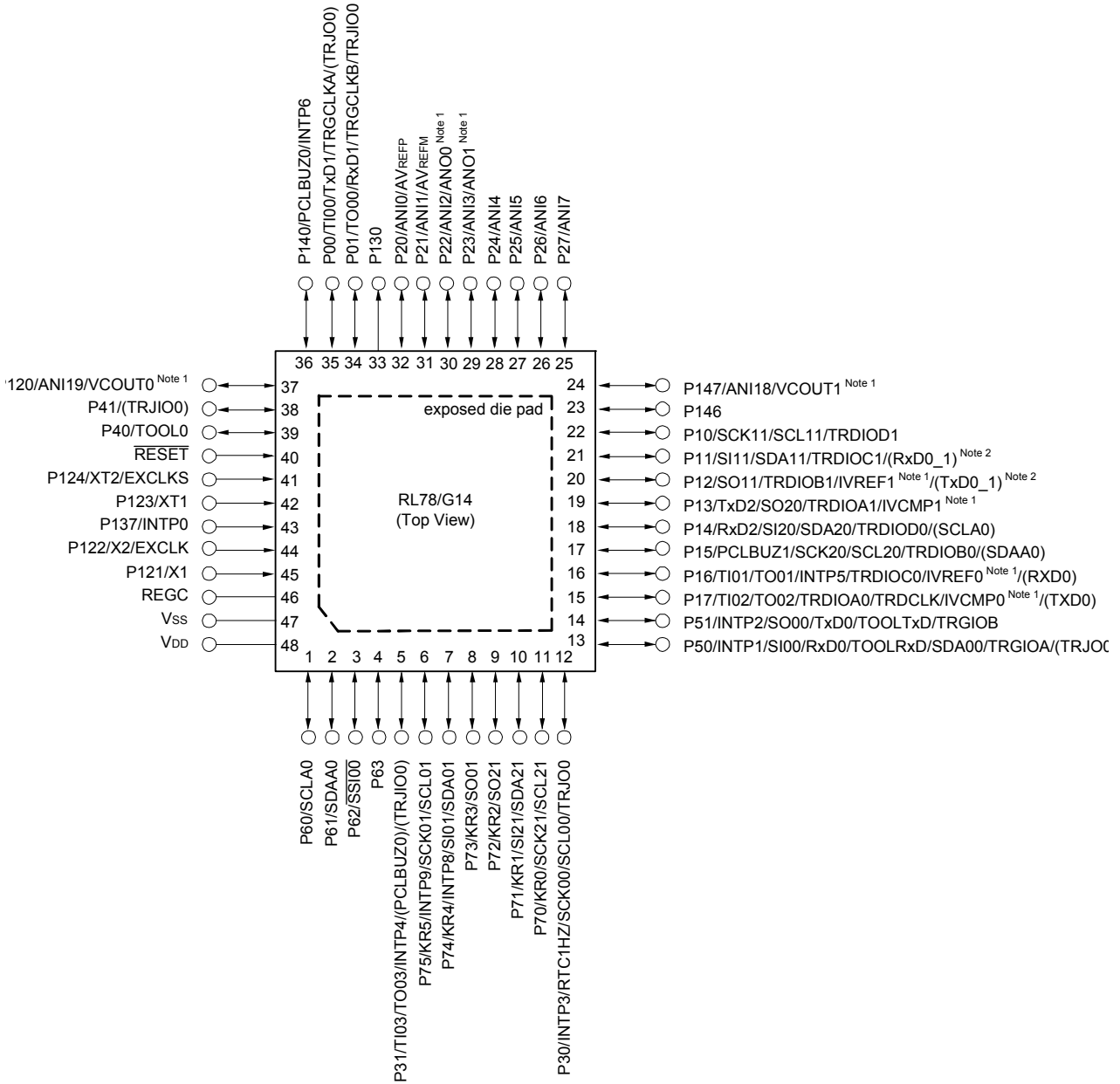
Note 2. Mounted on the 384 KB or more code flash memory products.

Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

- 48-pin plastic HWQFN (7 × 7 mm, 0.5 mm pitch)



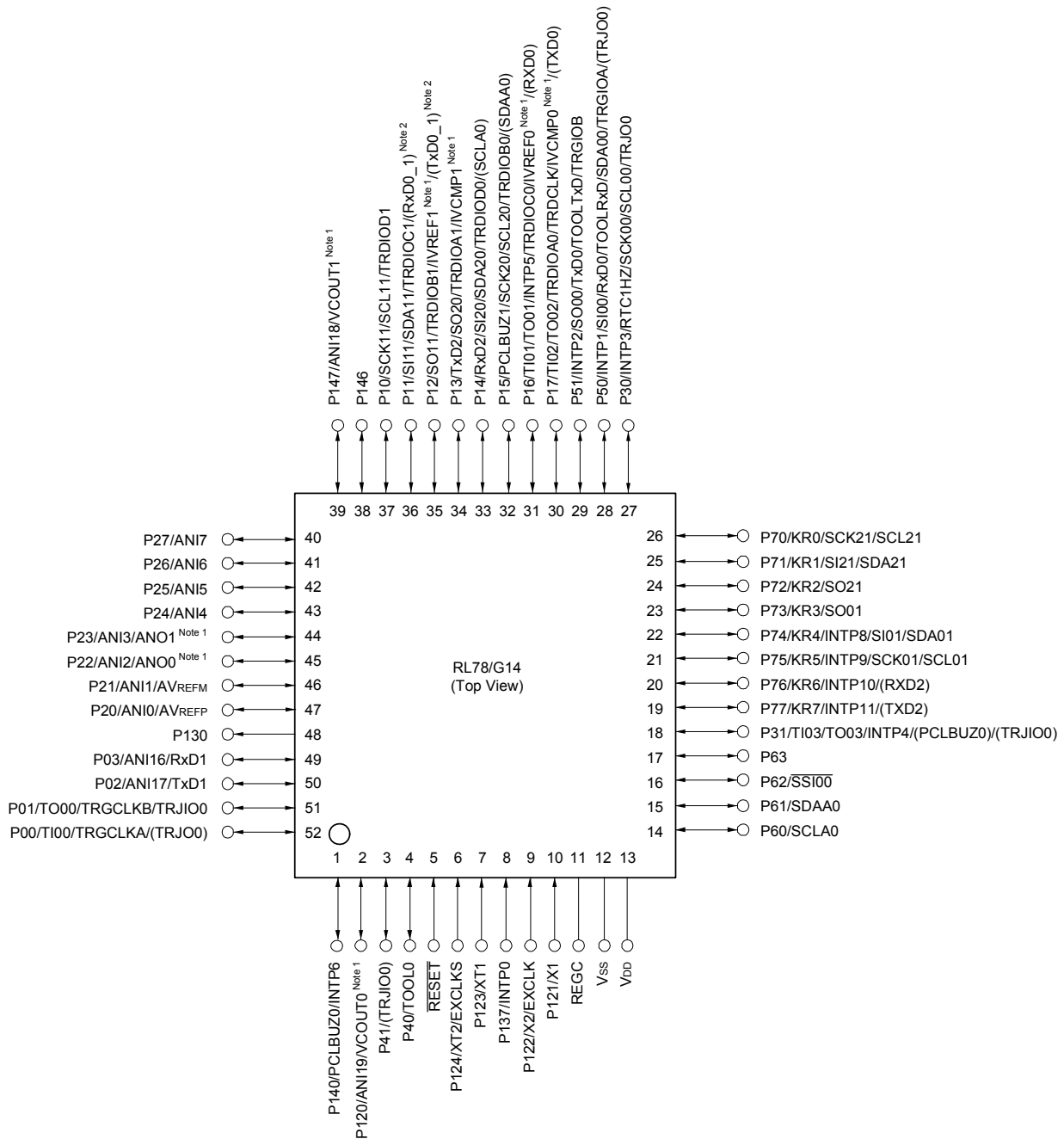
- Note 1.** Mounted on the 96 KB or more code flash memory products.
- Note 2.** Mounted on the 384 KB or more code flash memory products.

Caution Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

- Remark 1.** For pin identification, see 1.4 Pin Identification.
- Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).
- Remark 3.** It is recommended to connect an exposed die pad to Vss.

1.3.7 52-pin products

- 52-pin plastic LQFP (10 × 10 mm, 0.65 mm pitch)



Note 1. Mounted on the 96 KB or more code flash memory products.

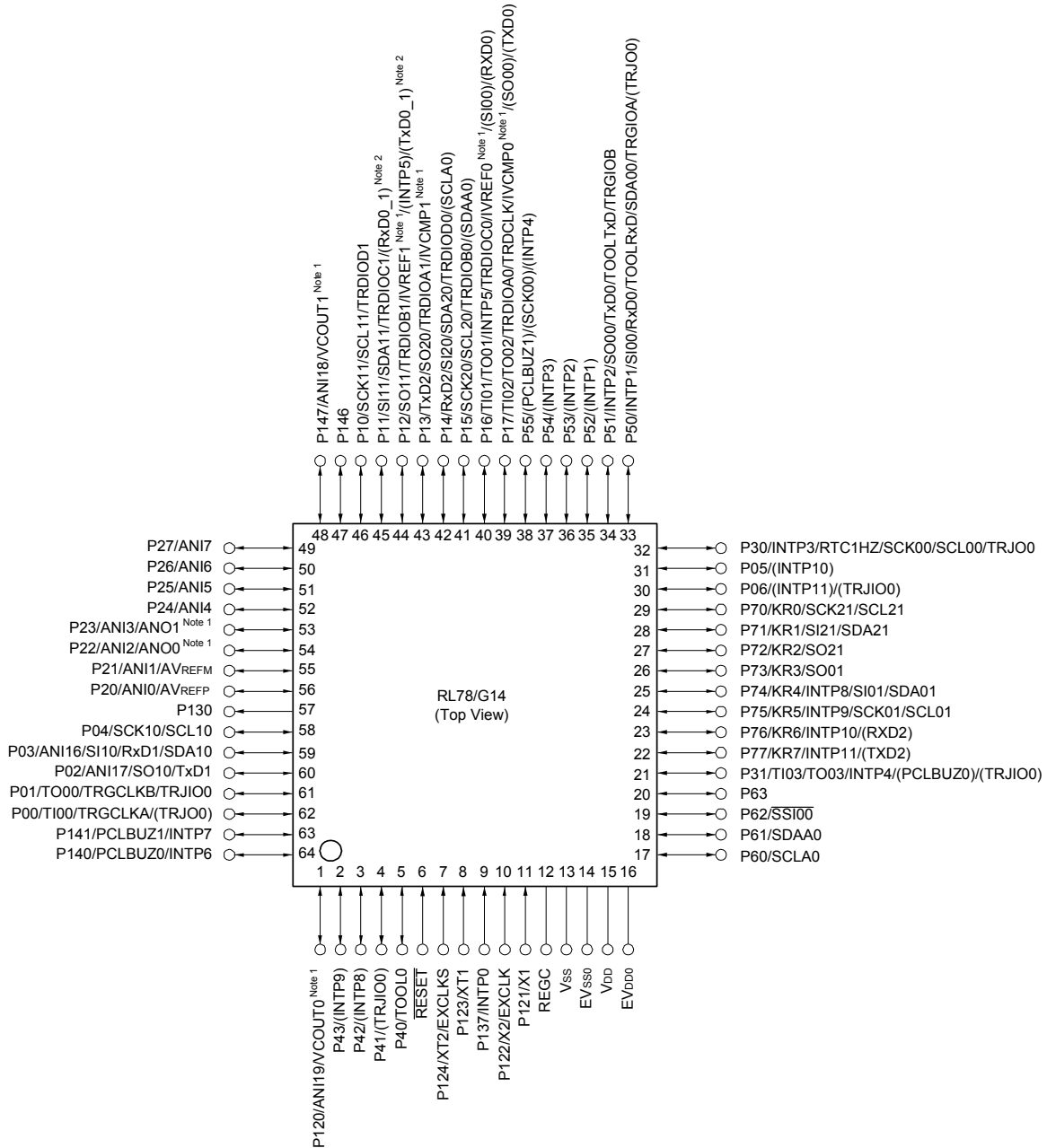
Caution Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.8 64-pin products

- 64-pin plastic LQFP (14 × 14 mm, 0.8 mm pitch)
- 64-pin plastic LQFP (12 × 12 mm, 0.65 mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.5 mm pitch)



Note 1. Mounted on the 96 KB or more code flash memory products.

Note 2. Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EVSS0 pin the same potential as Vss pin.

Caution 2. Make VDD pin the potential that is higher than EVDD0 pin.

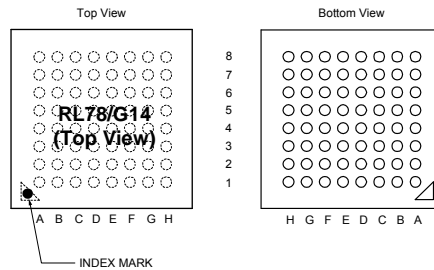
Caution 3. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the Vss and EVSS0 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

- 64-pin plastic FLGA (5 × 5 mm, 0.5 mm pitch)



	A	B	C	D	E	F	G	H	
8	EVDD0	EVSS0	P121/X1	P122/X2/ EXCLK	P137/INTP0	P123/XT1	P124/XT2/ EXCLKS	P120/ANI19/ VCOUT0 Note 1	8
7	P60/SCLA0	VDD	VSS	REGC	RESET	P01/TO00/ TRGCLKB/ TRJIO0	P00/TI00/ TRGCLKA/ (TRJIO0)	P140/ PCLBUZ0/ INTP6	7
6	P61/SDAA0	P62/SSIO0	P63	P40/TOOL0	P41/(TRJIO0)	P43/(INTP9)	P02/ANI17/ SO10/TxD1	P141/ PCLBUZ1/ INTP7	6
5	P77/KR7/ INTP11/(TXD2)	P31/TI03/ TO03/INTP4/ (PCLBUZ0)/ (TRJIO0)	P53/(INTP2)	P42/(INTP8)	P03/ANI16/ SI10/RxD1/ SDA10	P04/SCK10/ SCL10	P130	P20/ANI0/ AVREFP	5
4	P75/KR5/ INTP9/ SCK01/ SCL01	P76/KR6/ INTP10/ (RXD2)	P52/(INTP1)	P54/(INTP3)	P16/TI01/ TO01/INTP5/ TRDI0C0/ IVREF0 Note 1/ (SI00)/(RXD0)	P21/ANI1/ AVREFM	P22/ANI2/ ANO0 Note 1	P23/ANI3/ ANO1 Note 1	4
3	P70/KR0/ SCK21/ SCL21	P73/KR3/ SO01	P74/KR4/ INTP8/SI01/ SDA01	P17/TI02/TO02/ TRDIOA0/ TRDCLK/ IVCMP0 Note 1/ (SO00)/(TXD0)	P15/SCK20/ SCL20/ TRDIOB0/ (SDAA0)	P12/SO11/ TRDIOB1/ IVREF1 Note 1/ (INTP5)/ (TxD0_1) Note 2	P24/ANI4	P26/ANI6	3
2	P30/INTP3/ RTC1HZ/ SCK00/ SCL00/TRJIO0	P72/KR2/ SO21	P71/KR1/ SI21/SDA21	P06/(INTP11)/ (TRJIO0)	P14/RxD2/ SI20/SDA20/ TRDIOD0/ (SCLA0)	P11/SI11/ SDA11/ TRDI0C1/ (RxD0_1) Note 2	P25/ANI5	P27/ANI7	2
1	P05/(INTP10)	P50/INTP1/ SI00/RxD0/ TOOLRxD/ SDA00/ TRGIOA/ (TRJIO0)	P51/INTP2/ SO00/TxD0/ TOOLTxD/ TRGIOB	P55/ (PCLBUZ1)/ (SCK00)/ (INTP4)	P13/TxD2/ SO20/ TRDIOA1/ IVCMP1 Note 1	P10/SCK11/ SCL11/ TRDIOD1	P146	P147/ANI18/ VCOUT1 Note 1	1
	A	B	C	D	E	F	G	H	

Note 1. Mounted on the 96 KB or more code flash memory products.

Note 2. Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EVSS0 pin the same potential as VSS pin.

Caution 2. Make VDD pin the potential that is higher than EVDD0 pin.

Caution 3. Connect the REGC pin to VSS pin via a capacitor (0.47 to 1 μF).

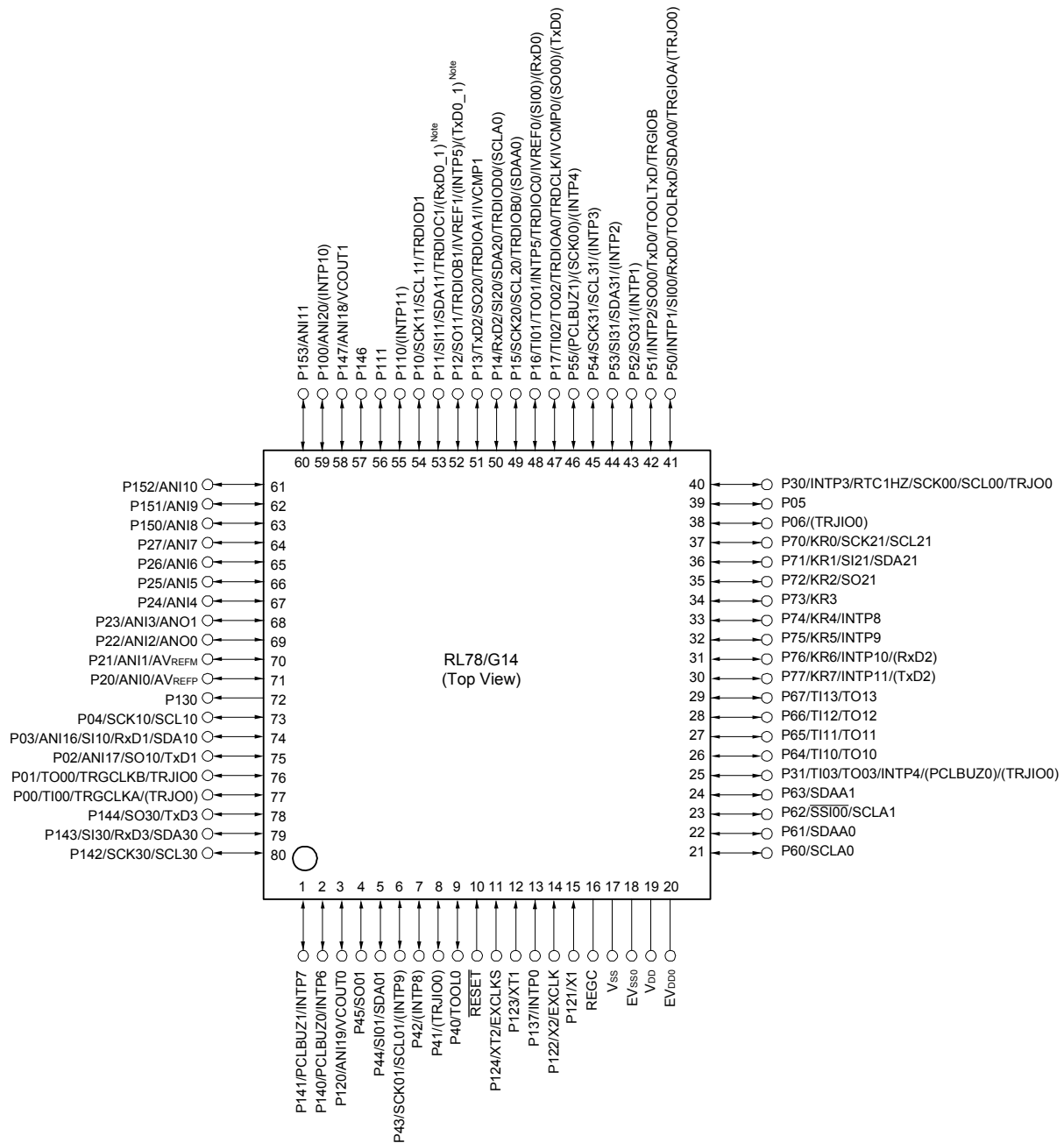
Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the VSS and EVSS0 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.9 80-pin products

- 80-pin plastic LQFP (14 × 14 mm, 0.65 mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.5 mm pitch)



Note Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EV_{SS0} pin the same potential as V_{SS} pin.

Caution 2. Make V_{DD} pin the potential that is higher than EV_{DD0} pin.

Caution 3. Connect the REGC pin to V_{SS} pin via a capacitor (0.47 to 1 μF).

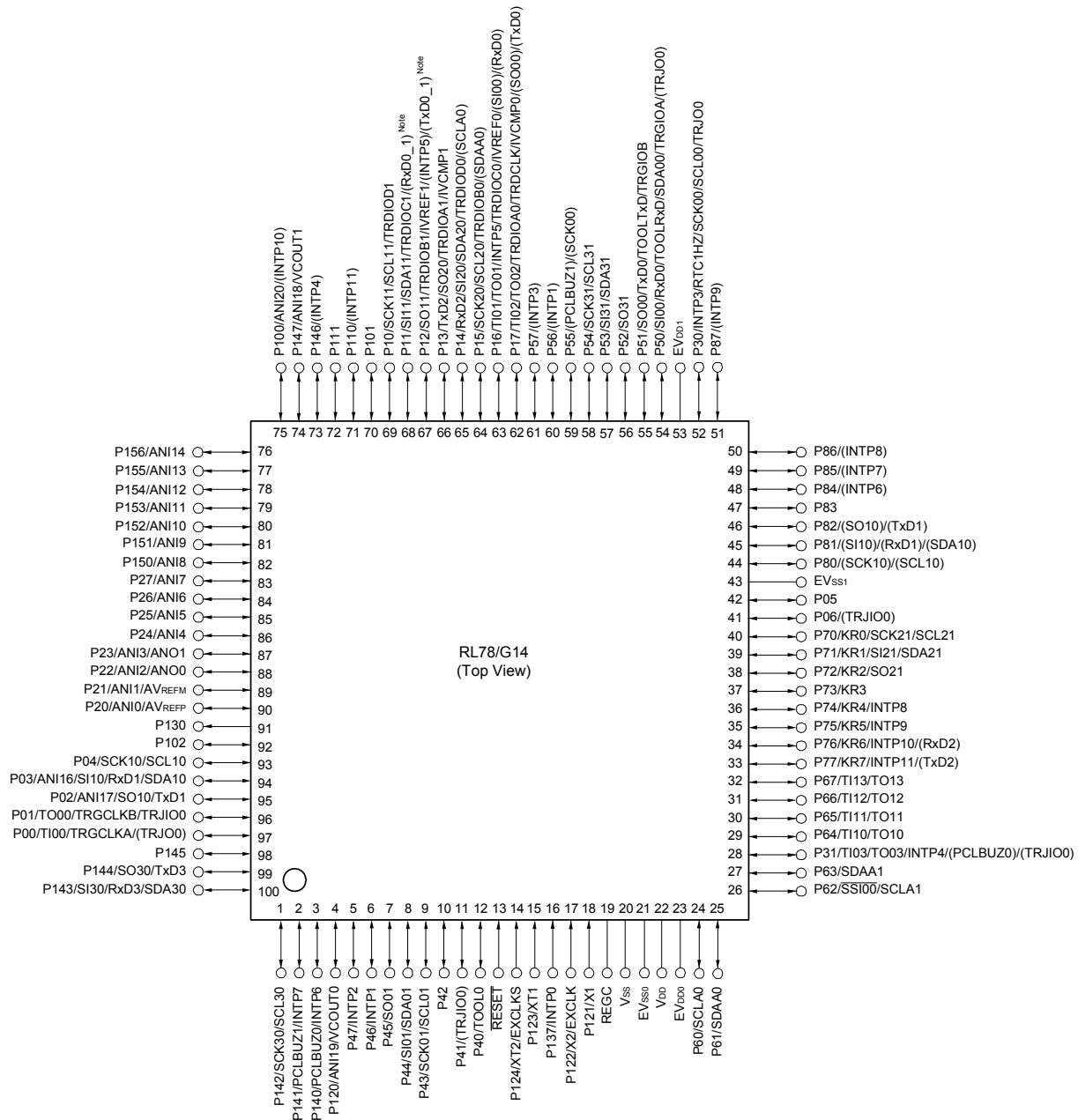
Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{DD0} pins and connect the V_{SS} and EV_{SS0} pins to separate ground lines.

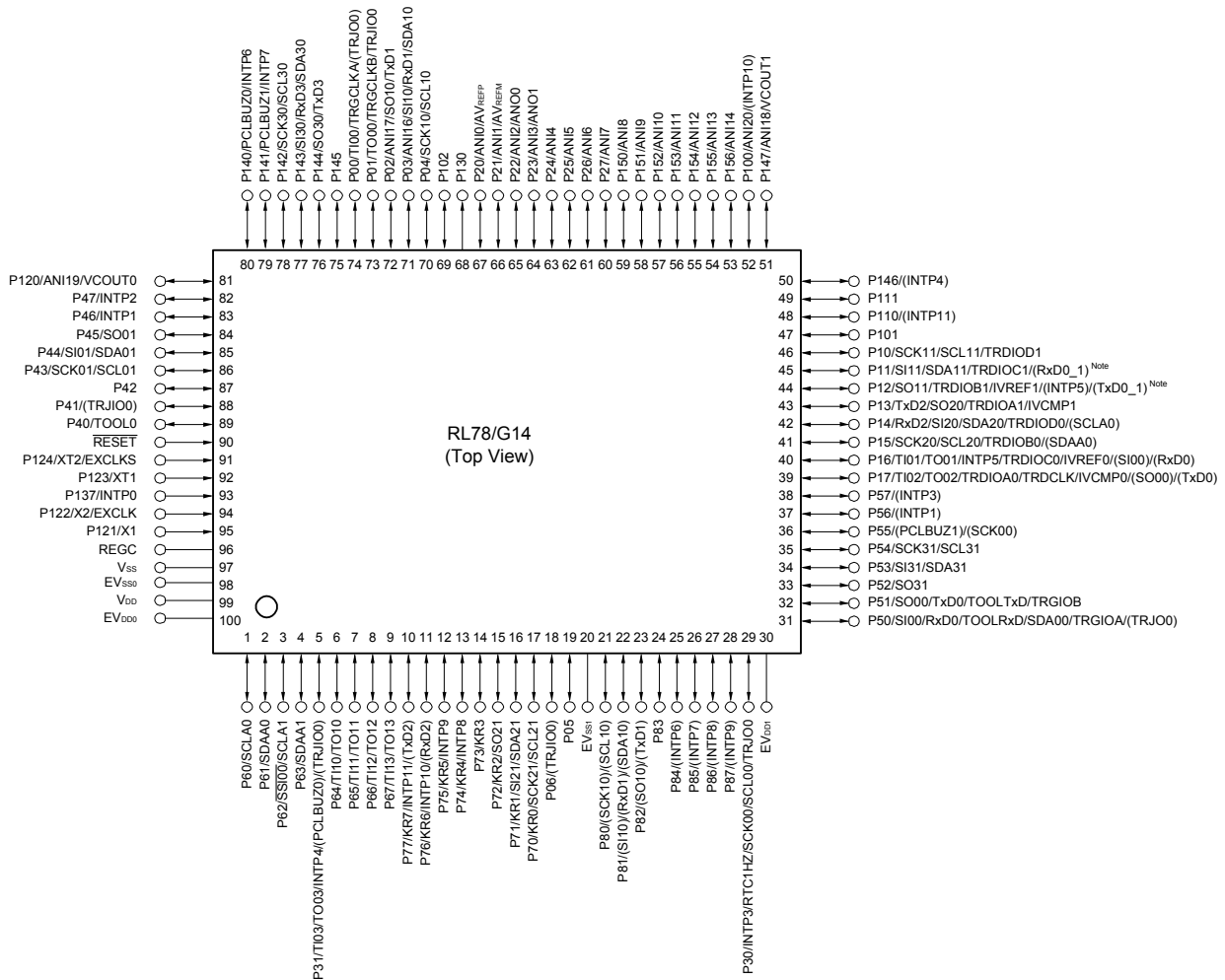
Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.3.10 100-pin products

- 100-pin plastic LFQFP (14 × 14 mm, 0.5 mm pitch)



- 100-pin plastic LQFP (14 × 20 mm, 0.65 mm pitch)



Note Mounted on the 384 KB or more code flash memory products.

Caution 1. Make EVss0, EVss1 pins the same potential as Vss pin.

Caution 2. Make VDD pin the potential that is higher than EVDD0, EVDD1 pins (EVDD0 = EVDD1).

Caution 3. Connect the REGC pin to Vss pin via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD, EVDD0 and EVDD1 pins and connect the Vss, EVss0 and EVss1 pins to separate ground lines.

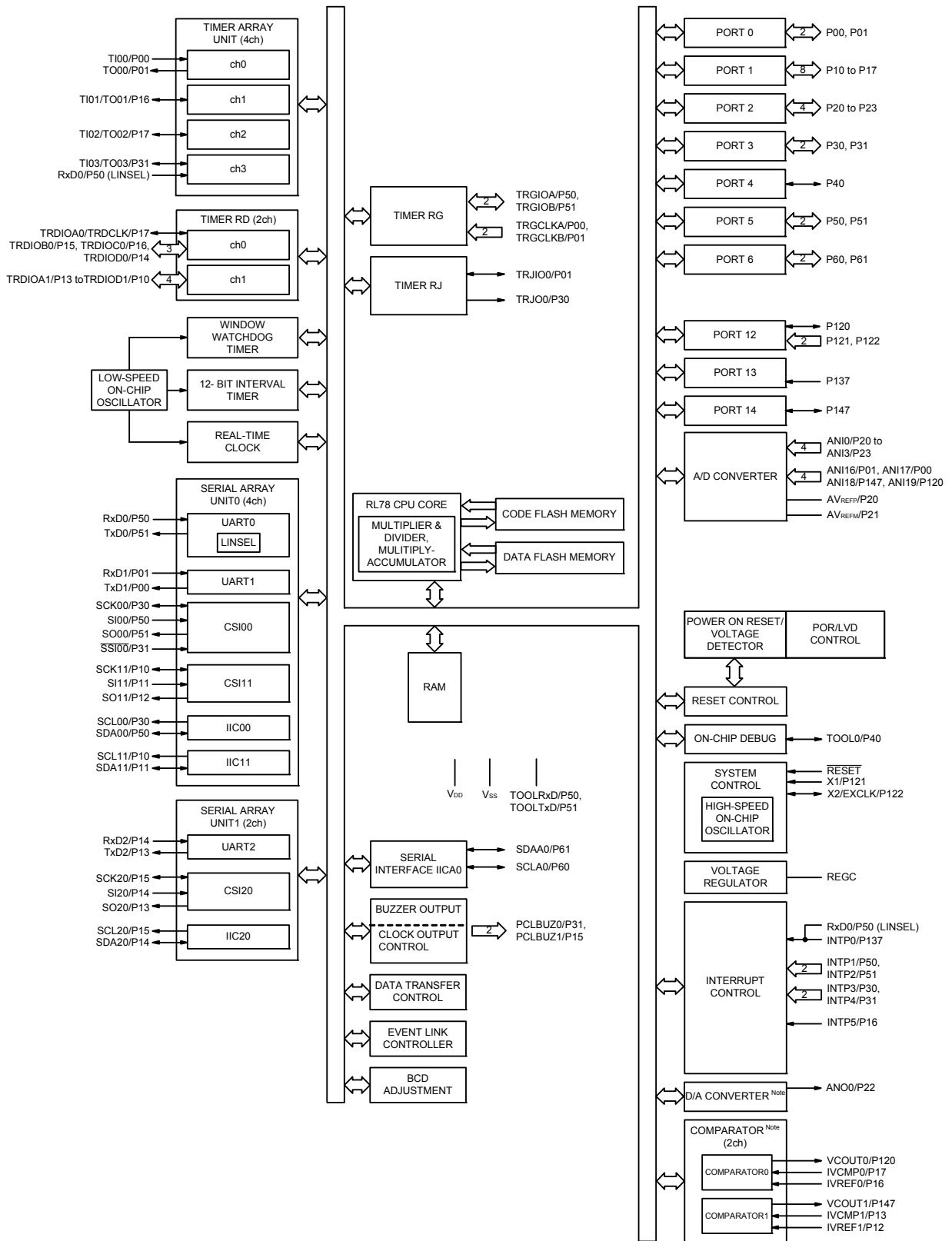
Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register 0, 1 (PIOR0, 1).

1.4 Pin Identification

ANI0 to ANI14,:	Analog input	RxD0 to RxD3:	Receive data
ANI16 to ANI20		SCK00, SCK01, SCK10,:	Serial clock input/output
ANO0, ANO1:	Analog output	SCK11, SCK20, SCK21,	
AVREFM:	A/D converter reference potential (– side) input	SCK30, SCK31	
AVREFP:	A/D converter reference potential (+ side) input	SCLA0, SCLA1,:	Serial clock input/output
		SCL00, SCL01, SCL10, SCL11,:	Serial clock output
		SCL20, SCL21, SCL30,	
EVDD0, EVDD1:	Power supply for port	SCL31	
EVSS0, EVSS1:	Ground for port	SDAA0, SDAA1, SDA00,:	Serial data input/output
EXCLK:	External clock input (main system clock)	SDA01, SDA10, SDA11,	
		SDA20, SDA21, SDA30,	
EXCLKS:	External clock input (subsystem clock)	SDA31	
		SI00, SI01, SI10, SI11,:	Serial data input
INTP0 to INTP11:	External interrupt input	SI20, SI21, SI30, SI31	
IVCMP0, IVCMP1:	Comparator input	SO00, SO01, SO10,:	Serial data output
IVREF0, IVREF1:	Comparator reference input	SO11, SO20, SO21,	
KR0 to KR7:	Key return	SO30, SO31	
P00 to P06:	Port 0	$\overline{\text{SSI00}}$:	Serial interface chip select input
P10 to P17:	Port 1	TI00 to TI03,:	Timer input
P20 to P27:	Port 2	TI10 to TI13	
P30, P31:	Port 3	TO00 to TO03,:	Timer output
P40 to P47:	Port 4	TO10 to TO13, TRJ00	
P50 to P57:	Port 5	TOOL0:	Data input/output for tool
P60 to P67:	Port 6	TOOLRxD, TOOLTxD:	Data input/output for external device
P70 to P77:	Port 7	TRDCLK, TRGCLKA,:	Timer external input clock
P80 to P87:	Port 8	TRGCLKB	
P100 to P102:	Port 10	TRDIOA0, TRDIOB0,:	Timer input/output
P110, P111:	Port 11	TRDIOC0, TRDIOD0,	
P120 to P124:	Port 12	TRDIOA1, TRDIOB1,	
P130, P137:	Port 13	TRDIOC1, TRDIOD1,	
P140 to P147:	Port 14	TRGIOA, TRGIOB, TRJIO0	
P150 to P156:	Port 15	TxD0 to TxD3:	Transmit data
PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output	VCOUT0, VCOUT1:	Comparator output
		VDD:	Power supply
REGC:	Regulator capacitance	VSS:	Ground
$\overline{\text{RESET}}$:	Reset	X1, X2:	Crystal oscillator (main system clock)
RTC1HZ:	Real-time clock correction clock (1 Hz) output	XT1, XT2:	Crystal oscillator (subsystem clock)

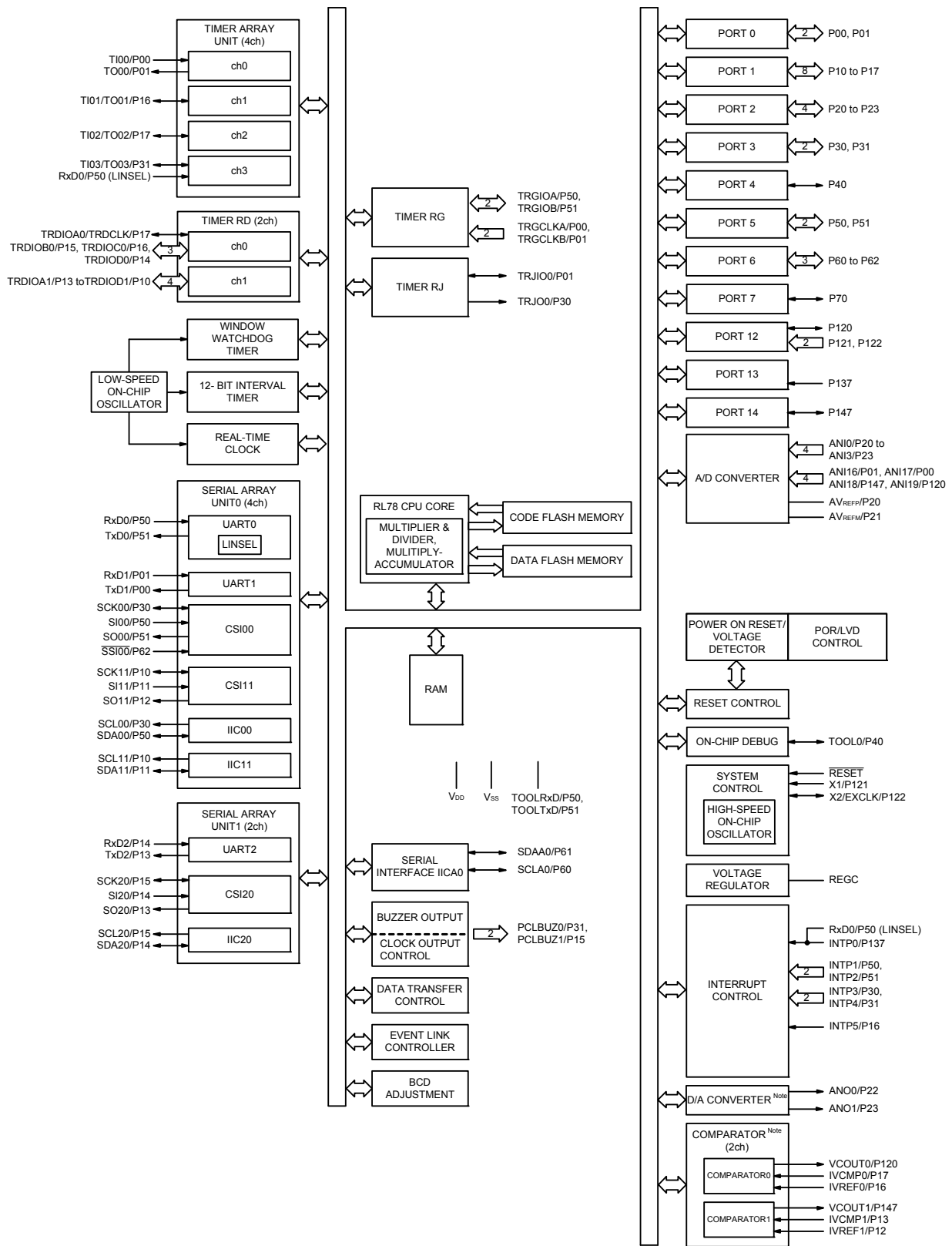
1.5 Block Diagram

1.5.1 30-pin products



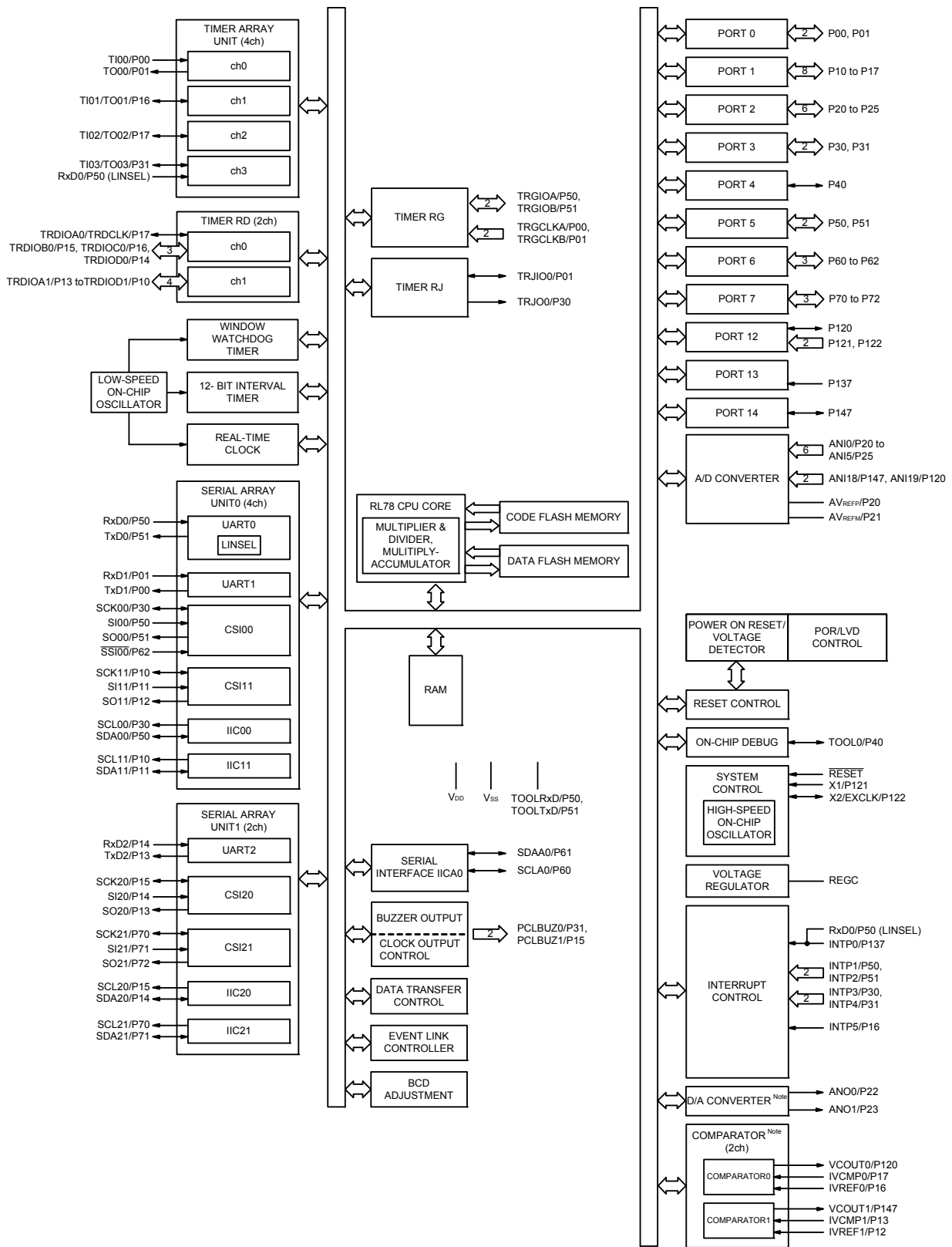
Note Mounted on the 96 KB or more code flash memory products.

1.5.2 32-pin products



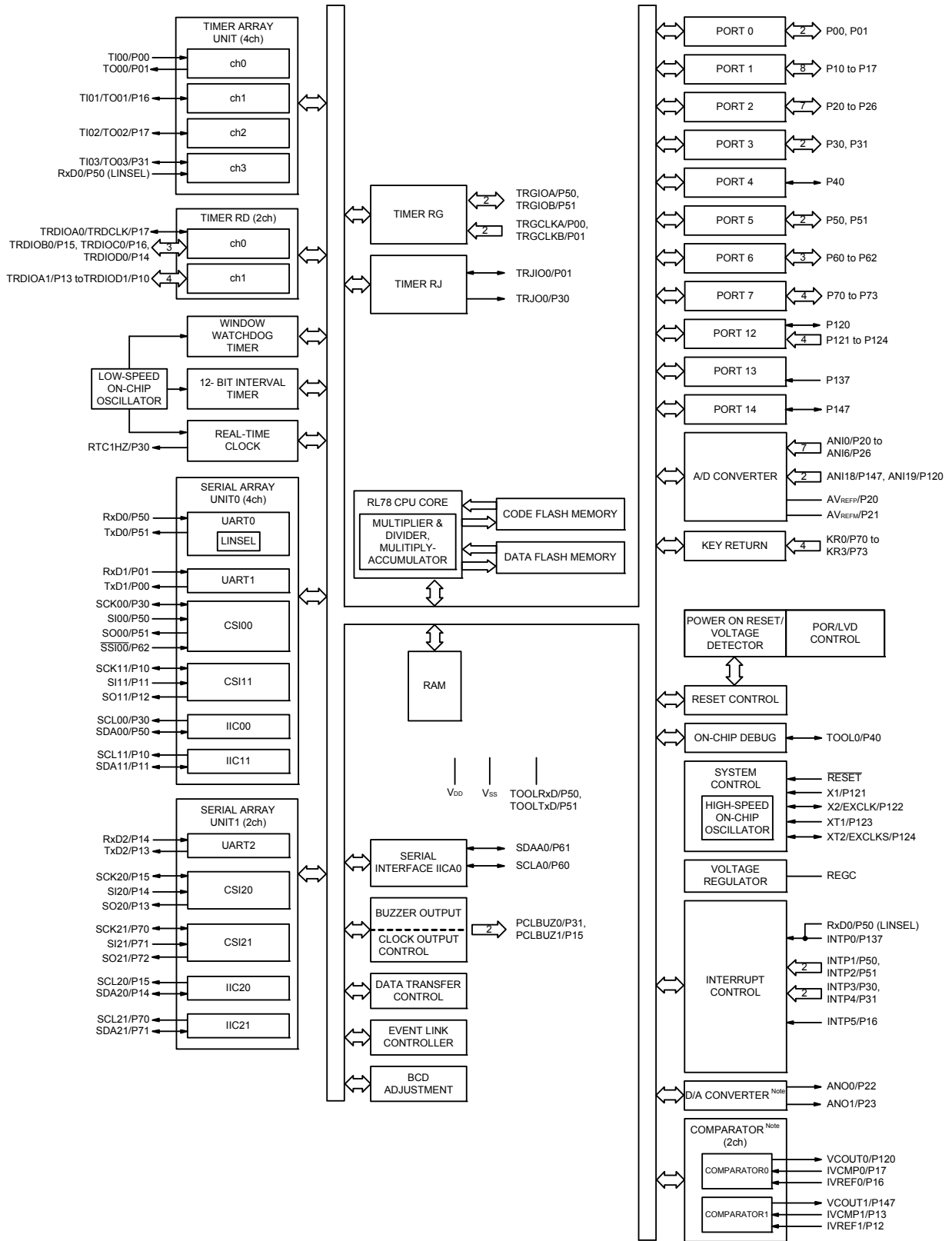
Note Mounted on the 96 KB or more code flash memory products.

1.5.3 36-pin products



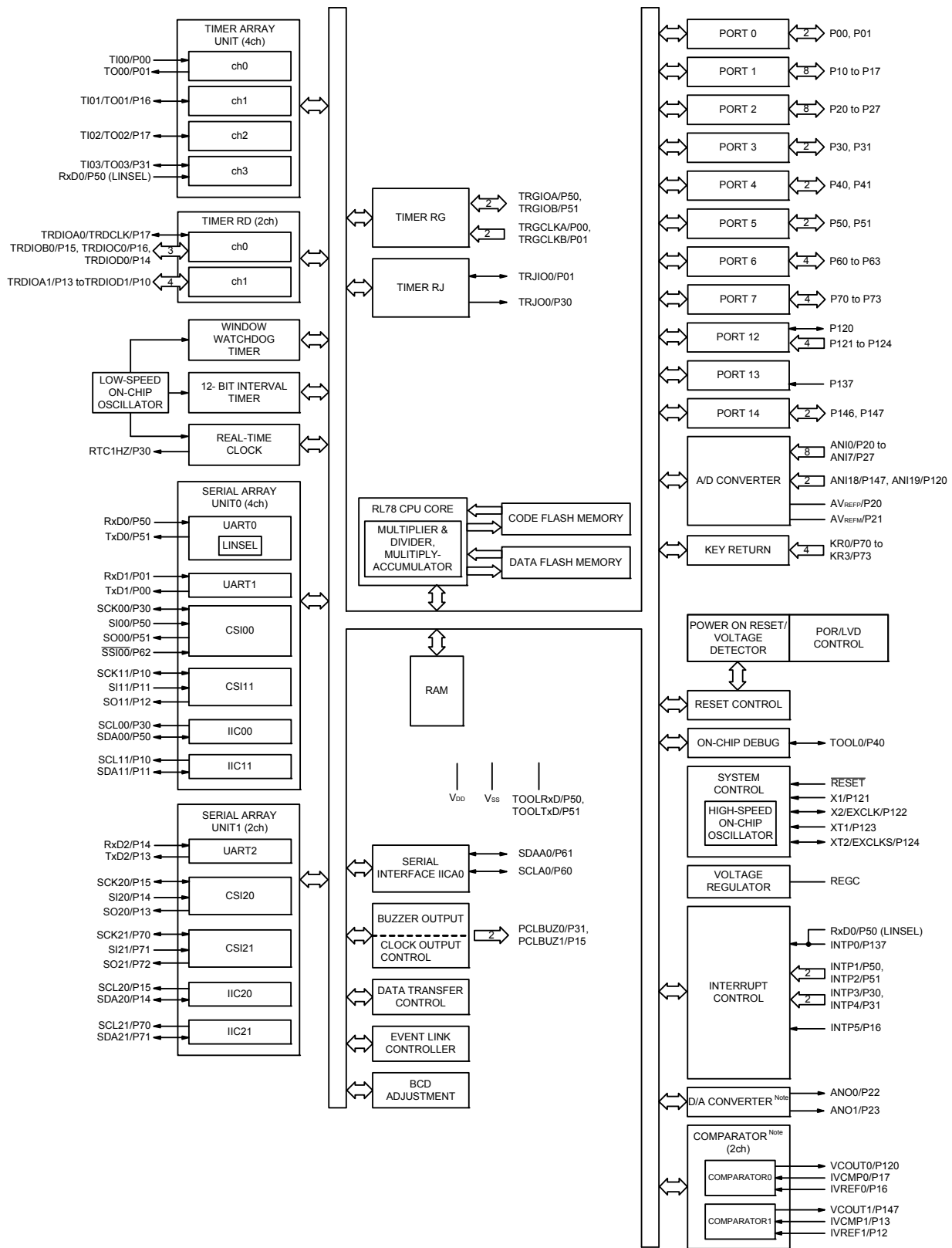
Note Mounted on the 96 KB or more code flash memory products.

1.5.4 40-pin products



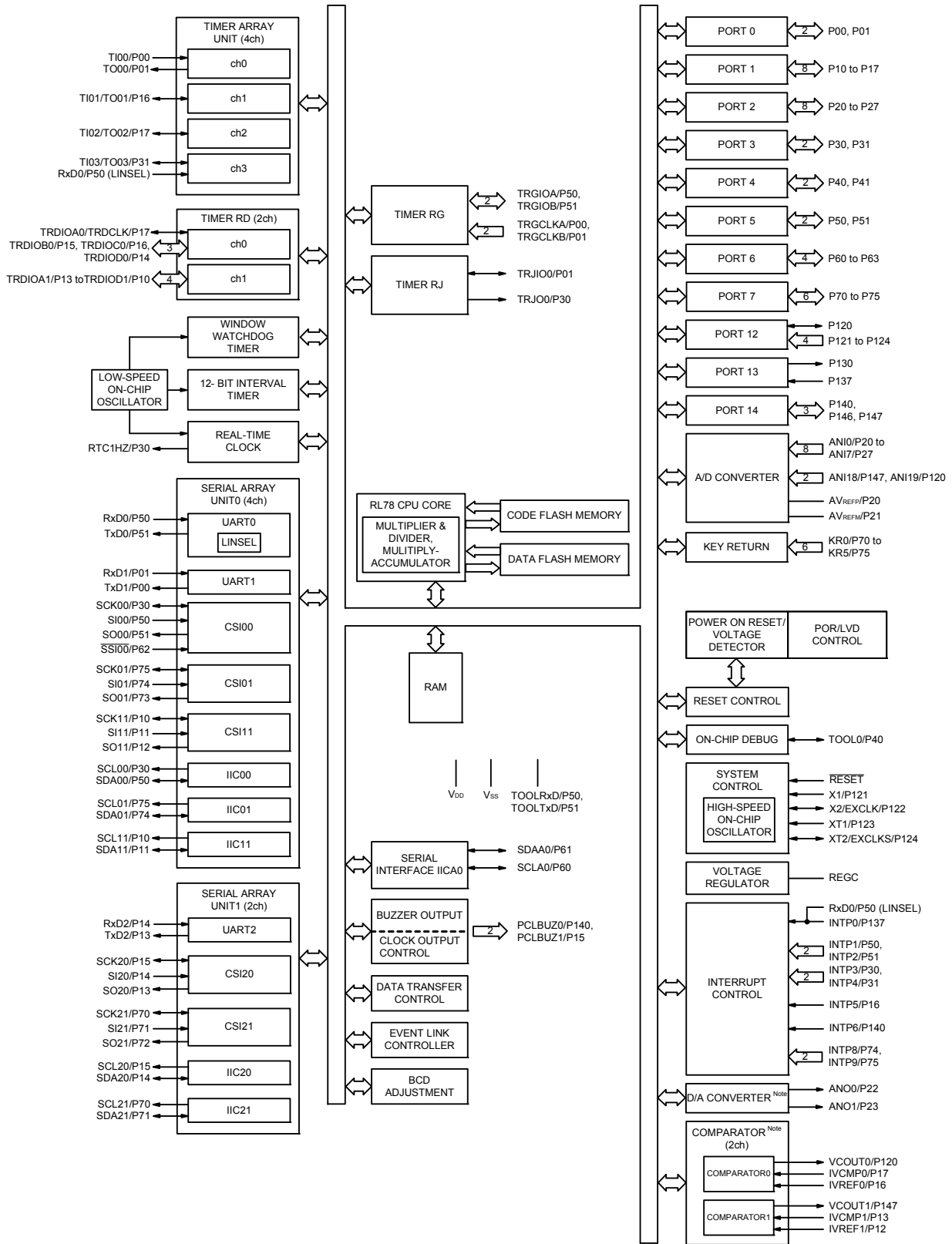
Note Mounted on the 96 KB or more code flash memory products.

1.5.5 44-pin products



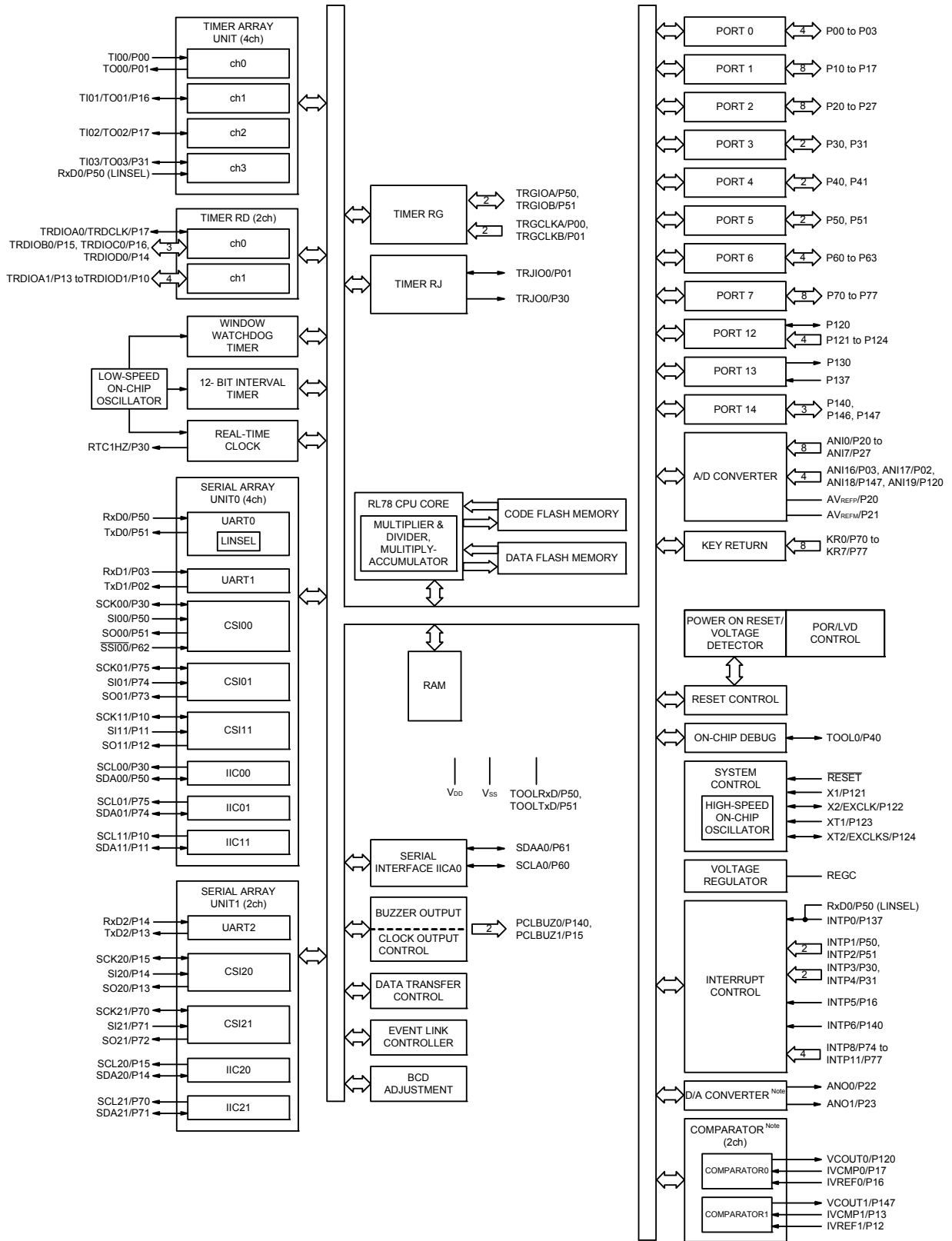
Note Mounted on the 96 KB or more code flash memory products.

1.5.6 48-pin products



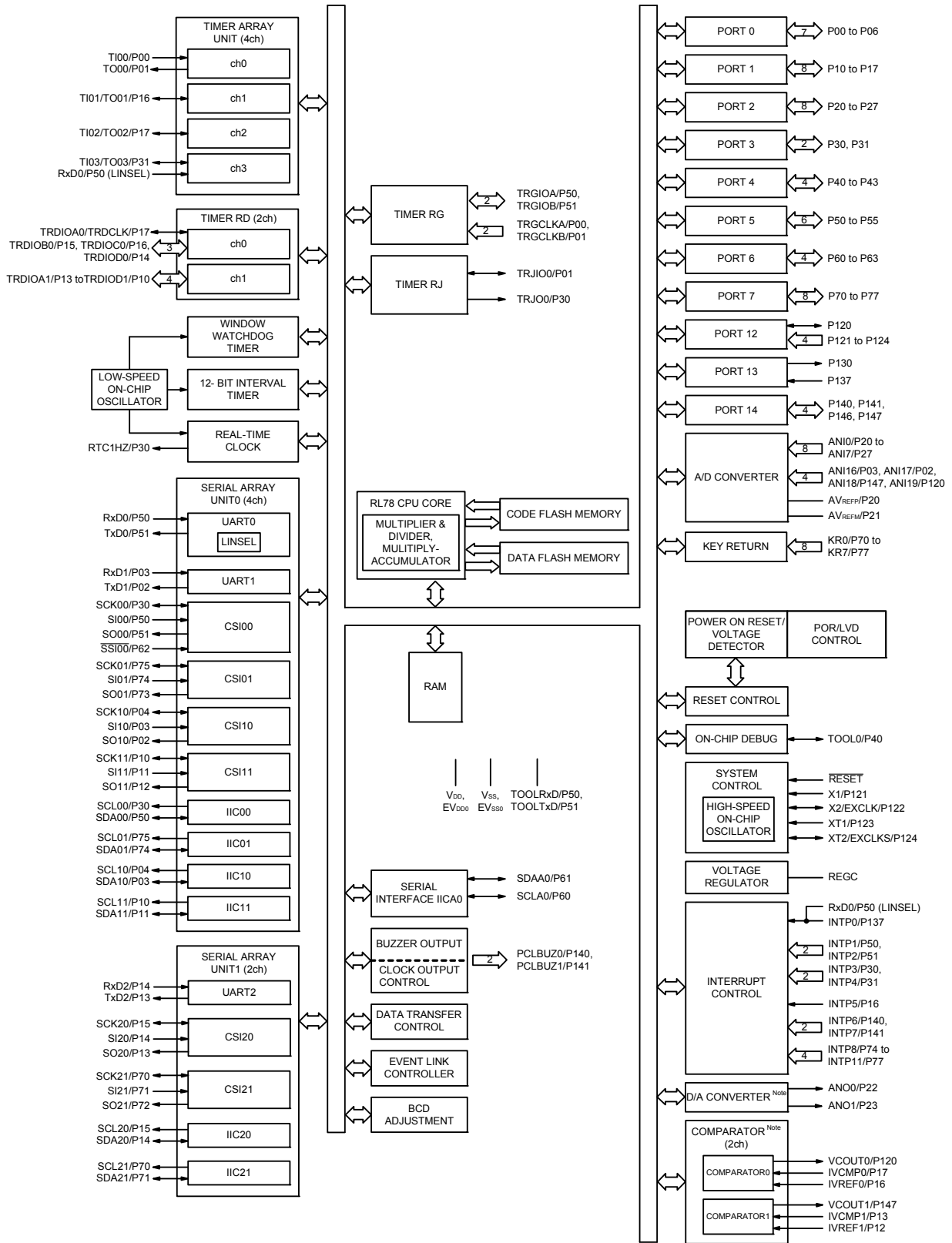
Note Mounted on the 96 KB or more code flash memory products.

1.5.7 52-pin products



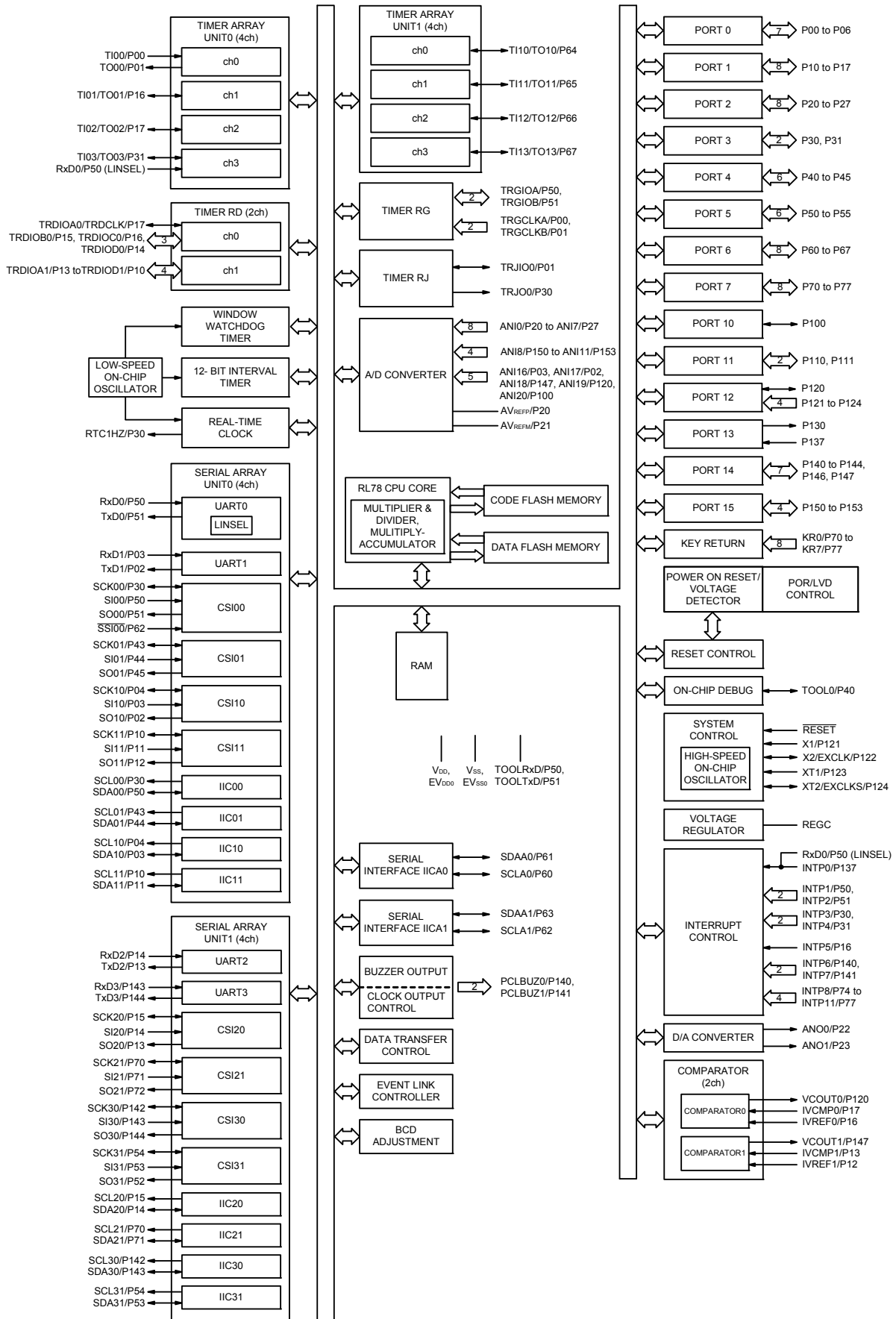
Note Mounted on the 96 KB or more code flash memory products.

1.5.8 64-pin products

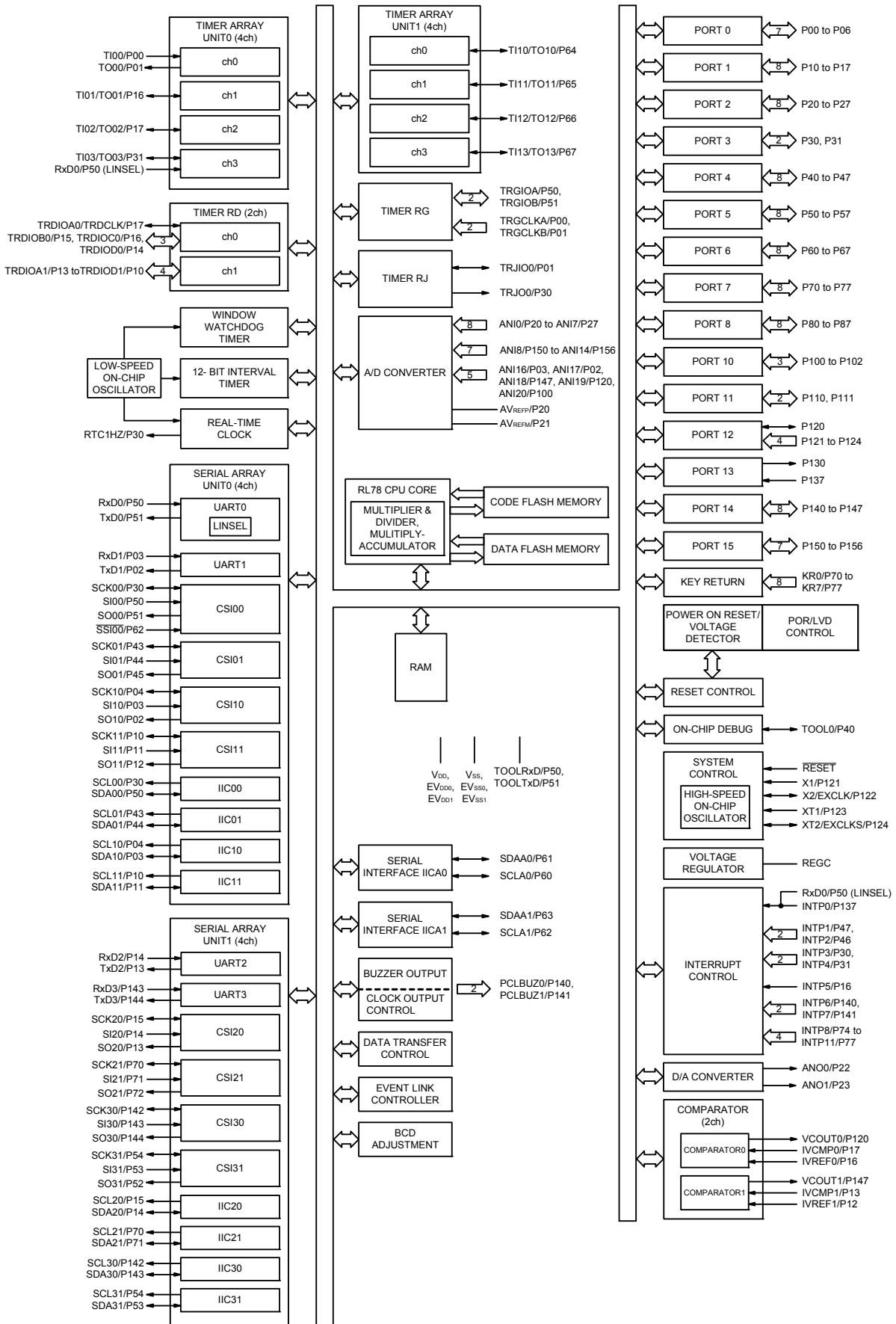


Note Mounted on the 96 KB or more code flash memory products.

1.5.9 80-pin products



1.5.10 100-pin products



1.6 Outline of Functions

[30-pin, 32-pin, 36-pin, 40-pin products (code flash memory 16 KB to 64 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item	30-pin		32-pin		36-pin		40-pin		
	R5F104Ax (x = A, C to E)		R5F104Bx (x = A, C to E)		R5F104Cx (x = A, C to E)		R5F104Ex (x = A, C to E)		
Code flash memory (KB)		16 to 64		16 to 64		16 to 64		16 to 64	
Data flash memory (KB)		4		4		4		4	
RAM (KB)		2.5 to 5.5 Note		2.5 to 5.5 Note		2.5 to 5.5 Note		2.5 to 5.5 Note	
Address space		1 MB							
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)							
	High-speed on-chip oscillator clock (f _{IH})	HS (high-speed main) mode: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)							
Subsystem clock		—						XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz	
Low-speed on-chip oscillator clock		15 kHz (TYP.): V _{DD} = 1.6 to 5.5 V							
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)							
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f _{IH} = 32 MHz operation)							
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)							
		—						30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)	
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 							
I/O port	Total	26		28		32		36	
	CMOS I/O	21		22		26		28	
	CMOS input	3		3		3		5	
	CMOS output	—		—		—		—	
	N-ch open-drain I/O (6 V tolerance)	2		3		3		3	
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)							
	Watchdog timer	1 channel							
	Real-time clock (RTC)	1 channel							
	12-bit interval timer	1 channel							
	Timer output	Timer outputs: 13 channels PWM outputs: 9 channels							
	RTC output	—						1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)	

(Note is listed on the next page.)

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xD (x = A to C, E to G, J, L): Start address FE900H
R5F104xE (x = A to C, E to G, J, L): Start address FE900H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

(2/2)

Item	30-pin	32-pin	36-pin	40-pin
	R5F104Ax (x = A, C to E)	R5F104Bx (x = A, C to E)	R5F104Cx (x = A, C to E)	R5F104Ex (x = A, C to E)
Clock output/buzzer output	2	2	2	2
	[30-pin, 32-pin, 36-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) [40-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)			
8/10-bit resolution A/D converter	8 channels	8 channels	8 channels	9 channels
Serial interface	[30-pin, 32-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel [36-pin, 40-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I ² C: 2 channels			
I ² C bus	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)	28 sources			29 sources
Event link controller (ELC)	Event input: 19 Event trigger output: 7			Event input: 20 Event trigger output: 7
Vectored interrupt sources	Internal	24	24	24
	External	6	6	7
Key interrupt	—	—	—	4
Reset	<ul style="list-style-type: none"> • Reset by \overline{RESET} pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access 			
Power-on-reset circuit	<ul style="list-style-type: none"> • Power-on-reset: 1.51 ±0.04 V ($T_A = -40$ to +85°C) 1.51 ±0.06 V ($T_A = -40$ to +105°C) • Power-down-reset: 1.50 ±0.04 V ($T_A = -40$ to +85°C) 1.50 ±0.06 V ($T_A = -40$ to +105°C) 			
Voltage detector	1.63 V to 4.06 V (14 stages)			
On-chip debug function	Provided			
Power supply voltage	$V_{DD} = 1.6$ to 5.5 V ($T_A = -40$ to +85°C) $V_{DD} = 2.4$ to 5.5 V ($T_A = -40$ to +105°C)			
Operating ambient temperature	$T_A = -40$ to +85°C (A: Consumer applications, D: Industrial applications), $T_A = -40$ to +105°C (G: Industrial applications)			

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

[30-pin, 32-pin, 36-pin, 40-pin products (code flash memory 96 KB to 256 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		30-pin	32-pin	36-pin	40-pin
		R5F104Ax (x = F, G)	R5F104Bx (x = F, G)	R5F104Cx (x = F, G)	R5F104Ex (x = F to H)
Code flash memory (KB)		96 to 128	96 to 128	96 to 128	96 to 192
Data flash memory (KB)		8	8	8	8
RAM (KB)		12 to 16 Note	12 to 16 Note	12 to 16 Note	12 to 20 Note
Address space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)			
	High-speed on-chip oscillator clock (f _{IH})	HS (high-speed main) mode: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)			
Subsystem clock		—			XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz
Low-speed on-chip oscillator clock		15 kHz (TYP.); V _{DD} = 1.6 to 5.5 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f _{IH} = 32 MHz operation)			
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)			
		—			30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 			
I/O port	Total	26	28	32	36
	CMOS I/O	21	22	26	28
	CMOS input	3	3	3	5
	CMOS output	—	—	—	—
	N-ch open-drain I/O (6 V tolerance)	2	3	3	3
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel			
	12-bit interval timer	1 channel			
	Timer output	Timer outputs: 13 channels PWM outputs: 9 channels			
	RTC output	—			1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)

(Note is listed on the next page.)

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

(2/2)

Item	30-pin	32-pin	36-pin	40-pin
	R5F104Ax (x = F, G)	R5F104Bx (x = F, G)	R5F104Cx (x = F, G)	R5F104Ex (x = F to H)
Clock output/buzzer output	2	2	2	2
	[30-pin, 32-pin, 36-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) [40-pin products] • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)			
8/10-bit resolution A/D converter	8 channels	8 channels	8 channels	9 channels
D/A converter	1 channel	2 channels		
Comparator	2 channels			
Serial interface	[30-pin, 32-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel [36-pin, 40-pin products] • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I ² C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I ² C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I ² C: 2 channels			
	I ² C bus	1 channel	1 channel	1 channel
Data transfer controller (DTC)	30 sources			31 sources
Event link controller (ELC)	Event input: 21 Event trigger output: 8	Event input: 21, Event trigger output: 9		Event input: 22 Event trigger output: 9
Vectored interrupt sources	Internal	24	24	24
	External	6	6	7
Key interrupt	—	—	—	4
Reset	<ul style="list-style-type: none"> Reset by \overline{RESET} pin Internal reset by watchdog timer Internal reset by power-on-reset Internal reset by voltage detector Internal reset by illegal instruction execution ^{Note} Internal reset by RAM parity error Internal reset by illegal-memory access 			
Power-on-reset circuit	<ul style="list-style-type: none"> Power-on-reset: 1.51 ±0.04 V ($T_A = -40$ to +85°C) 1.51 ±0.06 V ($T_A = -40$ to +105°C) Power-down-reset: 1.50 ±0.04 V ($T_A = -40$ to +85°C) 1.50 ±0.06 V ($T_A = -40$ to +105°C) 			
Voltage detector	1.63 V to 4.06 V (14 stages)			
On-chip debug function	Provided			
Power supply voltage	$V_{DD} = 1.6$ to 5.5 V ($T_A = -40$ to +85°C) $V_{DD} = 2.4$ to 5.5 V ($T_A = -40$ to +105°C)			
Operating ambient temperature	$T_A = -40$ to +85°C (A: Consumer applications, D: Industrial applications), $T_A = -40$ to +105°C (G: Industrial applications)			

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution not is issued by emulation with the in-circuit emulator or on-chip debug emulator.

[44-pin, 48-pin, 52-pin, 64-pin products (code flash memory 16 KB to 64 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		44-pin	48-pin	52-pin	64-pin
		R5F104Fx (x = A, C to E)	R5F104Gx (x = A, C to E)	R5F104Jx (x = C to E)	R5F104Lx (x = C to E)
Code flash memory (KB)		16 to 64	16 to 64	32 to 64	32 to 64
Data flash memory (KB)		4	4	4	4
RAM (KB)		2.5 to 5.5 Note	2.5 to 5.5 Note	4 to 5.5 Note	4 to 5.5 Note
Address space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)			
	High-speed on-chip oscillator clock (f _{IH})	HS (high-speed main) mode: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)			
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz			
Low-speed on-chip oscillator clock		15 kHz (TYP.): V _{DD} = 1.6 to 5.5 V			
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)			
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f _{IH} = 32 MHz operation)			
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)			
		30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)			
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 			
I/O port	Total	40	44	48	58
	CMOS I/O	31	34	38	48
	CMOS input	5	5	5	5
	CMOS output	—	1	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4	4	4
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel			
	12-bit interval timer	1 channel			
	Timer output	Timer outputs: 13 channels PWM outputs: 9 channels			
	RTC output	1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)			

(Note is listed on the next page.)

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xD (x = A to C, E to G, J, L): Start address FE900H
R5F104xE (x = A to C, E to G, J, L): Start address FE900H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

(2/2)

Item	44-pin	48-pin	52-pin	64-pin
	R5F104Fx (x = A, C to E)	R5F104Gx (x = A, C to E)	R5F104Jx (x = C to E)	R5F104Lx (x = C to E)
Clock output/buzzer output	2	2	2	2
	<ul style="list-style-type: none"> • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation) 			
8/10-bit resolution A/D converter	10 channels	10 channels	12 channels	12 channels
Serial interface	<p>[44-pin products]</p> <ul style="list-style-type: none"> • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels <p>[48-pin, 52-pin products]</p> <ul style="list-style-type: none"> • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels • CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels <p>[64-pin products]</p> <ul style="list-style-type: none"> • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels 			
	I ² C bus	1 channel	1 channel	1 channel
Data transfer controller (DTC)	29 sources	30 sources		31 sources
Event link controller (ELC)	Event input: 20 Event trigger output: 7			
Vectored interrupt sources	Internal	24	24	24
	External	7	10	13
Key interrupt	4	6	8	8
Reset	<ul style="list-style-type: none"> • Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access 			
Power-on-reset circuit	<ul style="list-style-type: none"> • Power-on-reset: 1.51 ±0.04 V (T_A = -40 to +85°C) 1.51 ±0.06 V (T_A = -40 to +105°C) • Power-down-reset: 1.50 ±0.04 V (T_A = -40 to +85°C) 1.50 ±0.06 V (T_A = -40 to +105°C) 			
Voltage detector	1.63 V to 4.06 V (14 stages)			
On-chip debug function	Provided			
Power supply voltage	V _{DD} = 1.6 to 5.5 V (T _A = -40 to +85°C) V _{DD} = 2.4 to 5.5 V (T _A = -40 to +105°C)			
Operating ambient temperature	T _A = -40 to +85°C (A: Consumer applications, D: Industrial applications), T _A = -40 to +105°C (G: Industrial applications)			

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[44-pin, 48-pin, 52-pin, 64-pin products (code flash memory 96 KB to 256 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		44-pin	48-pin	52-pin	64-pin
		R5F104Fx (x = F to H, J)	R5F104Gx (x = F to H, J)	R5F104Jx (x = F to H, J)	R5F104Lx (x = F to H, J)
Code flash memory (KB)		96 to 256	96 to 256	96 to 256	96 to 256
Data flash memory (KB)		8	8	8	8
RAM (KB)		12 to 24 Note	12 to 24 Note	12 to 24 Note	12 to 24 Note
Address space		1 MB			
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)			
	High-speed on-chip oscillator clock (f_{IH})	HS (high-speed main) mode: 1 to 32 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)			
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz			
Low-speed on-chip oscillator clock		15 kHz (TYP.): $V_{DD} = 1.6$ to 5.5 V			
General-purpose register		8 bits \times 32 registers (8 bits \times 8 registers \times 4 banks)			
Minimum instruction execution time		0.03125 μ s (High-speed on-chip oscillator clock: $f_{IH} = 32$ MHz operation)			
		0.05 μ s (High-speed system clock: $f_{MX} = 20$ MHz operation)			
		30.5 μ s (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)			
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits \times 8 bits, 16 bits \times 16 bits), Division (16 bits \div 16 bits, 32 bits \div 32 bits) • Multiplication and Accumulation (16 bits \times 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 			
I/O port	Total	40	44	48	58
	CMOS I/O	31	34	38	48
	CMOS input	5	5	5	5
	CMOS output	—	1	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4	4	4
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)			
	Watchdog timer	1 channel			
	Real-time clock (RTC)	1 channel			
	12-bit interval timer	1 channel			
	Timer output	Timer outputs: 14 channels PWM outputs: 9 channels			
	RTC output	1 • 1 Hz (subsystem clock: $f_{SUB} = 32.768$ kHz)			

(Note is listed on the next page.)

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xJ (x = F, G, J, L, M, P): Start address F9F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

(2/2)

Item	44-pin	48-pin	52-pin	64-pin	
	R5F104Fx (x = F to H, J)	R5F104Gx (x = F to H, J)	R5F104Jx (x = F to H, J)	R5F104Lx (x = F to H, J)	
Clock output/buzzer output	2	2	2	2	
	<ul style="list-style-type: none"> • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation) 				
8/10-bit resolution A/D converter	10 channels	10 channels	12 channels	12 channels	
D/A converter	2 channels				
Comparator	2 channels				
Serial interface	[44-pin products] <ul style="list-style-type: none"> • CSI: 1 channel/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 1 channel • CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels [48-pin, 52-pin products] <ul style="list-style-type: none"> • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels • CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels [64-pin products] <ul style="list-style-type: none"> • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels 				
	I ² C bus	1 channel	1 channel	1 channel	1 channel
Data transfer controller (DTC)	31 sources	32 sources		33 sources	
Event link controller (ELC)	Event input: 22 Event trigger output: 9				
Vectored interrupt sources	Internal	24	24	24	24
	External	7	10	12	13
Key interrupt	4	6	8	8	
Reset	<ul style="list-style-type: none"> • Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access 				
Power-on-reset circuit	<ul style="list-style-type: none"> • Power-on-reset: 1.51 ±0.04 V (T_A = -40 to +85°C) 1.51 ±0.06 V (T_A = -40 to +105°C) • Power-down-reset: 1.50 ±0.04 V (T_A = -40 to +85°C) 1.50 ±0.06 V (T_A = -40 to +105°C) 				
Voltage detector	1.63 V to 4.06 V (14 stages)				
On-chip debug function	Provided				
Power supply voltage	V _{DD} = 1.6 to 5.5 V (T _A = -40 to +85°C) V _{DD} = 2.4 to 5.5 V (T _A = -40 to +105°C)				
Operating ambient temperature	T _A = -40 to +85°C (A: Consumer applications, D: Industrial applications), T _A = -40 to +105°C (G: Industrial applications)				

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[48-pin, 64-pin products (code flash memory 384 KB to 512 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		48-pin	64-pin
		R5F104Gx (x = K, L)	R5F104Lx (x = K, L)
Code flash memory (KB)		384 to 512	384 to 512
Data flash memory (KB)		8	8
RAM (KB)		32 to 48 Note	32 to 48 Note
Address space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)	
	High-speed on-chip oscillator clock (f _{IH})	HS (high-speed main) mode: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)	
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz	
Low-speed on-chip oscillator clock		15 kHz (TYP.): V _{DD} = 1.6 to 5.5 V	
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f _{IH} = 32 MHz operation)	
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)	
		30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)	
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 	
I/O port	Total	44	58
	CMOS I/O	34	48
	CMOS input	5	5
	CMOS output	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4
Timer	16-bit timer	8 channels (TAU: 4 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)	
	Watchdog timer	1 channel	
	Real-time clock (RTC)	1 channel	
	12-bit interval timer	1 channel	
	Timer output	Timer outputs: 14 channels PWM outputs: 9 channels	
	RTC output	1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)	

(Note is listed on the next page.)

Note The flash library uses RAM in self-programming and rewriting of the data flash memory.
The target products and start address of the RAM areas used by the flash library are shown below.
R5F104xL (x = G, L, M, P): Start address F3F00H
For the RAM areas used by the flash library, see **Self RAM list of Flash Self-Programming Library for RL78 Family (R20UT2944)**.

(2/2)

Item	48-pin		64-pin	
	R5F104Gx (x = K, L)		R5F104Lx (x = K, L)	
Clock output/buzzer output	2		2	
	<ul style="list-style-type: none"> • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB} = 32.768$ kHz operation) 			
8/10-bit resolution A/D converter	10 channels		12 channels	
D/A converter	2 channels			
Comparator	2 channels			
Serial interface	[48-pin products] <ul style="list-style-type: none"> • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels • CSI: 1 channel/UART: 1 channel/simplified I²C: 1 channel • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels [64-pin products] <ul style="list-style-type: none"> • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels 			
	I ² C bus	1 channel		1 channel
Data transfer controller (DTC)	32 sources		33 sources	
Event link controller (ELC)	Event input: 22 Event trigger output: 9			
Vectored interrupt sources	Internal	24		24
	External	10		13
Key interrupt	6		8	
Reset	<ul style="list-style-type: none"> • Reset by \overline{RESET} pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access 			
Power-on-reset circuit	<ul style="list-style-type: none"> • Power-on-reset: 1.51 \pm0.04 V ($T_A = -40$ to $+85^\circ\text{C}$) 1.51 \pm0.06 V ($T_A = -40$ to $+105^\circ\text{C}$) • Power-down-reset: 1.50 \pm0.04 V ($T_A = -40$ to $+85^\circ\text{C}$) 1.50 \pm0.06 V ($T_A = -40$ to $+105^\circ\text{C}$) 			
Voltage detector	1.63 V to 4.06 V (14 stages)			
On-chip debug function	Provided			
Power supply voltage	$V_{DD} = 1.6$ to 5.5 V ($T_A = -40$ to $+85^\circ\text{C}$) $V_{DD} = 2.4$ to 5.5 V ($T_A = -40$ to $+105^\circ\text{C}$)			
Operating ambient temperature	$T_A = -40$ to $+85^\circ\text{C}$ (A: Consumer applications, D: Industrial applications), $T_A = -40$ to $+105^\circ\text{C}$ (G: Industrial applications)			

Note The illegal instruction is generated when instruction code FFH is executed.
 Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[80-pin, 100-pin products (code flash memory 96 KB to 256 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		80-pin	100-pin
		R5F104Mx (x = F to H, J)	R5F104Px (x = F to H, J)
Code flash memory (KB)		96 to 256	96 to 256
Data flash memory (KB)		8	8
RAM (KB)		12 to 24 Note	12 to 24 Note
Address space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)	
	High-speed on-chip oscillator clock (f_{IH})	HS (high-speed main) mode: 1 to 32 MHz ($V_{DD} = 2.7$ to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz ($V_{DD} = 2.4$ to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz ($V_{DD} = 1.8$ to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz ($V_{DD} = 1.6$ to 5.5 V)	
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz	
Low-speed on-chip oscillator clock		15 kHz (TYP.): $V_{DD} = 1.6$ to 5.5 V	
General-purpose register		8 bits \times 32 registers (8 bits \times 8 registers \times 4 banks)	
Minimum instruction execution time		0.03125 μ s (High-speed on-chip oscillator clock: $f_{IH} = 32$ MHz operation)	
		0.05 μ s (High-speed system clock: $f_{MX} = 20$ MHz operation)	
		30.5 μ s (Subsystem clock: $f_{SUB} = 32.768$ kHz operation)	
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits \times 8 bits, 16 bits \times 16 bits), Division (16 bits \div 16 bits, 32 bits \div 32 bits) • Multiplication and Accumulation (16 bits \times 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 	
I/O port	Total	74	92
	CMOS I/O	64	82
	CMOS input	5	5
	CMOS output	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4
Timer	16-bit timer	12 channels (TAU: 8 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)	
	Watchdog timer	1 channel	
	Real-time clock (RTC)	1 channel	
	12-bit interval timer	1 channel	
	Timer output	Timer outputs: 18 channels PWM outputs: 12 channels	
	RTC output	1 • 1 Hz (subsystem clock: $f_{SUB} = 32.768$ kHz)	

Note In the case of the 24 KB, this is about 23 KB when the self-programming function and data flash function are used (For details, see **CHAPTER 3** in the RL78/G14 User's Manual).

(2/2)

Item	80-pin		100-pin	
	R5F104Mx (x = F to H, J)		R5F104Px (x = F to H, J)	
Clock output/buzzer output	2		2	
	<ul style="list-style-type: none"> • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: f_{MAIN} = 20 MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: f_{SUB} = 32.768 kHz operation) 			
8/10-bit resolution A/D converter	17 channels		20 channels	
D/A converter	2 channels		2 channels	
Comparator	2 channels		2 channels	
Serial interface	[80-pin, 100-pin products]			
	<ul style="list-style-type: none"> • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels 			
I ² C bus	2 channels		2 channels	
Data transfer controller (DTC)	39 sources		39 sources	
Event link controller (ELC)	Event input: 26 Event trigger output: 9			
Vectored interrupt sources	Internal	32		32
	External	13		13
Key interrupt	8		8	
Reset	<ul style="list-style-type: none"> • Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access 			
Power-on-reset circuit	<ul style="list-style-type: none"> • Power-on-reset: 1.51 ±0.04 V (T_A = -40 to +85°C) 1.51 ±0.06 V (T_A = -40 to +105°C) • Power-down-reset: 1.50 ±0.04 V (T_A = -40 to +85°C) 1.50 ±0.06 V (T_A = -40 to +105°C) 			
Voltage detector	1.63 V to 4.06 V (14 stages)			
On-chip debug function	Provided			
Power supply voltage	V _{DD} = 1.6 to 5.5 V (T _A = -40 to +85°C) V _{DD} = 2.4 to 5.5 V (T _A = -40 to +105°C)			
Operating ambient temperature	T _A = -40 to +85°C (A: Consumer applications, D: Industrial applications), T _A = -40 to +105°C (G: Industrial applications)			

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

[80-pin, 100-pin products (code flash memory 384 KB to 512 KB)]

Caution This outline describes the functions at the time when Peripheral I/O redirection register 0, 1 (PIOR0, 1) are set to 00H.

(1/2)

Item		80-pin	100-pin
		R5F104Mx (x = K, L)	R5F104Px (x = K, L)
Code flash memory (KB)		384 to 512	384 to 512
Data flash memory (KB)		8	8
RAM (KB)		32 to 48 Note	32 to 48 Note
Address space		1 MB	
Main system clock	High-speed system clock	X1 (crystal/ceramic) oscillation, external main system clock input (EXCLK) HS (high-speed main) mode: 1 to 20 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)	
	High-speed on-chip oscillator clock (f _{IH})	HS (high-speed main) mode: 1 to 32 MHz (V _{DD} = 2.7 to 5.5 V), HS (high-speed main) mode: 1 to 16 MHz (V _{DD} = 2.4 to 5.5 V), LS (low-speed main) mode: 1 to 8 MHz (V _{DD} = 1.8 to 5.5 V), LV (low-voltage main) mode: 1 to 4 MHz (V _{DD} = 1.6 to 5.5 V)	
Subsystem clock		XT1 (crystal) oscillation, external subsystem clock input (EXCLKS) 32.768 kHz	
Low-speed on-chip oscillator clock		15 kHz (TYP.): V _{DD} = 1.6 to 5.5 V	
General-purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)	
Minimum instruction execution time		0.03125 μs (High-speed on-chip oscillator clock: f _{IH} = 32 MHz operation)	
		0.05 μs (High-speed system clock: f _{MX} = 20 MHz operation)	
		30.5 μs (Subsystem clock: f _{SUB} = 32.768 kHz operation)	
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), Division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (Set, reset, test, and Boolean operation), etc. 	
I/O port	Total	74	92
	CMOS I/O	64	82
	CMOS input	5	5
	CMOS output	1	1
	N-ch open-drain I/O (6 V tolerance)	4	4
Timer	16-bit timer	12 channels (TAU: 8 channels, Timer RJ: 1 channel, Timer RD: 2 channels, Timer RG: 1 channel)	
	Watchdog timer	1 channel	
	Real-time clock (RTC)	1 channel	
	12-bit interval timer	1 channel	
	Timer output	Timer outputs: 18 channels PWM outputs: 12 channels	
	RTC output	1 • 1 Hz (subsystem clock: f _{SUB} = 32.768 kHz)	

Note In the case of the 48 KB, this is about 47 KB when the self-programming function and data flash function are used (For details, see **CHAPTER 3** in the RL78/G14 User's Manual).

(2/2)

Item	80-pin		100-pin	
	R5F104Mx (x = K, L)		R5F104Px (x = K, L)	
Clock output/buzzer output	2		2	
	<ul style="list-style-type: none"> • 2.44 kHz, 4.88 kHz, 9.76 kHz, 1.25 MHz, 2.5 MHz, 5 MHz, 10 MHz (Main system clock: $f_{MAIN} = 20$ MHz operation) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (Subsystem clock: $f_{SUB} = 32.768$ kHz operation) 			
8/10-bit resolution A/D converter	17 channels		20 channels	
D/A converter	2 channels		2 channels	
Comparator	2 channels		2 channels	
Serial interface	[80-pin, 100-pin products]			
	<ul style="list-style-type: none"> • CSI: 2 channels/UART (UART supporting LIN-bus): 1 channel/simplified I²C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels • CSI: 2 channels/UART: 1 channel/simplified I²C: 2 channels 			
I ² C bus	2 channels		2 channels	
Data transfer controller (DTC)	39 sources		39 sources	
Event link controller (ELC)	Event input: 26 Event trigger output: 9			
Vectored interrupt sources	Internal	32		32
	External	13		13
Key interrupt	8		8	
Reset	<ul style="list-style-type: none"> • Reset by \overline{RESET} pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detector • Internal reset by illegal instruction execution ^{Note} • Internal reset by RAM parity error • Internal reset by illegal-memory access 			
Power-on-reset circuit	<ul style="list-style-type: none"> • Power-on-reset: 1.51 ±0.04 V ($T_A = -40$ to +85°C) 1.51 ±0.06 V ($T_A = -40$ to +105°C) • Power-down-reset: 1.50 ±0.04 V ($T_A = -40$ to +85°C) 1.50 ±0.06 V ($T_A = -40$ to +105°C) 			
Voltage detector	1.63 V to 4.06 V (14 stages)			
On-chip debug function	Provided			
Power supply voltage	V _{DD} = 1.6 to 5.5 V ($T_A = -40$ to +85°C) V _{DD} = 2.4 to 5.5 V ($T_A = -40$ to +105°C)			
Operating ambient temperature	T _A = -40 to +85°C (A: Consumer applications, D: Industrial applications), T _A = -40 to +105°C (G: Industrial applications)			

Note The illegal instruction is generated when instruction code FFH is executed.
Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS (TA = -40 to +85°C)

This chapter describes the following electrical specifications.

Target products A: Consumer applications TA = -40 to +85°C

R5F104xxAxx

D: Industrial applications TA = -40 to +85°C

R5F104xxDxx

G: Industrial applications when TA = -40 to +105°C products is used in the range of TA = -40 to +85°C

R5F104xxGxx

Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. With products not provided with an EVDD0, EVDD1, EVSS0, or EVSS1 pin, replace EVDD0 and EVDD1 with VDD, or replace EVSS0 and EVSS1 with VSS.

Caution 3. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G14 User's Manual.

2.1 Absolute Maximum Ratings

Absolute Maximum Ratings

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Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V _{DD}		-0.5 to +6.5	V
	EV _{DD0} , EV _{DD1}	EV _{DD0} = EV _{DD1}	-0.5 to +6.5	V
	EV _{SS0} , EV _{SS1}	EV _{SS0} = EV _{SS1}	-0.5 to +0.3	V
REGC pin input voltage	V _{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V _{DD} +0.3 Note 1	V
Input voltage	V _{I1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	-0.3 to EV _{DD0} +0.3 and -0.3 to V _{DD} +0.3 Note 2	V
	V _{I2}	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V _{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to V _{DD} +0.3 Note 2	V
Output voltage	V _{O1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-0.3 to EV _{DD0} +0.3 and -0.3 to V _{DD} +0.3 Note 2	V
	V _{O2}	P20 to P27, P150 to P156	-0.3 to V _{DD} +0.3 Note 2	V
Analog input voltage	V _{AI1}	ANI16 to ANI20	-0.3 to EV _{DD0} +0.3 and -0.3 to AV _{REF} (+) +0.3 Notes 2, 3	V
	V _{AI2}	ANI0 to ANI14	-0.3 to V _{DD} +0.3 and -0.3 to AV _{REF} (+) +0.3 Notes 2, 3	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Must be 6.5 V or lower.

Note 3. Do not exceed AV_{REF} (+) + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. AV_{REF} (+): + side reference voltage of the A/D converter.

Remark 3. V_{SS}: Reference voltage

Absolute Maximum Ratings

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Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	-100	mA
	IOH2	Per pin	P20 to P27, P150 to P156	-0.5	mA
		Total of all pins		-2	mA
	Output current, low	IOL1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	40
Total of all pins 170 mA			P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	100	mA
IOL2		Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature		TA	In normal operation mode		-40 to +85
	In flash memory programming mode				
Storage temperature	Tstg			-65 to +150	°C

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.2 Oscillator Characteristics

2.2.1 X1, XT1 characteristics

(TA = -40 to +85°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (fx) ^{Note}	Ceramic resonator/ crystal resonator	2.7 V ≤ VDD ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ VDD < 2.7 V	1.0		16.0	
		1.8 V ≤ VDD < 2.4 V	1.0		8.0	
		1.6 V ≤ VDD < 1.8 V	1.0		4.0	
XT1 clock oscillation frequency (fxT) ^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, refer to **5.4 System Clock Oscillator** in the RL78/G14 User's Manual.

2.2.2 On-chip oscillator characteristics

(TA = -40 to +85°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f _H			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85°C	1.8 V ≤ VDD ≤ 5.5 V	-1.0		+1.0	%
			1.6 V ≤ VDD < 1.8 V	-5.0		+5.0	%
		-40 to -20°C	1.8 V ≤ VDD < 5.5 V	-1.5		+1.5	%
			1.6 V ≤ VDD < 1.8 V	-5.5		+5.5	%
Low-speed on-chip oscillator clock frequency	f _L				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

2.3 DC Characteristics

2.3.1 Pin characteristics

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output current, high ^{Note 1}	IOH1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	1.6 V ≤ EVDD0 ≤ 5.5 V			-10.0 Note 2	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V			-55.0	mA
			2.7 V ≤ EVDD0 < 4.0 V			-10.0	mA
			1.8 V ≤ EVDD0 < 2.7 V			-5.0	mA
			1.6 V ≤ EVDD0 < 1.8 V			-2.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V			-80.0	mA
			2.7 V ≤ EVDD0 < 4.0 V			-19.0	mA
			1.8 V ≤ EVDD0 < 2.7 V			-10.0	mA
			1.6 V ≤ EVDD0 < 1.8 V			-5.0	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	1.6 V ≤ EVDD0 ≤ 5.5 V			-135.0 Note 4	mA
IOH2	Per pin for P20 to P27, P150 to P156	1.6 V ≤ VDD ≤ 5.5 V			-0.1 Note 2	mA	
	Total of all pins (When duty ≤ 70% ^{Note 3})	1.6 V ≤ VDD ≤ 5.5 V			-1.5	mA	

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the EVDD0, EVDD1, VDD pins to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOH × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOH = -10.0 mA

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \approx -8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Note 4. -100 mA for industrial applications (R5F104xxDxx, R5F104xxGxx).

Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output current, low Note 1	IOL1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147			20.0 Note 2	mA	
					15.0 Note 2	mA	
			Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% Note 3)	4.0 V ≤ EVDD0 ≤ 5.5 V		70.0	mA
				2.7 V ≤ EVDD0 < 4.0 V		15.0	mA
		1.8 V ≤ EVDD0 < 2.7 V			9.0	mA	
		1.6 V ≤ EVDD0 < 1.8 V			4.5	mA	
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% Note 3)	4.0 V ≤ EVDD0 ≤ 5.5 V		80.0	mA	
			2.7 V ≤ EVDD0 < 4.0 V		35.0	mA	
			1.8 V ≤ EVDD0 < 2.7 V		20.0	mA	
			1.6 V ≤ EVDD0 < 1.8 V		10.0	mA	
	Total of all pins (When duty ≤ 70% Note 3)				150.0	mA	
	IOL2	Per pin for P20 to P27, P150 to P156			0.4 Note 2	mA	
			Total of all pins (When duty ≤ 70% Note 3)	1.6 V ≤ VDD ≤ 5.5 V		5.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EVSS0, EVSS1, and VSS pins.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \approx 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

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Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	V _{IH1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Normal input buffer	0.8 EVDD0		EVDD0	V
	V _{IH2}	P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	2.2		EVDD0	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	2.0		EVDD0	V
			TTL input buffer 1.6 V ≤ EVDD0 < 3.3 V	1.5		EVDD0	V
	V _{IH3}	P20 to P27, P150 to P156		0.7 VDD		VDD	V
	V _{IH4}	P60 to P63		0.7 EVDD0		6.0	V
V _{IH5}	P121 to P124, P137, EXCLK, EXCLKS, RESET		0.8 VDD		VDD	V	
Input voltage, low	V _{IL1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Normal input buffer	0		0.2 EVDD0	V
	V _{IL2}	P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EVDD0 < 3.3 V	0		0.32	V
	V _{IL3}	P20 to P27, P150 to P156		0		0.3 VDD	V
	V _{IL4}	P60 to P63		0		0.3 EVDD0	V
V _{IL5}	P121 to P124, P137, EXCLK, EXCLKS, RESET		0		0.2 VDD	V	

Caution The maximum value of V_{IH} of pins P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 is EVDD0, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

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Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	VOH1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -10.0 mA	EVDD0 - 1.5		V
			4.0 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -3.0 mA	EVDD0 - 0.7		V
			1.8 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -1.5 mA	EVDD0 - 0.5		V
			1.6 V ≤ EVDD0 < 1.8 V, IOH1 = -1.0 mA	EVDD0 - 0.5		V
	VOH2	P20 to P27, P150 to P156	1.6 V ≤ VDD ≤ 5.5 V, IOH2 = -100 μA	VDD - 0.5		V
Output voltage, low	VOL1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 20.0 mA		1.3	V
			4.0 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 8.5 mA		0.7	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 3.0 mA		0.6	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 1.5 mA		0.4	V
			1.8 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 0.6 mA		0.4	V
			1.6 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 0.3 mA		0.4	V
	VOL2	P20 to P27, P150 to P156	1.6 V ≤ VDD ≤ 5.5 V, IOL2 = 400 μA		0.4	V
	VOL3	P60 to P63	4.0 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 15.0 mA		2.0	V
			4.0 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 5.0 mA		0.4	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 3.0 mA		0.4	V
			1.8 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 2.0 mA		0.4	V
			1.6 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 1.0 mA		0.4	V

Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

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Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Input leakage current, high	ILIH1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Vi = EVDD0			1	μA	
	ILIH2	P20 to P27, P137, P150 to P156, RESET	Vi = VDD			1	μA	
	ILIH3	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	Vi = VDD	In input port or external clock input		1	μA	
			In resonator connection		10	μA		
Input leakage current, low	ILIL1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Vi = EVSS0			-1	μA	
	ILIL2	P20 to P27, P137, P150 to P156, RESET	Vi = VSS			-1	μA	
	ILIL3	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	Vi = VSS	In input port or external clock input		-1	μA	
			In resonator connection		-10	μA		
On-chip pull-up resistance	Ru	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Vi = EVSS0, In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit		
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.4		mA	
						VDD = 3.0 V		2.4			
					fHOCO = 32 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.1		mA
							VDD = 3.0 V		2.1		
			HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V		5.1	8.7	mA	
						VDD = 3.0 V		5.1	8.7		
		fHOCO = 32 MHz, fIH = 32 MHz Note 3		Normal operation	VDD = 5.0 V		4.8	8.1	mA		
					VDD = 3.0 V		4.8	8.1			
		fHOCO = 48 MHz, fIH = 24 MHz Note 3		Normal operation	VDD = 5.0 V		4.0	6.9	mA		
					VDD = 3.0 V		4.0	6.9			
		fHOCO = 24 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V		3.8	6.3	mA			
				VDD = 3.0 V		3.8	6.3				
		fHOCO = 16 MHz, fIH = 16 MHz Note 3	Normal operation	VDD = 5.0 V		2.8	4.6	mA			
				VDD = 3.0 V		2.8	4.6				
		LS (low-speed main) mode Note 5	fHOCO = 8 MHz, fIH = 8 MHz Note 3	Normal operation	VDD = 3.0 V		1.3	2.0	mA		
					VDD = 2.0 V		1.3	2.0			
		LV (low-voltage main) mode Note 5	fHOCO = 4 MHz, fIH = 4 MHz Note 3	Normal operation	VDD = 3.0 V		1.3	1.8	mA		
					VDD = 2.0 V		1.3	1.8			
		HS (high-speed main) mode Note 5	fMX = 20 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		3.3	5.3	mA		
					Resonator connection		3.4	5.5			
				Normal operation	Square wave input		3.3	5.3	mA		
					Resonator connection		3.4	5.5			
			fMX = 10 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		2.0	3.1	mA		
					Resonator connection		2.1	3.2			
Normal operation	Square wave input				2.0	3.1	mA				
	Resonator connection				2.1	3.2					
LS (low-speed main) mode Note 5	fMX = 8 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		1.2	1.9	mA				
			Resonator connection		1.2	2.0					
	Normal operation	Square wave input		1.2	1.9	mA					
		Resonator connection		1.2	2.0						
Subsystem clock operation	fSUB = 32.768 kHz Note 4 TA = -40°C	Normal operation	Square wave input		4.7	6.1	μA				
			Resonator connection		4.7	6.1					
	Normal operation	Square wave input		4.7	6.1	μA					
		Resonator connection		4.7	6.1						
	Normal operation	Square wave input		4.8	6.7	μA					
		Resonator connection		4.8	6.7						
Normal operation	Square wave input		4.8	7.5	μA						
	Resonator connection		4.8	7.5							
Normal operation	Square wave input		5.4	8.9	μA						
	Resonator connection		5.4	8.9							

(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 3.** When high-speed system clock and subsystem clock are stopped.
- Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
- | | |
|-----------------------------|---|
| HS (high-speed main) mode: | 2.7 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 32 MHz |
| | 2.4 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 16 MHz |
| LS (low-speed main) mode: | 1.8 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 8 MHz |
| LV (low-voltage main) mode: | 1.6 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 4 MHz |
- Remark 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is T_A = 25°C

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)(2/2)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit		
Supply current Note 1	I _{DD2} Note 2	HALT mode Note 7	HS (high-speed main) mode Note 7	f _{HOCO} = 64 MHz, f _{IH} = 32 MHz Note 4	V _{DD} = 5.0 V		0.80	3.09	mA
					V _{DD} = 3.0 V		0.80	3.09	
				f _{HOCO} = 32 MHz, f _{IH} = 32 MHz Note 4	V _{DD} = 5.0 V		0.49	2.40	
					V _{DD} = 3.0 V		0.49	2.40	
				f _{HOCO} = 48 MHz, f _{IH} = 24 MHz Note 4	V _{DD} = 5.0 V		0.62	2.40	
					V _{DD} = 3.0 V		0.62	2.40	
			f _{HOCO} = 24 MHz, f _{IH} = 24 MHz Note 4	V _{DD} = 5.0 V		0.4	1.83		
				V _{DD} = 3.0 V		0.4	1.83		
			f _{HOCO} = 16 MHz, f _{IH} = 16 MHz Note 4	V _{DD} = 5.0 V		0.37	1.38		
				V _{DD} = 3.0 V		0.37	1.38		
			LS (low-speed main) mode Note 7	f _{HOCO} = 8 MHz, f _{IH} = 8 MHz Note 4	V _{DD} = 3.0 V		260	710	μA
					V _{DD} = 2.0 V		260	710	
			LV (low-voltage main) mode Note 7	f _{HOCO} = 4 MHz, f _{IH} = 4 MHz Note 4	V _{DD} = 3.0 V		420	700	μA
					V _{DD} = 2.0 V		420	700	
			HS (high-speed main) mode Note 7	f _{MX} = 20 MHz Note 3, V _{DD} = 5.0 V	Square wave input		0.28	1.55	mA
					Resonator connection		0.40	1.74	
				f _{MX} = 20 MHz Note 3, V _{DD} = 3.0 V	Square wave input		0.28	1.55	
					Resonator connection		0.40	1.74	
				f _{MX} = 10 MHz Note 3, V _{DD} = 5.0 V	Square wave input		0.19	0.86	
					Resonator connection		0.25	0.93	
				f _{MX} = 10 MHz Note 3, V _{DD} = 3.0 V	Square wave input		0.19	0.86	
					Resonator connection		0.25	0.93	
			LS (low-speed main) mode Note 7	f _{MX} = 8 MHz Note 3, V _{DD} = 3.0 V	Square wave input		95	550	μA
					Resonator connection		140	590	
				f _{MX} = 8 MHz Note 3, V _{DD} = 2.0 V	Square wave input		95	550	
					Resonator connection		140	590	
			Subsystem clock operation	f _{SUB} = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.25	0.57	μA
					Resonator connection		0.44	0.76	
				f _{SUB} = 32.768 kHz Note 5, TA = +25°C	Square wave input		0.30	0.57	
					Resonator connection		0.49	0.76	
f _{SUB} = 32.768 kHz Note 5, TA = +50°C	Square wave input			0.36	1.17				
	Resonator connection			0.59	1.36				
f _{SUB} = 32.768 kHz Note 5, TA = +70°C	Square wave input			0.49	1.97				
	Resonator connection			0.72	2.16				
f _{SUB} = 32.768 kHz Note 5, TA = +85°C	Square wave input		0.97	3.37					
	Resonator connection		1.16	3.56					
I _{DD3} Note 6	STOP mode Note 8	TA = -40°C		0.18	0.51	μA			
		TA = +25°C		0.24	0.51				
		TA = +50°C		0.29	1.10				
		TA = +70°C		0.41	1.90				
		TA = +85°C		0.90	3.30				

(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** During HALT instruction execution by flash memory.
- Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 4.** When high-speed system clock and subsystem clock are stopped.
- Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
- HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
 2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
- LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
- LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz
- Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is TA = 25°C

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit		
Supply current Note 1	I _{DD1}	Operating mode	HS (high-speed main) mode Note 5	f _{HOCO} = 64 MHz, f _{IH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.6		mA	
					Basic operation	V _{DD} = 3.0 V		2.6			
					f _{HOCO} = 32 MHz, f _{IH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.3		mA
						Basic operation	V _{DD} = 3.0 V		2.3		
				HS (high-speed main) mode Note 5	f _{HOCO} = 64 MHz, f _{IH} = 32 MHz Note 3	Normal operation	V _{DD} = 5.0 V		5.4	10.2	mA
					Normal operation	V _{DD} = 3.0 V		5.4	10.2		
			f _{HOCO} = 32 MHz, f _{IH} = 32 MHz Note 3		Normal operation	V _{DD} = 5.0 V		5.0	9.6		
			Normal operation		V _{DD} = 3.0 V		5.0	9.6			
			f _{HOCO} = 48 MHz, f _{IH} = 24 MHz Note 3		Normal operation	V _{DD} = 5.0 V		4.2	7.8		
			Normal operation	V _{DD} = 3.0 V		4.2	7.8				
			HS (high-speed main) mode Note 5	f _{HOCO} = 24 MHz, f _{IH} = 24 MHz Note 3	Normal operation	V _{DD} = 5.0 V		4.0	7.4	mA	
				Normal operation	V _{DD} = 3.0 V		4.0	7.4			
			HS (high-speed main) mode Note 5	f _{HOCO} = 16 MHz, f _{IH} = 16 MHz Note 3	Normal operation	V _{DD} = 5.0 V		3.0	5.3	mA	
				Normal operation	V _{DD} = 3.0 V		3.0	5.3			
			LS (low-speed main) mode Note 5	f _{HOCO} = 8 MHz, f _{IH} = 8 MHz Note 3	Normal operation	V _{DD} = 3.0 V		1.4	2.3	mA	
				Normal operation	V _{DD} = 2.0 V		1.4	2.3			
			LV (low-voltage main) mode Note 5	f _{HOCO} = 4 MHz, f _{IH} = 4 MHz Note 3	Normal operation	V _{DD} = 3.0 V		1.3	1.9	mA	
				Normal operation	V _{DD} = 2.0 V		1.3	1.9			
			HS (high-speed main) mode Note 5	f _{MX} = 20 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		3.4	6.2	mA	
						Resonator connection		3.6	6.4		
				f _{MX} = 20 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		3.4	6.2		
						Resonator connection		3.6	6.4		
				f _{MX} = 10 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		2.1	3.6		
						Resonator connection		2.2	3.7		
	f _{MX} = 10 MHz Note 2, V _{DD} = 3.0 V	Normal operation		Square wave input		2.1	3.6				
				Resonator connection		2.2	3.7				
	LS (low-speed main) mode Note 5	f _{MX} = 8 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		1.2	2.2	mA			
				Resonator connection		1.2	2.3				
		f _{MX} = 8 MHz Note 2, V _{DD} = 2.0 V	Normal operation	Square wave input		1.2	2.2				
				Resonator connection		1.2	2.3				
	Subsystem clock operation	f _{SUB} = 32.768 kHz Note 4 TA = -40°C	Normal operation	Square wave input		4.9	7.1	μA			
				Resonator connection		4.9	7.1				
		f _{SUB} = 32.768 kHz Note 4 TA = +25°C	Normal operation	Square wave input		4.9	7.1				
				Resonator connection		4.9	7.1				
		f _{SUB} = 32.768 kHz Note 4 TA = +50°C	Normal operation	Square wave input		5.1	8.8				
				Resonator connection		5.1	8.8				
	f _{SUB} = 32.768 kHz Note 4 TA = +70°C	Normal operation	Square wave input		5.5	10.5					
	Normal operation	Resonator connection		5.5	10.5						
	f _{SUB} = 32.768 kHz Note 4 TA = +85°C	Normal operation	Square wave input		6.5	14.5					
			Normal operation	Resonator connection		6.5	14.5				

(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 3.** When high-speed system clock and subsystem clock are stopped.
- Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
- | | |
|-----------------------------|---|
| HS (high-speed main) mode: | 2.7 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 32 MHz |
| | 2.4 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 16 MHz |
| LS (low-speed main) mode: | 1.8 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 8 MHz |
| LV (low-voltage main) mode: | 1.6 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 4 MHz |
- Remark 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit			
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.79	3.32	mA		
					VDD = 3.0 V		0.79	3.32			
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V		0.49	2.63			
					VDD = 3.0 V		0.49	2.63			
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.62	2.57			
					VDD = 3.0 V		0.62	2.57			
			fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V		0.4	2.00				
				VDD = 3.0 V		0.4	2.00				
			fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V		0.38	1.49				
				VDD = 3.0 V		0.38	1.49				
					LS (low-speed main) mode Note 7	fHOCO = 8 MHz, fIH = 8 MHz Note 4	VDD = 3.0 V		250	800	μA
							VDD = 2.0 V		250	800	
				LV (low-voltage main) mode Note 7	fHOCO = 4 MHz, fIH = 4 MHz Note 4	VDD = 3.0 V		420	755	μA	
						VDD = 2.0 V		420	755		
				HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input		0.30	1.63	mA	
						Resonator connection		0.40	1.85		
						fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input		0.30		1.63
							Resonator connection		0.40		1.85
					fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input		0.20	0.89		
						Resonator connection		0.25	0.97		
					fMX = 10 MHz Note 3, VDD = 3.0 V	Square wave input		0.20	0.89		
						Resonator connection		0.25	0.97		
				LS (low-speed main) mode Note 7	fMX = 8 MHz Note 3, VDD = 3.0 V	Square wave input		110	580	μA	
							Resonator connection		140		630
					fMX = 8 MHz Note 3, VDD = 2.0 V	Square wave input		110	580		
						Resonator connection		140	630		
				Subsystem clock operation	fsUB = 32.768 kHz Note 5, TA = -40°C	Square wave input		0.28	0.66	μA	
			Resonator connection				0.47	0.85			
		fsUB = 32.768 kHz Note 5, TA = +25°C	Square wave input			0.34	0.66				
			Resonator connection			0.53	0.85				
		fsUB = 32.768 kHz Note 5, TA = +50°C	Square wave input			0.37	2.35				
			Resonator connection			0.56	2.54				
		fsUB = 32.768 kHz Note 5, TA = +70°C	Square wave input			0.61	4.08				
			Resonator connection			0.80	4.27				
		fsUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		1.55	8.09					
				Resonator connection		1.74	8.28				
	IDD3 Note 6	STOP mode Note 8	TA = -40°C				0.19	0.57	μA		
			TA = +25°C				0.25	0.57			
			TA = +50°C				0.33	2.26			
			TA = +70°C				0.52	3.99			
			TA = +85°C				1.46	8.00			

(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** During HALT instruction execution by flash memory.
- Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 4.** When high-speed system clock and subsystem clock are stopped.
- Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz
- Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is TA = 25°C

(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit		
Supply current Note 1	I _{DD1}	Operating mode	HS (high-speed main) mode Note 5	f _{HOCO} = 64 MHz, f _{IH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.9		mA	
					Basic operation	V _{DD} = 3.0 V		2.9			
					f _{HOCO} = 32 MHz, f _{IH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.5		
				Basic operation	V _{DD} = 3.0 V		2.5				
			HS (high-speed main) mode Note 5	f _{HOCO} = 64 MHz, f _{IH} = 32 MHz Note 3	Normal operation	V _{DD} = 5.0 V		6.0	11.2	mA	
					Normal operation	V _{DD} = 3.0 V		6.0	11.2		
		f _{HOCO} = 32 MHz, f _{IH} = 32 MHz Note 3		Normal operation	V _{DD} = 5.0 V		5.5	10.6			
				Normal operation	V _{DD} = 3.0 V		5.5	10.6			
		f _{HOCO} = 48 MHz, f _{IH} = 24 MHz Note 3		Normal operation	V _{DD} = 5.0 V		4.7	8.6			
				Normal operation	V _{DD} = 3.0 V		4.7	8.6			
		f _{HOCO} = 24 MHz, f _{IH} = 24 MHz Note 3	Normal operation	V _{DD} = 5.0 V		4.4	8.2				
			Normal operation	V _{DD} = 3.0 V		4.4	8.2				
		f _{HOCO} = 16 MHz, f _{IH} = 16 MHz Note 3	Normal operation	V _{DD} = 5.0 V		3.3	5.9				
			Normal operation	V _{DD} = 3.0 V		3.3	5.9				
		LS (low-speed main) mode Note 5	f _{HOCO} = 8 MHz, f _{IH} = 8 MHz Note 3	Normal operation	V _{DD} = 3.0 V		1.5	2.5	mA		
				Normal operation	V _{DD} = 2.0 V		1.5	2.5			
		LV (low-voltage main) mode Note 5	f _{HOCO} = 4 MHz, f _{IH} = 4 MHz Note 3	Normal operation	V _{DD} = 3.0 V		1.5	2.1	mA		
				Normal operation	V _{DD} = 2.0 V		1.5	2.1			
		HS (high-speed main) mode Note 5	f _{MX} = 20 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		3.7	6.8	mA		
					Resonator connection		3.9	7.0			
			f _{MX} = 20 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		3.7	6.8			
					Resonator connection		3.9	7.0			
			f _{MX} = 10 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		2.3	4.1			
					Resonator connection		2.3	4.2			
f _{MX} = 10 MHz Note 2, V _{DD} = 3.0 V	Normal operation		Square wave input		2.3	4.1					
			Resonator connection		2.3	4.2					
LS (low-speed main) mode Note 5	f _{MX} = 8 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		1.4	2.4	mA				
			Resonator connection		1.4	2.5					
	f _{MX} = 8 MHz Note 2, V _{DD} = 2.0 V	Normal operation	Square wave input		1.4	2.4					
			Resonator connection		1.4	2.5					
Subsystem clock operation	f _{SUB} = 32.768 kHz Note 4 TA = -40°C	Normal operation	Square wave input		5.2		μA				
			Resonator connection		5.2						
	f _{SUB} = 32.768 kHz Note 4 TA = +25°C	Normal operation	Square wave input		5.3	7.7					
			Resonator connection		5.3	7.7					
	f _{SUB} = 32.768 kHz Note 4 TA = +50°C	Normal operation	Square wave input		5.5	10.6					
			Resonator connection		5.5	10.6					
f _{SUB} = 32.768 kHz Note 4 TA = +70°C	Normal operation	Square wave input		5.9	13.2						
		Resonator connection		6.0	13.2						
f _{SUB} = 32.768 kHz Note 4 TA = +85°C	Normal operation	Square wave input		6.8	17.5						
	Normal operation	Resonator connection		6.9	17.5						

(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 3.** When high-speed system clock and subsystem clock are stopped.
- Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
- | | |
|-----------------------------|---|
| HS (high-speed main) mode: | 2.7 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 32 MHz |
| | 2.4 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 16 MHz |
| LS (low-speed main) mode: | 1.8 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 8 MHz |
| LV (low-voltage main) mode: | 1.6 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 4 MHz |
- Remark 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C

(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit		
Supply current Note 1	I _{DD2} Note 2	HALT mode	HS (high-speed main) mode Note 7	f _{HOCO} = 64 MHz, f _{IH} = 32 MHz Note 4	V _{DD} = 5.0 V	0.93	3.32	mA		
					V _{DD} = 3.0 V	0.93	3.32			
				f _{HOCO} = 32 MHz, f _{IH} = 32 MHz Note 4	V _{DD} = 5.0 V	0.5	2.63			
					V _{DD} = 3.0 V	0.5	2.63			
				f _{HOCO} = 48 MHz, f _{IH} = 24 MHz Note 4	V _{DD} = 5.0 V	0.72	2.60			
					V _{DD} = 3.0 V	0.72	2.60			
			f _{HOCO} = 24 MHz, f _{IH} = 24 MHz Note 4	V _{DD} = 5.0 V	0.42	2.03				
				V _{DD} = 3.0 V	0.42	2.03				
			f _{HOCO} = 16 MHz, f _{IH} = 16 MHz Note 4	V _{DD} = 5.0 V	0.39	1.50				
				V _{DD} = 3.0 V	0.39	1.50				
					LS (low-speed main) mode Note 7	f _{HOCO} = 8 MHz, f _{IH} = 8 MHz Note 4	V _{DD} = 3.0 V	270	800	μA
						V _{DD} = 2.0 V	270	800		
				LV (low-voltage main) mode Note 7	f _{HOCO} = 4 MHz, f _{IH} = 4 MHz Note 4	V _{DD} = 3.0 V	450	755	μA	
						V _{DD} = 2.0 V	450	755		
				HS (high-speed main) mode Note 7	f _{MX} = 20 MHz Note 3, V _{DD} = 5.0 V	Square wave input	0.31	1.69	mA	
						Resonator connection	0.41	1.91		
						Square wave input	0.31	1.69		
						Resonator connection	0.41	1.91		
					f _{MX} = 10 MHz Note 3, V _{DD} = 5.0 V	Square wave input	0.21	0.94		
						Resonator connection	0.26	1.02		
					f _{MX} = 10 MHz Note 3, V _{DD} = 3.0 V	Square wave input	0.21	0.94		
						Resonator connection	0.26	1.02		
				LS (low-speed main) mode Note 7	f _{MX} = 8 MHz Note 3, V _{DD} = 3.0 V	Square wave input	110	610	μA	
						Resonator connection	150	660		
					f _{MX} = 8 MHz Note 3, V _{DD} = 2.0 V	Square wave input	110	610		
						Resonator connection	150	660		
		Subsystem clock operation	f _{SUB} = 32.768 kHz Note 5, T _A = -40°C	Square wave input	0.31		μA			
				Resonator connection	0.50					
			f _{SUB} = 32.768 kHz Note 5, T _A = +25°C	Square wave input	0.38	0.76				
				Resonator connection	0.57	0.95				
			f _{SUB} = 32.768 kHz Note 5, T _A = +50°C	Square wave input	0.47	3.59				
				Resonator connection	0.70	3.78				
			f _{SUB} = 32.768 kHz Note 5, T _A = +70°C	Square wave input	0.80	6.20				
				Resonator connection	1.00	6.39				
		f _{SUB} = 32.768 kHz Note 5, T _A = +85°C	Square wave input	1.65	10.56					
			Resonator connection	1.84	10.75					
	I _{DD3} Note 6	STOP mode Note 8	T _A = -40°C			0.19		μA		
			T _A = +25°C			0.30	0.59			
			T _A = +50°C			0.41	3.42			
			T _A = +70°C			0.80	6.03			
			T _A = +85°C			1.53	10.39			

(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** During HALT instruction execution by flash memory.
- Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 4.** When high-speed system clock and subsystem clock are stopped.
- Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
- HS (high-speed main) mode: 2.7 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 32 MHz
2.4 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 16 MHz
- LS (low-speed main) mode: 1.8 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 8 MHz
- LV (low-voltage main) mode: 1.6 V ≤ V_{DD} ≤ 5.5 V@1 MHz to 4 MHz
- Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is TA = 25°C

(4) Peripheral Functions (Common to all products)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	IFIL Note 1				0.20		μA
RTC operating current	IRTC Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	IIIT Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	IWDT Notes 1, 2, 5	fil = 15 kHz			0.22		μA
A/D converter operating current	IADC Notes 1, 6	When conversion at maximum speed	Normal mode, AVREFP = VDD = 5.0 V		1.3	1.7	mA
			Low voltage mode, AVREFP = VDD = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	IADREF Note 1				75.0		μA
Temperature sensor operating current	ITMPS Note 1				75.0		μA
D/A converter operating current	IDAC Notes 1, 11, 13	Per D/A converter channel				1.5	mA
Comparator operating current	ICMP Notes 1, 12, 13	VDD = 5.0 V, Regulator output voltage = 2.1 V	Window mode		12.5		μA
			Comparator high-speed mode		6.5		μA
			Comparator low-speed mode		1.7		μA
		VDD = 5.0 V, Regulator output voltage = 1.8 V	Window mode		8.0		μA
			Comparator high-speed mode		4.0		μA
			Comparator low-speed mode		1.3		μA
LVD operating current	ILVD Notes 1, 7				0.08		μA
Self-programming operating current	IFSP Notes 1, 9				2.50	12.20	mA
BGO operating current	IBGO Notes 1, 8				2.50	12.20	mA
SNOOZE operating current	ISNOZ Note 1	ADC operation	The mode is performed Note 10		0.50	0.60	mA
			The A/D conversion operations are performed, Low voltage mode, AVREFP = VDD = 3.0 V		1.20	1.44	
		CSI/JART operation		0.70	0.84		
		DTC operation		3.10			

Note 1. Current flowing to VDD.

Note 2. When high speed on-chip oscillator and high-speed system clock are stopped.

Note 3. Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IRTC, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added. IDD2 subsystem clock operation includes the operational current of the real-time clock.

Note 4. Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IIIT, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added.

- Note 5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and IWDT when the watchdog timer is in operation.
- Note 6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2 and IADC when the A/D converter operates in an operation mode or the HALT mode.
- Note 7.** Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and ILVD when the LVD circuit is in operation.
- Note 8.** Current flowing during programming of the data flash.
- Note 9.** Current flowing during self-programming.
- Note 10.** For shift time to the SNOOZE mode, see **23.3.3 SNOOZE mode** in the RL78/G14 User's Manual.
- Note 11.** Current flowing only to the D/A converter. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2 and IDAC when the D/A converter operates in an operation mode or the HALT mode.
- Note 12.** Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2, or IDD3 and ICMP when the comparator circuit is in operation.
- Note 13.** A comparator and D/A converter are provided in products with 96 KB or more code flash memory.
- Remark 1.** f_{IL}: Low-speed on-chip oscillator clock frequency
- Remark 2.** f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 3.** f_{CLK}: CPU/peripheral hardware clock frequency
- Remark 4.** Temperature condition of the TYP. value is TA = 25°C

2.4 AC Characteristics

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Instruction cycle (minimum instruction execution time)	Tcy	Main system clock (fMAIN) operation	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ VDD < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.125		1	μs
			LV (low-voltage main) mode	1.6 V ≤ VDD ≤ 5.5 V	0.25		1	μs
			Subsystem clock (fSUB) operation	1.8 V ≤ VDD ≤ 5.5 V	28.5	30.5	31.3	μs
		In the self-programming mode	HS (high-speed main) mode	2.7 V ≤ VDD ≤ 5.5 V	0.03125		1	μs
				2.4 V ≤ VDD < 2.7 V	0.0625		1	μs
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.125		1	μs
LV (low-voltage main) mode	1.8 V ≤ VDD ≤ 5.5 V		0.25		1	μs		
External system clock frequency	fex	2.7 V ≤ VDD ≤ 5.5 V		1.0		20.0	MHz	
		2.4 V ≤ VDD ≤ 2.7 V		1.0		16.0	MHz	
		1.8 V ≤ VDD < 2.4 V		1.0		8.0	MHz	
		1.6 V ≤ VDD < 1.8 V		1.0		4.0	MHz	
	fexs			32		35	kHz	
External system clock input high-level width, low-level width	texH, texL	2.7 V ≤ VDD ≤ 5.5 V		24			ns	
		2.4 V ≤ VDD ≤ 2.7 V		30			ns	
		1.8 V ≤ VDD < 2.4 V		60			ns	
		1.6 V ≤ VDD < 1.8 V		120			ns	
	texHS, texLS			13.7			μs	
Ti00 to Ti03, Ti10 to Ti13 input high-level width, low-level width	ttrIH, ttrIL			1/fMCK + 10			ns	
Timer RJ input cycle	fc	TRJIO	2.7 V ≤ EVDD0 ≤ 5.5 V	100			ns	
			1.8 V ≤ EVDD0 < 2.7 V	300			ns	
			1.6 V ≤ EVDD0 < 1.8 V	500			ns	
Timer RJ input high-level width, low-level width	trJIH, trJIL	TRJIO	2.7 V ≤ EVDD0 ≤ 5.5 V	40			ns	
			1.8 V ≤ EVDD0 < 2.7 V	120			ns	
			1.6 V ≤ EVDD0 < 1.8 V	200			ns	

Note The following conditions are required for low voltage interface when EVDD0 < VDD

1.8 V ≤ EVDD0 < 2.7 V: MIN. 125 ns

1.6 V ≤ EVDD0 < 1.8 V: MIN. 250 ns

Remark fMCK: Timer array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

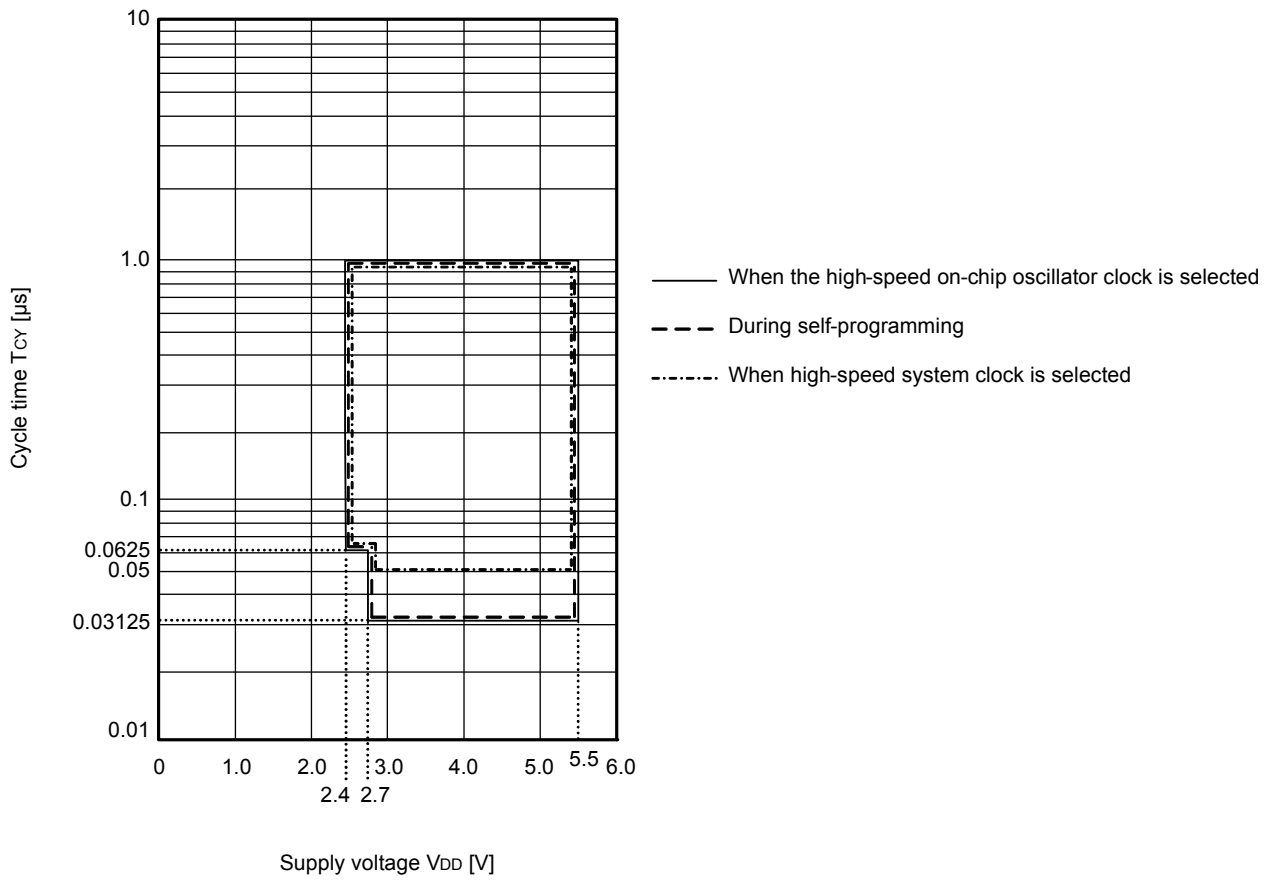
(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

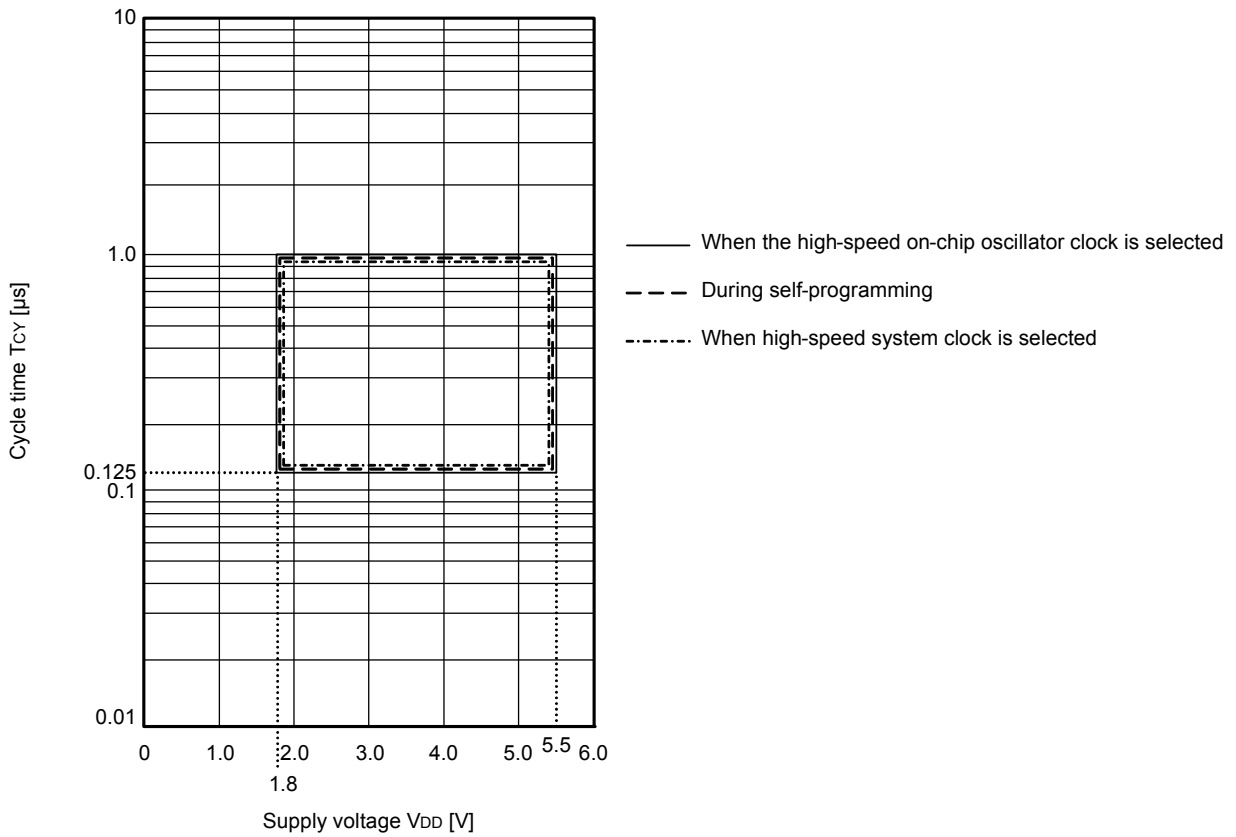
Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Timer RD input high-level width, low-level width	tTDIH, tTDIL	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1		3/fCLK			ns
Timer RD forced cutoff signal input low-level width	tTDSIL	P130/INTP0	2MHz < fCLK ≤ 32 MHz	1			μs
			fCLK ≤ 2 MHz	1/fCLK + 1			
Timer RG input high-level width, low-level width	tTGIH, tTGIL	TRGIOA, TRGIOB		2.5/fCLK			ns
TO00 to TO03, TO10 to TO13, TRJIO0, TRJO0, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRGIOA, TRGIOB output frequency	fTO	HS (high-speed main) mode	4.0 V ≤ EVDD0 ≤ 5.5 V			16	MHz
			2.7 V ≤ EVDD0 < 4.0 V			8	MHz
			1.8 V ≤ EVDD0 < 2.7 V			4	MHz
			1.6 V ≤ EVDD0 < 1.8 V			2	MHz
		LS (low-speed main) mode	1.8 V ≤ EVDD0 ≤ 5.5 V			4	MHz
			1.6 V ≤ EVDD0 < 1.8 V			2	MHz
LV (low-voltage main) mode	1.6 V ≤ EVDD0 ≤ 5.5 V			2	MHz		
PCLBUZ0, PCLBUZ1 output frequency	fPCL	HS (high-speed main) mode	4.0 V ≤ EVDD0 ≤ 5.5 V			16	MHz
			2.7 V ≤ EVDD0 < 4.0 V			8	MHz
			1.8 V ≤ EVDD0 < 2.7 V			4	MHz
			1.6 V ≤ EVDD0 < 1.8 V			2	MHz
		LS (low-speed main) mode	1.8 V ≤ EVDD0 ≤ 5.5 V			4	MHz
			1.6 V ≤ EVDD0 < 1.8 V			2	MHz
LV (low-voltage main) mode	1.8 V ≤ EVDD0 ≤ 5.5 V			4	MHz		
		1.6 V ≤ EVDD0 < 1.8 V			2	MHz	
Interrupt input high-level width, low-level width	tINTH, tINTL	INTP0	1.6 V ≤ VDD ≤ 5.5 V	1			μs
		INTP1 to INTP11	1.6 V ≤ EVDD0 ≤ 5.5 V	1			μs
Key interrupt input low-level width	tKR	KR0 to KR7	1.8 V ≤ EVDD0 ≤ 5.5 V	250			ns
			1.6 V ≤ EVDD0 < 1.8 V	1			μs
RESET low-level width	tRSL			10			μs

Minimum Instruction Execution Time during Main System Clock Operation

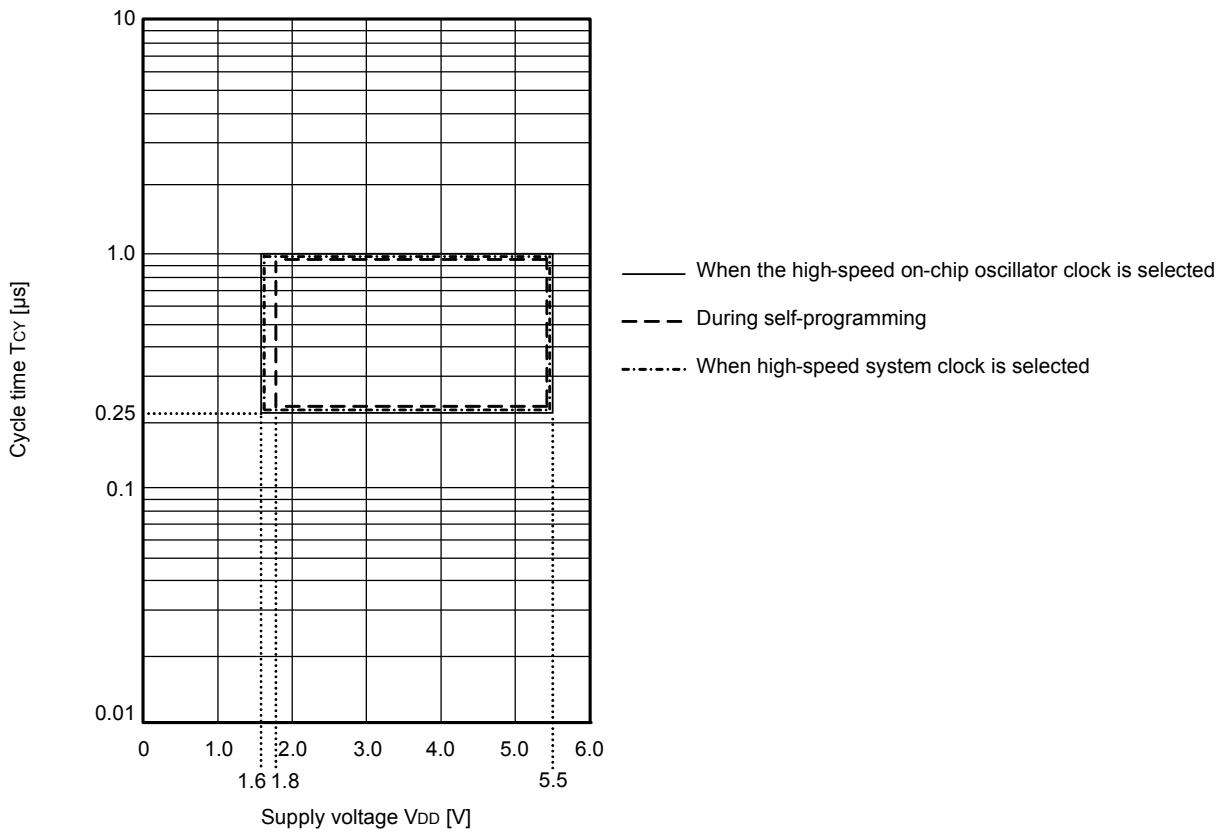
T_{CY} vs V_{DD} (HS (high-speed main) mode)



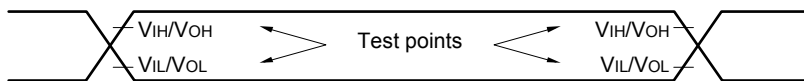
T_{CY} vs V_{DD} (LS (low-speed main) mode)



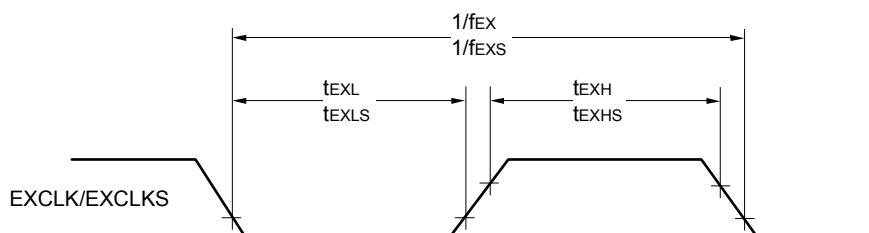
T_{CY} vs V_{DD} (LV (low-voltage main) mode)



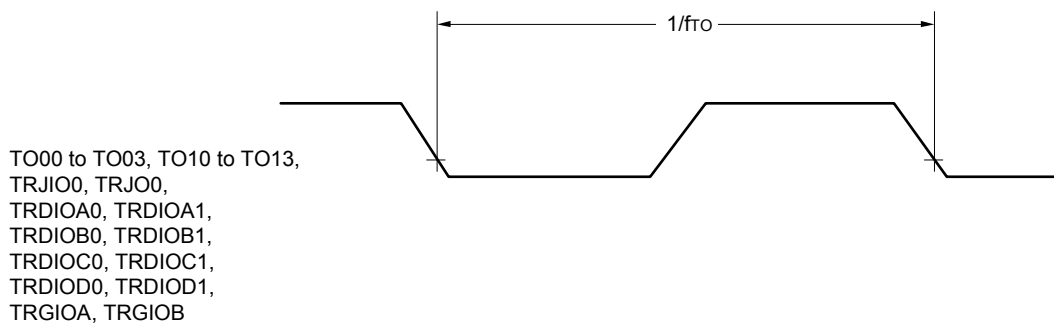
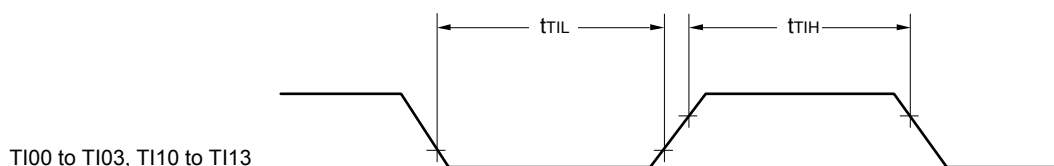
AC Timing Test Points

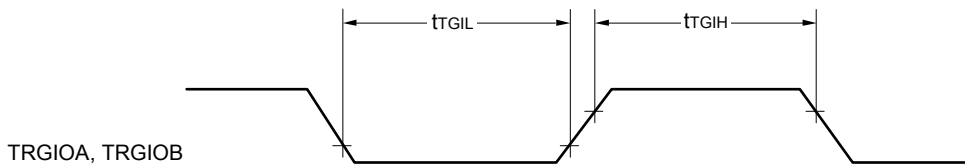
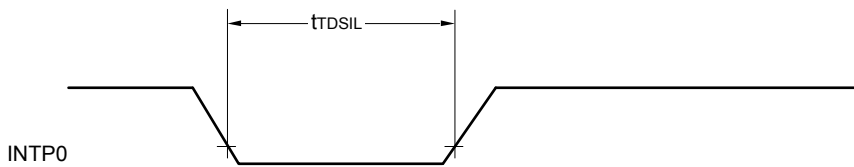
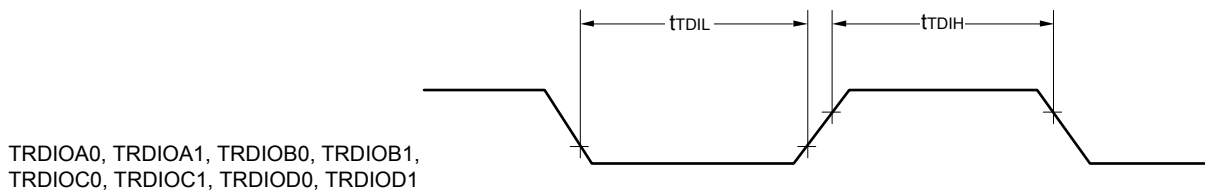
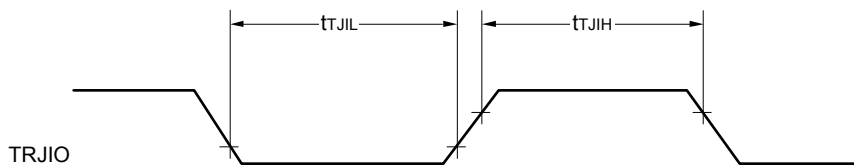


External System Clock Timing

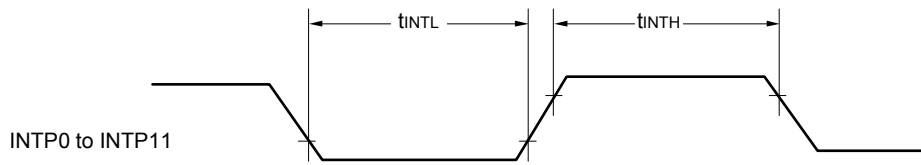


TI/TO Timing

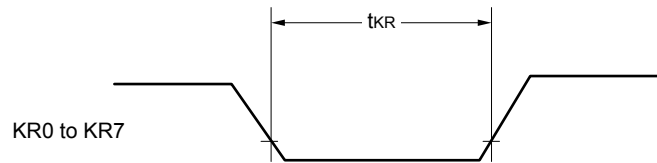




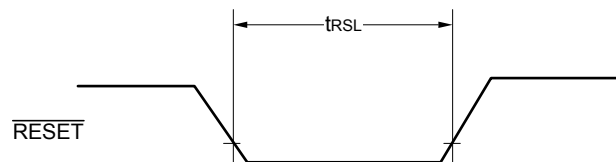
Interrupt Request Input Timing



Key Interrupt Input Timing

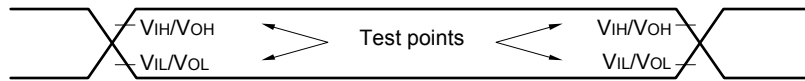


RESET Input Timing



2.5 Peripheral Functions Characteristics

AC Timing Test Points



2.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		LS (low-speed main) Mode		LV (low-voltage main) Mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 1		2.4 V ≤ EVDD0 ≤ 5.5 V		fMCK/6 Note 2		fMCK/6		fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note 3		5.3		1.3		0.6	Mbps
		1.8 V ≤ EVDD0 ≤ 5.5 V		fMCK/6 Note 2		fMCK/6		fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note 3		5.3		1.3		0.6	Mbps
		1.7 V ≤ EVDD0 ≤ 5.5 V		fMCK/6 Note 2		fMCK/6 Note 2		fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note 3		5.3		1.3		0.6	Mbps
		1.6 V ≤ EVDD0 ≤ 5.5 V	—			fMCK/6 Note 2		fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note 3	—			1.3		0.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

Note 2. The following conditions are required for low voltage interface when EVDD0 < VDD.

2.4 V ≤ EVDD0 < 2.7 V: MAX. 2.6 Mbps

1.8 V ≤ EVDD0 < 2.4 V: MAX. 1.3 Mbps

1.6 V ≤ EVDD0 < 1.8 V: MAX. 0.6 Mbps

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

HS (high-speed main) mode: 32 MHz (2.7 V ≤ VDD ≤ 5.5 V)

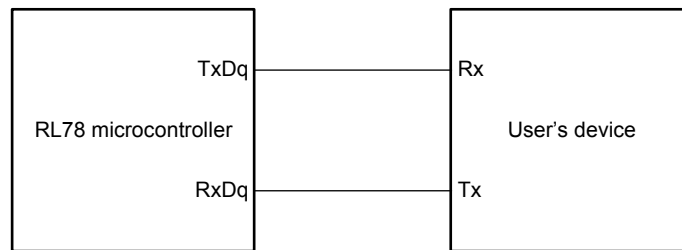
16 MHz (2.4 V ≤ VDD ≤ 5.5 V)

LS (low-speed main) mode: 8 MHz (1.8 V ≤ VDD ≤ 5.5 V)

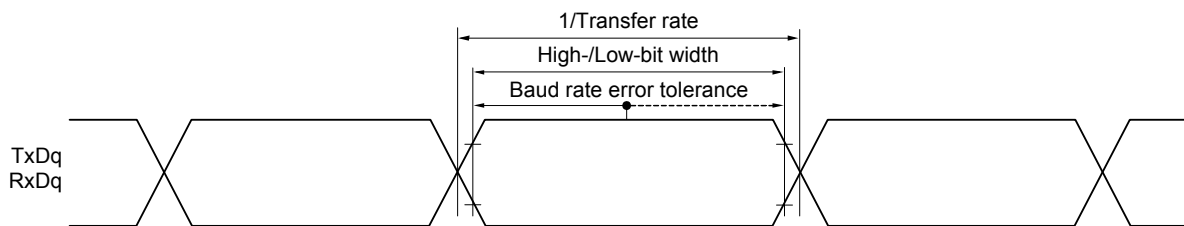
LV (low-voltage main) mode: 4 MHz (1.6 V ≤ VDD ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remark 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

Remark 2. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)**(TA = -40 to +85°C, 2.7 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	tkCY1	tkCY1 ≥ 2/fCLK 4.0 V ≤ EVDD0 ≤ 5.5 V	62.5		250		500		ns
			83.3		250		500		ns
SCKp high-/low-level width	tkH1, tkL1	4.0 V ≤ EVDD0 ≤ 5.5 V	tkCY1/2 - 7		tkCY1/2 - 50		tkCY1/2 - 50		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V	tkCY1/2 - 10		tkCY1/2 - 50		tkCY1/2 - 50		ns
Slp setup time (to SCKp↑) Note 1	tsIK1	4.0 V ≤ EVDD0 ≤ 5.5 V	23		110		110		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V	33		110		110		ns
Slp hold time (from SCKp↑) Note 2	tsIH1	2.7 V ≤ EVDD0 ≤ 5.5 V	10		10		10		ns
Delay time from SCKp↓ to SOp output Note 3	tkSO1	C = 20 pF Note 4		10		10		10	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. This value is valid only when CSI00's peripheral I/O redirect function is not used.

Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0),
g: PIM and POM numbers (g = 1)

Remark 3. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00))

(3) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)
(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	tkCY1	tkCY1 ≥ 4/fCLK	2.7 V ≤ EVDD0 ≤ 5.5 V	125		500		1000		ns
			2.4 V ≤ EVDD0 ≤ 5.5 V	250		500		1000		ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	500		500		1000		ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	1000		1000		1000		ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		1000		1000		ns
SCKp high-/low-level width	tkH1, tkL1	4.0 V ≤ EVDD0 ≤ 5.5 V	tkCY1/2 - 12		tkCY1/2 - 50		tkCY1/2 - 50		ns	
		2.7 V ≤ EVDD0 ≤ 5.5 V	tkCY1/2 - 18		tkCY1/2 - 50		tkCY1/2 - 50		ns	
		2.4 V ≤ EVDD0 ≤ 5.5 V	tkCY1/2 - 38		tkCY1/2 - 50		tkCY1/2 - 50		ns	
		1.8 V ≤ EVDD0 ≤ 5.5 V	tkCY1/2 - 50		tkCY1/2 - 50		tkCY1/2 - 50		ns	
		1.7 V ≤ EVDD0 ≤ 5.5 V	tkCY1/2 - 100		tkCY1/2 - 100		tkCY1/2 - 100		ns	
		1.6 V ≤ EVDD0 ≤ 5.5 V	—		tkCY1/2 - 100		tkCY1/2 - 100		ns	
Slp setup time (to SCKp↑) Note 1	tsIK1	4.0 V ≤ EVDD0 ≤ 5.5 V	44		110		110		ns	
		2.7 V ≤ EVDD0 ≤ 5.5 V	44		110		110		ns	
		2.4 V ≤ EVDD0 ≤ 5.5 V	75		110		110		ns	
		1.8 V ≤ EVDD0 ≤ 5.5 V	110		110		110		ns	
		1.7 V ≤ EVDD0 ≤ 5.5 V	220		220		220		ns	
		1.6 V ≤ EVDD0 ≤ 5.5 V	—		220		220		ns	
Slp hold time (from SCKp↑) Note 2	tkSI1	1.7 V ≤ EVDD0 ≤ 5.5 V	19		19		19		ns	
		1.6 V ≤ EVDD0 ≤ 5.5 V	—		19		19		ns	
Delay time from SCKp↓ to SOp output Note 3	tkSO1	1.7 V ≤ EVDD0 ≤ 5.5 V C = 30 pF Note 4		25		25		25	ns	
		1.6 V ≤ EVDD0 ≤ 5.5 V C = 30 pF Note 4		—		25		25	ns	

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. fMCK: Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)
(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
				MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	tkCY2	4.0 V ≤ EVDD0 ≤ 5.5 V	20 MHz < fMCK	8/fMCK	—	—	—	—	ns	
			fMCK ≤ 20 MHz	6/fMCK	—	6/fMCK	6/fMCK	ns		
		2.7 V ≤ EVDD0 ≤ 5.5 V	16 MHz < fMCK	8/fMCK	—	—	—	ns		
			fMCK ≤ 16 MHz	6/fMCK	—	6/fMCK	6/fMCK	ns		
		2.4 V ≤ EVDD0 ≤ 5.5 V		6/fMCK and 500	6/fMCK and 500	6/fMCK and 500	6/fMCK and 500	ns		
		1.8 V ≤ EVDD0 ≤ 5.5 V		6/fMCK and 750	6/fMCK and 750	6/fMCK and 750	6/fMCK and 750	ns		
		1.7 V ≤ EVDD0 ≤ 5.5 V		6/fMCK and 1500	6/fMCK and 1500	6/fMCK and 1500	6/fMCK and 1500	ns		
		1.6 V ≤ EVDD0 ≤ 5.5 V		—	6/fMCK and 1500	6/fMCK and 1500	6/fMCK and 1500	ns		
SCKp high-/low-level width	tkH2, tkL2	4.0 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 - 7	tkCY2/2 - 7	tkCY2/2 - 7	tkCY2/2 - 7	ns		
		2.7 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 - 8	tkCY2/2 - 8	tkCY2/2 - 8	tkCY2/2 - 8	ns		
		1.8 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 - 18	tkCY2/2 - 18	tkCY2/2 - 18	tkCY2/2 - 18	ns		
		1.7 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 - 66	tkCY2/2 - 66	tkCY2/2 - 66	tkCY2/2 - 66	ns		
		1.6 V ≤ EVDD0 ≤ 5.5 V		—	tkCY2/2 - 66	tkCY2/2 - 66	tkCY2/2 - 66	ns		
Slp setup time (to SCKp↑) Note 1	tsIK2	2.7 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 20	1/fMCK + 30	1/fMCK + 30	1/fMCK + 30	ns		
		1.8 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 30	1/fMCK + 30	1/fMCK + 30	1/fMCK + 30	ns		
		1.7 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 40	1/fMCK + 40	1/fMCK + 40	1/fMCK + 40	ns		
		1.6 V ≤ EVDD0 ≤ 5.5 V		—	1/fMCK + 40	1/fMCK + 40	1/fMCK + 40	ns		
Slp hold time (from SCKp↑) Note 2	tkSI2	1.8 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 31	1/fMCK + 31	1/fMCK + 31	1/fMCK + 31	ns		
		1.7 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 250	1/fMCK + 250	1/fMCK + 250	1/fMCK + 250	ns		
		1.6 V ≤ EVDD0 ≤ 5.5 V		—	1/fMCK + 250	1/fMCK + 250	1/fMCK + 250	ns		
Delay time from SCKp↓ to SOp output Note 3	tkSO2	C = 30 pF Note 4	2.7 V ≤ EVDD0 ≤ 5.5 V	2/fMCK + 44	2/fMCK + 110	2/fMCK + 110	2/fMCK + 110	ns		
			2.4 V ≤ EVDD0 ≤ 5.5 V	2/fMCK + 75	2/fMCK + 110	2/fMCK + 110	2/fMCK + 110	ns		
			1.8 V ≤ EVDD0 ≤ 5.5 V	2/fMCK + 100	2/fMCK + 110	2/fMCK + 110	2/fMCK + 110	ns		
			1.7 V ≤ EVDD0 ≤ 5.5 V	2/fMCK + 220	2/fMCK + 220	2/fMCK + 220	2/fMCK + 220	ns		
			1.6 V ≤ EVDD0 ≤ 5.5 V	—	2/fMCK + 220	2/fMCK + 220	2/fMCK + 220	ns		

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

(4) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

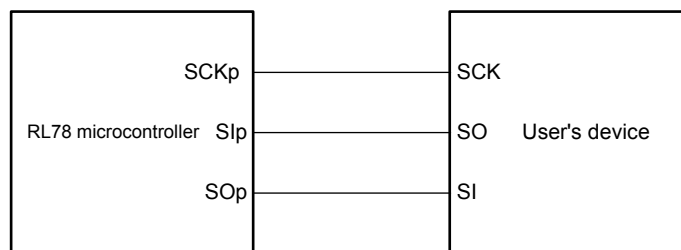
(2/2)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit	
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
SSI00 setup time	tSSIK	DAPmn = 0	2.7 V ≤ EVDD0 ≤ 5.5 V	120		120		120		ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	200		200		200		ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	400		400		400		ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		400		400		ns
		DAPmn = 1	2.7 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 120		1/fMCK + 120		1/fMCK + 120		ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 200		1/fMCK + 200		1/fMCK + 200		ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 400		1/fMCK + 400		1/fMCK + 400		ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		1/fMCK + 400		1/fMCK + 400		ns
SSI00 hold time	tkSSI	DAPmn = 0	2.7 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 120		1/fMCK + 120		1/fMCK + 120		ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 200		1/fMCK + 200		1/fMCK + 200		ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 400		1/fMCK + 400		1/fMCK + 400		ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		1/fMCK + 400		1/fMCK + 400		ns
		DAPmn = 1	2.7 V ≤ EVDD0 ≤ 5.5 V	120		120		120		ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	200		200		200		ns
			1.7 V ≤ EVDD0 ≤ 5.5 V	400		400		400		ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		400		400		ns

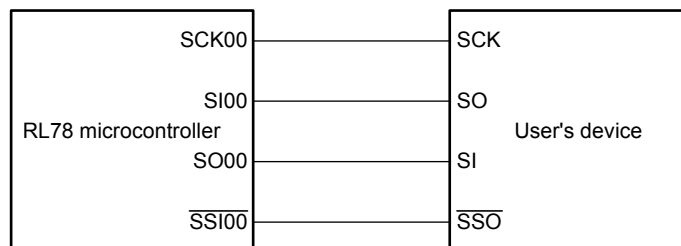
Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

CSI mode connection diagram (during communication at same potential)



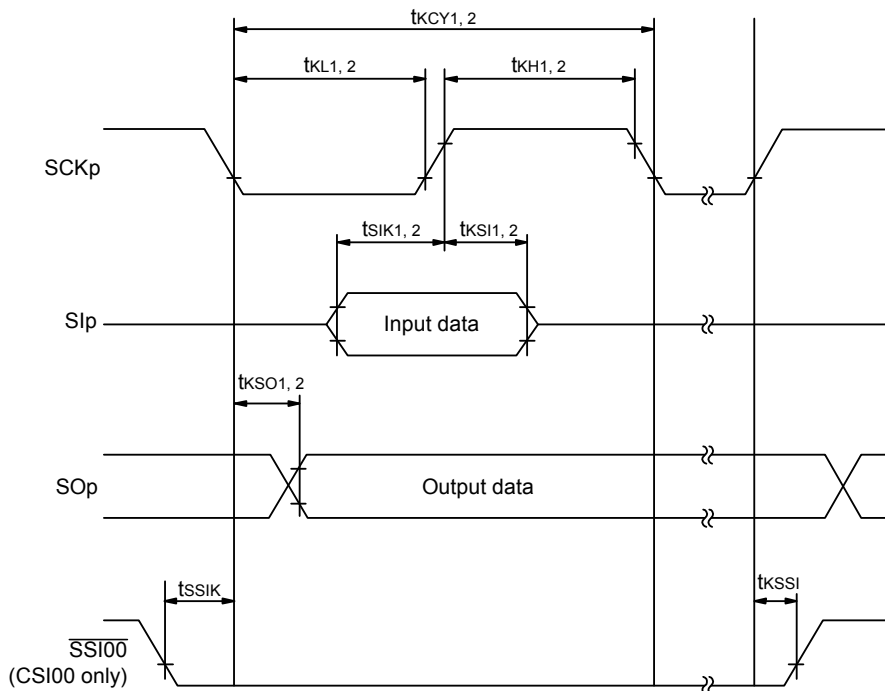
**CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))**



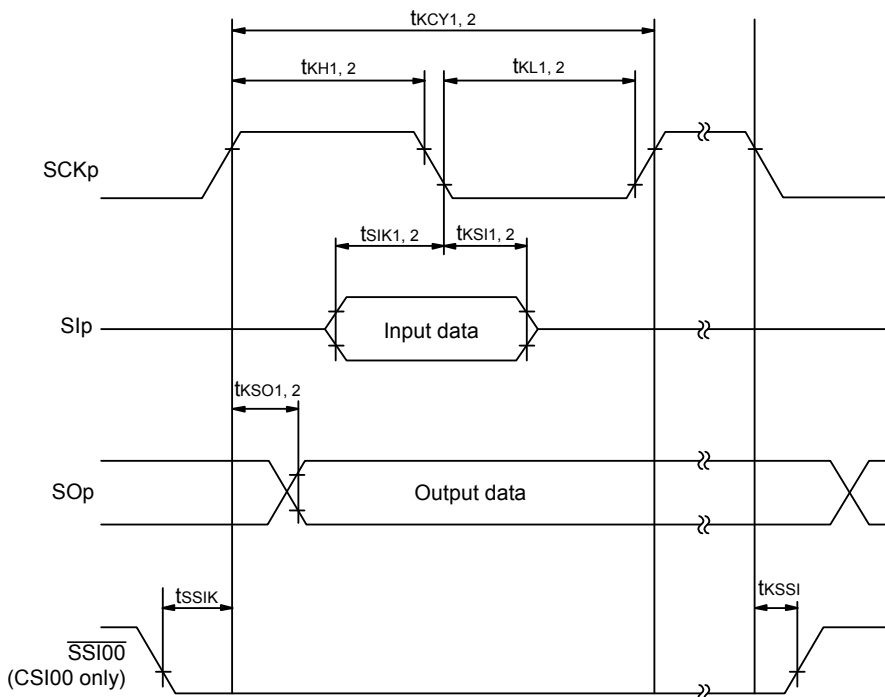
Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(5) During communication at same potential (simplified I²C mode)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f _{SCL}	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ		400 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
		1.7 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ		250 Note 1		250 Note 1		250 Note 1	kHz
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ		—		250 Note 1		250 Note 1	kHz
Hold time when SCLr = "L"	t _{LOW}	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	—		1850		1850		ns
Hold time when SCLr = "H"	t _{HIGH}	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1150		1150		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1550		1550		1550		ns
		1.7 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1850		1850		1850		ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	—		1850		1850		ns

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

(5) During communication at same potential (simplified I²C mode)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	tsu: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK + 85 Note 2		1/fMCK + 145 Note 2		1/fMCK + 145 Note 2		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1/fMCK + 145 Note 2		1/fMCK + 145 Note 2		1/fMCK + 145 Note 2		ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1/fMCK + 230 Note 2		1/fMCK + 230 Note 2		1/fMCK + 230 Note 2		ns
		1.7 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1/fMCK + 290 Note 2		1/fMCK + 290 Note 2		1/fMCK + 290 Note 2		ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	—		1/fMCK + 290 Note 2		1/fMCK + 290 Note 2		ns
Data hold time (transmission)	tHD: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	0	405	0	405	0	405	ns
		1.7 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	—		0	405	0	405	ns

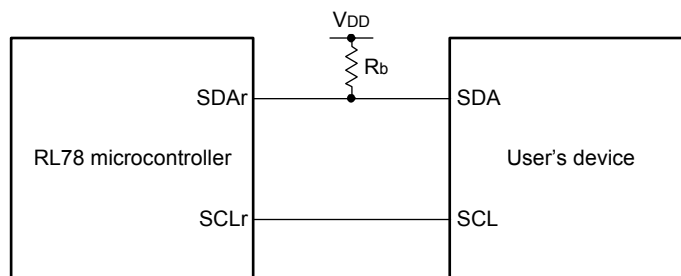
Note 1. The value must also be equal to or less than fMCK/4.

Note 2. Set the fMCK value to keep the hold time of SCLr = "L" and SCLr = "H".

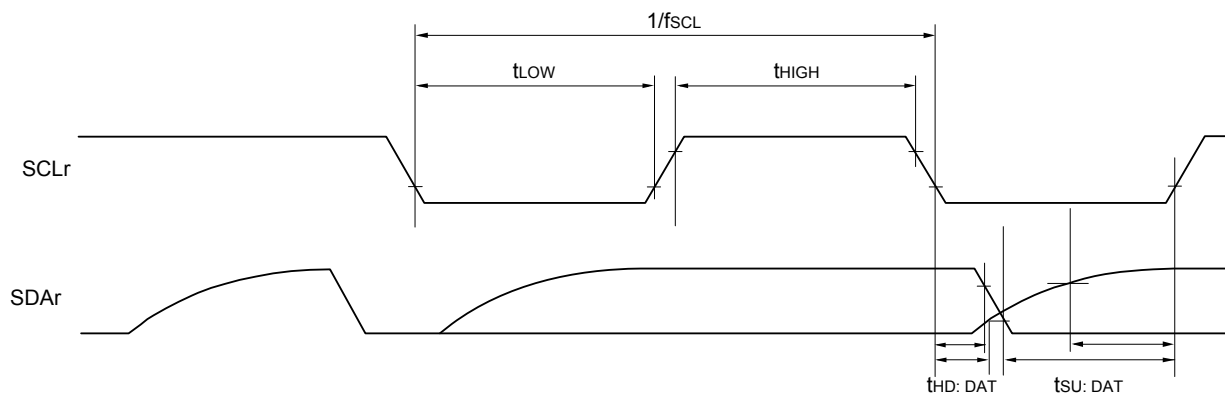
Caution Select the normal input buffer and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remark 1. R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 3 to 5, 14),
h: POM number (h = 0, 1, 3 to 5, 7, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKS_{mn} bit of serial mode register mn (SMR_{mn}). m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit	
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Transfer rate		reception	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V		f _{MCK} /6 Note 1		f _{MCK} /6 Note 1		f _{MCK} /6 Note 1	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Note 4		5.3		1.3		0.6	Mbps
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V		f _{MCK} /6 Note 1		f _{MCK} /6 Note 1		f _{MCK} /6 Note 1	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Note 4		5.3		1.3		0.6	Mbps
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V		f _{MCK} /6 Notes 1, 2, 3		f _{MCK} /6 Notes 1, 2		f _{MCK} /6 Notes 1, 2	bps
			Theoretical value of the maximum transfer rate f _{MCK} = f _{CLK} Note 4		5.3		1.3		0.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

Note 2. Use it with EVDD0 ≥ Vb.

Note 3. The following conditions are required for low voltage interface when EVDD0 < VDD.

2.4 V ≤ EVDD0 < 2.7 V: MAX. 2.6 Mbps

1.8 V ≤ EVDD0 < 2.4 V: MAX. 1.3 Mbps

Note 4. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode: 32 MHz (2.7 V ≤ VDD ≤ 5.5 V)

16 MHz (2.4 V ≤ VDD ≤ 5.5 V)

LS (low-speed main) mode: 8 MHz (1.8 V ≤ VDD ≤ 5.5 V)

LV (low-voltage main) mode: 4 MHz (1.6 V ≤ VDD ≤ 5.5 V)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

Remark 1. V_b [V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10 to 13)

Remark 4. UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit	
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Transfer rate		transmission	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V		Note 1		Note 1		Note 1	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 1.4 kΩ, Vb = 2.7 V		2.8 Note 2		2.8 Note 2		2.8 Note 2	Mbps
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V		Note 3		Note 3		Note 3	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 2.7 kΩ, Vb = 2.3 V		1.2 Note 4		1.2 Note 4		1.2 Note 4	Mbps
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V		Notes 5, 6		Notes 5, 6		Notes 5, 6	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 5.5 kΩ, Vb = 1.6 V		0.43 Note 7		0.43 Note 7		0.43 Note 7	Mbps

Note 1. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when $4.0\text{ V} \leq \text{EVDD}_0 \leq 5.5\text{ V}$ and $2.7\text{ V} \leq V_b \leq 4.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.7\text{ V} \leq \text{EVDD}_0 < 4.0\text{ V}$ and $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use it with $EV_{DD0} \geq V_b$.

Note 6. The smaller maximum transfer rate derived by using $f_{mck}/6$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $1.8 \text{ V} \leq EV_{DD0} < 3.3 \text{ V}$ and $1.6 \text{ V} \leq V_b \leq 2.0 \text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

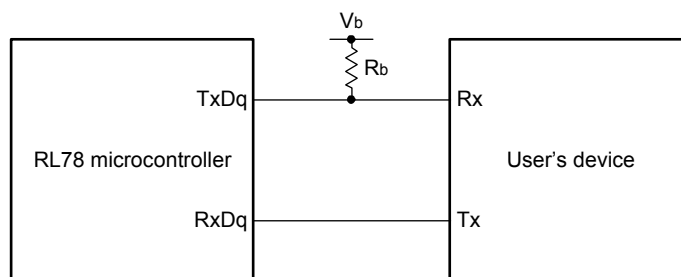
* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 7. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

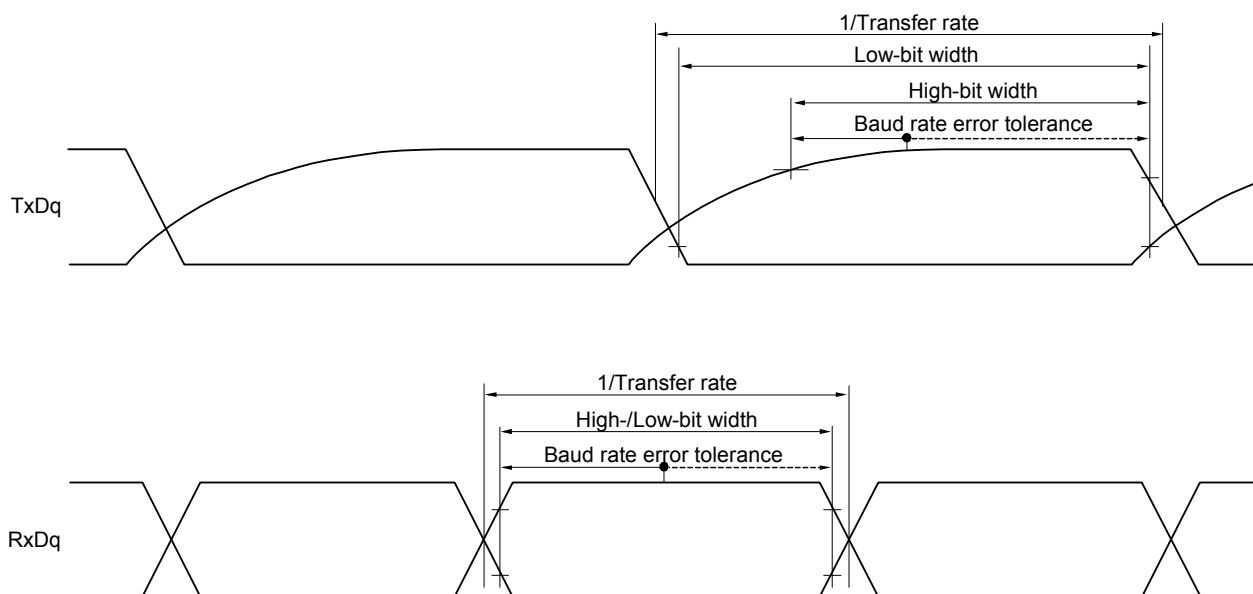
Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



- Remark 1.** R_b[Ω]: Communication line (TxDq) pull-up resistance,
C_b[F]: Communication line (TxDq) load capacitance, V_b[V]: Communication line voltage
- Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)
- Remark 3.** f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))
- Remark 4.** UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)**(TA = -40 to +85°C, 2.7 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	tkCY1	tkCY1 ≥ 2/fCLK 4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	200		1150		1150		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	300		1150		1150		ns
SCKp high-level width	tkH1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	tkCY1/2 - 50		tkCY1/2 - 50		tkCY1/2 - 50		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	tkCY1/2 - 120		tkCY1/2 - 120		tkCY1/2 - 120		ns
SCKp low-level width	tkL1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	tkCY1/2 - 7		tkCY1/2 - 50		tkCY1/2 - 50		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	tkCY1/2 - 10		tkCY1/2 - 50		tkCY1/2 - 50		ns
Slp setup time (to SCKp↑) Note 1	tSIK1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	58		479		479		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	121		479		479		ns
Slp hold time (from SCKp↑) Note 1	tKSI1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	10		10		10		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↓ to SOP out- put Note 1	tkSO1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ		60		60		60	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ		130		130		130	ns

(Notes, Caution, and Remarks are listed on the next page.)

(7) Communication at different potential (2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output, corresponding CSI00 only)**(TA = -40 to +85°C, 2.7 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↓) Note 2	tsIK1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	23		110		110		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	33		110		110		ns
Slp hold time (from SCKp↓) Note 2	tkSI1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ	10		10		10		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ	10		10		10		ns
Delay time from SCKp↑ to SOp output Note 2	tkSO1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 20 pF, Rb = 1.4 kΩ		10		10		10	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 20 pF, Rb = 2.7 kΩ		10		10		10	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

Remark 1. Rb[Ω]: Communication line (SCKp, SOp) pull-up resistance, Cb[F]: Communication line (SCKp, SOp) load capacitance, Vb[V]: Communication line voltage

Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM number (g = 3, 5)

Remark 3. fMCK: Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

Remark 4. This value is valid only when CSI00's peripheral I/O redirect function is not used.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit	
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
SCKp cycle time	tkCY1	tkCY1 ≥ 4/fCLK	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	300		1150		1150		ns
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	500		1150		1150		ns
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note, Cb = 30 pF, Rb = 5.5 kΩ	1150		1150		1150		ns
SCKp high-level width	tkH1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	tkCY1/2 - 75		tkCY1/2 - 75		tkCY1/2 - 75		ns	
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	tkCY1/2 - 170		tkCY1/2 - 170		tkCY1/2 - 170		ns
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note, Cb = 30 pF, Rb = 5.5 kΩ	tkCY1/2 - 458		tkCY1/2 - 458		tkCY1/2 - 458		ns
SCKp low-level width	tkL1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	tkCY1/2 - 12		tkCY1/2 - 50		tkCY1/2 - 50		ns	
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	tkCY1/2 - 18		tkCY1/2 - 50		tkCY1/2 - 50		ns
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note, Cb = 30 pF, Rb = 5.5 kΩ	tkCY1/2 - 50		tkCY1/2 - 50		tkCY1/2 - 50		ns

Note Use it with EVDD0 ≥ Vb.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↑) Note 1	tSIK1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	81		479		479		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	177		479		479		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rb = 5.5 kΩ	479		479		479		ns
Slp hold time (from SCKp↑) Note 1	tKSI1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↓ to SOp output Note 1	tKSO1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		100		100		100	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		195		195		195	ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rb = 5.5 kΩ		483		483		483	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.**Note 2.** Use it with EVDD0 ≥ Vb.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(3/3)**

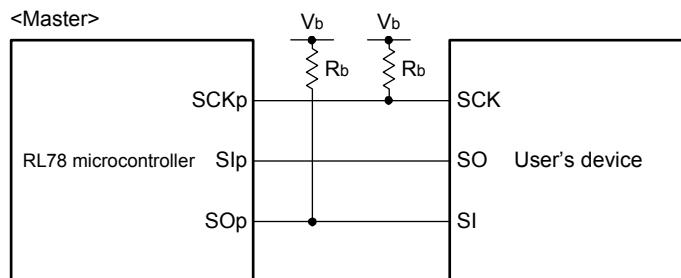
Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Slp setup time (to SCKp↓) Note 1	tSIK1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	44		110		110		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	44		110		110		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rb = 5.5 kΩ	110		110		110		ns
Slp hold time (from SCKp↓) Note 1	tKSI1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	19		19		19		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	19		19		19		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rb = 5.5 kΩ	19		19		19		ns
Delay time from SCKp↑ to SOp output Note 1	tKSO1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		25		25		25	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		25		25		25	ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rb = 5.5 kΩ		25		25		25	ns

Note 1. When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.**Note 2.** Use it with EVDD0 ≥ Vb.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

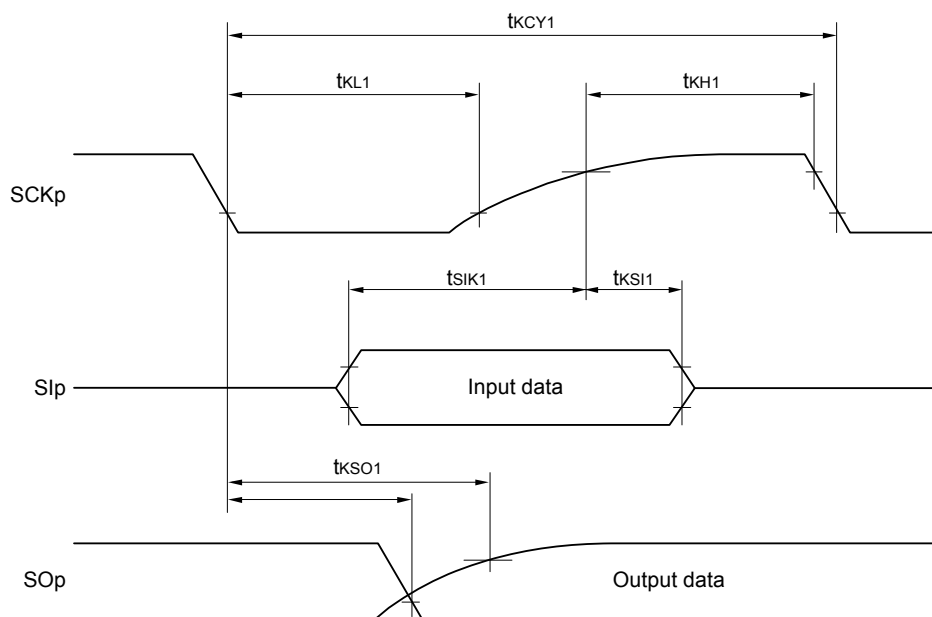
(Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential)

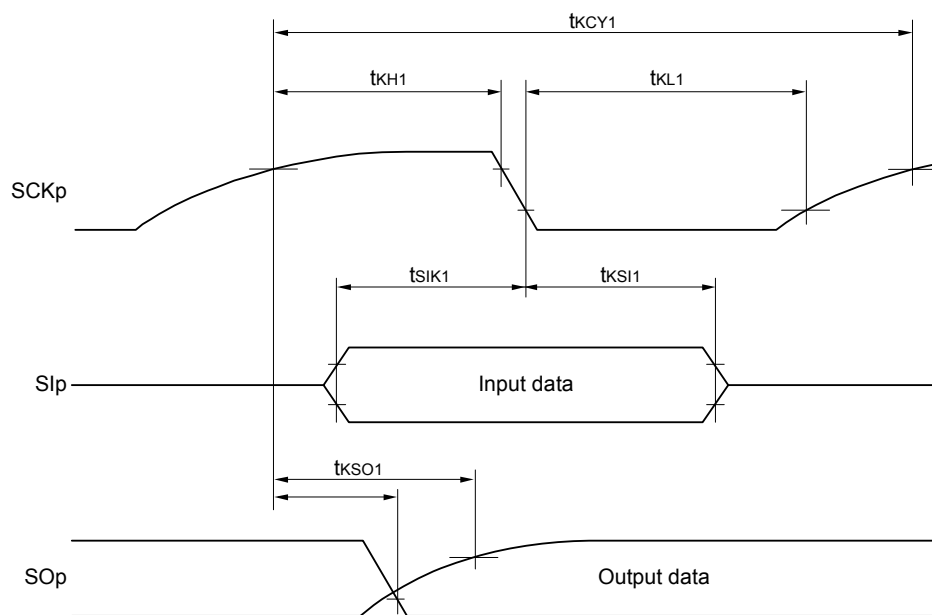


- Remark 1.** Rb[Ω]: Communication line (SCKp, SOp) pull-up resistance, Cb[F]: Communication line (SCKp, SOp) load capacitance, Vb[V]: Communication line voltage
- Remark 2.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)
- Remark 3.** fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))
- Remark 4.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

**CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

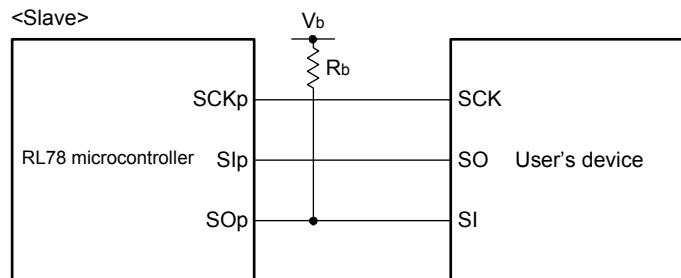
(9) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit	
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
SCKp cycle time Note 1	tkcy2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	24 MHz < fmck	14/fmck		—		—	ns	
			20 MHz < fmck ≤ 24 MHz	12/fmck		—		—	ns	
			8 MHz < fmck ≤ 20 MHz	10/fmck		—		—	ns	
			4 MHz < fmck ≤ 8 MHz	8/fmck		16/fmck		—	ns	
			fmck ≤ 4 MHz	6/fmck		10/fmck		10/fmck	ns	
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	24 MHz < fmck	20/fmck		—		—	ns	
			20 MHz < fmck ≤ 24 MHz	16/fmck		—		—	ns	
			16 MHz < fmck ≤ 20 MHz	14/fmck		—		—	ns	
			8 MHz < fmck ≤ 16 MHz	12/fmck		—		—	ns	
			4 MHz < fmck ≤ 8 MHz	8/fmck		16/fmck		—	ns	
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2	24 MHz < fmck	48/fmck		—		—	ns	
			20 MHz < fmck ≤ 24 MHz	36/fmck		—		—	ns	
			16 MHz < fmck ≤ 20 MHz	32/fmck		—		—	ns	
			8 MHz < fmck ≤ 16 MHz	26/fmck		—		—	ns	
			4 MHz < fmck ≤ 8 MHz	16/fmck		16/fmck		—	ns	
SCKp high-/ low-level width	tkH2, tkL2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	tkcy2/2 - 12		tkcy2/2 - 50		tkcy2/2 - 50		ns	
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	tkcy2/2 - 18		tkcy2/2 - 50		tkcy2/2 - 50		ns	
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2	tkcy2/2 - 50		tkcy2/2 - 50		tkcy2/2 - 50		ns	
	Slp setup time (to SCKp↑) Note 3	tsik2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	1/fmck + 20		1/fmck + 30		1/fmck + 30		ns
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	1/fmck + 20		1/fmck + 30		1/fmck + 30		ns
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2	1/fmck + 30		1/fmck + 30		1/fmck + 30		ns
	Slp hold time (from SCKp↑) Note 4	tksl2		1/fmck + 31		1/fmck + 31		1/fmck + 31		ns
	Delay time from SCKp↓ to SOp output Note 5	tkso2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		2/fmck + 120		2/fmck + 573		2/fmck + 573	ns
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		2/fmck + 214		2/fmck + 573		2/fmck + 573	ns
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 30 pF, Rv = 5.5 kΩ		2/fmck + 573		2/fmck + 573		2/fmck + 573	ns

(Notes, Caution, and Remarks are listed on the next page.)

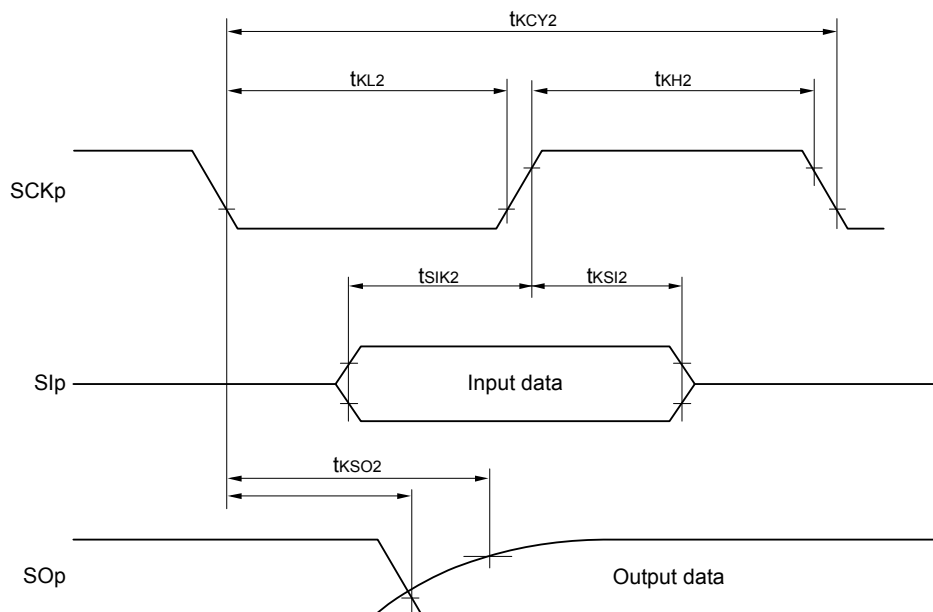
- Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps
- Note 2.** Use it with $EV_{DD0} \geq V_b$.
- Note 3.** When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The Slp setup time becomes “to $SCKp_{\downarrow}$ ” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.
- Note 4.** When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The Slp hold time becomes “from $SCKp_{\downarrow}$ ” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.
- Note 5.** When $DAP_{mn} = 0$ and $CKP_{mn} = 0$, or $DAP_{mn} = 1$ and $CKP_{mn} = 1$. The delay time to SOp output becomes “from $SCKp_{\uparrow}$ ” when $DAP_{mn} = 0$ and $CKP_{mn} = 1$, or $DAP_{mn} = 1$ and $CKP_{mn} = 0$.
- Caution** Select the TTL input buffer for the Slp pin and $SCKp$ pin, and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)

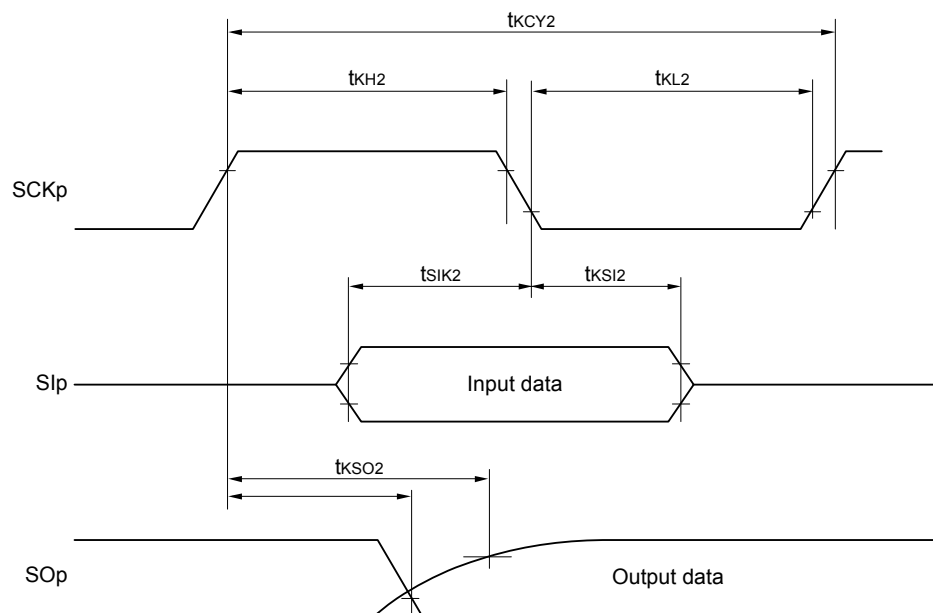


- Remark 1.** $R_b[\Omega]$: Communication line (SOp) pull-up resistance, $C_b[F]$: Communication line (SOp) load capacitance, $V_b[V]$: Communication line voltage
- Remark 2.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)
- Remark 3.** f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the $CKSmn$ bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))
- Remark 4.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)**



Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)**(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	fSCL	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 1		300 Note 1		300 Note 1	kHz
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 1		300 Note 1		300 Note 1	kHz
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ		400 Note 1		300 Note 1		300 Note 1	kHz
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ		400 Note 1		300 Note 1		300 Note 1	kHz
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
Hold time when SCLr = "L"	tLOW	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1550		1550		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	475		1550		1550		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	1150		1550		1550		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	1150		1550		1550		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ	1550		1550		1550		ns
Hold time when SCLr = "H"	tHIGH	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	245		610		610		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	200		610		610		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	675		610		610		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	600		610		610		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ	610		610		610		ns

(10) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)**(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	tsu:DAT	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK + 135 Note 3		1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	1/fMCK + 135 Note 3		1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ	1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		1/fMCK + 190 Note 3		ns
Data hold time (transmission)	tHD:DAT	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V Note 2, Cb = 100 pF, Rb = 5.5 kΩ	0	405	0	405	0	405	ns

Note 1. The value must also be equal to or less than fMCK/4.

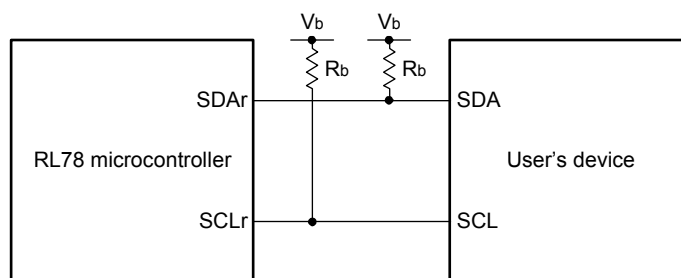
Note 2. Use it with EVDD0 ≥ Vb.

Note 3. Set the fMCK value to keep the hold time of SCLr = "L" and SCLr = "H".

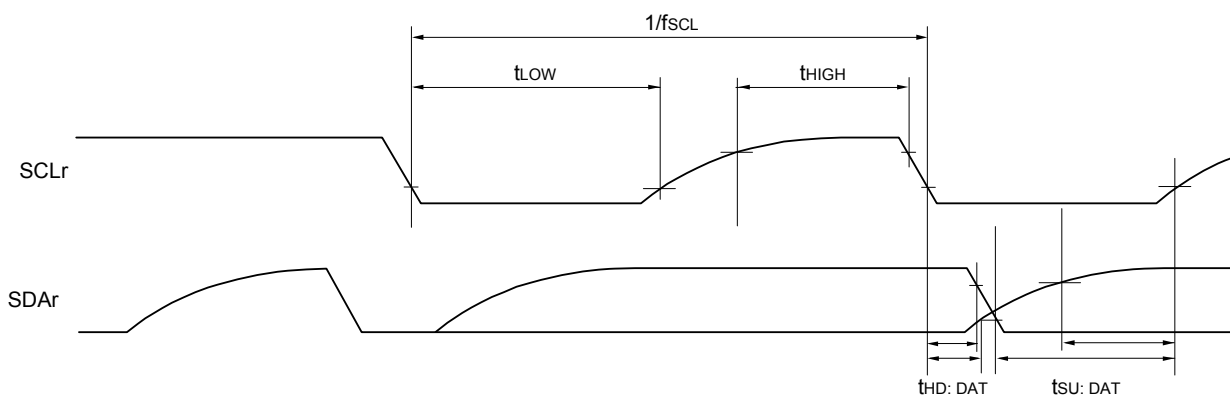
Caution Select the TTL input buffer and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



Remark 1. R_b[Ω]: Communication line (SDAr, SCLr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance, V_b[V]: Communication line voltage

Remark 2. r: IIC number (r = 00, 01, 10, 11, 20, 30, 31), g: PIM, POM number (g = 0, 1, 3 to 5, 14)

Remark 3. f_{MCK}: Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
 n: Channel number (n = 0, 2), mn = 00, 01, 02, 10, 12, 13)

2.5.2 Serial interface IICA

(1) I²C standard mode

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit	
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
SCLA0 clock frequency	f _{SCL}	Standard mode: f _{CLK} ≥ 1 MHz	2.7 V ≤ EVDD0 ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.8 V ≤ EVDD0 ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.7 V ≤ EVDD0 ≤ 5.5 V	0	100	0	100	0	100	kHz
			1.6 V ≤ EVDD0 ≤ 5.5 V	—		0	100	0	100	kHz
Setup time of restart condition	t _{SU, STA}	2.7 V ≤ EVDD0 ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.8 V ≤ EVDD0 ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.7 V ≤ EVDD0 ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.6 V ≤ EVDD0 ≤ 5.5 V	—		4.7		4.7		μs	
Hold time Note 1	t _{HD, STA}	2.7 V ≤ EVDD0 ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.8 V ≤ EVDD0 ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.7 V ≤ EVDD0 ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.6 V ≤ EVDD0 ≤ 5.5 V	—		4.0		4.0		μs	
Hold time when SCLA0 = "L"	t _{LOW}	2.7 V ≤ EVDD0 ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.8 V ≤ EVDD0 ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.7 V ≤ EVDD0 ≤ 5.5 V	4.7		4.7		4.7		μs	
		1.6 V ≤ EVDD0 ≤ 5.5 V	—		4.7		4.7		μs	
Hold time when SCLA0 = "H"	t _{HIGH}	2.7 V ≤ EVDD0 ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.8 V ≤ EVDD0 ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.7 V ≤ EVDD0 ≤ 5.5 V	4.0		4.0		4.0		μs	
		1.6 V ≤ EVDD0 ≤ 5.5 V	—		4.0		4.0		μs	

(Notes, Caution, and Remark are listed on the next page.)

(1) I²C standard mode**(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Data setup time (reception)	tsu: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V	250		250		250		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V	250		250		250		ns
		1.7 V ≤ EVDD0 ≤ 5.5 V	250		250		250		ns
		1.6 V ≤ EVDD0 ≤ 5.5 V	—		250		250		ns
Data hold time (transmission) Note 2	tHD: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
		1.8 V ≤ EVDD0 ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
		1.7 V ≤ EVDD0 ≤ 5.5 V	0	3.45	0	3.45	0	3.45	μs
		1.6 V ≤ EVDD0 ≤ 5.5 V	—		0	3.45	0	3.45	μs
Setup time of stop condition	tsu: STO	2.7 V ≤ EVDD0 ≤ 5.5 V	4.0		4.0		4.0		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V	4.0		4.0		4.0		μs
		1.7 V ≤ EVDD0 ≤ 5.5 V	4.0		4.0		4.0		μs
		1.6 V ≤ EVDD0 ≤ 5.5 V	—		4.0		4.0		μs
Bus-free time	tBUF	2.7 V ≤ EVDD0 ≤ 5.5 V	4.7		4.7		4.7		μs
		1.8 V ≤ EVDD0 ≤ 5.5 V	4.7		4.7		4.7		μs
		1.7 V ≤ EVDD0 ≤ 5.5 V	4.7		4.7		4.7		μs
		1.6 V ≤ EVDD0 ≤ 5.5 V	—		4.7		4.7		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

(2) I²C fast mode

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit	
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
SCLA0 clock frequency	fSCL	Fast mode: fCLK ≥ 3.5 MHz	2.7 V ≤ EVDD0 ≤ 5.5 V	0	400	0	400	0	400	kHz
			1.8 V ≤ EVDD0 ≤ 5.5 V	0	400	0	400	0	400	kHz
Setup time of restart condition	tsu: STA	2.7 V ≤ EVDD0 ≤ 5.5 V	0.6		0.6		0.6		μs	
		1.8 V ≤ EVDD0 ≤ 5.5 V	0.6		0.6		0.6		μs	
Hold time ^{Note 1}	tHD: STA	2.7 V ≤ EVDD0 ≤ 5.5 V	0.6		0.6		0.6		μs	
		1.8 V ≤ EVDD0 ≤ 5.5 V	0.6		0.6		0.6		μs	
Hold time when SCLA0 = "L"	tLOW	2.7 V ≤ EVDD0 ≤ 5.5 V	1.3		1.3		1.3		μs	
		1.8 V ≤ EVDD0 ≤ 5.5 V	1.3		1.3		1.3		μs	
Hold time when SCLA0 = "H"	tHIGH	2.7 V ≤ EVDD0 ≤ 5.5 V	0.6		0.6		0.6		μs	
		1.8 V ≤ EVDD0 ≤ 5.5 V	0.6		0.6		0.6		μs	
Data setup time (reception)	tsu: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V	100		100		100		ns	
		1.8 V ≤ EVDD0 ≤ 5.5 V	100		100		100		ns	
Data hold time (transmission) ^{Note 2}	tHD: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V	0	0.9	0	0.9	0	0.9	μs	
		1.8 V ≤ EVDD0 ≤ 5.5 V	0	0.9	0	0.9	0	0.9	μs	
Setup time of stop condition	tsu: STO	2.7 V ≤ EVDD0 ≤ 5.5 V	0.6		0.6		0.6		μs	
		1.8 V ≤ EVDD0 ≤ 5.5 V	0.6		0.6		0.6		μs	
Bus-free time	tBUF	2.7 V ≤ EVDD0 ≤ 5.5 V	1.3		1.3		1.3		μs	
		1.8 V ≤ EVDD0 ≤ 5.5 V	1.3		1.3		1.3		μs	

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

(3) I²C fast mode plus

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fSCL	Fast mode plus: fCLK ≥ 10 MHz 2.7 V ≤ EVDD0 ≤ 5.5 V	0	1000	—	—	—	—	kHz
Setup time of restart condition	tSU: STA	2.7 V ≤ EVDD0 ≤ 5.5 V	0.26		—	—	—	—	μs
Hold time Note 1	tHD: STA	2.7 V ≤ EVDD0 ≤ 5.5 V	0.26		—	—	—	—	μs
Hold time when SCLA0 = "L"	tLOW	2.7 V ≤ EVDD0 ≤ 5.5 V	0.5		—	—	—	—	μs
Hold time when SCLA0 = "H"	tHIGH	2.7 V ≤ EVDD0 ≤ 5.5 V	0.26		—	—	—	—	μs
Data setup time (reception)	tSU: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V	50		—	—	—	—	ns
Data hold time (transmission) Note 2	tHD: DAT	2.7 V ≤ EVDD0 ≤ 5.5 V	0	0.45	—	—	—	—	μs
Setup time of stop condition	tSU: STO	2.7 V ≤ EVDD0 ≤ 5.5 V	0.26		—	—	—	—	μs
Bus-free time	tBUF	2.7 V ≤ EVDD0 ≤ 5.5 V	0.5		—	—	—	—	μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

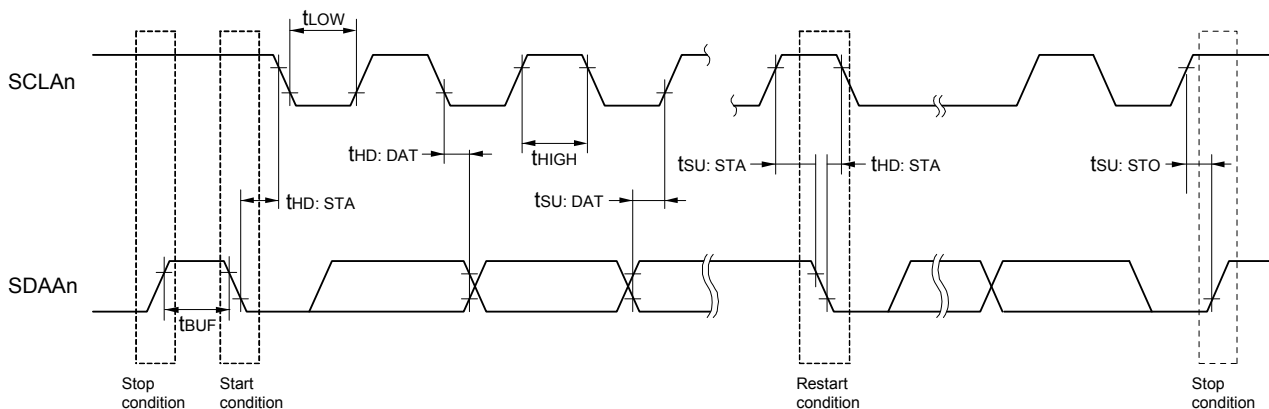
Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

Note 3. The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.

Fast mode plus: Cb = 120 pF, Rb = 1.1 kΩ

I²C serial transfer timing



Remark n = 0, 1

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage	Reference voltage (+) = AV _{REFP} Reference voltage (-) = AV _{REFM}	Reference voltage (+) = V _{DD} Reference voltage (-) = V _{SS}	Reference voltage (+) = V _{BGR} Reference voltage (-) = AV _{REFM}
ANI0 to ANI14		Refer to 2.6.1 (1).	Refer to 2.6.1 (3).	Refer to 2.6.1 (4).
ANI16 to ANI20		Refer to 2.6.1 (2).		
Internal reference voltage Temperature sensor output voltage		Refer to 2.6.1 (1).		

(1) When reference voltage (+) = AV_{REFP}/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AV_{REFM}/ANI1 (ADREFM = 1), target pin: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

(TA = -40 to +85°C, 1.6 V ≤ AV_{REFP} ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V, Reference voltage (+) = AV_{REFP}, Reference voltage (-) = AV_{REFM} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error Note 1	AINL	10-bit resolution AV _{REFP} = V _{DD} Note 3	1.8 V ≤ AV _{REFP} ≤ 5.5 V	1.2	±3.5	LSB
			1.6 V ≤ AV _{REFP} ≤ 5.5 V Note 4	1.2	±7.0	LSB
Conversion time	t _{CONV}	10-bit resolution Target pin: ANI2 to ANI14	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125	39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875	39	μs
			1.8 V ≤ V _{DD} ≤ 5.5 V	17	39	μs
			1.6 V ≤ V _{DD} ≤ 5.5 V	57	95	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V _{DD} ≤ 5.5 V	2.375	39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.5625	39	μs
Zero-scale error Notes 1, 2	E _{ZS}	10-bit resolution AV _{REFP} = V _{DD} Note 3	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±0.25	%FSR
			1.6 V ≤ AV _{REFP} ≤ 5.5 V Note 4		±0.50	%FSR
Full-scale error Notes 1, 2	E _{FS}	10-bit resolution AV _{REFP} = V _{DD} Note 3	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±0.25	%FSR
			1.6 V ≤ AV _{REFP} ≤ 5.5 V Note 4		±0.50	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AV _{REFP} = V _{DD} Note 3	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±2.5	LSB
			1.6 V ≤ AV _{REFP} ≤ 5.5 V Note 4		±5.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution AV _{REFP} = V _{DD} Note 3	1.8 V ≤ AV _{REFP} ≤ 5.5 V		±1.5	LSB
			1.6 V ≤ AV _{REFP} ≤ 5.5 V Note 4		±2.0	LSB
Analog input voltage	V _{AIN}	ANI2 to ANI14	0		AV _{REFP}	V
		Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)			V _{BGR} Note 5	V
		Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)			V _{TMPS25} Note 5	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When AV_{REFP} < V_{DD}, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AV_{REFP} = V_{DD}.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AV_{REFP} = V_{DD}.

Note 4. Values when the conversion time is set to 57 μs (min.) and 95 μs (max.).

Note 5. Refer to 2.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin: ANI16 to ANI20

(TA = -40 to +85°C, $1.6\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $1.6\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Resolution	RES		8		10	bit	
Overall error Note 1	AINL	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		1.2	±5.0	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5		1.2	±8.5	LSB
Conversion time	t _{CONV}	10-bit resolution Target ANI pin: ANI16 to ANI20	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
			$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	57		95	μs
Zero-scale error Notes 1, 2	E _{ZS}	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			±0.35	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5			±0.60	%FSR
Full-scale error Notes 1, 2	E _{FS}	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			±0.35	%FSR
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5			±0.60	%FSR
Integral linearity error Note 1	ILE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			±3.5	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5			±6.0	LSB
Differential linearity error Note 1	DLE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			±2.0	LSB
			$1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ Note 5			±2.5	LSB
Analog input voltage	V _{AIN}	ANI16 to ANI20	0		AV_{REFP} and EV_{DD0}	V	

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When $EV_{DD0} \leq AV_{REFP} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Note 4. When $AV_{REFP} < EV_{DD0} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Zero-scale error/Full-scale error: Add $\pm 0.20\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.

Integral linearity error/ Differential linearity error: Add ± 2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Note 5. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

- (3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI14, ANI16 to ANI20, internal reference voltage, and temperature sensor output voltage

(TA = -40 to +85°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Resolution	RES		8		10	bit	
Overall error Note 1	AINL	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V		1.2	±7.0	LSB
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3		1.2	±10.5	LSB
Conversion time	t _{CONV}	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI20	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875		39	μs
			1.8 V ≤ V _{DD} ≤ 5.5 V	17		39	μs
			1.6 V ≤ V _{DD} ≤ 5.5 V	57		95	μs
		10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V _{DD} ≤ 5.5 V	2.375		39	μs
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.5625		39	μs
2.4 V ≤ V _{DD} ≤ 5.5 V	17			39	μs		
Zero-scale error Notes 1, 2	E _{ZS}	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±0.85	%FSR
Full-scale error Notes 1, 2	E _{FS}	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±0.85	%FSR
Integral linearity error Note 1	ILE	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±4.0	LSB
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±6.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution	1.8 V ≤ V _{DD} ≤ 5.5 V			±2.0	LSB
			1.6 V ≤ V _{DD} ≤ 5.5 V Note 3			±2.5	LSB
Analog input voltage	V _{AIN}	ANI0 to ANI14	0		V _{DD}	V	
		ANI16 to ANI20	0		EV _{DD0}	V	
		Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)			V _{BGR} Note 4	V	
		Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)			V _{TMPS25} Note 4	V	

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. When the conversion time is set to 57 μs (min.) and 95 μs (max.).

Note 4. Refer to 2.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

- (4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 to ANI14, ANI16 to ANI20

(TA = -40 to +85°C, 2.4 V ≤ VDD ≤ 5.5 V, 1.6 V ≤ EVDD = EVDD1 ≤ VDD, VSS = EVSS0 = EVSS1 = 0 V, Reference voltage (+) = VBGR ^{Note 3}, Reference voltage (-) = AVREFM = 0 V ^{Note 4}, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	tCONV	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	Ezs	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±0.60	% FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±1.0	LSB
Analog input voltage	VAIN			0		VBGR ^{Note 3}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to **2.6.2 Temperature sensor characteristics/internal reference voltage characteristic**.

Note 4. When reference voltage (-) = VSS, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AVREFM.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AVREFM.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AVREFM.

2.6.2 Temperature sensor characteristics/internal reference voltage characteristic

(TA = -40 to +85°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	VTMPS25	Setting ADS register = 80H, TA = +25°C		1.05		V
Internal reference voltage	VBGR	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	FVTMPS	Temperature sensor that depends on the temperature		-3.6		mV/°C
Operation stabilization wait time	tAMP		5			μs

2.6.3 D/A converter characteristics

(TA = -40 to +85°C, 1.6 V ≤ EVSS0 = EVSS1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 MΩ	1.8 V ≤ VDD ≤ 5.5 V			±2.5	LSB
		Rload = 8 MΩ	1.8 V ≤ VDD ≤ 5.5 V			±2.5	LSB
Settling time	tSET	Cload = 20 pF	2.7 V ≤ VDD ≤ 5.5 V			3	μs
			1.6 V ≤ VDD < 2.7 V			6	μs

2.6.4 Comparator

(TA = -40 to +85°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage range	Ivref		0		EVDD0 - 1.4	V	
	Ivcmp		-0.3		EVDD0 + 0.3	V	
Output delay	td	VDD = 3.0 V Input slew rate > 50 mV/μs	Comparator high-speed mode, standard mode			1.2	μs
			Comparator high-speed mode, window mode			2.0	μs
			Comparator low-speed mode, standard mode		3.0	5.0	μs
High-electric-potential reference voltage	VTW+	Comparator high-speed mode, window mode		0.76 VDD		V	
Low-electric-potential reference voltage	VTW-	Comparator high-speed mode, window mode		0.24 VDD		V	
Operation stabilization wait time	tcMP		100			μs	
Internal reference voltage Note	VBGR	2.4 V ≤ VDD ≤ 5.5 V, HS (high-speed main) mode	1.38	1.45	1.50	V	

Note Not usable in LS (low-speed main) mode, LV (low-voltage main) mode, sub-clock operation, or STOP mode.

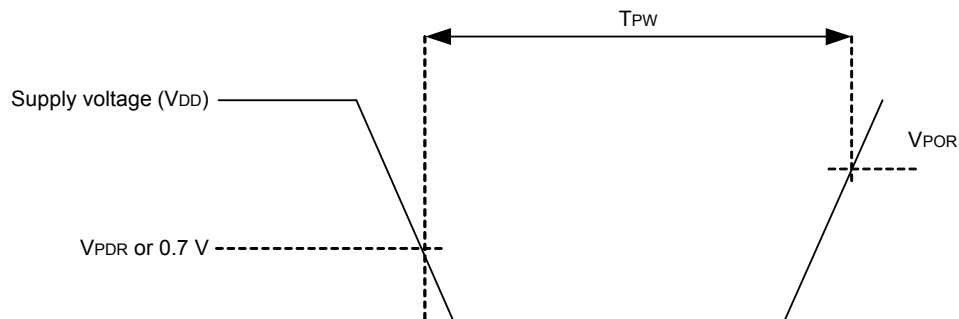
2.6.5 POR circuit characteristics

(TA = -40 to +85°C, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power on/down reset threshold	VPOR	Voltage threshold on VDD rising	1.47	1.51	1.55	V
	VPDR	Voltage threshold on VDD falling Note 1	1.46	1.50	1.54	V
Minimum pulse width Note 2	TPW		300			μs

Note 1. However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in 2.4 AC Characteristics.

Note 2. Minimum time required for a POR reset when VDD exceeds below VPDR. This is also the minimum time required for a POR reset from when VDD exceeds below 0.7 V to when VDD exceeds VPOR while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



2.6.6 LVD circuit characteristics

(1) Reset Mode and Interrupt Mode

(TA = -40 to +85°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	Supply voltage level	VLVD0	Rising edge	3.98	4.06	4.14	V
			Falling edge	3.90	3.98	4.06	V
		VLVD1	Rising edge	3.68	3.75	3.82	V
			Falling edge	3.60	3.67	3.74	V
		VLVD2	Rising edge	3.07	3.13	3.19	V
			Falling edge	3.00	3.06	3.12	V
		VLVD3	Rising edge	2.96	3.02	3.08	V
			Falling edge	2.90	2.96	3.02	V
		VLVD4	Rising edge	2.86	2.92	2.97	V
			Falling edge	2.80	2.86	2.91	V
		VLVD5	Rising edge	2.76	2.81	2.87	V
			Falling edge	2.70	2.75	2.81	V
		VLVD6	Rising edge	2.66	2.71	2.76	V
			Falling edge	2.60	2.65	2.70	V
		VLVD7	Rising edge	2.56	2.61	2.66	V
			Falling edge	2.50	2.55	2.60	V
		VLVD8	Rising edge	2.45	2.50	2.55	V
			Falling edge	2.40	2.45	2.50	V
		VLVD9	Rising edge	2.05	2.09	2.13	V
			Falling edge	2.00	2.04	2.08	V
		VLVD10	Rising edge	1.94	1.98	2.02	V
			Falling edge	1.90	1.94	1.98	V
		VLVD11	Rising edge	1.84	1.88	1.91	V
			Falling edge	1.80	1.84	1.87	V
		VLVD12	Rising edge	1.74	1.77	1.81	V
			Falling edge	1.70	1.73	1.77	V
VLVD13	Rising edge	1.64	1.67	1.70	V		
	Falling edge	1.60	1.63	1.66	V		
Minimum pulse width		tLW		300			μs
Detection delay time						300	μs

(2) Interrupt & Reset Mode**(TA = -40 to +85°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Voltage detection threshold	VLVDA0	VPOC2, VPOC1, VPOC0 = 0, 0, 0, falling reset voltage	1.60	1.63	1.66	V	
	VLVDA1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.74	1.77	1.81	V
			Falling interrupt voltage	1.70	1.73	1.77	V
	VLVDA2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	1.84	1.88	1.91	V
			Falling interrupt voltage	1.80	1.84	1.87	V
	VLVDA3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	2.86	2.92	2.97	V
			Falling interrupt voltage	2.80	2.86	2.91	V
	VLVDB0	VPOC2, VPOC1, VPOC0 = 0, 0, 1, falling reset voltage	1.80	1.84	1.87	V	
	VLVDB1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	1.94	1.98	2.02	V
			Falling interrupt voltage	1.90	1.94	1.98	V
	VLVDB2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.05	2.09	2.13	V
			Falling interrupt voltage	2.00	2.04	2.08	V
VLVDB3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.07	3.13	3.19	V	
		Falling interrupt voltage	3.00	3.06	3.12	V	
VLVDC0	VPOC2, VPOC1, VPOC0 = 0, 1, 0, falling reset voltage	2.40	2.45	2.50	V		
VLVDC1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.56	2.61	2.66	V	
		Falling interrupt voltage	2.50	2.55	2.60	V	
VLVDC2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.66	2.71	2.76	V	
		Falling interrupt voltage	2.60	2.65	2.70	V	
VLVDC3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.68	3.75	3.82	V	
		Falling interrupt voltage	3.60	3.67	3.74	V	
VLVDD0	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage	2.70	2.75	2.81	V		
VLVDD1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.86	2.92	2.97	V	
		Falling interrupt voltage	2.80	2.86	2.91	V	
VLVDD2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.96	3.02	3.08	V	
		Falling interrupt voltage	2.90	2.96	3.02	V	
VLVDD3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.98	4.06	4.14	V	
		Falling interrupt voltage	3.90	3.98	4.06	V	

2.6.7 Power supply voltage rising slope characteristics**(TA = -40 to +85°C, VSS = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SVDD				54	V/ms

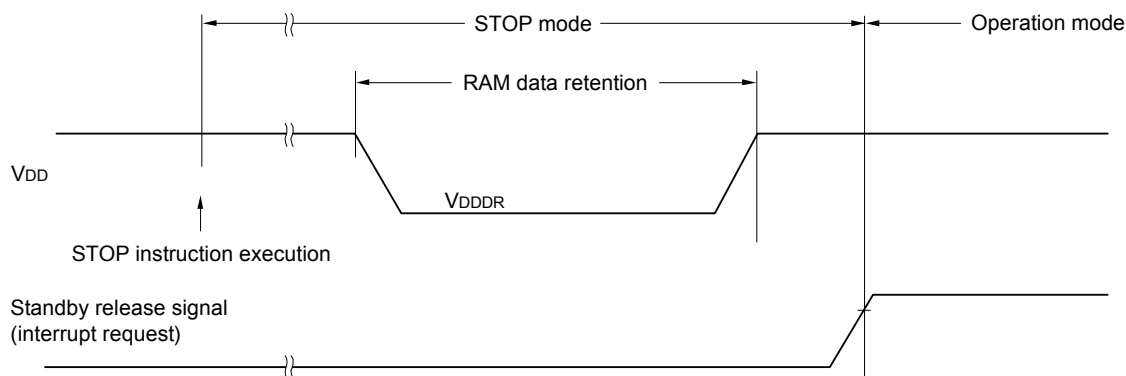
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until VDD reaches the operating voltage range shown in 2.4 AC Characteristics.

2.7 RAM Data Retention Characteristics

(TA = -40 to +85°C, VSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.46 <small>Note</small>		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



2.8 Flash Memory Programming Characteristics

(TA = -40 to +85°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK	1.8 V ≤ VDD ≤ 5.5 V	1		32	MHz
Number of code flash rewrites <small>Notes 1, 2, 3</small>	C _{erwr}	Retained for 20 years TA = 85°C	1,000			Times
Number of data flash rewrites <small>Notes 1, 2, 3</small>		Retained for 1 year TA = 25°C		1,000,000		
		Retained for 5 years TA = 85°C	100,000			
		Retained for 20 years TA = 85°C	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.9 Dedicated Flash Memory Programmer Communication (UART)

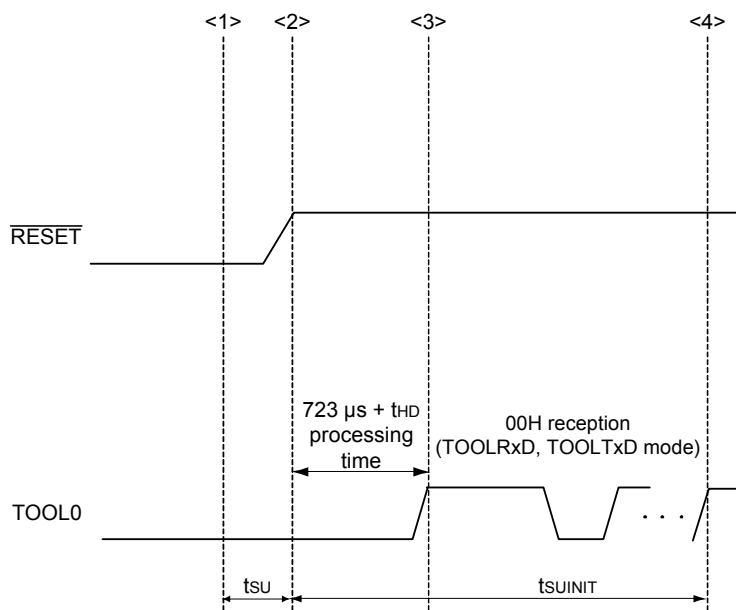
(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.10 Timing of Entry to Flash Memory Programming Modes

(TA = -40 to +85°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	tsuINIT	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	tsu	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	tHD	POR and LVD reset must end before the external reset ends.	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset ends (POR and LVD reset must end before the external reset ends).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark tsuINIT: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.
 tsu: How long from when the TOOL0 pin is placed at the low level until a pin reset ends
 tHD: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

3. ELECTRICAL SPECIFICATIONS (G: INDUSTRIAL APPLICATIONS $T_A = -40$ to $+105^\circ\text{C}$)

This chapter describes the following electrical specifications.

Target products G: Industrial applications $T_A = -40$ to $+105^\circ\text{C}$

R5F104xxGxx

Caution 1. The RL78 microcontrollers have an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

Caution 2. With products not provided with an EVDD0, EVDD1, EVSS0, or EVSS1 pin, replace EVDD0 and EVDD1 with VDD, or replace EVSS0 and EVSS1 with VSS.

Caution 3. The pins mounted depend on the product. Refer to 2.1 Port Functions to 2.2.1 Functions for each product in the RL78/G14 User's Manual.

Caution 4. Please contact Renesas Electronics sales office for derating of operation under $T_A = +85$ to $+105^\circ\text{C}$. Derating is the systematic reduction of load for the sake of improved reliability.

Remark When RL78/G14 is used in the range of $T_A = -40$ to $+85^\circ\text{C}$, see 2. ELECTRICAL SPECIFICATIONS ($T_A = -40$ to $+85^\circ\text{C}$).

Operation of products rated “G: Industrial applications (TA = -40 to + 105°C)” at ambient operating temperatures above 85°C differs from that of products rated “A: Consumer applications” and “D: Industrial applications” in the ways listed below.

Parameter	A: Consumer applications, D: Industrial applications	G: Industrial applications
Operating ambient temperature	TA = -40 to +85°C	TA = -40 to +105°C
Operating mode Operating voltage range	HS (high-speed main) mode: 2.7 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 32 MHz 2.4 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 16 MHz LS (low-speed main) mode: 1.8 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 8 MHz LV (low-voltage main) mode: 1.6 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 4 MHz	HS (high-speed main) mode only: 2.7 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 32 MHz 2.4 V ≤ V _{DD} ≤ 5.5 V@1 MHz to 16 MHz
High-speed on-chip oscillator clock accuracy	1.8 V ≤ V _{DD} ≤ 5.5 V: ±1.0% @ TA = -20 to +85°C ±1.5% @ TA = -40 to -20°C 1.6 V ≤ V _{DD} < 1.8 V: ±5.0% @ TA = -20 to +85°C ±5.5% @ TA = -40 to -20°C	2.4 V ≤ V _{DD} ≤ 5.5 V: ±2.0% @ TA = +85 to +105°C ±1.0% @ TA = -20 to +85°C ±1.5% @ TA = -40 to -20°C
Serial array unit	UART CSI: f _{CLK} /2 (16 Mbps supported), f _{CLK} /4 Simplified I ² C communication	UART CSI: f _{CLK} /4 Simplified I ² C communication
IICA	Standard mode Fast mode Fast mode plus	Standard mode Fast mode
Voltage detector	• Rising: 1.67 V to 4.06 V (14 stages) • Falling: 1.63 V to 3.98 V (14 stages)	• Rising: 2.61 V to 4.06 V (8 stages) • Falling: 2.55 V to 3.98 V (8 stages)

Remark The electrical characteristics of products rated “G: Industrial applications (TA = -40 to + 105°C)” at ambient operating temperatures above 85°C differ from those of products rated “A: Consumer applications” and “D: Industrial applications”. For details, refer to 3.1 to 3.10.

3.1 Absolute Maximum Ratings

Absolute Maximum Ratings

(1/2)

Parameter	Symbols	Conditions	Ratings	Unit
Supply voltage	V _{DD}		-0.5 to +6.5	V
	EV _{DD0} , EV _{DD1}	EV _{DD0} = EV _{DD1}	-0.5 to +6.5	V
	EV _{SS0} , EV _{SS1}	EV _{SS0} = EV _{SS1}	-0.5 to +0.3	V
REGC pin input voltage	V _{IREGC}	REGC	-0.3 to +2.8 and -0.3 to V _{DD} +0.3 Note 1	V
Input voltage	V _{I1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	-0.3 to EV _{DD0} +0.3 and -0.3 to V _{DD} +0.3 Note 2	V
	V _{I2}	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	V _{I3}	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to V _{DD} +0.3 Note 2	V
Output voltage	V _{O1}	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-0.3 to EV _{DD0} +0.3 and -0.3 to V _{DD} +0.3 Note 2	V
	V _{O2}	P20 to P27, P150 to P156	-0.3 to V _{DD} +0.3 Note 2	V
Analog input voltage	V _{AI1}	ANI16 to ANI20	-0.3 to EV _{DD0} +0.3 and -0.3 to AV _{REF} (+) +0.3 Notes 2, 3	V
	V _{AI2}	ANI0 to ANI14	-0.3 to V _{DD} +0.3 and -0.3 to AV _{REF} (+) +0.3 Notes 2, 3	V

Note 1. Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Must be 6.5 V or lower.

Note 3. Do not exceed AV_{REF} (+) + 0.3 V in case of A/D conversion target pin.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. AV_{REF} (+): + side reference voltage of the A/D converter.

Remark 3. V_{SS}: Reference voltage

Absolute Maximum Ratings

(2/2)

Parameter	Symbols	Conditions		Ratings	Unit
Output current, high	IOH1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	-40	mA
		Total of all pins	P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	-70	mA
		-170 mA	P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	-100	mA
	IOH2	Per pin	P20 to P27, P150 to P156	-0.5	mA
		Total of all pins		-2	mA
	Output current, low	IOL1	Per pin	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	40
Total of all pins			P00 to P04, P40 to P47, P102, P120, P130, P140 to P145	70	mA
170 mA			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147	100	mA
IOL2		Per pin	P20 to P27, P150 to P156	1	mA
		Total of all pins		5	mA
Operating ambient temperature		TA	In normal operation mode	-40 to +105	°C
	In flash memory programming mode				
Storage temperature	Tstg		-65 to +150	°C	

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.2 Oscillator Characteristics

3.2.1 X1, XT1 characteristics

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Resonator	Resonator	Conditions	MIN.	TYP.	MAX.	Unit
X1 clock oscillation frequency (fX) ^{Note}	Ceramic resonator/ crystal resonator	2.7 V ≤ VDD ≤ 5.5 V	1.0		20.0	MHz
		2.4 V ≤ VDD < 2.7 V	1.0		16.0	
XT1 clock oscillation frequency (fXT) ^{Note}	Crystal resonator		32	32.768	35	kHz

Note Indicates only permissible oscillator frequency ranges. Refer to **AC Characteristics** for instruction execution time. Request evaluation by the manufacturer of the oscillator circuit mounted on a board to check the oscillator characteristics.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after a reset release, check the X1 clock oscillation stabilization time using the oscillation stabilization time counter status register (OSTC) by the user. Determine the oscillation stabilization time of the OSTC register and the oscillation stabilization time select register (OSTS) after sufficiently evaluating the oscillation stabilization time with the resonator to be used.

Remark When using the X1 oscillator and XT1 oscillator, refer to 5.4 System Clock Oscillator in the RL78/G14 User's Manual.

3.2.2 On-chip oscillator characteristics

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Oscillators	Parameters	Conditions		MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Notes 1, 2	f _H			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy		-20 to +85°C	2.4 V ≤ VDD ≤ 5.5 V	-1.0		+1.0	%
		-40 to -20°C	2.4 V ≤ VDD ≤ 5.5 V	-1.5		+1.5	%
		+85 to +105°C	2.4 V ≤ VDD ≤ 5.5 V	-2.0		+2.0	%
Low-speed on-chip oscillator clock frequency	f _L				15		kHz
Low-speed on-chip oscillator clock frequency accuracy				-15		+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to **AC Characteristics** for instruction execution time.

3.3 DC Characteristics

3.3.1 Pin characteristics

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Output current, high ^{Note 1}	IOH1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	2.4 V ≤ EVDD0 ≤ 5.5 V			-3.0 Note 2	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V			-30.0	mA
			2.7 V ≤ EVDD0 < 4.0 V			-10.0	mA
			2.4 V ≤ EVDD0 < 2.7 V			-5.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V			-30.0	mA
			2.7 V ≤ EVDD0 < 4.0 V			-19.0	mA
	2.4 V ≤ EVDD0 < 2.7 V				-10.0	mA	
	Total of all pins (When duty ≤ 70% ^{Note 3})	2.4 V ≤ EVDD0 ≤ 5.5 V			-60.0	mA	
	IOH2	Per pin for P20 to P27, P150 to P156	2.4 V ≤ VDD ≤ 5.5 V			-0.1 Note 2	mA
		Total of all pins (When duty ≤ 70% ^{Note 3})	2.4 V ≤ VDD ≤ 5.5 V			-1.5	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the EVDD0, EVDD1, VDD pins to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOH × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOH = -10.0 mA

$$\text{Total output current of pins} = (-10.0 \times 0.7)/(80 \times 0.01) \approx -8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low ^{Note 1}	IOL1	Per pin for P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147			8.5 Note 2	mA
					15.0 Note 2	mA
					40.0	mA
		Total of P00 to P04, P40 to P47, P102, P120, P130, P140 to P145 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V		40.0	mA
			2.7 V ≤ EVDD0 < 4.0 V		15.0	mA
			2.4 V ≤ EVDD0 < 2.7 V		9.0	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P100, P101, P110, P111, P146, P147 (When duty ≤ 70% ^{Note 3})	4.0 V ≤ EVDD0 ≤ 5.5 V		40.0	mA
	2.7 V ≤ EVDD0 < 4.0 V			35.0	mA	
	2.4 V ≤ EVDD0 < 2.7 V			20.0	mA	
	Total of all pins (When duty ≤ 70% ^{Note 3})			80.0	mA	
	IOL2	Per pin for P20 to P27, P150 to P156			0.4 Note 2	mA
2.4 V ≤ VDD ≤ 5.5 V				5.0	mA	

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the EVSS0, EVSS1, and VSS pins.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70%.

The output current value that has changed to the duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

- Total output current of pins = (IOL × 0.7)/(n × 0.01)

<Example> Where n = 80% and IOL = 10.0 mA

$$\text{Total output current of pins} = (10.0 \times 0.7)/(80 \times 0.01) \approx 8.7 \text{ mA}$$

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(3/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Input voltage, high	VIH1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Normal input buffer	0.8 EVDD0		EVDD0	V
	VIH2	P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	2.2		EVDD0	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	2.0		EVDD0	V
			TTL input buffer 2.4 V ≤ EVDD0 < 3.3 V	1.5		EVDD0	V
	VIH3	P20 to P27, P150 to P156		0.7 VDD		VDD	V
	VIH4	P60 to P63		0.7 EVDD0		6.0	V
VIH5	P121 to P124, P137, EXCLK, EXCLKS, RESET		0.8 VDD		VDD	V	
Input voltage, low	UIL1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Normal input buffer	0		0.2 EVDD0	V
	UIL2	P01, P03, P04, P10, P14 to P17, P30, P43, P44, P50, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	0		0.5	V
			TTL input buffer 2.4 V ≤ EVDD0 < 3.3 V	0		0.32	V
	UIL3	P20 to P27, P150 to P156		0		0.3 VDD	V
	UIL4	P60 to P63		0		0.3 EVDD0	V
UIL5	P121 to P124, P137, EXCLK, EXCLKS, RESET		0		0.2 VDD	V	

Caution The maximum value of VIH of pins P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, and P142 to P144 is EVDD0, even in the N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(4/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage, high	VOH1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -3.0 mA			V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -2.0 mA			V
			2.4 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -1.5 mA			V
	VOH2	P20 to P27, P150 to P156	2.4 V ≤ VDD ≤ 5.5 V, IOH2 = -100 μA			V
Output voltage, low	VOL1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P130, P140 to P147	4.0 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 8.5 mA		0.7	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 3.0 mA		0.6	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 1.5 mA		0.4	V
			2.4 V ≤ EVDD0 ≤ 5.5 V, IOL1 = 0.6 mA		0.4	V
	VOL2	P20 to P27, P150 to P156	2.4 V ≤ VDD ≤ 5.5 V, IOL2 = 400 μA		0.4	V
	VOL3	P60 to P63	4.0 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 15.0 mA		2.0	V
			4.0 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 5.0 mA		0.4	V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 3.0 mA		0.4	V
			2.4 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 2.0 mA		0.4	V

Caution P00, P02 to P04, P10, P11, P13 to P15, P17, P30, P43 to P45, P50 to P55, P71, P74, P80 to P82, P142 to P144 do not output high level in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(5/5)

Items	Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Input leakage current, high	ILIH1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Vi = EVDD0			1	μA	
	ILIH2	P20 to P27, P137, P150 to P156, RESET	Vi = VDD			1	μA	
	ILIH3	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	Vi = VDD	In input port or external clock input		1	μA	
				In resonator connection		10	μA	
Input leakage current, low	ILIL1	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Vi = EVSS0			-1	μA	
	ILIL2	P20 to P27, P137, P150 to P156, RESET	Vi = VSS			-1	μA	
	ILIL3	P121 to P124 (X1, X2, EXCLK, XT1, XT2, EXCLKS)	Vi = VSS	In input port or external clock input		-1	μA	
				In resonator connection		-10	μA	
On-chip pull-up resistance	Ru	P00 to P06, P10 to P17, P30, P31, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P100 to P102, P110, P111, P120, P140 to P147	Vi = EVSS0, In input port		10	20	100	kΩ

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

3.3.2 Supply current characteristics

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit		
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.4		mA	
						VDD = 3.0 V		2.4			
					fHOCO = 32 MHz, fIH = 32 MHz Note 3	Basic operation	VDD = 5.0 V		2.1		mA
							VDD = 3.0 V		2.1		
				HS (high-speed main) mode Note 5	fHOCO = 64 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V		5.1	9.3	mA
						VDD = 3.0 V		5.1	9.3		
					fHOCO = 32 MHz, fIH = 32 MHz Note 3	Normal operation	VDD = 5.0 V		4.8	8.7	mA
							VDD = 3.0 V		4.8	8.7	
					fHOCO = 48 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V		4.0	7.3	mA
							VDD = 3.0 V		4.0	7.3	
				fHOCO = 24 MHz, fIH = 24 MHz Note 3	Normal operation	VDD = 5.0 V		3.8	6.7	mA	
						VDD = 3.0 V		3.8	6.7		
				fHOCO = 16 MHz, fIH = 16 MHz Note 3	Normal operation	VDD = 5.0 V		2.8	4.9	mA	
						VDD = 3.0 V		2.8	4.9		
			HS (high-speed main) mode Note 5	fMX = 20 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		3.3	5.7	mA	
						Resonator connection		3.4	5.8		
				fMX = 20 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		3.3	5.7	mA	
						Resonator connection		3.4	5.8		
				fMX = 10 MHz Note 2, VDD = 5.0 V	Normal operation	Square wave input		2.0	3.4	mA	
						Resonator connection		2.1	3.5		
				fMX = 10 MHz Note 2, VDD = 3.0 V	Normal operation	Square wave input		2.0	3.4	mA	
	Resonator connection					2.1	3.5				
	Subsystem clock operation	fSUB = 32.768 kHz Note 4 TA = -40°C	Normal operation	Square wave input		4.7	6.1	μA			
				Resonator connection		4.7	6.1				
		fSUB = 32.768 kHz Note 4 TA = +25°C	Normal operation	Square wave input		4.7	6.1	μA			
				Resonator connection		4.7	6.1				
		fSUB = 32.768 kHz Note 4 TA = +50°C	Normal operation	Square wave input		4.8	6.7	μA			
				Resonator connection		4.8	6.7				
	fSUB = 32.768 kHz Note 4 TA = +70°C	Normal operation	Square wave input		4.8	7.5	μA				
			Resonator connection		4.8	7.5					
	fSUB = 32.768 kHz Note 4 TA = +85°C	Normal operation	Square wave input		5.4	8.9	μA				
			Resonator connection		5.4	8.9					
	fSUB = 32.768 kHz Note 4 TA = +105°C	Normal operation	Square wave input		7.2	21.0	μA				
			Resonator connection		7.3	21.1					

(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 3.** When high-speed system clock and subsystem clock are stopped.
- Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

Remark 1. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation, temperature condition of the TYP. value is TA = 25°C

(1) Flash ROM: 16 to 64 KB of 30- to 64-pin products**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)(2/2)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V	0.80	4.36	mA
					VDD = 3.0 V	0.80	4.36	
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V	0.49	3.67	
					VDD = 3.0 V	0.49	3.67	
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V	0.62	3.42	
					VDD = 3.0 V	0.62	3.42	
			fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V	0.4	2.85		
				VDD = 3.0 V	0.4	2.85		
			fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V	0.37	2.08		
				VDD = 3.0 V	0.37	2.08		
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input	0.28	2.45	mA
					Resonator connection	0.40	2.57	
				fMX = 20 MHz Note 3, VDD = 3.0 V	Square wave input	0.28	2.45	
					Resonator connection	0.40	2.57	
				fMX = 10 MHz Note 3, VDD = 5.0 V	Square wave input	0.19	1.28	
					Resonator connection	0.25	1.36	
				fMX = 10 MHz Note 3, VDD = 3.0 V	Square wave input	0.19	1.28	
					Resonator connection	0.25	1.36	
		Subsystem clock operation	fsUB = 32.768 kHz Note 5, TA = -40°C	Square wave input	0.25	0.57	μA	
				Resonator connection	0.44	0.76		
			fsUB = 32.768 kHz Note 5, TA = +25°C	Square wave input	0.30	0.57		
				Resonator connection	0.49	0.76		
			fsUB = 32.768 kHz Note 5, TA = +50°C	Square wave input	0.36	1.17		
				Resonator connection	0.59	1.36		
fsUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.49	1.97				
	Resonator connection		0.72	2.16				
fsUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		0.97	3.37				
	Resonator connection		1.16	3.56				
fsUB = 32.768 kHz Note 5, TA = +105°C	Square wave input		3.20	17.10				
	Resonator connection		3.40	17.50				
IDD3 Note 6	STOP mode Note 8	TA = -40°C		0.18	0.51	μA		
		TA = +25°C		0.24	0.51			
		TA = +50°C		0.29	1.10			
		TA = +70°C		0.41	1.90			
		TA = +85°C		0.90	3.30			
		TA = +105°C		3.10	17.00			

(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into V_{DD} and EV_{DD0}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** During HALT instruction execution by flash memory.
- Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 4.** When high-speed system clock and subsystem clock are stopped.
- Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
- Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is TA = 25°C

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)**

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit		
Supply current Note 1	I _{DD1}	Operating mode	HS (high-speed main) mode Note 5	f _{HOCO} = 64 MHz, f _{IH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.6		mA	
					Basic operation	V _{DD} = 3.0 V		2.6			
				f _{HOCO} = 32 MHz, f _{IH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.3			
					Basic operation	V _{DD} = 3.0 V		2.3			
			HS (high-speed main) mode Note 5	f _{HOCO} = 64 MHz, f _{IH} = 32 MHz Note 3	Normal operation	V _{DD} = 5.0 V		5.4	10.9		mA
					Normal operation	V _{DD} = 3.0 V		5.4	10.9		
		f _{HOCO} = 32 MHz, f _{IH} = 32 MHz Note 3		Normal operation	V _{DD} = 5.0 V		5.0	10.3			
				Normal operation	V _{DD} = 3.0 V		5.0	10.3			
		f _{HOCO} = 48 MHz, f _{IH} = 24 MHz Note 3		Normal operation	V _{DD} = 5.0 V		4.2	8.2			
				Normal operation	V _{DD} = 3.0 V		4.2	8.2			
		HS (high-speed main) mode Note 5	f _{HOCO} = 24 MHz, f _{IH} = 24 MHz Note 3	Normal operation	V _{DD} = 5.0 V		4.0	7.8	mA		
				Normal operation	V _{DD} = 3.0 V		4.0	7.8			
			f _{HOCO} = 16 MHz, f _{IH} = 16 MHz Note 3	Normal operation	V _{DD} = 5.0 V		3.0	5.6			
				Normal operation	V _{DD} = 3.0 V		3.0	5.6			
			HS (high-speed main) mode Note 5	f _{MX} = 20 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		3.4		6.6	mA
					Normal operation	Resonator connection		3.6		6.7	
		f _{MX} = 20 MHz Note 2, V _{DD} = 3.0 V		Normal operation	Square wave input		3.4	6.6			
				Normal operation	Resonator connection		3.6	6.7			
		HS (high-speed main) mode Note 5	f _{MX} = 10 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		2.1	3.9	mA		
				Normal operation	Resonator connection		2.2	4.0			
			f _{MX} = 10 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		2.1	3.9			
				Normal operation	Resonator connection		2.2	4.0			
		Subsystem clock operation			f _{SUB} = 32.768 kHz Note 4 T _A = -40°C	Normal operation	Square wave input		4.9	7.1	μA
						Normal operation	Resonator connection		4.9	7.1	
f _{SUB} = 32.768 kHz Note 4 T _A = +25°C	Normal operation				Square wave input		4.9	7.1			
	Normal operation				Resonator connection		4.9	7.1			
f _{SUB} = 32.768 kHz Note 4 T _A = +50°C	Normal operation				Square wave input		5.1	8.8			
	Normal operation				Resonator connection		5.1	8.8			
f _{SUB} = 32.768 kHz Note 4 T _A = +70°C	Normal operation	Square wave input		5.5	10.5						
	Normal operation	Resonator connection		5.5	10.5						
f _{SUB} = 32.768 kHz Note 4 T _A = +85°C	Normal operation	Square wave input		6.5	14.5						
	Normal operation	Resonator connection		6.5	14.5						
f _{SUB} = 32.768 kHz Note 4 T _A = +105°C	Normal operation	Square wave input		13.0	58.0						
	Normal operation	Resonator connection		13.0	58.0						

(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into V_{DD} , EV_{DD0} , and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} , and EV_{DD1} , or V_{SS} , EV_{SS0} , and EV_{SS1} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 3.** When high-speed system clock and subsystem clock are stopped.
- Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

Remark 1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HOCO} : High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f_{IH} : High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

(2) Flash ROM: 96 to 256 KB of 30- to 100-pin products**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit		
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V	0.79	4.86	mA	
					VDD = 3.0 V	0.79	4.86		
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V	0.49	4.17		
					VDD = 3.0 V	0.49	4.17		
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V	0.62	3.82		
					VDD = 3.0 V	0.62	3.82		
			fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V	0.4	3.25			
				VDD = 3.0 V	0.4	3.25			
			fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V	0.38	2.28			
				VDD = 3.0 V	0.38	2.28			
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input	0.30	2.65		mA
					Resonator connection	0.40	2.77		
		fMX = 20 MHz Note 3, VDD = 3.0 V		Square wave input	0.30	2.65			
				Resonator connection	0.40	2.77			
		fMX = 10 MHz Note 3, VDD = 5.0 V		Square wave input	0.20	1.36			
				Resonator connection	0.25	1.46			
		fMX = 10 MHz Note 3, VDD = 3.0 V		Square wave input	0.20	1.36			
				Resonator connection	0.25	1.46			
		Subsystem clock operation		fSUB = 32.768 kHz Note 5, TA = -40°C	Square wave input	0.28	0.66	μA	
					Resonator connection	0.47	0.85		
				fSUB = 32.768 kHz Note 5, TA = +25°C	Square wave input	0.34	0.66		
					Resonator connection	0.53	0.85		
			fSUB = 32.768 kHz Note 5, TA = +50°C	Square wave input	0.37	2.35			
				Resonator connection	0.56	2.54			
fSUB = 32.768 kHz Note 5, TA = +70°C	Square wave input	0.61	4.08						
	Resonator connection	0.80	4.27						
fSUB = 32.768 kHz Note 5, TA = +85°C	Square wave input	1.55	8.09						
	Resonator connection	1.74	8.28						
fSUB = 32.768 kHz Note 5, TA = +105°C	Square wave input	6.00	51.00						
	Resonator connection	6.00	51.00						
IDD3 Note 6	STOP mode Note 8	TA = -40°C		0.19	0.57	μA			
		TA = +25°C		0.25	0.57				
		TA = +50°C		0.33	2.26				
		TA = +70°C		0.52	3.99				
		TA = +85°C		1.46	8.00				
		TA = +105°C		5.50	50.00				

(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** During HALT instruction execution by flash memory.
- Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 4.** When high-speed system clock and subsystem clock are stopped.
- Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
- Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is TA = 25°C

(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit		
Supply current Note 1	I _{DD1}	Operating mode	HS (high-speed main) mode Note 5	f _{HOCO} = 64 MHz, f _{IH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.9		mA	
						V _{DD} = 3.0 V		2.9			
					f _{HOCO} = 32 MHz, f _{IH} = 32 MHz Note 3	Basic operation	V _{DD} = 5.0 V		2.5		
							V _{DD} = 3.0 V		2.5		
			HS (high-speed main) mode Note 5	f _{HOCO} = 64 MHz, f _{IH} = 32 MHz Note 3	Normal operation	V _{DD} = 5.0 V		6.0	11.2	mA	
						V _{DD} = 3.0 V		6.0	11.2		
		f _{HOCO} = 32 MHz, f _{IH} = 32 MHz Note 3		Normal operation	V _{DD} = 5.0 V		5.5	10.6			
					V _{DD} = 3.0 V		5.5	10.6			
		f _{HOCO} = 48 MHz, f _{IH} = 24 MHz Note 3		Normal operation	V _{DD} = 5.0 V		4.7	8.6			
					V _{DD} = 3.0 V		4.7	8.6			
		f _{HOCO} = 24 MHz, f _{IH} = 24 MHz Note 3		Normal operation	V _{DD} = 5.0 V		4.4	8.2			
					V _{DD} = 3.0 V		4.4	8.2			
		f _{HOCO} = 16 MHz, f _{IH} = 16 MHz Note 3		Normal operation	V _{DD} = 5.0 V		3.3	5.9			
					V _{DD} = 3.0 V		3.3	5.9			
		HS (high-speed main) mode Note 5	f _{MX} = 20 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		3.7	6.8	mA		
					Resonator connection		3.9	7.0			
			f _{MX} = 20 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		3.7	6.8			
					Resonator connection		3.9	7.0			
			f _{MX} = 10 MHz Note 2, V _{DD} = 5.0 V	Normal operation	Square wave input		2.3	4.1			
					Resonator connection		2.3	4.2			
			f _{MX} = 10 MHz Note 2, V _{DD} = 3.0 V	Normal operation	Square wave input		2.3	4.1			
					Resonator connection		2.3	4.2			
		Subsystem clock operation	f _{SUB} = 32.768 kHz Note 4 TA = -40°C	Normal operation	Square wave input		5.2	7.7	μA		
					Resonator connection		5.2	7.7			
f _{SUB} = 32.768 kHz Note 4 TA = +25°C	Normal operation		Square wave input		5.3	7.7					
			Resonator connection		5.3	7.7					
f _{SUB} = 32.768 kHz Note 4 TA = +50°C	Normal operation		Square wave input		5.5	10.6					
			Resonator connection		5.5	10.6					
f _{SUB} = 32.768 kHz Note 4 TA = +70°C	Normal operation		Square wave input		5.9	13.2					
			Resonator connection		6.0	13.2					
f _{SUB} = 32.768 kHz Note 4 TA = +85°C	Normal operation		Square wave input		6.8	17.5					
			Resonator connection		6.9	17.5					
f _{SUB} = 32.768 kHz Note 4 TA = +105°C	Normal operation	Square wave input		15.5	77.8						
		Resonator connection		15.5	77.8						

(Notes and Remarks are listed on the next page.)

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- Note 1.** Total current flowing into V_{DD} , EV_{DD0} , and EV_{DD1} , including the input leakage current flowing when the level of the input pin is fixed to V_{DD} , EV_{DD0} , and EV_{DD1} , or V_{SS} , EV_{SS0} , and EV_{SS1} . The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 3.** When high-speed system clock and subsystem clock are stopped.
- Note 4.** When high-speed on-chip oscillator and high-speed system clock are stopped. When AMPHS1 = 1 (Ultra-low power consumption oscillation). However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 5.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$

Remark 1. f_{MX} : High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 2. f_{HOCO} : High-speed on-chip oscillator clock frequency (64 MHz max.)

Remark 3. f_{IH} : High-speed on-chip oscillator clock frequency (32 MHz max.)

Remark 4. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 5. Except subsystem clock operation, temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

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(3) Flash ROM: 384 to 512 KB of 48- to 100-pin products**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode Note 7	fHOCO = 64 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V	0.93	5.16	mA
					VDD = 3.0 V	0.93	5.16	
				fHOCO = 32 MHz, fIH = 32 MHz Note 4	VDD = 5.0 V	0.5	4.47	
					VDD = 3.0 V	0.5	4.47	
				fHOCO = 48 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V	0.72	4.08	
					VDD = 3.0 V	0.72	4.08	
			fHOCO = 24 MHz, fIH = 24 MHz Note 4	VDD = 5.0 V	0.42	3.51		
				VDD = 3.0 V	0.42	3.51		
			fHOCO = 16 MHz, fIH = 16 MHz Note 4	VDD = 5.0 V	0.39	2.38		
				VDD = 3.0 V	0.39	2.38		
			HS (high-speed main) mode Note 7	fMX = 20 MHz Note 3, VDD = 5.0 V	Square wave input	0.31	2.83	mA
					Resonator connection	0.41	2.92	
		fMX = 20 MHz Note 3, VDD = 3.0 V		Square wave input	0.31	2.83		
				Resonator connection	0.41	2.92		
		fMX = 10 MHz Note 3, VDD = 5.0 V		Square wave input	0.21	1.46		
				Resonator connection	0.26	1.57		
		fMX = 10 MHz Note 3, VDD = 3.0 V		Square wave input	0.21	1.46		
				Resonator connection	0.26	1.57		
		Subsystem clock oper- ation	fsUB = 32.768 kHz Note 5, TA = -40°C	Square wave input	0.31	0.76	μA	
				Resonator connection	0.50	0.95		
			fsUB = 32.768 kHz Note 5, TA = +25°C	Square wave input	0.38	0.76		
Resonator connection	0.57			0.95				
fsUB = 32.768 kHz Note 5, TA = +50°C	Square wave input		0.47	3.59				
	Resonator connection		0.70	3.78				
fsUB = 32.768 kHz Note 5, TA = +70°C	Square wave input		0.80	6.20				
	Resonator connection		1.00	6.39				
fsUB = 32.768 kHz Note 5, TA = +85°C	Square wave input		1.65	10.56				
	Resonator connection		1.84	10.75				
fsUB = 32.768 kHz Note 5, TA = +105°C	Square wave input		8.00	65.7				
	Resonator connection		8.00	65.7				
IDD3 Note 6	STOP mode Note 8	TA = -40°C		0.19	0.63	μA		
		TA = +25°C		0.30	0.63			
		TA = +50°C		0.41	3.47			
		TA = +70°C		0.80	6.08			
		TA = +85°C		1.53	10.44			
		TA = +105°C		6.50	67.14			

(Notes and Remarks are listed on the next page.)

- Note 1.** Total current flowing into V_{DD}, EV_{DD0}, and EV_{DD1}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0}, and EV_{DD1}, or V_{SS}, EV_{SS0}, and EV_{SS1}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the A/D converter, D/A converter, comparator, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors and the current flowing during data flash rewrite.
- Note 2.** During HALT instruction execution by flash memory.
- Note 3.** When high-speed on-chip oscillator and subsystem clock are stopped.
- Note 4.** When high-speed system clock and subsystem clock are stopped.
- Note 5.** When high-speed on-chip oscillator and high-speed system clock are stopped. When RTCLPC = 1 and setting ultra-low current consumption (AMPHS1 = 1). The current flowing into the RTC is included. However, not including the current flowing into the 12-bit interval timer and watchdog timer.
- Note 6.** Not including the current flowing into the RTC, 12-bit interval timer, and watchdog timer.
- Note 7.** Relationship between operation voltage width, operation frequency of CPU and operation mode is as below.
 HS (high-speed main) mode: $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }32\text{ MHz}$
 $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}@1\text{ MHz to }16\text{ MHz}$
- Note 8.** Regarding the value for current to operate the subsystem clock in STOP mode, refer to that in HALT mode.
- Remark 1.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 2.** f_{HOCO}: High-speed on-chip oscillator clock frequency (64 MHz max.)
- Remark 3.** f_{IH}: High-speed on-chip oscillator clock frequency (32 MHz max.)
- Remark 4.** f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)
- Remark 5.** Except subsystem clock operation and STOP mode, temperature condition of the TYP. value is TA = 25°C

(4) Peripheral Functions (Common to all products)**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Low-speed on-chip oscillator operating current	IFIL Note 1				0.20		μA
RTC operating current	IRTC Notes 1, 2, 3				0.02		μA
12-bit interval timer operating current	IIT Notes 1, 2, 4				0.02		μA
Watchdog timer operating current	IWDT Notes 1, 2, 5	fil = 15 kHz			0.22		μA
A/D converter operating current	IADC Notes 1, 6	When conversion at maximum speed	Normal mode, AVREFP = VDD = 5.0 V		1.3	1.7	mA
			Low voltage mode, AVREFP = VDD = 3.0 V		0.5	0.7	mA
A/D converter reference voltage current	IADREF Note 1				75.0		μA
Temperature sensor operating current	ITMPS Note 1				75.0		μA
D/A converter operating current	IDAC Notes 1, 11, 13	Per D/A converter channel				1.5	mA
Comparator operating current	ICMP Notes 1, 12, 13	VDD = 5.0 V, Regulator output voltage = 2.1 V	Window mode		12.5		μA
			Comparator high-speed mode		6.5		μA
			Comparator low-speed mode		1.7		μA
		VDD = 5.0 V, Regulator output voltage = 1.8 V	Window mode		8.0		μA
			Comparator high-speed mode		4.0		μA
			Comparator low-speed mode		1.3		μA
LVD operating current	ILVD Notes 1, 7				0.08		μA
Self-programming operating current	IFSP Notes 1, 9				2.50	12.20	mA
BGO operating current	IBGO Notes 1, 8				2.50	12.20	mA
SNOOZE operating current	ISNOZ Note 1	ADC operation	The mode is performed Note 10		0.50	1.10	mA
			The A/D conversion operations are performed, Low voltage mode, AVREFP = VDD = 3.0 V		1.20	2.04	
		CSI/JART operation		0.70	1.54		
		DTC operation		3.10			

Note 1. Current flowing to VDD.**Note 2.** When high speed on-chip oscillator and high-speed system clock are stopped.**Note 3.** Current flowing only to the real-time clock (RTC) (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IRTC, when the real-time clock operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added. IDD2 subsystem clock operation includes the operational current of the real-time clock.**Note 4.** Current flowing only to the 12-bit interval timer (excluding the operating current of the low-speed on-chip oscillator and the XT1 oscillator). The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IIT, when the 12-bit interval timer operates in operation mode or HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be added.

- Note 5.** Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The supply current of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer is in operation.
- Note 6.** Current flowing only to the A/D converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.
- Note 7.** Current flowing only to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} or I_{DD3} and I_{LVD} when the LVD circuit is in operation.
- Note 8.** Current flowing during programming of the data flash.
- Note 9.** Current flowing during self-programming.
- Note 10.** For shift time to the SNOOZE mode, see **23.3.3 SNOOZE mode** in the RL78/G14 User's Manual.
- Note 11.** Current flowing only to the D/A converter. The supply current of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{DAC} when the D/A converter operates in an operation mode or the HALT mode.
- Note 12.** Current flowing only to the comparator circuit. The supply current of the RL78 microcontrollers is the sum of I_{DD1} , I_{DD2} , or I_{DD3} and I_{CMP} when the comparator circuit is in operation.
- Note 13.** A comparator and D/A converter are provided in products with 96 KB or more code flash memory.

Remark 1. f_{IL} : Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB} : Subsystem clock frequency (XT1 clock oscillation frequency)

Remark 3. f_{CLK} : CPU/peripheral hardware clock frequency

Remark 4. Temperature condition of the TYP. value is $T_A = 25^\circ\text{C}$

3.4 AC Characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

Items	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T _{cy}	Main system clock (f _{MAIN}) operation	HS (high-speed main) mode	$2.7\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$	0.03125		1	μs
				$2.4\text{ V} \leq \text{VDD} < 2.7\text{ V}$	0.0625		1	μs
		Subsystem clock (f _{SUB}) operation		$2.4\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$	28.5	30.5	31.3	μs
		In the self-programming mode	HS (high-speed main) mode	$2.7\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$	0.03125		1	μs
$2.4\text{ V} \leq \text{VDD} < 2.7\text{ V}$	0.0625				1	μs		
External system clock frequency	f _{EX}	$2.7\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$		1.0		20.0	MHz	
		$2.4\text{ V} \leq \text{VDD} \leq 2.7\text{ V}$		1.0		16.0	MHz	
	f _{EXS}			32		35	kHz	
External system clock input high-level width, low-level width	t _{EXH} ,	$2.7\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$		24			ns	
	t _{EXL}	$2.4\text{ V} \leq \text{VDD} \leq 2.7\text{ V}$		30			ns	
	t _{EXHS} , t _{EXLS}			13.7			μs	
T100 to T103, T110 to T113 input high-level width, low-level width	t _{TIH} , t _{TIL}			$1/f_{\text{MCK}} + 10$ Note			ns	
Timer RJ input cycle	f _c	TRJIO		$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	100		ns	
				$2.4\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$	300		ns	
Timer RJ input high-level width, low-level width	t _{TJH} , t _{TJL}	TRJIO		$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	40		ns	
				$2.4\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$	120		ns	

Note The following conditions are required for low voltage interface when $\text{EVDD0} < \text{VDD}$
 $2.4\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$: MIN. 125 ns

Remark f_{MCK}: Timer array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of timer mode register mn (TMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3))

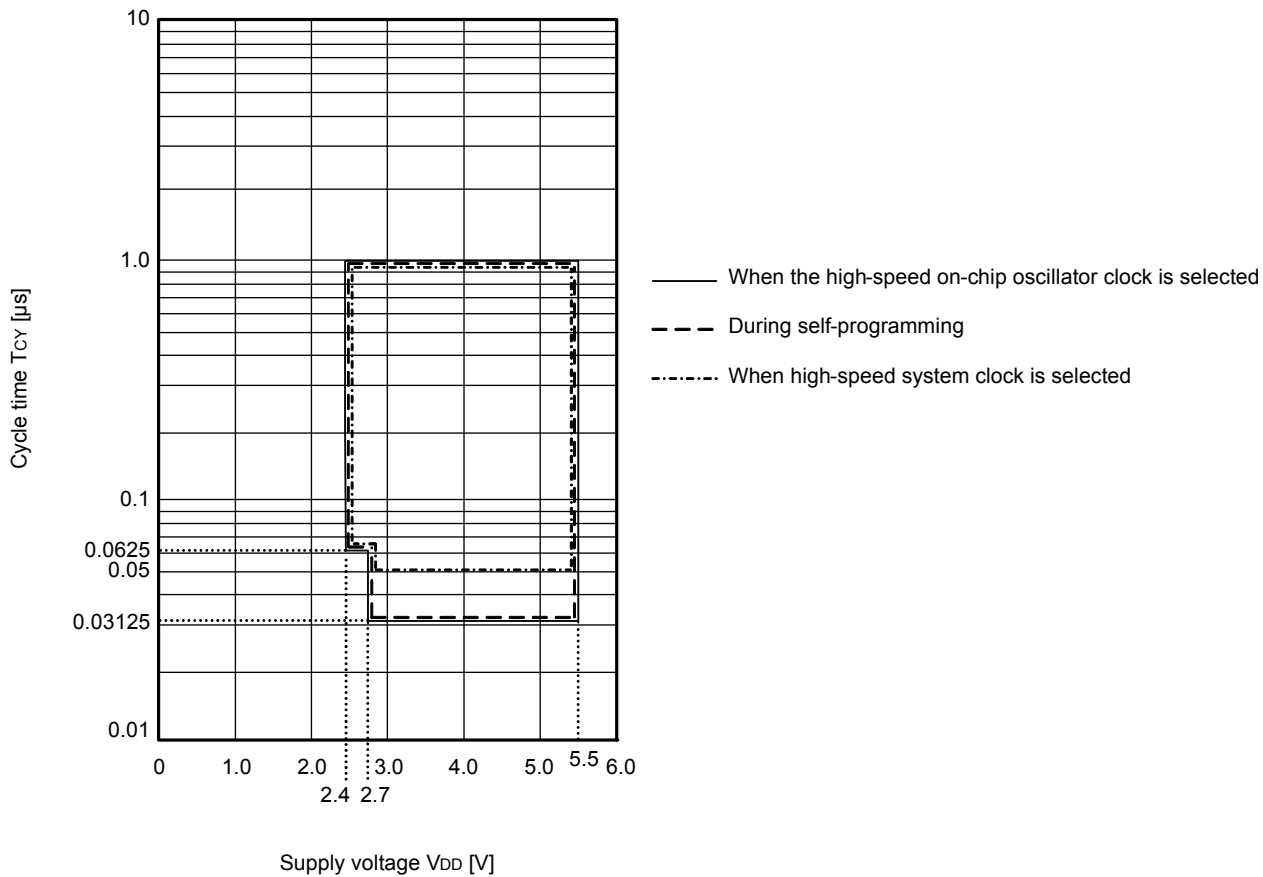
(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

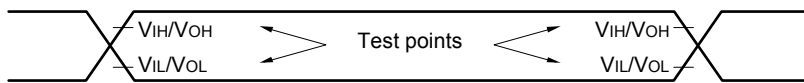
Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Timer RD input high-level width, low-level width	tTDIH, tTDIL	TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1		3/fCLK			ns
Timer RD forced cutoff signal input low-level width	tTDSIL	P130/INTP0	2MHz < fCLK ≤ 32 MHz	1			μs
			fCLK ≤ 2 MHz	1/fCLK + 1			
Timer RG input high-level width, low-level width	tTGIH, tTGIL	TRGIOA, TRGIOB		2.5/fCLK			ns
TO00 to TO03, TO10 to TO13, TRJIO0, TRJO0, TRDIOA0, TRDIOA1, TRDIOB0, TRDIOB1, TRDIOC0, TRDIOC1, TRDIOD0, TRDIOD1, TRGIOA, TRGIOB output frequency	fTO	HS (high-speed main) mode	4.0 V ≤ EVDD0 ≤ 5.5 V			16	MHz
			2.7 V ≤ EVDD0 < 4.0 V			8	MHz
			2.4 V ≤ EVDD0 < 2.7 V			4	MHz
PCLBUZ0, PCLBUZ1 output frequency	fPCL	HS (high-speed main) mode	4.0 V ≤ EVDD0 ≤ 5.5 V			16	MHz
			2.7 V ≤ EVDD0 < 4.0 V			8	MHz
			2.4 V ≤ EVDD0 < 2.7 V			4	MHz
Interrupt input high-level width, low-level width	tINTH, tINTL	INTP0	2.4 V ≤ VDD ≤ 5.5 V	1			μs
		INTP1 to INTP11	2.4 V ≤ EVDD0 ≤ 5.5 V	1			μs
Key interrupt input low-level width	tKR	KR0 to KR7	2.4 V ≤ EVDD0 ≤ 5.5 V	250			ns
RESET low-level width	tRSL			10			μs

Minimum Instruction Execution Time during Main System Clock Operation

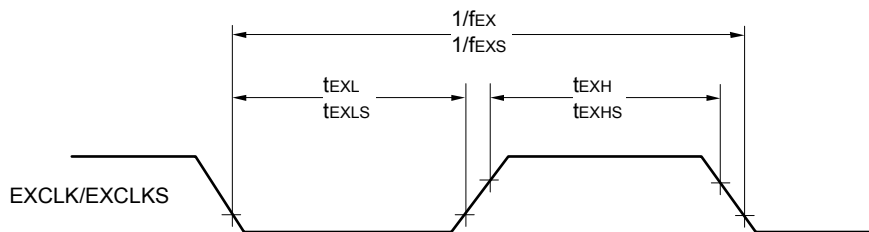
T_{CY} vs V_{DD} (HS (high-speed main) mode)



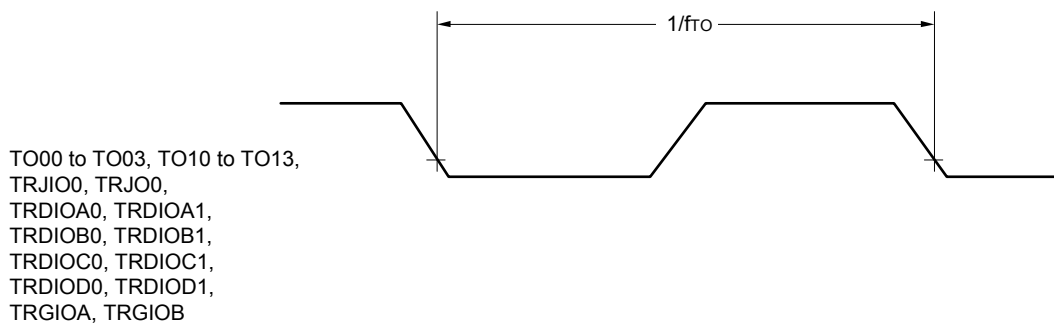
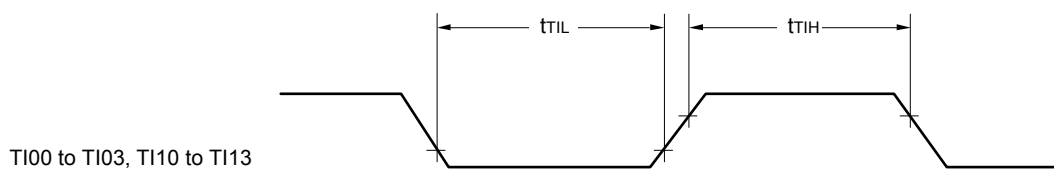
AC Timing Test Points

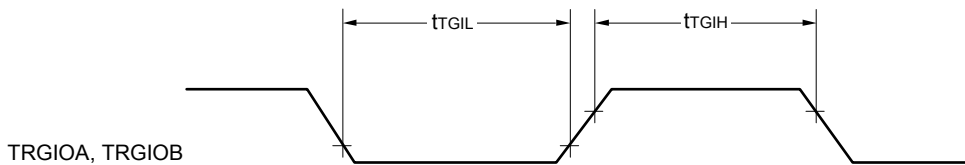
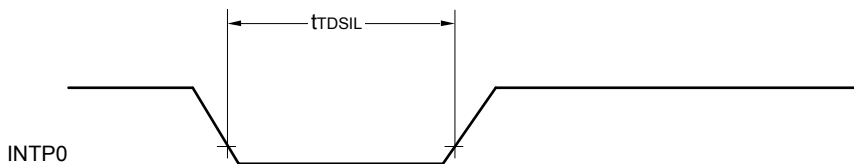
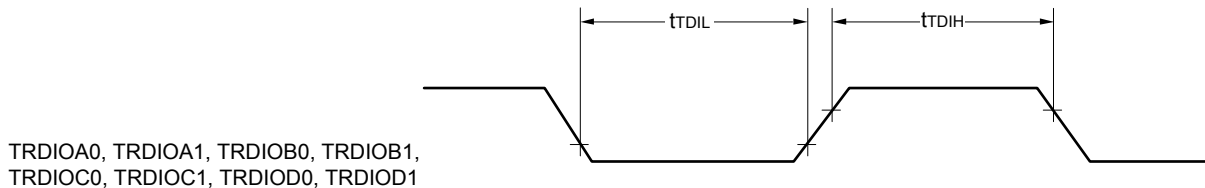
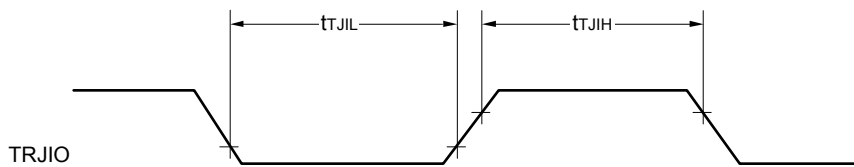


External System Clock Timing

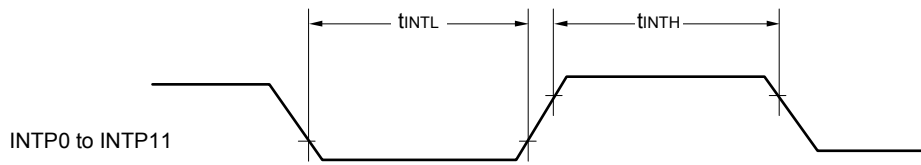


TI/TO Timing

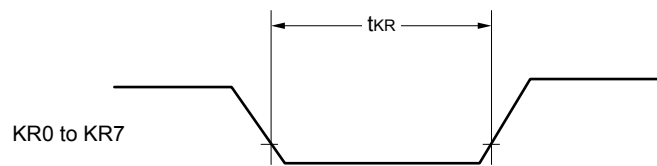




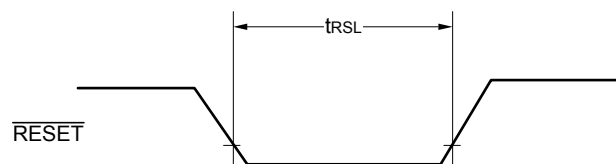
Interrupt Request Input Timing



Key Interrupt Input Timing

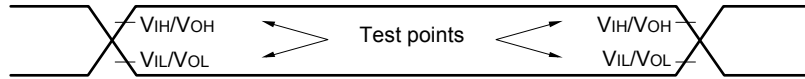


$\overline{\text{RESET}}$ Input Timing



3.5 Peripheral Functions Characteristics

AC Timing Test Points



3.5.1 Serial array unit

(1) During communication at same potential (UART mode)

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) Mode		Unit
			MIN.	MAX.	
Transfer rate Note 1		2.4 V ≤ EVDD0 ≤ 5.5 V		fMCK/12 Note 2	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note 3		2.6	Mbps

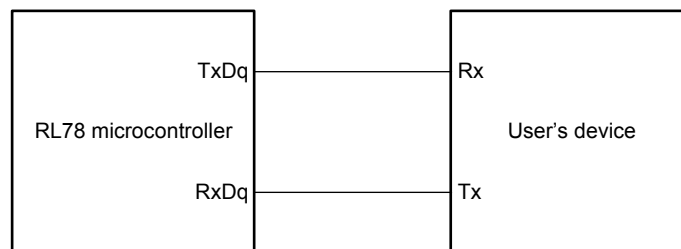
Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.
However, the SNOOZE mode cannot be used when FRQSEL4 = 1.

Note 2. The following conditions are required for low voltage interface when EVDD0 < VDD.
2.4 V ≤ EVDD0 < 2.7 V: MAX. 1.3 Mbps

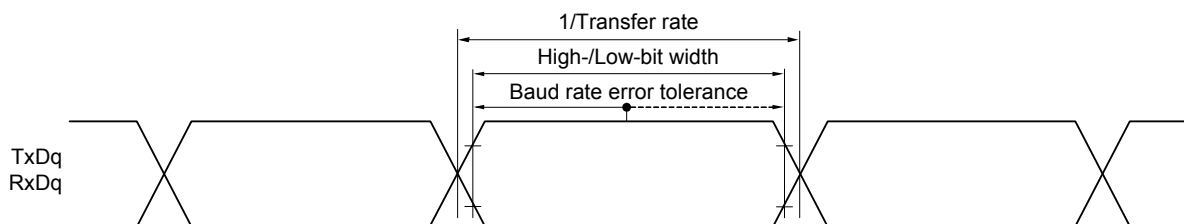
Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:
HS (high-speed main) mode: 32 MHz (2.7 V ≤ VDD ≤ 5.5 V)
16 MHz (2.4 V ≤ VDD ≤ 5.5 V)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remark 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit	
			MIN.	MAX.		
SCKp cycle time	t_{KCY1}	$t_{\text{KCY1}} \geq 4/f_{\text{CLK}}$	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	250		ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	500		ns
SCKp high-/low-level width	$t_{\text{KH1}}, t_{\text{KL1}}$	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$t_{\text{KCY1}}/2 - 24$		ns	
		$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$t_{\text{KCY1}}/2 - 36$		ns	
		$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$t_{\text{KCY1}}/2 - 76$		ns	
Slp setup time (to SCKp \uparrow) Note 1	t_{SIK1}	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	66		ns	
		$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	66		ns	
		$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	113		ns	
Slp hold time (from SCKp \uparrow) Note 2	t_{SH1}		38		ns	
Delay time from SCKp \downarrow to SOp output Note 3	t_{KS01}	$C = 30\text{ pF}$ Note 4		50	ns	

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp \uparrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKS $_{mn}$ bit of serial mode register mn (SMR $_{mn}$). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)
(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions		HS (high-speed main) mode		Unit
				MIN.	MAX.	
SCKp cycle time Note 5	tkCY2	4.0 V ≤ EVDD0 ≤ 5.5 V	20 MHz < fMCK	16/fMCK		ns
			fMCK ≤ 20 MHz	12/fMCK		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V	16 MHz < fMCK	16/fMCK		ns
			fMCK ≤ 16 MHz	12/fMCK		ns
		2.4 V ≤ EVDD0 ≤ 5.5 V		12/fMCK and 1000		ns
SCKp high-/low-level width	tkH2, tkL2	4.0 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 - 14		ns
		2.7 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 - 16		ns
		2.4 V ≤ EVDD0 ≤ 5.5 V		tkCY2/2 - 36		ns
Slp setup time (to SCKp↑) Note 1	tSIK2	2.7 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 40		ns
		2.4 V ≤ EVDD0 ≤ 5.5 V		1/fMCK + 60		ns
Slp hold time (from SCKp↑) Note 2	tKSI2			1/fMCK + 62		ns
Delay time from SCKp↓ to SOp output Note 3	tkSO2	C = 30 pF Note 4	2.7 V ≤ EVDD0 ≤ 5.5 V		2/fMCK + 66	ns
			2.4 V ≤ EVDD0 ≤ 5.5 V		2/fMCK + 113	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), g: PIM number (g = 0, 1, 3 to 5, 14)

Remark 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00 to 03, 10 to 13))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

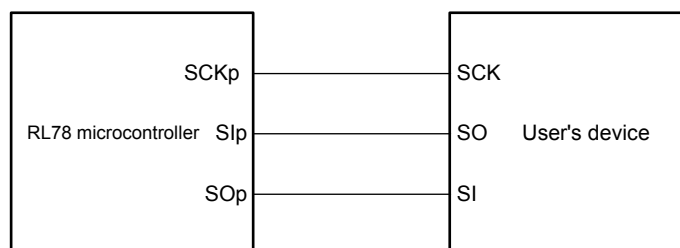
(2/2)

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit	
			MIN.	MAX.		
SSI00 setup time	tSSIK	DAPmn = 0	2.7 V ≤ EVDD0 ≤ 5.5 V	240		ns
			2.4 V ≤ EVDD0 ≤ 5.5 V	400		ns
		DAPmn = 1	2.7 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 240		ns
			2.4 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 400		ns
SSI00 hold time	tkSSI	DAPmn = 0	2.7 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 240		ns
			2.4 V ≤ EVDD0 ≤ 5.5 V	1/fMCK + 400		ns
		DAPmn = 1	2.7 V ≤ EVDD0 ≤ 5.5 V	240		ns
			2.4 V ≤ EVDD0 ≤ 5.5 V	400		ns

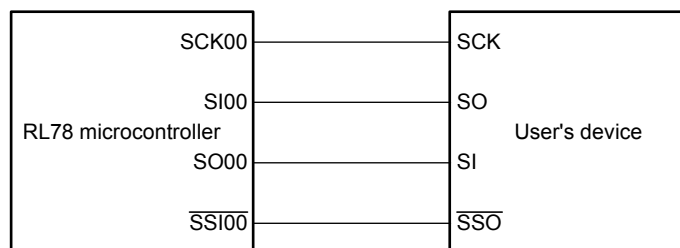
Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM number (g = 3, 5)

CSI mode connection diagram (during communication at same potential)



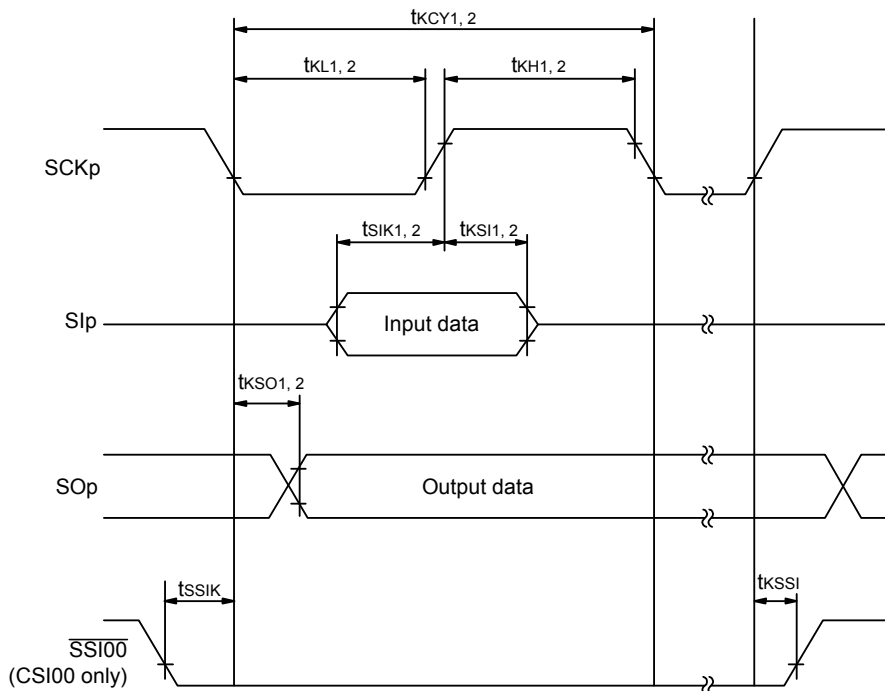
**CSI mode connection diagram (during communication at same potential)
(Slave Transmission of slave select input function (CSI00))**



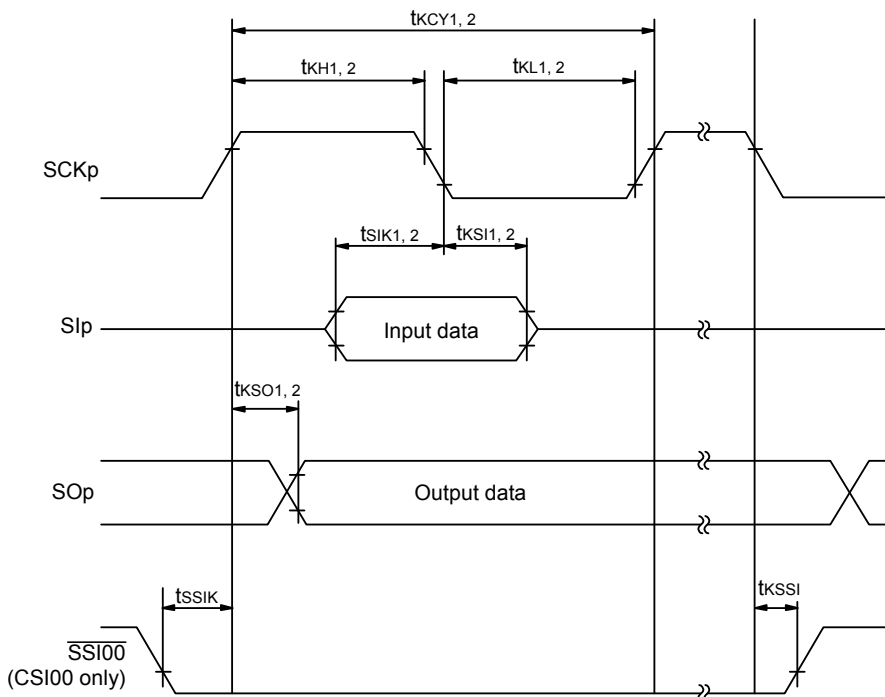
Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)

Remark 2. m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

(4) During communication at same potential (simplified I²C mode)**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

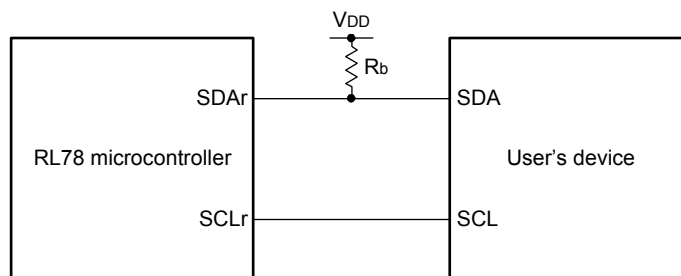
Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f _{SCL}	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ		400 Note 1	kHz
		2.4 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ		100 Note 1	kHz
Hold time when SCLr = "L"	t _{LOW}	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	1200		ns
		2.4 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	4600		ns
Hold time when SCLr = "H"	t _{HIGH}	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	1200		ns
		2.4 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	4600		ns
Data setup time (reception)	t _{SU: DAT}	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	1/f _{MCK} + 220 Note 2		ns
		2.4 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1/f _{MCK} + 580 Note 2		ns
Data hold time (transmission)	t _{HD: DAT}	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	0	770	ns
		2.4 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	0	1420	ns

Note 1. The value must also be equal to or less than f_{MCK}/4.**Note 2.** Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

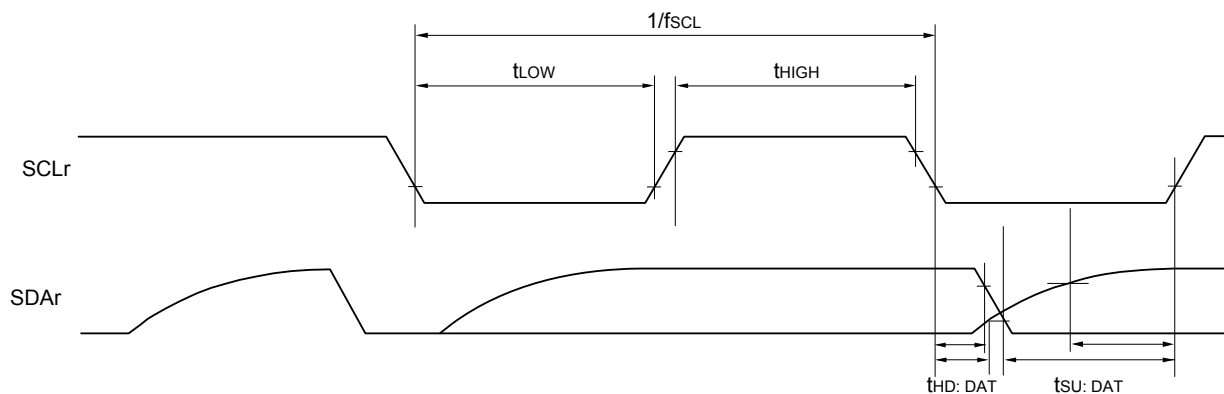
Caution Select the normal input buffer and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remark 1. $R_b[\Omega]$: Communication line (SDAr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 3 to 5, 14),
h: POM number (h = 0, 1, 3 to 5, 7, 14)

Remark 3. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1),
n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)**($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)****(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit	
			MIN.	MAX.		
Transfer rate		reception	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$		$f_{\text{MCK}}/12$ Note 1	bps
			Theoretical value of the maximum transfer rate $f_{\text{MCK}} = f_{\text{CLK}}$ Note 3		2.6	Mbps
			$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$		$f_{\text{MCK}}/12$ Note 1	bps
			Theoretical value of the maximum transfer rate $f_{\text{MCK}} = f_{\text{CLK}}$ Note 3		2.6	Mbps
			$2.4\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$		$f_{\text{MCK}}/12$ Notes 1, 2	bps
			Theoretical value of the maximum transfer rate $f_{\text{MCK}} = f_{\text{CLK}}$ Note 3		2.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

However, the SNOOZE mode cannot be used when $\text{FRQSEL4} = 1$.

Note 2. The following conditions are required for low voltage interface when $\text{EVDD0} < \text{VDD}$.

$2.4\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$: MAX. 1.3 Mbps

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (f_{CLK}) are:

HS (high-speed main) mode: 32 MHz ($2.7\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$)

16 MHz ($2.4\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/ EVDD tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

Remark 1. V_b [V]: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

Remark 3. f_{MCK} : Serial array unit operation clock frequency

(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,

n: Channel number (mn = 00 to 03, 10 to 13)

Remark 4. UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

(5) Communication at different potential (1.8 V, 2.5 V, 3 V) (UART mode)**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit	
			MIN.	MAX.		
Transfer rate		transmission	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V		Note 1	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 1.4 kΩ, Vb = 2.7 V		2.6 Note 2	Mbps
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V		Note 3	bps	
		Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 2.7 kΩ, Vb = 2.3 V		1.2 Note 4	Mbps	
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V		Note 5	bps	
		Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 5.5 kΩ, Vb = 1.6 V		0.43 Note 6	Mbps	

Note 1. The smaller maximum transfer rate derived by using $f_{MCK}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 4.0 V ≤ EVDD0 ≤ 5.5 V and 2.7 V ≤ Vb ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 2. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

Note 3. The smaller maximum transfer rate derived by using $f_{MCK}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when 2.7 V ≤ EVDD0 < 4.0 V and 2.3 V ≤ Vb ≤ 2.7 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 4. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Note 5. The smaller maximum transfer rate derived by using $f_{MCK}/12$ or the following expression is the valid maximum transfer rate.

Expression for calculating the transfer rate when $2.4\text{ V} \leq EV_{DD} < 3.3\text{ V}$ and $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

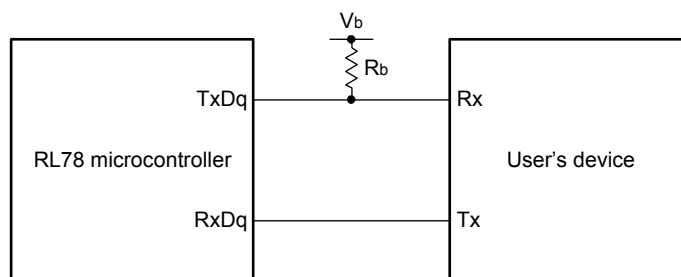
* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 6. This value as an example is calculated when the conditions described in the "Conditions" column are met. Refer to **Note 5** above to calculate the maximum transfer rate under conditions of the customer.

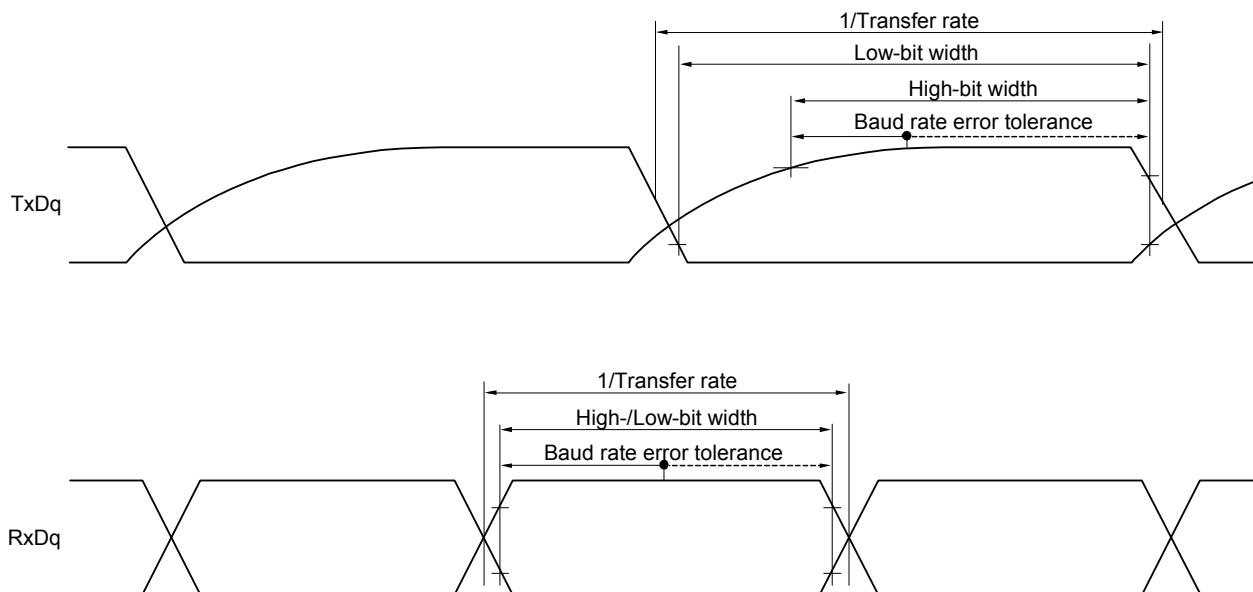
Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

UART mode connection diagram (during communication at different potential)



UART mode bit width (during communication at different potential) (reference)



Remark 1. $R_b[\Omega]$: Communication line (TxDq) pull-up resistance,
 $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

Remark 3. f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
 m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

Remark 4. UART2 cannot communicate at different potential when bit 1 (PIOR01) of peripheral I/O redirection register 0 (PIOR0) is 1.

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCKp cycle time	tkCY1	tkCY1 ≥ 4/fCLK 4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	600		ns
			1000		ns
			2300		ns
SCKp high-level width	tkH1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	tkCY1/2 - 150		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	tkCY1/2 - 340		ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ	tkCY1/2 - 916		ns
SCKp low-level width	tkL1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	tkCY1/2 - 24		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	tkCY1/2 - 36		ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ	tkCY1/2 - 100		ns

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/3)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp↑) ^{Note}	tsIK1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	162		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	354		ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ	958		ns
Slp hold time (from SCKp↑) ^{Note}	tkS11	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	38		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	38		ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ	38		ns
Delay time from SCKp↓ to SOp output ^{Note}	tkSO1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		200	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		390	ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ		966	ns

Note When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

(6) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (master mode, SCKp... internal clock output)**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(3/3)**

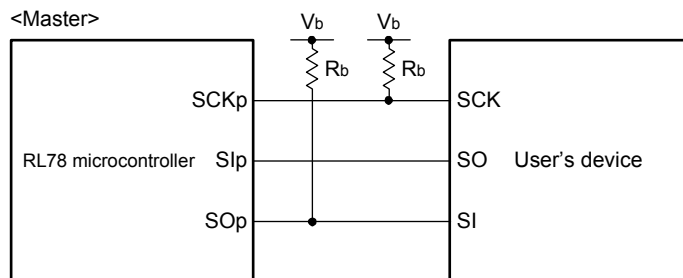
Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Slp setup time (to SCKp↓) ^{Note}	tsIK1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	88		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	88		ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ	220		ns
Slp hold time (from SCKp↓) ^{Note}	tkS11	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	38		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	38		ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ	38		ns
Delay time from SCKp↑ to SOp output ^{Note}	tkSO1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		50	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		50	ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rb = 5.5 kΩ		50	ns

Note When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (VDD tolerance (for the 30- to 52-pin products)/EVDD tolerance (for the 64- to 100-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

CSI mode connection diagram (during communication at different potential)



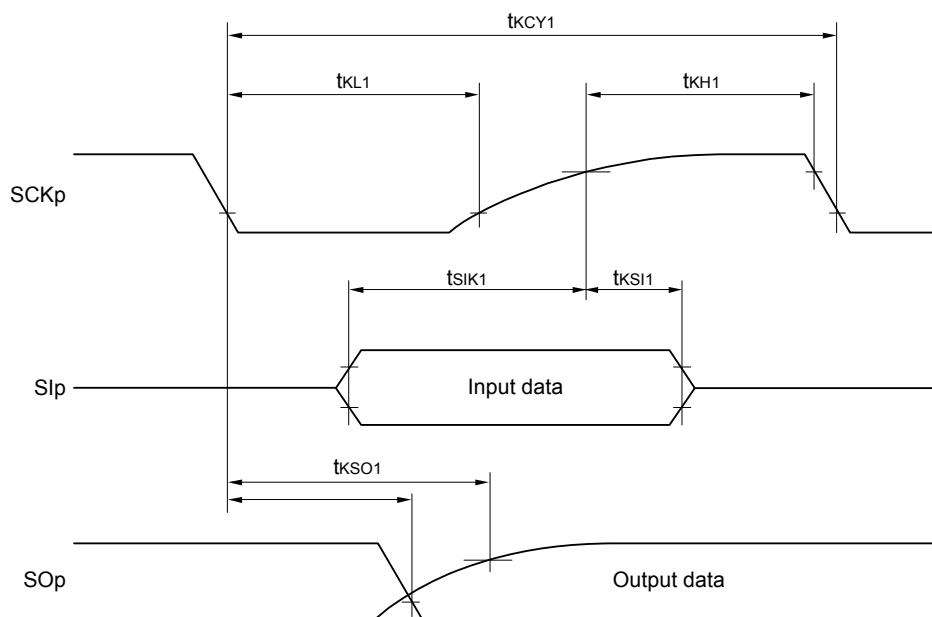
Remark 5. $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage

Remark 6. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)

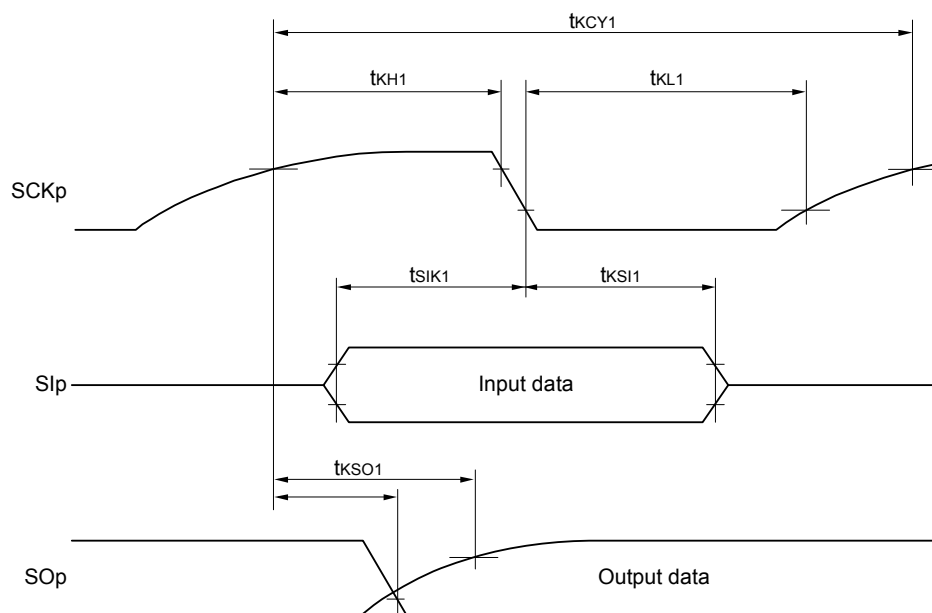
Remark 7. f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

Remark 8. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (master mode) (during communication at different potential)
(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
 g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

(7) Communication at different potential (1.8 V, 2.5 V, 3 V) (CSI mode) (slave mode, SCKp... external clock input)**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)**

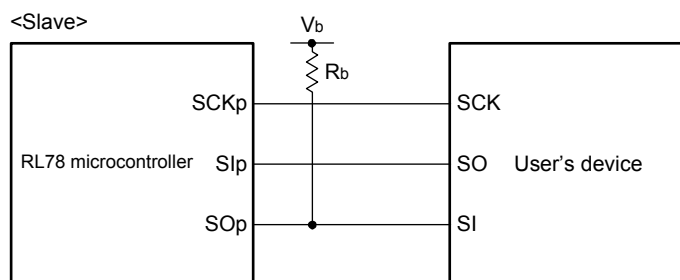
Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit	
			MIN.	MAX.		
SCKp cycle time ^{Note 1}	tkcy2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	24 MHz < fmck	28/fmck		ns
			20 MHz < fmck ≤ 24 MHz	24/fmck		ns
			8 MHz < fmck ≤ 20 MHz	20/fmck		ns
			4 MHz < fmck ≤ 8 MHz	16/fmck		ns
			fmck ≤ 4 MHz	12/fmck		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	24 MHz < fmck	40/fmck		ns
			20 MHz < fmck ≤ 24 MHz	32/fmck		ns
			16 MHz < fmck ≤ 20 MHz	28/fmck		ns
			8 MHz < fmck ≤ 16 MHz	24/fmck		ns
			4 MHz < fmck ≤ 8 MHz	16/fmck		ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V	24 MHz < fmck	96/fmck		ns
			20 MHz < fmck ≤ 24 MHz	72/fmck		ns
			16 MHz < fmck ≤ 20 MHz	64/fmck		ns
			8 MHz < fmck ≤ 16 MHz	52/fmck		ns
			4 MHz < fmck ≤ 8 MHz	32/fmck		ns
		fmck ≤ 4 MHz	20/fmck		ns	
		SCKp high-/low-level width		tkcy2/2 - 24		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V				
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V				
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V		tkcy2/2 - 100		ns
Slp setup time (to SCKp↑) ^{Note 2}	tsik2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V	1/fmck + 40		ns	
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V	1/fmck + 40		ns	
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V	1/fmck + 60		ns	
Slp hold time (from SCKp↑) ^{Note 3}	tksl2		1/fmck + 62		ns	
Delay time from SCKp↓ to SOp output ^{Note 4}	tkso2	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ		2/fmck + 240	ns	
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ		2/fmck + 428	ns	
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 30 pF, Rv = 5.5 kΩ		2/fmck + 1146	ns	

(Notes, Caution, and Remarks are listed on the next page.)

- Note 1.** Transfer rate in the SNOOZE mode: MAX. 1 Mbps
- Note 2.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 3.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.
- Note 4.** When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

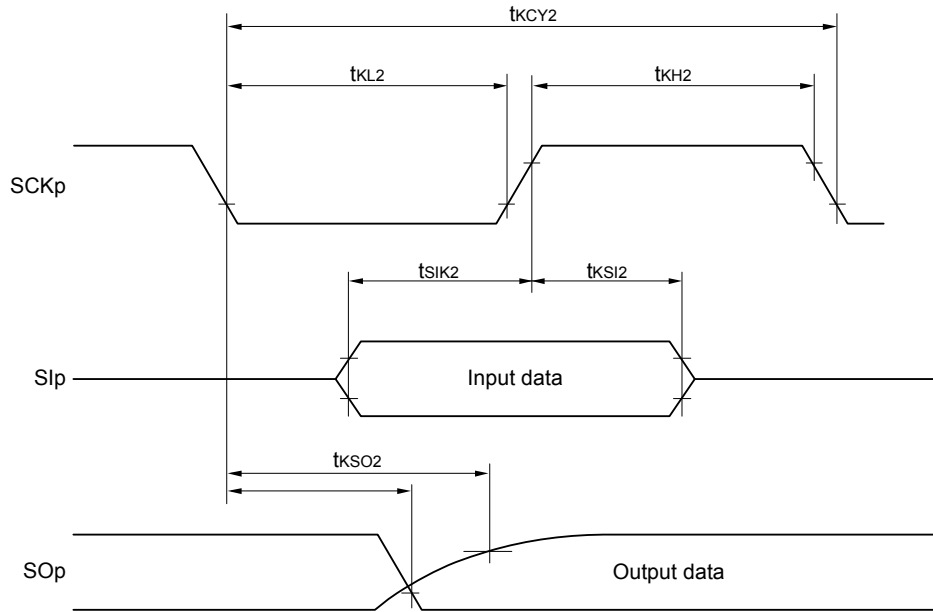
Caution Select the TTL input buffer for the SIp pin and SCKp pin, and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/ EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SOp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

CSI mode connection diagram (during communication at different potential)

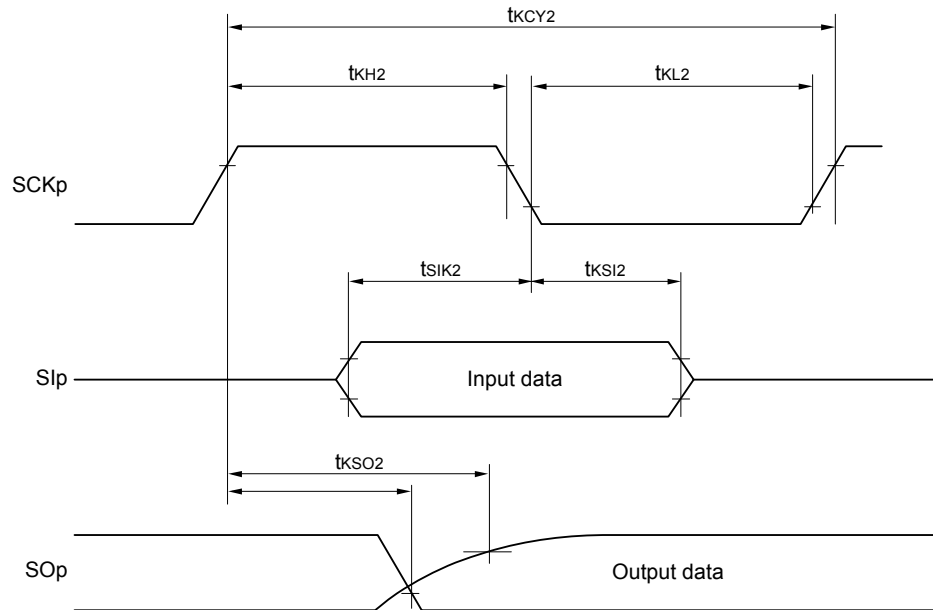


- Remark 1.** $R_b[\Omega]$: Communication line (SOp) pull-up resistance, $C_b[F]$: Communication line (SOp) load capacitance, $V_b[V]$: Communication line voltage
- Remark 2.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM number (g = 0, 1, 3 to 5, 14)
- Remark 3.** f_{MCK} : Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13))
- Remark 4.** CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.
Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

**CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$.)**



**CSI mode serial transfer timing (slave mode) (during communication at different potential)
(When $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.)**



Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3),
g: PIM and POM number (g = 0, 1, 3 to 5, 14)

Remark 2. CSI01 of 48-, 52-, 64-pin products, and CSI11 and CSI21 cannot communicate at different potential. Use other CSI for communication at different potential.

Also, communication at different potential cannot be performed during clock synchronous serial communication with the slave select function.

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(1/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f _{SCL}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ		400 Note 1	kHz
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ		400 Note 1	kHz
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ		100 Note 1	kHz
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ		100 Note 1	kHz
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 100 pF, Rb = 5.5 kΩ		100 Note 1	kHz
Hold time when SCLr = "L"	t _{LOW}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	1200		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	1200		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	4600		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	4600		ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 100 pF, Rb = 5.5 kΩ	4650		ns
Hold time when SCLr = "H"	t _{HIGH}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 50 pF, Rb = 2.7 kΩ	620		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 50 pF, Rb = 2.7 kΩ	500		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 100 pF, Rb = 2.8 kΩ	2700		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 100 pF, Rb = 2.7 kΩ	2400		ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V, Cb = 100 pF, Rb = 5.5 kΩ	1830		ns

(8) Communication at different potential (1.8 V, 2.5 V, 3 V) (simplified I²C mode)**(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)****(2/2)**

Parameter	Symbol	Conditions	HS (high-speed main) mode		Unit
			MIN.	MAX.	
Data setup time (reception)	t _{SU:DAT}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 340 Note 2		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 340 Note 2		ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1/f _{MCK} + 760 Note 2		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1/f _{MCK} + 760 Note 2		ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 100 pF, R _b = 5.5 kΩ	1/f _{MCK} + 570 Note 2		ns
Data hold time (transmission)	t _{HD:DAT}	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	0	770	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	0	770	ns
		4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	0	1420	ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	0	1420	ns
		2.4 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V, C _b = 100 pF, R _b = 5.5 kΩ	0	1215	ns

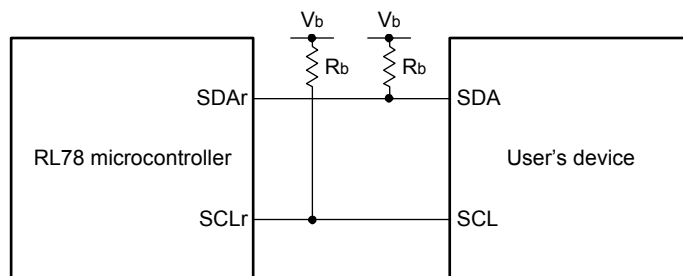
Note 1. The value must also be equal to or less than f_{MCK}/4.

Note 2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

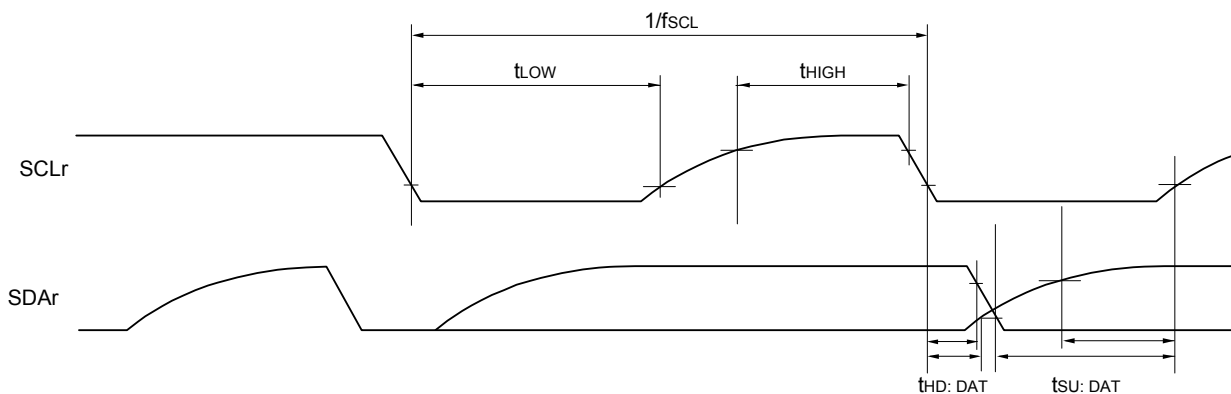
Caution Select the TTL input buffer and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SDAr pin and the N-ch open drain output (V_{DD} tolerance (for the 30- to 52-pin products)/EV_{DD} tolerance (for the 64- to 100-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Simplified I²C mode connection diagram (during communication at different potential)



Simplified I²C mode serial transfer timing (during communication at different potential)



- Remark 1.** $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
- Remark 2.** r: IIC number (r = 00, 01, 10, 11, 20, 30, 31), g: PIM, POM number (g = 0, 1, 3 to 5, 14)
- Remark 3.** f_{MCK} : Serial array unit operation clock frequency
 (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0, 2), mn = 00, 01, 02, 10, 12, 13)

3.5.2 Serial interface IICA

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	HS (high-speed main) mode				Unit
			Standard mode		Fast mode		
			MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	fSCL	Fast mode: fCLK ≥ 3.5 MHz	—	—	0	400	kHz
		Standard mode: fCLK ≥ 1 MHz	0	100	—	—	kHz
Setup time of restart condition	tSU: STA		4.7		0.6		μs
Hold time ^{Note 1}	tHD: STA		4.0		0.6		μs
Hold time when SCLA0 = "L"	tLOW		4.7		1.3		μs
Hold time when SCLA0 = "H"	tHIGH		4.0		0.6		μs
Data setup time (reception)	tSU: DAT		250		100		ns
Data hold time (transmission) ^{Note 2}	tHD: DAT		0	3.45	0	0.9	μs
Setup time of stop condition	tSU: STO		4.0		0.6		μs
Bus-free time	tBUF		4.7		1.3		μs

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

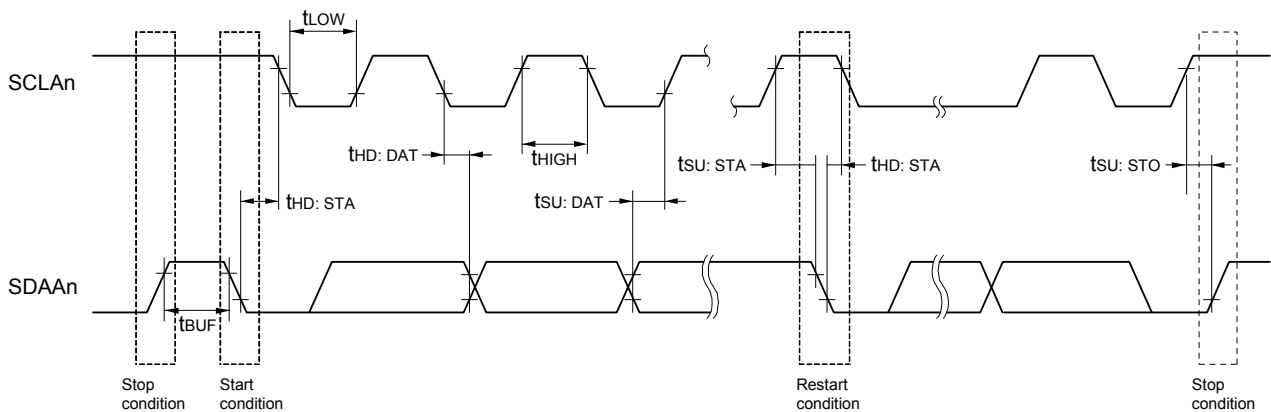
Caution The values in the above table are applied even when bit 2 (PIOR02) in the peripheral I/O redirection register 0 (PIOR0) is 1. At this time, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

Remark The maximum value of C_b (communication line capacitance) and the value of R_b (communication line pull-up resistor) at that time in each mode are as follows.

Standard mode: C_b = 400 pF, R_b = 2.7 kΩ

Fast mode: C_b = 320 pF, R_b = 1.1 kΩ

IICA serial transfer timing



Remark n = 0, 1

3.6 Analog Characteristics

3.6.1 A/D converter characteristics

Classification of A/D converter characteristics

Input channel	Reference Voltage	Reference voltage (+) = AVREFP Reference voltage (-) = AVREFM	Reference voltage (+) = VDD Reference voltage (-) = VSS	Reference voltage (+) = VBGR Reference voltage (-) = AVREFM
ANI0 to ANI14		Refer to 3.6.1 (1).	Refer to 3.6.1 (3).	Refer to 3.6.1 (4).
ANI16 to ANI20		Refer to 3.6.1 (2).		
Internal reference voltage Temperature sensor output voltage		Refer to 3.6.1 (1).		

(1) When reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage

(TA = -40 to +105°C, 2.4 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V, Reference voltage (+) = AVREFP,
Reference voltage (-) = AVREFM = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RES		8		10	bit
Overall error Note 1	AINL	10-bit resolution AVREFP = VDD Note 3	2.4 V ≤ AVREFP ≤ 5.5 V	1.2	±3.5	LSB
Conversion time	tCONV	10-bit resolution Target pin: ANI2 to ANI14	3.6 V ≤ VDD ≤ 5.5 V	2.125	39	μs
			2.7 V ≤ VDD ≤ 5.5 V	3.1875	39	μs
			2.4 V ≤ VDD ≤ 5.5 V	17	39	μs
		10-bit resolution Target pin: Internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ VDD ≤ 5.5 V	2.375	39	μs
			2.7 V ≤ VDD ≤ 5.5 V	3.5625	39	μs
			2.4 V ≤ VDD ≤ 5.5 V	17	39	μs
Zero-scale error Notes 1, 2	EZS	10-bit resolution AVREFP = VDD Note 3	2.4 V ≤ AVREFP ≤ 5.5 V		±0.25	%FSR
Full-scale error Notes 1, 2	EFS	10-bit resolution AVREFP = VDD Note 3	2.4 V ≤ AVREFP ≤ 5.5 V		±0.25	%FSR
Integral linearity error Note 1	ILE	10-bit resolution AVREFP = VDD Note 3	2.4 V ≤ AVREFP ≤ 5.5 V		±2.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution AVREFP = VDD Note 3	2.4 V ≤ AVREFP ≤ 5.5 V		±1.5	LSB
Analog input voltage	VAIN	ANI2 to ANI14		0	AVREFP	V
		Internal reference voltage output (2.4 V ≤ VDD ≤ 5.5 V, HS (high-speed main) mode)			VBGR Note 4	V
		Temperature sensor output voltage (2.4 V ≤ VDD ≤ 5.5 V, HS (high-speed main) mode)			VTMPS25 Note 4	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When AVREFP < VDD, the MAX. values are as follows.

Overall error: Add ±1.0 LSB to the MAX. value when AVREFP = VDD.

Zero-scale error/Full-scale error: Add ±0.05%FSR to the MAX. value when AVREFP = VDD.

Integral linearity error/ Differential linearity error: Add ±0.5 LSB to the MAX. value when AVREFP = VDD.

Note 4. Refer to 3.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

(2) When reference voltage (+) = $AV_{REFP}/ANI0$ ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = $AV_{REFM}/ANI1$ ($ADREFM = 1$), target pin: ANI16 to ANI20

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{DD0} = EV_{DD1} \leq V_{DD} \leq 5.5\text{ V}$, $2.4\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$,

$V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, Reference voltage (+) = AV_{REFP} , Reference voltage (-) = $AV_{REFM} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8		10	bit
Overall error Note 1	AINL	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$		1.2	± 5.0	LSB
Conversion time	t_{CONV}	10-bit resolution Target ANI pin: ANI16 to ANI20	$3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	2.125		39	μs
			$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	3.1875		39	μs
			$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	17		39	μs
Zero-scale error Notes 1, 2	E_{ZS}	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 0.35	%FSR
Full-scale error Notes 1, 2	E_{FS}	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 0.35	%FSR
Integral linearity error Note 1	ILE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 3.5	LSB
Differential linearity error Note 1	DLE	10-bit resolution $EV_{DD0} \leq AV_{REFP} = V_{DD}$ Notes 3, 4	$2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$			± 2.0	LSB
Analog input voltage	V_{AIN}	ANI16 to ANI20		0		AV_{REFP} and EV_{DD0}	V

Note 1. Excludes quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When $EV_{DD0} \leq AV_{REFP} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 1.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
 Zero-scale error/Full-scale error: Add $\pm 0.05\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
 Integral linearity error/ Differential linearity error: Add ± 0.5 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

Note 4. When $AV_{REFP} < EV_{DD0} \leq V_{DD}$, the MAX. values are as follows.

Overall error: Add ± 4.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.
 Zero-scale error/Full-scale error: Add $\pm 0.20\%$ FSR to the MAX. value when $AV_{REFP} = V_{DD}$.
 Integral linearity error/ Differential linearity error: Add ± 2.0 LSB to the MAX. value when $AV_{REFP} = V_{DD}$.

- (3) When reference voltage (+) = V_{DD} (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) = V_{SS} (ADREFM = 0), target pin: ANI0 to ANI14, ANI16 to ANI20, internal reference voltage, and temperature sensor output voltage

(TA = -40 to +105°C, 2.4 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V, Reference voltage (+) = V_{DD}, Reference voltage (-) = V_{SS})

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit	
Resolution	RES			8		10	bit	
Overall error Note 1	AINL	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V		1.2	±7.0	LSB	
Conversion time	t _{CONV}	10-bit resolution Target pin: ANI0 to ANI14, ANI16 to ANI20	3.6 V ≤ V _{DD} ≤ 5.5 V	2.125		39	μs	
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.1875		39	μs	
			2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs	
		10-bit resolution Target pin: internal reference voltage, and temperature sensor output voltage (HS (high-speed main) mode)	3.6 V ≤ V _{DD} ≤ 5.5 V	2.375		39	μs	
			2.7 V ≤ V _{DD} ≤ 5.5 V	3.5625		39	μs	
			2.4 V ≤ V _{DD} ≤ 5.5 V	17		39	μs	
Zero-scale error Notes 1, 2	E _{ZS}	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR	
Full-scale error Notes 1, 2	E _{FS}	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±0.60	%FSR	
Integral linearity error Note 1	ILE	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±4.0	LSB	
Differential linearity error Note 1	DLE	10-bit resolution	2.4 V ≤ V _{DD} ≤ 5.5 V			±2.0	LSB	
Analog input voltage	V _{AIN}	ANI0 to ANI14		0		V _{DD}	V	
		ANI16 to ANI20		0		EV _{DD0}	V	
		Internal reference voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)		V _{BGR} Note 3				V
		Temperature sensor output voltage (2.4 V ≤ V _{DD} ≤ 5.5 V, HS (high-speed main) mode)		V _{TMPS25} Note 3				V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to 3.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

(4) When reference voltage (+) = Internal reference voltage (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), target pin: ANI0, ANI2 to ANI14, ANI16 to ANI20

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, 1.6 V ≤ EVDD = EVDD1 ≤ VDD, VSS = EVSS0 = EVSS1 = 0 V,

Reference voltage (+) = VBGR ^{Note 3}, Reference voltage (-) = AVREFM = 0 V ^{Note 4}, HS (high-speed main) mode)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES			8			bit
Conversion time	tCONV	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V	17		39	μs
Zero-scale error ^{Notes 1, 2}	Ezs	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±0.60	% FSR
Integral linearity error ^{Note 1}	ILE	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±2.0	LSB
Differential linearity error ^{Note 1}	DLE	8-bit resolution	2.4 V ≤ VDD ≤ 5.5 V			±1.0	LSB
Analog input voltage	VAIN			0		VBGR ^{Note 3}	V

Note 1. Excludes quantization error (±1/2 LSB).

Note 2. This value is indicated as a ratio (% FSR) to the full-scale value.

Note 3. Refer to 3.6.2 Temperature sensor characteristics/internal reference voltage characteristic.

Note 4. When reference voltage (-) = VSS, the MAX. values are as follows.

Zero-scale error: Add ±0.35%FSR to the MAX. value when reference voltage (-) = AVREFM.

Integral linearity error: Add ±0.5 LSB to the MAX. value when reference voltage (-) = AVREFM.

Differential linearity error: Add ±0.2 LSB to the MAX. value when reference voltage (-) = AVREFM.

3.6.2 Temperature sensor characteristics/internal reference voltage characteristic

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$, HS (high-speed main) mode)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature sensor output voltage	VTMPS25	Setting ADS register = 80H, $T_A = +25^\circ\text{C}$		1.05		V
Internal reference voltage	VBGR	Setting ADS register = 81H	1.38	1.45	1.5	V
Temperature coefficient	FVTMPS	Temperature sensor that depends on the temperature		-3.6		mV/ $^\circ\text{C}$
Operation stabilization wait time	tAMP		5			μs

3.6.3 D/A converter characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq EV_{SS0} = EV_{SS1} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = EV_{SS0} = EV_{SS1} = 0\text{ V}$)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	RES					8	bit
Overall error	AINL	Rload = 4 M Ω	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.5	LSB
		Rload = 8 M Ω	$2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.5	LSB
Settling time	tSET	Cload = 20 pF	$2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			3	μs
			$2.4\text{ V} \leq V_{DD} < 2.7\text{ V}$			6	μs

3.6.4 Comparator

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage range	Ivref		0		EVDD0 - 1.4	V
	Ivcmp		-0.3		EVDD0 + 0.3	V
Output delay	td	VDD = 3.0 V Input slew rate > 50 mV/μs	Comparator high-speed mode, standard mode		1.2	μs
			Comparator high-speed mode, window mode		2.0	μs
			Comparator low-speed mode, standard mode	3.0	5.0	μs
High-electric-potential reference voltage	VTW+	Comparator high-speed mode, window mode		0.76 VDD		V
Low-electric-potential reference voltage	VTW-	Comparator high-speed mode, window mode		0.24 VDD		V
Operation stabilization wait time	tcMP		100			μs
Internal reference voltage Note	VBGR	2.4 V ≤ VDD ≤ 5.5 V, HS (high-speed main) mode	1.38	1.45	1.50	V

Note Not usable in sub-clock operation or STOP mode.

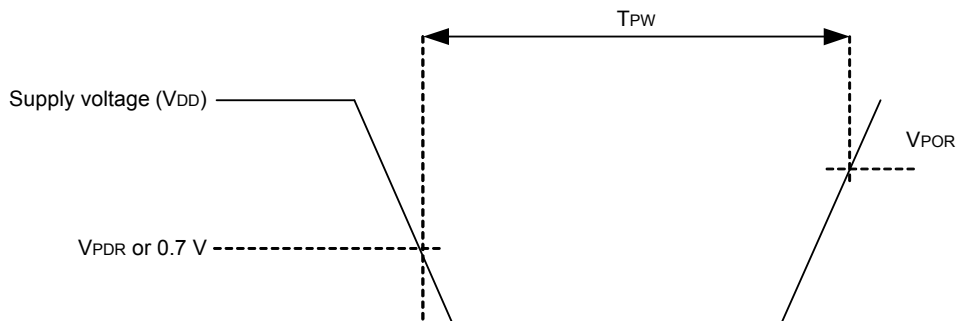
3.6.5 POR circuit characteristics

(TA = -40 to +105°C, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power on/down reset threshold	VPOR	Voltage threshold on VDD rising	1.45	1.51	1.57	V
	VPDR	Voltage threshold on VDD falling Note 1	1.44	1.50	1.56	V
Minimum pulse width Note 2	TPW		300			μs

Note 1. However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in 3.4 AC Characteristics.

Note 2. Minimum time required for a POR reset when VDD exceeds below VPDR. This is also the minimum time required for a POR reset from when VDD exceeds below 0.7 V to when VDD exceeds VPOR while STOP mode is entered or the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



3.6.6 LVD circuit characteristics

(1) Reset Mode and Interrupt Mode

(TA = -40 to +105°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit		
Voltage detection threshold	Supply voltage level	VLVD0	Rising edge	3.90	4.06	4.22	V		
			Falling edge	3.83	3.98	4.13	V		
		VLVD1	Rising edge	3.60	3.75	3.90	V		
			Falling edge	3.53	3.67	3.81	V		
		VLVD2	Rising edge	3.01	3.13	3.25	V		
			Falling edge	2.94	3.06	3.18	V		
		VLVD3	Rising edge	2.90	3.02	3.14	V		
			Falling edge	2.85	2.96	3.07	V		
		VLVD4	Rising edge	2.81	2.92	3.03	V		
			Falling edge	2.75	2.86	2.97	V		
		VLVD5	Rising edge	2.70	2.81	2.92	V		
			Falling edge	2.64	2.75	2.86	V		
		VLVD6	Rising edge	2.61	2.71	2.81	V		
			Falling edge	2.55	2.65	2.75	V		
		VLVD7	Rising edge	2.51	2.61	2.71	V		
			Falling edge	2.45	2.55	2.65	V		
		Minimum pulse width		tLW		300			μs
		Detection delay time						300	μs

(2) Interrupt & Reset Mode**(TA = -40 to +105°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit	
Voltage detection threshold	VLVDD0	VPOC2, VPOC1, VPOC0 = 0, 1, 1, falling reset voltage	2.64	2.75	2.86	V	
	VLVDD1	LVIS1, LVIS0 = 1, 0	Rising release reset voltage	2.81	2.92	3.03	V
			Falling interrupt voltage	2.75	2.86	2.97	V
	VLVDD2	LVIS1, LVIS0 = 0, 1	Rising release reset voltage	2.90	3.02	3.14	V
			Falling interrupt voltage	2.85	2.96	3.07	V
	VLVDD3	LVIS1, LVIS0 = 0, 0	Rising release reset voltage	3.90	4.06	4.22	V
			Falling interrupt voltage	3.83	3.98	4.13	V

3.6.7 Power supply voltage rising slope characteristics**(TA = -40 to +105°C, VSS = 0 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	SVDD				54	V/ms

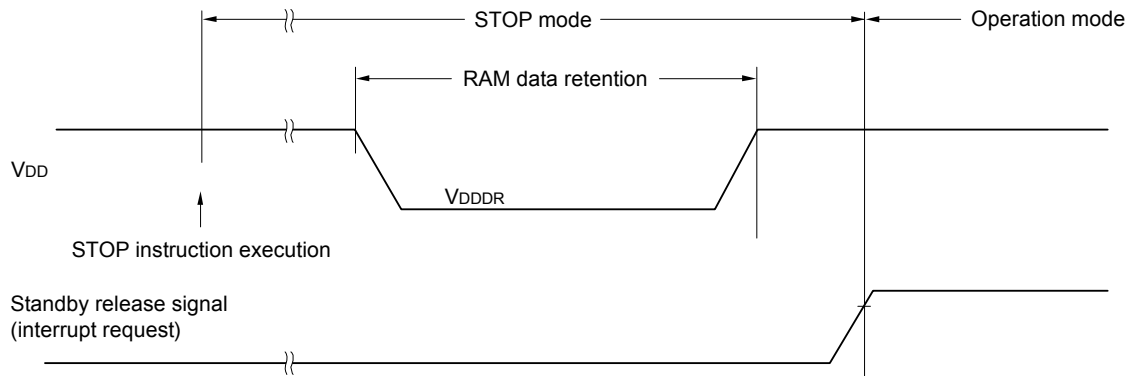
Caution Make sure to keep the internal reset state by the LVD circuit or an external reset until VDD reaches the operating voltage range shown in 3.4 AC Characteristics.

3.7 RAM Data Retention Characteristics

(TA = -40 to +105°C, VSS = 0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	VDDDR		1.44 Note		5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



3.8 Flash Memory Programming Characteristics

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	fCLK	2.4 V ≤ VDD ≤ 5.5 V	1		32	MHz
Number of code flash rewrites Notes 1, 2, 3	C _{erwr}	Retained for 20 years TA = 85°C Note 4	1,000			Times
Number of data flash rewrites Notes 1, 2, 3		Retained for 1 year TA = 25°C		1,000,000		
		Retained for 5 years TA = 85°C Note 4	100,000			
		Retained for 20 years TA = 85°C Note 4	10,000			

- Note 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.
- Note 2.** When using flash memory programmer and Renesas Electronics self-programming library
- Note 3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.
- Note 4.** This temperature is the average value at which data are retained.

3.9 Dedicated Flash Memory Programmer Communication (UART)

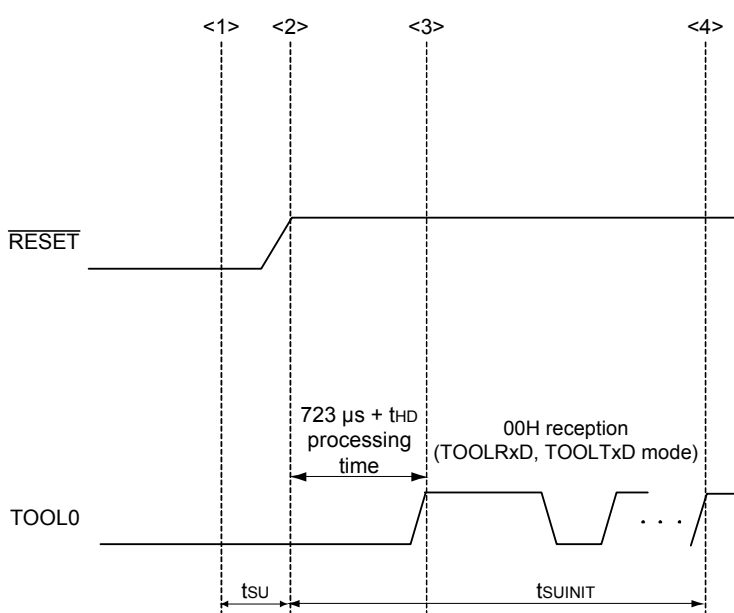
(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

3.10 Timing of Entry to Flash Memory Programming Modes

(TA = -40 to +105°C, 2.4 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	tsuINIT	POR and LVD reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	tsu	POR and LVD reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	tHD	POR and LVD reset must end before the external reset ends.	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset ends (POR and LVD reset must end before the external reset ends).
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark tsuINIT: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

tsu: How long from when the TOOL0 pin is placed at the low level until a pin reset ends

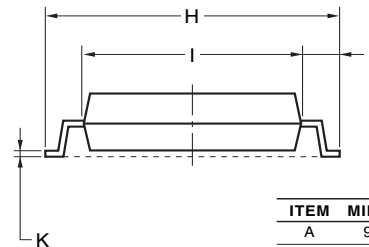
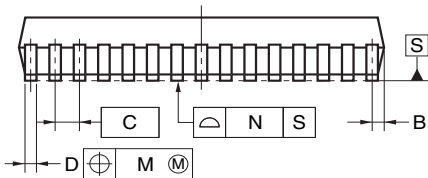
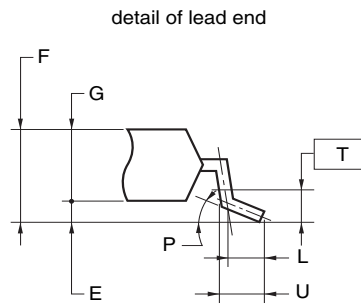
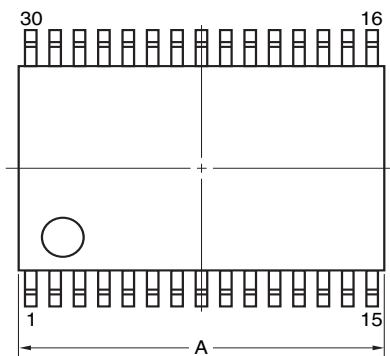
tHD: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

4. PACKAGE DRAWINGS

4.1 30-pin products

R5F104AAASP, R5F104ACASP, R5F104ADASP, R5F104AEASP, R5F104AFASP, R5F104AGASP
 R5F104AADSP, R5F104ACDSP, R5F104ADDSP, R5F104AEDSP, R5F104AFDSP, R5F104AGDSP
 R5F104AAGSP, R5F104ACGSP, R5F104ADGSP, R5F104AEGSP, R5F104AFGSP, R5F104AGGSP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



NOTE
 Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

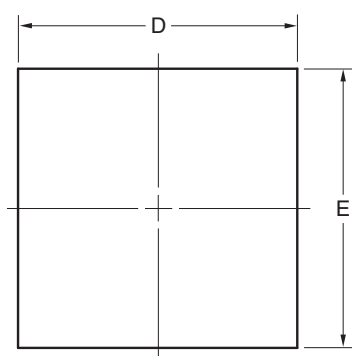
ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	0.24 ^{+0.08} _{-0.07}
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	3° ^{+5°} _{-3°}
T	0.25
U	0.6±0.15

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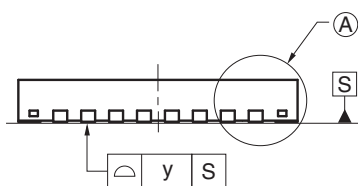
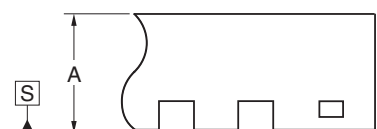
4.2 32-pin products

R5F104BAANA, R5F104BCANA, R5F104BDANA, R5F104BEANA, R5F104BFANA, R5F104BGANA
 R5F104BADNA, R5F104BCDNA, R5F104BDDNA, R5F104BEDNA, R5F104BFDNA, R5F104BGDNA
 R5F104BAGNA, R5F104BCGNA, R5F104BDGNA, R5F104BEGNA, R5F104BFGNA, R5F104BGGNA

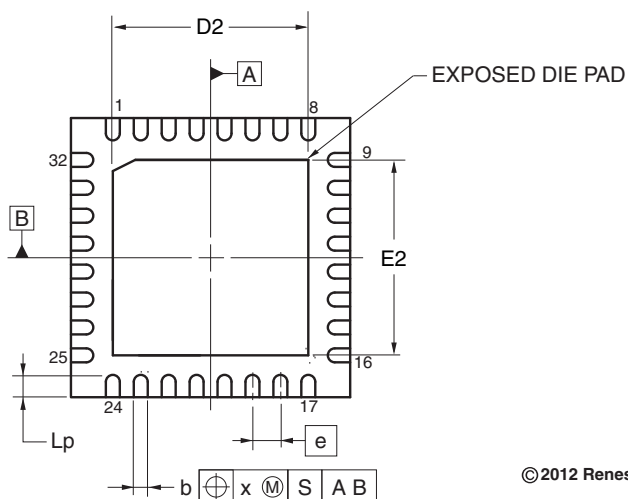
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN32-5x5-0.50	PWQN0032KB-A	P32K8-50-3B4-4	0.06



DETAIL OF (A) PART



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.95	5.00	5.05
E	4.95	5.00	5.05
A	0.70	0.75	0.80
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05

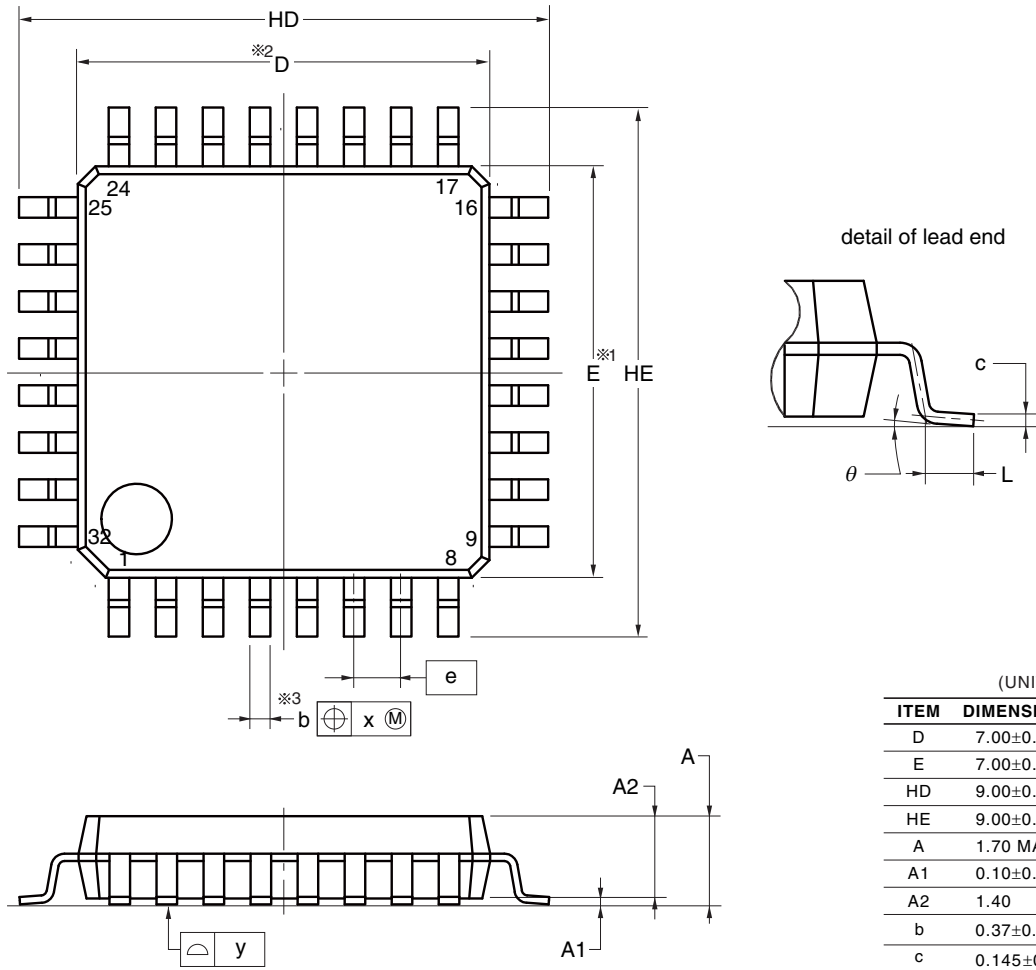


ITEM	A	D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS		3.45	3.50	3.55	3.45	3.50	3.55

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R5F104BAAFP, R5F104BCAFP, R5F104BDAFP, R5F104BEAFP, R5F104BF AFP, R5F104BG AFP
 R5F104BADFP, R5F104BCDFP, R5F104BDDFP, R5F104BEDFP, R5F104BFDFP, R5F104BGDFP
 R5F104BAGFP, R5F104BCGFP, R5F104BDGFP, R5F104BEGFP, R5F104BFGFP, R5F104BGGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.10
E	7.00±0.10
HD	9.00±0.20
HE	9.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	0.37±0.05
c	0.145±0.055
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

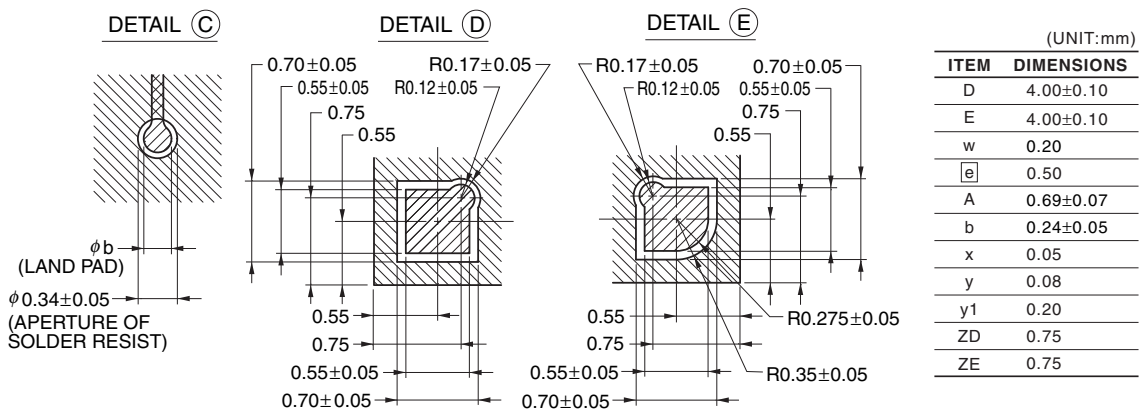
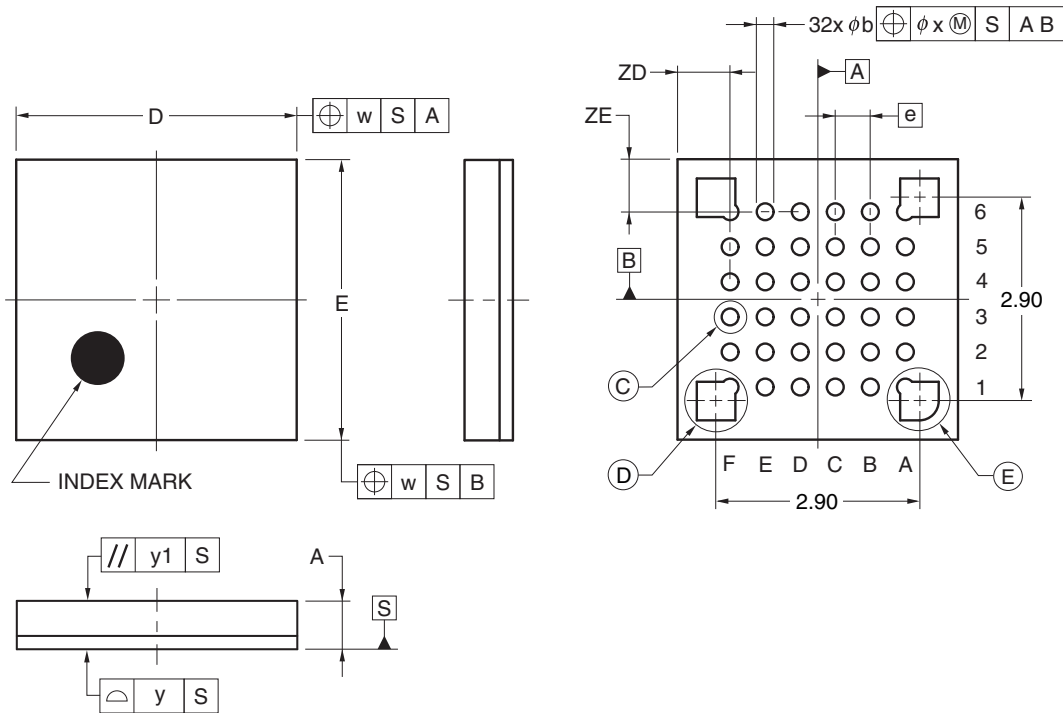
NOTE
 1. Dimensions "※1" and "※2" do not include mold flash.
 2. Dimension "※3" does not include trim offset.

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4.3 36-pin products

R5F104CAALA, R5F104CCALA, R5F104CDALA, R5F104CEALA, R5F104CFALA, R5F104CGALA
 R5F104CAGLA, R5F104CCGLA, R5F104CDGLA, R5F104CEGLA, R5F104CFGLA, R5F104CGGLA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-WFLGA36-4x4-0.50	PWLG0036KA-A	P36FC-50-AA4-2	0.023

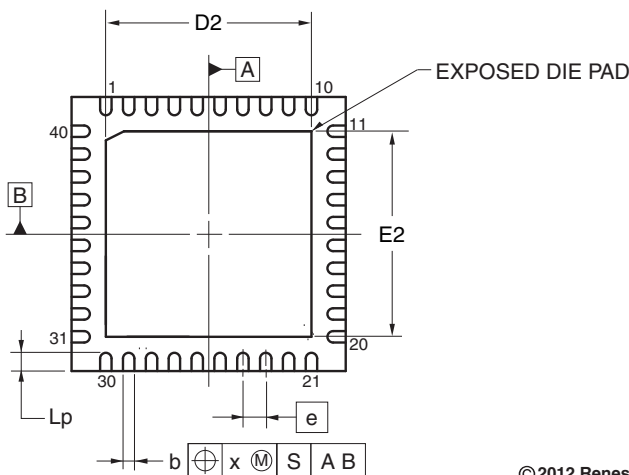
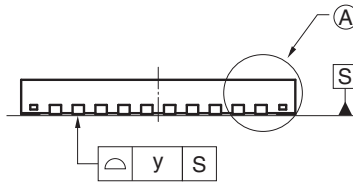
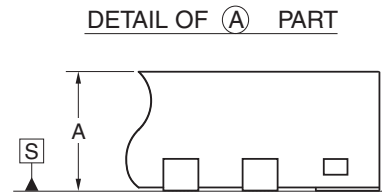
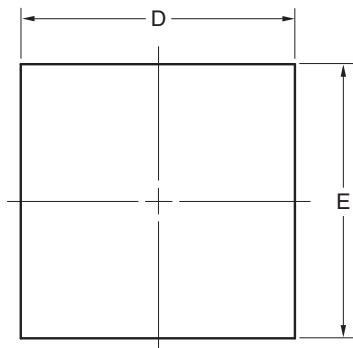


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4.4 40-pin products

R5F104EAANA, R5F104ECANA, R5F104EDANA, R5F104EEANA, R5F104EFANA, R5F104EGANA, R5F104EHANA
 R5F104EADNA, R5F104ECDNA, R5F104EDDNA, R5F104EEDNA, R5F104EFDNA, R5F104EGDNA, R5F104EHDNA
 R5F104EAGNA, R5F104ECGNA, R5F104EDGNA, R5F104EEGNA, R5F104EFGNA, R5F104EGGNA, R5F104EHGNA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN40-6x6-0.50	PWQN0040KC-A	P40K8-50-4B4-4	0.09



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	5.95	6.00	6.05
E	5.95	6.00	6.05
A	0.70	0.75	0.80
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05

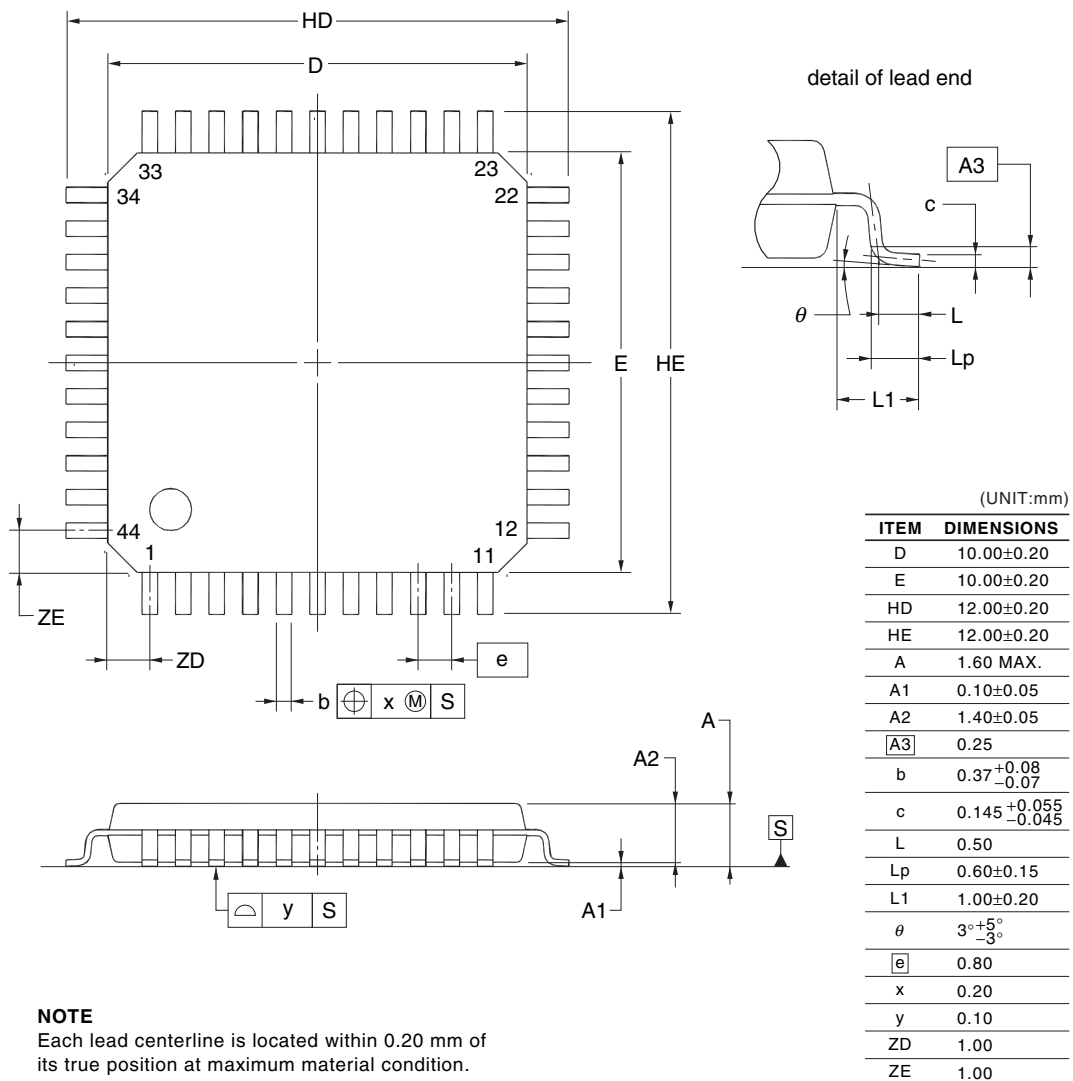
ITEM	A	D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS		4.45	4.50	4.55	4.45	4.50	4.55

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4.5 44-pin products

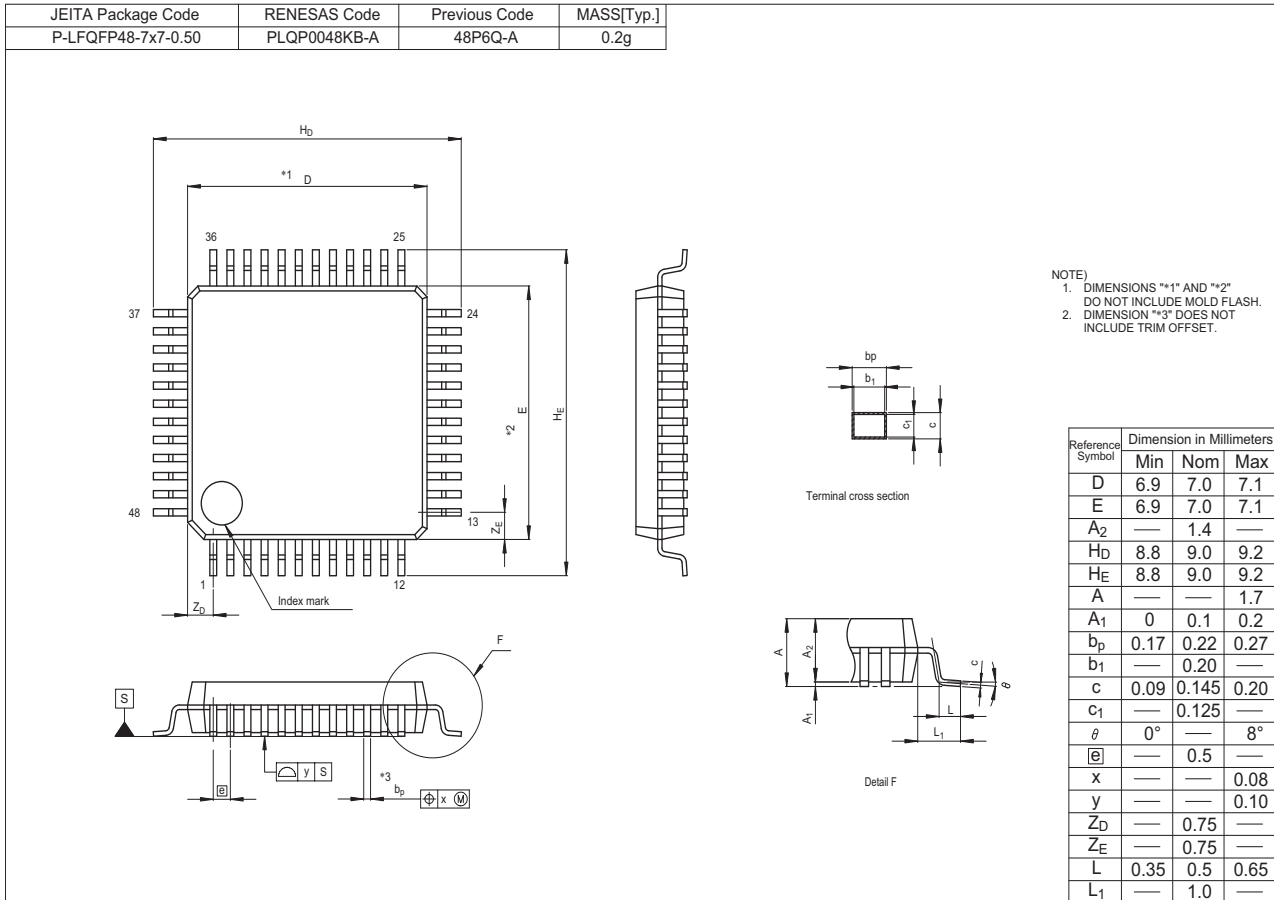
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 R5F104FADFP, R5F104FCDFP, R5F104FDDFP, R5F104FEDFP, R5F104FFDFP, R5F104FGDFP,
 R5F104FHDFP, R5F104FJDFP
 R5F104FAGFP, R5F104FCGFP, R5F104FDGFP, R5F104FEGFP, R5F104FFGFP, R5F104FGGFP,
 R5F104FHGFP, R5F104FJGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP44-10x10-0.80	PLQP0044GC-A	P44GB-80-UES-2	0.36



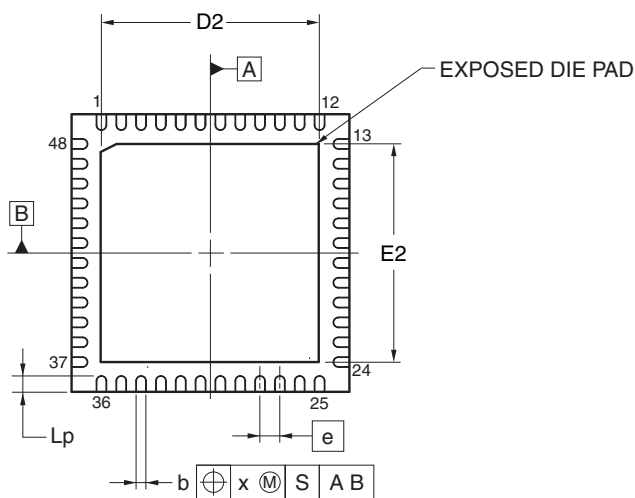
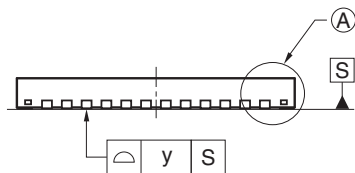
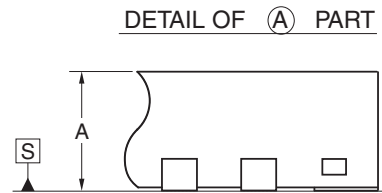
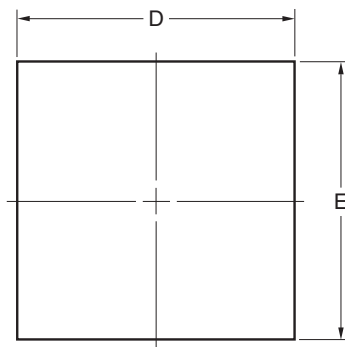
NOTE
 Each lead centerline is located within 0.20 mm of its true position at maximum material condition.

R5F104GKAFB, R5F104GLAFB
 R5F104GKGFB, R5F104GLGFB



R5F104GAANA, R5F104GCANA, R5F104GDANA, R5F104GEANA, R5F104GFANA, R5F104GGANA,
 R5F104GHANA, R5F104GJANA
 R5F104GADNA, R5F104GCDNA, R5F104GDDNA, R5F104GEDNA, R5F104GFDNA, R5F104GGDNA,
 R5F104GHDNA, R5F104GJDNA
 R5F104GAGNA, R5F104GCGNA, R5F104GDGNA, R5F104GEGNA, R5F104GFGNA, R5F104GGGNA,
 R5F104GHGNA, R5F104GJGNA
 R5F104GKANA, R5F104GLANA
 R5F104GKGNA, R5F104GLGNA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-HWQFN48-7x7-0.50	PWQN0048KB-A	48PJN-A P48K8-50-5B4-5	0.13



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.95	7.00	7.05
E	6.95	7.00	7.05
A	0.70	0.75	0.80
b	0.18	0.25	0.30
e	—	0.50	—
Lp	0.30	0.40	0.50
x	—	—	0.05
y	—	—	0.05

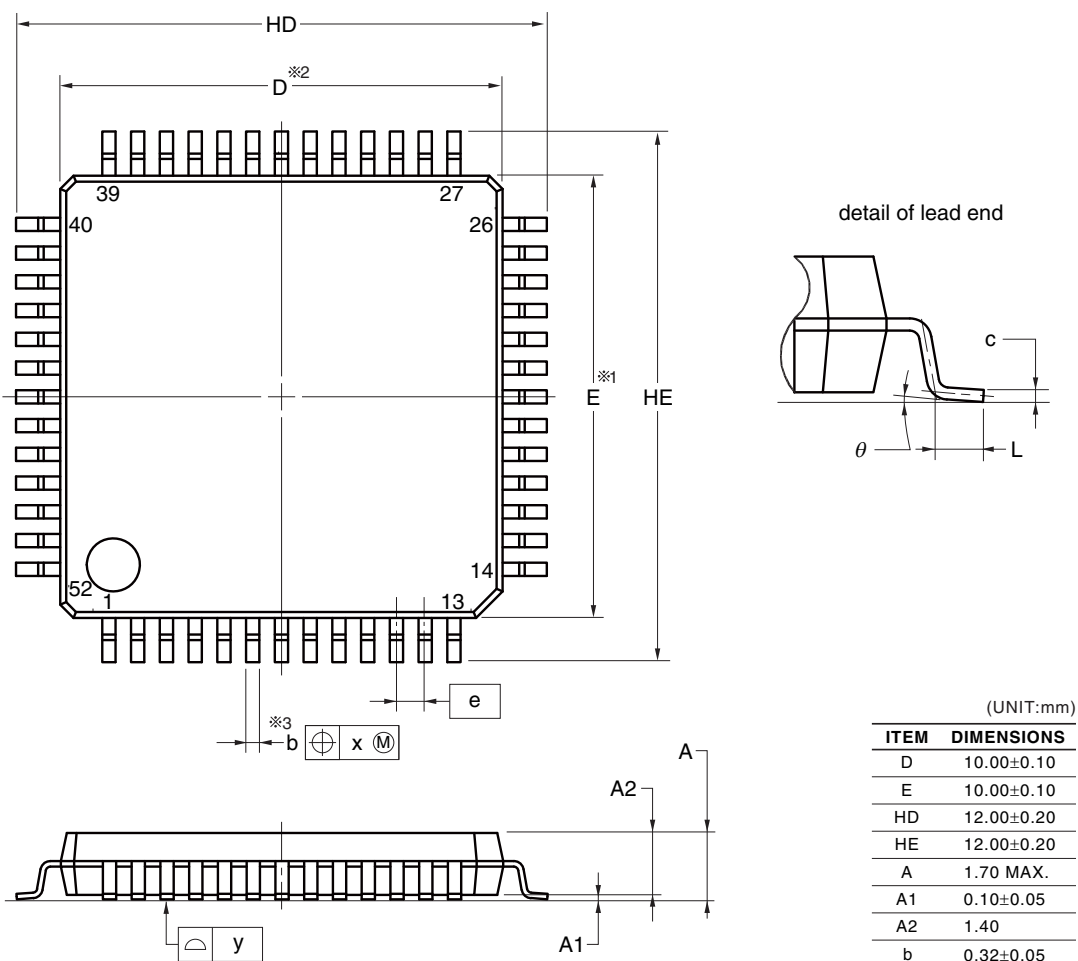
ITEM		D2			E2		
		MIN	NOM	MAX	MIN	NOM	MAX
EXPOSED DIE PAD VARIATIONS	A	5.45	5.50	5.55	5.45	5.50	5.55

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4.7 52-pin products

R5F104JCAFA, R5F104JDAFA, R5F104JEAFA, R5F104JFAFA, R5F104JGAFA, R5F104JHAFA, R5F104JJAFA
 R5F104JCDAFA, R5F104JDDFA, R5F104JEDFA, R5F104JFDFA, R5F104JGDFA, R5F104JHDFA, R5F104JJDFA
 R5F104JCGFA, R5F104JDGFA, R5F104JEGFA, R5F104JFGFA, R5F104JGGFA, R5F104JHGFA, R5F104JJGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	P52GB-65-GBS-1	0.3



NOTE

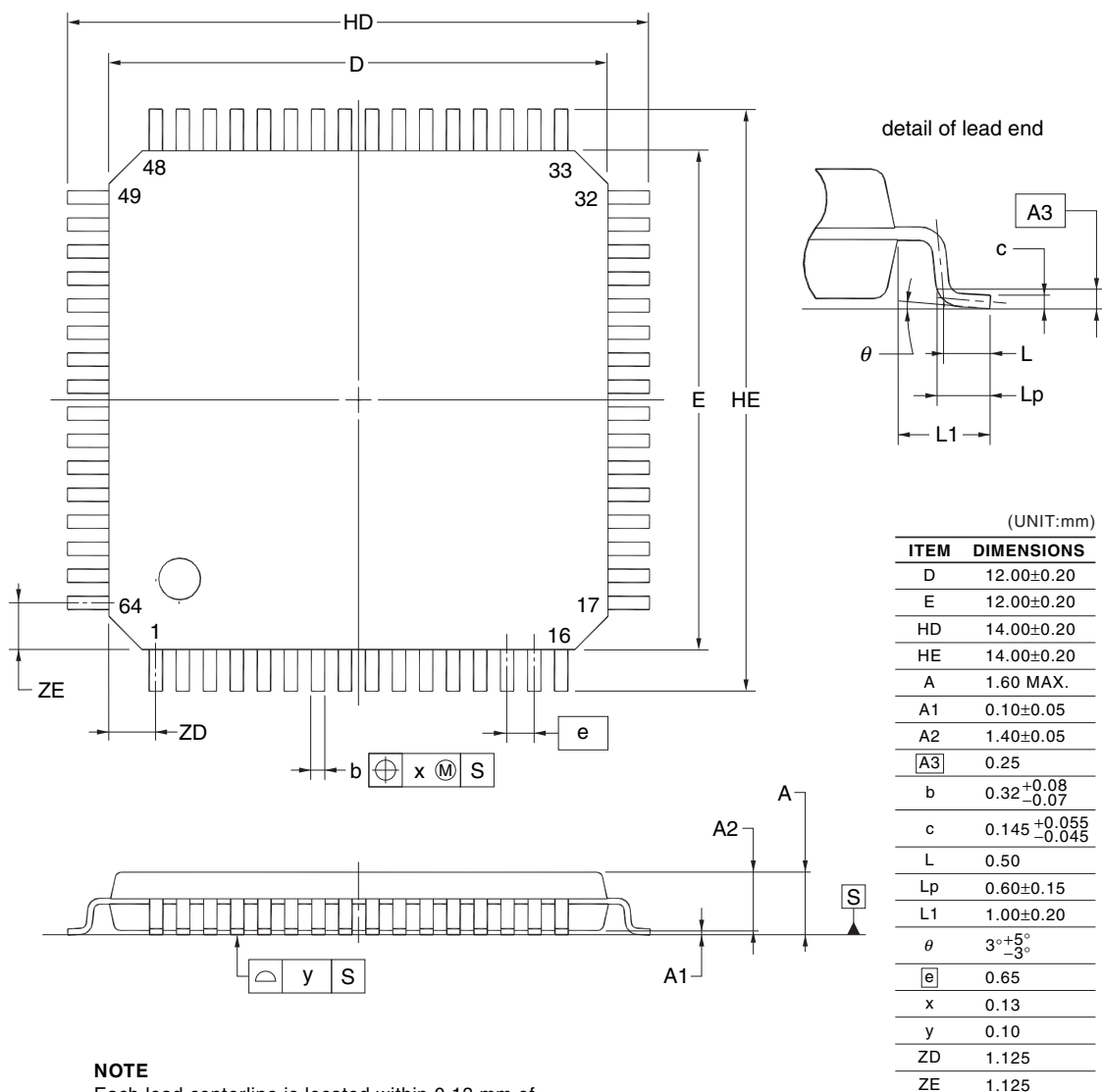
1. Dimensions "※1" and "※2" do not include mold flash.
2. Dimension "※3" does not include trim offset.

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4.8 64-pin products

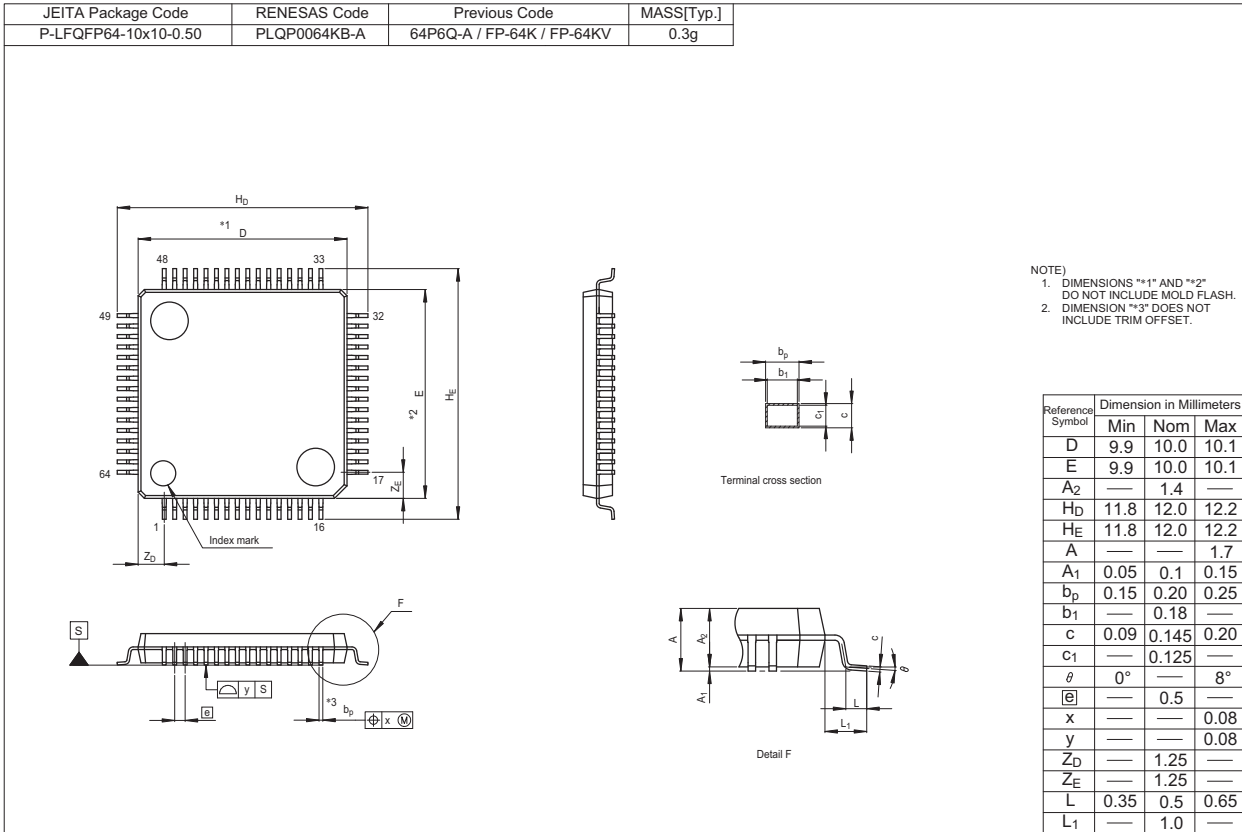
R5F104LCAFA, R5F104LDAFA, R5F104LEAFA, R5F104LFAFA, R5F104LGAFa, R5F104LHAFA, R5F104LJAFA
 R5F104LCDFA, R5F104LDDFA, R5F104LEDFA, R5F104LFDFA, R5F104LGDFa, R5F104LHDFa, R5F104LJDFa
 R5F104LCGFA, R5F104LDGFA, R5F104LEGFA, R5F104LFGFA, R5F104LGGFA, R5F104LHGFA, R5F104LJGFA
 R5F104LKAFA, R5F104LLAFA
 R5F104LKGFA, R5F104LLGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51



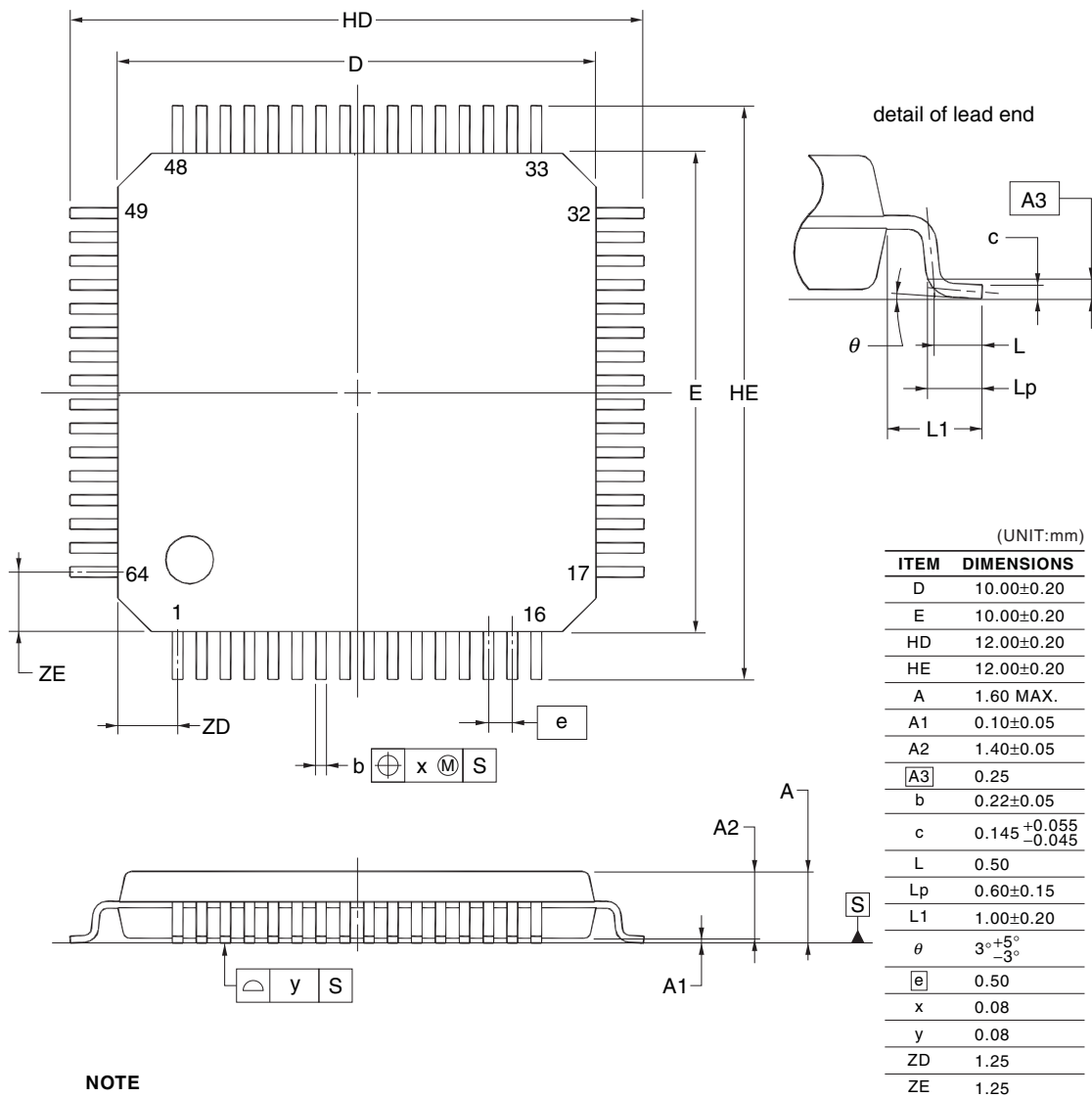
NOTE
 Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

R5F104LKAFB, R5F104LLAFB
 R5F104LKGFB, R5F104LLGFB



R5F104LCAFB, R5F104LDAFB, R5F104LEAFB, R5F104LFAFB, R5F104LGAFB, R5F104LHAFB,
 R5F104LJAFB
 R5F104LCDFB, R5F104LDDFB, R5F104LEDFB, R5F104LDFB, R5F104LGDFB, R5F104LHDFB,
 R5F104LJDFB
 R5F104LCGFB, R5F104LDGFB, R5F104LEGFB, R5F104LFGFB, R5F104LGGFB, R5F104LHGFB,
 R5F104LJGFB

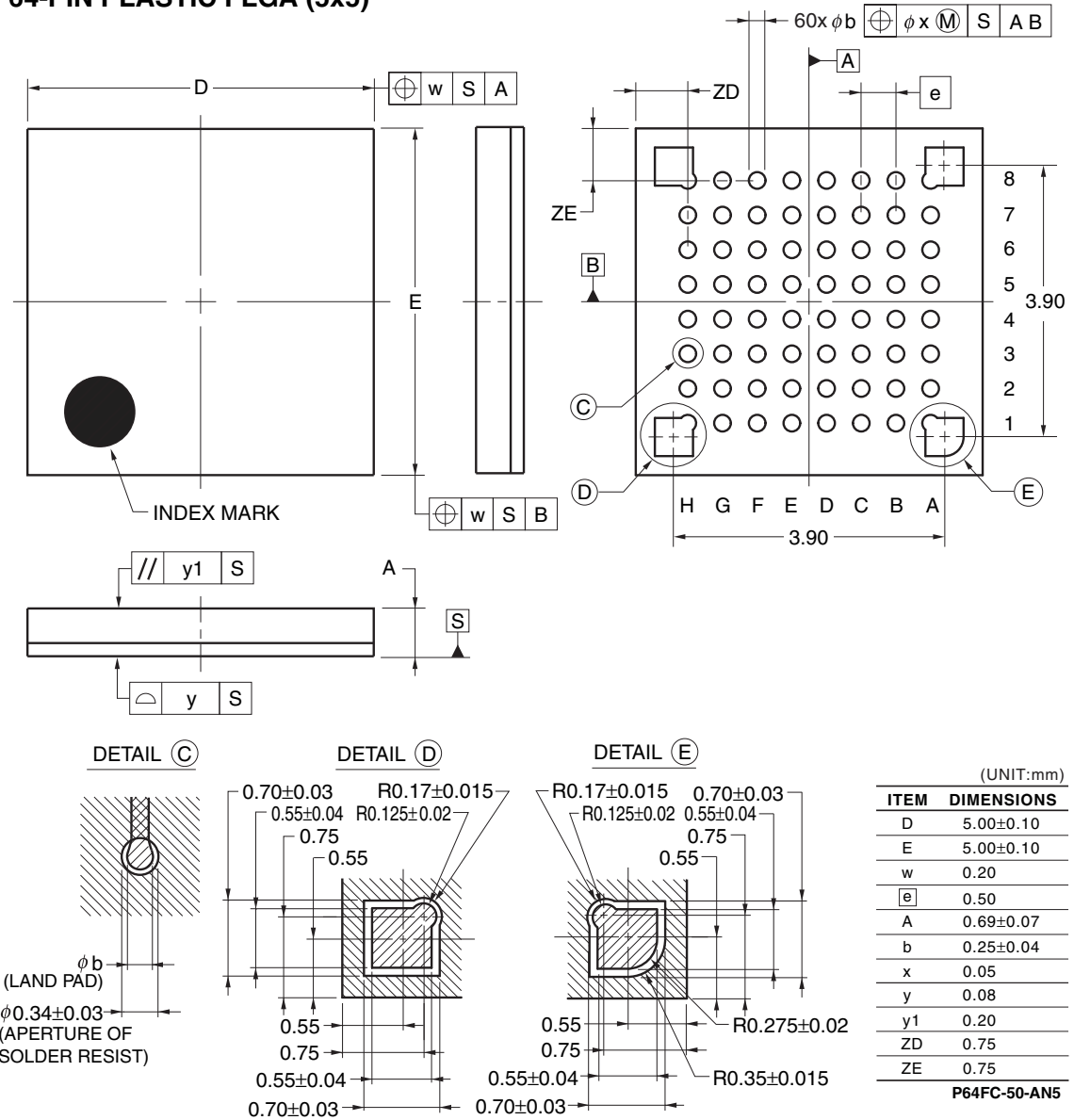
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP64-10x10-0.50	PLQP0064KF-A	P64GB-50-UEU-2	0.35



NOTE
 Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F104LCALA, R5F104LDALA, R5F104LEALA, R5F104LFALA, R5F104LGALA, R5F104LHALA, R5F104LJALA
 R5F104LKALA, R5F104LLALA
 R5F104LCGLA, R5F104LDGLA, R5F104LEGLA, R5F104LFGLA, R5F104LGGLA, R5F104LHGLA, R5F104LJGLA
 R5F104LKGLA, R5F104LLGLA

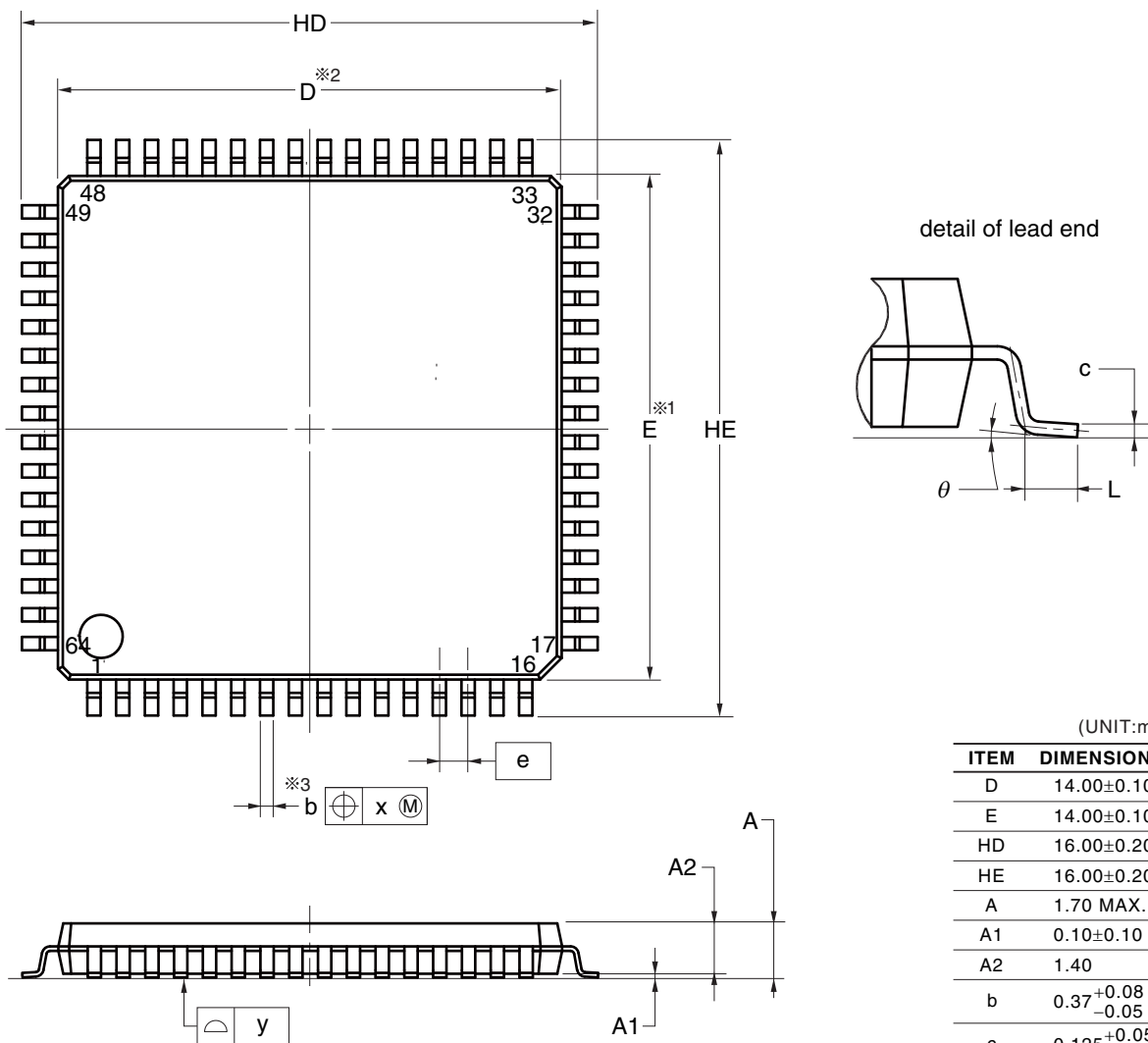
64-PIN PLASTIC FLGA (5x5)



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R5F104LCAFP, R5F104LDAFP, R5F104LEAFP, R5F104LFAFP, R5F104LGAFP, R5F104LHAFP, R5F104LJAFP
 R5F104LCDFP, R5F104LDDFP, R5F104LEDFP, R5F104LDFP, R5F104LGDFP, R5F104LHDFP, R5F104LJDFP
 R5F104LCGFP, R5F104LDGFP, R5F104LEGFP, R5F104LFGFP, R5F104LGGFP, R5F104LHGFP, R5F104LJGFP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-14x14-0.80	PLQP0064GA-A	P64GC-80-GBW-1	0.7



(UNIT:mm)

ITEM	DIMENSIONS
D	14.00±0.10
E	14.00±0.10
HD	16.00±0.20
HE	16.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	0.37 ^{+0.08} _{-0.05}
c	0.125 ^{+0.05} _{-0.02}
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

NOTE

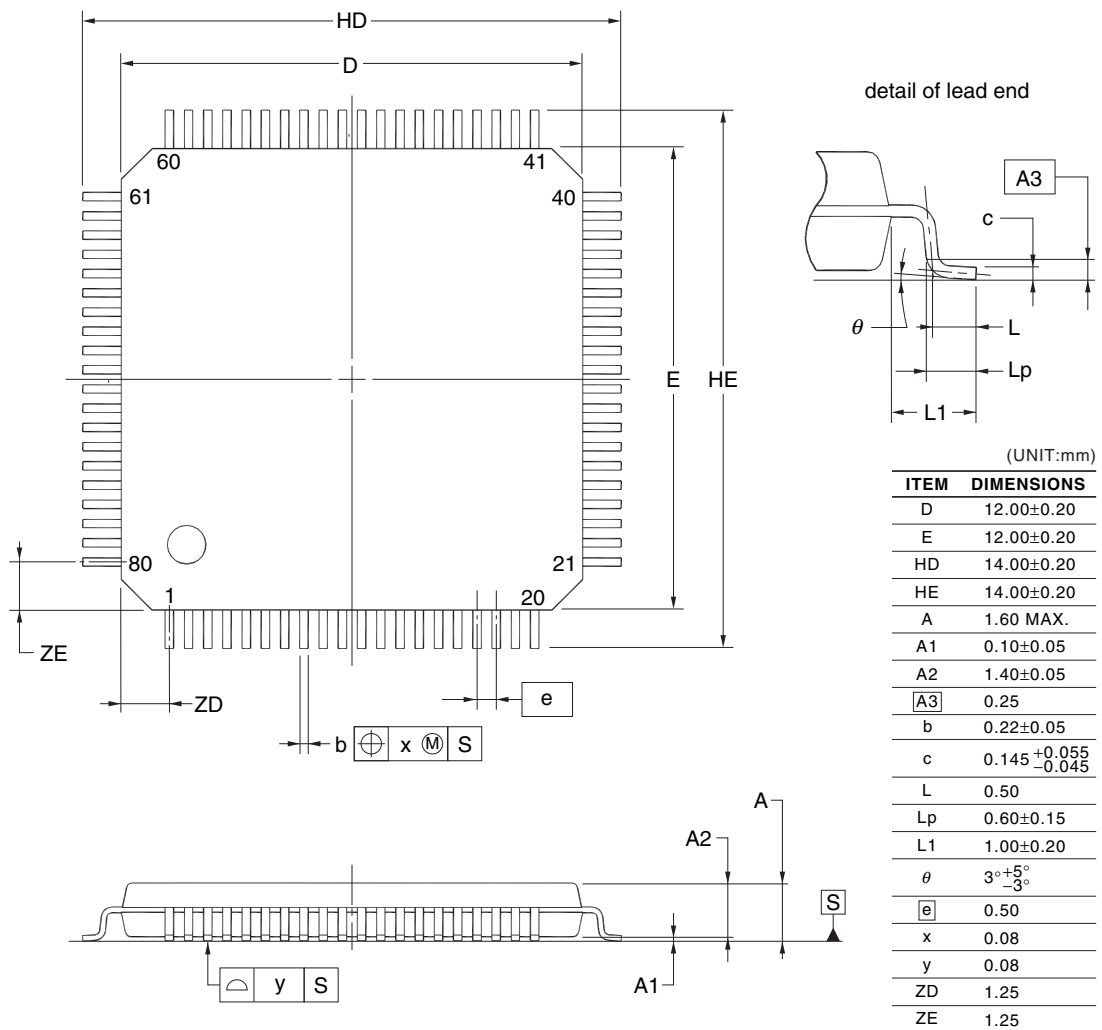
1. Dimensions “*1” and “*2” do not include mold flash.
2. Dimension “*3” does not include trim offset.

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4.9 80-pin products

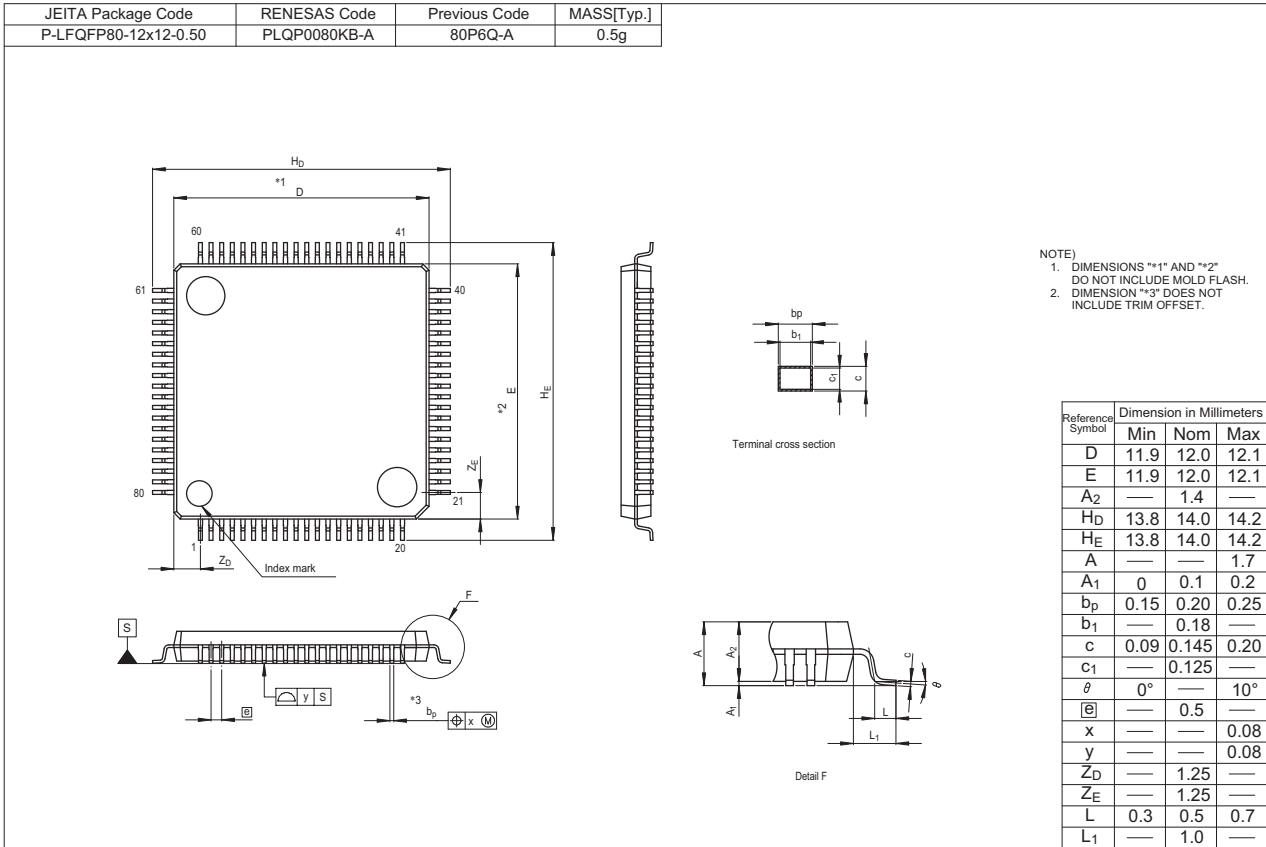
R5F104MFAFB, R5F104MGAFB, R5F104MHAFB, R5F104MJAFB
 R5F104MDFB, R5F104MGDFB, R5F104MHDFB, R5F104MJDFB
 R5F104MFGFB, R5F104MGGFB, R5F104MHGFB, R5F104MJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP80-12x12-0.50	PLQP0080KE-A	P80GK-50-8EU-2	0.53



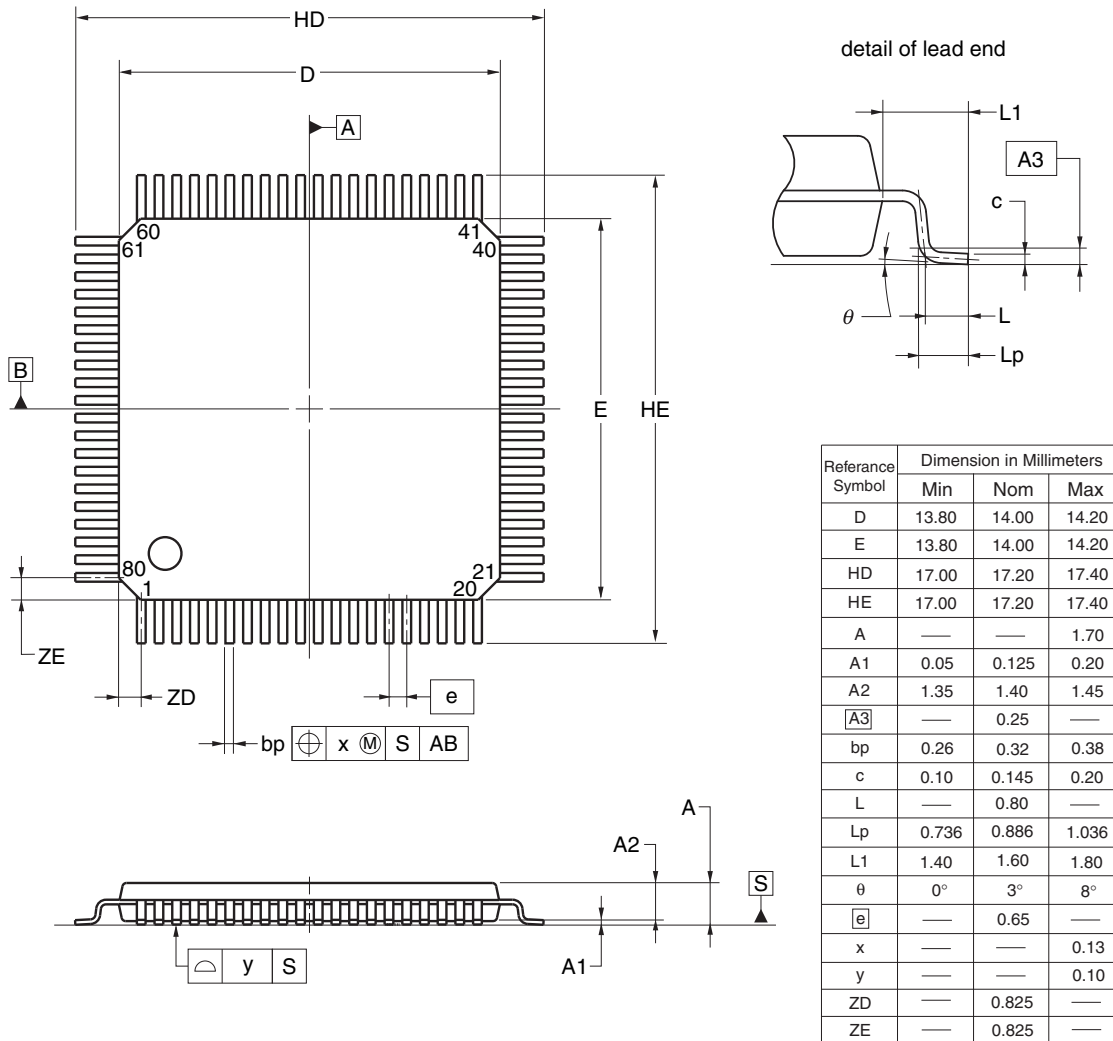
NOTE
 Each lead centerline is located within 0.08 mm of its true position at maximum material condition.

R5F104MKAFB, R5F104MLAFB
 R5F104MKGFB, R5F104MLGFB



R5F104MFAFA, R5F104MGAFA, R5F104MHFAFA, R5F104MJFAFA
 R5F104MFDFA, R5F104MGDFA, R5F104MHDFA, R5F104MJDFA
 R5F104MFGFA, R5F104MGGFA, R5F104MHGFA, R5F104MJGFA
 R5F104MKAFA, R5F104MLAFA
 R5F104MKGFA, R5F104MLGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP80-14x14-0.65	PLQP0080JB-E	P80GC-65-UBT-2	0.69

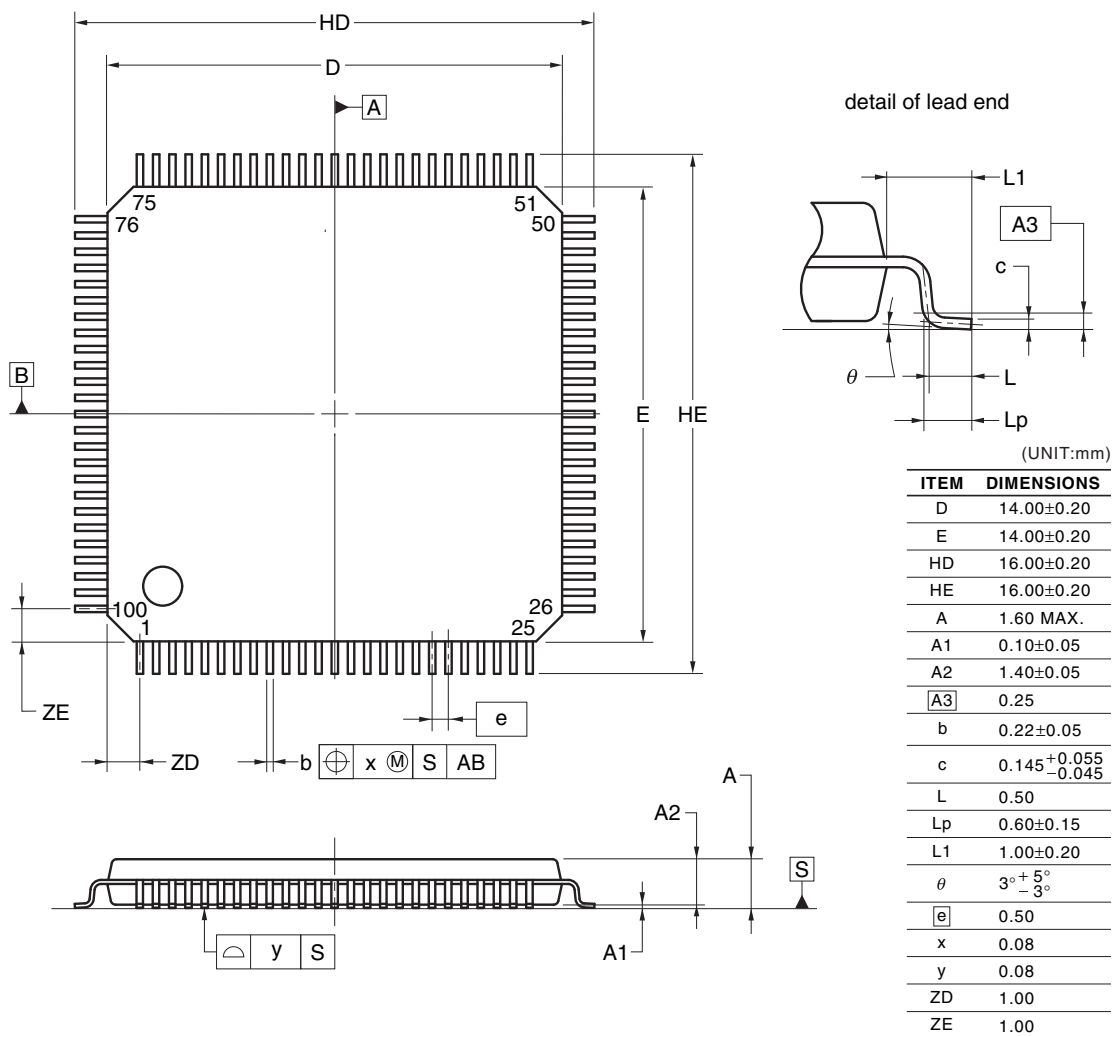


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4.10 100-pin products

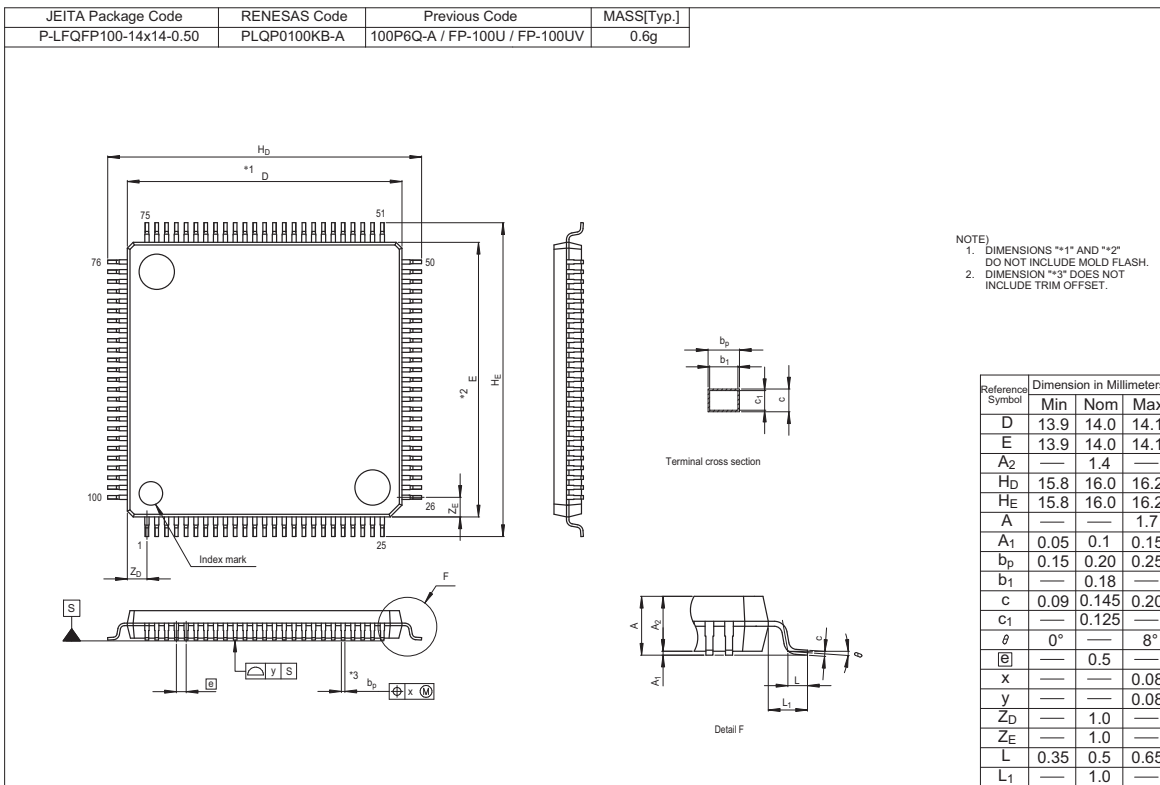
R5F104PFAFB, R5F104PGAFA, R5F104PHAFA, R5F104PJAFB
 R5F104PFDFB, R5F104PGDFB, R5F104PHDFB, R5F104PJDFB
 R5F104PFGFB, R5F104PGGFB, R5F104PHGFB, R5F104PJGFB

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP100-14x14-0.50	PLQP0100KE-A	P100GC-50-GBR-1	0.69



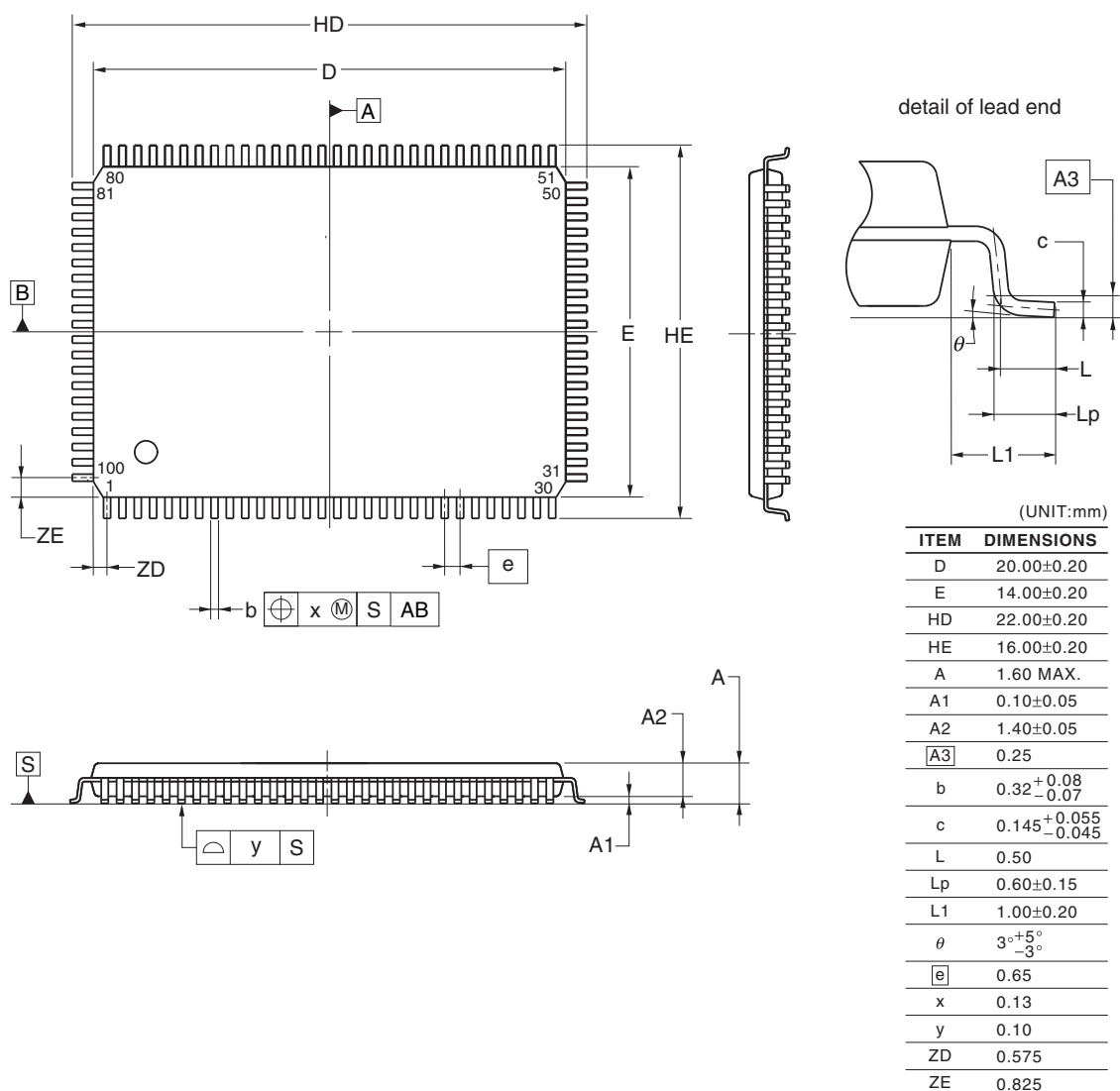
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R5F104PKAFB, R5F104PLAFB
 R5F104PKGFB, R5F104PLGFB



R5F104PFAFA, R5F104PGAFA, R5F104PHAFA, R5F104PJAJA
 R5F104PFDFA, R5F104PGDFA, R5F104PHDFA, R5F104PJJFA
 R5F104PFGFA, R5F104PGGFA, R5F104PHGFA, R5F104PJJFA
 R5F104PKAJA, R5F104PLAJA
 R5F104PKGFA, R5F104PLGFA

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP100-14x20-0.65	PLQP0100JC-A	P100GF-65-GBN-1	0.92



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REVISION HISTORY

RL78/G14 Datasheet

Rev.	Date	Description	
		Page	Summary
0.01	Feb 10, 2011	—	First Edition issued
0.02	May 01, 2011	1 to 2	1.1 Features revised
		3	1.2 Ordering Information revised
		4 to 13	1.3 Pin Configuration (Top View) revised
		14	1.4 Pin Identification revised
		15 to 17	1.5.1 30-pin products to 1.5.3 36-pin products revised
		23 to 26	1.6 Outline of Functions revised
0.03	Jul 28, 2011	1	1.1 Features revised
1.00	Feb 21, 2012	1 to 40	1. OUTLINE revised
		41 to 97	2. ELECTRICAL SPECIFICATIONS added
2.00	Oct 25, 2013	1	Modification of 1.1 Features
		3 to 8	Modification of 1.2 Ordering Information
		9 to 22	Modification of package type in 1.3 Pin Configuration (Top View)
		34 to 43	Modification of description of subsystem clock in 1.6 Outline of Functions
		34 to 43	Modification of description of timer output in 1.6 Outline of Functions
		34 to 43	Modification of error of data transfer controller in 1.6 Outline of Functions
		34 to 43	Modification of error of event link controller in 1.6 Outline of Functions
		45, 46	Modification of description of Tables in 2.1 Absolute Maximum Ratings
		47	Modification of Tables, notes, cautions, and remarks in 2.2 Oscillator Characteristics
		48	Modification of error of conditions of high level input voltage in 2.3.1 Pin characteristics
		49	Modification of error of conditions of low level output voltage in 2.3.1 Pin characteristics
		53 to 62	Modification of Notes and Remarks in 2.3.2 Supply current characteristics
		65, 66	Addition of Minimum Instruction Execution Time during Main System Clock Operation
		67 to 69	Addition of AC Timing Test Points
		70 to 97	Addition of LS mode and LV mode characteristics in 2.5.1 Serial array unit
		98 to 101	Addition of LS mode and LV mode characteristics in 2.5.2 Serial interface IICA
		102 to 105	Addition of characteristics about conversion of internal reference voltage and temperature sensor in 2.6.1 A/D converter characteristics
107	Addition of characteristic in 2.6.4 Comparator		
107	Deletion of detection delay in 2.6.5 POR circuit characteristics		
109	Modification of 2.6.7 Power supply voltage rising slope characteristics		
110	Modification of 2.7 Data Memory STOP Mode Low Supply Voltage Data Retention Characteristics		
110	Addition of characteristic in 2.8 Flash Memory Programming Characteristics		
111	Addition of description in 2.10 Timing for Switching Flash Memory Programming Modes		

REVISION HISTORY

RL78/G14 Datasheet

Rev.	Date	Description	
		Page	Summary
2.00	Oct 25, 2013	112 to 169 171 to 187	Addition of CHAPTER 3 ELECTRICAL SPECIFICATIONS Modification of 4.1 30-pin products to 4.10 100-pin products
3.00	Feb 07, 2014	All 1 2 3 6 to 8 15, 16 17 18, 19 20 21, 22 35, 37, 39, 41, 43, 45, 47 42, 43 46, 47 65 to 68 118 137 to 140 180 189, 190 191 193 to 195 198, 199 201, 202	Addition of products with maximum 512 KB flash ROM and 48 KB RAM Modification of 1.1 Features Modification of ROM, RAM capacities and addition of note 3 Modification of Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G14 Addition of part number Modification of 1.3.6 48-pin products Modification of 1.3.7 52-pin products Modification of 1.3.8 64-pin products Modification of 1.3.9 80-pin products Modification of 1.3.10 100-pin products Modification of operating ambient temperature in 1.6 Outline of Functions Addition of table of 48-pin, 52-pin, 64-pin products (code flash memory 384 KB to 512 KB) Addition of table of 80-pin, 100-pin products (code flash memory 384 KB to 512 KB) Addition of (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products Modification of 2.7 Data Memory Retention Characteristics Addition of (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products Modification of 3.7 Data Memory Retention Characteristics Addition and modification of 4.6 48-pin products Modification of 4.7 52-pin products Addition and modification of 4.8 64-pin products Addition and modification of 4.9 80-pin products Addition and modification of 4.10 100-pin products
3.20	Jan 05, 2015	p.2 p.6 p.6 to 8 p.17 p.36, 39, 42, 45, 48, 50, 52 p.46, 48 p.47 p.62, 64, 66, 68, 70, 72	Deletion of R5F104JK and R5F104JL from the list of ROM and RAM capacities and modification of note Deletion of ordering part numbers of R5F104JK and R5F104JL from 52-pin plastic LQFP package in 1.2 Ordering Information Deletion of note 2 in 1.2 Ordering Information Deletion of note 2 in 1.3.7 52-pin products Modification of description in 1.6 Outline of Functions Deletion of description of 52-pin in 1.6 Outline of Functions Modification of note of 1.6 Outline of Functions Modification of specifications in 2.3.2 Supply current characteristics

REVISION HISTORY	RL78/G14 Datasheet
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Rev.	Date	Description	
		Page	Summary
3.20	Jan 05, 2015	p.135, 137, 139, 141, 143, 145 p.197	Modification of specifications in 3.3.2 Supply current characteristics Modification of part number in 4.7 52-pin products
3.30	Aug 12, 2016	p.143, 145	Addition of maximum values in (3) Flash ROM: 384 to 512 KB of 48- to 100-pin products of 3.3.2 Supply current characteristics

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NOTES FOR CMOS DEVICES

- (1) **VOLTAGE APPLICATION WAVEFORM AT INPUT PIN:** Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).
- (2) **HANDLING OF UNUSED INPUT PINS:** Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.
- (3) **PRECAUTION AGAINST ESD:** A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.
- (4) **STATUS BEFORE INITIALIZATION:** Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.
- (5) **POWER ON/OFF SEQUENCE:** In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.
- (6) **INPUT OF SIGNAL DURING POWER OFF STATE :** Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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Renesas Electronics America Inc.

2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited

9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.

Room 1709, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.

Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited

Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

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13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.

80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.

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Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.

No.77C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.

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