RENESAS

RL78/G10

RENESAS MCU

True Low Power Platform (as low as 46 µA/MHz), 2.0 to 5.5V Operation,
1 to 4 Kbyte Flash for General Purpose Applications

R01DS0207EJ0100
Rev.1.00
Apr 15, 2013

1. OUTLINE

1.1 Features

Ultra-Low Power Technology
- 2.0 to 5.5 V operation from a single supply
- Stop (RAM retained): 0.56 µA
- Operating: 46 µA /MHz

RL78-S1 Core
- Instruction execution: 78 % of instructions can be executed in 1 to 2 clock cycles
- CISC architecture (Harvard) with 3-stage pipeline
- Multiply: 8 x 8 to 16-bit result in 2 clock cycles
- 16-bit barrel shifter for shift & rotate in 2 clock cycle
- 1-wire on-chip debug function

Main Flash Memory
- Density: 1 to 4 Kbyte
- Flash memory rewritable voltage: 4.5 to 5.5 V

RAM
- 128 to 512 Byte size options
- Supports operands or instructions
- Back-up retention in all modes

High-speed On-chip Oscillator
- 20 MHz with +/-2 % accuracy over voltage (2.0 to 5.5 V) and temperature (-20 to +85°C)
- Pre-configured settings: 20 MHz, 10 MHz, 5 MHz, 2.5 MHz, and 1.25 MHz

Reset and Supply Management
- Selectable power-on reset (SPOR) generator with 4 setting options

Multiple Communication Interfaces
- 1 x I^2C master
- 1 x I^2C multi-master (only for 16-pin product)
- 1 x UART (7-, 8-bit)
- Up to 2 x CSI/SPI (7-, 8-bit)

Extended-Function Timers
- Multi-function 16-bit timers: Up to 4 channels
- Interval timer: 12-bit, 1 channel (only for 16-pin product)
- 15 kHz watchdog timer : 1 channel

Rich Analog
- ADC: Up to 8 channels, 10-bit resolution, 3.4 µs conversion time
- Supports 2.4 V
- 1 x comparator (only for 16-pin product)

Safety Features
- Detects execution of illegal instruction
- Detects watchdog timer program loop

General Purpose I/O
- High-current (up to 20 mA per pin)
- Open-drain, internal pull-up support

External Interrupt
- External interrupt input: 4
- Key interrupt input: 6

Operating Ambient Temperature
- Standard: -40 to +85°C

Package Type and Pin Count
- SSOP: 10 and 16 pin

*** There is difference in specifications between every product. Please refer to specification for details.**

○ ROM, RAM capacities

Flash ROM	RAM	10 pins	16 pins
4 KB	512 B	–	R5F10Y47ASP Note 2
2 KB	256 B	R5F10Y16ASP	R5F10Y46ASP Note 2
1 KB	128 B	R5F10Y14ASP	R5F10Y44ASP Note 2

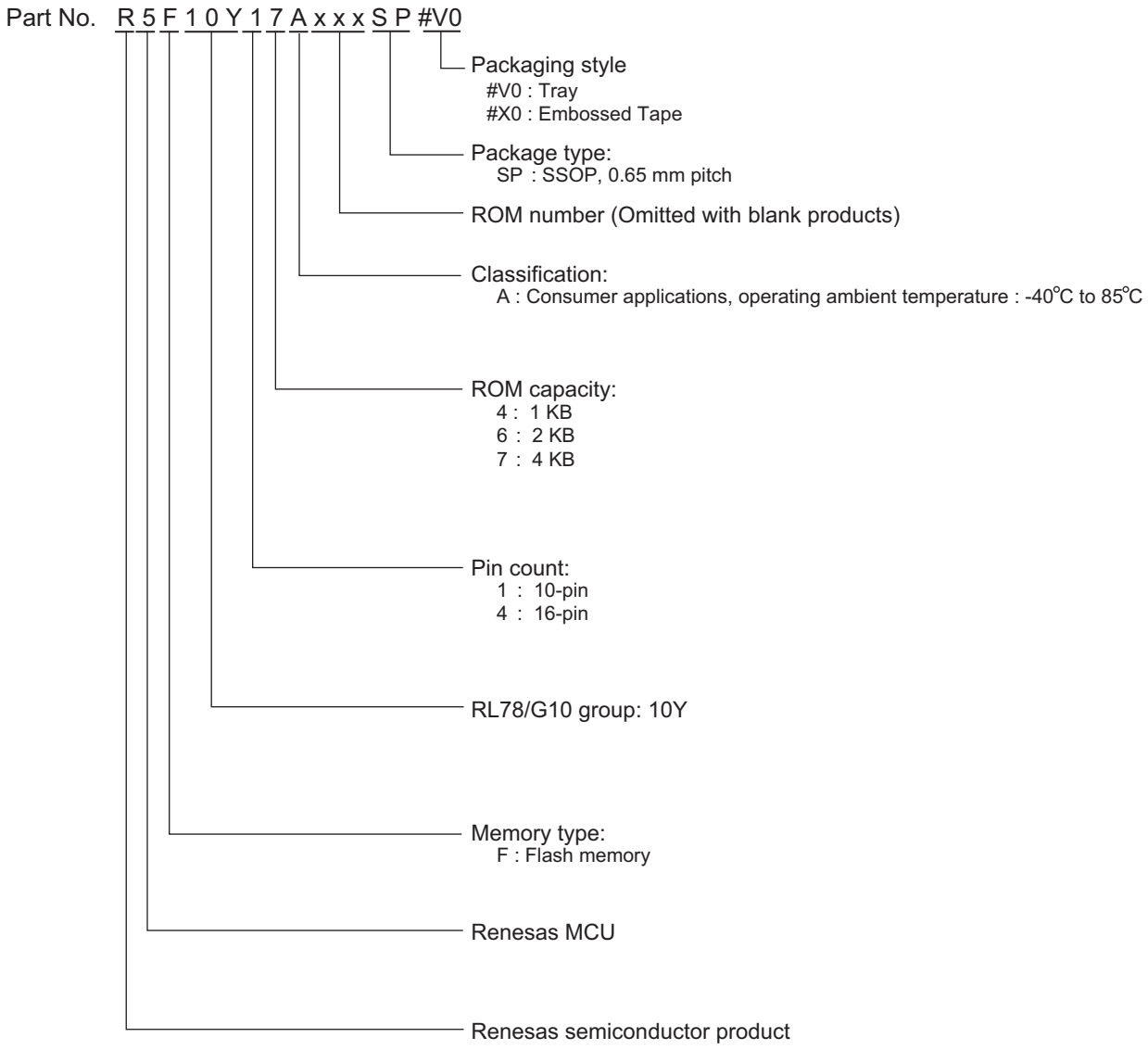
Notes 1. 16-pin products only

2. Under development

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

1.2 List of Part Number

Figure 1-1. Classification of Part Number



Pin count	Package	Part Number
10 pins	10-pin plastic LSSOP (4.4 × 3.6 mm, 0.65mmpitch)	R5F10Y16ASP#V0, R5F10Y16ASP#X0
		R5F10Y14ASP#V0, R5F10Y14ASP#X0
16 pins	16-pin plastic SSOP (4.4 × 5.0 mm, 0.65mmpitch)	R5F10Y47ASP Note
		R5F10Y46ASP Note
		R5F10Y44ASP Note

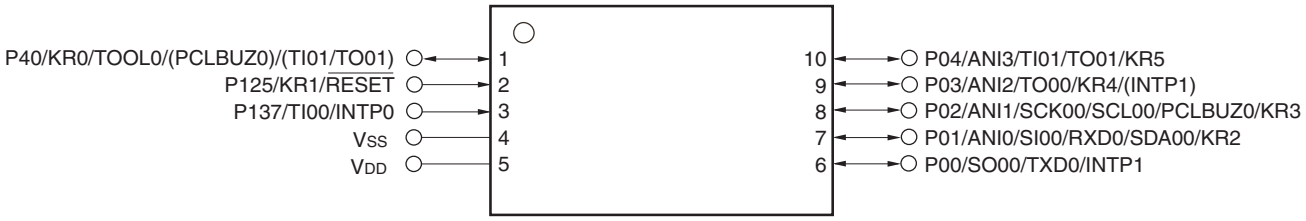
Note Under development

Caution The part number represents the number at the time of publication.
Be sure to review the latest part number through the target product page in the Renesas Electronics Corp.website.

1.3 Pin Configuration (Top View)

1.3.1 10-pin products

- 10-pin plastic LSSOP (4.4 × 3.6)

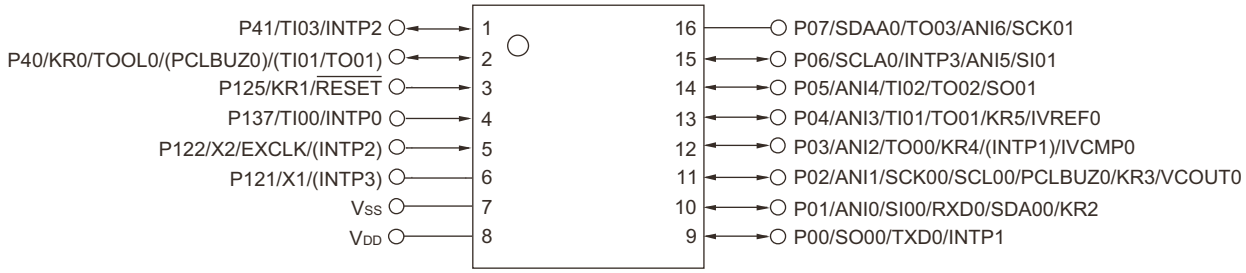


Remarks 1. For pin identification, see **1.4 Pin Identification**.

2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.3.2 16-pin products

- 16-pin plastic SSOP (4.4 × 5.0)



Remarks 1. For pin identification, see **1.4 Pin Identification**.

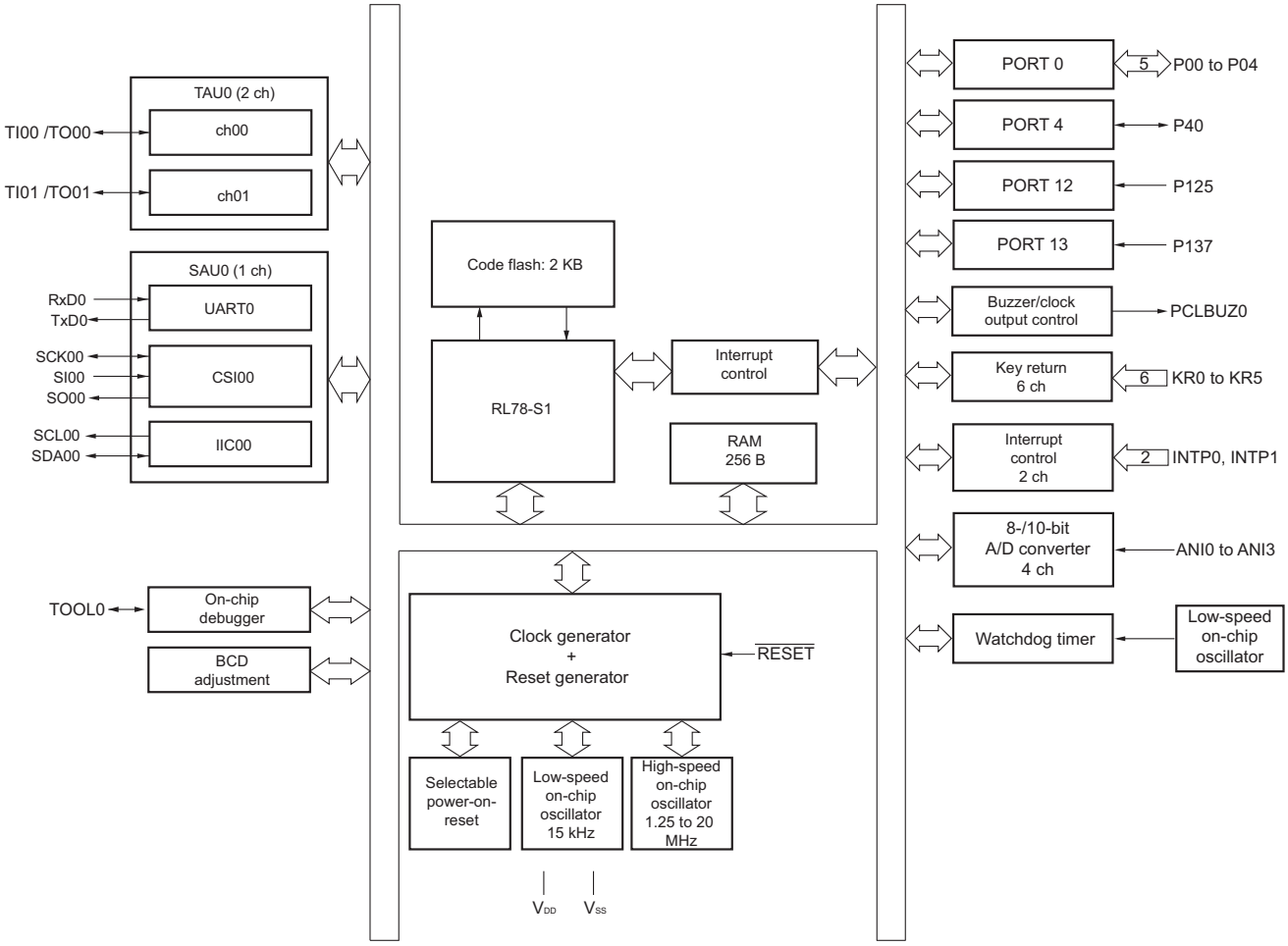
2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

1.4 Pin Identification

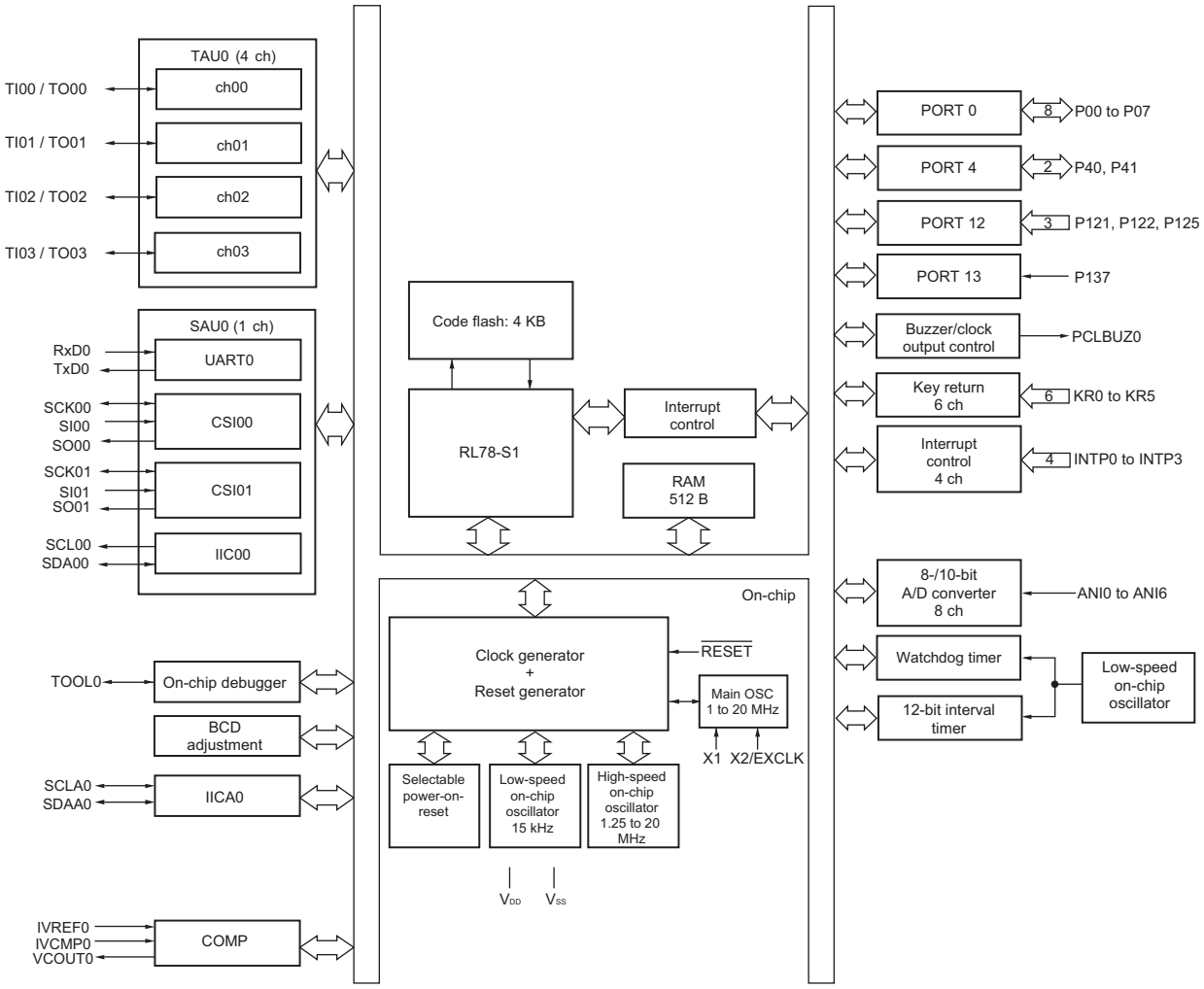
ANI0 to ANI6 : Analog Input
INTP0 to INTP3 : External Interrupt Input
KR0 to KR5 : Key Return
P00 to P07 : Port 0
P40, P41 : Port 4
P121, P122, P125 : Port 12
P137 : Port 13
PCLBUZ0 : Programmable Clock Output/ Buzzer Output
EXCLK : External Clock Input
X1, X2 : Crystal Oscillator
IVCMP0 : Comparator Input
VCOUT0 : Comparator Output
IVREF0 : Comparator Reference Input
$\overline{\text{RESET}}$: Reset
RxD0 : Receive Data
SCK00, SCK01 : Serial Clock Input/Output
SCL00, SCLA0 : Serial Clock Output
SDA00, SDAA0 : Serial Data Input/Output
SI00, SI01 : Serial Data Input
SO00, SO01 : Serial Data Output
TI00 to TI03 : Timer Input
TO00 to TO03 : Timer Output
TOOL0 : Data Input/Output for Tool
TxD0 : Transmit Data
V_{DD} : Power Supply
V_{SS} : Ground

1.5 Block Diagram

1.5.1 10-pin products



1.5.2 16-pin products



1.6 Outline of Functions

This outline describes the function at the time when Peripheral I/O redirection register (PIOR) is set to 00H.

Item		10-pin		16-pin		
		R5F10Y16ASP	R5F10Y14ASP	R5F10Y47ASP	R5F10Y46ASP	R5F10Y44ASP
Code flash memory		2 KB	1 KB	4 KB	2 KB	1 KB
RAM		256 B	128 B	512 B	256 B	128 B
Main system clock	High-speed system clock	—		X1, X2 (crystal/ceramic) oscillation, external main system clock input (EXCLK): 1 to 20 MHz: V_{DD} = 2.7 to 5.5 V 1 to 5 MHz: V_{DD} = 2.0 to 5.5 V		
	High-speed on-chip oscillator clock	• 1.25 to 20 MHz (V_{DD} = 2.7 to 5.5 V) • 1.25 to 5 MHz (V_{DD} = 2.0 to 5.5 V)				
Low-speed on-chip oscillator clock		15 kHz (TYP)				
General-purpose register		8-bit register × 8				
Minimum instruction execution time		0.05 μs (20 MHz operation)				
Instruction set		• Data transfer (8 bits) • Adder and subtractor/logical operation (8 bits) • Multiplication (8 bits × 8 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc.				
I/O port	Total	8		14		
	CMOS I/O	6 (N-ch open-drain output (V_{DD} tolerance): 2)		10 (N-ch open-drain output (V_{DD} tolerance): 4)		
	CMOS input	2		4		
Timer	16-bit timer	2 channels		4 channels		
	Watchdog timer	1 channel				
	12-bit interval timer	—		1 channel		
	Timer output	2 channels (PWM output: 1)		4 channels (PWM outputs: 3[Note 1])		
Clock output/buzzer output		1				
		2.44 kHz to 10 MHz: (Peripheral hardware clock: f_{MAIN} = 20 MHz operation)				
Comparator		—		1		
8-/10-bit resolution A/D converter		4 channels		8 channels		
Serial interface		[10-pin products] CSI: 1 channel/simplified I^2C: 1 channel/UART: 1 channel [16-pin products] CSI: 2 channels/simplified I^2C: 1 channel/UART: 1 channel				
	I^2C bus	—		1 channel		
Vectored interrupt sources	Internal	8		14		
	External	3		5		
Key interrupt		6				
Reset		• Reset by $\overline{\text{RESET}}$ pin • Internal reset by watchdog timer • Internal reset by selectable power-on-reset • Internal reset by illegal instruction execution [Note 2] • Internal reset by data retention lower limit voltage				
Selectable power-on-reset circuit		Detection voltage: 2.0 V/2.4 V/2.7 V/4.0 V				
On-chip debug function		Provided				
Power supply voltage		V_{DD} = 2.0 to 5.5 V				
Operating ambient temperature		T_A = - 40 to + 85 °C				

Notes 1. The number of outputs varies, depending on the setting of channels in use and the number of the master (see **6.8.3 Operation as multiple PWM output function in the RL78/G10 User's Manual**).

2. The illegal instruction is generated when instruction code FFH is executed. Reset by the illegal instruction execution not issued by emulation with the on-chip debug emulator.

2. ELECTRICAL SPECIFICATIONS

Cautions 1. This chapter explains the electrical specifications of two products, the R5F10Y16ASP and the R5F10Y14ASP.

2. Electrical specifications for the 16-pin products are T. B. D. because these products are under development.

3. The RL78/G10 has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production, because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

4. The pins mounted depend on the product. Refer to 2.1 Port Functions and 2.2.1 Functions for each product in the RL78/G10 User's Manual.

2.1 Absolute Maximum Ratings

(T_A = 25°C)

Parameter	Symbols	Conditions		Ratings	Unit
Supply Voltage	V_{DD}			−0.5 to +6.5	V
Input Voltage	V_{I1}			−0.3 to V_{DD} + 0.3[Note]	V
Output Voltage	V_{O1}			−0.3 to V_{DD} + 0.3	V
Output current, high	I_{OH1}	Per pin		−40	mA
		Total of all pins -140 mA	P40	−40	mA
			P00 to P04	−100	mA
Output current, low	I_{OL1}	Per pin		40	mA
		Total of all pins 140 mA	P40	40	mA
			P00 to P04	100	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C

Note Must be 6.5 V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remarks 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

2. The reference voltage is V_{SS}.

2.2 Oscillator Characteristics

2.2.1 On-chip oscillator characteristics

(T_A = −40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Oscillators	Parameters	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator oscillation clock frequency [Notes 1, 2]	f_{IH}		1.25		20	MHz
High-speed on-chip oscillator oscillation clock frequency accuracy		T_A = -20 to +85°C	-2.0		+2.0	%
		T_A = -40 to -20°C	-3.0		+3.0	%
Low-speed on-chip oscillator oscillation clock frequency [Note 3]	f_{IL}			15		kHz
Low-speed on-chip oscillator oscillation clock frequency accuracy			-15		+15	%

Notes 1. High-speed on-chip oscillator frequency is selected by bits 0 to 2 of option byte (000C2H).

2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

3. This only indicates the oscillator characteristics.

2.3 DC Characteristics

2.3.1 Pin characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions			MIN.	TYP.	MAX.	Unit
Output current, high[Note 1]	I_{OH1}	P00, P01, P02 to P04, P40	Per pin				-10.0[Note 2]	mA
		P40	Total[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			-10.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			-2.0	mA
				2.0 V ≤ V_{DD} < 2.7 V			-1.5	mA
		P00, P01, P02 to P04	Total[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			-50.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			-10.0	mA
				2.0 V ≤ V_{DD} < 2.7 V			-7.5	mA
		Total of all pins[Note 3]					-60.0	mA
Output current, low[Note 4]	I_{OL1}	P00 to P04, P40	Per pin				20.0[Note 2]	mA
		P40	Total[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			20.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			3.0	mA
				2.0 V ≤ V_{DD} < 2.7 V			0.6	mA
		P00 to P04	Total[Note 3]	4.0 V ≤ V_{DD} ≤ 5.5 V			80.0	mA
				2.7 V ≤ V_{DD} < 4.0 V			12.0	mA
				2.0 V ≤ V_{DD} < 2.7 V			2.4	mA
		Total of all pins[Note 3]					100.0	mA
Input voltage, high	V_{IH1}				0.8 V_{DD}		V_{DD}	V
Input voltage, low	V_{IL1}				0		0.2 V_{DD}	V
Output voltage, high[Note 5]	V_{OH1}	4.0 V ≤ V_{DD} ≤ 5.5 V		I_{OH} = -10 mA	V_{DD}-1.5			V
				I_{OH} = -3.0 mA	V_{DD}-0.7			V
		2.7 V ≤ V_{DD} ≤ 5.5 V		I_{OH} = -2.0 mA	V_{DD}-0.6			V
		2.0 V ≤ V_{DD} ≤ 5.5 V		I_{OH} = -1.5 mA	V_{DD}-0.5			V
Output voltage, low[Note 6]	V_{OL1}	4.0 V ≤ V_{DD} ≤ 5.5 V		I_{OL} = 20 mA			1.3	V
				I_{OL} = 8.5 mA			0.7	V
		2.7 V ≤ V_{DD} ≤ 5.5 V		I_{OL} = 3.0 mA			0.6	V
				I_{OL} = 1.5 mA			0.4	V
		2.0 V ≤ V_{DD} ≤ 5.5 V		I_{OL} = 0.6 mA			0.4	V
Input leakage current, high	I_{LIH1}	V_I = V_{DD}					1	μA
Input leakage current,low	I_{LIL1}	V_I = V_{SS}					-1	μA
On-chip pull-up resistance	R_U	V_I = V_{SS}			10	20	100	kΩ

Notes 1. Value of current at which the device operation is guaranteed even if the current flows from the V_{DD} pin to an output pin.

2. Do not exceed the total current value.

3. This is the output current value under conditions where the duty factor ≤ 70%.
The output current value when the duty factor > 70% can be calculated with the following expression (when changing the duty factor to n%).

- Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)
  <Example> Where n = 80 % and I_{OH} = - 10.0 mA
  Total output current of pins = (- 10.0 × 0.7)/(80 × 0.01) ≅ - 8.7 mA
- Total output current of pins = (I_{OL} × 0.7)/(n × 0.01)
  <Example> Where n = 80 % and I_{OL} = 10.0 mA
  Total output current of pins = (10.0 × 0.7)/(80 × 0.01) ≅ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor. A current higher than the absolute maximum rating must not flow into one pin.

4. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the V_{SS} pin.
5. The value under the condition which satisfies the high-level output current (I_{OH1}).
6. The value under the condition which satisfies the low-level output current (I_{OL1}).

Cautions 1. P00 and P01 do not output high level in N-ch open-drain mode.
2. The maximum value of V_{IH} of P00 and P01 is V_{DD} even in N-ch open-drain mode.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port.

2.3.2 Supply current characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions				MIN.	TYP.	MAX.	Unit
Supply current Note 1	I_{DD1}	Operating mode	Basic operation	f_{IH} = 20 MHz	V_{DD} = 3.0 V, 5.0 V		0.91		mA
			Normal operation	f_{IH} = 20 MHz	V_{DD} = 3.0 V, 5.0 V		1.57	2.04	
				f_{IH} = 5 MHz	V_{DD} = 3.0 V, 5.0 V		0.85	1.15	
	I_{DD2} Note 2	HALT mode		f_{IH} = 20 MHz	V_{DD} = 3.0 V, 5.0 V		350	820	µA
				f_{IH} = 5 MHz	V_{DD} = 3.0 V, 5.0 V		290	600	
	I_{DD3} Note 3	STOP mode		V_{DD} = 3.0 V			0.56	2.00	µA
WDT supply current Note 4	I_{WDT}	f_{IL} = 15 kHz					0.31		µA
ADC supply current Note 5	I_{ADC}	During conversion at the highest speed		V_{DD} = 5.0 V			1.30	1.90	mA
				V_{DD} = 3.0 V			0.50		

Notes 1. Total current flowing into V_{DD}, including the input leakage current flowing when the level of the input pin is fixed to V_{DD} or V_{SS}. The values below the MAX. column include the peripheral operation current. However, not including the current flowing into the watchdog timer, A/D converter, I/O port, and on-chip pull-up/pull-down resistors.

2. During HALT instruction execution by flash memory.

3. When the high-speed on-chip oscillator is stopped.

4. Current flowing only to the watchdog timer (including the operating current of the low-speed on-chip oscillator). The current value of the RL78 microcontrollers is the sum of I_{DD1}, I_{DD2} or I_{DD3} and I_{WDT} when the watchdog timer operates.

5. Current flowing only to the A/D converter. The current value of the RL78 microcontrollers is the sum of I_{DD1} or I_{DD2} and I_{ADC} when the A/D converter operates in an operation mode or the HALT mode.

Remarks 1. f_{IL}: Low-speed on-chip oscillator clock frequency

2. f_{IH}: High-speed on-chip oscillator clock frequency

3. Temperature condition of the TYP. value is T_A = 25°C

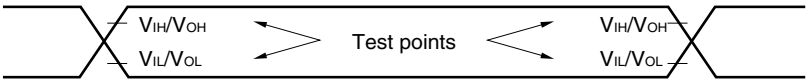
2.4 AC Characteristics

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

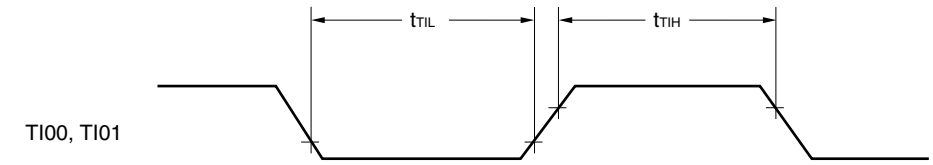
Items	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	2.7 V ≤ V_{DD} ≤ 5.5 V	0.05		0.8	μs
			2.0 V ≤ V_{DD} ≤ 5.5 V	0.2		0.8	μs
TI00, TI01 input high-level width, low-level width	t_{TIH}, t_{TIL}	Noise filter is not used		1/f_{MCK} + 10			ns
TO00, TO01 output frequency	f_{TO}	4.0 V ≤ V_{DD} ≤ 5.5 V				10	MHz
		2.7 V ≤ V_{DD} < 4.0 V				5	MHz
		2.0 V ≤ V_{DD} < 2.7 V				2.5	MHz
PCLBUZ0 output frequency	f_{PCL}	4.0 V ≤ V_{DD} ≤ 5.5 V				10	MHz
		2.7 V ≤ V_{DD} < 4.0 V				5	MHz
		2.0 V ≤ V_{DD} < 2.7 V				2.5	MHz
$\overline{\text{RESET}}$ low-level width	t_{RSL}			10			μs

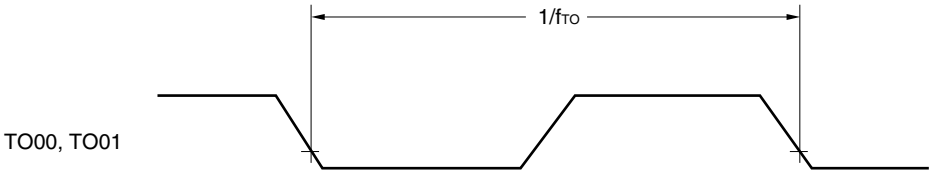
Remark f_{MCK}: Timer array unit operation clock frequency

AC Timing Test Points

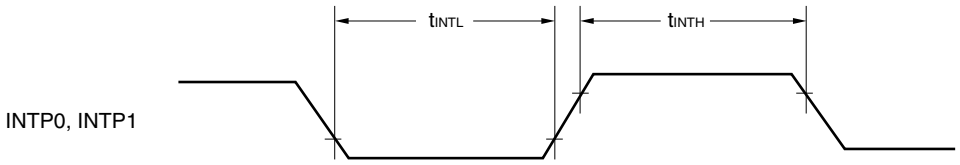


TI/TO Timing

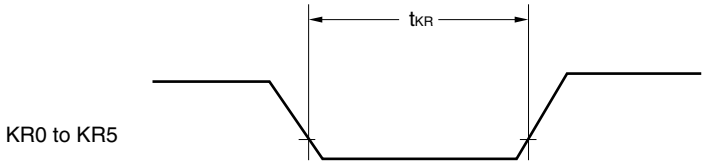




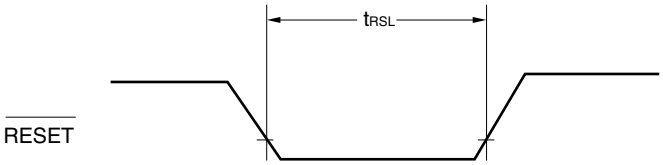
Interrupt Request Input Timing



Key Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



2.5 Serial Communication Characteristics

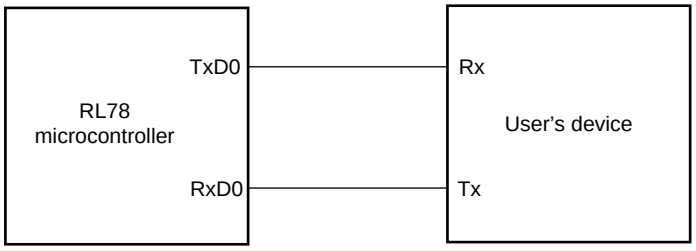
2.5.1 Serial array unit

(1) UART mode

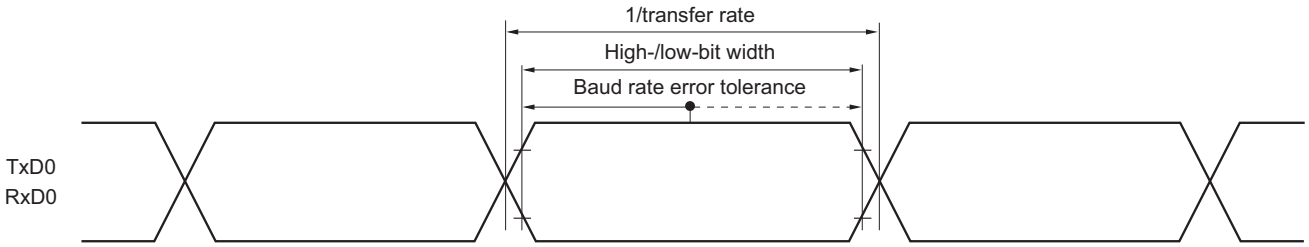
(T_A = −40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate					f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate f_{CLK} = f_{MCK} = 20 MHz			3.3	Mbps

UART mode connection diagram



UART mode bit width (reference)



Remark f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

(2) CSI mode (master mode, SCKp... internal clock output)

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	2.7 V ≤ V_{DD} ≤ 5.5 V	200			ns
			2.0 V ≤ V_{DD} ≤ 5.5 V	800			ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}	2.7 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2-18			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY1}/2-50			ns
SIp setup time (to SCKp↑) Note 1	t_{SIK1}	2.7 V ≤ V_{DD} ≤ 5.5 V		47			ns
		2.0 V ≤ V_{DD} ≤ 5.5 V		110			ns
SIp hold time (from SCKp↑) Note 2	t_{KSI1}			19			ns
Delay time from SCKp↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4				25	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes “to SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SCKp and SOp output lines.

Remarks 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

(3) CSI mode (slave mode, SCKp... external clock input)

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
SCKp cycle time	t_{KCY2}	2.7 V ≤ V_{DD} ≤ 5.5 V	f_{MCK} = 20 MHz	8/f_{MCK}			ns
			f_{MCK} ≤ 10 MHz	6/f_{MCK}			ns
		2.0 V ≤ V_{DD} < 2.7 V		6/f_{MCK}			ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}	2.0 V ≤ V_{DD} ≤ 5.5 V		t_{KCY2}/2			ns
SIp setup time (to SCKp↑)[Note 1]	t_{SIK2}	2.7 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 20			ns
		2.0 V ≤ V_{DD} < 2.7 V		1/f_{MCK} + 30			ns
SIp hold time (from SCKp↑) [Note 2]	t_{KSI2}	2.0 V ≤ V_{DD} ≤ 5.5 V		1/f_{MCK} + 31			ns
Delay time from SCKp↓ to SOp output [Note 3]	t_{KSO2}	C = 30 pF [Note 4]	2.7 V ≤ V_{DD} ≤ 5.5 V			2/f_{MCK} + 50	ns
			2.0 V ≤ V_{DD} < 2.7 V			2/f_{MCK} + 110	ns

Notes 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp setup time becomes "to SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The SIp hold time becomes "from SCKp↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

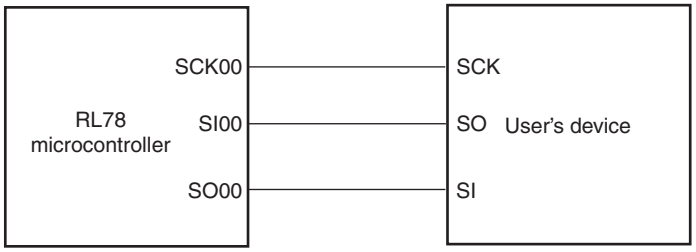
3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes "from SCKp↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

4. C is the load capacitance of the SOp output lines.

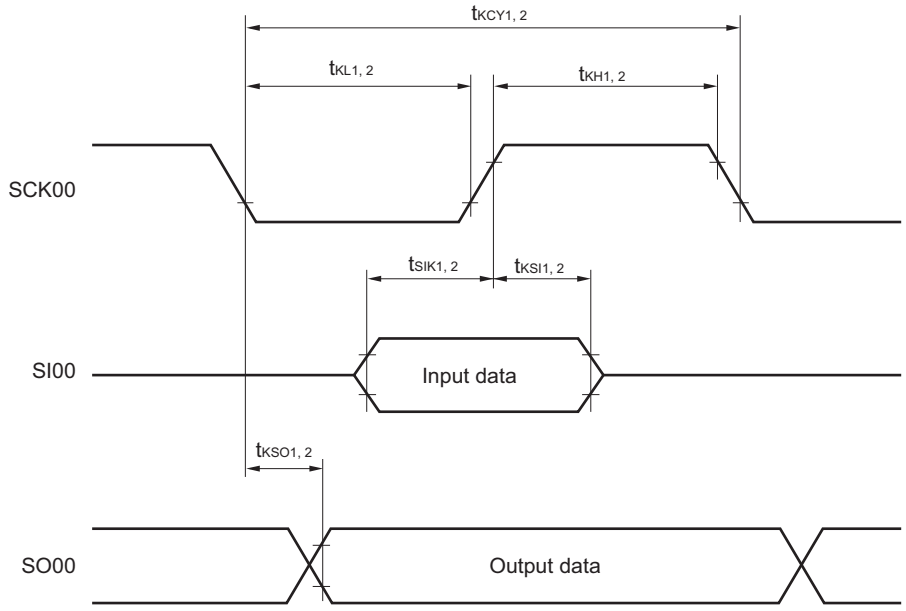
Remarks 1. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0)

2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00))

CSI mode connection diagram



CSI mode serial transfer timing
(When DAP00 = 0 and CKP00 = 0, or DAP00 = 1 and CKP00 = 1.)



(4) Simplified I²C mode

(T_A = –40 to +85°C, 2.0 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
SCLr clock frequency	f_{SCL}	2.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ		400 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	2.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		ns
Hold time when SCLr = "H"	t_{HIGH}	2.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1150		ns
Data setup time (reception)	$t_{SU:DAT}$	2.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	1/f_{MCK} + 145 Note 2		ns
Data hold time (transmission)	$t_{HD:DAT}$	2.0 V ≤ V_{DD} ≤ 5.5 V, C_b = 100 pF, R_b = 3 kΩ	0	355	ns

Notes 1. The value must also be equal to or less than f_{MCK}/4.

2. Set the f_{MCK} value to keep the hold time of SCLr = "L" and SCLr = "H".

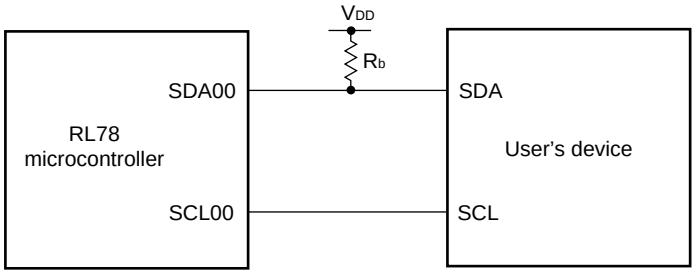
Caution Select the N-ch open drain output (V_{DD} tolerance) mode for the SDAr pin by using the port output mode register 0 (POM0).

Remarks 1. R_b [Ω]: Communication line (SDAr) pull-up resistance, C_b [F]: Communication line (SCLr, SDAr) load capacitance

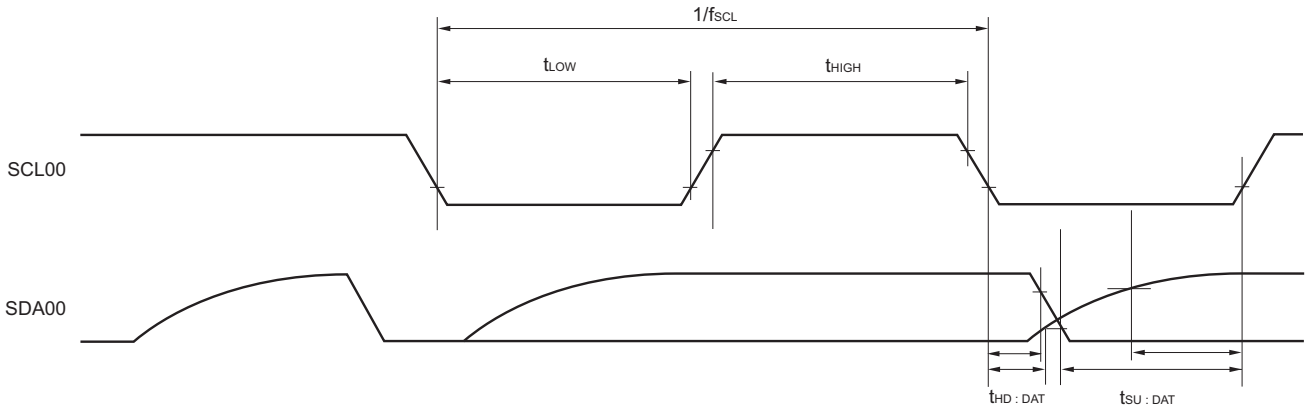
2. r: IIC number (r = 00)

3. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 00))

Simplified I²C mode connection diagram



Simplified I²C mode serial transfer timing



2.6 Analog Characteristics

2.6.1 A/D converter characteristics

(Target ANI pin : ANI0 to ANI3)

(T_A = –40 to +85°C, 2.4 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution	R_{ES}			8		10	bit
Overall error[Note 1]	AINL	10-bit resolution	V_{DD} = 5 V		±1.7	±3.1[Note 2]	LSB
			V_{DD} = 3 V		±2.3	±4.5[Note 2]	LSB
Conversion time	t_{CONV}	10-bit resolution	2.7 V ≤ V_{DD} ≤ 5.5 V	3.4		18.4	µs
			2.4 V ≤ V_{DD} ≤ 5.5 V	4.6		18.4	µs
Zero-scale error[Note 1]	E_{ZS}	10-bit resolution	V_{DD} = 5 V			±0.19[Note 2]	%FSR
			V_{DD} = 3 V			±0.39[Note 2]	%FSR
Full-scale error[Note 1]	E_{FS}	10-bit resolution	V_{DD} = 5 V			±0.29[Note 2]	%FSR
			V_{DD} = 3 V			±0.42[Note 2]	%FSR
Integral linearity error[Note 1]	ILE	10-bit resolution	V_{DD} = 5 V			±1.8[Note 2]	LSB
			V_{DD} = 3 V			±1.7[Note 2]	LSB
Differential linearity error[Note 1]	DLE	10-bit resolution	V_{DD} = 5 V			±1.4[Note 2]	LSB
			V_{DD} = 3 V			±1.5[Note 2]	LSB
Analog input voltage	V_{AIN}			0		V_{DD}	V

Notes 1. Excludes quantization error (±1/2 LSB).

2. This is the characteristic evaluation value plus or minus 3. These values are not used in the shipping inspection.

2.6.2 SPOR circuit characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Detection supply voltage	V_{SPOR0}	Power supply rise time	4.08	4.28	4.45	V
		Power supply fall time	4.00	4.20	4.37	V
	V_{SPOR1}	Power supply rise time	2.76	2.90	3.02	V
		Power supply fall time	2.70	2.84	2.96	V
	V_{SPOR2}	Power supply rise time	2.44	2.57	2.68	V
		Power supply fall time	2.40	2.52	2.62	V
	V_{SPOR3}	Power supply rise time	2.05	2.16	2.25	V
		Power supply fall time	2.00	2.11	2.20	V
Minimum pulse width[Note]	T_{SPW}		300			µs

Note Time required for the reset operation by the SPOR when V_{DD} becomes under V_{SPDR}.

2.6.3 Power supply voltage rising slope characteristics

(T_A = –40 to +85°C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply voltage rising slope	S_{VDD}				54	V/ms

2.6.4 Data retention power supply voltage characteristics

(T_A = –40 to +85°C, Vss = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention power supply voltage range	V_{DDDR}		1.9		5.5	V

Caution Data is retained until the power supply voltage becomes under the minimum value of the data retention power supply voltage range. Note that data in the RAM and RESF registers might not be cleared even if the power supply voltage becomes under the minimum value of the data retention power supply voltage range.

2.7 Flash Memory Programming Characteristics

(T_A = 0 to + 40°C, 4.5 V ≤ V_{DD} ≤ 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Code flash memory rewritable times Notes 1, 2, 3	C_{erwr}	Retained for 20 years.	T_A = + 85°C	1000			Times

Notes 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

2. When using flash memory programmer.

3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

2.8 Dedicated Flash Memory Programmer Communication (UART)

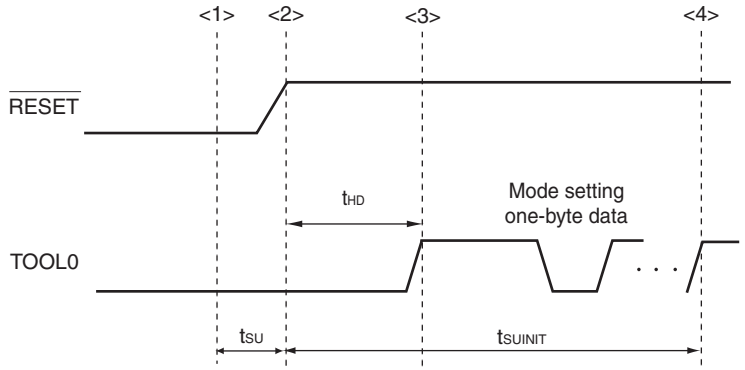
(T_A = 0 to + 40°C, 4.5 V ≤ V_{DD} ≤ 5.5V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate				115,200		bps

Remark The transfer rate during flash memory programming is fixed to 115,200 bps.

2.9 Timing of Entry to Flash Memory Programming Modes

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	SPOR reset must end before the external reset ends.			100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset ends	t_{SU}	SPOR reset must end before the external reset ends.	10			μs
How long the TOOL0 pin must be kept at the low level after an external reset ends	t_{HD}	SPOR reset must end before the external reset ends.	1			ms



<1> The low level is input to the TOOL0 pin.
<2> The external reset ends (SPOR reset must end before the external reset ends.).
<3> The TOOL0 pin is set to the high level.
<4> Setting of entry to the flash memory programming mode by UART reception.

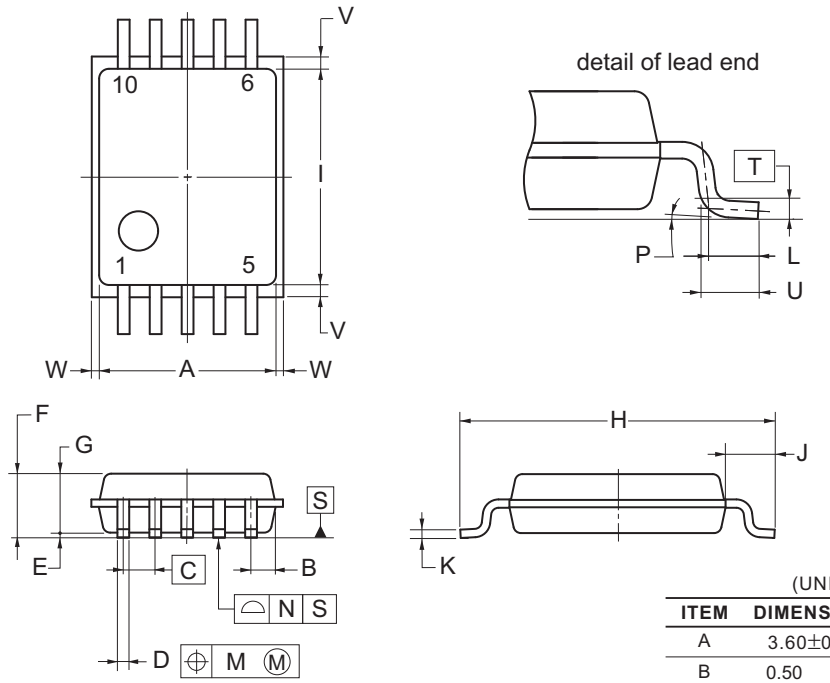
Remark t_{SUINIT}: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the resets end.
t_{SU}: How long from when the TOOL0 pin is placed at the low level until an external reset ends (MIN. 10 μs)
t_{HD}: How long to keep the TOOL0 pin at the low level from when the external reset ends

3. PACKAGE DRAWINGS

3.1 10-pin products

R5F10Y16ASP, R5F10Y14ASP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP10-4.4x3.6-0.65	PLSP0010JA-A	P10MA-65-CAC-2	0.05



(UNIT:mm)

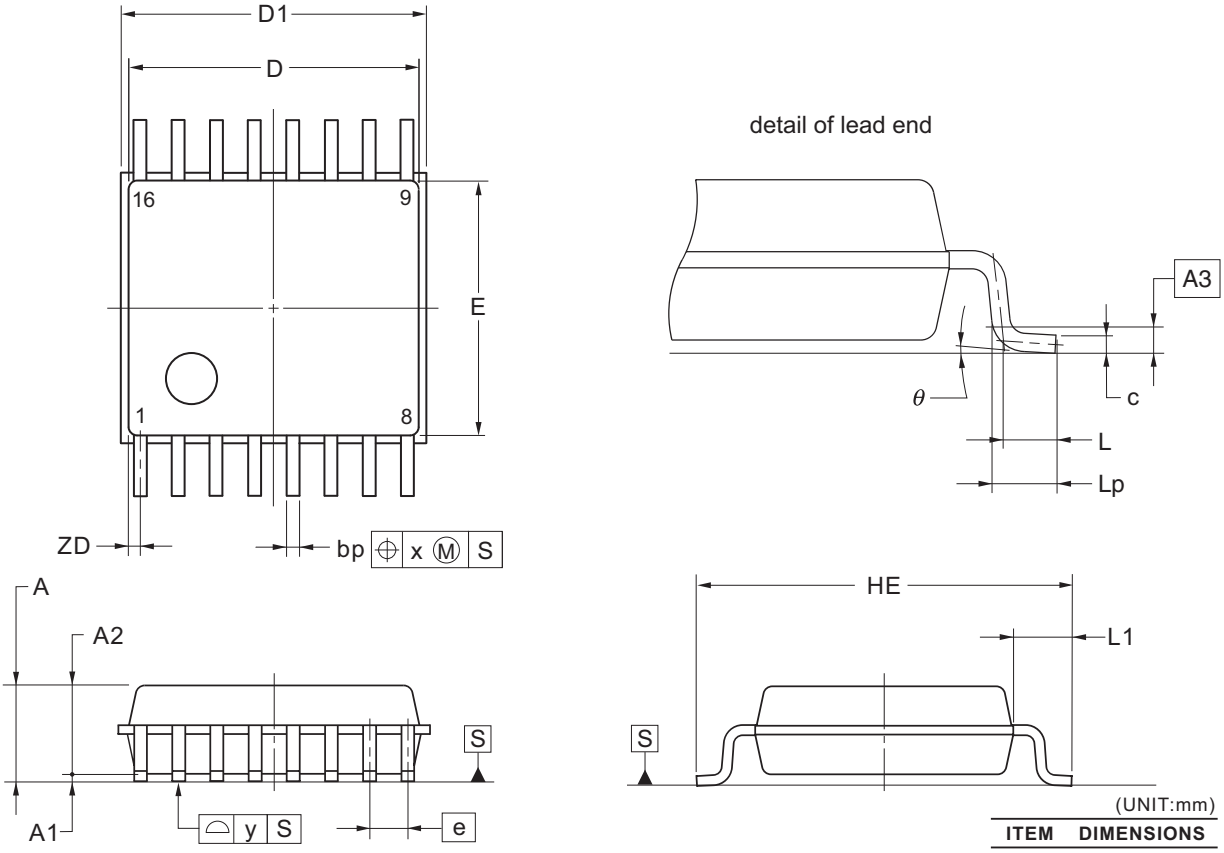
ITEM	DIMENSIONS
A	3.60±0.10
B	0.50
C	0.65 (T.P.)
D	0.24±0.08
E	0.10±0.05
F	1.45 MAX.
G	1.20±0.10
H	6.40±0.20
I	4.40±0.10
J	1.00±0.20
K	$0.17^{+0.08}_{-0.07}$
L	0.50
M	0.13
N	0.10
P	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
T	0.25 (T.P.)
U	0.60±0.15
V	0.25 MAX.
W	0.15 MAX.

NOTE
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

3.2 16-pin products

R5F10Y47ASP, R5F10Y46ASP, R5F10Y44ASP

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-SSOP16-4.4x5-0.65	PRSP0016JC-A	P16MA-65-FAA-2	0.08



(UNIT:mm)

ITEM	DIMENSIONS
D	5.00±0.15
D1	5.20±0.15
E	4.40±0.20
HE	6.40±0.20
A	1.725 MAX.
A1	0.125±0.05
A2	1.50
A3	0.25
e	0.65
bp	$0.22^{+0.08}_{-0.07}$
c	$0.15^{+0.03}_{-0.04}$
L	0.50
Lp	0.60±0.10
L1	1.00±0.20
x	0.13
y	0.10
θ	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
ZD	0.325

Revision History	RL78/G10 Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Apr 15, 2013	-	First Edition issued

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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