

RX66T Group Renesas MCUs

R01DS0315EJ0110

Rev.1.10

Feb 08, 2019

160-MHz, 32-bit RX MCU, on-chip FPU, 928 CoreMark, Supportive of 5V power supply, up to 1-MB flash memory, up to 128-KB SRAM, 32-KB data flash memory, 16-KB SRAM with ECC, Simultaneous sampling with 3 units of 12-bit A/D converter (up to 7 channels), Single-end/pseudo differential input supportive amplifier (6 channels), Analog comparator (6 channels), 160 MHz PWM (4 channels for 3-phase complementary, 2 channels for 5-phase complementary, 10 channels for single-phase complementary), 4-channel high-resolution PWM with resolution of 195 ps at the minimum, Host/function or OTG controller with full-speed USB 2.0 transfer, CAN, Encryption functions (optional)

Features

■ 32-bit RXv3 CPU core

- Maximum operating frequency: 160 MHz
Capable of 928 CoreMark in operation at 160 MHz
- JTAG and FINE (one-line) debugging interfaces

■ Low-power design and architecture

- Operation from a single 2.7- to 5.5-V supply
- Four low-power modes

■ On-chip code flash memory

- Supports versions with 1 Mbytes/512 Kbytes/256 Kbytes
- No wait cycles at up to 120 MHz or when the ROM cache is hit
- User code is programmable by on-board or off-board programming.

■ On-chip data flash memory

- 32 Kbytes, reprogrammable up to 100,000 times
- Programming/erasing as background operations (BGOs)

■ On-chip SRAM, no wait states

- 128K/64 Kbytes of SRAM (no wait states)
- 16 Kbytes of RAM with ECC (with wait)

■ Data transfer

- DMAcA: 8 channels
- DTCa: 1 channel

■ ELC

- Module operation can be initiated by event signals without using interrupts
- Linked operation between modules is possible when the CPU is in sleep mode

■ Reset and supply management

- Power-on reset (POR)
- Low voltage detection (LVDA) with voltage settings

■ Clock functions

- Frequency of resonator for main clock oscillator: 8 to 24 MHz (this can be used as the PLL reference clock)
- High-speed on-chip oscillator: 16 MHz/18 MHz/20 MHz (this can be used as the PLL reference clock)
- Low-speed on-chip oscillator: 240 kHz

■ Independent watchdog timer

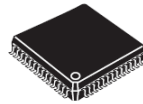
- 120-kHz IWDt-dedicated on-chip oscillator clock operation

■ Useful functions for IEC60730 compliance

- Oscillation-stoppage detection, functions for self-diagnosis and detection of disconnection for the A/D converter, clock frequency accuracy measurement circuit, independent watchdog timer, RAM test-assisting function by DOC, and CRCA, etc.
- Register write protection function can protect values in important registers against overwriting.

■ External bus

- Bus clock at 40 MHz (max)
- Four CS areas
- 8- or 16-bit bus space is selectable per area



PLQP0144KA-B 20 × 20 mm, 0.5 mm pitch
 PLQP0112JA-B 20 × 20 mm, 0.65 mm pitch
 PLQP0100KB-B 14 × 14 mm, 0.5 mm pitch
 PLQP0080JA-A 14 × 14 mm, 0.65 mm pitch
 PLQP0080KB-B 12 × 12 mm, 0.5 mm pitch
 PLQP0064KB-B 10 × 10 mm, 0.5 mm pitch

■ Various communications interfaces

- Host/function or OTG controller (1 channel) with full-speed USB 2.0 (USBb) transfer
- CAN (compliant with ISO11898-1), incorporating 32 mailboxes (1 channel)
- SCIj and SCiH with multiple functionalities (up to 6 channels)
Choose from among asynchronous mode, clock-synchronous mode, smart-card interface mode, simplified SPI, simplified I²C, and extended serial mode.
- SCiI with 16-byte transmission and reception FIFOs (1 channel)
- I²C bus interface (RIICa) for transfer at up to 400 kbps (fast mode), capable of SMBus operation (1 channel)
- RSPiD (1 channel) for transfer at up to 30 Mbps

■ Up to 31 extended-function timers

- 32-bit GPTW (10 channels): operation at 160 MHz, input capture, output compare, PWM waveforms: 10 output channels in single-phase complementary PWM mode/3 output channels in 3-phase complementary PWM mode/2 output channels in 5-phase complementary PWM mode, phase-counting mode, linkage with comparator (counting operation, PWM negate control)
- 16-bit MTU3d (9 channels): operation at 160 MHz, input capture, output compare, PWM waveforms: 2 output channels in 3-phase complementary PWM mode, phase-counting mode
- 8-bit TMR (8 channels)
- 16-bit CMT (4 channels)

■ High-resolution PWM waveform generation circuit (HRPWM): 4 channels

- Controlling the timing of rising or falling of the PWM output waveform for 32-bit GPTW is realized with minimum of 195 ps resolution (in operation at 160 MHz)

■ 12-bit A/D converter (S12ADH): total of 30 channels for three units

- Up to three 12-bit units of sample-and-hold circuit included
Unit 0 (8 channels for 3 sample-and-hold circuits),
Unit 1 (8 channels for 3 sample-and-hold circuits),
Unit 2 (14 channels)
- Programmable gain amplifier with pseudo differential amplification (3 channels × 2)

■ Analog Comparator (CMPC): 6 channels

■ 12-bit D/A converter: 2 channels

- Usable as a reference voltage for the analog comparator

■ Temperature sensor for measuring temperature within the chip

■ Encryption functions (Trusted Secure IP Lite)

- 128- or 256-bit key length of AES for ECB, CBC, GCM, others
- True random number generator
- Unauthorized access to the encryption engine is disabled and imposture and falsification of information are prevented
- Safe management of keys

■ Up to 110 pins for general I/O ports

- 5-V tolerance, open drain, input pull-up, switchable driving ability

■ Recommended operating temp. range (Topr)

- -40°C to +85°C
- -40°C to +105°C

1. Overview

1.1 Outline of Specifications

Table 1.1 lists the specifications in outline, and Table 1.2 gives a comparison of the functions of products in different packages.

Table 1.1 shows the outline of maximum specifications, and the number of peripheral module channels differs depending on the pin number on the package and the code flash memory capacity. For details, see Table 1.2, Comparison of Functions for Different Packages.

Table 1.1 Outline of Specifications (1/9)

| Classification | Module/Function | Description |
|----------------|-------------------|---|
| CPU | CPU | <ul style="list-style-type: none"> Maximum operating frequency: 160 MHz 32-bit RX CPU (RXv3) Minimum instruction execution time: One instruction per state (cycle of the system clock) Address space: 4-Gbyte linear Register set of the CPU <ul style="list-style-type: none"> General purpose: Sixteen 32-bit registers Control: Ten 32-bit registers Accumulator: Two 72-bit registers 111 instructions <ul style="list-style-type: none"> Standard provided instructions: 111 <ul style="list-style-type: none"> Basic instructions: 77 Single precision floating point instructions: 11 DSP instructions: 23 Addressing modes: 11 Data arrangement <ul style="list-style-type: none"> Instructions: Little endian Data: Selectable as little endian or big endian On-chip 32-bit multiplier: 32 × 32 → 64 bits On-chip divider: 32/32 → 32 bits Barrel shifter: 32 bits |
| | FPU | <ul style="list-style-type: none"> Single-precision (32-bit) floating-point number Data types and floating-point exceptions in conformance with the IEEE754 standard |
| Memory | Code flash memory | <ul style="list-style-type: none"> Capacity: 1 Mbyte, 512 Kbytes, 256 Kbytes ROM cache: Operation of an 8-Kbyte instruction fetching cache can be enabled or disabled (this is disabled by default). <ul style="list-style-type: none"> While ROM cache operation is enabled: <ul style="list-style-type: none"> - when the cache is hit, one-cycle access up to 160 MHz - when the cache is missed: <ul style="list-style-type: none"> one to two cycles if ICLK ≤ 120 MHz (bus wait: 0 cycles), two to three cycles if ICLK > 120 MHz (bus wait: 1 cycle). While ROM cache operation is disabled: <ul style="list-style-type: none"> one cycle if ICLK ≤ 120 MHz (bus wait: 0 cycles), two cycles if ICLK > 120 MHz (bus wait: 1 cycle). On-board programming: Five types Off-board programming (parallel programmer mode) (This is not available for 80/64-pin products) The trusted memory (TM) function protects against the reading of programs from blocks 8 and 9. |
| | Data flash memory | <ul style="list-style-type: none"> Capacity: 32 Kbytes Programming/erasing: 100,000 times |
| | Unique ID | <ul style="list-style-type: none"> 12-byte unique ID for the device |
| | RAM | <ul style="list-style-type: none"> Capacity: 128 Kbytes, 64 Kbytes 160 MHz No-wait access SED (single error detection) |
| | RAM with ECC | <ul style="list-style-type: none"> Capacity: 16 Kbytes 00FF C000h to 00FF FFFFh (16 Kbytes) SEC-DED (single error correction/double error detection) |

Table 1.1 Outline of Specifications (2/9)

| Classification | Module/Function | Description |
|----------------------------------|--------------------------|---|
| Operating modes | | <ul style="list-style-type: none"> Operating modes by the mode-setting pins at the time of release from the reset state <ul style="list-style-type: none"> Single-chip mode Boot mode (SCI interface) Boot mode (USB interface) Boot mode (FINE interface) User boot mode Selection of operating mode by register setting <ul style="list-style-type: none"> Single-chip mode, user boot mode, On-chip ROM disabled extended mode, On-chip ROM enabled extended mode Endian selectable |
| Clock | Clock generation circuit | <ul style="list-style-type: none"> Main clock oscillator, low-speed/high-speed on-chip oscillator, PLL frequency synthesizer, and IWDG-dedicated on-chip oscillator The peripheral module clocks can be set to frequencies above that of the system clock. Main-clock oscillation stoppage detection Separate frequency-division and multiplication settings for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, PCLKD), flash-IF clock (FCLK) and external bus clock (BCLK) The CPU and other bus masters run in synchronization with the system clock (ICLK): Up to 160 MHz Peripheral modules of MTU3 (Internal peripheral bus), GPTW (Internal peripheral bus), HRPWM (Internal peripheral bus), RSPI, and SCI11 run in synchronization with PCLKA, which operates at up to 120 MHz. Other peripheral modules run in synchronization with PCLKB: Up to 60 MHz MTU3 (counter reference clocks), GPTW (counter reference clocks), and HRPWM (reference clocks) are synchronized with PCLKC: Up to 160 MHz ADCLK in the S12AD runs in synchronization with PCLKD: Up to 60 MHz Flash IF run in synchronization with the flash-IF clock (FCLK): Up to 60 MHz Devices connected to the external bus run in synchronization with the external bus clock (BCLK): Up to 40 MHz Multiplication is possible with using the high-speed on-chip oscillator (HOCO) as a reference clock of the PLL circuit |
| Reset | | <p>Nine types of reset</p> <ul style="list-style-type: none"> RES# pin reset: Generated when the RES# pin is driven low. Power-on reset: Generated when the RES# pin is driven high and VCC rises. Voltage-monitoring 0 reset: Generated when VCC falls. Voltage-monitoring 1 reset: Generated when VCC falls. Voltage-monitoring 2 reset: Generated when VCC falls. Deep software standby reset: Generated in response to an interrupt to trigger release from deep software standby. Independent watchdog timer reset: Generated when the independent watchdog timer underflows, or a refresh error occurs. Watchdog timer reset: Generated when the watchdog timer underflows, or a refresh error occurs. Software reset: Generated by register setting. |
| Power-on reset | | <p>If the RES# pin is at the high level when power is supplied, an internal reset is generated. After VCC has exceeded the voltage detection level and the specified period has elapsed, the reset is cancelled.</p> |
| Voltage detection circuit (LVDA) | | <p>Monitors the voltage being input to the VCC pin and generates an internal reset or internal interrupt.</p> <ul style="list-style-type: none"> Voltage detection circuit 0 <ul style="list-style-type: none"> Capable of generating an internal reset The option-setting memory can be used to select enabling or disabling of the reset. Voltage detection level: Selectable from two different levels Voltage detection circuits 1 and 2 <ul style="list-style-type: none"> Voltage detection level: Selectable from five different levels Digital filtering (1/2, 1/4, 1/8, and 1/16 LOCO frequency) Capable of generating an internal reset Two types of timing are selectable for release from reset <ul style="list-style-type: none"> An internal interrupt can be requested. Detection of voltage rising above and falling below thresholds is selectable. Maskable or non-maskable interrupt is selectable Voltage detection monitoring Event linking |

Table 1.1 Outline of Specifications (3/9)

| Classification | Module/Function | Description |
|------------------------|----------------------------------|--|
| Low power consumption | Low power consumption facilities | <ul style="list-style-type: none"> Module stop function Four low power consumption modes Sleep mode, all-module clock stop mode, software standby mode, and deep software standby mode |
| Interrupt | Interrupt controller (ICUC) | <ul style="list-style-type: none"> Interrupt vectors: 256 External interrupts: 16 (pins IRQ0 to IRQ15) Software interrupts: 2 sources Non-maskable interrupts: 7 sources Sixteen levels specifiable for the order of priority Method of interrupt source selection: The interrupt vectors consist of 256 vectors (208 sources are fixed. The remaining 135 vectors are selected from among the other 48 sources.) |
| External bus extension | | <ul style="list-style-type: none"> The external address space can be divided into four areas (CS0 to CS3), each with independent control of access settings. Capacity of each area: 2 Mbytes (CS0 to CS3) A chip-select signal (CS0# to CS3#) can be output for each area. Each area is specifiable as an 8- or 16-bit bus space. The data arrangement in each area is selectable as little or big endian (only for data). Bus format: Separate bus, multiplex bus Wait control Write buffer facility |
| DMA | DMA controller (DMACa) | <ul style="list-style-type: none"> 8 channels Three transfer modes: Normal transfer, repeat transfer, and block transfer Request sources: Software trigger, external interrupts, and interrupt requests from peripheral functions |
| | Data transfer controller (DTCa) | <ul style="list-style-type: none"> Three transfer modes: Normal transfer, repeat transfer, and block transfer Request sources: External interrupts and interrupt requests from peripheral functions |
| I/O ports | Programmable I/O ports | <ul style="list-style-type: none"> I/O ports for the 144-pin LFQFP I/O pins: 110 Input pin: 9 Pull-up resistors: 110 Open-drain outputs: 110 5-V tolerance: 4 Large current output: 15 I/O ports for the 112-pin LQFP I/O pins: 84 Input pin: 9 Pull-up resistors: 84 Open-drain outputs: 84 5-V tolerance: 2 Large current output: 15 I/O ports for the 100-pin LFQFP (with PGA pseudo-differential input, and with USB) I/O pins: 69 Input pin: 9 Pull-up resistors: 69 Open-drain outputs: 69 5-V tolerance: 3 Large current output: 15 I/O ports for the 100-pin LFQFP (with PGA pseudo-differential input, and without USB) I/O pins: 72 Input pin: 9 Pull-up resistors: 72 Open-drain outputs: 72 5-V tolerance: 2 (products with 64 Kbytes of RAM), 3 (products with 128 Kbytes of RAM) Large current output: 15 I/O ports for the 100-pin LFQFP (without PGA pseudo-differential input, and without USB) I/O pins: 73 Input pin: 7 Pull-up resistors: 73 Open-drain outputs: 73 5-V tolerance: 2 (products with 64 Kbytes of RAM), 3 (products with 128 Kbytes of RAM) Large current output: 15 |

Table 1.1 Outline of Specifications (4/9)

| Classification | Module/Function | Description |
|-----------------------------|------------------------------------|---|
| I/O ports | Programmable I/O ports | <ul style="list-style-type: none"> I/O ports for the 80-pin LFQFP, 80-pin LQFP I/O pins: 52 Input pin: 9 Pull-up resistors: 52 Open-drain outputs: 52 5-V tolerance: 2 Large current output: 14 I/O ports for the 64-pin LFQFP I/O pins: 39 Input pin: 7 Pull-up resistors: 39 Open-drain outputs: 39 5-V tolerance: 2 Large current output: 14 |
| Event link controller (ELC) | | <ul style="list-style-type: none"> Event signals such as interrupt request signals can be interlinked with the operation of functions such as timer counting, eliminating the need for intervention by the CPU to control the functions. 188 internal event signals can be freely combined for interlinked operation with connected functions. Event signals from peripheral modules can be used to change the states of output pins (of ports B and E). Changes in the states of pins (of ports B and E) being used as inputs can be interlinked with the operation of peripheral modules. |
| Timers | 8-bit timers (TMR) | <ul style="list-style-type: none"> (8 bits × 2 channels) × 4 units Select from among seven internal clock signals (PCLKB/1, PCLKB/2, PCLKB/8, PCLKB/32, PCLKB/64, PCLKB/1024, PCLKB/8192) and one external clock signal Capable of output of pulse trains with desired duty cycles or of PWM signals The 2 channels of each unit can be cascaded to create a 16-bit timer Generation of triggers for A/D converter conversion Capable of generating baud-rate clocks for SCI5, SCI6, and SCI12 Event linking by the ELC |
| | Compare match timer (CMT) | <ul style="list-style-type: none"> (16 bits × 2 channels) × 2 units Select from among four internal clock signals (PCLKB/8, PCLKB/32, PCLKB/128, PCLKB/512) Event linking by the ELC |
| | Watchdog timer (WDTA) | <ul style="list-style-type: none"> 14 bits × 1 channel Select from among 6 counter-input clock signals (PCLKB/4, PCLKB/64, PCLKB/128, PCLKB/512, PCLKB/2048, PCLKB/8192) |
| | Independent watchdog timer (IWDTa) | <ul style="list-style-type: none"> 14 bits × 1 channel Counter-input clock: IWDT-dedicated on-chip oscillator Dedicated clock/1, dedicated clock/16, dedicated clock/32, dedicated clock/64, dedicated clock/128, dedicated clock/256 Window function: The positions where the window starts and ends are specifiable (the window defines the timing with which refreshing is enabled and disabled). Event linking by the ELC |

Table 1.1 Outline of Specifications (5/9)

| Classification | Module/Function | Description |
|----------------|--|---|
| Timers | Multifunction timer pulse unit 3 (MTU3d) | <ul style="list-style-type: none"> • 9 channels (16 bits × 9 channels) • Maximum of 28 pulse-input/output and 3 pulse-input possible • Select from among 14 counter-input clock signals for each channel (PCLKC/1, PCLKC/2, PCLKC/4, PCLKC/8, PCLKC/16, PCLKC/32, PCLKC/64, PCLKC/256, PCLKC/1024, MTCLKA, MTCLKB, MTCLKC, MTCLKD, MTIOC1A) 11 of the signals are available for channels 1, 3, 4, 12 are available for channel 2, and 10 are available for channel 5. • 43 output compare/input capture registers • Counter clear operation (synchronous clearing by compare match/input capture) • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous register input/output by synchronous counter operation • Buffered operation • Support for cascade-connected operation • 45 interrupt sources • Automatic transfer of register data • Pulse output mode Toggle/PWM/complementary PWM/reset-synchronized PWM • Complementary PWM output mode Outputs non-overlapping waveforms for controlling 3-phase inverters Automatic specification of dead times PWM duty cycle: Selectable as any value from 0% to 100% Delay can be applied to requests for A/D conversion. Non-generation of interrupt requests at peak or trough values of counters can be selected. Double buffer configuration • Reset synchronous PWM mode Three phases of positive and negative PWM waveforms can be output with desired duty cycles. • Phase-counting mode: 16-bit mode (channels 1 and 2); 32-bit mode (channels 1 and 2) • Counter functionality for dead-time compensation • Generation of triggers for A/D converter conversion The timing of the generation of requests to start A/D conversion can be monitored by an external pin. • A/D converter start triggers can be skipped • Digital filter function for signals on the input capture and external counter clock pins • Event linking by the ELC • Internal peripheral bus clock: PCLKA • Counter reference clock: PCLKC • Frequency ratio: PCLKA to PCLKC = 1: N (N = 1 or 2) |
| | Port output enable 3 (POE3B) | <ul style="list-style-type: none"> • Control of the high-impedance state of the MTU3/GPTW's waveform output pins, and control of switching to the general I/O port pin • 9 pins for input from signal sources: POE0, POE4, POE8, POE9, POE10, POE11, POE12, POE13, POE14 • Initiation by detection of short-circuited outputs (detection of PWM outputs that have become an active level simultaneously) • Initiation by comparator detection/oscillation stop detection/software • Additional programming of output control target pins is enabled |

Table 1.1 Outline of Specifications (6/9)

| Classification | Module/Function | Description |
|------------------------|--|---|
| Timers | General PWM timer (GPTW) | <ul style="list-style-type: none"> • 32 bits × 10 channels • Counting up or down (sawtooth-wave), counting up and down (triangle-wave) selectable for all channels • Clock sources independently selectable for each channel • 2 input/output pins per channel • 2 output compare/input capture registers per channel • For the 2 output compare/input capture registers of each channel, 4 registers are provided as buffer registers and are capable of operating as comparison registers when buffering is not in use. • In output compare operation, buffer switching can be at peaks or troughs, enabling the generation of laterally asymmetrically PWM waveforms. • Registers for setting up frame intervals on each channel (with capability for generating interrupts on overflow or underflow) • Generation of dead times in PWM operation • Capable of synchronous start, stop, or clearing of counter for any channel • Capable of a start, stop, clearing, or up-/down-counting of the counter supporting maximum of 8 ELC events • Capable of a start, stop, clearing, or up-/down-counting of the counter supporting input level comparison • Capable of a start, stop, clearing, or up-/down-counting of the counter supporting maximum of 4 external triggers • Output pin disabling function by a dead time error or a short circuit detection among output pins • Capable of generating conversion start triggers for the A/D converters as well as monitoring external pins for a start timing of conversion. • Capable of outputting events, such as compare-match from A to F and overflow/underflow, to ELC • Capable of using noise filter of input capture • Internal peripheral bus clock: PCLKA • Counter reference clock: PCLKC • Frequency ratio: PCLKA to PCLKC = 1: N (N = 1 or 2) |
| | High resolution PWM (HRPWM) | <ul style="list-style-type: none"> • Capable of generating the PWM waveform that is generated by GPTW0 through GPTW3 with resolution of minimum of 195 ps. |
| | Port output enable for GPTW (POEG) | <ul style="list-style-type: none"> • Controlling the output disable for GPTW waveform output • Initiation by input level detection of GTETRG pins • Initiation by output disable request from GPTW • Initiation by detection of comparator interrupt request • Initiation by detection of oscillation stop or by software |
| Communication function | USB 2.0 FS host/function module (USBb) | <ul style="list-style-type: none"> • Includes a UDC (USB Device Controller) and transceiver for USB 2.0 FS • One port • Compliance with the USB 2.0 specification • Transfer rate: Full speed (12 Mbps), low speed (1.5 Mbps) (host only) • Self-power mode and bus power are selectable • OTG (On the Go) operation is possible (low-speed is not supported) • Incorporates 2 Kbytes of RAM as a transfer buffer • External pull-up and pull-down resistors are not required |

Table 1.1 Outline of Specifications (7/9)

| Classification | Module/Function | Description |
|------------------------|---|---|
| Communication function | Serial communications interfaces (SCIj, SCli, SClh) | <ul style="list-style-type: none"> • 7 channels SCIj: SCI1, SCI5, SCI6, SCI8, SCI9 SCli: SCI11 SClh: SCI12 • SCIj, SCli, SClh Serial communications modes: Asynchronous, clock synchronous, and smart-card interface Multi-processor function On-chip baud rate generator allows selection of the desired bit rate Choice of LSB-first or MSB-first transfer Average transfer rate clock can be input from TMR timers for SCI5, SCI6, and SCI12 Start-bit detection: Level or edge detection is selectable. Simple I²C Simple SPI 7, 8, 9-bit transfer mode Bit rate modulation Double-speed mode Data match detection (SCI12 is not supported) Event linking by the ELC (supported by SCI5 only) • SCli Only Capable of serial sending and receiving with 16-byte FIFO-buffered structure both at transmission and reception sections • SClh Only Supports the serial communications protocol, which contains the start frame and information frame Supports the LIN format |
| | I ² C bus interface (RIICa) | <ul style="list-style-type: none"> • 1 channel Communication formats I²C bus format/SMBus format Supports the multi-master Max. transfer rate: 400 kbps • Event linking by the ELC |
| | CAN module (CAN) | <ul style="list-style-type: none"> • 1 channel • Compliance with the ISO11898-1 specification (standard frame and extended frame) • 32 mailboxes per channel |
| | Serial peripheral interface (RSPic) | <ul style="list-style-type: none"> • 1 channel • RSPi transfer facility Using the MOSI (master out, slave in), MISO (master in, slave out), SSL (slave select), and RSPCK (RSPi clock) signals enables serial transfer through SPI operation (four lines) or clock-synchronous operation (three lines) Capable of handling serial transfer as a master or slave • Data formats Switching between MSB first and LSB first The number of bits in each transfer can be changed to any number of bits from 8 to 16, 20, 24, or 32 bits. 128-bit buffers for transmission and reception Up to four frames can be transmitted or received in a single transfer operation (with each frame having up to 32 bits) • Buffered structure Double buffers for both transmission and reception • RSPCK can be stopped with the receive buffer full for master reception. • Event linking by the ELC |

Table 1.1 Outline of Specifications (8/9)

| Classification | Module/Function | Description |
|-------------------------------|------------------------------------|---|
| 12-bit A/D converter (S12ADH) | | <ul style="list-style-type: none"> • 12 bits (8 channels × 2 units, 14 channels × 1 unit) • 12-bit resolution • Minimum conversion time 0.9 μs per channel (when ADCLK operates at 60 MHz) • Operating mode Scan mode (single scan mode, continuous scan mode, or 3 group scan mode) Group A priority control (only for 3 group scan mode) • Sample-and-hold function channel-dedicated sample-and-hold function (unit 0 × 3 channels, unit 1 × 3 channels) included • Sampling variable Sampling time can be set up for each channel. • Conversion function in order of arbitrarily selected channels (Serial conversion of the same channel cannot be allowed) • Double trigger mode (A/D conversion data duplicated) • Three ways to start A/D conversion Software trigger, synchronous trigger (MTU, TMR, ELC), external trigger • Prioritization in group scanning can be controlled among group A, B, and C. • Digital comparison Method: Comparison to detect voltages above or below thresholds and window comparison Measurement: Comparison of two results of conversion or comparison of a value in the comparison register and a result of conversion • Self-diagnostic function • Detection of analog input disconnection • Event linking by the ELC • Input signal amplification function by the programmable gain amplifier (unit 0 × 3 channels, unit 1 × 3 channels) Capable of supporting single end/pseudo-differential input |
| 12-bit D/A converter (R12DAb) | | <ul style="list-style-type: none"> • 2 channels • 12-bit resolution • Output voltage: 0 V to AVCC2 • Capable of providing as a reference voltage for comparator • Event linking by the ELC |
| Comparator C (CMPC) | | <ul style="list-style-type: none"> • 6 channels • Function to compare the reference voltage and the analog input voltage • Reference voltage is selectable from 4 inputs • Analog input voltage is selectable from 4 inputs • Digital filtering |
| Temperature sensor | | <ul style="list-style-type: none"> • 1 channel • Relative precision: ±1.0°C • The voltage of the temperature is converted into a digital value by the 12-bit A/D converter (unit 2). |
| Safety | Memory protection unit (MPU) | <ul style="list-style-type: none"> • Protection area: Eight areas (max.) can be specified in the range from 0000 0000h to FFFF FFFFh. • Minimum protection unit: 16 bytes • Reading from, writing to, and enabling the execution access can be specified for each area. • An access exception occurs when the detected access is not in the permitted area. |
| | Trusted Memory (TM) Function | <ul style="list-style-type: none"> • Protects against the reading of programs from blocks 8 and 9 of the code flash memory • Instruction fetching by the CPU is the only form of access to these areas when the TM function is enabled. |
| | Register write protection function | <ul style="list-style-type: none"> • Protects important registers from being overwritten for in case a program runs out of control. |

Table 1.1 Outline of Specifications (9/9)

| Classification | Module/Function | Description |
|-----------------------|--|--|
| Safety | CRC calculator (CRCA) | <ul style="list-style-type: none"> • Generation of CRC codes for 8-/32-bit data 8-bit data Selectable from the following three polynomials $X^8 + X^2 + X + 1$, $X^{16} + X^{15} + X^2 + 1$, $X^{16} + X^{12} + X^5 + 1$ 32-bit data Selectable from the following two polynomials $X^{32} + X^{26} + X^{23} + X^{22} + X^{16} + X^{12} + X^{11} + X^{10} + X^8 + X^7 + X^5 + X^4 + X^2 + X + 1$, $X^{32} + X^{28} + X^{27} + X^{26} + X^{25} + X^{23} + X^{22} + X^{20} + X^{19} + X^{18} + X^{14} + X^{13} + X^{11} + X^{10} + X^9 + X^8 + X^6 + 1$ • Generation of CRC codes for use with LSB-first or MSB-first communications is selectable |
| | Main clock oscillation stop detection function | <ul style="list-style-type: none"> • Main clock oscillation stop detection: Available |
| | Clock frequency accuracy measurement circuit (CAC) | <ul style="list-style-type: none"> • Monitors the clock output from the main clock oscillator, low- and high-speed on-chip oscillators, the PLL frequency synthesizer, IWDWT-dedicated on-chip oscillator, and PCLKB. |
| | Data operation circuit (DOC) | <ul style="list-style-type: none"> • The function to compare, add, or subtract 16-bit data |
| Encryption functions | Trusted Secure IP (TSIP-Lite) | <ul style="list-style-type: none"> • Access management circuit • Encryption engine 128- or 256-bit key sizes of AES Block cipher mode of operation: GCM, ECB, CBC, CMAC, XTS, CTR, GCTR • Hash function • True random number generator • Prevention from illicit copying of a key |
| Operating frequency | | Up to 160 MHz |
| Power supply voltage | | VCC = 2.7 to 5.5V AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V (VCC ≤ AVCC0 = AVCC1 = AVCC2) With USB in use: VCC_USB = 3.0 to 3.6V (VCC ≥ VCC_USB) With USB not in use: VCC_USB = VCC VSS = AVSS0 = AVSS1 = AVSS2 = VSS_USB = 0V |
| Operating temperature | | D-version: -40 to +85°C G-version: -40 to +105°C |
| Package | | 144-pin LQFP 0.5 mm pitch 112-pin LQFP 0.65 mm pitch 100-pin LQFP 0.5 mm pitch 80-pin LQFP 0.5 mm pitch 80-pin LQFP 0.65 mm pitch 64-pin LQFP 0.5 mm pitch |
| Debugging interfaces | | <ul style="list-style-type: none"> • JTAG and One-line FINE interfaces |

Table 1.2 Comparison of Functions for Different Packages (1/2)

| Module/Functions | | RX66T Group | | | | | | | | |
|----------------------------|--|------------------------------------|----------|--------------------|---------------------------------------|------------------------------------|-------------|--------------------|---------------------------------------|----------|
| | | RAM 128 Kbytes | | | | RAM 64 Kbytes | | | | |
| | | With PGA pseudo-differential input | | | Without PGA pseudo-differential input | With PGA pseudo-differential input | | | Without PGA pseudo-differential input | |
| | | With USB | | Without USB | | With USB | | Without USB | | |
| | | 144 Pins | 100 Pins | 100 Pins | 100 Pins | 112 Pins | 100 Pins | 80 Pins | 64 Pins | 100 Pins |
| Code flash memory capacity | | Maximum 1 Mbyte | | | | Maximum 512 Kbytes | | | | |
| External bus | External bus width | 16 bits | | | | | — | — | 16 bits | |
| | Address Space | 2 Mbytes × 4 areas | | 2 Mbytes × 3 areas | | — | — | 2 Mbytes × 3 areas | | |
| External interrupts | NMI | Available | | | | | | | | |
| | IRQ | 16 channels | | | | | 13 channels | 11 channels | 16 channels | |
| DMA | DMA controller | Available | | | | | | | | |
| | Data transfer controller | Available | | | | | | | | |
| Timers | Multifunction timer pulse unit 3 | 9 channels (Ch. 0 to 7, Ch. 9) | | | | | | | | |
| | General PWM timer | 10 channels | | | | | | | | |
| | High resolution PWM | 4 channels | | | | | | | | |
| | Port output enable 3 | Available | | | | | | | | |
| | Port Output Enable for GPTW | Available | | | | | | | | |
| | 8-bit timer | 2 channels × 4 units | | | | | | | | |
| | Compare match timer | 2 channels × 2 units | | | | | | | | |
| | Independent watchdog timer | Available | | | | | | | | |
| Communication functions | USB 2.0 FS host/function module | 1 channel | — | | | | | | | |
| | Serial communications interfaces (SCIj) | 5 channels (SCI1, 5, 6, 8, 9) | | | | | | | | |
| | Serial communications interfaces (SCIl) | 1 channel (SCI11) | | | | | | | | |
| | Serial communications interfaces (SCIlh) | 1 channel (SCI12) | | | | | | | | |
| | I ² C bus interfaces | 1 channel | | | | | | | | |
| | Serial peripheral interface | 1 channel | | | | | | | | |
| | CAN module | 1 channel | | | | | | | | |

Table 1.2 Comparison of Functions for Different Packages (2/2)

| Module/Functions | RX66T Group | | | | | | | | |
|--|--|--|--|--|--|---|--|--|--|
| | RAM 128 Kbytes | | | | RAM 64 Kbytes | | | | |
| | With PGA pseudo-differential input | | | Without PGA pseudo-differential input | With PGA pseudo-differential input | | | | Without PGA pseudo-differential input |
| | With USB | | Without USB | | | | | | |
| | 144 Pins | 100 Pins | 100 Pins | 100 Pins | 112 Pins | 100 Pins | 80 Pins | 64 Pins | 100 Pins |
| 12-bit A/D Converter | AN000 to 007*1 (unit 0: 8 channels) | AN000 to 003, 007*1 (unit 0: 5 channels) | AN000 to 003 (unit 0: 4 channels) | AN000 to 003, 007*1 (unit 0: 5 channels) | AN000 to 003, 007*1 (unit 0: 5 channels) | AN000 to 003, 007*1 (unit 0: 5 channels) | AN000 to 002, 007*1 (unit 0: 4 channels) | AN000 to 003 (unit 0: 4 channels) | AN000 to 003 (unit 0: 4 channels) |
| | AN100 to 107*1 (unit 1: 8 channels) | AN100 to 103, 107*1 (unit 1: 5 channels) | AN100 to 103 (unit 1: 4 channels) | AN100 to 103, 107*1 (unit 1: 5 channels) | AN100 to 103, 107*1 (unit 1: 5 channels) | AN100 to 102, 107*1 (unit 1: 4 channels) | AN100 to 103 (unit 1: 4 channels) | AN100 to 103 (unit 1: 4 channels) | AN100 to 103 (unit 1: 4 channels) |
| | AN200 to 211, 216, 217 (unit 2: 14 channels) | AN200 to 203, 206 to 211, 216, 217 (unit 2: 12 channels) | AN200 to 211, 216, 217 (unit 2: 14 channels) | AN200 to 203, 206 to 211, 216, 217 (unit 2: 12 channels) | AN200 to 203, 208, 210, 211, 216, 217 (unit 2: 9 channels) | AN200 to 202, 210, 211, 216, 217 (unit 2: 7 channels) | AN200 to 211, 216, 217 (unit 2: 14 channels) | AN200 to 211, 216, 217 (unit 2: 14 channels) | AN200 to 211, 216, 217 (unit 2: 14 channels) |
| 3 channels simultaneous sampling function | 3 channels × 2 units (unit 0, 1) | | | | | | | | |
| Programmable gain amplifier | 6 channels | | | | | | | | |
| Comparator C | 6 channels | | | | | | | | |
| D/A converter | 2 channels | | | | | | | | |
| Temperature sensor | 1 channel | | | | | | | | |
| CRC calculator | Available | | | | | | | | |
| Clock frequency accuracy measurement circuit | Available | | | | | | | | |
| Trusted Secure IP (TSIP-Lite) | Available/Not available | | | | | | | | |
| Event link controller | Available | | | | | | | | |
| Packages | 144-pin LQFP | 100-pin LQFP | 100-pin LQFP | 100-pin LQFP | 112-pin LQFP | 100-pin LQFP | 80-pin LQFP, LQFP | 64-pin LQFP | 100-pin LQFP |

Note 1. AN007 and AN107 cannot be used when PGA pseudo-differential input is enabled.

1.2 List of Products

Table 1.3 is a list of products, and Figure 1.1 shows how to read the product part no.

Table 1.3 List of Products (1/3)

| Group | Part No. | Part No. (for Orders) | Package | Code Flash Memory Capacity | RAM Capacit y | Data Flash Memory Capacity | PGA pseudo- differential input | TSIP-Lite | USB | Operati ng temper ature | Note |
|-------|------------------|--------------------------|------------------|-------------------------------------|---------------------|-------------------------------------|---|------------------|------------------|----------------------------------|------|
| RX66T | R5F566TKCD FB | R5F566TKCD FB#30 | PLQP0144KA- B | 1 Mbyte | 128 Kbytes | 32 Kbytes | Available | Not available | Available | -40 to 85°C | |
| | R5F566TKGD FB | R5F566TKGD FB#30 | PLQP0144KA- B | 1 Mbyte | 128 Kbytes | 32 Kbytes | Available | Available | Available | -40 to 85°C | |
| | R5F566TFCD FB | R5F566TFCD FB#30 | PLQP0144KA- B | 512 Kbytes | 128 Kbytes | 32 Kbytes | Available | Not available | Available | -40 to 85°C | |
| | R5F566TFGD FB | R5F566TFGD FB#30 | PLQP0144KA- B | 512 Kbytes | 128 Kbytes | 32 Kbytes | Available | Available | Available | -40 to 85°C | |
| | R5F566TEAD FH | R5F566TEAD FH#30 | PLQP0112JA- B | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 85°C | |
| | R5F566TEED FH | R5F566TEED FH#30 | PLQP0112JA- B | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 85°C | |
| | R5F566TAAD FH | R5F566TAAD FH#30 | PLQP0112JA- B | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 85°C | |
| | R5F566TAED FH | R5F566TAED FH#30 | PLQP0112JA- B | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 85°C | |
| | R5F566TKAD FP | R5F566TKAD FP#30 | PLQP0100KB- B | 1 Mbyte | 128 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 85°C | |
| | R5F566TKBD FP | R5F566TKBD FP#30 | PLQP0100KB- B | 1 Mbyte | 128 Kbytes | 32 Kbytes | Not available | Not available | Not available | -40 to 85°C | |
| | R5F566TKCD FP | R5F566TKCD FP#30 | PLQP0100KB- B | 1 Mbyte | 128 Kbytes | 32 Kbytes | Available | Not available | Available | -40 to 85°C | |
| | R5F566TKED FP | R5F566TKED FP#30 | PLQP0100KB- B | 1 Mbyte | 128 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 85°C | |
| | R5F566TKFD FP | R5F566TKFD FP#30 | PLQP0100KB- B | 1 Mbyte | 128 Kbytes | 32 Kbytes | Not available | Available | Not available | -40 to 85°C | |
| | R5F566TKGD FP | R5F566TKGD FP#30 | PLQP0100KB- B | 1 Mbyte | 128 Kbytes | 32 Kbytes | Available | Available | Available | -40 to 85°C | |
| | R5F566TFADF P | R5F566TFADF P#30 | PLQP0100KB- B | 512 Kbytes | 128 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 85°C | |
| | R5F566TFBD FP | R5F566TFBD FP#30 | PLQP0100KB- B | 512 Kbytes | 128 Kbytes | 32 Kbytes | Not available | Not available | Not available | -40 to 85°C | |
| | R5F566TFCD FP | R5F566TFCD FP#30 | PLQP0100KB- B | 512 Kbytes | 128 Kbytes | 32 Kbytes | Available | Not available | Available | -40 to 85°C | |
| | R5F566TFED FP | R5F566TFED FP#30 | PLQP0100KB- B | 512 Kbytes | 128 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 85°C | |
| | R5F566TFFDF P | R5F566TFFDF P#30 | PLQP0100KB- B | 512 Kbytes | 128 Kbytes | 32 Kbytes | Not available | Available | Not available | -40 to 85°C | |
| | R5F566TFGD FP | R5F566TFGD FP#30 | PLQP0100KB- B | 512 Kbytes | 128 Kbytes | 32 Kbytes | Available | Available | Available | -40 to 85°C | |
| | R5F566TEAD FP | R5F566TEAD FP#30 | PLQP0100KB- B | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 85°C | |
| | R5F566TEBD FP | R5F566TEBD FP#30 | PLQP0100KB- B | 512 Kbytes | 64 Kbytes | 32 Kbytes | Not available | Not available | Not available | -40 to 85°C | |
| | R5F566TEED FP | R5F566TEED FP#30 | PLQP0100KB- B | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 85°C | |
| | R5F566TEFD FP | R5F566TEFD FP#30 | PLQP0100KB- B | 512 Kbytes | 64 Kbytes | 32 Kbytes | Not available | Available | Not available | -40 to 85°C | |
| | R5F566TAAD FP | R5F566TAAD FP#30 | PLQP0100KB- B | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 85°C | |
| | R5F566TABD FP | R5F566TABD FP#30 | PLQP0100KB- B | 256 Kbytes | 64 Kbytes | 32 Kbytes | Not available | Not available | Not available | -40 to 85°C | |
| | R5F566TAED FP | R5F566TAED FP#30 | PLQP0100KB- B | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 85°C | |

Table 1.3 List of Products (2/3)

| Group | Part No. | Part No. (for Orders) | Package | Code Flash Memory Capacity | RAM Capacit y | Data Flash Memory Capacity | PGA pseudo- differential input | TSIP-Lite | USB | Operati ng temper ature | Note |
|-------|--------------|--------------------------|--------------|-------------------------------------|---------------------|-------------------------------------|---|------------------|------------------|----------------------------------|------|
| RX66T | R5F566TAFDFP | R5F566TAFDFP#30 | PLQP0100KB-B | 256 Kbytes | 64 Kbytes | 32 Kbytes | Not available | Available | Not available | -40 to 85°C | |
| | R5F566TEADFF | R5F566TEADFF#30 | PLQP0080JA-A | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 85°C | |
| | R5F566TEEDFF | R5F566TEEDFF#30 | PLQP0080JA-A | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 85°C | |
| | R5F566TAADFF | R5F566TAADFF#30 | PLQP0080JA-A | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 85°C | |
| | R5F566TAEDFF | R5F566TAEDFF#30 | PLQP0080JA-A | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 85°C | |
| | R5F566TEADFN | R5F566TEADFN#30 | PLQP0080KB-B | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 85°C | |
| | R5F566TEEDFN | R5F566TEEDFN#30 | PLQP0080KB-B | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 85°C | |
| | R5F566TAADFN | R5F566TAADFN#30 | PLQP0080KB-B | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 85°C | |
| | R5F566TAEDFN | R5F566TAEDFN#30 | PLQP0080KB-B | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 85°C | |
| | R5F566TEADFM | R5F566TEADFM#30 | PLQP0064KB-C | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 85°C | |
| | R5F566TEEDFM | R5F566TEEDFM#30 | PLQP0064KB-C | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 85°C | |
| | R5F566TAADFM | R5F566TAADFM#30 | PLQP0064KB-C | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 85°C | |
| | R5F566TAEDFM | R5F566TAEDFM#30 | PLQP0064KB-C | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 85°C | |
| | R5F566TKCGFB | R5F566TKCGFB#30 | PLQP0144KA-B | 1 Mbyte | 128 Kbytes | 32 Kbytes | Available | Not available | Available | -40 to 105°C | |
| | R5F566TKGGFB | R5F566TKGGFB#30 | PLQP0144KA-B | 1 Mbyte | 128 Kbytes | 32 Kbytes | Available | Available | Available | -40 to 105°C | |
| | R5F566TFCGFB | R5F566TFCGFB#30 | PLQP0144KA-B | 512 Kbytes | 128 Kbytes | 32 Kbytes | Available | Not available | Available | -40 to 105°C | |
| | R5F566TFGGFB | R5F566TFGGFB#30 | PLQP0144KA-B | 512 Kbytes | 128 Kbytes | 32 Kbytes | Available | Available | Available | -40 to 105°C | |
| | R5F566TEAGFH | R5F566TEAGFH#30 | PLQP0112JA-B | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 105°C | |
| | R5F566TEEGFH | R5F566TEEGFH#30 | PLQP0112JA-B | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 105°C | |
| | R5F566TAAGFH | R5F566TAAGFH#30 | PLQP0112JA-B | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 105°C | |
| | R5F566TAEGFH | R5F566TAEGFH#30 | PLQP0112JA-B | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 105°C | |
| | R5F566TKAGFP | R5F566TKAGFP#30 | PLQP0100KB-B | 1 Mbyte | 128 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 105°C | |
| | R5F566TKBGFP | R5F566TKBGFP#30 | PLQP0100KB-B | 1 Mbyte | 128 Kbytes | 32 Kbytes | Not available | Not available | Not available | -40 to 105°C | |
| | R5F566TKCGFP | R5F566TKCGFP#30 | PLQP0100KB-B | 1 Mbyte | 128 Kbytes | 32 Kbytes | Available | Not available | Available | -40 to 105°C | |
| | R5F566TKEGFP | R5F566TKEGFP#30 | PLQP0100KB-B | 1 Mbyte | 128 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 105°C | |
| | R5F566TKFGFP | R5F566TKFGFP#30 | PLQP0100KB-B | 1 Mbyte | 128 Kbytes | 32 Kbytes | Not available | Available | Not available | -40 to 105°C | |
| | R5F566TKGGFP | R5F566TKGGFP#30 | PLQP0100KB-B | 1 Mbyte | 128 Kbytes | 32 Kbytes | Available | Available | Available | -40 to 105°C | |
| | R5F566TFAGFP | R5F566TFAGFP#30 | PLQP0100KB-B | 512 Kbytes | 128 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 105°C | |
| | R5F566TFBGFP | R5F566TFBGFP#30 | PLQP0100KB-B | 512 Kbytes | 128 Kbytes | 32 Kbytes | Not available | Not available | Not available | -40 to 105°C | |

Table 1.3 List of Products (3/3)

| Group | Part No. | Part No. (for Orders) | Package | Code Flash Memory Capacity | RAM Capacit y | Data Flash Memory Capacity | PGA pseudo- differential input | TSIP-Lite | USB | Operati ng temper ature | Note |
|-------|-------------------|--------------------------|------------------|-------------------------------------|---------------------|-------------------------------------|---|------------------|------------------|----------------------------------|------|
| RX66T | R5F566TF CG FP | R5F566TF CG FP#30 | PLQP0100KB- B | 512 Kbytes | 128 Kbytes | 32 Kbytes | Available | Not available | Available | -40 to 105°C | |
| | R5F566TF EG FP | R5F566TF EG FP#30 | PLQP0100KB- B | 512 Kbytes | 128 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 105°C | |
| | R5F566TF FG FP | R5F566TF FG FP#30 | PLQP0100KB- B | 512 Kbytes | 128 Kbytes | 32 Kbytes | Not available | Available | Not available | -40 to 105°C | |
| | R5F566TF GG FP | R5F566TF GG FP#30 | PLQP0100KB- B | 512 Kbytes | 128 Kbytes | 32 Kbytes | Available | Available | Available | -40 to 105°C | |
| | R5F566TE AG FP | R5F566TE AG FP#30 | PLQP0100KB- B | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 105°C | |
| | R5F566TE BG FP | R5F566TE BG FP#30 | PLQP0100KB- B | 512 Kbytes | 64 Kbytes | 32 Kbytes | Not available | Not available | Not available | -40 to 105°C | |
| | R5F566TE EG FP | R5F566TE EG FP#30 | PLQP0100KB- B | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 105°C | |
| | R5F566TE FG FP | R5F566TE FG FP#30 | PLQP0100KB- B | 512 Kbytes | 64 Kbytes | 32 Kbytes | Not available | Available | Not available | -40 to 105°C | |
| | R5F566TA AG FP | R5F566TA AG FP#30 | PLQP0100KB- B | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 105°C | |
| | R5F566TAB G FP | R5F566TAB G FP#30 | PLQP0100KB- B | 256 Kbytes | 64 Kbytes | 32 Kbytes | Not available | Not available | Not available | -40 to 105°C | |
| | R5F566TA EG FP | R5F566TA EG FP#30 | PLQP0100KB- B | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 105°C | |
| | R5F566TAF G FP | R5F566TAF G FP#30 | PLQP0100KB- B | 256 Kbytes | 64 Kbytes | 32 Kbytes | Not available | Available | Not available | -40 to 105°C | |
| | R5F566TE AG FF | R5F566TE AG FF#30 | PLQP0080JA- A | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 105°C | |
| | R5F566TE EG FF | R5F566TE EG FF#30 | PLQP0080JA- A | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 105°C | |
| | R5F566TA AG FF | R5F566TA AG FF#30 | PLQP0080JA- A | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 105°C | |
| | R5F566TA EG FF | R5F566TA EG FF#30 | PLQP0080JA- A | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 105°C | |
| | R5F566TE AG FN | R5F566TE AG FN#30 | PLQP0080KB- B | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 105°C | |
| | R5F566TE EG FN | R5F566TE EG FN#30 | PLQP0080KB- B | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 105°C | |
| | R5F566TA AG FN | R5F566TA AG FN#30 | PLQP0080KB- B | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 105°C | |
| | R5F566TA EG FN | R5F566TA EG FN#30 | PLQP0080KB- B | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 105°C | |
| | R5F566TE AG FM | R5F566TE AG FM#30 | PLQP0064KB- C | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 105°C | |
| | R5F566TE EG FM | R5F566TE EG FM#30 | PLQP0064KB- C | 512 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 105°C | |
| | R5F566TA AG FM | R5F566TA AG FM#30 | PLQP0064KB- C | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Not available | Not available | -40 to 105°C | |
| | R5F566TA EG FM | R5F566TA EG FM#30 | PLQP0064KB- C | 256 Kbytes | 64 Kbytes | 32 Kbytes | Available | Available | Not available | -40 to 105°C | |

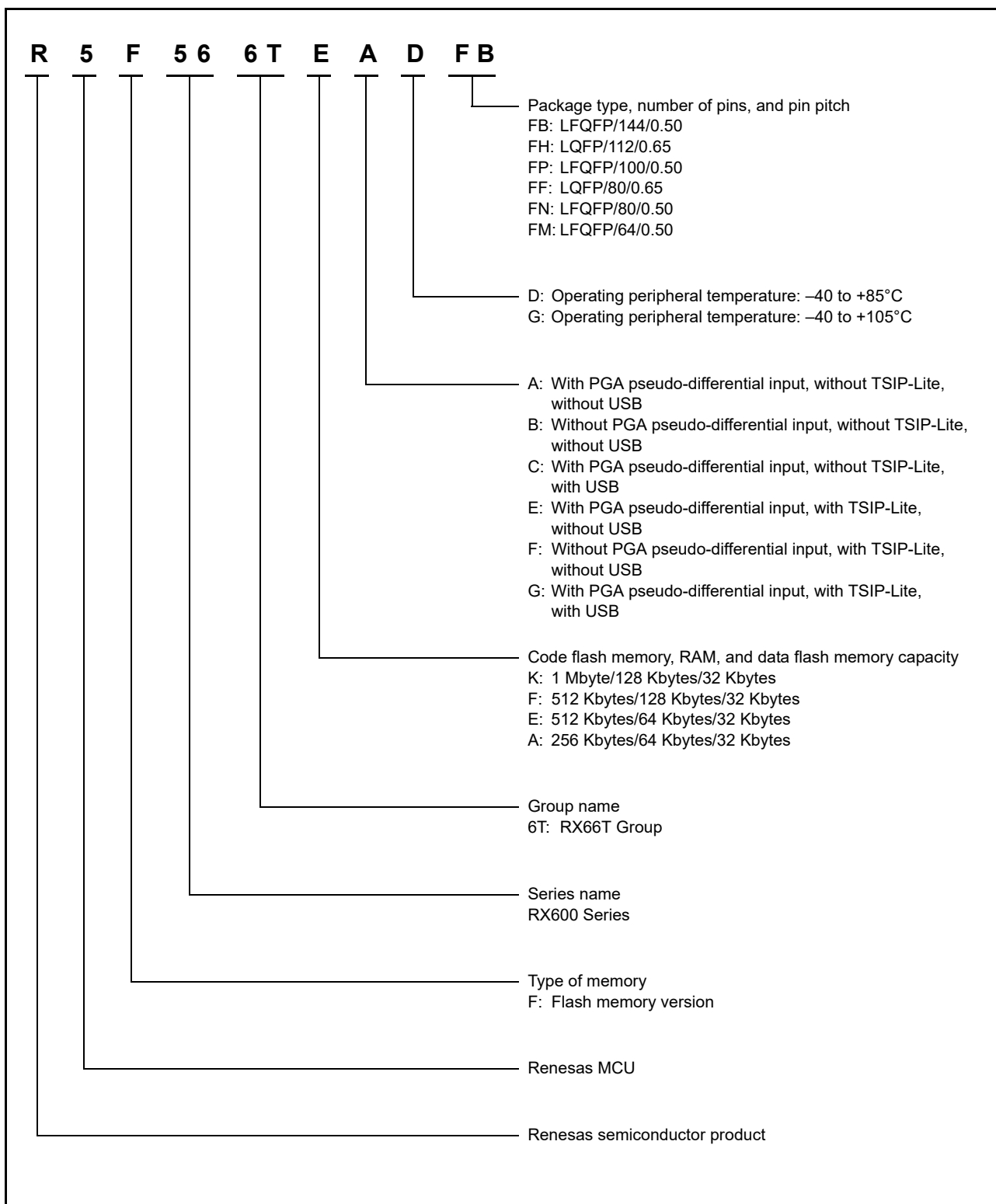


Figure 1.1 How to Read the Product Part Number

1.3 Block Diagram

Figure 1.2 shows a block diagram.

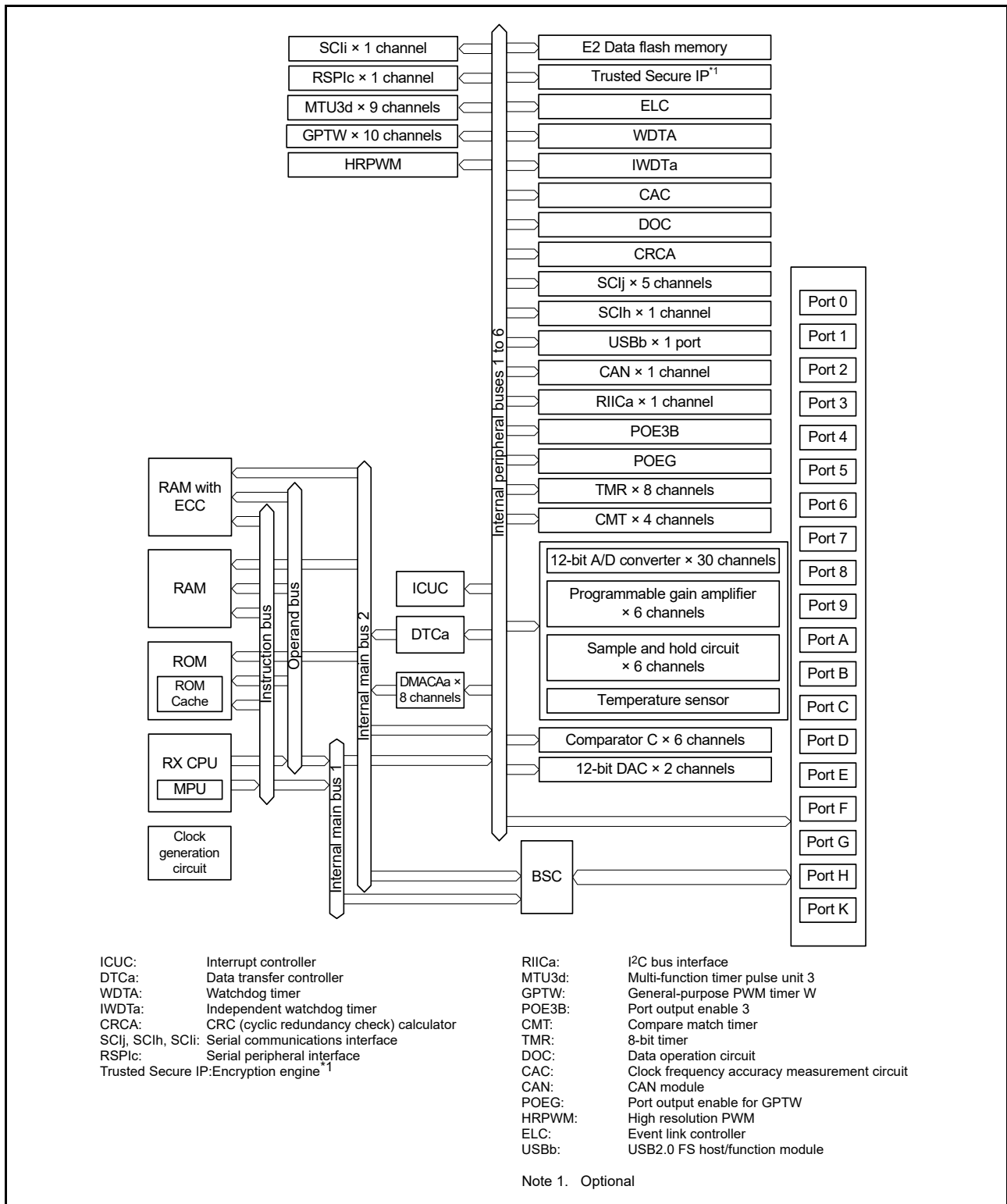


Figure 1.2 Block Diagram

1.4 Pin Functions

Table 1.4 lists the pin functions.

Table 1.4 Pin Functions (1/6)

| Classifications | Pin Name | I/O | Description |
|------------------------|--|--------|---|
| Digital power supply | VCC | — | Power supply pin. Connect this pin to the system power supply. Connect the pin to VSS via a 0.1- μ F multilayer ceramic capacitor. The capacitor should be placed close to the pin. |
| | VCL | — | Connect this pin to VSS via a 0.47- μ F multilayer ceramic capacitor. The capacitor should be placed close to the pin. |
| | VSS | — | Ground pin. Connect it to the system power supply (0 V). |
| Clock | XTAL | Output | Pins for a crystal resonator. An external clock signal can be input through the EXTAL pin. |
| | EXTAL | Input | |
| | BCLK | Output | Outputs the external bus clock for external devices. |
| CAC | CACREF | Input | Input pin for the clock frequency accuracy measurement circuit. |
| Operating mode control | MD | Input | Pins for setting the operating mode. The signal levels on these pins must not be changed during operation. |
| | UB | Input | Enable pin for boot mode (USB interface) and user boot mode |
| | UPSEL | Input | Selects the power supply method in boot mode (USB interface). The low level selects self-power mode and the high level selects bus power mode. |
| System control | RES# | Input | Reset pin. This MCU enters the reset state when this signal goes low. |
| | EMLE | Input | Input pin for the on-chip emulator enable signal. When the on-chip emulator is used, this pin should be driven high. When not used, it should be driven low. |
| On-chip emulator | FINED | I/O | FINE interface pin. |
| | TRST# | Input | Pins for the on-chip emulator. When the EMLE pin is driven high, these pins are dedicated for the on-chip emulator. |
| | TMS | Input | |
| | TDI | Input | |
| | TCK | Input | |
| | TDO | Output | |
| | TRCLK | Output | This pin outputs the clock for synchronization with the trace data. |
| | TRSYNC | Output | This pin indicates that output from the TRDATA0 to TRDATA3 pins is valid. |
| | TRSYNC1 | Output | This pin indicates that output from the TRDATA4 to TRDATA7 pins is valid. |
| | TRDATA0, TRDATA1, TRDATA2, TRDATA3, TRDATA4, TRDATA5, TRDATA6, TRDATA7 | Output | These pins output the trace information. |
| Address bus | A0 to A20 | Output | Output pins for the address |
| Data bus | D0 to D15 | I/O | Input and output pins for the bidirectional data bus |
| Multiplexed bus | A0/D0 to A15/D15 | I/O | Address/data multiplexed bus |
| Bus control | RD# | Output | Strobe signal which indicates that reading from the external bus interface space is in progress |
| | WR# | Output | Strobe signal which indicates that writing to the external bus interface space is in progress, in 1-write strobe mode |
| | WR0#, WR1# | Output | Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8) is valid in writing to the external bus interface space, in byte strobe mode |

Table 1.4 Pin Functions (2/6)

| Classifications | Pin Name | I/O | Description |
|-----------------------------------|--|--|---|
| Bus control | BC0#, BC1# | Output | Strobe signals which indicate that either group of data bus pins (D7 to D0, D15 to D8) is valid in access to the external bus interface space, in 1-write strobe mode |
| | ALE | Output | Address latch signal when address/data multiplexed bus is selected |
| | WAIT# | Input | Input pin for wait request signals in access to the external space |
| | CS0# to CS3# | Output | Select signals for CS areas |
| Interrupt | NMI | Input | Non-maskable interrupt request pin |
| | IRQ0 to IRQ15 | Input | Maskable interrupt request pins |
| | IRQ0-DS to IRQ15-DS | Input | Maskable interrupt request pins or pins which can also be used as triggers for release from deep software standby |
| Multi-function timer pulse unit 3 | MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D | I/O | The TGRA0 to TGRD0 input capture input/output compare output/PWM output pins |
| | MTIOC0A#, MTIOC0B#, MTIOC0C#, MTIOC0D# | I/O | The TGRA0 to TGRD0 input capture inverted input/output compare inverted output/PWM inverted output pins. |
| | MTIOC1A, MTIOC1B | I/O | The TGRA1 and TGRB1 input capture input/output compare output/PWM output pins. |
| | MTIOC1A#, MTIOC1B# | I/O | The TGRA1 and TGRB1 input capture inverted input/output compare inverted output/PWM inverted output pins. |
| | MTIOC2A, MTIOC2B | I/O | The TGRA2 and TGRB2 input capture input/output compare output/PWM output pins. |
| | MTIOC2A#, MTIOC2B# | I/O | The TGRA2 and TGRB2 input capture inverted input/output compare inverted output/PWM inverted output pins. |
| | MTIOC3A, MTIOC3B, MTIOC3C, MTIOC3D | I/O | The TGRA3 to TGRD3 input capture input/output compare output/PWM output pins. |
| | MTIOC3A#, MTIOC3B#, MTIOC3C#, MTIOC3D# | I/O | The TGRA3 to TGRD3 input capture inverted input/output compare inverted output/PWM inverted output pins. |
| | MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D | I/O | The TGRA4 to TGRD4 input capture input/output compare output/PWM output pins |
| | MTIOC4A#, MTIOC4B#, MTIOC4C#, MTIOC4D# | I/O | The TGRA4 to TGRD4 input capture inverted input/output compare inverted output/PWM inverted output pins. |
| | MTIC5U, MTIC5V, MTIC5W | Input | The TGRU5, TGRV5, and TGRW5 input capture input/external pulse input pins |
| | MTIC5U#, MTIC5V#, MTIC5W# | Input | The TGRU5, TGRV5, and TGRW5 input capture inverted input/external pulse inverted input pins. |
| | MTIOC6A, MTIOC6B, MTIOC6C, MTIOC6D | I/O | The TGRA6 to TGRD6 input capture input/output compare output/PWM output pins |
| | MTIOC6A#, MTIOC6B#, MTIOC6C#, MTIOC6D# | I/O | The TGRA6 to TGRD6 input capture inverted input/output compare inverted output/PWM inverted output pins. |
| | MTIOC7A, MTIOC7B, MTIOC7C, MTIOC7D | I/O | The TGRA7 to TGRD7 input capture input/output compare output/PWM output pins |
| | MTIOC7A#, MTIOC7B#, MTIOC7C#, MTIOC7D# | I/O | The TGRA7 to TGRD7 input capture inverted input/output compare inverted output/PWM inverted output pins. |
| | MTIOC9A, MTIOC9B, MTIOC9C, MTIOC9D | I/O | The TGRA9 to TGRD9 input capture input/output compare output/PWM output pins |
| | MTIOC9A#, MTIOC9B#, MTIOC9C#, MTIOC9D# | I/O | The TGRA9 to TGRD9 input capture inverted input/output compare inverted output/PWM inverted output pins. |
| | MTCLKA, MTCLKB, MTCLKC, MTCLKD | Input | Input pins for the external clock. |
| | MTCLKA#, MTCLKB#, MTCLKC#, MTCLKD# | Input | Inverted input pins for the external clock. |
| ADSM0, ADSM1 | Output | A/D conversion start request frame synchronization signal output pins. | |

Table 1.4 Pin Functions (3/6)

| Classifications | Pin Name | I/O | Description |
|---|--|--------|---|
| General PWM timer | GTETRGA, GTETRGB, GTETRGC, GTETRGD | Input | External trigger input pin |
| | GTIOC0A to GTIOC9A, GTIOC0B to GTIOC9B | I/O | Input capture input/output compare output/PWM output pins |
| | GTIOC0A# to GTIOC9A#, GTIOC0B# to GTIOC9B# | I/O | Input capture inverted input/output compare inverted output/ PWM inverted output pins |
| | GTADSM0, GTADSM1 | Output | A/D conversion start request monitoring output pins |
| 8-bit timer | TMO0 to TMO7 | Output | Compare match output pins. |
| | TMCI0 to TMCI7 | Input | Input pins for the external clock to be input to the counter. |
| | TMRI0 to TMRI7 | Input | Counter reset input pins. |
| Port output enable 3 | POE0#, POE4#, POE8#, POE9#, POE10#, POE11#, POE12#, POE13#, POE14# | Input | Input pins for request signals to switch the MTU3 and GPTW pins between the high impedance state |
| Serial communications interface (SCIj) | • Asynchronous mode/clock synchronous mode | | |
| | SCK1, SCK5, SCK6, SCK8, SCK9 | I/O | Input/output pins for the clock |
| | RXD1, RXD5, RXD6, RXD8, RXD9 | Input | Input pins for received data |
| | TXD1, TXD5, TXD6, TXD8, TXD9 | Output | Output pins for transmitted data |
| | CTS1#, CTS5#, CTS6#, CTS8#, CTS9# | Input | Input pins for controlling the start of transmission and reception. |
| | RTS1#, RTS5#, RTS6#, RTS8#, RTS9# | Output | Output pins for controlling the start of transmission and reception. |
| | • Simple I ² C mode | | |
| | SSCL1, SSCL5, SSCL6, SSCL8, SSCL9 | I/O | Input/output pins for the I ² C clock. |
| | SSDA1, SSDA5, SSDA6, SSDA8, SSDA9 | I/O | Input/output pins for the I ² C data. |
| | • Simple SPI mode | | |
| | SCK1, SCK5, SCK6, SCK8, SCK9 | I/O | Input/output pins for the clock |
| | SMISO1, SMISO5, SMISO6, SMISO8, SMISO9 | I/O | Input/output pins for slave transmit data. |
| | SMOSI1, SMOSI5, SMOSI6, SMOSI8, SMOSI9 | I/O | Input/output pins for master transmit data. |
| | SS1#, SS5#, SS6#, SS8#, SS9# | Input | Chip-select input pins. |
| Serial communications interface (SCIh) | • Asynchronous mode/clock synchronous mode | | |
| | SCK12 | I/O | Input/output pin for the clock |
| | RXD12 | Input | Input pin for received data |
| | TXD12 | Output | Output pin for transmitted data |
| | CTS12# | Input | Input pin for controlling the start of transmission and reception |
| | RTS12# | Output | Output pin for controlling the start of transmission and reception |
| | • Simple I ² C mode | | |
| | SSCL12 | I/O | Input/output pin for the I ² C clock |
| | SSDA12 | I/O | Input/output pin for the I ² C data |

Table 1.4 Pin Functions (4/6)

| Classifications | Pin Name | I/O | Description | |
|--|--|---------|--|--|
| Serial communications interface (SCIh) | • Simple SPI mode | | | |
| | SCK12 | I/O | Input/output pin for the clock | |
| | SMISO12 | I/O | Input/output pin for slave transmission of data | |
| | SMOSI12 | I/O | Input/output pin for master transmission of data | |
| | SS12# | Input | Chip-select input pin | |
| | • Extended serial mode | | | |
| | RDX12 | Input | Input pin for received data | |
| | TXDX12 | Output | Output pin for transmitted data | |
| | SIOX12 | I/O | Input/output pin for received or transmitted data | |
| Serial communications interface (SCIi) | • Asynchronous mode/clock synchronous mode | | | |
| | SCK11 | I/O | Input/output pin for the clock | |
| | RXD11 | Input | Input pin for received data | |
| | TXD11 | Output | Output pin for transmitted data | |
| | CTS11# | Input | Input pin for controlling the start of transmission and reception | |
| | RTS11# | Output | Output pin for controlling the start of transmission and reception | |
| | • Simple I ² C mode | | | |
| | SSCL11 | I/O | Input/output pin for the I ² C clock | |
| | SSDA11 | I/O | Input/output pin for the I ² C data | |
| | • Simple SPI mode | | | |
| | SCK11 | I/O | Input/output pin for the clock | |
| | SMISO11 | I/O | Input/output pin for slave transmission of data | |
| | SMOSI11 | I/O | Input/output pin for master transmission of data | |
| | SS11# | Input | Chip-select input pin | |
| | I ² C bus interface | SCL | I/O | Input/output pin for I ² C bus interface clocks. Bus can be directly driven by the N-channel open drain output. |
| | | SDA | I/O | Input/output pin for I ² C bus interface data. Bus can be directly driven by the N-channel open drain output. |
| | USB 2.0 host/function module | VCC_USB | Input | Power supply pins |
| VSS_USB | | Input | Ground pins | |
| USB0_DP | | I/O | Input or output USB transceiver D+ data | |
| USB0_DM | | I/O | Input or output USB transceiver D- data. | |
| USB0_EXICEN | | Output | Connect to the OTG power IC. | |
| USB0_ID | | Input | Connect to the OTG power IC. | |
| USB0_VBUSEN | | Output | USB VBUS power enable pins | |
| USB0_OVRCURA, USB0_OVRCURB | | Input | USB overcurrent pins | |
| USB0_VBUS | | Input | USB cable connection/disconnection detection input pins | |
| CAN module | CRX | Input | Input pins | |
| | CTX | Output | Output pins | |
| Serial peripheral interface | RSPCKA | I/O | Input/output pin for the RSPI clock. | |
| | MOSIA | I/O | Input/output pin for transmitting data from the RSPI master. | |
| | MISOA | I/O | Input/output pin for transmitting data from the RSPI slave. | |
| | SSLA0 | I/O | Input/output pin to select the slave for the RSPI. | |
| | SSLA1 to SSLA3 | Output | Output pins to select the slave for the RSPI. | |

Table 1.4 Pin Functions (5/6)

| Classifications | Pin Name | I/O | Description |
|----------------------|---|--------|--|
| 12-bit A/D converter | AN000 to AN002, AN100 to AN102 | Input | Input pins for the analog signals to be processed by the A/D converter. (Positive side input at PGA pseudo-differential input.) |
| | AN003 to AN007, AN103 to AN107, AN200 to AN211, AN216 to AN217 | Input | Input pins for the analog signals to be processed by the A/D converter. |
| | ADST0, ADST1, ADST2 | Output | Output pins for A/D conversion status. |
| | ADTRG0#, ADTRG1#, ADTRG2# | Input | Input pins for the external trigger signals that start the A/D conversion. |
| | PGAVSS0, PGAVSS1 | Input | A common reference ground pin for PGA pseudo-differential input in the unit |
| 12-bit D/A converter | DA0, DA1 | Output | Output pins for the analog signals to be processed by the D/A converter |
| Comparator C | COMP0 to COMP5 | Output | Comparator detection result output pins. |
| | CVREFC0, CVREFC1 | Input | Analog reference voltage supply pins for comparator C. |
| | CMPCnm | Input | Analog input pin for CMPCnm (n = 0 to 5, m = 0 to 3) |
| Analog power supply | AVCC0 | — | Analog voltage supply pin for 12-bit A/D converter unit 0. Connect the AVCC0 pin to AVCC1 or AVCC2 when 12-bit A/D converter unit 0 is not used. |
| | AVSS0 | — | Analog ground pin for 12-bit A/D converter unit 0. Connect the AVSS0 pin to AVSS1 or AVSS2 when 12-bit A/D converter unit 0 is not used. |
| | AVCC1 | — | Analog voltage supply pin for 12-bit A/D converter unit 1. Connect this pin to AVCC0 when not using the 12-bit A/D converter 1 but using the 12-bit A/D converter 0. Connect this pin to AVCC2 when not using the 12-bit A/D converter 0 and the 12-bit A/D converter 1. |
| | AVSS1 | — | Analog ground pin for 12-bit A/D converter unit 1. Connect this pin to AVSS0 when not using the 12-bit A/D converter 1 but using the 12-bit A/D converter 0. Connect this pin to AVSS2 when not using the 12-bit A/D converter 0 and the 12-bit A/D converter 1. |
| | AVCC2 | — | Analog voltage supply pin for the 12-bit A/D converter unit 2, reference voltage supply pin for the 12-bit D/A converter, analog voltage supply pin for the comparator C, and analog voltage supply pin for the temperature sensor. Connect this pin to either of AVCC0 or AVCC1 when not using the 12-bit A/D converter unit 2, 12-bit D/A converter, comparator C, and temperature sensor. |
| | AVSS2 | — | Analog ground pin for the 12-bit A/D converter unit 2, reference ground pin for the D/A converter, analog ground pin for the comparator C, and analog ground pin for the temperature sensor. Connect this pin to either of AVSS0 or AVSS1 when not using the 12-bit A/D converter unit 2, 12-bit D/A converter, comparator C, and temperature sensor. |

Table 1.4 Pin Functions (6/6)

| Classifications | Pin Name | I/O | Description |
|-----------------|------------|-----|--|
| I/O ports | P00, P01 | I/O | 2-bit input/output pins. |
| | P10 to P17 | I/O | 8-bit input/output pins. |
| | P20 to P27 | I/O | 8-bit input/output pins. |
| | P30 to P37 | I/O | 8-bit input/output pins. |
| | P40 to P47 | I/O | 8-bit input/output pins (P40 to P42, P44 to P46: input). |
| | P50 to P55 | I/O | 6-bit input/output pins. |
| | P60 to P65 | I/O | 6-bit input/output pins. |
| | P70 to P76 | I/O | 7-bit input/output pins. |
| | P80 to P82 | I/O | 3-bit input/output pins. |
| | P90 to P96 | I/O | 7-bit input/output pins. |
| | PA0 to PA7 | I/O | 8-bit input/output pins. |
| | PB0 to PB7 | I/O | 8-bit input/output pins. |
| | PC0 to PC6 | I/O | 7-bit input/output pins. |
| | PD0 to PD7 | I/O | 8-bit input/output pins. |
| | PE0 to PE6 | I/O | 7-bit input/output pins (PE2: input). |
| | PF0 to PF3 | I/O | 4-bit input/output pins. |
| | PG0 to PG2 | I/O | 3-bit input/output pins. |
| | PH0 to PH7 | I/O | 8-bit input/output pins (PH0, PH4: input). |
| | PK0 to PK2 | I/O | 3-bit input/output pins. |

Note: When not using any of the A/D converter, D/A converter, comparator C and temperature sensor, connect the AVCC0, AVCC1 and AVCC2 pins to VCC, and connect the AVSS0, AVSS1 and AVSS2 pins to VSS, respectively.

Note: When the pin functions have "-DS" appended to their names, they can also be used as triggers for release from deep software standby.

1.5 Pin Assignments

Figure 1.3 to Figure 1.9 show the pin assignments. Table 1.5 to Table 1.11 show the lists of pins and pin functions.

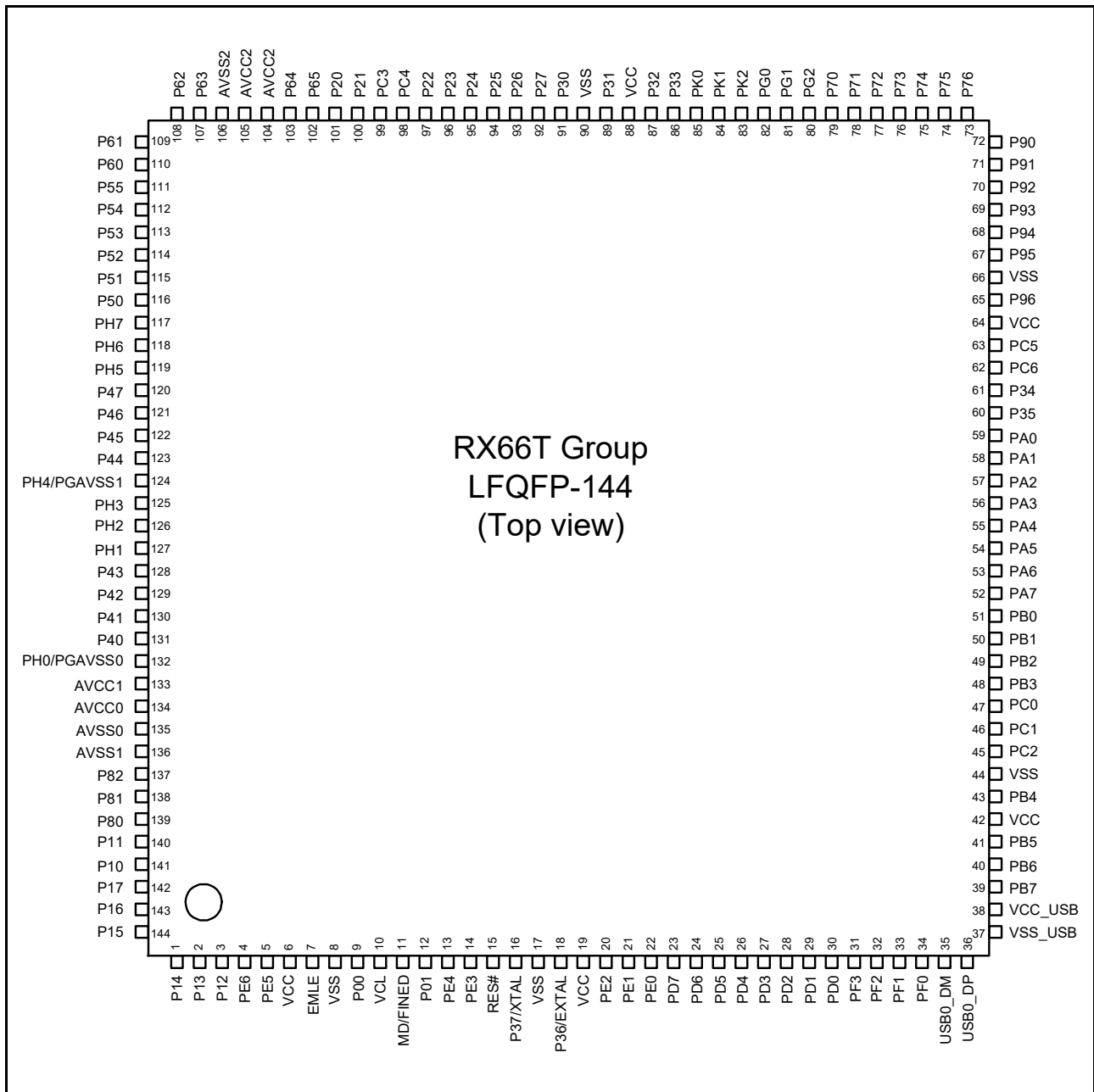


Figure 1.3 Pin Assignment (144-pin LQFP) with PGA pseudo-differential input and with USB pin

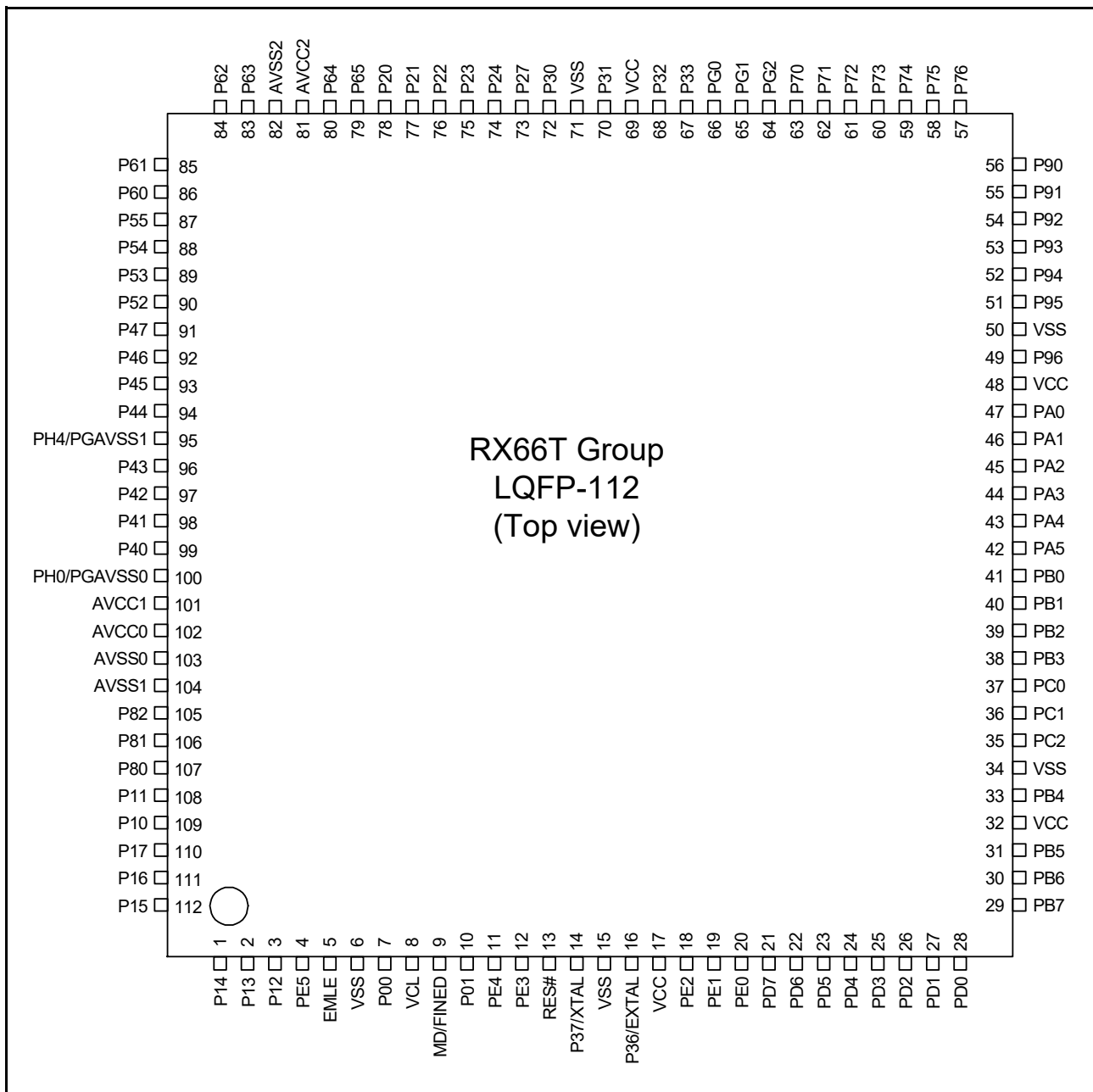


Figure 1.4 Pin Assignment (112-pin LQFP) with PGA pseudo-differential input and without USB pin

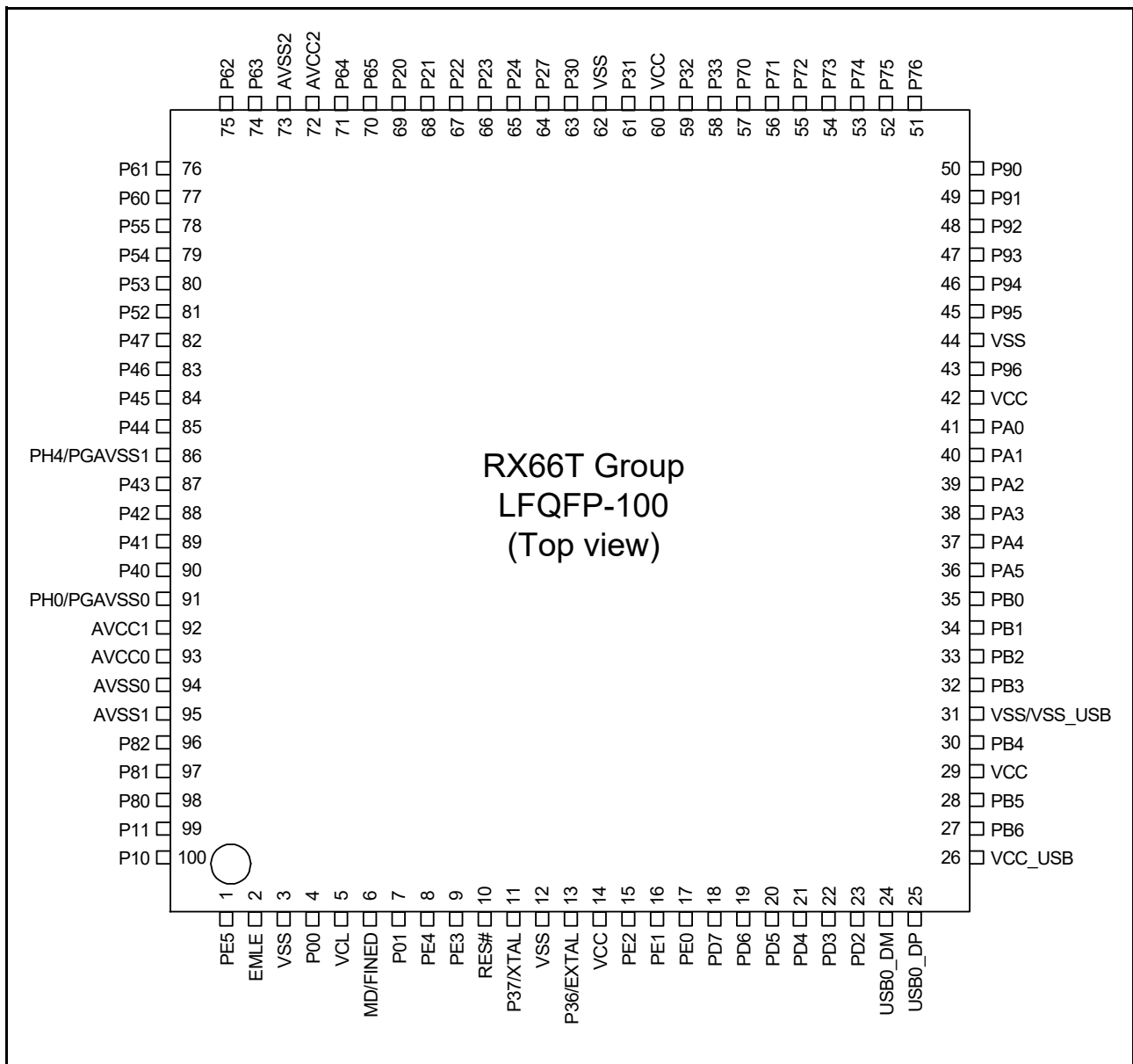


Figure 1.5 Pin Assignment (100-pin LQFP) with PGA pseudo-differential input and with USB pin

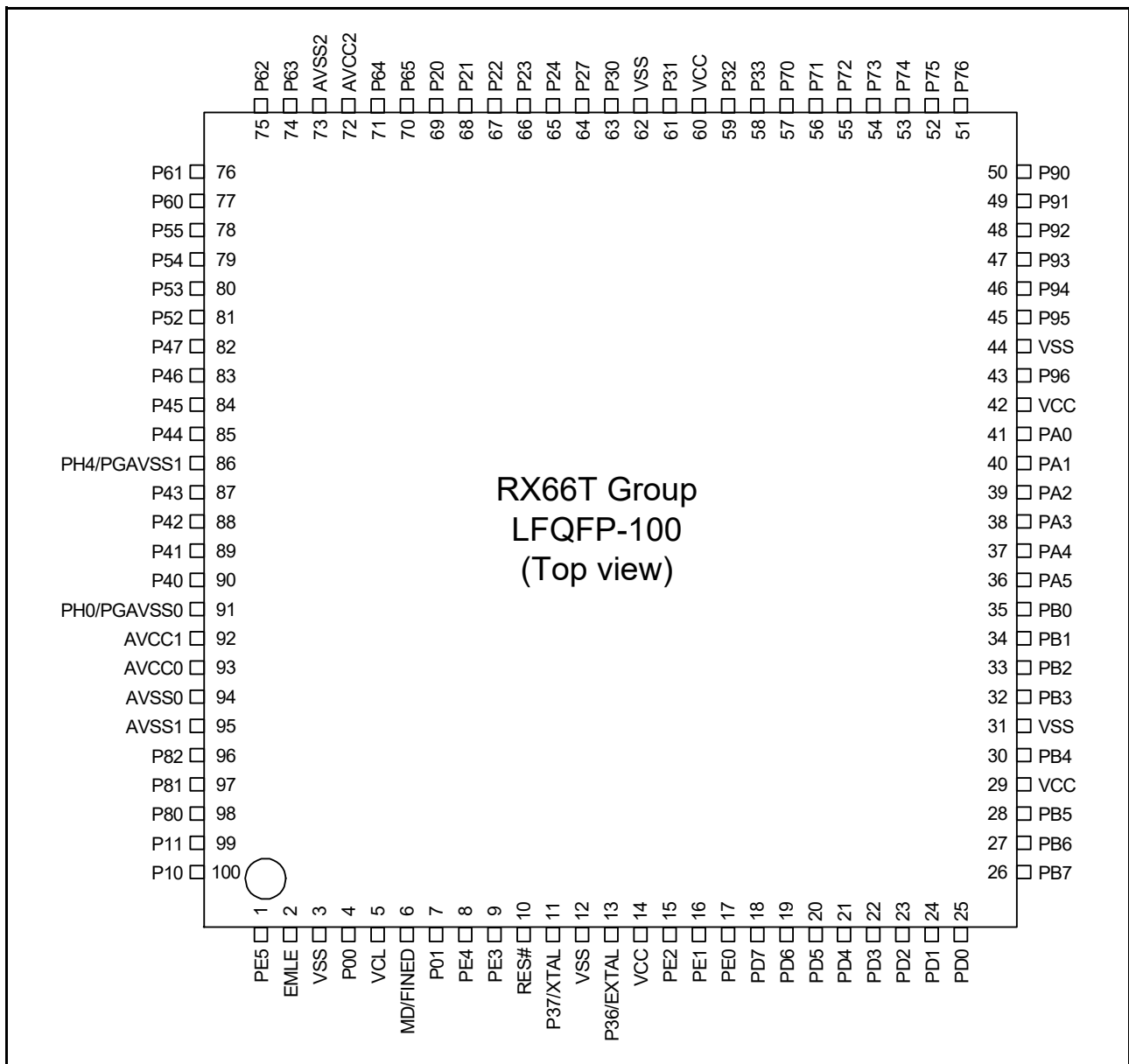


Figure 1.6 Pin Assignment (100-pin LQFP) with PGA pseudo-differential input and without USB pin

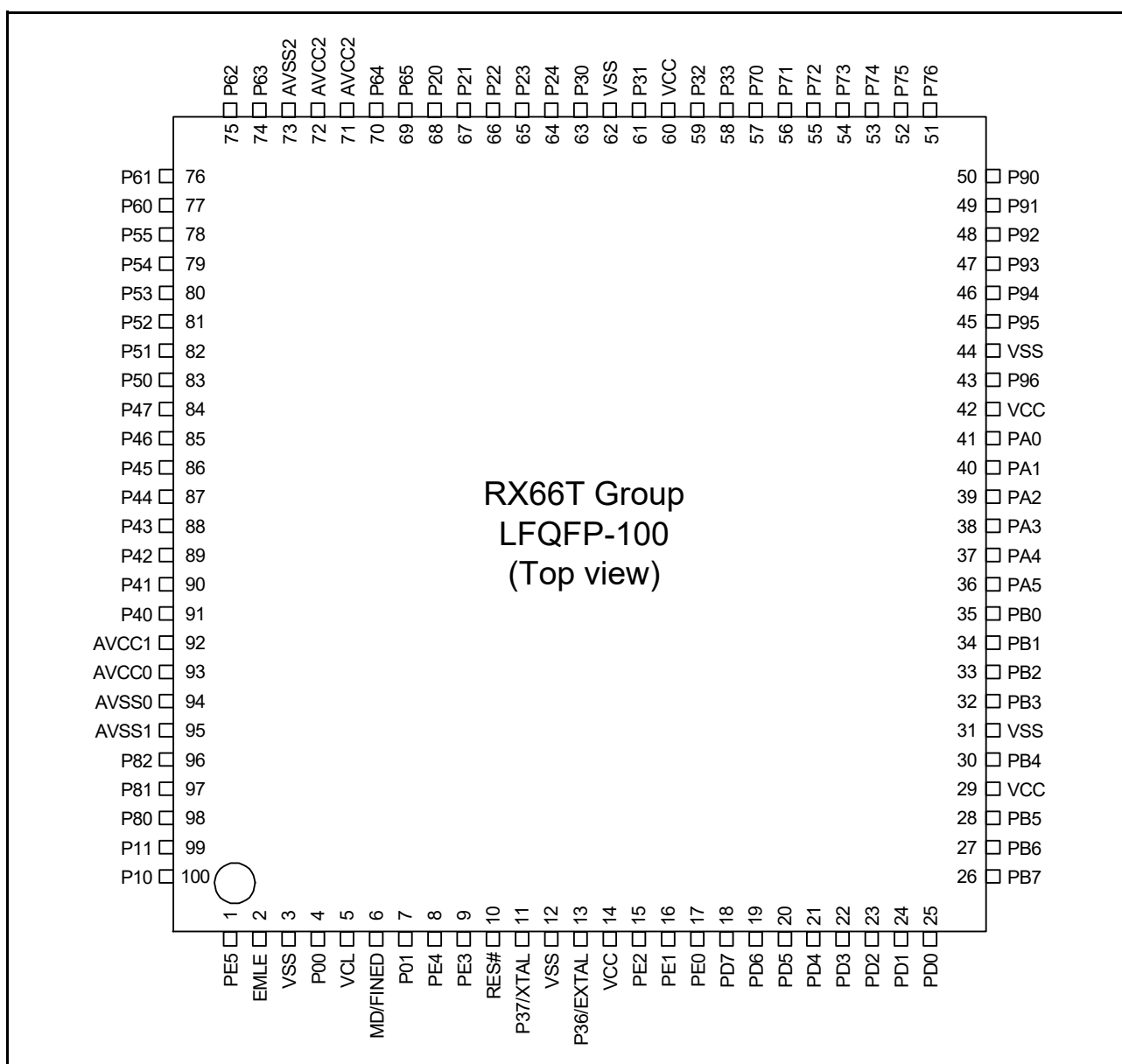


Figure 1.7 Pin Assignment (100-pin LQFP) without PGA pseudo-differential input and without USB pin

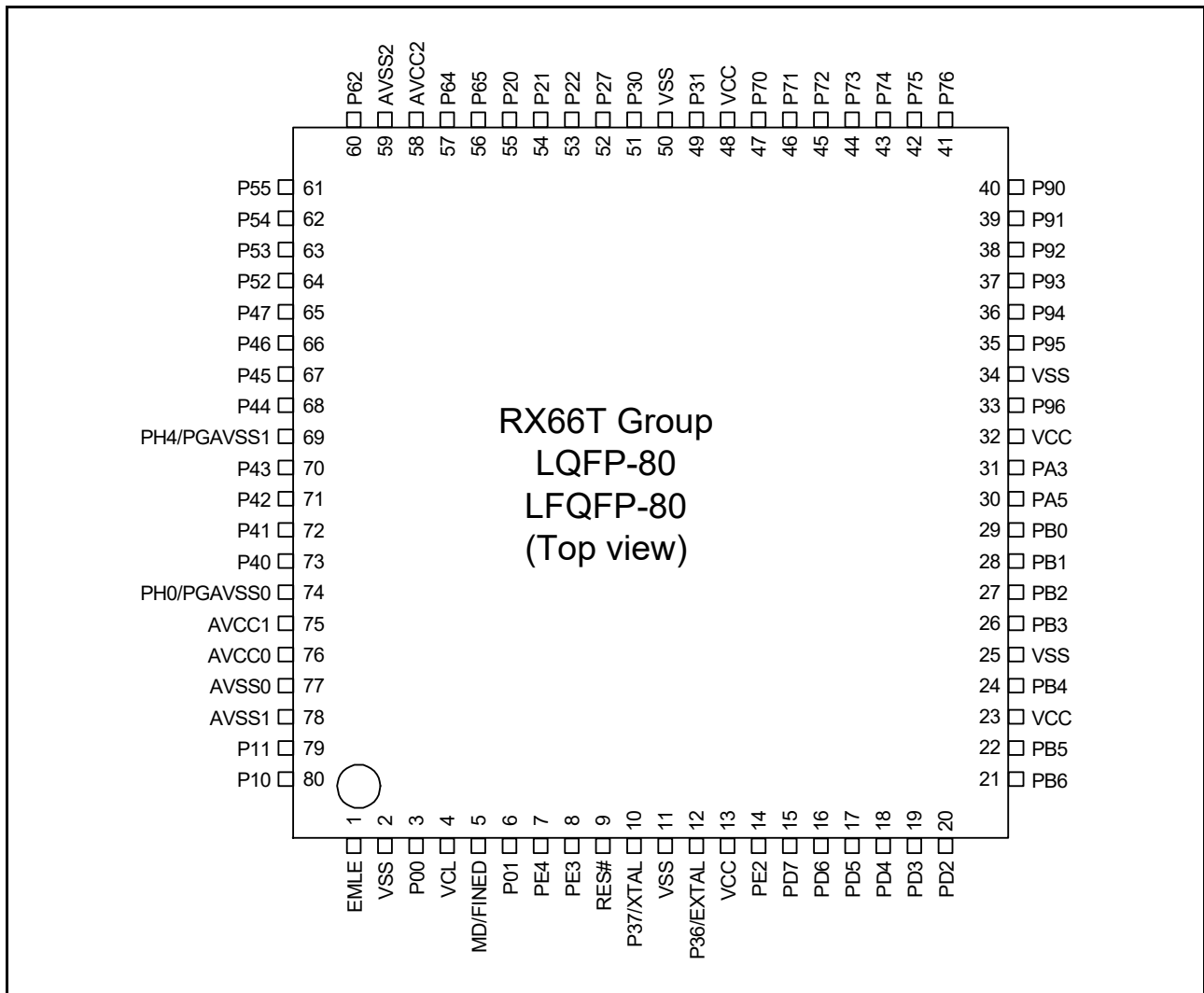


Figure 1.8 Pin Assignment (80-pin LQFP and LFQFP) with PGA pseudo-differential input and without USB pin

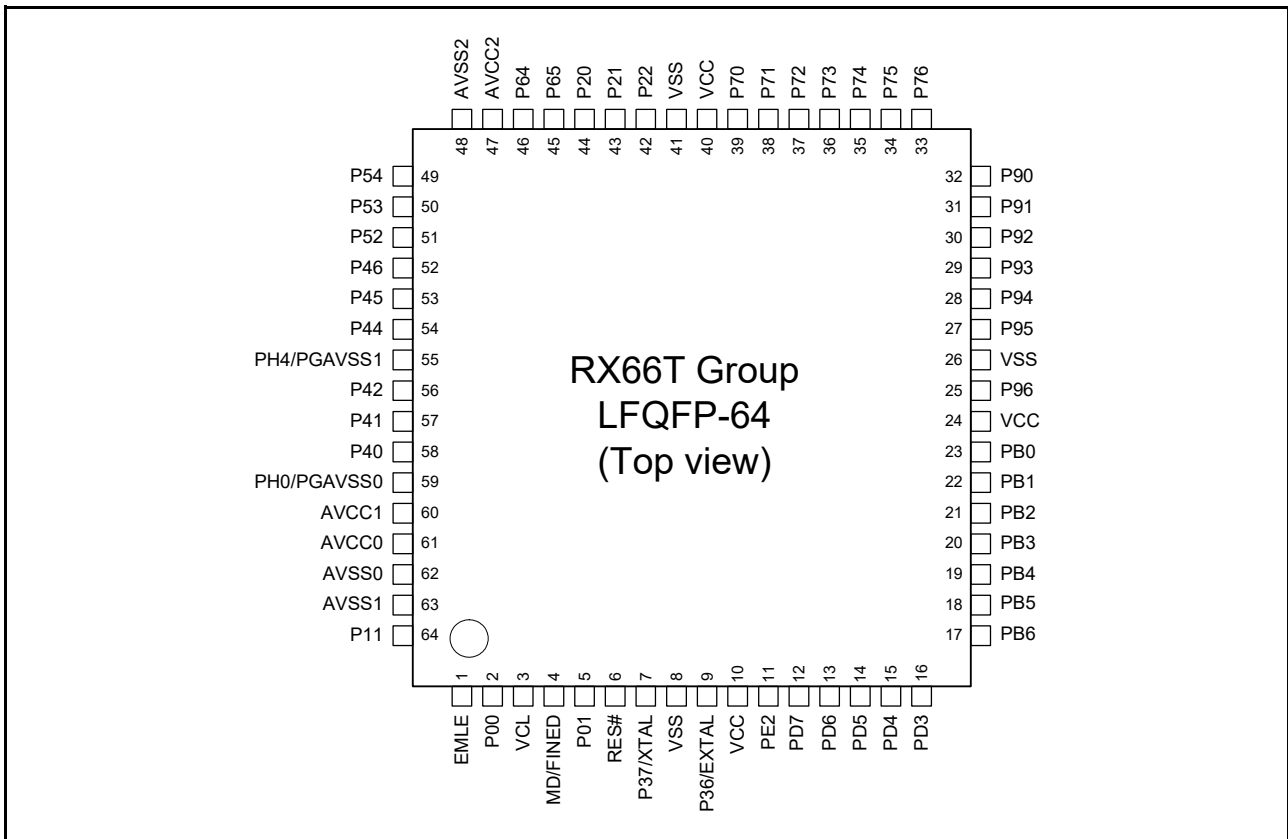


Figure 1.9 Pin Assignment (64-pin LQFP) with PGA pseudo-differential input and without USB pin

Table 1.5 List of Pin and Pin Functions (144-pin with PGA pseudo-differential input and with USB pin) (1/7)

| Pin Number 144-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Communica tions (USB) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|-------------------------|---|--|-----------------------------|-------------------------|--------|-----------------|
| 1 | | P14 | | MTIOC4B/ MTIOC4B#/ GTIOC2A/GTIOC9A/ GTIOC2A#/ GTIOC9A# | | | IRQ11 | | |
| 2 | | P13 | | MTIOC4A/ MTIOC4A#/ GTIOC1A/GTIOC8A/ GTIOC1A#/ GTIOC8A# | | | IRQ10 | | |
| 3 | | P12 | | MTIOC3B/ MTIOC3B#/ GTIOC0A/GTIOC7A/ GTIOC0A#/ GTIOC7A# | | | IRQ9 | | |
| 4 | | PE6 | RD# | GTETRG A/ GTETRG B/ GTETRG C/ GTETRG D/POE10# | | | IRQ3 | | |
| 5 | | PE5 | BCLK | MTIOC9D/ MTIOC9D#/ GTIOC3A/ GTETRG B/ GTIOC3A#/ GTETRG D | SCK9/CTS9#/ RTS9#/SS9# | | IRQ0 | | ADST0 |
| 6 | VCC | | | | | | | | |
| 7 | EMLE | | | | | | | | |
| 8 | VSS | | | | | | | | |
| 9 | UB | P00 | A11 | MTIOC9A/ MTIOC9A#/CACREF | RXD9/SMISO9/ SSCL9/RXD12/ SMISO12/SSCL12/ RXDX12 | | IRQ2 | | ADST1/ COMP0 |
| 10 | VCL | | | | | | | | |
| 11 | MD/FINED | | | | | | | | |
| 12 | | P01 | A10 | MTIOC9C/ MTIOC9C#/ GTETRG A/ GTETRG B/ GTETRG C/ GTETRG D/POE12# | TXD9/SMOSI9/ SSDA9/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12 | | IRQ4 | | ADST2/ COMP1 |
| 13 | | PE4 | A9 | MTCLKC/MTCLKC#/ GTETRG A/ GTETRG B/ GTETRG C/ GTETRG D/POE10# | SCK9 | | IRQ1 | | |
| 14 | | PE3 | A8 | MTCLKD/MTCLKD#/ GTETRG A/ GTETRG B/ GTETRG C/ GTETRG D/POE11# | CTS9#/RTS9#/ SS9# | | IRQ2-DS | | |
| 15 | RES# | | | | | | | | |
| 16 | XTAL | P37 | | | | | | | |
| 17 | VSS | | | | | | | | |
| 18 | EXTAL | P36 | | | | | | | |
| 19 | VCC | | | | | | | | |
| 20 | UPSEL | PE2 | | POE10# | | | NMI | | |
| 21 | | PE1 | WR0#/WR# | MTIOC9D/ MTIOC9D#/TMO5 | CTS5#/RTS5#/ SS5#/CTS12#/ RTS12#/SS12#/ SSLA3 | | IRQ15 | | |
| 22 | | PE0 | WR1#/ BC1#/ WAIT# | MTIOC9B/ MTIOC9B#/TMC11/ TMC15 | RXD5/SMISO5/ SSCL5/SSLA2/ CRX0 | USB0_OVR CURB | IRQ7 | | |

Table 1.5 List of Pin and Pin Functions (144-pin with PGA pseudo-differential input and with USB pin) (2/7)

| Pin Number 144-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Communica tions (USB) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|----------|--|--|-----------------------------|-------------------------|--------|--------|
| 23 | TRST# | PD7 | | MTIOC9A/ MTIOC9A#/ GTIOC0A/GTIOC3A/ GTIOC0A#/ GTIOC3A#/TMR11/ TMR15 | TXD5/SMOSI5/ SSDA5/SSLA1/ CTX0 | | IRQ8 | | |
| 24 | TMS | PD6 | | MTIOC9C/ MTIOC9C#/ GTIOC0B/GTIOC3B/ GTIOC0B#/ GTIOC3B#/TMO1 | CTS1#/RTS1#/ SS1#/CTS11#/ RTS11#/SS11#/ SSLA0 | | IRQ5 | | ADST0 |
| 25 | TDI | PD5 | | GTIOC1A/ GTETRG A/ GTIOC1A#/TMR10/ TMR16 | RXD1/SMISO1/ SSCL1/RXD11/ SMISO11/SSCL11 | | IRQ6 | | |
| 26 | TCK | PD4 | | GTIOC1B/ GTETRGB/ GTIOC1B#/TMC10/ TMC16 | SCK1/SCK11 | | IRQ2 | | |
| 27 | TDO | PD3 | | GTIOC2A/ GTETRGC/ GTIOC2A#/TMO0 | TXD1/SMOSI1/ SSDA1/TXD11/ SMOSI11/SSDA11 | | | | |
| 28 | TRCLK | PD2 | A7 | GTIOC2B/GTIOC0A/ GTIOC2B#/ GTIOC0A#/TMC11/ TMO4 | SCK5/SCK8/ MOSIA | USB0_VBUS | | | |
| 29 | TRDATA3 | PD1 | A6 | GTIOC3A/GTIOC0B/ GTIOC3A#/ GTIOC0B#/TMO2 | RXD8/SMISO8/ SSCL8/MISOA | | | | |
| 30 | TRDATA2 | PD0 | A5 | GTIOC3B/GTIOC1A/ GTIOC3B#/ GTIOC1A#/TMO6 | TXD8/SMOSI8/ SSDA8/RSPCKA | | | | |
| 31 | TRDATA7 | PF3 | A19/CS3# | GTETRG A/TMO7 | CTS11#/RTS11#/ SS11#/CRX0 | | IRQ14 | | COMP0 |
| 32 | TRDATA6 | PF2 | A18/CS2# | GTETRGB/TMO3 | SCK11/CTX0 | | IRQ5 | | COMP1 |
| 33 | TRDATA5 | PF1 | A17/CS1# | GTETRGC/TMO5 | RXD11/SMISO11/ SSCL11 | | IRQ13 | | COMP2 |
| 34 | TRDATA4 | PF0 | A0/BC0# | GTETRGD/TMO1 | TXD11/SMOSI11/ SSDA11 | | IRQ12 | | COMP3 |
| 35 | | | | | | USB0_DM | | | |
| 36 | | | | | | USB0_DP | | | |
| 37 | VSS_USB | | | | | | | | |
| 38 | VCC_USB | | | | | | | | |
| 39 | TRDATA1 | PB7 | A4 | GTIOC1B/ GTIOC1B# | SCK5/SCK11/ SCK12 | USB0_OVR CURB | | | |
| 40 | TRDATA0 | PB6 | A3 | GTIOC2A/ GTIOC2A# | RXD5/SMISO5/ SSCL5/RXD11/ SMISO11/SSCL11/ RXD12/SMISO12/ SSCL12/RXDX12/ CRX0 | USB0_OVR CURA | IRQ2 | | |
| 41 | TRSYNC | PB5 | A2 | GTIOC2B/ GTIOC2B# | TXD5/SMOSI5/ SSDA5/TXD11/ SMOSI11/SSDA11/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/CTX0 | USB0_VBUS EN | | | |
| 42 | VCC | | | | | | | | |
| 43 | TRSYNC1 | PB4 | A1 | GTETRG A/ GTETRGB/ GTETRGC/ GTETRGD/POE8# | CTS5#/RTS5#/ SS5#/SCK11/ CTS11#/RTS11#/ SS11# | USB0_OVR CURB | IRQ3-DS | | |
| 44 | VSS | | | | | | | | |

Table 1.5 List of Pin and Pin Functions (144-pin with PGA pseudo-differential input and with USB pin) (3/7)

| Pin Number 144-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Communica tions (USB) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|------------|--|--|-------------------------------------|-------------------------|--------|-----------------|
| 45 | | PC2 | CS1# | MTIOC0D/ MTIOC0D#/ GTADSM0 | SCK8 | USB0_ID/ USB0_OVR CURA | IRQ15 | | ADSM0/ COMP5 |
| 46 | | PC1 | A16 | MTIOC0C/ MTIOC0C#/ GTADSM1 | TXD8/SMOSI8/ SSDA8 | USB0_EXIC EN/ USB0_VBUS EN | IRQ13 | | ADSM1/ COMP4 |
| 47 | | PC0 | CS0# | MTIOC0B/ MTIOC0B# | RXD8/SMISO8/ SSCL8 | USB0_VBUS | IRQ12 | | COMP3 |
| 48 | | PB3 | A7 | MTIOC0A/ MTIOC0A#/ CACREF | SCK6/RSPCKA | | IRQ9 | | |
| 49 | | PB2 | A6 | MTIOC0B/ MTIOC0B#/ GTADSM0/TMRI0 | TXD6/SMOSI6/ SSDA6/SDA | | | | ADSM0 |
| 50 | | PB1 | A5 | MTIOC0C/ MTIOC0C#/ GTADSM1/TMCI0 | RXD6/SMISO6/ SSCL6/SCL | | IRQ4 | | ADSM1 |
| 51 | | PB0 | A0/BC0#/A4 | MTIOC0D/ MTIOC0D#/ TMO0 | TXD6/SMOSI6/ SSDA6/CTS11#/ RTS11#/SS11#/ MOSIA | | IRQ8 | | ADTRG2# |
| 52 | | PA7 | A15 | MTCLKA/MTCLKC/ MTCLKA#/ MTCLKC#/ GTADSM0/TMO2 | RXD11/SMISO11/ SSCL11/RXD12/ SMISO12/SSCL12/ RXDX12/CRX0 | | | | ADSM0 |
| 53 | | PA6 | A14 | MTCLKB/MTCLKD/ MTCLKB#/ MTCLKD#/ GTADSM1/TMO6 | TXD11/SMOSI11/ SSDA11/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/ CTX0 | | IRQ7 | | ADSM1 |
| 54 | | PA5 | A3 | MTIOC1A/ MTIOC1A#/ TMCI3 | RXD6/SMISO6/ SSCL6/RXD8/ SMISO8/SSCL8/ MISOA | | IRQ1 | | ADTRG1# |
| 55 | | PA4 | A2 | MTIOC1B/ MTIOC1B#/ TMCI7 | SCK6/TXD8/ SMOSI8/SSDA8/ RSPCKA | | | | ADTRG0# |
| 56 | | PA3 | A1 | MTIOC2A/ MTIOC2A#/ GTADSM0/TMRI7 | TXD9/SMOSI9/ SSDA9/SCK8/ SSLA0 | | | | |
| 57 | | PA2 | A0/BC0# | MTIOC2B/ MTIOC2B#/ GTADSM1/TMO7 | CTS6#/RTS6#/ SS6#/RXD9/ SMISO9/SSCL9/ SCK11/SSLA1 | | | | |
| 58 | | PA1 | | MTIOC6A/ MTIOC6A#/ TMO4 | TXD9/SMOSI9/ SSDA9/RXD11/ SMISO11/SSCL11/ SSLA2/CRX0 | USB0_ID/ USB0_OVR CURA | IRQ14-DS | | ADTRG0# |
| 59 | | PA0 | | MTIOC6C/ MTIOC6C#/ TMO2 | SCK9/TXD11/ SMOSI11/SSDA11/ SSLA3/CTX0 | USB0_EXIC EN/ USB0_VBUS EN | | | |
| 60 | | P35 | A13 | MTIOC2A/MTIOC9A/ MTIOC2A#/ MTIOC9A#/ GTADSM0/TMO0 | CTS8#/RTS8#/ SS8#/TXD1/ SMOSI1/SSDA1 | | IRQ6 | | |
| 61 | | P34 | A12 | MTIOC2B/MTIOC9B/ MTIOC2B#/ MTIOC9B#/ GTADSM1/ GTETRGB/TMO4 | CTS9#/RTS9#/ SS9#/RXD1/ SMISO1/SSCL1 | USB0_OVR CURB | IRQ3 | | |
| 62 | | PC6 | | MTIOC1A/MTIOC9C/ MTIOC1A#/ MTIOC9C# | RXD11/SMISO11/ SSCL11/CRX0 | | IRQ11-DS | | |

Table 1.5 List of Pin and Pin Functions (144-pin with PGA pseudo-differential input and with USB pin) (4/7)

| Pin Number 144-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Communica tions (USB) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|----------------|--|---|-----------------------------|-------------------------|--------|--------|
| 63 | | PC5 | | MTIOC1B/MTIOC9D/ MTIOC1B#/ MTIOC9D# | TXD11/SMOSI11/ SSDA11/CTX0 | | IRQ10-DS | | |
| 64 | VCC | | | | | | | | |
| 65 | | P96 | CS0#/ WAIT# | GTETRGA/ GTETRGB/ GTETRCG/ GTETRGD/POE4# | CTS8#/RTS8#/ SS8# | | IRQ4-DS | | |
| 66 | VSS | | | | | | | | |
| 67 | | P95 | | MTIOC6B/ MTIOC6B#/ GTIOC4A/GTIOC7A/ GTIOC4A#/ GTIOC7A# | | | | | |
| 68 | | P94 | | MTIOC7A/ MTIOC7A#/ GTIOC5A/GTIOC8A/ GTIOC5A#/ GTIOC8A# | | | | | |
| 69 | | P93 | | MTIOC7B/ MTIOC7B#/ GTIOC6A/GTIOC9A/ GTIOC6A#/ GTIOC9A# | | | | | |
| 70 | | P92 | | MTIOC6D/ MTIOC6D#/ GTIOC4B/GTIOC7B/ GTIOC4B#/ GTIOC7B# | | | | | |
| 71 | | P91 | | MTIOC7C/ MTIOC7C#/ GTIOC5B/GTIOC8B/ GTIOC5B#/ GTIOC8B# | | | | | |
| 72 | | P90 | | MTIOC7D/ MTIOC7D#/ GTIOC6B/GTIOC9B/ GTIOC6B#/ GTIOC9B# | | | | | |
| 73 | | P76 | D0 [A0/D0] | MTIOC4D/ MTIOC4D#/ GTIOC2B/GTIOC6B/ GTIOC2B#/ GTIOC6B# | | | | | |
| 74 | | P75 | D1 [A1/D1] | MTIOC4C/ MTIOC4C#/ GTIOC1B/GTIOC5B/ GTIOC1B#/ GTIOC5B# | | | | | |
| 75 | | P74 | D2 [A2/D2] | MTIOC3D/ MTIOC3D#/ GTIOC0B/GTIOC4B/ GTIOC0B#/ GTIOC4B# | | | | | |
| 76 | | P73 | D3 [A3/D3] | MTIOC4B/ MTIOC4B#/ GTIOC2A/GTIOC6A/ GTIOC2A#/ GTIOC6A# | | | | | |
| 77 | | P72 | D4 [A4/D4] | MTIOC4A/ MTIOC4A#/ GTIOC1A/GTIOC5A/ GTIOC1A#/ GTIOC5A# | | | | | |

Table 1.5 List of Pin and Pin Functions (144-pin with PGA pseudo-differential input and with USB pin) (5/7)

| Pin Number 144-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Communica tions (USB) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|-------------------|--|---|-----------------------------|-------------------------|--------|-------------------|
| 78 | | P71 | D5 [A5/D5] | MTIOC3B/ MTIOC3B#/ GTIOC0A/GTIOC4A/ GTIOC0A#/ GTIOC4A# | | | | | |
| 79 | | P70 | D6 [A6/D6] | GTETRG A/ GTETRG B/ GTETRG C/ GTETRG D/POE0# | CTS9#/RTS9#/ SS9# | | IRQ5-DS | | |
| 80 | | PG2 | D11 [A11/ D11] | GTETRG A/ GTIOC0B/ GTIOC0B# | SCK9 | | IRQ2 | | COMP0 |
| 81 | | PG1 | D12 [A12/ D12] | GTIOC0A/ GTIOC0A# | TXD9/SMOSI9/ SSDA9 | | IRQ1 | | COMP1 |
| 82 | | PG0 | D13 [A13/ D13] | GTIOC1B/ GTIOC1B# | RXD9/SMISO9/ SSCL9 | | IRQ0 | | COMP2 |
| 83 | | PK2 | D14 [A14/ D14] | GTIOC1A/ GTIOC1A#/POE12# | CTS9#/RTS9#/ SS9#/SCK5 | | IRQ9-DS | | COMP3 |
| 84 | | PK1 | D15 [A15/ D15] | GTIOC2B/ GTIOC2B#/POE13# | CTS8#/RTS8#/ SS8#/TXD5/ SMOSI5/SSDA5 | | IRQ8-DS | | COMP4 |
| 85 | | PK0 | CS1# | GTIOC2A/ GTIOC2A#/POE14# | RXD5/SMISO5/ SSCL5 | | IRQ15-DS | | COMP5 |
| 86 | | P33 | D7 [A7/D7] | MTIOC3A/MTCLKA/ MTIOC3A#/ MTCLKA#/GTIOC3B/ GTIOC3B#/TMO0 | SSLA3 | | IRQ13-DS | | |
| 87 | | P32 | D8 [A8/D8] | MTIOC3C/MTCLKB/ MTIOC3C#/ MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6 | SSLA2 | | IRQ12-DS | | |
| 88 | VCC | | | | | | | | |
| 89 | | P31 | D9 [A9/D9] | MTIOC0A/MTCLKC/ MTIOC0A#/ MTCLKC#/TMRI6 | SSLA1 | | IRQ6 | | |
| 90 | VSS | | | | | | | | |
| 91 | | P30 | D10 [A10/ D10] | MTIOC0B/MTCLKD/ MTIOC0B#/ MTCLKD#/TMCI6 | SCK8/CTS8#/ RTS8#/SS8#/ SSLA0 | | IRQ7 | | COMP3 |
| 92 | | P27 | CS3# | MTIOC1A/MTIOC0C/ MTIOC1A#/ MTIOC0C#/POE9# | | | IRQ15 | | |
| 93 | | P26 | CS2# | MTIOC9A/ MTIOC9A# | CTS1#/RTS1#/ SS1# | | IRQ11 | | ADST0 |
| 94 | | P25 | CS3# | MTIOC9C/ MTIOC9C# | SCK1 | | IRQ10 | | ADST1 |
| 95 | | P24 | D11 [A11/ D11] | MTIC5U/MTIC5U#/ TMCI2/TMO6 | CTS8#/RTS8#/ SS8#/SCK8/ RSPCKA | | IRQ4 | | COMP0 |
| 96 | | P23 | D12 [A12/ D12] | MTIC5V/MTIC5V#/ TMO2/CACREF | TXD8/SMOSI8/ SSDA8/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/ MOSIA/CTX0 | | IRQ11 | | COMP1 |
| 97 | | P22 | D13 [A13/ D13] | MTIC5W/MTCLKD/ MTIC5W#/ MTCLKD#/ MTIOC9B/TMRI2/ TMO4 | RXD8/SMISO8/ SSCL8/RXD12/ SMISO12/SSCL12/ RXDX12/MISOA/ CRX0 | | IRQ10 | | ADTRG2#/ COMP2 |
| 98 | | PC4 | A20 | MTIOC9B/ MTIOC9B# | TXD1/SMOSI1/ SSDA1/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12 | | | | ADST2/ COMP5 |

Table 1.5 List of Pin and Pin Functions (144-pin with PGA pseudo-differential input and with USB pin) (6/7)

| Pin Number 144-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Communica tions (USB) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|-------------------|---|--|-----------------------------|-------------------------|-----------------------------|-------------------|
| 99 | | PC3 | | MTIOC9D/ MTIOC9D# | RXD1/SMISO1/ SSCL1/RXD12/ SMISO12/SSCL12/ RXDX12 | | IRQ14 | | COMP4 |
| 100 | | P21 | D14 [A14/ D14] | MTIOC9A/MTCLKA/ MTIOC9A#/ MTCLKA#/TMC14 | TXD8/SMOSI8/ SSDA8/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/ MOSIA | | IRQ6-DS | AN217 | ADTRG1#/ COMP5 |
| 101 | | P20 | D15 [A15/ D15] | MTIOC9C/MTCLKB/ MTIOC9C#/ MTCLKB#/TMR14 | CTS8#/RTS8#/ SS8#/SCK8/ RSPCKA | | IRQ7-DS | AN216 | ADTRG0#/ COMP4 |
| 102 | | P65 | A12 | | | | IRQ9 | AN211/ CMPC53/ DA1 | |
| 103 | | P64 | A13 | | | | IRQ8 | AN210/ CMPC33/ DA0 | |
| 104 | AVCC2 | | | | | | | | |
| 105 | AVCC2 | | | | | | | | |
| 106 | AVSS2 | | | | | | | | |
| 107 | | P63 | A14/A12 | | | | IRQ7 | AN209/ CMPC23 | |
| 108 | | P62 | A15/A13 | | | | IRQ6 | AN208/ CMPC43 | |
| 109 | | P61 | A16/A14 | | | | IRQ5 | AN207/ CMPC13 | |
| 110 | | P60 | A17/A15 | | | | IRQ4 | AN206/ CMPC03 | |
| 111 | | P55 | A18/A16 | | | | IRQ3 | AN203/ CMPC32 | |
| 112 | | P54 | A19/A17 | | | | IRQ2 | AN202/ CMPC22 | |
| 113 | | P53 | A20/A18 | | | | IRQ1 | AN201/ CMPC12 | |
| 114 | | P52 | | | | | IRQ0 | AN200/ CMPC02 | |
| 115 | | P51 | | | | | | AN205/ CMPC52 | |
| 116 | | P50 | | | | | | AN204/ CMPC42 | |
| 117 | | PH7 | | | | | | AN106/ CVREFC1 | |
| 118 | | PH6 | | | | | | AN105 | |
| 119 | | PH5 | | | | | | AN104 | |
| 120 | | P47 | | | | | | AN103 | |
| 121 | | P46 | | | | | | AN102/ CMPC50/ CMPC51 | |
| 122 | | P45 | | | | | | AN101/ CMPC40/ CMPC41 | |
| 123 | | P44 | | | | | | AN100/ CMPC30/ CMPC31 | |
| 124 | | PH4 | | | | | | AN107/ PGAVSS1 | |
| 125 | | PH3 | | | | | | AN006/ CVREFC0 | |
| 126 | | PH2 | | | | | | AN005 | |

Table 1.5 List of Pin and Pin Functions (144-pin with PGA pseudo-differential input and with USB pin) (7/7)

| Pin Number 144-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Communica tions (USB) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|-----------|---|--|-----------------------------|-------------------------|-----------------------------|--------|
| 127 | | PH1 | | | | | | AN004 | |
| 128 | | P43 | | | | | | AN003 | |
| 129 | | P42 | | | | | | AN002/ CMPC20/ CMPC21 | |
| 130 | | P41 | | | | | | AN001/ CMPC10/ CMPC11 | |
| 131 | | P40 | | | | | | AN000/ CMPC00/ CMPC01 | |
| 132 | | PH0 | | | | | | AN007/ PGAVSS0 | |
| 133 | AVCC1 | | | | | | | | |
| 134 | AVCC0 | | | | | | | | |
| 135 | AVSS0 | | | | | | | | |
| 136 | AVSS1 | | | | | | | | |
| 137 | | P82 | ALE/WAIT# | MTIC5U/MTIC5U#/ TMO4 | SCK6/SCK12 | | IRQ3 | | COMP5 |
| 138 | | P81 | CS2# | MTIC5V/MTIC5V#/ TMC14 | TXD6/SMOSI6/ SSDA6/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12 | | | | COMP4 |
| 139 | | P80 | CS1# | MTIC5W/MTIC5W#/ TMR14 | RXD6/SMISO6/ SSCL6/RXD12/ SMISO12/SSCL12/ RXDX12 | | IRQ5 | | COMP3 |
| 140 | | P11 | RD# | MTIOC3A/MTCLKC/ MTIOC3A#/ MTCLKC#/ MTIOC9D/GTIOC3B/ GTETRGA/ GTIOC3B#/ GTETRGC/TMO3/ POE9# | | | IRQ1-DS | | |
| 141 | | P10 | | MTIOC9B/MTCLKD/ MTIOC9B#/ MTCLKD#/ GTETRGA/ GTETRGD/TMR13/ POE12# | CTS6#/RTS6#/ SS6# | | IRQ0-DS | | |
| 142 | | P17 | | MTIOC4D/ MTIOC4D#/ GTIOC2B/GTIOC9B/ GTIOC2B#/ GTIOC9B# | | | IRQ14 | | |
| 143 | | P16 | | MTIOC4C/ MTIOC4C#/ GTIOC1B/GTIOC8B/ GTIOC1B#/ GTIOC8B# | | | IRQ13 | | |
| 144 | | P15 | | MTIOC3D/ MTIOC3D#/ GTIOC0B/GTIOC7B/ GTIOC0B#/ GTIOC7B# | | | IRQ12 | | |

Table 1.6 List of Pin and Pin Functions (112-pin with PGA pseudo-differential input and without USB pin) (1/5)

| Pin Number 112-pin LQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|-------------------------------|---|----------|---------------------|--|---|-------------------------|--------|-----------------|
| 1 | | P14 | | MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC9A/ GTIOC2A#/GTIOC9A# | | IRQ11 | | |
| 2 | | P13 | | MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC8A/ GTIOC1A#/GTIOC8A# | | IRQ10 | | |
| 3 | | P12 | | MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC7A/ GTIOC0A#/GTIOC7A# | | IRQ9 | | |
| 4 | | PE5 | BCLK | MTIOC9D/MTIOC9D#/ GTIOC3A/GTETRGB/ GTIOC3A#/GTETRGD | SCK9/CTS9#/RTS9#/ SS9# | IRQ0 | | ADST0 |
| 5 | EMLE | | | | | | | |
| 6 | VSS | | | | | | | |
| 7 | UB | P00 | A11 | MTIOC9A/MTIOC9A#/ CACREF | RXD9/SMISO9/SSCL9/ RXD12/SMISO12/ SSCL12/RXD12 | IRQ2 | | ADST1/ COMP0 |
| 8 | VCL | | | | | | | |
| 9 | MD/FINED | | | | | | | |
| 10 | | P01 | A10 | MTIOC9C/MTIOC9C#/ GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE12# | TXD9/SMOSI9/SSDA9/ TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12 | IRQ4 | | ADST2/ COMP1 |
| 11 | | PE4 | A9 | MTCLKC/MTCLKC#/ GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE10# | SCK9 | IRQ1 | | |
| 12 | | PE3 | A8 | MTCLKD/MTCLKD#/ GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE11# | CTS9#/RTS9#/SS9# | IRQ2-DS | | |
| 13 | RES# | | | | | | | |
| 14 | XTAL | P37 | | | | | | |
| 15 | VSS | | | | | | | |
| 16 | EXTAL | P36 | | | | | | |
| 17 | VCC | | | | | | | |
| 18 | | PE2 | | POE10# | | NMI | | |
| 19 | | PE1 | WR0#/WR# | MTIOC9D/MTIOC9D#/ TMO5 | CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/ SS12#/SSLA3 | IRQ15 | | |
| 20 | | PE0 | WR1#/BC1#/ WAIT# | MTIOC9B/MTIOC9B#/ TMCI1/TMCI5 | RXD5/SMISO5/SSCL5/ SSLA2/CRX0 | IRQ7 | | |
| 21 | TRST# | PD7 | | MTIOC9A/MTIOC9A#/ GTIOC0A/GTIOC3A/ GTIOC0A#/GTIOC3A#/ TMR11/TMR15 | TXD5/SMOSI5/SSDA5/ SSLA1/CTX0 | IRQ8 | | |
| 22 | TMS | PD6 | | MTIOC9C/MTIOC9C#/ GTIOC0B/GTIOC3B/ GTIOC0B#/GTIOC3B#/ TMO1 | CTS1#/RTS1#/SS1#/ CTS11#/RTS11#/ SS11#/SSLA0 | IRQ5 | | ADST0 |
| 23 | TDI | PD5 | | GTIOC1A/GTETRGA/ GTIOC1A#/TMR10/ TMR16 | RXD1/SMISO1/SSCL1/ RXD11/SMISO11/ SSCL11 | IRQ6 | | |
| 24 | TCK | PD4 | | GTIOC1B/GTETRGB/ GTIOC1B#/TMCI0/ TMCI6 | SCK1/SCK11 | IRQ2 | | |
| 25 | TDO | PD3 | | GTIOC2A/GTETRGC/ GTIOC2A#/TMO0 | TXD1/SMOSI1/SSDA1/ TXD11/SMOSI11/ SSDA11 | | | |

Table 1.6 List of Pin and Pin Functions (112-pin with PGA pseudo-differential input and without USB pin) (2/5)

| Pin Number 112-pin LQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|-------------------------------|---|----------|------------|--|--|-------------------------|--------|-----------------|
| 26 | TRCLK | PD2 | A7 | GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/ TMC11/TMO4 | SCK5/SCK8/MOSIA | | | |
| 27 | TRDATA3 | PD1 | A6 | GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/ TMO2 | RXD8/SMISO8/SSCL8/ MISOA | | | |
| 28 | TRDATA2 | PD0 | A5 | GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/ TMO6 | TXD8/SMOSI8/SSDA8/ RSPCKA | | | |
| 29 | TRDATA1 | PB7 | A4 | GTIOC1B/GTIOC1B# | SCK5/SCK11/SCK12 | | | |
| 30 | TRDATA0 | PB6 | A3 | GTIOC2A/GTIOC2A# | RXD5/SMISO5/SSCL5/ RXD11/SMISO11/ SSCL11/RXD12/ SMISO12/SSCL12/ RXDX12/CRX0 | IRQ2 | | |
| 31 | TRSYNC | PB5 | A2 | GTIOC2B/GTIOC2B# | TXD5/SMOSI5/SSDA5/ TXD11/SMOSI11/ SSDA11/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0 | | | |
| 32 | VCC | | | | | | | |
| 33 | | PB4 | A1 | GTETRG/GTETRGRB/ GTETRG/GTETRGRD/ POE8# | CTS5#/RTS5#/SS5#/ SCK11/CTS11#/ RTS11#/SS11# | IRQ3-DS | | |
| 34 | VSS | | | | | | | |
| 35 | | PC2 | CS1# | MTIOC0D/MTIOC0D#/ GTADSM0 | SCK8 | IRQ15 | | ADSM0/ COMP5 |
| 36 | | PC1 | A16 | MTIOC0C/MTIOC0C#/ GTADSM1 | TXD8/SMOSI8/SSDA8 | IRQ13 | | ADSM1/ COMP4 |
| 37 | | PC0 | CS0# | MTIOC0B/MTIOC0B# | RXD8/SMISO8/SSCL8 | IRQ12 | | COMP3 |
| 38 | | PB3 | | MTIOC0A/MTIOC0A#/ CACREF | SCK6/RSPCKA | IRQ9 | | |
| 39 | | PB2 | | MTIOC0B/MTIOC0B#/ GTADSM0/TMRI0 | TXD6/SMOSI6/SSDA6/ SDA | | | ADSM0 |
| 40 | | PB1 | | MTIOC0C/MTIOC0C#/ GTADSM1/TMCI0 | RXD6/SMISO6/SSCL6/ SCL | IRQ4 | | ADSM1 |
| 41 | | PB0 | A0/BC0# | MTIOC0D/MTIOC0D#/ TMO0 | TXD6/SMOSI6/SSDA6/ CTS11#/RTS11#/ SS11#/MOSIA | IRQ8 | | ADTRG2# |
| 42 | | PA5 | | MTIOC1A/MTIOC1A#/ TMCI3 | RXD6/SMISO6/SSCL6/ RXD8/SMISO8/SSCL8/ MISOA | IRQ1 | | ADTRG1# |
| 43 | | PA4 | | MTIOC1B/MTIOC1B#/ TMCI7 | SCK6/TXD8/SMOSI8/ SSDA8/RSPCKA | | | ADTRG0# |
| 44 | | PA3 | | MTIOC2A/MTIOC2A#/ GTADSM0/TMRI7 | TXD9/SMOSI9/SSDA9/ SCK8/SSLA0 | | | |
| 45 | | PA2 | A0/BC0# | MTIOC2B/MTIOC2B#/ GTADSM1/TMO7 | CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/ SSLA1 | | | |
| 46 | | PA1 | | MTIOC6A/MTIOC6A#/ TMO4 | TXD9/SMOSI9/SSDA9/ RXD11/SMISO11/ SSCL11/SSLA2/CRX0 | IRQ14-DS | | ADTRG0# |
| 47 | | PA0 | | MTIOC6C/MTIOC6C#/ TMO2 | SCK9/TXD11/SMOSI11/ SSDA11/SSLA3/CTX0 | | | |
| 48 | VCC | | | | | | | |
| 49 | | P96 | CS0#/WAIT# | GTETRG/GTETRGRB/ GTETRG/GTETRGRD/ POE4# | CTS8#/RTS8#/SS8# | IRQ4-DS | | |
| 50 | VSS | | | | | | | |

Table 1.6 List of Pin and Pin Functions (112-pin with PGA pseudo-differential input and without USB pin) (3/5)

| Pin Number 112-pin LQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|-------------------------------|---|----------|---------------|---|--|-------------------------|--------|--------|
| 51 | | P95 | | MTIOC6B/MTIOC6B#/ GTIOC4A/GTIOC7A/ GTIOC4A#/GTIOC7A# | | | | |
| 52 | | P94 | | MTIOC7A/MTIOC7A#/ GTIOC5A/GTIOC8A/ GTIOC5A#/GTIOC8A# | | | | |
| 53 | | P93 | | MTIOC7B/MTIOC7B#/ GTIOC6A/GTIOC9A/ GTIOC6A#/GTIOC9A# | | | | |
| 54 | | P92 | | MTIOC6D/MTIOC6D#/ GTIOC4B/GTIOC7B/ GTIOC4B#/GTIOC7B# | | | | |
| 55 | | P91 | | MTIOC7C/MTIOC7C#/ GTIOC5B/GTIOC8B/ GTIOC5B#/GTIOC8B# | | | | |
| 56 | | P90 | | MTIOC7D/MTIOC7D#/ GTIOC6B/GTIOC9B/ GTIOC6B#/GTIOC9B# | | | | |
| 57 | | P76 | D0 [A0/D0] | MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/ GTIOC2B#/GTIOC6B# | | | | |
| 58 | | P75 | D1 [A1/D1] | MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/ GTIOC1B#/GTIOC5B# | | | | |
| 59 | | P74 | D2 [A2/D2] | MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/ GTIOC0B#/GTIOC4B# | | | | |
| 60 | | P73 | D3 [A3/D3] | MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/ GTIOC2A#/GTIOC6A# | | | | |
| 61 | | P72 | D4 [A4/D4] | MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/ GTIOC1A#/GTIOC5A# | | | | |
| 62 | | P71 | D5 [A5/D5] | MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/ GTIOC0A#/GTIOC4A# | | | | |
| 63 | | P70 | D6 [A6/D6] | GTETRGA/GTETRGB/ GTETRC/GTETRGD/ POE0# | CTS9#/RTS9#/SS9# | IRQ5-DS | | |
| 64 | | PG2 | D11 [A11/D11] | GTETRGA/GTIOC0B/ GTIOC0B# | SCK9 | IRQ2 | | COMP0 |
| 65 | | PG1 | D12 [A12/D12] | GTIOC0A/GTIOC0A# | TXD9/SMOS9/SSDA9 | IRQ1 | | COMP1 |
| 66 | | PG0 | D13 [A13/D13] | GTIOC1B/GTIOC1B# | RXD9/SMISO9/SSCL9 | IRQ0 | | COMP2 |
| 67 | | P33 | D7 [A7/D7] | MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/ GTIOC3B/GTIOC3B#/ TMO0 | SSLA3 | IRQ13-DS | | |
| 68 | | P32 | D8 [A8/D8] | MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/ GTIOC3A/GTIOC3A#/ TMO6 | SSLA2 | IRQ12-DS | | |
| 69 | VCC | | | | | | | |
| 70 | | P31 | D9 [A9/D9] | MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/ TMR16 | SSLA1 | IRQ6 | | |
| 71 | VSS | | | | | | | |
| 72 | | P30 | D10 [A10/D10] | MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/ TMC16 | SCK8/CTS8#/RTS8#/ SS8#/SSLA0 | IRQ7 | | COMP3 |
| 73 | | P27 | | MTIOC1A/MTIOC0C/ MTIOC1A#/ MTIOC0C#/POE9# | | IRQ15 | | |

Table 1.6 List of Pin and Pin Functions (112-pin with PGA pseudo-differential input and without USB pin) (4/5)

| Pin Number 112-pin LQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|-------------------------------|---|----------|---------------|--|--|-------------------------|-----------------------------|-------------------|
| 74 | | P24 | D11 [A11/D11] | MTIC5U/MTIC5U#/ TMC12/TMO6 | CTS8#/RTS8#/SS8#/ SCK8/RSPCKA | IRQ4 | | COMP0 |
| 75 | | P23 | D12 [A12/D12] | MTIC5V/MTIC5V#/ TMO2/CACREF | TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/MOSIA/CTX0 | IRQ11 | | COMP1 |
| 76 | | P22 | D13 [A13/D13] | MTIC5W/ MTCLKD/MTIC5W#/ MTCLKD#/MTIOC9B/ TMR12/TMO4 | RXD8/SMISO8/SSCL8/ RXD12/SMISO12/ SSCL12/RXD12/ MISOA/CRX0 | IRQ10 | | ADTRG2#/ COMP2 |
| 77 | | P21 | D14 [A14/D14] | MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/ TMC14 | TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/MOSIA | IRQ6-DS | AN217 | ADTRG1#/ COMP5 |
| 78 | | P20 | D15 [A15/D15] | MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/ TMR14 | CTS8#/RTS8#/SS8#/ SCK8/RSPCKA | IRQ7-DS | AN216 | ADTRG0#/ COMP4 |
| 79 | | P65 | A12 | | | IRQ9 | AN211/ CMPC53/ DA1 | |
| 80 | | P64 | A13 | | | IRQ8 | AN210/ CMPC33/ DA0 | |
| 81 | AVCC2 | | | | | | | |
| 82 | AVSS2 | | | | | | | |
| 83 | | P63 | A14 | | | IRQ7 | AN209/ CMPC23 | |
| 84 | | P62 | A15 | | | IRQ6 | AN208/ CMPC43 | |
| 85 | | P61 | A16 | | | IRQ5 | AN207/ CMPC13 | |
| 86 | | P60 | A17 | | | IRQ4 | AN206/ CMPC03 | |
| 87 | | P55 | A18 | | | IRQ3 | AN203/ CMPC32 | |
| 88 | | P54 | A19 | | | IRQ2 | AN202/ CMPC22 | |
| 89 | | P53 | A20 | | | IRQ1 | AN201/ CMPC12 | |
| 90 | | P52 | | | | IRQ0 | AN200/ CMPC02 | |
| 91 | | P47 | | | | | AN103 | |
| 92 | | P46 | | | | | AN102/ CMPC50/ CMPC51 | |
| 93 | | P45 | | | | | AN101/ CMPC40/ CMPC41 | |
| 94 | | P44 | | | | | AN100/ CMPC30/ CMPC31 | |
| 95 | | PH4 | | | | | AN107/ PGAVSS1 | |
| 96 | | P43 | | | | | AN003 | |
| 97 | | P42 | | | | | AN002/ CMPC20/ CMPC21 | |
| 98 | | P41 | | | | | AN001/ CMPC10/ CMPC11 | |

Table 1.6 List of Pin and Pin Functions (112-pin with PGA pseudo-differential input and without USB pin) (5/5)

| Pin Number 112-pin LQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|-------------------------------|---|----------|-----------|---|---|-------------------------|-----------------------------|--------|
| 99 | | P40 | | | | | AN000/ CMPC00/ CMPC01 | |
| 100 | | PH0 | | | | | AN007/ PGAVSS0 | |
| 101 | AVCC1 | | | | | | | |
| 102 | AVCC0 | | | | | | | |
| 103 | AVSS0 | | | | | | | |
| 104 | AVSS1 | | | | | | | |
| 105 | | P82 | ALE/WAIT# | MTIC5U/MTIC5U#/ TMO4 | SCK6/SCK12 | IRQ3 | | COMP5 |
| 106 | | P81 | CS2# | MTIC5V/MTIC5V#/ TMC14 | TXD6/SMOSI6/SSDA6/ TXD12/SMOS12/ SSDA12/TXDX12/ SIOX12 | | | COMP4 |
| 107 | | P80 | CS1# | MTIC5W/MTIC5W#/ TMR14 | RXD6/SMISO6/SSCL6/ RXD12/SMISO12/ SSCL12/RXDX12 | IRQ5 | | COMP3 |
| 108 | | P11 | RD# | MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/ MTIOC9D/GTIOC3B/ GTETRGA/GTIOC3B#/ GTETRGC/TMO3/ POE9# | | IRQ1-DS | | |
| 109 | | P10 | | MTIOC9B/MTCLKD/ MTIOC9B#/MTCLKD#/ GTETRGB/GTETRGD/ TMR13/POE12# | CTS6#/RTS6#/SS6# | IRQ0-DS | | |
| 110 | | P17 | | MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC9B/ GTIOC2B#/GTIOC9B# | | IRQ14 | | |
| 111 | | P16 | | MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC8B/ GTIOC1B#/GTIOC8B# | | IRQ13 | | |
| 112 | | P15 | | MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC7B/ GTIOC0B#/GTIOC7B# | | IRQ12 | | |

Table 1.7 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and with USB pin) (1/5)

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Communica tions (USB) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|-------------------------|---|--|-----------------------------|-------------------------|--------|-----------------|
| 1 | | PE5 | BCLK | MTIOC9D/ MTIOC9D#/ GTIOC3A/ GTETRGB/ GTIOC3A#/ GTETRGD | SCK9/CTS9#/ RTS9#/SS9# | | IRQ0 | | ADST0 |
| 2 | EMLE | | | | | | | | |
| 3 | VSS | | | | | | | | |
| 4 | UB | P00 | A11 | MTIOC9A/ MTIOC9A#/CACREF | RXD9/SMISO9/ SSCL9/RXD12/ SMISO12/SSCL12/ RXDX12 | | IRQ2 | | ADST1/ COMP0 |
| 5 | VCL | | | | | | | | |
| 6 | MD/FINED | | | | | | | | |
| 7 | | P01 | A10 | MTIOC9C/ MTIOC9C#/ GTETRGA/ GTETRGB/ GTETRGC/ GTETRGC/ GTETRGC/POE12# | TXD9/SMOSI9/ SSDA9/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12 | | IRQ4 | | ADST2/ COMP1 |
| 8 | | PE4 | A9 | MTCLKC/MTCLKC#/ GTETRGA/ GTETRGB/ GTETRGC/ GTETRGC/POE10# | SCK9 | | IRQ1 | | |
| 9 | | PE3 | A8 | MTCLKD/MTCLKD#/ GTETRGA/ GTETRGB/ GTETRGC/ GTETRGC/POE11# | CTS9#/RTS9#/ SS9# | | IRQ2-DS | | |
| 10 | RES# | | | | | | | | |
| 11 | XTAL | P37 | | | | | | | |
| 12 | VSS | | | | | | | | |
| 13 | EXTAL | P36 | | | | | | | |
| 14 | VCC | | | | | | | | |
| 15 | UPSEL | PE2 | | POE10# | | | NMI | | |
| 16 | | PE1 | WR0#/WR# | MTIOC9D/ MTIOC9D#/TMO5 | CTS5#/RTS5#/ SS5#/CTS12#/ RTS12#/SS12#/ SSLA3 | | IRQ15 | | |
| 17 | | PE0 | WR1#/ BC1#/ WAIT# | MTIOC9B/ MTIOC9B#/TMC11/ TMC15 | RXD5/SMISO5/ SSCL5/SSLA2/ CRX0 | USB0_OVR CURB | IRQ7 | | |
| 18 | TRST# | PD7 | | MTIOC9A/ MTIOC9A#/ GTIOC0A/GTIOC3A/ GTIOC0A#/ GTIOC3A#/TMR11/ TMR15 | TXD5/SMOSI5/ SSDA5/SSLA1/ CTX0 | | IRQ8 | | |
| 19 | TMS | PD6 | | MTIOC9C/ MTIOC9C#/ GTIOC0B/GTIOC3B/ GTIOC0B#/ GTIOC3B#/TMO1 | CTS1#/RTS1#/ SS1#/CTS11#/ RTS11#/SS11#/ SSLA0 | | IRQ5 | | ADST0 |
| 20 | TDI | PD5 | | GTIOC1A/ GTETRGA/ GTIOC1A#/TMR10/ TMR16 | RXD1/SMISO1/ SSCL1/RXD11/ SMISO11/SSCL11 | | IRQ6 | | |
| 21 | TCK | PD4 | | GTIOC1B/ GTETRGB/ GTIOC1B#/TMC10/ TMC16 | SCK1/SCK11 | | IRQ2 | | |

Table 1.7 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and with USB pin) (2/5)

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Communica tions (USB) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|------------|--|---|-------------------------------------|-------------------------|--------|---------|
| 22 | TDO | PD3 | | GTIOC2A/ GTETRGC/ GTIOC2A#/TMO0 | TXD1/SMOSI1/ SSDA1/TXD11/ SMOSI11/SSDA11 | | | | |
| 23 | TRCLK | PD2 | A7 | GTIOC2B/GTIOC0A/ GTIOC2B#/ GTIOC0A#/TMC11/ TMO4 | SCK5/SCK8/ MOSIA | USB0_VBUS | | | |
| 24 | | | | | | USB0_DM | | | |
| 25 | | | | | | USB0_DP | | | |
| 26 | VCC_USB | | | | | | | | |
| 27 | TRDATA0 | PB6 | A3 | GTIOC2A/ GTIOC2A# | RXD5/SMISO5/ SSCL5/RXD11/ SMISO11/SSCL11/ RXD12/SMISO12/ SSCL12/RXD12/ CRX0 | USB0_OVR CURA | IRQ2 | | |
| 28 | TRSYNC | PB5 | A2 | GTIOC2B/ GTIOC2B# | TXD5/SMOSI5/ SSDA5/TXD11/ SMOSI11/SSDA11/ TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/CTX0 | USB0_VBUS EN | | | |
| 29 | VCC | | | | | | | | |
| 30 | | PB4 | A1 | GTETPGA/ GTETRGB/ GTETRGC/ GTETRGD/POE8# | CTS5#/RTS5#/ SS5#/SCK11/ CTS11#/RTS11#/ SS11# | USB0_OVR CURB | IRQ3-DS | | |
| 31 | VSS/VSS_USB | | | | | | | | |
| 32 | | PB3 | A7 | MTIOC0A/ MTIOC0A#/CACREF | SCK6/RSPCKA | | IRQ9 | | |
| 33 | | PB2 | A6 | MTIOC0B/ MTIOC0B#/ GTADSM0/TMRI0 | TXD6/SMOSI6/ SSDA6/SDA | | | | ADSM0 |
| 34 | | PB1 | A5 | MTIOC0C/ MTIOC0C#/ GTADSM1/TMC10 | RXD6/SMISO6/ SSCL6/SCL | | IRQ4 | | ADSM1 |
| 35 | | PB0 | A0/BC0#/A4 | MTIOC0D/ MTIOC0D#/TMO0 | TXD6/SMOSI6/ SSDA6/CTS11#/ RTS11#/SS11#/ MOSIA | | IRQ8 | | ADTRG2# |
| 36 | | PA5 | A3 | MTIOC1A/ MTIOC1A#/TMC13 | RXD6/SMISO6/ SSCL6/RXD8/ SMISO8/SSCL8/ MISOA | | IRQ1 | | ADTRG1# |
| 37 | | PA4 | A2 | MTIOC1B/ MTIOC1B#/TMC17 | SCK6/TXD8/ SMOSI8/SSDA8/ RSPCKA | | | | ADTRG0# |
| 38 | | PA3 | A1 | MTIOC2A/ MTIOC2A#/ GTADSM0/TMRI7 | TXD9/SMOSI9/ SSDA9/SCK8/ SSLA0 | | | | |
| 39 | | PA2 | A0/BC0# | MTIOC2B/ MTIOC2B#/ GTADSM1/TMO7 | CTS6#/RTS6#/ SS6#/RXD9/ SMISO9/SSCL9/ SCK11/SSLA1 | | | | |
| 40 | | PA1 | | MTIOC6A/ MTIOC6A#/TMO4 | TXD9/SMOSI9/ SSDA9/RXD11/ SMISO11/SSCL11/ SSLA2/CRX0 | USB0_ID/ USB0_OVR CURA | IRQ14-DS | | ADTRG0# |
| 41 | | PA0 | | MTIOC6C/ MTIOC6C#/TMO2 | SCK9/TXD11/ SMOSI11/SSDA11/ SSLA3/CTX0 | USB0_EXIC EN/ USB0_VBUS EN | | | |
| 42 | VCC | | | | | | | | |

Table 1.7 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and with USB pin) (3/5)

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Communica tions (USB) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|----------------|--|---|-----------------------------|-------------------------|--------|--------|
| 43 | | P96 | CS0#/ WAIT# | GTETRG/ A/ GTETRGB/ GTETRG/ C/ GTETRG/ D/POE4# | CTS8#/RTS8#/ SS8# | | IRQ4-DS | | |
| 44 | VSS | | | | | | | | |
| 45 | | P95 | | MTIOC6B/ MTIOC6B#/ GTIOC4A/GTIOC7A/ GTIOC4A#/ GTIOC7A# | | | | | |
| 46 | | P94 | | MTIOC7A/ MTIOC7A#/ GTIOC5A/GTIOC8A/ GTIOC5A#/ GTIOC8A# | | | | | |
| 47 | | P93 | | MTIOC7B/ MTIOC7B#/ GTIOC6A/GTIOC9A/ GTIOC6A#/ GTIOC9A# | | | | | |
| 48 | | P92 | | MTIOC6D/ MTIOC6D#/ GTIOC4B/GTIOC7B/ GTIOC4B#/ GTIOC7B# | | | | | |
| 49 | | P91 | | MTIOC7C/ MTIOC7C#/ GTIOC5B/GTIOC8B/ GTIOC5B#/ GTIOC8B# | | | | | |
| 50 | | P90 | | MTIOC7D/ MTIOC7D#/ GTIOC6B/GTIOC9B/ GTIOC6B#/ GTIOC9B# | | | | | |
| 51 | | P76 | D0 [A0/D0] | MTIOC4D/ MTIOC4D#/ GTIOC2B/GTIOC6B/ GTIOC2B#/ GTIOC6B# | | | | | |
| 52 | | P75 | D1 [A1/D1] | MTIOC4C/ MTIOC4C#/ GTIOC1B/GTIOC5B/ GTIOC1B#/ GTIOC5B# | | | | | |
| 53 | | P74 | D2 [A2/D2] | MTIOC3D/ MTIOC3D#/ GTIOC0B/GTIOC4B/ GTIOC0B#/ GTIOC4B# | | | | | |
| 54 | | P73 | D3 [A3/D3] | MTIOC4B/ MTIOC4B#/ GTIOC2A/GTIOC6A/ GTIOC2A#/ GTIOC6A# | | | | | |
| 55 | | P72 | D4 [A4/D4] | MTIOC4A/ MTIOC4A#/ GTIOC1A/GTIOC5A/ GTIOC1A#/ GTIOC5A# | | | | | |
| 56 | | P71 | D5 [A5/D5] | MTIOC3B/ MTIOC3B#/ GTIOC0A/GTIOC4A/ GTIOC0A#/ GTIOC4A# | | | | | |
| 57 | | P70 | D6 [A6/D6] | GTETRG/ A/ GTETRGB/ GTETRG/ C/ GTETRG/ D/POE0# | CTS9#/RTS9#/ SS9# | | IRQ5-DS | | |

Table 1.7 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and with USB pin) (4/5)

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Communica tions (USB) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|-------------------|---|---|-----------------------------|-------------------------|--------------------------|-------------------|
| 58 | | P33 | D7 [A7/D7] | MTIOC3A/MTCLKA/ MTIOC3A#/ MTCLKA#/GTIOC3B/ GTIOC3B#/TMO0 | SSLA3 | | IRQ13-DS | | |
| 59 | | P32 | D8 [A8/D8] | MTIOC3C/MTCLKB/ MTIOC3C#/ MTCLKB#/GTIOC3A/ GTIOC3A#/TMO6 | SSLA2 | | IRQ12-DS | | |
| 60 | VCC | | | | | | | | |
| 61 | | P31 | D9 [A9/D9] | MTIOC0A/MTCLKC/ MTIOC0A#/ MTCLKC#/TMRI6 | SSLA1 | | IRQ6 | | |
| 62 | VSS | | | | | | | | |
| 63 | | P30 | D10 [A10/ D10] | MTIOC0B/MTCLKD/ MTIOC0B#/ MTCLKD#/TMCI6 | SCK8/CTS8#/ RTS8#/SS8#/ SSLA0 | | IRQ7 | | COMP3 |
| 64 | | P27 | CS3# | MTIOC1A/MTIOC0C/ MTIOC1A#/ MTIOC0C#/POE9# | | | IRQ15 | | |
| 65 | | P24 | D11 [A11/ D11] | MTIC5U/MTIC5U#/ TMCI2/TMO6 | CTS8#/RTS8#/ SS8#/SCK8/ RSPCKA | | IRQ4 | | COMP0 |
| 66 | | P23 | D12 [A12/ D12] | MTIC5V/MTIC5V#/ TMO2/CACREF | TXD8/SMOSI8/ SSDA8/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/ MOSIA/CTX0 | | IRQ11 | | COMP1 |
| 67 | | P22 | D13 [A13/ D13] | MTIC5W/MTCLKD/ MTIC5W#/ MTCLKD#/ MTIOC9B/TMRI2/ TMO4 | RXD8/SMISO8/ SSCL8/RXD12/ SMISO12/SSCL12/ RXDX12/MISOA/ CRX0 | | IRQ10 | | ADTRG2#/ COMP2 |
| 68 | | P21 | D14 [A14/ D14] | MTIOC9A/MTCLKA/ MTIOC9A#/ MTCLKA#/TMCI4 | TXD8/SMOSI8/ SSDA8/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/ MOSIA | | IRQ6-DS | AN217 | ADTRG1#/ COMP5 |
| 69 | | P20 | D15 [A15/ D15] | MTIOC9C/MTCLKB/ MTIOC9C#/ MTCLKB#/TMRI4 | CTS8#/RTS8#/ SS8#/SCK8/ RSPCKA | | IRQ7-DS | AN216 | ADTRG0#/ COMP4 |
| 70 | | P65 | A12 | | | | IRQ9 | AN211/ CMPC53/ DA1 | |
| 71 | | P64 | A13 | | | | IRQ8 | AN210/ CMPC33/ DA0 | |
| 72 | AVCC2 | | | | | | | | |
| 73 | AVSS2 | | | | | | | | |
| 74 | | P63 | A14/A12 | | | | IRQ7 | AN209/ CMPC23 | |
| 75 | | P62 | A15/A13 | | | | IRQ6 | AN208/ CMPC43 | |
| 76 | | P61 | A16/A14 | | | | IRQ5 | AN207/ CMPC13 | |
| 77 | | P60 | A17/A15 | | | | IRQ4 | AN206/ CMPC03 | |
| 78 | | P55 | A18/A16 | | | | IRQ3 | AN203/ CMPC32 | |
| 79 | | P54 | A19/A17 | | | | IRQ2 | AN202/ CMPC22 | |
| 80 | | P53 | A20/A18 | | | | IRQ1 | AN201/ CMPC12 | |

Table 1.7 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and with USB pin) (5/5)

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Communica tions (USB) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|-----------|---|--|-----------------------------|-------------------------|-----------------------------|--------|
| 81 | | P52 | | | | | IRQ0 | AN200/ CMPC02 | |
| 82 | | P47 | | | | | | AN103 | |
| 83 | | P46 | | | | | | AN102/ CMPC50/ CMPC51 | |
| 84 | | P45 | | | | | | AN101/ CMPC40/ CMPC41 | |
| 85 | | P44 | | | | | | AN100/ CMPC30/ CMPC31 | |
| 86 | | PH4 | | | | | | AN107/ PGAVSS1 | |
| 87 | | P43 | | | | | | AN003 | |
| 88 | | P42 | | | | | | AN002/ CMPC20/ CMPC21 | |
| 89 | | P41 | | | | | | AN001/ CMPC10/ CMPC11 | |
| 90 | | P40 | | | | | | AN000/ CMPC00/ CMPC01 | |
| 91 | | PH0 | | | | | | AN007/ PGAVSS0 | |
| 92 | AVCC1 | | | | | | | | |
| 93 | AVCC0 | | | | | | | | |
| 94 | AVSS0 | | | | | | | | |
| 95 | AVSS1 | | | | | | | | |
| 96 | | P82 | ALE/WAIT# | MTIC5U/MTIC5U#/ TMO4 | SCK6/SCK12 | | IRQ3 | | COMP5 |
| 97 | | P81 | CS2# | MTIC5V/MTIC5V#/ TMC14 | TXD6/SMOSI6/ SSDA6/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12 | | | | COMP4 |
| 98 | | P80 | CS1# | MTIC5W/MTIC5W#/ TMRI4 | RXD6/SMISO6/ SSCL6/RXD12/ SMISO12/SSCL12/ RXDX12 | | IRQ5 | | COMP3 |
| 99 | | P11 | RD# | MTIOC3A/MTCLKC/ MTIOC3A#/ MTCLKC#/ MTIOC9D/GTIOC3B/ GTETRGA/ GTIOC3B#/ GTETRGC/TMO3/ POE9# | | | IRQ1-DS | | |
| 100 | | P10 | | MTIOC9B/MTCLKD/ MTIOC9B#/ MTCLKD#/ GTETRGB/ GTETRGD/TMRI3/ POE12# | CTS6#/RTS6#/ SS6# | | IRQ0-DS | | |

Table 1.8 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and without USB pin) (1/5)

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|---------------------|--|---|-------------------------|--------|-----------------|
| 1 | | PE5 | BCLK | MTIOC9D/MTIOC9D#/ GTIOC3A/GTETRGB/ GTIOC3A#/GTETRGD | SCK9/CTS9#/RTS9#/ SS9# | IRQ0 | | ADST0 |
| 2 | EMLE | | | | | | | |
| 3 | VSS | | | | | | | |
| 4 | UB | P00 | A11 | MTIOC9A/MTIOC9A#/ CACREF | RXD9/SMISO9/SSCL9/ RXD12/SMISO12/ SSCL12/RXD12 | IRQ2 | | ADST1/ COMP0 |
| 5 | VCL | | | | | | | |
| 6 | MD/FINED | | | | | | | |
| 7 | | P01 | A10 | MTIOC9C/MTIOC9C#/ GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE12# | TXD9/SMOSI9/SSDA9/ TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12 | IRQ4 | | ADST2/ COMP1 |
| 8 | | PE4 | A9 | MTCLKC/MTCLKC#/ GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE10# | SCK9 | IRQ1 | | |
| 9 | | PE3 | A8 | MTCLKD/MTCLKD#/ GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE11# | CTS9#/RTS9#/SS9# | IRQ2-DS | | |
| 10 | RES# | | | | | | | |
| 11 | XTAL | P37 | | | | | | |
| 12 | VSS | | | | | | | |
| 13 | EXTAL | P36 | | | | | | |
| 14 | VCC | | | | | | | |
| 15 | | PE2 | | POE10# | | NMI | | |
| 16 | | PE1 | WR0#/WR# | MTIOC9D/MTIOC9D#/ TMO5 | CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/ SS12#/SSLA3 | IRQ15 | | |
| 17 | | PE0 | WR1#/BC1#/ WAIT# | MTIOC9B/MTIOC9B#/ TMC11/TMC15 | RXD5/SMISO5/SSCL5/ SSLA2/CRX0 | IRQ7 | | |
| 18 | TRST# | PD7 | | MTIOC9A/MTIOC9A#/ GTIOC0A/GTIOC3A/ GTIOC0A#/GTIOC3A#/ TMR11/TMR15 | TXD5/SMOSI5/SSDA5/ SSLA1/CTX0 | IRQ8 | | |
| 19 | TMS | PD6 | | MTIOC9C/MTIOC9C#/ GTIOC0B/GTIOC3B/ GTIOC0B#/GTIOC3B#/ TMO1 | CTS1#/RTS1#/SS1#/ CTS11#/RTS11#/ SS11#/SSLA0 | IRQ5 | | ADST0 |
| 20 | TDI | PD5 | | GTIOC1A/GTETRGA/ GTIOC1A#/TMR10/ TMR16 | RXD1/SMISO1/SSCL1/ RXD11/SMISO11/ SSCL11 | IRQ6 | | |
| 21 | TCK | PD4 | | GTIOC1B/GTETRGB/ GTIOC1B#/TMC10/ TMC16 | SCK1/SCK11 | IRQ2 | | |
| 22 | TDO | PD3 | | GTIOC2A/GTETRGC/ GTIOC2A#/TMO0 | TXD1/SMOSI1/SSDA1/ TXD11/SMOSI11/ SSDA11 | | | |
| 23 | TRCLK | PD2 | A7 | GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/ TMC11/TMO4 | SCK5/SCK8/MOSIA | | | |
| 24 | TRDATA3 | PD1 | A6 | GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/ TMO2 | RXD8/SMISO8/SSCL8/ MISOA | | | |
| 25 | TRDATA2 | PD0 | A5 | GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/ TMO6 | TXD8/SMOSI8/SSDA8/ RSPCKA | | | |
| 26 | TRDATA1 | PB7 | A4 | GTIOC1B/GTIOC1B# | SCK5/SCK11/SCK12 | | | |

Table 1.8 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and without USB pin) (2/5)

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|--------------|---|--|-------------------------|--------|---------|
| 27 | TRDATA0 | PB6 | A3 | GTIOC2A/GTIOC2A# | RXD5/SMISO5/SSCL5/ RXD11/SMISO11/ SSCL11/RXD12/ SMISO12/SSCL12/ RXDX12/CRX0 | IRQ2 | | |
| 28 | TRSYNC | PB5 | A2 | GTIOC2B/GTIOC2B# | TXD5/SMOSI5/SSDA5/ TXD11/SMOSI11/ SSDA11/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0 | | | |
| 29 | VCC | | | | | | | |
| 30 | | PB4 | A1 | GTETRG/GTETRGB/ GTETRGC/GTETRGD/ POE8# | CTS5#/RTS5#/SS5#/ SCK11/CTS11#/ RTS11#/SS11# | IRQ3-DS | | |
| 31 | VSS | | | | | | | |
| 32 | | PB3 | A7*1 | MTIOC0A/MTIOC0A#/ CACREF | SCK6/RSPCKA | IRQ9 | | |
| 33 | | PB2 | A6*1 | MTIOC0B/MTIOC0B#/ GTADSM0/TMRI0 | TXD6/SMOSI6/SSDA6/ SDA | | | ADSM0 |
| 34 | | PB1 | A5*1 | MTIOC0C/MTIOC0C#/ GTADSM1/TMCI0 | RXD6/SMISO6/SSCL6/ SCL | IRQ4 | | ADSM1 |
| 35 | | PB0 | A0/A4*1/BC0# | MTIOC0D/MTIOC0D#/ TMO0 | TXD6/SMOSI6/SSDA6/ CTS11#/RTS11#/ SS11#/MOSIA | IRQ8 | | ADTRG2# |
| 36 | | PA5 | A3*1 | MTIOC1A/MTIOC1A#/ TMCI3 | RXD6/SMISO6/SSCL6/ RXD8/SMISO8/SSCL8/ MISOA | IRQ1 | | ADTRG1# |
| 37 | | PA4 | A2*1 | MTIOC1B/MTIOC1B#/ TMCI7 | SCK6/TXD8/SMOSI8/ SSDA8/RSPCKA | | | ADTRG0# |
| 38 | | PA3 | A1*1 | MTIOC2A/MTIOC2A#/ GTADSM0/TMRI7 | TXD9/SMOSI9/SSDA9/ SCK8/SSLA0 | | | |
| 39 | | PA2 | A0/BC0# | MTIOC2B/MTIOC2B#/ GTADSM1/TMO7 | CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/ SCK11*1/SSLA1 | | | |
| 40 | | PA1 | | MTIOC6A/MTIOC6A#/ TMO4 | TXD9/SMOSI9/SSDA9/ RXD11/SMISO11/ SSCL11/SSLA2/CRX0 | IRQ14-DS | | ADTRG0# |
| 41 | | PA0 | | MTIOC6C/MTIOC6C#/ TMO2 | SCK9/TXD11/SMOSI11/ SSDA11/SSLA3/CTX0 | | | |
| 42 | VCC | | | | | | | |
| 43 | | P96 | CS0#/WAIT# | GTETRG/GTETRGB/ GTETRGC/GTETRGD/ POE4# | CTS8#/RTS8#/SS8# | IRQ4-DS | | |
| 44 | VSS | | | | | | | |
| 45 | | P95 | | MTIOC6B/MTIOC6B#/ GTIOC4A/GTIOC7A/ GTIOC4A#GTIOC7A# | | | | |
| 46 | | P94 | | MTIOC7A/MTIOC7A#/ GTIOC5A/GTIOC8A/ GTIOC5A#GTIOC8A# | | | | |
| 47 | | P93 | | MTIOC7B/MTIOC7B#/ GTIOC6A/GTIOC9A/ GTIOC6A#GTIOC9A# | | | | |
| 48 | | P92 | | MTIOC6D/MTIOC6D#/ GTIOC4B/GTIOC7B/ GTIOC4B#GTIOC7B# | | | | |
| 49 | | P91 | | MTIOC7C/MTIOC7C#/ GTIOC5B/GTIOC8B/ GTIOC5B#GTIOC8B# | | | | |
| 50 | | P90 | | MTIOC7D/MTIOC7D#/ GTIOC6B/GTIOC9B/ GTIOC6B#GTIOC9B# | | | | |

Table 1.8 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and without USB pin) (3/5)

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|---------------|---|--|-------------------------|--------------------------|-------------------|
| 51 | | P76 | D0 [A0/D0] | MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/ GTIOC2B#/GTIOC6B# | | | | |
| 52 | | P75 | D1 [A1/D1] | MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/ GTIOC1B#/GTIOC5B# | | | | |
| 53 | | P74 | D2 [A2/D2] | MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/ GTIOC0B#/GTIOC4B# | | | | |
| 54 | | P73 | D3 [A3/D3] | MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/ GTIOC2A#/GTIOC6A# | | | | |
| 55 | | P72 | D4 [A4/D4] | MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/ GTIOC1A#/GTIOC5A# | | | | |
| 56 | | P71 | D5 [A5/D5] | MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/ GTIOC0A#/GTIOC4A# | | | | |
| 57 | | P70 | D6 [A6/D6] | GTETRG/GTETRGB/ GTETRGC/GTETRGD/ POE0# | CTS9#/RTS9#/SS9# | IRQ5-DS | | |
| 58 | | P33 | D7 [A7/D7] | MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/ GTIOC3B/GTIOC3B#/ TMO0 | SSLA3 | IRQ13-DS | | |
| 59 | | P32 | D8 [A8/D8] | MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/ GTIOC3A/GTIOC3A#/ TMO6 | SSLA2 | IRQ12-DS | | |
| 60 | VCC | | | | | | | |
| 61 | | P31 | D9 [A9/D9] | MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/ TMR16 | SSLA1 | IRQ6 | | |
| 62 | VSS | | | | | | | |
| 63 | | P30 | D10 [A10/D10] | MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/ TMC16 | SCK8/CTS8#/RTS8#/ SS8#/SSLA0 | IRQ7 | | COMP3 |
| 64 | | P27 | CS3*1 | MTIOC1A/MTIOC0C/ MTIOC1A#/ MTIOC0C#/POE9# | | IRQ15 | | |
| 65 | | P24 | D11 [A11/D11] | MTIC5U/MTIC5U#/ TMC12/TMO6 | CTS8#/RTS8#/SS8#/ SCK8/RSPCKA | IRQ4 | | COMP0 |
| 66 | | P23 | D12 [A12/D12] | MTIC5V/MTIC5V#/ TMO2/CACREF | TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/MOSIA/CTX0 | IRQ11 | | COMP1 |
| 67 | | P22 | D13 [A13/D13] | MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/ MTIOC9B/TMRI2/ TMO4 | RXD8/SMISO8/SSCL8/ RXD12/SMISO12/ SSCL12/RXD12/ MISOA/CRX0 | IRQ10 | | ADTRG2#/ COMP2 |
| 68 | | P21 | D14 [A14/D14] | MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/ TMC14 | TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/MOSIA | IRQ6-DS | AN217 | ADTRG1#/ COMP5 |
| 69 | | P20 | D15 [A15/D15] | MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/ TMRI4 | CTS8#/RTS8#/SS8#/ SCK8/RSPCKA | IRQ7-DS | AN216 | ADTRG0#/ COMP4 |
| 70 | | P65 | A12 | | | IRQ9 | AN211/ CMPC53/ DA1 | |
| 71 | | P64 | A13 | | | IRQ8 | AN210/ CMPC33/ DA0 | |

Table 1.8 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and without USB pin) (4/5)

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|-----------|--|--|-------------------------|-----------------------------|--------|
| 72 | AVCC2 | | | | | | | |
| 73 | AVSS2 | | | | | | | |
| 74 | | P63 | A12*/A14 | | | IRQ7 | AN209/ CMPC23 | |
| 75 | | P62 | A13*/A15 | | | IRQ6 | AN208/ CMPC43 | |
| 76 | | P61 | A14*/A16 | | | IRQ5 | AN207/ CMPC13 | |
| 77 | | P60 | A15*/A17 | | | IRQ4 | AN206/ CMPC03 | |
| 78 | | P55 | A16*/A18 | | | IRQ3 | AN203/ CMPC32 | |
| 79 | | P54 | A17*/A19 | | | IRQ2 | AN202/ CMPC22 | |
| 80 | | P53 | A18*/A20 | | | IRQ1 | AN201/ CMPC12 | |
| 81 | | P52 | | | | IRQ0 | AN200/ CMPC02 | |
| 82 | | P47 | | | | | AN103 | |
| 83 | | P46 | | | | | AN102/ CMPC50/ CMPC51 | |
| 84 | | P45 | | | | | AN101/ CMPC40/ CMPC41 | |
| 85 | | P44 | | | | | AN100/ CMPC30/ CMPC31 | |
| 86 | | PH4 | | | | | AN107/ PGAVSS1 | |
| 87 | | P43 | | | | | AN003 | |
| 88 | | P42 | | | | | AN002/ CMPC20/ CMPC21 | |
| 89 | | P41 | | | | | AN001/ CMPC10/ CMPC11 | |
| 90 | | P40 | | | | | AN000/ CMPC00/ CMPC01 | |
| 91 | | PH0 | | | | | AN007/ PGAVSS0 | |
| 92 | AVCC1 | | | | | | | |
| 93 | AVCC0 | | | | | | | |
| 94 | AVSS0 | | | | | | | |
| 95 | AVSS1 | | | | | | | |
| 96 | | P82 | ALE/WAIT# | MTIC5U/MTIC5U#/ TMO4 | SCK6/SCK12 | IRQ3 | | COMP5 |
| 97 | | P81 | CS2# | MTIC5V/MTIC5V#/ TMCi4 | TXD6/SMOSI6/SSDA6/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12 | | | COMP4 |
| 98 | | P80 | CS1# | MTIC5W/MTIC5W#/ TMRi4 | RXD6/SMISO6/SSCL6/ RXD12/SMISO12/ SSCL12/RXDX12 | IRQ5 | | COMP3 |

**Table 1.8 List of Pin and Pin Functions (100-pin with PGA pseudo-differential input and without USB pin)
(5/5)**

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|-----|---|--|-------------------------|--------|--------|
| 99 | | P11 | RD# | MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/ MTIOC9D/GTIOC3B/ GTETRG/GTIOC3B#/ GTETRG/TMO3/ POE9# | | IRQ1-DS | | |
| 100 | | P10 | | MTIOC9B/MTCLKD/ MTIOC9B#/MTCLKD#/ GTETRGB/GTETRGD/ TMR13/POE12# | CTS6#/RTS6#/SS6# | IRQ0-DS | | |

Note 1. These pins are only enabled for products with 128 Kbytes of RAM.

Table 1.9 List of Pin and Pin Functions (100-pin without PGA pseudo-differential input and without USB pin) (1/5)

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|---------------------|--|---|-------------------------|--------|-----------------|
| 1 | | PE5 | BCLK | MTIOC9D/MTIOC9D#/ GTIOC3A/GTETRGB/ GTIOC3A#/GTETRGD | SCK9/CTS9#/RTS9#/ SS9# | IRQ0 | | ADST0 |
| 2 | EMLE | | | | | | | |
| 3 | VSS | | | | | | | |
| 4 | UB | P00 | A11 | MTIOC9A/MTIOC9A#/ CACREF | RXD9/SMISO9/SSCL9/ RXD12/SMISO12/ SSCL12/RXD12 | IRQ2 | | ADST1/ COMP0 |
| 5 | VCL | | | | | | | |
| 6 | MD/FINED | | | | | | | |
| 7 | | P01 | A10 | MTIOC9C/MTIOC9C#/ GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE12# | TXD9/SMOSI9/SSDA9/ TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12 | IRQ4 | | ADST2/ COMP1 |
| 8 | | PE4 | A9 | MTCLKC/MTCLKC#/ GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE10# | SCK9 | IRQ1 | | |
| 9 | | PE3 | A8 | MTCLKD/MTCLKD#/ GTETRGA/GTETRGB/ GTETRGC/GTETRGD/ POE11# | CTS9#/RTS9#/SS9# | IRQ2-DS | | |
| 10 | RES# | | | | | | | |
| 11 | XTAL | P37 | | | | | | |
| 12 | VSS | | | | | | | |
| 13 | EXTAL | P36 | | | | | | |
| 14 | VCC | | | | | | | |
| 15 | | PE2 | | POE10# | | NMI | | |
| 16 | | PE1 | WR0#/WR# | MTIOC9D/MTIOC9D#/ TMO5 | CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/ SS12#/SSLA3 | IRQ15 | | |
| 17 | | PE0 | WR1#/BC1#/ WAIT# | MTIOC9B/MTIOC9B#/ TMC11/TMC15 | RXD5/SMISO5/SSCL5/ SSLA2/CRX0 | IRQ7 | | |
| 18 | TRST# | PD7 | | MTIOC9A/MTIOC9A#/ GTIOC0A/GTIOC3A/ GTIOC0A#/GTIOC3A#/ TMR11/TMR15 | TXD5/SMOSI5/SSDA5/ SSLA1/CTX0 | IRQ8 | | |
| 19 | TMS | PD6 | | MTIOC9C/MTIOC9C#/ GTIOC0B/GTIOC3B/ GTIOC0B#/GTIOC3B#/ TMO1 | CTS1#/RTS1#/SS1#/ CTS11#/RTS11#/ SS11#/SSLA0 | IRQ5 | | ADST0 |
| 20 | TDI | PD5 | | GTIOC1A/GTETRGA/ GTIOC1A#/TMR10/ TMR16 | RXD1/SMISO1/SSCL1/ RXD11/SMISO11/ SSCL11 | IRQ6 | | |
| 21 | TCK | PD4 | | GTIOC1B/GTETRGB/ GTIOC1B#/TMC10/ TMC16 | SCK1/SCK11 | IRQ2 | | |
| 22 | TDO | PD3 | | GTIOC2A/GTETRGC/ GTIOC2A#/TMO0 | TXD1/SMOSI1/SSDA1/ TXD11/SMOSI11/ SSDA11 | | | |
| 23 | TRCLK | PD2 | A7 | GTIOC2B/GTIOC0A/ GTIOC2B#/GTIOC0A#/ TMC11/TMO4 | SCK5/SCK8/MOSIA | | | |
| 24 | TRDATA3 | PD1 | A6 | GTIOC3A/GTIOC0B/ GTIOC3A#/GTIOC0B#/ TMO2 | RXD8/SMISO8/SSCL8/ MISOA | | | |
| 25 | TRDATA2 | PD0 | A5 | GTIOC3B/GTIOC1A/ GTIOC3B#/GTIOC1A#/ TMO6 | TXD8/SMOSI8/SSDA8/ RSPCKA | | | |
| 26 | TRDATA1 | PB7 | A4 | GTIOC1B/GTIOC1B# | SCK5/SCK11/SCK12 | | | |

Table 1.9 List of Pin and Pin Functions (100-pin without PGA pseudo-differential input and without USB pin) (2/5)

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|--------------|---|--|-------------------------|--------|---------|
| 27 | TRDATA0 | PB6 | A3 | GTIOC2A/GTIOC2A# | RXD5/SMISO5/SSCL5/ RXD11/SMISO11/ SSCL11/RXD12/ SMISO12/SSCL12/ RDX12/CRX0 | IRQ2 | | |
| 28 | TRSYNC | PB5 | A2 | GTIOC2B/GTIOC2B# | TXD5/SMOSI5/SSDA5/ TXD11/SMOSI11/ SSDA11/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0 | | | |
| 29 | VCC | | | | | | | |
| 30 | | PB4 | A1 | GTETRG/GTETRGB/ GTETRGC/GTETRGD/ POE8# | CTS5#/RTS5#/SS5#/ SCK11/CTS11#/ RTS11#/SS11# | IRQ3-DS | | |
| 31 | VSS | | | | | | | |
| 32 | | PB3 | A7*1 | MTIOC0A/MTIOC0A#/ CACREF | SCK6/RSPCKA | IRQ9 | | |
| 33 | | PB2 | A6*1 | MTIOC0B/MTIOC0B#/ GTADSM0/TMRI0 | TXD6/SMOSI6/SSDA6/ SDA | | | ADSM0 |
| 34 | | PB1 | A5*1 | MTIOC0C/MTIOC0C#/ GTADSM1/TMCI0 | RXD6/SMISO6/SSCL6/ SCL | IRQ4 | | ADSM1 |
| 35 | | PB0 | A0/A4*1/BC0# | MTIOC0D/MTIOC0D#/ TMO0 | TXD6/SMOSI6/SSDA6/ CTS11#/RTS11#/ SS11#/MOSIA | IRQ8 | | ADTRG2# |
| 36 | | PA5 | A3*1 | MTIOC1A/MTIOC1A#/ TMCI3 | RXD6/SMISO6/SSCL6/ RXD8/SMISO8/SSCL8/ MISOA | IRQ1 | | ADTRG1# |
| 37 | | PA4 | A2*1 | MTIOC1B/MTIOC1B#/ TMCI7 | SCK6/TXD8/SMOSI8/ SSDA8/RSPCKA | | | ADTRG0# |
| 38 | | PA3 | A1*1 | MTIOC2A/MTIOC2A#/ GTADSM0/TMRI7 | TXD9/SMOSI9/SSDA9/ SCK8/SSLA0 | | | |
| 39 | | PA2 | A0/BC0# | MTIOC2B/MTIOC2B#/ GTADSM1/TMO7 | CTS6#/RTS6#/SS6#/ RXD9/SMISO9/SSCL9/ SCK11*1/SSLA1 | | | |
| 40 | | PA1 | | MTIOC6A/MTIOC6A#/ TMO4 | TXD9/SMOSI9/SSDA9/ RXD11/SMISO11/ SSCL11/SSLA2/CRX0 | IRQ14-DS | | ADTRG0# |
| 41 | | PA0 | | MTIOC6C/MTIOC6C#/ TMO2 | SCK9/TXD11/SMOSI11/ SSDA11/SSLA3/CTX0 | | | |
| 42 | VCC | | | | | | | |
| 43 | | P96 | CS0#/WAIT# | GTETRG/GTETRGB/ GTETRGC/GTETRGD/ POE4# | CTS8#/RTS8#/SS8# | IRQ4-DS | | |
| 44 | VSS | | | | | | | |
| 45 | | P95 | | MTIOC6B/MTIOC6B#/ GTIOC4A/GTIOC7A/ GTIOC4A#GTIOC7A# | | | | |
| 46 | | P94 | | MTIOC7A/MTIOC7A#/ GTIOC5A/GTIOC8A/ GTIOC5A#GTIOC8A# | | | | |
| 47 | | P93 | | MTIOC7B/MTIOC7B#/ GTIOC6A/GTIOC9A/ GTIOC6A#GTIOC9A# | | | | |
| 48 | | P92 | | MTIOC6D/MTIOC6D#/ GTIOC4B/GTIOC7B/ GTIOC4B#GTIOC7B# | | | | |
| 49 | | P91 | | MTIOC7C/MTIOC7C#/ GTIOC5B/GTIOC8B/ GTIOC5B#GTIOC8B# | | | | |
| 50 | | P90 | | MTIOC7D/MTIOC7D#/ GTIOC6B/GTIOC9B/ GTIOC6B#GTIOC9B# | | | | |

Table 1.9 List of Pin and Pin Functions (100-pin without PGA pseudo-differential input and without USB pin) (3/5)

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|---------------|---|---|-------------------------|--------------------------|-------------------|
| 51 | | P76 | D0 [A0/D0] | MTIOC4D/MTIOC4D#/ GTIOC2B/GTIOC6B/ GTIOC2B#/GTIOC6B# | | | | |
| 52 | | P75 | D1 [A1/D1] | MTIOC4C/MTIOC4C#/ GTIOC1B/GTIOC5B/ GTIOC1B#/GTIOC5B# | | | | |
| 53 | | P74 | D2 [A2/D2] | MTIOC3D/MTIOC3D#/ GTIOC0B/GTIOC4B/ GTIOC0B#/GTIOC4B# | | | | |
| 54 | | P73 | D3 [A3/D3] | MTIOC4B/MTIOC4B#/ GTIOC2A/GTIOC6A/ GTIOC2A#/GTIOC6A# | | | | |
| 55 | | P72 | D4 [A4/D4] | MTIOC4A/MTIOC4A#/ GTIOC1A/GTIOC5A/ GTIOC1A#/GTIOC5A# | | | | |
| 56 | | P71 | D5 [A5/D5] | MTIOC3B/MTIOC3B#/ GTIOC0A/GTIOC4A/ GTIOC0A#/GTIOC4A# | | | | |
| 57 | | P70 | D6 [A6/D6] | GTETRG/GTETRGB/ GTETRGC/GTETRGD/ POE0# | CTS9#/RTS9#/SS9# | IRQ5-DS | | |
| 58 | | P33 | D7 [A7/D7] | MTIOC3A/MTCLKA/ MTIOC3A#/MTCLKA#/ GTIOC3B/GTIOC3B#/ TMO0 | SSLA3 | IRQ13-DS | | |
| 59 | | P32 | D8 [A8/D8] | MTIOC3C/MTCLKB/ MTIOC3C#/MTCLKB#/ GTIOC3A/GTIOC3A#/ TMO6 | SSLA2 | IRQ12-DS | | |
| 60 | VCC | | | | | | | |
| 61 | | P31 | D9 [A9/D9] | MTIOC0A/MTCLKC/ MTIOC0A#/MTCLKC#/ TMR16 | SSLA1 | IRQ6 | | |
| 62 | VSS | | | | | | | |
| 63 | | P30 | D10 [A10/D10] | MTIOC0B/MTCLKD/ MTIOC0B#/MTCLKD#/ TMC16 | SCK8/CTS8#/RTS8#/ SS8#/SSLA0 | IRQ7 | | COMP3 |
| 64 | | P24 | D11 [A11/D11] | MTIC5U/MTIC5U#/ TMC12/TMO6 | CTS8#/RTS8#/SS8#/ SCK8/RSPCKA | IRQ4 | | COMP0 |
| 65 | | P23 | D12 [A12/D12] | MTIC5V/MTIC5V#/ TMO2/CACREF | TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/MOSIA/CTX0 | IRQ11 | | COMP1 |
| 66 | | P22 | D13 [A13/D13] | MTIC5W/MTCLKD/ MTIC5W#/MTCLKD#/ MTIOC9B/TMR12/ TMO4 | RXD8/SMOSI8/SSCL8/ RXD12/SMOSI12/ SSCL12/RXDX12/ MISOA/CRX0 | IRQ10 | | ADTRG2#/ COMP2 |
| 67 | | P21 | D14 [A14/D14] | MTIOC9A/MTCLKA/ MTIOC9A#/MTCLKA#/ TMC14 | TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/MOSIA | IRQ6-DS | AN217 | ADTRG1#/ COMP5 |
| 68 | | P20 | D15 [A15/D15] | MTIOC9C/MTCLKB/ MTIOC9C#/MTCLKB#/ TMR14 | CTS8#/RTS8#/SS8#/ SCK8/RSPCKA | IRQ7-DS | AN216 | ADTRG0#/ COMP4 |
| 69 | | P65 | A12 | | | IRQ9 | AN211/ CMPC53/ DA1 | |
| 70 | | P64 | A13 | | | IRQ8 | AN210/ CMPC33/ DA0 | |
| 71 | AVCC2 | | | | | | | |
| 72 | AVCC2 | | | | | | | |

Table 1.9 List of Pin and Pin Functions (100-pin without PGA pseudo-differential input and without USB pin) (4/5)

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|-----------|---|---|-------------------------|-----------------------------|--------|
| 73 | AVSS2 | | | | | | | |
| 74 | | P63 | A12*/A14 | | | IRQ7 | AN209/ CMPC23 | |
| 75 | | P62 | A13*/A15 | | | IRQ6 | AN208/ CMPC43 | |
| 76 | | P61 | A14*/A16 | | | IRQ5 | AN207/ CMPC13 | |
| 77 | | P60 | A15*/A17 | | | IRQ4 | AN206/ CMPC03 | |
| 78 | | P55 | A16*/A18 | | | IRQ3 | AN203/ CMPC32 | |
| 79 | | P54 | A17*/A19 | | | IRQ2 | AN202/ CMPC22 | |
| 80 | | P53 | A18*/A20 | | | IRQ1 | AN201/ CMPC12 | |
| 81 | | P52 | | | | IRQ0 | AN200/ CMPC02 | |
| 82 | | P51 | | | | | AN205/ CMPC52 | |
| 83 | | P50 | | | | | AN204/ CMPC42 | |
| 84 | | P47 | | | | | AN103 | |
| 85 | | P46 | | | | | AN102/ CMPC50/ CMPC51 | |
| 86 | | P45 | | | | | AN101/ CMPC40/ CMPC41 | |
| 87 | | P44 | | | | | AN100/ CMPC30/ CMPC31 | |
| 88 | | P43 | | | | | AN003 | |
| 89 | | P42 | | | | | AN002/ CMPC20/ CMPC21 | |
| 90 | | P41 | | | | | AN001/ CMPC10/ CMPC11 | |
| 91 | | P40 | | | | | AN000/ CMPC00/ CMPC01 | |
| 92 | AVCC1 | | | | | | | |
| 93 | AVCC0 | | | | | | | |
| 94 | AVSS0 | | | | | | | |
| 95 | AVSS1 | | | | | | | |
| 96 | | P82 | ALE/WAIT# | MTIC5U/MTIC5U#/ TMO4 | SCK6/SCK12 | IRQ3 | | COMP5 |
| 97 | | P81 | CS2# | MTIC5V/MTIC5V#/ TMC14 | TXD6/SMOSI6/SSDA6/ TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12 | | | COMP4 |
| 98 | | P80 | CS1# | MTIC5W/MTIC5W#/ TMR14 | RXD6/SMISO6/SSCL6/ RXD12/SMISO12/ SSCL12/RXD12 | IRQ5 | | COMP3 |
| 99 | | P11 | RD# | MTIOC3A/MTCLKC/ MTIOC3A#/MTCLKC#/ MTIOC9D/GTIOC3B/ GTETRGA/GTIOC3B#/ GTETRGC/TMO3/ POE9# | | IRQ1-DS | | |

Table 1.9 List of Pin and Pin Functions (100-pin without PGA pseudo-differential input and without USB pin) (5/5)

| Pin Number 100-Pin LFQFP | Power Supply Clock System Control | I/O Port | Bus | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|--------------------------------|---|----------|-----|--|--|-------------------------|--------|--------|
| 100 | | P10 | | MTIOC9B/MTCLKD/ MTIOC9B#/MTCLKD#/ GTETRGE/GTETRGD/ TMR13/POE12# | CTS6#/RTS6#/SS6# | IRQ0-DS | | |

Note 1. These pins are only enabled for products with 128 Kbytes of RAM.

Table 1.10 List of Pin and Pin Functions (80-pin with PGA pseudo-differential input and without USB pin) (1/5)

| Pin Number | Power Supply Clock System Control | I/O Port | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|------------|---|----------|--|--|-------------------------|--------|-----------------|
| 1 | EMLE | | | | | | |
| 2 | VSS | | | | | | |
| 3 | UB | P00 | MTIOC9A/ MTIOC9A#/ CACREF | RXD9/SMISO9/SSCL9/ RXD12/SMISO12/ SSCL12/RXDX12 | IRQ2 | | ADST1/ COMP0 |
| 4 | VCL | | | | | | |
| 5 | MD/FINED | | | | | | |
| 6 | | P01 | MTIOC9C/ MTIOC9C#/ GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/ POE12# | TXD9/SMOSI9/SSDA9/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12 | IRQ4 | | ADST2/ COMP1 |
| 7 | | PE4 | MTCLKC/ MTCLKC#/ GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/ POE10# | SCK9 | IRQ1 | | |
| 8 | | PE3 | MTCLKD/ MTCLKD#/ GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/ POE11# | CTS9#/RTS9#/SS9# | IRQ2-DS | | |
| 9 | RES# | | | | | | |
| 10 | XTAL | P37 | | | | | |
| 11 | VSS | | | | | | |
| 12 | EXTAL | P36 | | | | | |
| 13 | VCC | | | | | | |
| 14 | | PE2 | POE10# | | NMI | | |
| 15 | TRST# | PD7 | MTIOC9A/ MTIOC9A#/ GTIOC0A/ GTIOC3A/ GTIOC0A#/ GTIOC3A#/ TMR11/TMR15 | TXD5/SMOSI5/SSDA5/ SSLA1/CTX0 | IRQ8 | | |
| 16 | TMS | PD6 | MTIOC9C/ MTIOC9C#/ GTIOC0B/ GTIOC3B/ GTIOC0B#/ GTIOC3B#/ TMO1 | CTS1#/RTS1#/SS1#/ CTS11#/RTS11#/SS11#/ SSLA0 | IRQ5 | | ADST0 |
| 17 | TDI | PD5 | GTIOC1A/ GTETRGA/ GTIOC1A#/ TMR10/TMR16 | RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11 | IRQ6 | | |
| 18 | TCK | PD4 | GTIOC1B/ GTETRGB/ GTIOC1B#/ TMC10/TMC16 | SCK1/SCK11 | IRQ2 | | |
| 19 | TDO | PD3 | GTIOC2A/ GTETRGC/ GTIOC2A#/ TMO0 | TXD1/SMOSI1/SSDA1/ TXD11/SMOSI11/SSDA11 | | | |

Table 1.10 List of Pin and Pin Functions (80-pin with PGA pseudo-differential input and without USB pin) (2/5)

| Pin Number | Power Supply Clock System Control | I/O Port | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|------------|---|----------|--|--|-------------------------|--------|---------|
| 20 | | PD2 | GTIOC2B/ GTIOC0A/ GTIOC2B#/ GTIOC0A#/ TMC11/TMO4 | SCK5/SCK8/MOSIA | | | |
| 21 | | PB6 | GTIOC2A/ GTIOC2A# | RXD5/SMISO5/SSCL5/ RXD11/SMISO11/ SSCL11/RXD12/ SMISO12/SSCL12/ RXDX12/CRX0 | IRQ2 | | |
| 22 | | PB5 | GTIOC2B/ GTIOC2B# | TXD5/SMOSI5/SSDA5/ TXD11/SMOSI11/ SSDA11/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0 | | | |
| 23 | VCC | | | | | | |
| 24 | | PB4 | GTETRGA/ GTETRQB/ GTETRGC/ GTETRGD/ POE8# | CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/ SS11# | IRQ3-DS | | |
| 25 | VSS | | | | | | |
| 26 | | PB3 | MTIOC0A/ MTIOC0A#/ CACREF | SCK6/RSPCKA | IRQ9 | | |
| 27 | | PB2 | MTIOC0B/ MTIOC0B#/ GTADSM0/ TMRI0 | TXD6/SMOSI6/SSDA6/ SDA | | | ADSM0 |
| 28 | | PB1 | MTIOC0C/ MTIOC0C#/ GTADSM1/ TMC10 | RXD6/SMISO6/SSCL6/ SCL | IRQ4 | | ADSM1 |
| 29 | | PB0 | MTIOC0D/ MTIOC0D#/ TMO0 | TXD6/SMOSI6/SSDA6/ CTS11#/RTS11#/SS11#/ MOSIA | IRQ8 | | ADTRG2# |
| 30 | | PA5 | MTIOC1A/ MTIOC1A#/ TMC13 | RXD6/SMISO6/SSCL6/ RXD8/SMISO8/SSCL8/ MISOA | IRQ1 | | ADTRG1# |
| 31 | | PA3 | MTIOC2A/ MTIOC2A#/ GTADSM0/ TMRI7 | TXD9/SMOSI9/SSDA9/ SCK8/SSLA0 | | | |
| 32 | VCC | | | | | | |
| 33 | | P96 | GTETRGA/ GTETRQB/ GTETRGC/ GTETRGD/ POE4# | CTS8#/RTS8#/SS8# | IRQ4-DS | | |
| 34 | VSS | | | | | | |
| 35 | | P95 | MTIOC6B/ MTIOC6B#/ GTIOC4A/ GTIOC7A/ GTIOC4A#/ GTIOC7A# | | | | |
| 36 | | P94 | MTIOC7A/ MTIOC7A#/ GTIOC5A/ GTIOC8A/ GTIOC5A#/ GTIOC8A# | | | | |

Table 1.10 List of Pin and Pin Functions (80-pin with PGA pseudo-differential input and without USB pin) (3/5)

| Pin Number | Power Supply Clock System Control | I/O Port | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|------------|---|----------|--|--|-------------------------|--------|--------|
| 37 | | P93 | MTIOC7B/ MTIOC7B#/ GTIOC6A/ GTIOC9A/ GTIOC6A#/ GTIOC9A# | | | | |
| 38 | | P92 | MTIOC6D/ MTIOC6D#/ GTIOC4B/ GTIOC7B/ GTIOC4B#/ GTIOC7B# | | | | |
| 39 | | P91 | MTIOC7C/ MTIOC7C#/ GTIOC5B/ GTIOC8B/ GTIOC5B#/ GTIOC8B# | | | | |
| 40 | | P90 | MTIOC7D/ MTIOC7D#/ GTIOC6B/ GTIOC9B/ GTIOC6B#/ GTIOC9B# | | | | |
| 41 | | P76 | MTIOC4D/ MTIOC4D#/ GTIOC2B/ GTIOC6B/ GTIOC2B#/ GTIOC6B# | | | | |
| 42 | | P75 | MTIOC4C/ MTIOC4C#/ GTIOC1B/ GTIOC5B/ GTIOC1B#/ GTIOC5B# | | | | |
| 43 | | P74 | MTIOC3D/ MTIOC3D#/ GTIOC0B/ GTIOC4B/ GTIOC0B#/ GTIOC4B# | | | | |
| 44 | | P73 | MTIOC4B/ MTIOC4B#/ GTIOC2A/ GTIOC6A/ GTIOC2A#/ GTIOC6A# | | | | |
| 45 | | P72 | MTIOC4A/ MTIOC4A#/ GTIOC1A/ GTIOC5A/ GTIOC1A#/ GTIOC5A# | | | | |
| 46 | | P71 | MTIOC3B/ MTIOC3B#/ GTIOC0A/ GTIOC4A/ GTIOC0A#/ GTIOC4A# | | | | |
| 47 | | P70 | GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/ POE0# | CTS9#/RTS9#/SS9# | IRQ5-DS | | |
| 48 | VCC | | | | | | |

Table 1.10 List of Pin and Pin Functions (80-pin with PGA pseudo-differential input and without USB pin) (4/5)

| Pin Number | Power Supply Clock System Control | I/O Port | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|------------|---|----------|--|---|-------------------------|-------------------------|-------------------|
| 49 | | P31 | MTIOC0A/ MTCLKC/ MTIOC0A#/ MTCLKC#/ TMR16 | SSLA1 | IRQ6 | | |
| 50 | VSS | | | | | | |
| 51 | | P30 | MTIOC0B/ MTCLKD/ MTIOC0B#/ MTCLKD#/ TMC16 | SCK8/CTS8#/RTS8#/ SS8#/SSLA0 | IRQ7 | | COMP3 |
| 52 | | P27 | MTIOC1A/ MTIOC0C/ MTIOC1A#/ MTIOC0C#/ POE9# | | IRQ15 | | |
| 53 | | P22 | MTIC5W/ MTCLKD/ MTIC5W#/ MTCLKD#/ MTIOC9B/ TMR12/TMO4 | RXD8/SMISO8/SSCL8/ RXD12/SMISO12/ SSCL12/RXD12/ MISOA/CRX0 | IRQ10 | | ADTRG2#/ COMP2 |
| 54 | | P21 | MTIOC9A/ MTCLKA/ MTIOC9A#/ MTCLKA#/ TMC14 | TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12/MOSIA | IRQ6-DS | AN217 | ADTRG1#/ COMP5 |
| 55 | | P20 | MTIOC9C/ MTCLKB/ MTIOC9C#/ MTCLKB#/ TMR14 | CTS8#/RTS8#/SS8#/ SCK8/RSPCKA | IRQ7-DS | AN216 | ADTRG0#/ COMP4 |
| 56 | | P65 | | | IRQ9 | AN211/CMPC53/ DA1 | |
| 57 | | P64 | | | IRQ8 | AN210/CMPC33/ DA0 | |
| 58 | AVCC2 | | | | | | |
| 59 | AVSS2 | | | | | | |
| 60 | | P62 | | | IRQ6 | AN208/CMPC43 | |
| 61 | | P55 | | | IRQ3 | AN203/CMPC32 | |
| 62 | | P54 | | | IRQ2 | AN202/CMPC22 | |
| 63 | | P53 | | | IRQ1 | AN201/CMPC12 | |
| 64 | | P52 | | | IRQ0 | AN200/CMPC02 | |
| 65 | | P47 | | | | AN103 | |
| 66 | | P46 | | | | AN102/CMPC50/ CMPC51 | |
| 67 | | P45 | | | | AN101/CMPC40/ CMPC41 | |
| 68 | | P44 | | | | AN100/CMPC30/ CMPC31 | |
| 69 | | PH4 | | | | AN107/PGAVSS1 | |
| 70 | | P43 | | | | AN003 | |
| 71 | | P42 | | | | AN002/CMPC20/ CMPC21 | |
| 72 | | P41 | | | | AN001/CMPC10/ CMPC11 | |
| 73 | | P40 | | | | AN000/CMPC00/ CMPC01 | |
| 74 | | PH0 | | | | AN007/PGAVSS0 | |

Table 1.10 List of Pin and Pin Functions (80-pin with PGA pseudo-differential input and without USB pin) (5/5)

| Pin Number 80-Pin LQFP 80-Pin LFQFP | Power Supply Clock System Control | I/O Port | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|---|---|----------|---|--|-------------------------|--------|--------|
| 75 | AVCC1 | | | | | | |
| 76 | AVCC0 | | | | | | |
| 77 | AVSS0 | | | | | | |
| 78 | AVSS1 | | | | | | |
| 79 | | P11 | MTIOC3A/ MTCLKC/ MTIOC3A#/ MTCLKC#/ MTIOC9D/ GTIOC3B/ GTETRGA/ GTIOC3B#/ GTETRGC/ TMO3/POE9# | | IRQ1-DS | | |
| 80 | | P10 | MTIOC9B/ MTCLKD/ MTIOC9B#/ MTCLKD#/ GTETRGB/ GTETRGD/ TMR13/POE12# | CTS6#/RTS6#/SS6# | IRQ0-DS | | |

Table 1.11 List of Pin and Pin Functions (64-pin with PGA pseudo-differential input and without USB pin) (1/4)

| Pin Number | Power Supply Clock System Control | I/O Port | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|------------|---|----------|--|--|-------------------------|--------|-----------------|
| 1 | EMLE | | | | | | |
| 2 | UB | P00 | MTIOC9A/ MTIOC9A#/ CACREF | RXD9/SMISO9/SSCL9/ RXD12/SMISO12/ SSCL12/RXD12 | IRQ2 | | ADST1/ COMP0 |
| 3 | VCL | | | | | | |
| 4 | MD/FINED | | | | | | |
| 5 | | P01 | MTIOC9C/ MTIOC9C#/ GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/ POE12# | TXD9/SMOSI9/SSDA9/ TXD12/SMOSI12/ SSDA12/TXD12/ SIOX12 | IRQ4 | | ADST2/ COMP1 |
| 6 | RES# | | | | | | |
| 7 | XTAL | P37 | | | | | |
| 8 | VSS | | | | | | |
| 9 | EXTAL | P36 | | | | | |
| 10 | VCC | | | | | | |
| 11 | | PE2 | POE10# | | NMI | | |
| 12 | TRST# | PD7 | MTIOC9A/ MTIOC9A#/ GTIOC0A/ GTIOC3A/ GTIOC0A#/ GTIOC3A#/ TMRI1/TMRI5 | TXD5/SMOSI5/SSDA5/ SSLA1/CTX0 | IRQ8 | | |
| 13 | TMS | PD6 | MTIOC9C/ MTIOC9C#/ GTIOC0B/ GTIOC3B/ GTIOC0B#/ GTIOC3B#/ TMO1 | CTS1#/RTS1#/SS1#/ CTS11#/RTS11#/SS11#/ SSLA0 | IRQ5 | | ADST0 |
| 14 | TDI | PD5 | GTIOC1A/ GTETRGA/ GTIOC1A#/ TMRI0/TMRI6 | RXD1/SMISO1/SSCL1/ RXD11/SMISO11/SSCL11 | IRQ6 | | |
| 15 | TCK | PD4 | GTIOC1B/ GTETRGB/ GTIOC1B#/ TMCI0/TMCI6 | SCK1/SCK11 | IRQ2 | | |
| 16 | TDO | PD3 | GTIOC2A/ GTETRGC/ GTIOC2A#/ TMO0 | TXD1/SMOSI1/SSDA1/ TXD11/SMOSI11/SSDA11 | | | |
| 17 | | PB6 | GTIOC2A/ GTIOC2A# | RXD5/SMISO5/SSCL5/ RXD11/SMISO11/ SSCL11/RXD12/ SMISO12/SSCL12/ RXDX12/CRX0 | IRQ2 | | |
| 18 | | PB5 | GTIOC2B/ GTIOC2B# | TXD5/SMOSI5/SSDA5/ TXD11/SMOSI11/ SSDA11/TXD12/ SMOSI12/SSDA12/ TXDX12/SIOX12/CTX0 | | | |
| 19 | | PB4 | GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/ POE8# | CTS5#/RTS5#/SS5#/ SCK11/CTS11#/RTS11#/ SS11# | IRQ3-DS | | |
| 20 | | PB3 | MTIOC0A/ MTIOC0A#/ CACREF | SCK6/RSPCKA | IRQ9 | | |

Table 1.11 List of Pin and Pin Functions (64-pin with PGA pseudo-differential input and without USB pin) (2/4)

| Pin Number | Power Supply Clock System Control | I/O Port | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|------------|-----------------------------------|----------|--|---|----------------------|--------|---------|
| 21 | | PB2 | MTIOC0B/ MTIOC0B#/ GTADSM0/ TMR10 | TXD6/SMOSI6/SSDA6/ SDA | | | ADSM0 |
| 22 | | PB1 | MTIOC0C/ MTIOC0C#/ GTADSM1/ TMC10 | RXD6/SMISO6/SSCL6/ SCL | IRQ4 | | ADSM1 |
| 23 | | PB0 | MTIOC0D/ MTIOC0D#/ TMO0 | TXD6/SMOSI6/SSDA6/ CTS11#/RTS11#/SS11#/ MOSIA | IRQ8 | | ADTRG2# |
| 24 | VCC | | | | | | |
| 25 | | P96 | GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/ POE4# | CTS8#/RTS8#/SS8# | IRQ4-DS | | |
| 26 | VSS | | | | | | |
| 27 | | P95 | MTIOC6B/ MTIOC6B#/ GTIOC4A/ GTIOC7A/ GTIOC4A#/ GTIOC7A# | | | | |
| 28 | | P94 | MTIOC7A/ MTIOC7A#/ GTIOC5A/ GTIOC8A/ GTIOC5A#/ GTIOC8A# | | | | |
| 29 | | P93 | MTIOC7B/ MTIOC7B#/ GTIOC6A/ GTIOC9A/ GTIOC6A#/ GTIOC9A# | | | | |
| 30 | | P92 | MTIOC6D/ MTIOC6D#/ GTIOC4B/ GTIOC7B/ GTIOC4B#/ GTIOC7B# | | | | |
| 31 | | P91 | MTIOC7C/ MTIOC7C#/ GTIOC5B/ GTIOC8B/ GTIOC5B#/ GTIOC8B# | | | | |
| 32 | | P90 | MTIOC7D/ MTIOC7D#/ GTIOC6B/ GTIOC9B/ GTIOC6B#/ GTIOC9B# | | | | |
| 33 | | P76 | MTIOC4D/ MTIOC4D#/ GTIOC2B/ GTIOC6B/ GTIOC2B#/ GTIOC6B# | | | | |
| 34 | | P75 | MTIOC4C/ MTIOC4C#/ GTIOC1B/ GTIOC5B/ GTIOC1B#/ GTIOC5B# | | | | |

Table 1.11 List of Pin and Pin Functions (64-pin with PGA pseudo-differential input and without USB pin) (3/4)

| Pin Number | Power Supply Clock System Control | I/O Port | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|------------|-----------------------------------|----------|--|--|----------------------|-------------------------|-------------------|
| 35 | | P74 | MTIOC3D/ MTIOC3D#/ GTIOC0B/ GTIOC4B/ GTIOC0B#/ GTIOC4B# | | | | |
| 36 | | P73 | MTIOC4B/ MTIOC4B#/ GTIOC2A/ GTIOC6A/ GTIOC2A#/ GTIOC6A# | | | | |
| 37 | | P72 | MTIOC4A/ MTIOC4A#/ GTIOC1A/ GTIOC5A/ GTIOC1A#/ GTIOC5A# | | | | |
| 38 | | P71 | MTIOC3B/ MTIOC3B#/ GTIOC0A/ GTIOC4A/ GTIOC0A#/ GTIOC4A# | | | | |
| 39 | | P70 | GTETRGA/ GTETRGB/ GTETRGC/ GTETRGD/ POE0# | CTS9#/RTS9#/SS9# | IRQ5-DS | | |
| 40 | VCC | | | | | | |
| 41 | VSS | | | | | | |
| 42 | | P22 | MTIC5W/ MTCLKD/ MTIC5W#/ MTCLKD#/ MTIOC9B/ TMR12/TMO4 | RXD8/SMISO8/SSCL8/ RXD12/SMISO12/ SSCL12/RXDX12/ MISOA/CRX0 | IRQ10 | | ADTRG2#/ COMP2 |
| 43 | | P21 | MTIOC9A/ MTCLKA/ MTIOC9A#/ MTCLKA#/ TMCI4 | TXD8/SMOSI8/SSDA8/ TXD12/SMOSI12/ SSDA12/TXDX12/ SIOX12/MOSIA | IRQ6-DS | AN217 | ADTRG1#/ COMP5 |
| 44 | | P20 | MTIOC9C/ MTCLKB/ MTIOC9C#/ MTCLKB#/ TMR14 | CTS8#/RTS8#/SS8#/ SCK8/RSPCKA | IRQ7-DS | AN216 | ADTRG0#/ COMP4 |
| 45 | | P65 | | | IRQ9 | AN211/CMPC53/ DA1 | |
| 46 | | P64 | | | IRQ8 | AN210/CMPC33/ DA0 | |
| 47 | AVCC2 | | | | | | |
| 48 | AVSS2 | | | | | | |
| 49 | | P54 | | | IRQ2 | AN202/CMPC22 | |
| 50 | | P53 | | | IRQ1 | AN201/CMPC12 | |
| 51 | | P52 | | | IRQ0 | AN200/CMPC02 | |
| 52 | | P46 | | | | AN102/CMPC50/ CMPC51 | |
| 53 | | P45 | | | | AN101/CMPC40/ CMPC41 | |
| 54 | | P44 | | | | AN100/CMPC30/ CMPC31 | |
| 55 | | PH4 | | | | AN107/PGAVSS1 | |

Table 1.11 List of Pin and Pin Functions (64-pin with PGA pseudo-differential input and without USB pin) (4/4)

| Pin Number | Power Supply Clock System Control | I/O Port | Timer (MTU, GPTW, TMR, POE, POEG, CAC) | Communications (SCI, RSPI, RIIC, CAN) | Interrupt (IRQ, NMI) | Analog | Others |
|------------|---|----------|---|--|-------------------------|-------------------------|--------|
| 56 | | P42 | | | | AN002/CMPC20/ CMPC21 | |
| 57 | | P41 | | | | AN001/CMPC10/ CMPC11 | |
| 58 | | P40 | | | | AN000/CMPC00/ CMPC01 | |
| 59 | | PH0 | | | | AN007/PGAVSS0 | |
| 60 | AVCC1 | | | | | | |
| 61 | AVCC0 | | | | | | |
| 62 | AVSS0 | | | | | | |
| 63 | AVSS1 | | | | | | |
| 64 | | P11 | MTIOC3A/ MTCLKC/ MTIOC3A#/ MTCLKC#/ MTIOC9D/ GTIOC3B/ GTETRGA/ GTIOC3B#/ GTETRGC/ TMO3/POE9# | | IRQ1-DS | | |

2. CPU

Figure 2.1 shows register set of the CPU.

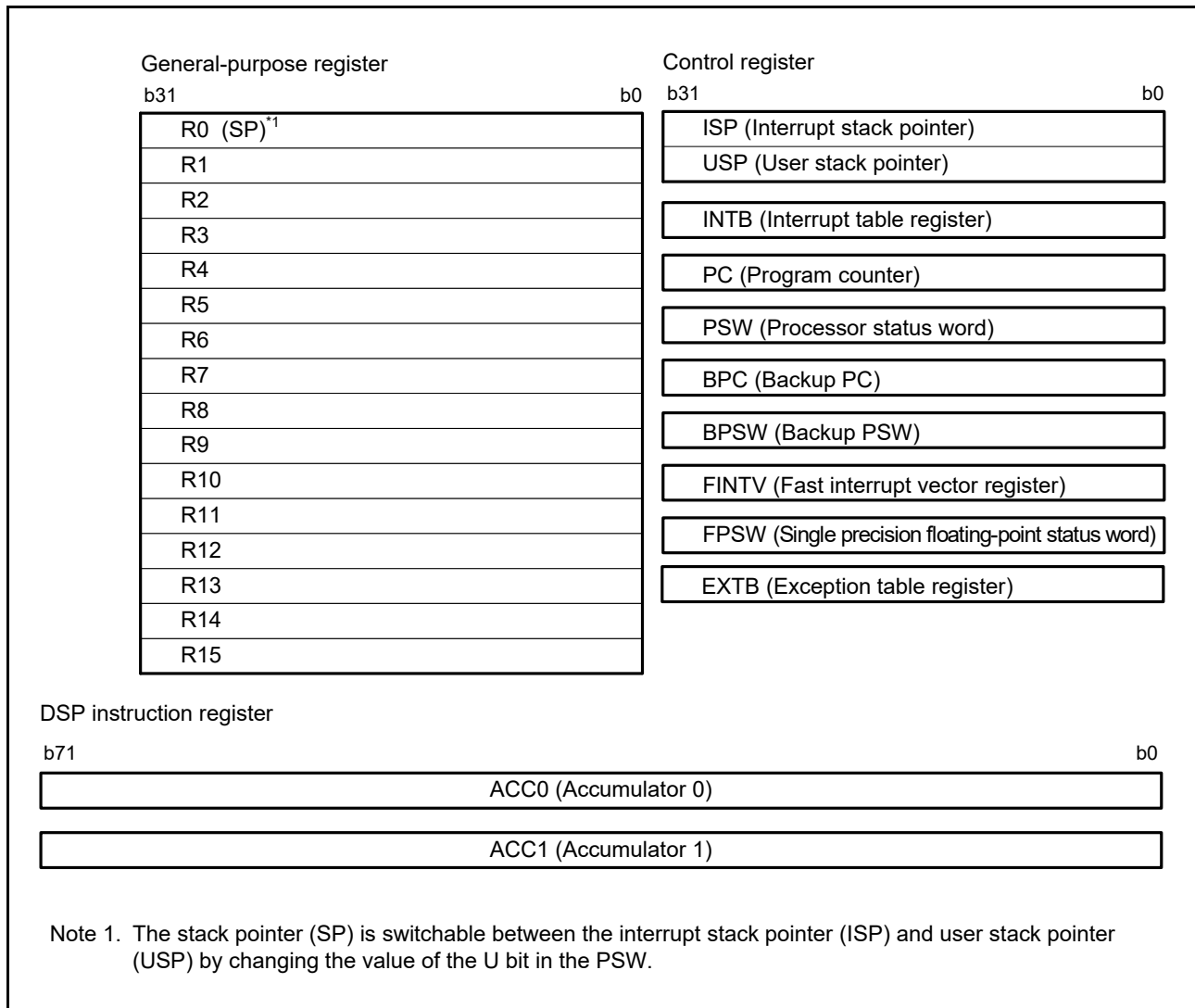


Figure 2.1 Register Set of the CPU

2.1 General-Purpose Registers (R0 to R15)

This CPU has sixteen 32-bit general-purpose registers (R0 to R15). R0 to R15 can be used as data registers or address registers.

R0, a general-purpose register, also functions as the stack pointer (SP).

The stack pointer is switched to operate as the interrupt stack pointer (ISP) or user stack pointer (USP) by the value of the stack pointer select bit (U) in the processor status word (PSW).

2.2 Control Registers

(1) Interrupt Stack Pointer (ISP) / User Stack Pointer (USP)

The stack pointer (SP) can be either of two types, the interrupt stack pointer (ISP) or the user stack pointer (USP). Whether the stack pointer operates as the ISP or USP depends on the value of the stack pointer select bit (U) in the processor status word (PSW).

(2) Exception Table Register (EXTB)

The exception table register (EXTB) specifies the address where the exception vector table starts.

(3) Interrupt Table Register (INTB)

The interrupt table register (INTB) specifies the address where the interrupt vector table starts.

(4) Program Counter (PC)

The program counter (PC) indicates the address of the instruction being executed.

(5) Processor Status Word (PSW)

The processor status word (PSW) indicates the results of instruction execution or the state of the CPU.

(6) Backup PC (BPC)

The backup PC (BPC) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the program counter (PC) are saved in the BPC register.

(7) Backup PSW (BPSW)

The backup PSW (BPSW) is provided to speed up response to interrupts.

After a fast interrupt has been generated, the contents of the processor status word (PSW) are saved in the BPSW. The allocation of bits in the BPSW corresponds to that in the PSW.

(8) Fast Interrupt Vector Register (FINTV)

The fast interrupt vector register (FINTV) is provided to speed up response to interrupts.

The FINTV register specifies a branch destination address when a fast interrupt has been generated.

(9) Single-Precision Floating-Point Status Word (FPSW)

The single-precision floating-point status word (FPSW) indicates the results of single-precision floating-point operations.

When an exception handling enable bit (Ej) enables the exception handling (Ej = 1), the exception cause can be identified by checking the corresponding Cj flag in the exception handling routine. If the exception handling is masked (Ej = 0), the occurrence of exception can be checked by reading the Fj flag at the end of a series of processing. Once the Fj flag has been set to 1, this value is retained until it is set to 0 by software (j = X, U, Z, O, or V).

2.3 Accumulator

The accumulator (ACC0 or ACC1) is a 72-bit register used for DSP instructions. The accumulator is handled as a 96-bit register for reading and writing. At this time, when bits 95 to 72 of the accumulator are read, the value where the value of bit 71 is sign extended is read. Writing to bits 95 to 72 of the accumulator is ignored. ACC0 is also used for the multiply and multiply-and-accumulate instructions; EMUL, EMULU, FMUL, MUL, and RMPA, in which case the prior value in ACC0 is modified by execution of the instruction.

Use the MVTACGU, MVTACHI, and MVTACLO instructions for writing to the accumulator. The MVTACGU, MVTACHI, and MVTACLO instructions write data to bits 95 to 64, the higher-order 32 bits (bits 63 to 32), and the lower-order 32 bits (bits 31 to 0), respectively.

Use the MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions for reading data from the accumulator. The MVFACGU, MVFACHI, MVFACMI, and MVFACLO instructions read data from the guard bits (bits 95 to 64), higher-order 32 bits (bits 63 to 32), the middle 32 bits (bits 47 to 16), and the lower-order 32 bits (bits 31 to 0), respectively.

3. Address Space

3.1 Address Space

This MCU has a 4-Gbyte address space, consisting of the range of addresses from 0000 0000h to FFFF FFFFh. Figure 3.1 shows the memory maps in the respective operating modes. Accessible areas will differ according to the operating mode and states of control bits.

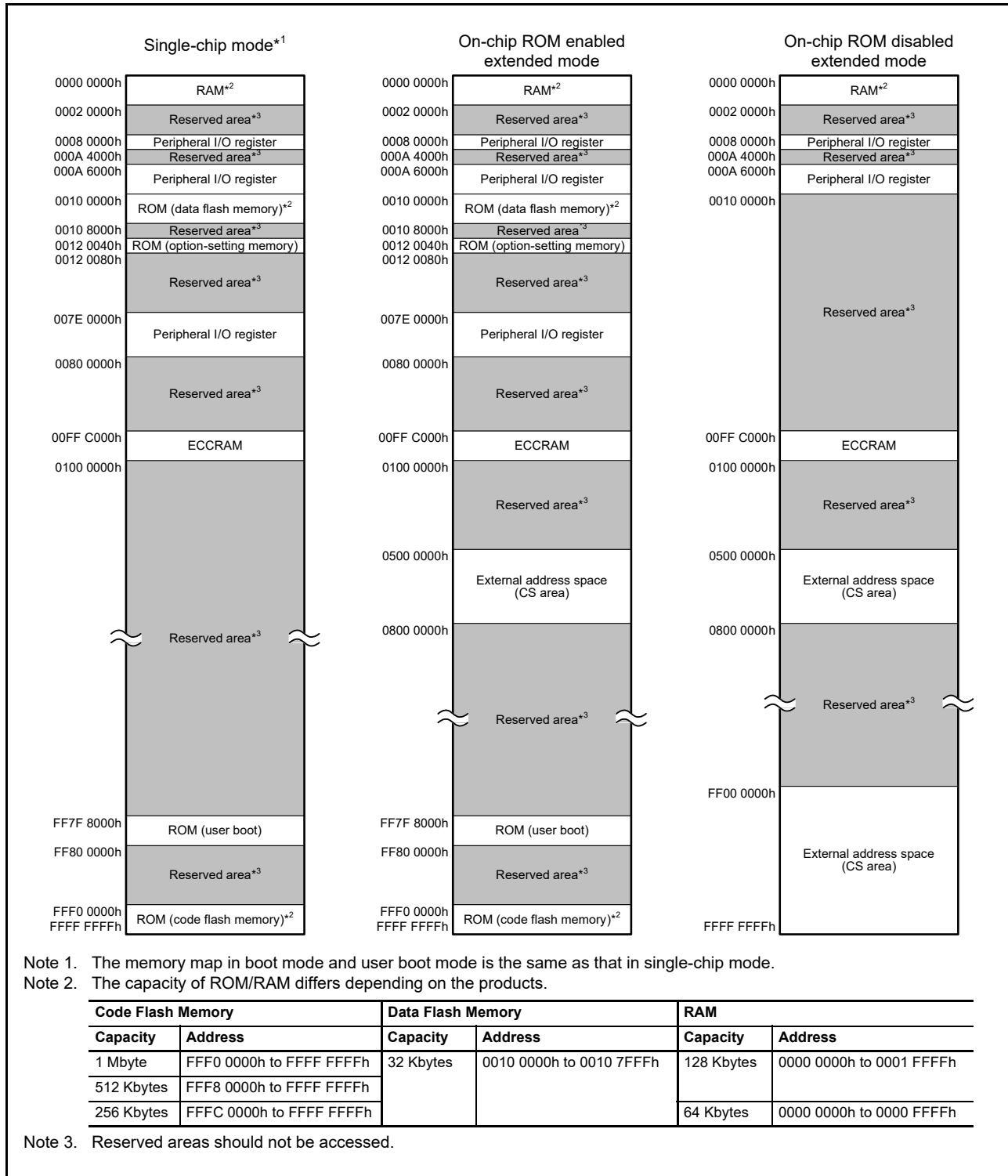


Figure 3.1 Memory Map in Each Operating Mode

3.2 External Address Space

The external address space is divided into four CS areas (CS0 to CS3), each corresponding to the CSn# signal output from a CSn# (n = 0 to 3) pin.

Figure 3.2 shows the address ranges corresponding to the individual CS areas (CS0 to CS3) in on-chip ROM disabled extended mode.

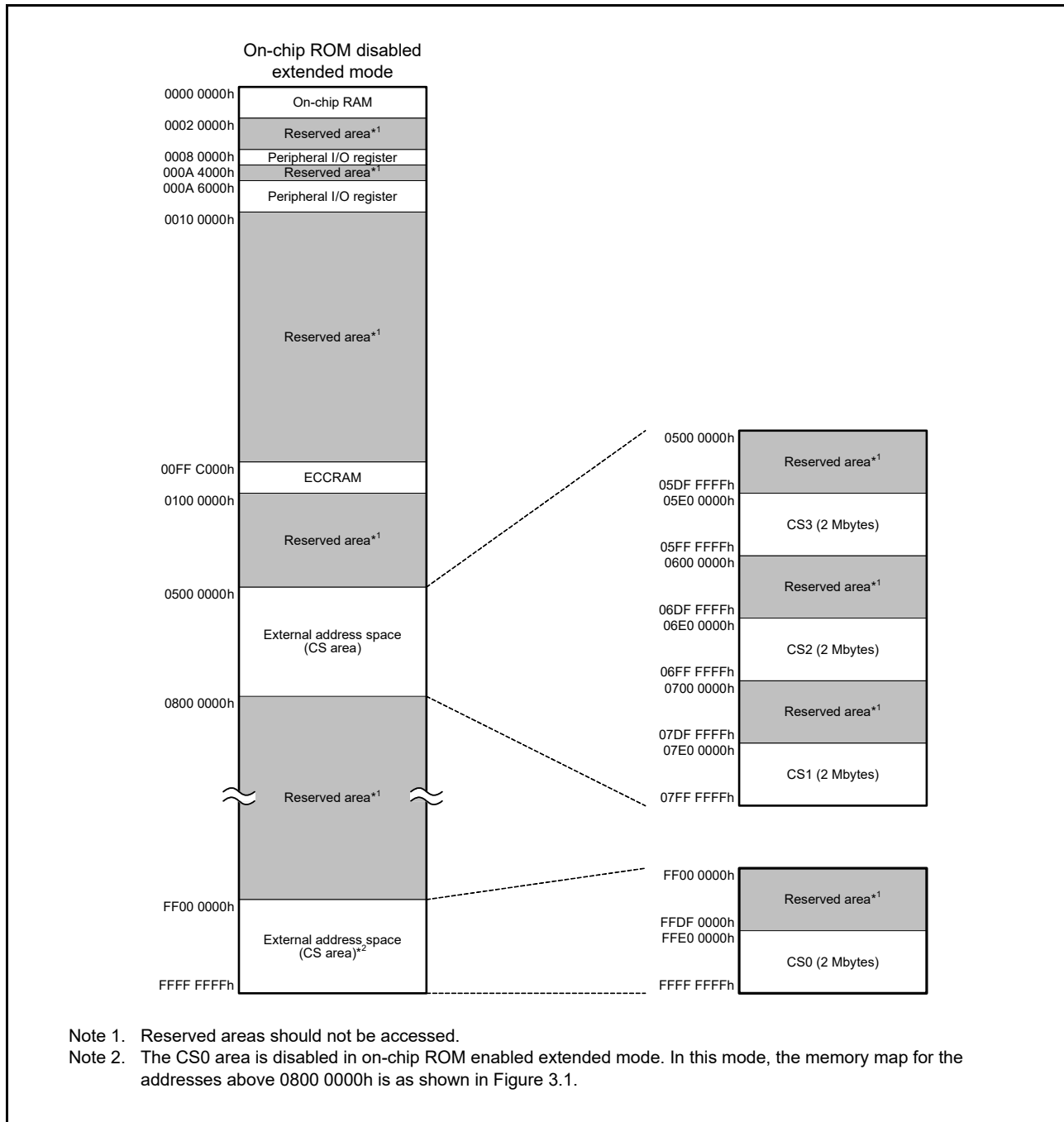


Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode)

4. I/O Registers

This section gives information on the on-chip I/O register addresses. The information is given as shown below. Notes on writing to registers are also given at the end.

(1) I/O register addresses (address order)

- Registers are listed from the lower allocation addresses.
- Registers are classified according to module symbols.
- The number of access cycles indicates the number of cycles based on the specified reference clock.
- Among the internal I/O register area, addresses not listed in the list of registers are reserved. Reserved addresses must not be accessed. Do not access these addresses; otherwise, the operation when accessing these bits and subsequent operations cannot be guaranteed.

(2) Notes on writing to I/O registers

When writing to an I/O register, the CPU starts executing the subsequent instruction before completing I/O register write. This may cause the subsequent instruction to be executed before the post-update I/O register value is reflected on the operation.

As described in the following examples, special care is required for the cases in which the subsequent instruction must be executed after the post-update I/O register value is actually reflected.

[Examples of cases requiring special care]

- The subsequent instruction must be executed while an interrupt request is disabled with the IENj bit in IERN of the ICU (interrupt request enable bit) set to 0.
- A WAIT instruction is executed immediately after the preprocessing for causing a transition to the low power consumption state.

In the above cases, after writing to an I/O register, wait until the write operation is completed using the following procedure and then execute the subsequent instruction.

- Write to an I/O register.
- Read the value from the I/O register to a general register.
- Execute the operation using the value read.
- Execute the subsequent instruction.

[Instruction examples]

- Byte-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.B #SFR_DATA, [R1]
CMP [R1].UB, R1
;; Next process
```

- Word-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.W #SFR_DATA, [R1]
CMP [R1].W, R1
;; Next process
```


- Longword-size I/O registers

```
MOV.L #SFR_ADDR, R1
MOV.L #SFR_DATA, [R1]
CMP [R1].L, R1
;; Next process
```

If multiple registers are written to and a subsequent instruction should be executed after the write operations are entirely completed, only read the I/O register that was last written to and execute the operation using the value; it is not necessary to read or execute operation for all the registers that were written to.

(3) Number of Access Cycles to I/O Registers

For the number of I/O register access cycles, refer to Table 4.1, List of I/O Registers (Address Order).

The number of access cycles to I/O registers is obtained by following equation.*1

Number of access cycles to I/O registers = Number of bus cycles for internal main bus 1 +
 Number of divided clock synchronization cycles +
 Number of bus cycles for internal peripheral busses 1 to 6

The number of bus cycles of internal peripheral bus 1 to 6 differs according to the register to be accessed. When peripheral functions connected to internal peripheral bus 2 to 6 or registers for the external bus control unit (except for bus error related registers) are accessed, the number of divided clock synchronization cycles is added.

The number of divided clock synchronization cycles differs depending on the frequency ratio between ICLK and PCLK (or FCLK, BCLK) or bus access timing.

In the peripheral function unit, when the frequency ratio of ICLK is equal to or greater than that of PCLK (or FCLK), the sum of the number of bus cycles for internal main bus 1 and the number of the divided clock synchronization cycles will be one cycle of PCLK (or FCLK) at a maximum. Therefore, one PCLK (or FCLK) has been added to the number of access states shown in Table 4.1.

When the frequency ratio of ICLK is lower than that of PCLK (or FCLK), the subsequent bus access is started from the ICLK cycle following the completion of the access to the peripheral functions. Therefore, the access cycles are described on an ICLK basis.

In the external bus control unit, the sum of the number of bus cycles for internal main bus 1 and the number of divided clock synchronization cycles will be one cycle of BCLK at a maximum. Therefore, one BCLK is added to the number of access cycles shown in Table 4.1.

Note 1. This applies to the number of cycles when the access from the CPU does not conflict with the instruction fetching to the external memory or bus access from the different bus master (DMAC or DTC).

(4) Notes on Sleep Mode and Mode Transitions

During sleep mode or mode transitions, do not write to the registers related to system control (indicated by 'SYSTEM' in the Module Symbol column in Table 4.1, List of I/O Registers (Address Order)).

(5) Restrictions in Relation to RMPA and String-Manipulation Instructions

The allocation of data to be handled by RMPA or string-manipulation instructions to I/O registers is prohibited, and operation is not guaranteed if this restriction is not observed.

4.1 I/O Register Addresses (Address Order)

Table 4.1 List of I/O Registers (Address Order) (1 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-------------|--------------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 0000h | SYSTEM | Mode Monitor Register | MDMONR | 16 | 16 | 3 ICLK | | Operating Modes |
| 0008 0002h | SYSTEM | Mode Status Register | MDSR | 16 | 16 | 3 ICLK | | Operating Modes |
| 0008 0006h | SYSTEM | System Control Register 0 | SYSCR0 | 16 | 16 | 3 ICLK | | Operating Modes |
| 0008 0008h | SYSTEM | System Control Register 1 | SYSCR1 | 16 | 16 | 3 ICLK | | Operating Modes |
| 0008 000Ch | SYSTEM | Standby Control Register | SBYCR | 16 | 16 | 3 ICLK | | Low Power Consumption |
| 0008 0010h | SYSTEM | Module Stop Control Register A | MSTPCRA | 32 | 32 | 3 ICLK | | Low Power Consumption |
| 0008 0014h | SYSTEM | Module Stop Control Register B | MSTPCRB | 32 | 32 | 3 ICLK | | Low Power Consumption |
| 0008 0018h | SYSTEM | Module Stop Control Register C | MSTPCRC | 32 | 32 | 3 ICLK | | Low Power Consumption |
| 0008 001Ch | SYSTEM | Module Stop Control Register D | MSTPCRD | 32 | 32 | 3 ICLK | | Low Power Consumption |
| 0008 0020h | SYSTEM | System Clock Control Register | SCKCR | 32 | 32 | 3 ICLK | | Clock Generation Circuit |
| 0008 0024h | SYSTEM | System Clock Control Register 2 | SCKCR2 | 16 | 16 | 3 ICLK | | Clock Generation Circuit |
| 0008 0026h | SYSTEM | System Clock Control Register 3 | SCKCR3 | 16 | 16 | 3 ICLK | | Clock Generation Circuit |
| 0008 0028h | SYSTEM | PLL Control Register | PLLCR | 16 | 16 | 3 ICLK | | Clock Generation Circuit |
| 0008 002Ah | SYSTEM | PLL Control Register 2 | PLLCR2 | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0030h | SYSTEM | External Bus Clock Control Register | BCKCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0032h | SYSTEM | Main Clock Oscillator Control Register | MOSCCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0034h | SYSTEM | Low-Speed On-Chip Oscillator Control Register | LOCOCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0035h | SYSTEM | IWDT-Dedicated On-Chip Oscillator Control Register | ILOCOCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0036h | SYSTEM | High-Speed On-Chip Oscillator Control Register | HOCOOCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0037h | SYSTEM | High-Speed On-Chip Oscillator Control Register 2 | HOCOOCR2 | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 003Ch | SYSTEM | Oscillation Stabilization Flag Register | OSCOVFSR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |

Table 4.1 List of I/O Registers (Address Order) (2 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 0040h | SYSTEM | Oscillation Stop Detection Control Register | OSTDCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 0041h | SYSTEM | Oscillation Stop Detection Status Register | OSTDSR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 00A1h | SYSTEM | Sleep Mode Return Clock Source Switching Register | RSTCKCR | 8 | 8 | 3 ICLK | | Low Power Consumption |
| 0008 00A2h | SYSTEM | Main Clock Oscillator Wait Control Register | MOSCWTCR | 8 | 8 | 3 ICLK | | Clock Generation Circuit |
| 0008 00C0h | SYSTEM | Reset Status Register 2 | RSTSR2 | 8 | 8 | 3 ICLK | | Resets |
| 0008 00C2h | SYSTEM | Software Reset Register | SWRR | 16 | 16 | 3 ICLK | | Resets |
| 0008 00E0h | SYSTEM | Voltage Monitoring 1 Circuit Control Register 1 | LVD1CR1 | 8 | 8 | 3 ICLK | | LVDA |
| 0008 00E1h | SYSTEM | Voltage Monitoring 1 Circuit Status Register | LVD1SR | 8 | 8 | 3 ICLK | | LVDA |
| 0008 00E2h | SYSTEM | Voltage Monitoring 2 Circuit Control Register 1 | LVD2CR1 | 8 | 8 | 3 ICLK | | LVDA |
| 0008 00E3h | SYSTEM | Voltage Monitoring 2 Circuit Status Register | LVD2SR | 8 | 8 | 3 ICLK | | LVDA |
| 0008 03FEh | SYSTEM | Protect Register | PRCR | 16 | 16 | 3 ICLK | | Register Write Protection Function |
| 0008 1000h | FLASH | ROM Cache Enable Register | ROMCE | 16 | 16 | 2 ICLK | | Flash |
| 0008 1004h | FLASH | ROM Cache Invalidate Register | ROMCIV | 16 | 16 | 2 ICLK | | Flash |
| 0008 101Ch | SYSTEM | Memory Wait Cycle Setting Register | MEMWAIT | 8 | 8 | 2 ICLK | | Clock Generation Circuit |
| 0008 1040h | FLASH | Non-Cacheable Area 0 Address Register | NCRG0 | 32 | 32 | 2 ICLK | | Flash |
| 0008 1044h | FLASH | Non-Cacheable Area 0 Setting Register | NCRC0 | 32 | 32 | 2 ICLK | | Flash |
| 0008 1048h | FLASH | Non-Cacheable Area 1 Address Register | NCRG1 | 32 | 32 | 2 ICLK | | Flash |
| 0008 104Ch | FLASH | Non-Cacheable Area 1 Setting Register | NCRC1 | 32 | 32 | 2 ICLK | | Flash |
| 0008 1200h | RAM | RAM Operating Mode Control Register | RAMMODE | 8 | 8 | 2 ICLK | | RAM |
| 0008 1201h | RAM | RAM Error Status Register | RAMSTS | 8 | 8 | 2 ICLK | | RAM |
| 0008 1204h | RAM | RAM Protection Register | RAMPRCR | 8 | 8 | 2 ICLK | | RAM |
| 0008 1208h | RAM | RAM Error Address Capture Register | RAMECAD | 32 | 32 | 2 ICLK | | RAM |
| 0008 12C0h | RAM | ECCRAM Operating Mode Control Register | ECCRAMMODE | 8 | 8 | 2 ICLK | | RAM |
| 0008 12C1h | RAM | ECCRAM 2-Bit Error Status Register | ECCRAM2STS | 8 | 8 | 2 ICLK | | RAM |
| 0008 12C2h | RAM | ECCRAM 1-Bit Error Information Update Enable Register | ECCRAM1STSEN | 8 | 8 | 2 ICLK | | RAM |
| 0008 12C3h | RAM | ECCRAM 1-Bit Error Status Register | ECCRAM1STS | 8 | 8 | 2 ICLK | | RAM |
| 0008 12C4h | RAM | ECCRAM Protection Register | ECCRAMPRCR | 8 | 8 | 2 ICLK | | RAM |
| 0008 12C8h | RAM | ECCRAM 2-Bit Error Address Capture Register | ECCRAM2ECAD | 32 | 32 | 2 ICLK | | RAM |
| 0008 12CCh | RAM | ECCRAM 1-Bit Error Address Capture Register | ECCRAM1ECAD | 32 | 32 | 2 ICLK | | RAM |
| 0008 12D0h | RAM | ECCRAM Protection Register 2 | ECCRAMPRCR2 | 8 | 8 | 2 ICLK | | RAM |

Table 4.1 List of I/O Registers (Address Order) (3 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 12D4h | RAM | ECCRAM Test Control Register | ECCRAMETS T | 8 | 8 | 2 | ICLK | RAM |
| 0008 1300h | BSC | Bus Error Status Clear Register | BERCLR | 8 | 8 | 2 | ICLK | Buses |
| 0008 1304h | BSC | Bus Error Monitoring Enable Register | BEREN | 8 | 8 | 2 | ICLK | Buses |
| 0008 1308h | BSC | Bus Error Status Register 1 | BERSR1 | 8 | 8 | 2 | ICLK | Buses |
| 0008 130Ah | BSC | Bus Error Status Register 2 | BERSR2 | 16 | 16 | 2 | ICLK | Buses |
| 0008 1310h | BSC | Bus Priority Control Register | BUSPRI | 16 | 16 | 2 | ICLK | Buses |
| 0008 2000h | DMAC0 | DMA Source Address Register | DMSAR | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 2004h | DMAC0 | DMA Destination Address Register | DMDAR | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 2008h | DMAC0 | DMA Transfer Count Register | DMCRA | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 200Ch | DMAC0 | DMA Block Transfer Count Register | DMCRB | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 2010h | DMAC0 | DMA Transfer Mode Register | DMTMD | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 2013h | DMAC0 | DMA Interrupt Setting Register | DMINT | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 2014h | DMAC0 | DMA Address Mode Register | DMAMD | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 2018h | DMAC0 | DMA Offset Register | DMOFR | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 201Ch | DMAC0 | DMA Transfer Enable Register | DMCNT | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 201Dh | DMAC0 | DMA Software Start Register | DMREQ | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 201Eh | DMAC0 | DMA Status Register | DMSTS | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 201Fh | DMAC0 | DMA Request Source Flag Control Register | DMCSL | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 2040h | DMAC1 | DMA Source Address Register | DMSAR | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 2044h | DMAC1 | DMA Destination Address Register | DMDAR | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 2048h | DMAC1 | DMA Transfer Count Register | DMCRA | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 204Ch | DMAC1 | DMA Block Transfer Count Register | DMCRB | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 2050h | DMAC1 | DMA Transfer Mode Register | DMTMD | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 2053h | DMAC1 | DMA Interrupt Setting Register | DMINT | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 2054h | DMAC1 | DMA Address Mode Register | DMAMD | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 205Ch | DMAC1 | DMA Transfer Enable Register | DMCNT | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 205Dh | DMAC1 | DMA Software Start Register | DMREQ | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 205Eh | DMAC1 | DMA Status Register | DMSTS | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 205Fh | DMAC1 | DMA Request Source Flag Control Register | DMCSL | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 2080h | DMAC2 | DMA Source Address Register | DMSAR | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 2084h | DMAC2 | DMA Destination Address Register | DMDAR | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 2088h | DMAC2 | DMA Transfer Count Register | DMCRA | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 208Ch | DMAC2 | DMA Block Transfer Count Register | DMCRB | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 2090h | DMAC2 | DMA Transfer Mode Register | DMTMD | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 2093h | DMAC2 | DMA Interrupt Setting Register | DMINT | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 2094h | DMAC2 | DMA Address Mode Register | DMAMD | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 209Ch | DMAC2 | DMA Transfer Enable Register | DMCNT | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 209Dh | DMAC2 | DMA Software Start Register | DMREQ | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 209Eh | DMAC2 | DMA Status Register | DMSTS | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 209Fh | DMAC2 | DMA Request Source Flag Control Register | DMCSL | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 20C0h | DMAC3 | DMA Source Address Register | DMSAR | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 20C4h | DMAC3 | DMA Destination Address Register | DMDAR | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 20C8h | DMAC3 | DMA Transfer Count Register | DMCRA | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 20CCh | DMAC3 | DMA Block Transfer Count Register | DMCRB | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 20D0h | DMAC3 | DMA Transfer Mode Register | DMTMD | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 20D3h | DMAC3 | DMA Interrupt Setting Register | DMINT | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 20D4h | DMAC3 | DMA Address Mode Register | DMAMD | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 20DCh | DMAC3 | DMA Transfer Enable Register | DMCNT | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 20DDh | DMAC3 | DMA Software Start Register | DMREQ | 8 | 8 | 2 | ICLK | DMACAa |

Table 4.1 List of I/O Registers (Address Order) (4 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 20DEh | DMAC3 | DMA Status Register | DMSTS | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 20DFh | DMAC3 | DMA Request Source Flag Control Register | DMCSL | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 2100h | DMAC4 | DMA Source Address Register | DMSAR | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 2104h | DMAC4 | DMA Destination Address Register | DMDAR | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 2108h | DMAC4 | DMA Transfer Count Register | DMCRA | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 210Ch | DMAC4 | DMA Block Transfer Count Register | DMCRB | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 2110h | DMAC4 | DMA Transfer Mode Register | DMTMD | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 2113h | DMAC4 | DMA Interrupt Setting Register | DMINT | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 2114h | DMAC4 | DMA Address Mode Register | DMAMD | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 211Ch | DMAC4 | DMA Transfer Enable Register | DMCNT | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 211Dh | DMAC4 | DMA Software Start Register | DMREQ | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 211Eh | DMAC4 | DMA Status Register | DMSTS | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 211Fh | DMAC4 | DMA Request Source Flag Control Register | DMCSL | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 2140h | DMAC5 | DMA Source Address Register | DMSAR | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 2144h | DMAC5 | DMA Destination Address Register | DMDAR | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 2148h | DMAC5 | DMA Transfer Count Register | DMCRA | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 214Ch | DMAC5 | DMA Block Transfer Count Register | DMCRB | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 2150h | DMAC5 | DMA Transfer Mode Register | DMTMD | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 2153h | DMAC5 | DMA Interrupt Setting Register | DMINT | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 2154h | DMAC5 | DMA Address Mode Register | DMAMD | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 215Ch | DMAC5 | DMA Transfer Enable Register | DMCNT | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 215Dh | DMAC5 | DMA Software Start Register | DMREQ | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 215Eh | DMAC5 | DMA Status Register | DMSTS | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 215Fh | DMAC5 | DMA Request Source Flag Control Register | DMCSL | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 2180h | DMAC6 | DMA Source Address Register | DMSAR | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 2184h | DMAC6 | DMA Destination Address Register | DMDAR | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 2188h | DMAC6 | DMA Transfer Count Register | DMCRA | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 218Ch | DMAC6 | DMA Block Transfer Count Register | DMCRB | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 2190h | DMAC6 | DMA Transfer Mode Register | DMTMD | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 2193h | DMAC6 | DMA Interrupt Setting Register | DMINT | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 2194h | DMAC6 | DMA Address Mode Register | DMAMD | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 219Ch | DMAC6 | DMA Transfer Enable Register | DMCNT | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 219Dh | DMAC6 | DMA Software Start Register | DMREQ | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 219Eh | DMAC6 | DMA Status Register | DMSTS | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 219Fh | DMAC6 | DMA Request Source Flag Control Register | DMCSL | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 21C0h | DMAC7 | DMA Source Address Register | DMSAR | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 21C4h | DMAC7 | DMA Destination Address Register | DMDAR | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 21C8h | DMAC7 | DMA Transfer Count Register | DMCRA | 32 | 32 | 2 | ICLK | DMACAa |
| 0008 21CCh | DMAC7 | DMA Block Transfer Count Register | DMCRB | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 21D0h | DMAC7 | DMA Transfer Mode Register | DMTMD | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 21D3h | DMAC7 | DMA Interrupt Setting Register | DMINT | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 21D4h | DMAC7 | DMA Address Mode Register | DMAMD | 16 | 16 | 2 | ICLK | DMACAa |
| 0008 21DCh | DMAC7 | DMA Transfer Enable Register | DMCNT | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 21DDh | DMAC7 | DMA Software Start Register | DMREQ | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 21DEh | DMAC7 | DMA Status Register | DMSTS | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 21DFh | DMAC7 | DMA Request Source Flag Control Register | DMCSL | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 2200h | DMAC | DMAC Module Start Register | DMAST | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 2204h | DMAC | DMAC74 Interrupt Status Monitor Register | DMIST | 8 | 8 | 2 | ICLK | DMACAa |
| 0008 2400h | DTC | DTC Control Register | DTCCR | 8 | 8 | 2 | ICLK | DTCa |
| 0008 2404h | DTC | DTC Vector Base Register | DTCVBR | 32 | 32 | 2 | ICLK | DTCa |

Table 4.1 List of I/O Registers (Address Order) (5 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 2408h | DTC | DTC Address Mode Register | DTCADM0D | 8 | 8 | 2 ICLK | | DTCa |
| 0008 240Ch | DTC | DTC Module Start Register | DTCST | 8 | 8 | 2 ICLK | | DTCa |
| 0008 240Eh | DTC | DTC Status Register | DTCSTS | 16 | 16 | 2 ICLK | | DTCa |
| 0008 3002h | BSC | CS0 Mode Register | CS0MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3004h | BSC | CS0 Wait Control Register 1 | CS0WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3008h | BSC | CS0 Wait Control Register 2 | CS0WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3012h | BSC | CS1 Mode Register | CS1MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3014h | BSC | CS1 Wait Control Register 1 | CS1WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3018h | BSC | CS1 Wait Control Register 2 | CS1WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3022h | BSC | CS2 Mode Register | CS2MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3024h | BSC | CS2 Wait Control Register 1 | CS2WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3028h | BSC | CS2 Wait Control Register 2 | CS2WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3032h | BSC | CS3 Mode Register | CS3MOD | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3034h | BSC | CS3 Wait Control Register 1 | CS3WCR1 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3038h | BSC | CS3 Wait Control Register 2 | CS3WCR2 | 32 | 32 | 1, 2 BCLK | | Buses |
| 0008 3802h | BSC | CS0 Control Register | CS0CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 380Ah | BSC | CS0 Recovery Cycle Register | CS0REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3812h | BSC | CS1 Control Register | CS1CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 381Ah | BSC | CS1 Recovery Cycle Register | CS1REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3822h | BSC | CS2 Control Register | CS2CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 382Ah | BSC | CS2 Recovery Cycle Register | CS2REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3832h | BSC | CS3 Control Register | CS3CR | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 383Ah | BSC | CS3 Recovery Cycle Register | CS3REC | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 3880h | BSC | CS Recovery Cycle Insertion Enable Register | CSRECEN | 16 | 16 | 1, 2 BCLK | | Buses |
| 0008 6400h | MPU | Region-0 Start Page Number Register | RSPAGE0 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6404h | MPU | Region-0 End Page Number Register | REPAGE0 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6408h | MPU | Region-1 Start Page Number Register | RSPAGE1 | 32 | 32 | 1 ICLK | | MPU |
| 0008 640Ch | MPU | Region-1 End Page Number Register | REPAGE1 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6410h | MPU | Region-2 Start Page Number Register | RSPAGE2 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6414h | MPU | Region-2 End Page Number Register | REPAGE2 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6418h | MPU | Region-3 Start Page Number Register | RSPAGE3 | 32 | 32 | 1 ICLK | | MPU |
| 0008 641Ch | MPU | Region-3 End Page Number Register | REPAGE3 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6420h | MPU | Region-4 Start Page Number Register | RSPAGE4 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6424h | MPU | Region-4 End Page Number Register | REPAGE4 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6428h | MPU | Region-5 Start Page Number Register | RSPAGE5 | 32 | 32 | 1 ICLK | | MPU |
| 0008 642Ch | MPU | Region-5 End Page Number Register | REPAGE5 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6430h | MPU | Region-6 Start Page Number Register | RSPAGE6 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6434h | MPU | Region-6 End Page Number Register | REPAGE6 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6438h | MPU | Region-7 Start Page Number Register | RSPAGE7 | 32 | 32 | 1 ICLK | | MPU |
| 0008 643Ch | MPU | Region-7 End Page Number Register | REPAGE7 | 32 | 32 | 1 ICLK | | MPU |
| 0008 6500h | MPU | Memory-Protection Enable Register | MPEN | 32 | 32 | 1 ICLK | | MPU |
| 0008 6504h | MPU | Background Access Control Register | MPBAC | 32 | 32 | 1 ICLK | | MPU |
| 0008 6508h | MPU | Memory-Protection Error Status-Clearing Register | MPECLR | 32 | 32 | 1 ICLK | | MPU |
| 0008 650Ch | MPU | Memory-Protection Error Status Register | MPESTS | 32 | 32 | 1 ICLK | | MPU |
| 0008 6514h | MPU | Data Memory-Protection Error Address Register | MPDEA | 32 | 32 | 1 ICLK | | MPU |
| 0008 6520h | MPU | Region Search Address Register | MPSA | 32 | 32 | 1 ICLK | | MPU |
| 0008 6524h | MPU | Region Search Operation Register | MPOPS | 16 | 16 | 1 ICLK | | MPU |
| 0008 6526h | MPU | Region Invalidation Operation Register | MPOPI | 16 | 16 | 1 ICLK | | MPU |
| 0008 6528h | MPU | Instruction-Hit Region Register | MHITI | 32 | 32 | 1 ICLK | | MPU |
| 0008 652Ch | MPU | Data-Hit Region Register | MHITD | 32 | 32 | 1 ICLK | | MPU |

Table 4.1 List of I/O Registers (Address Order) (6 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|--------------------------|---------------|--|----------------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 7010h to 0008 70FFh | ICU | Interrupt Request Register 016 to Interrupt Request Register 255 | IR016 to IR255 | 8 | 8 | 2 ICLK | | ICUC |
| 0008 711Ah to 0008 71FFh | ICU | DTC Transfer Request Enable Register 026 to DTC Transfer Request Enable Register 255 | DTCER026 to DTCER255 | 8 | 8 | 2 ICLK | | ICUC |
| 0008 7202h to 0008 721Fh | ICU | Interrupt Request Enable Register 02 to Interrupt Request Enable Register 1F | IER02 to IER1F | 8 | 8 | 2 ICLK | | ICUC |
| 0008 72E0h | ICU | Software Interrupt Generation Register | SWINTR | 8 | 8 | 2 ICLK | | ICUC |
| 0008 72E1h | ICU | Software Interrupt 2 Generation Register | SWINT2R | 8 | 8 | 2 ICLK | | ICUC |
| 0008 72F0h | ICU | Fast Interrupt Set Register | FIR | 16 | 16 | 2 ICLK | | ICUC |
| 0008 7300h to 0008 73FFh | ICU | Interrupt Source Priority Register 000 to Interrupt Source Priority Register 255 | IPR000 to IPR255 | 8 | 8 | 2 ICLK | | ICUC |
| 0008 7400h | ICU | DMAC Trigger Select Register 0 | DMRSR0 | 8 | 8 | 2 ICLK | | ICUC |
| 0008 7404h | ICU | DMAC Trigger Select Register 1 | DMRSR1 | 8 | 8 | 2 ICLK | | ICUC |
| 0008 7408h | ICU | DMAC Trigger Select Register 2 | DMRSR2 | 8 | 8 | 2 ICLK | | ICUC |
| 0008 740Ch | ICU | DMAC Trigger Select Register 3 | DMRSR3 | 8 | 8 | 2 ICLK | | ICUC |
| 0008 7410h | ICU | DMAC Trigger Select Register 4 | DMRSR4 | 8 | 8 | 2 ICLK | | ICUC |
| 0008 7414h | ICU | DMAC Trigger Select Register 5 | DMRSR5 | 8 | 8 | 2 ICLK | | ICUC |
| 0008 7418h | ICU | DMAC Trigger Select Register 6 | DMRSR6 | 8 | 8 | 2 ICLK | | ICUC |
| 0008 741Ch | ICU | DMAC Trigger Select Register 7 | DMRSR7 | 8 | 8 | 2 ICLK | | ICUC |
| 0008 7500h to 0008 750Fh | ICU | IRQ Control Register 0 to IRQ Control Register 15 | IRQCR0 to IRQCR15 | 8 | 8 | 2 ICLK | | ICUC |
| 0008 7520h | ICU | IRQ Pin Digital Filter Enable Register 0 | IRQFLTE0 | 8 | 8 | 2 ICLK | | ICUC |
| 0008 7521h | ICU | IRQ Pin Digital Filter Enable Register 1 | IRQFLTE1 | 8 | 8 | 2 ICLK | | ICUC |
| 0008 7528h | ICU | IRQ Pin Digital Filter Setting Register 0 | IRQFLTC0 | 16 | 16 | 2 ICLK | | ICUC |
| 0008 752Ah | ICU | IRQ Pin Digital Filter Setting Register 1 | IRQFLTC1 | 16 | 16 | 2 ICLK | | ICUC |
| 0008 7580h | ICU | Non-Maskable Interrupt Status Register | NMISR | 8 | 8 | 2 ICLK | | ICUC |
| 0008 7581h | ICU | Non-Maskable Interrupt Enable Register | NMIER | 8 | 8 | 2 ICLK | | ICUC |
| 0008 7582h | ICU | Non-Maskable Interrupt Status Clear Register | NMICLR | 8 | 8 | 2 ICLK | | ICUC |
| 0008 7583h | ICU | NMI Pin Interrupt Control Register | NMICR | 8 | 8 | 2 ICLK | | ICUC |
| 0008 7590h | ICU | NMI Pin Digital Filter Enable Register | NMIFLTE | 8 | 8 | 2 ICLK | | ICUC |
| 0008 7594h | ICU | NMI Pin Digital Filter Setting Register | NMIFLTC | 8 | 8 | 2 ICLK | | ICUC |
| 0008 7600h | ICU | Group BE0 Interrupt Request Register | GRPBE0 | 32 | 32 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUC |
| 0008 7630h | ICU | Group BL0 Interrupt Request Register | GRPBL0 | 32 | 32 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUC |
| 0008 7634h | ICU | Group BL1 Interrupt Request Register | GRPBL1 | 32 | 32 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUC |
| 0008 7640h | ICU | Group BE0 Interrupt Request Enable Register | GENBE0 | 32 | 32 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUC |
| 0008 7670h | ICU | Group BL0 Interrupt Request Enable Register | GENBL0 | 32 | 32 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUC |
| 0008 7674h | ICU | Group BL1 Interrupt Request Enable Register | GENBL1 | 32 | 32 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUC |
| 0008 7680h | ICU | Group BE0 Interrupt Clear Register | GCRBE0 | 32 | 32 | 2 ICLK to 1 PCLKB | 2 ICLK | ICUC |
| 0008 7830h | ICU | Group AL0 Interrupt Request Register | GRPAL0 | 32 | 32 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 7870h | ICU | Group AL0 Interrupt Request Enable Register | GENAL0 | 32 | 32 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 7900h | ICU | Software Configurable Interrupt A Request Register 0 | PIAR0 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 7901h | ICU | Software Configurable Interrupt A Request Register 1 | PIAR1 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 7902h | ICU | Software Configurable Interrupt A Request Register 2 | PIAR2 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 7903h | ICU | Software Configurable Interrupt A Request Register 3 | PIAR3 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |

Table 4.1 List of I/O Registers (Address Order) (7 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 7904h | ICU | Software Configurable Interrupt A Request Register 4 | PIAR4 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 7905h | ICU | Software Configurable Interrupt A Request Register 5 | PIAR5 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 7906h | ICU | Software Configurable Interrupt A Request Register 6 | PIAR6 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 7907h | ICU | Software Configurable Interrupt A Request Register 7 | PIAR7 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 7908h | ICU | Software Configurable Interrupt A Request Register 8 | PIAR8 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 7909h | ICU | Software Configurable Interrupt A Request Register 9 | PIAR9 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 790Ah | ICU | Software Configurable Interrupt A Request Register A | PIARA | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 790Bh | ICU | Software Configurable Interrupt A Request Register B | PIARB | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 790Ch | ICU | Software Configurable Interrupt A Request Register C | PIARC | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 790Dh | ICU | Software Configurable Interrupt A Request Register D | PIARD | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 790Eh | ICU | Software Configurable Interrupt A Request Register E | PIARE | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 790Fh | ICU | Software Configurable Interrupt A Request Register F | PIARF | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 7910h | ICU | Software Configurable Interrupt A Request Register 10 | PIAR10 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 7911h | ICU | Software Configurable Interrupt A Request Register 11 | PIAR11 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 7912h | ICU | Software Configurable Interrupt A Request Register 12 | PIAR12 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79D0h | ICU | Software Configurable Interrupt A Source Select Register 208 | SLIAR208 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79D1h | ICU | Software Configurable Interrupt A Source Select Register 209 | SLIAR209 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79D2h | ICU | Software Configurable Interrupt A Source Select Register 210 | SLIAR210 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79D3h | ICU | Software Configurable Interrupt A Source Select Register 211 | SLIAR211 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79D4h | ICU | Software Configurable Interrupt A Source Select Register 212 | SLIAR212 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79D5h | ICU | Software Configurable Interrupt A Source Select Register 213 | SLIAR213 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79D6h | ICU | Software Configurable Interrupt A Source Select Register 214 | SLIAR214 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79D7h | ICU | Software Configurable Interrupt A Source Select Register 215 | SLIAR215 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79D8h | ICU | Software Configurable Interrupt A Source Select Register 216 | SLIAR216 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79D9h | ICU | Software Configurable Interrupt A Source Select Register 217 | SLIAR217 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79DAh | ICU | Software Configurable Interrupt A Source Select Register 218 | SLIAR218 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79DBh | ICU | Software Configurable Interrupt A Source Select Register 219 | SLIAR219 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79DCh | ICU | Software Configurable Interrupt A Source Select Register 220 | SLIAR220 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79DDh | ICU | Software Configurable Interrupt A Source Select Register 221 | SLIAR221 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79DEh | ICU | Software Configurable Interrupt A Source Select Register 222 | SLIAR222 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79DFh | ICU | Software Configurable Interrupt A Source Select Register 223 | SLIAR223 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |

Table 4.1 List of I/O Registers (Address Order) (8 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 79E0h | ICU | Software Configurable Interrupt A Source Select Register 224 | SLIAR224 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79E1h | ICU | Software Configurable Interrupt A Source Select Register 225 | SLIAR225 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79E2h | ICU | Software Configurable Interrupt A Source Select Register 226 | SLIAR226 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79E3h | ICU | Software Configurable Interrupt A Source Select Register 227 | SLIAR227 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79E4h | ICU | Software Configurable Interrupt A Source Select Register 228 | SLIAR228 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79E5h | ICU | Software Configurable Interrupt A Source Select Register 229 | SLIAR229 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79E6h | ICU | Software Configurable Interrupt A Source Select Register 230 | SLIAR230 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79E7h | ICU | Software Configurable Interrupt A Source Select Register 231 | SLIAR231 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79E8h | ICU | Software Configurable Interrupt A Source Select Register 232 | SLIAR232 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79E9h | ICU | Software Configurable Interrupt A Source Select Register 233 | SLIAR233 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79EAh | ICU | Software Configurable Interrupt A Source Select Register 234 | SLIAR234 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79EBh | ICU | Software Configurable Interrupt A Source Select Register 235 | SLIAR235 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79ECh | ICU | Software Configurable Interrupt A Source Select Register 236 | SLIAR236 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79EDh | ICU | Software Configurable Interrupt A Source Select Register 237 | SLIAR237 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79EEh | ICU | Software Configurable Interrupt A Source Select Register 238 | SLIAR238 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79EFh | ICU | Software Configurable Interrupt A Source Select Register 239 | SLIAR239 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79F0h | ICU | Software Configurable Interrupt A Source Select Register 240 | SLIAR240 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79F1h | ICU | Software Configurable Interrupt A Source Select Register 241 | SLIAR241 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79F2h | ICU | Software Configurable Interrupt A Source Select Register 242 | SLIAR242 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79F3h | ICU | Software Configurable Interrupt A Source Select Register 243 | SLIAR243 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79F4h | ICU | Software Configurable Interrupt A Source Select Register 244 | SLIAR244 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79F5h | ICU | Software Configurable Interrupt A Source Select Register 245 | SLIAR245 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79F6h | ICU | Software Configurable Interrupt A Source Select Register 246 | SLIAR246 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79F7h | ICU | Software Configurable Interrupt A Source Select Register 247 | SLIAR247 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79F8h | ICU | Software Configurable Interrupt A Source Select Register 248 | SLIAR248 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79F9h | ICU | Software Configurable Interrupt A Source Select Register 249 | SLIAR249 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79FAh | ICU | Software Configurable Interrupt A Source Select Register 250 | SLIAR250 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79FBh | ICU | Software Configurable Interrupt A Source Select Register 251 | SLIAR251 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79FCh | ICU | Software Configurable Interrupt A Source Select Register 252 | SLIAR252 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79FDh | ICU | Software Configurable Interrupt A Source Select Register 253 | SLIAR253 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 79FEh | ICU | Software Configurable Interrupt A Source Select Register 254 | SLIAR254 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |

Table 4.1 List of I/O Registers (Address Order) (9 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 79FFh | ICU | Software Configurable Interrupt A Source Select Register 255 | SLIAR255 | 8 | 8 | 2 ICLK to 1 PCLKA | 2 ICLK | ICUC |
| 0008 7A00h | ICU | Software Configurable Interrupt Source Select Register Write Protect Register | SLIPRCR | 8 | 8 | 2 ICLK to 1 PCLKA/B | 2 ICLK | ICUC |
| 0008 8000h | CMT | Compare Match Timer Start Register 0 | CMSTR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8002h | CMT0 | Compare Match Timer Control Register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8004h | CMT0 | Compare Match Counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8006h | CMT0 | Compare Match Constant Register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8008h | CMT1 | Compare Match Timer Control Register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 800Ah | CMT1 | Compare Match Counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 800Ch | CMT1 | Compare Match Constant Register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8010h | CMT | Compare Match Timer Start Register 1 | CMSTR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8012h | CMT2 | Compare Match Timer Control Register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8014h | CMT2 | Compare Match Counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8016h | CMT2 | Compare Match Constant Register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8018h | CMT3 | Compare Match Timer Control Register | CMCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 801Ah | CMT3 | Compare Match Counter | CMCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 801Ch | CMT3 | Compare Match Constant Register | CMCOR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CMT |
| 0008 8020h | WDT | WDT Refresh Register | WDTRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | WDTA |
| 0008 8022h | WDT | WDT Control Register | WDTCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | WDTA |
| 0008 8024h | WDT | WDT Status Register | WDTSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | WDTA |
| 0008 8026h | WDT | WDT Reset Control Register | WDTRCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | WDTA |
| 0008 8030h | IWDT | IWDT Refresh Register | IWDTRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | IWDTa |
| 0008 8032h | IWDT | IWDT Control Register | IWDTCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | IWDTa |
| 0008 8034h | IWDT | IWDT Status Register | IWDTSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | IWDTa |
| 0008 8036h | IWDT | IWDT Reset Control Register | IWDTRCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | IWDTa |
| 0008 8038h | IWDT | IWDT Count Stop Control Register | IWDCSTPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | IWDTa |
| 0008 8040h | DA | D/A Data Register 0 | DADR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | R12DAb |
| 0008 8042h | DA | D/A Data Register 1 | DADR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | R12DAb |
| 0008 8044h | DA | D/A Control Register | DACR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | R12DAb |
| 0008 8045h | DA | Data Register Format Select Register | DADPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | R12DAb |
| 0008 8046h | DA | D/A A/D Synchronous Start Control Register | DAADSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | R12DAb |
| 0008 8049h | DA | D/A Destination Select Register | DADSELR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | R12DAb |
| 0008 8200h | TMR0 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8201h | TMR1 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8202h | TMR0 | Timer Control/Status Register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8203h | TMR1 | Timer Control/Status Register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8204h | TMR0 | Time Constant Register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8204h | TMR01 | Time Constant Register A | TCORA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8205h | TMR1 | Time Constant Register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8206h | TMR0 | Time Constant Register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8206h | TMR01 | Time Constant Register B | TCORB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8207h | TMR1 | Time Constant Register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8208h | TMR0 | Timer Counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8208h | TMR01 | Timer Counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8209h | TMR1 | Timer Counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 820Ah | TMR0 | Timer Counter Control Register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 820Ah | TMR01 | Timer Counter Control Register | TCCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 820Bh | TMR1 | Timer Counter Control Register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 820Ch | TMR0 | Timer Counter Start Register | TCSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 820Dh | TMR1 | Timer Counter Start Register | TCSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |

Table 4.1 List of I/O Registers (Address Order) (10 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|--------------------------------|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 8210h | TMR2 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8211h | TMR3 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8212h | TMR2 | Timer Control/Status Register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8213h | TMR3 | Timer Control/Status Register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8214h | TMR2 | Time Constant Register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8214h | TMR23 | Time Constant Register A | TCORA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8215h | TMR3 | Time Constant Register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8216h | TMR2 | Time Constant Register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8216h | TMR23 | Time Constant Register B | TCORB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8217h | TMR3 | Time Constant Register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8218h | TMR2 | Timer Counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8218h | TMR23 | Timer Counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8219h | TMR3 | Timer Counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 821Ah | TMR2 | Timer Counter Control Register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 821Ah | TMR23 | Timer Counter Control Register | TCCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 821Bh | TMR3 | Timer Counter Control Register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 821Ch | TMR2 | Timer Counter Start Register | TCSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 821Dh | TMR3 | Timer Counter Start Register | TCSTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8220h | TMR4 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8221h | TMR5 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8222h | TMR4 | Timer Control/Status Register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8223h | TMR5 | Timer Control/Status Register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8224h | TMR4 | Time Constant Register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8224h | TMR45 | Time Constant Register A | TCORA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8225h | TMR5 | Time Constant Register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8226h | TMR4 | Time Constant Register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8226h | TMR45 | Time Constant Register B | TCORB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8227h | TMR5 | Time Constant Register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8228h | TMR4 | Timer Counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8228h | TMR45 | Timer Counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8229h | TMR5 | Timer Counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 822Ah | TMR4 | Timer Counter Control Register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 822Ah | TMR45 | Timer Counter Control Register | TCCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 822Bh | TMR5 | Timer Counter Control Register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8230h | TMR6 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8231h | TMR7 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8232h | TMR6 | Timer Control/Status Register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8233h | TMR7 | Timer Control/Status Register | TCSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8234h | TMR6 | Time Constant Register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8234h | TMR67 | Time Constant Register A | TCORA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8235h | TMR7 | Time Constant Register A | TCORA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8236h | TMR6 | Time Constant Register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8236h | TMR67 | Time Constant Register B | TCORB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8237h | TMR7 | Time Constant Register B | TCORB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8238h | TMR6 | Timer Counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8238h | TMR67 | Timer Counter | TCNT | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 8239h | TMR7 | Timer Counter | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 823Ah | TMR6 | Timer Counter Control Register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 823Ah | TMR67 | Timer Counter Control Register | TCCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | TMR |
| 0008 823Bh | TMR7 | Timer Counter Control Register | TCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | TMR |

Table 4.1 List of I/O Registers (Address Order) (11 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 8280h | CRC | CRC Control Register | CRCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CRCA |
| 0008 8284h | CRC | CRC Data Input Register | CRCDIR | 32 | 8, 32 | 2, 3 PCLKB | 2 ICLK | CRCA |
| 0008 8288h | CRC | CRC Data Output Register | CRCDOR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CRCA |
| 0008 8300h | RIIC0 | I ² C-bus Control Register 1 | ICCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8301h | RIIC0 | I ² C-bus Control Register 2 | ICCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8302h | RIIC0 | I ² C-bus Mode Register 1 | ICMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8303h | RIIC0 | I ² C-bus Mode Register 2 | ICMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8304h | RIIC0 | I ² C-bus Mode Register 3 | ICMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8305h | RIIC0 | I ² C-bus Function Enable Register | ICFER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8306h | RIIC0 | I ² C-bus Status Enable Register | ICSER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8307h | RIIC0 | I ² C-bus Interrupt Enable Register | ICIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8308h | RIIC0 | I ² C-bus Status Register 1 | ICSR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8309h | RIIC0 | I ² C-bus Status Register 2 | ICSR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 830Ah | RIIC0 | Slave Address Register L0 | SARL0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 830Bh | RIIC0 | Slave Address Register U0 | SARU0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 830Ch | RIIC0 | Slave Address Register L1 | SARL1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 830Dh | RIIC0 | Slave Address Register U1 | SARU1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 830Eh | RIIC0 | Slave Address Register L2 | SARL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 830Fh | RIIC0 | Slave Address Register U2 | SARU2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8310h | RIIC0 | I ² C-bus Bit Rate Low-Level Register | ICBRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8311h | RIIC0 | I ² C-bus Bit Rate High-Level Register | ICBRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8312h | RIIC0 | I ² C-bus Transmit Data Register | ICDRT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 8313h | RIIC0 | I ² C-bus Receive Data Register | ICDRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | RIICa |
| 0008 9000h | S12AD | A/D Control Register | ADCSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9004h | S12AD | A/D Channel Select Register A0 | ADANSA0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9008h | S12AD | A/D-Converted Value Addition/Average Function Channel Select Register 0 | ADADS0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 900Ch | S12AD | A/D-Converted Value Addition/Average Count Select Register | ADADC | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 900Eh | S12AD | A/D Control Extended Register | ADCER | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9010h | S12AD | A/D Conversion Start Trigger Select Register | ADSTRGR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9014h | S12AD | A/D Channel Select Register B0 | ADANSB0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9018h | S12AD | A/D Data Duplication Register | ADDBLDR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 901Eh | S12AD | A/D Self-Diagnosis Data Register | ADRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9020h | S12AD | A/D Data Register 0 | ADDR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9022h | S12AD | A/D Data Register 1 | ADDR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9024h | S12AD | A/D Data Register 2 | ADDR2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9026h | S12AD | A/D Data Register 3 | ADDR3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9028h | S12AD | A/D Data Register 4 | ADDR4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 902Ah | S12AD | A/D Data Register 5 | ADDR5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 902Ch | S12AD | A/D Data Register 6 | ADDR6 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 902Eh | S12AD | A/D Data Register 7 | ADDR7 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9066h | S12AD | A/D Sample-and-Hold Circuit Control Register | ADSHCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 907Ah | S12AD | A/D Disconnection Detection Control Register | ADDISCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 907Ch | S12AD | A/D Sample-and-Hold Operating Mode Select Register | ADSHMSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 907Dh | S12AD | A/D Event Link Control Register | ADELCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9080h | S12AD | A/D Group Scan Priority Control Register | ADGSPCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9084h | S12AD | A/D Data Duplication Register A | ADDBLDR A | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9086h | S12AD | A/D Data Duplication Register B | ADDBLDR B | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 908Ch | S12AD | A/D Comparison Function Window A/B Status Monitoring Register | ADWINMON | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |

Table 4.1 List of I/O Registers (Address Order) (12 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 9090h | S12AD | A/D Compare Control Register | ADCMPCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9094h | S12AD | A/D Comparison Function Window A Channel Select Register 0 | ADCMPSNR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9098h | S12AD | A/D Comparison Function Window A Comparison Condition Setting Register 0 | ADCMPLR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 909Ch | S12AD | A/D Comparison Function Window A Lower Level Setting Register | ADCMPLR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 909Eh | S12AD | A/D Comparison Function Window A Upper Level Setting Register | ADCMPLR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 90A0h | S12AD | A/D Comparison Function Window A Channel Status Register 0 | ADCMPSR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 90A6h | S12AD | A/D Comparison Function Window B Channel Select Register | ADCMPSNR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 90A8h | S12AD | A/D Comparison Function Window B Lower Level Setting Register | ADWINLLB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 90AAh | S12AD | A/D Comparison Function Window B Upper Level Setting Register | ADWINULB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 90ACh | S12AD | A/D Comparison Function Window B Channel Status Register | ADCMPSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 90D4h | S12AD | A/D Channel Select Register C0 | ADANSC0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 90D9h | S12AD | A/D Group C Trigger Select Register | ADGCTRGR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 90E0h | S12AD | A/D Sampling State Register 0 | ADSSTR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 90E1h | S12AD | A/D Sampling State Register 1 | ADSSTR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 90E2h | S12AD | A/D Sampling State Register 2 | ADSSTR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 90E3h | S12AD | A/D Sampling State Register 3 | ADSSTR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 90E4h | S12AD | A/D Sampling State Register 4 | ADSSTR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 90E5h | S12AD | A/D Sampling State Register 5 | ADSSTR5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 90E6h | S12AD | A/D Sampling State Register 6 | ADSSTR6 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 90E7h | S12AD | A/D Sampling State Register 7 | ADSSTR7 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 91A0h | S12AD | A/D Programmable Gain Amplifier Control Register | ADPGACR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 91A2h | S12AD | A/D Programmable Gain Amplifier Gain Setting Register 0 | ADPGAGS0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 91B0h | S12AD | A/D Programmable Gain Amplifier Differential Input Control Register | ADPGADCR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 91C0h | S12AD | A/D Channel Conversion Order Setting Register 0 | ADSCS0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 91C1h | S12AD | A/D Channel Conversion Order Setting Register 1 | ADSCS1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 91C2h | S12AD | A/D Channel Conversion Order Setting Register 2 | ADSCS2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 91C3h | S12AD | A/D Channel Conversion Order Setting Register 3 | ADSCS3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 91C4h | S12AD | A/D Channel Conversion Order Setting Register 4 | ADSCS4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 91C5h | S12AD | A/D Channel Conversion Order Setting Register 5 | ADSCS5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 91C6h | S12AD | A/D Channel Conversion Order Setting Register 6 | ADSCS6 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 91C7h | S12AD | A/D Channel Conversion Order Setting Register 7 | ADSCS7 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9200h | S12AD1 | A/D Control Register | ADCSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9204h | S12AD1 | A/D Channel Select Register A0 | ADANSA0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9208h | S12AD1 | A/D-Converted Value Addition/Average Function Channel Select Register 0 | ADADS0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 920Ch | S12AD1 | A/D-Converted Value Addition/Average Count Select Register | ADADC | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 920Eh | S12AD1 | A/D Control Extended Register | ADCER | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9210h | S12AD1 | A/D Conversion Start Trigger Select Register | ADSTRGR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9214h | S12AD1 | A/D Channel Select Register B0 | ADANSB0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9218h | S12AD1 | A/D Data Duplication Register | ADDBLDR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 921Eh | S12AD1 | A/D Self-Diagnosis Data Register | ADRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9220h | S12AD1 | A/D Data Register 0 | ADDR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9222h | S12AD1 | A/D Data Register 1 | ADDR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |

Table 4.1 List of I/O Registers (Address Order) (13 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 9224h | S12AD1 | A/D Data Register 2 | ADDR2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9226h | S12AD1 | A/D Data Register 3 | ADDR3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9228h | S12AD1 | A/D Data Register 4 | ADDR4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 922Ah | S12AD1 | A/D Data Register 5 | ADDR5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 922Ch | S12AD1 | A/D Data Register 6 | ADDR6 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 922Eh | S12AD1 | A/D Data Register 7 | ADDR7 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9266h | S12AD1 | A/D Sample-and-Hold Circuit Control Register | ADSHCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 927Ah | S12AD1 | A/D Disconnection Detection Control Register | ADDISCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 927Ch | S12AD1 | A/D Sample-and-Hold Operating Mode Select Register | ADSHMSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 927Dh | S12AD1 | A/D Event Link Control Register | ADELCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9280h | S12AD1 | A/D Group Scan Priority Control Register | ADGSPCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9284h | S12AD1 | A/D Data Duplication Register A | ADDBLDRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9286h | S12AD1 | A/D Data Duplication Register B | ADDBLDRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 928Ch | S12AD1 | A/D Comparison Function Window A/B Status Monitoring Register | ADWINMON | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9290h | S12AD1 | A/D Comparison Function Control Register | ADCMPPCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9294h | S12AD1 | A/D Comparison Function Window A Channel Select Register 0 | ADCMPANSR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9298h | S12AD1 | A/D Comparison Function Window A Comparison Condition Setting Register 0 | ADCMPLR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 929Ch | S12AD1 | A/D Comparison Function Window A Lower Level Setting Register | ADCMPDR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 929Eh | S12AD1 | A/D Comparison Function Window A Upper Level Setting Register | ADCMPDR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 92A0h | S12AD1 | A/D Comparison Function Window A Channel Status Register 0 | ADCMPSR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 92A6h | S12AD1 | A/D Comparison Function Window B Channel Select Register | ADCMPBNSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 92A8h | S12AD1 | A/D Comparison Function Window B Lower Level Setting Register | ADWINLLB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 92AAh | S12AD1 | A/D Comparison Function Window B Upper Level Setting Register | ADWINULB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 92ACh | S12AD1 | A/D Comparison Function Window B Channel Status Register | ADCMPBSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 92D4h | S12AD1 | A/D Channel Select Register C0 | ADANSC0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 92D9h | S12AD1 | A/D Group C Trigger Select Register | ADGCTRGR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 92E0h | S12AD1 | A/D Sampling State Register 0 | ADSSTR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 92E1h | S12AD1 | A/D Sampling State Register 1 | ADSSTR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 92E2h | S12AD1 | A/D Sampling State Register 2 | ADSSTR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 92E3h | S12AD1 | A/D Sampling State Register 3 | ADSSTR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 92E4h | S12AD1 | A/D Sampling State Register 4 | ADSSTR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 92E5h | S12AD1 | A/D Sampling State Register 5 | ADSSTR5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 92E6h | S12AD1 | A/D Sampling State Register 6 | ADSSTR6 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 92E7h | S12AD1 | A/D Sampling State Register 7 | ADSSTR7 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 93A0h | S12AD1 | A/D Programmable Gain Amplifier Control Register | ADPGACR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 93A2h | S12AD1 | A/D Programmable Gain Amplifier Gain Setting Register 0 | ADPGAGS0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 93B0h | S12AD1 | A/D Programmable Gain Amplifier Differential Input Control Register | ADPGADCR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 93C0h | S12AD1 | A/D Channel Conversion Order Setting Register 0 | ADSCS0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 93C1h | S12AD1 | A/D Channel Conversion Order Setting Register 1 | ADSCS1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 93C2h | S12AD1 | A/D Channel Conversion Order Setting Register 2 | ADSCS2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 93C3h | S12AD1 | A/D Channel Conversion Order Setting Register 3 | ADSCS3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 93C4h | S12AD1 | A/D Channel Conversion Order Setting Register 4 | ADSCS4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 93C5h | S12AD1 | A/D Channel Conversion Order Setting Register 5 | ADSCS5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |

Table 4.1 List of I/O Registers (Address Order) (14 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 93C6h | S12AD1 | A/D Channel Conversion Order Setting Register 6 | ADSCS6 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 93C7h | S12AD1 | A/D Channel Conversion Order Setting Register 7 | ADSCS7 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9400h | S12AD2 | A/D Control Register | ADCSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9404h | S12AD2 | A/D Channel Select Register A0 | ADANSA0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9406h | S12AD2 | A/D Channel Select Register A1 | ADANSA1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9408h | S12AD2 | A/D-Converted Value Addition/Average Function Channel Select Register 0 | ADADS0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 940Ah | S12AD2 | A/D-Converted Value Addition/Average Function Channel Select Register 1 | ADADS1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 940Ch | S12AD2 | A/D-Converted Value Addition/Average Count Select Register | ADADC | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 940Eh | S12AD2 | A/D Control Extended Register | ADCER | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9410h | S12AD2 | A/D Conversion Start Trigger Select Register | ADSTRGR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9412h | S12AD2 | A/D Conversion Extended Input Control Register | ADEXICR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9414h | S12AD2 | A/D Channel Select Register B0 | ADANSB0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9416h | S12AD2 | A/D Channel Select Register B1 | ADANSB1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9418h | S12AD2 | A/D Data Duplication Register | ADDBLDR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 941Ah | S12AD2 | A/D Temperature Sensor Data Register | ADTSDR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 941Ch | S12AD2 | A/D Internal Reference Voltage Data Register | ADOCDR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 941Eh | S12AD2 | A/D Self-Diagnosis Data Register | ADRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9420h | S12AD2 | A/D Data Register 0 | ADDR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9422h | S12AD2 | A/D Data Register 1 | ADDR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9424h | S12AD2 | A/D Data Register 2 | ADDR2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9426h | S12AD2 | A/D Data Register 3 | ADDR3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9428h | S12AD2 | A/D Data Register 4 | ADDR4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 942Ah | S12AD2 | A/D Data Register 5 | ADDR5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 942Ch | S12AD2 | A/D Data Register 6 | ADDR6 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 942Eh | S12AD2 | A/D Data Register 7 | ADDR7 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9430h | S12AD2 | A/D Data Register 8 | ADDR8 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9432h | S12AD2 | A/D Data Register 9 | ADDR9 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9434h | S12AD2 | A/D Data Register 10 | ADDR10 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9436h | S12AD2 | A/D Data Register 11 | ADDR11 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9440h | S12AD2 | A/D Data Register 16 | ADDR16 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9442h | S12AD2 | A/D Data Register 17 | ADDR17 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 947Ah | S12AD2 | A/D Disconnection Detection Control Register | ADDISCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 947Dh | S12AD2 | A/D Event Link Control Register | ADELCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9480h | S12AD2 | A/D Group Scan Priority Control Register | ADGSPCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9484h | S12AD2 | A/D Data Duplication Register A | ADDBLDRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9486h | S12AD2 | A/D Data Duplication Register B | ADDBLDRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 948Ch | S12AD2 | A/D Comparison Function Window A/B Status Monitoring Register | ADWINMON | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9490h | S12AD2 | A/D Comparison Function Control Register | ADCMPCR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9492h | S12AD2 | A/D Comparison Function Window A Extended Input Select Register | ADCMPANSE R | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9493h | S12AD2 | A/D Comparison Function Window A Extended Input Comparison Condition Setting Register | ADCMPLER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9494h | S12AD2 | A/D Comparison Function Window A Channel Select Register 0 | ADCMPANSR 0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9496h | S12AD2 | A/D Comparison Function Window A Channel Select Register 1 | ADCMPANSR 1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 9498h | S12AD2 | A/D Comparison Function Window A Comparison Condition Setting Register 0 | ADCMPLR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 949Ah | S12AD2 | A/D Comparison Function Window A Comparison Condition Setting Register 1 | ADCMPLR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |

Table 4.1 List of I/O Registers (Address Order) (15 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 949Ch | S12AD2 | A/D Comparison Function Window A Lower Level Setting Register | ADCMPPDR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 949Eh | S12AD2 | A/D Comparison Function Window A Upper Level Setting Register | ADCMPPDR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94A0h | S12AD2 | A/D Comparison Function Window A Channel Status Register 0 | ADCMPSR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94A2h | S12AD2 | A/D Comparison Function Window A Channel Status Register 1 | ADCMPSR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94A4h | S12AD2 | A/D Comparison Function Window A Extended Input Channel Status Register | ADCMPSER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94A6h | S12AD2 | A/D Comparison Function Window B Channel Select Register | ADCMPSNR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94A8h | S12AD2 | A/D Comparison Function Window B Lower Level Setting Register | ADWINLLB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94AAh | S12AD2 | A/D Comparison Function Window B Upper Level Setting Register | ADWINULB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94ACh | S12AD2 | A/D Comparison Function Window B Channel Status Register | ADCMPSBR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94D4h | S12AD2 | A/D Channel Select Register C0 | ADANSC0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94D6h | S12AD2 | A/D Channel Select Register C1 | ADANSC1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94D8h | S12AD2 | A/D Group C Extended Input Control Register | ADGCXCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94D9h | S12AD2 | A/D Group C Trigger Select Register | ADGCTRGR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94DDh | S12AD2 | A/D Sampling State Register L | ADSSTRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94DEh | S12AD2 | A/D Sampling State Register T | ADSSTRT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94DFh | S12AD2 | A/D Sampling State Register O | ADSSTRO | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94E0h | S12AD2 | A/D Sampling State Register 0 | ADSSTR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94E1h | S12AD2 | A/D Sampling State Register 1 | ADSSTR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94E2h | S12AD2 | A/D Sampling State Register 2 | ADSSTR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94E3h | S12AD2 | A/D Sampling State Register 3 | ADSSTR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94E4h | S12AD2 | A/D Sampling State Register 4 | ADSSTR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94E5h | S12AD2 | A/D Sampling State Register 5 | ADSSTR5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94E6h | S12AD2 | A/D Sampling State Register 6 | ADSSTR6 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94E7h | S12AD2 | A/D Sampling State Register 7 | ADSSTR7 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94E8h | S12AD2 | A/D Sampling State Register 8 | ADSSTR8 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94E9h | S12AD2 | A/D Sampling State Register 9 | ADSSTR9 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94EAh | S12AD2 | A/D Sampling State Register 10 | ADSSTR10 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 94EBh | S12AD2 | A/D Sampling State Register 11 | ADSSTR11 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 95C0h | S12AD2 | A/D Channel Conversion Order Setting Register 0 | ADSCS0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 95C1h | S12AD2 | A/D Channel Conversion Order Setting Register 1 | ADSCS1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 95C2h | S12AD2 | A/D Channel Conversion Order Setting Register 2 | ADSCS2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 95C3h | S12AD2 | A/D Channel Conversion Order Setting Register 3 | ADSCS3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 95C4h | S12AD2 | A/D Channel Conversion Order Setting Register 4 | ADSCS4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 95C5h | S12AD2 | A/D Channel Conversion Order Setting Register 5 | ADSCS5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 95C6h | S12AD2 | A/D Channel Conversion Order Setting Register 6 | ADSCS6 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 95C7h | S12AD2 | A/D Channel Conversion Order Setting Register 7 | ADSCS7 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 95C8h | S12AD2 | A/D Channel Conversion Order Setting Register 8 | ADSCS8 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 95C9h | S12AD2 | A/D Channel Conversion Order Setting Register 9 | ADSCS9 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 95CAh | S12AD2 | A/D Channel Conversion Order Setting Register 10 | ADSCS10 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 95CBh | S12AD2 | A/D Channel Conversion Order Setting Register 11 | ADSCS11 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 95D0h | S12AD2 | A/D Channel Conversion Order Setting Register 12 | ADSCS12 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 95D1h | S12AD2 | A/D Channel Conversion Order Setting Register 13 | ADSCS13 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 95E2h | S12AD2 | A/D Internal Reference Voltage Monitoring Circuit Enable Register | ADVMONCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |

Table 4.1 List of I/O Registers (Address Order) (16 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 95E4h | S12AD2 | A/D Internal Reference Voltage Monitoring Circuit Output Enable Register | ADVMONO | 8 | 8 | 2, 3 PCLKB | 2 ICLK | S12ADH |
| 0008 A020h | SC11 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A020h | SMC11 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A021h | SC11 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A022h | SC11 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A022h | SMC11 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A023h | SC11 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A024h | SC11 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A024h | SMC11 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A025h | SC11 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A026h | SMC11 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A027h | SC11 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A028h | SC11 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A029h | SC11 | I ² C Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A02Ah | SC11 | I ² C Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A02Bh | SC11 | I ² C Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A02Ch | SC11 | I ² C Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A02Dh | SC11 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A02Eh | SC11 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A02Fh | SC11 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A02Eh | SC11 | Transmit Data Register HL | TDRHL | 16 | 8, 16 | 2 to 5 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A030h | SC11 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A031h | SC11 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A030h | SC11 | Receive Data Register HL | RDRHL | 16 | 8, 16 | 2 to 5 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A032h | SC11 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A033h | SC11 | Data Comparison Control Register | DCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A03Ah | SC11 | Comparison Data Register H | CDR.H | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A03Bh | SC11 | Comparison Data Register L | CDR.L | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A03Ah | SC11 | Comparison Data Register | CDR | 16 | 8, 16 | 2 to 5 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A03Ch | SC11 | Serial Port Register | SPTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |
| 0008 A0A0h | SC15 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SC1j, SC1i, SC1h |

Table 4.1 List of I/O Registers (Address Order) (17 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|----------------------------------|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 A0A0h | SMCI5 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0A1h | SCI5 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0A2h | SCI5 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0A2h | SMCI5 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0A3h | SCI5 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0A4h | SCI5 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0A4h | SMCI5 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0A5h | SCI5 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0A6h | SMCI5 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0A7h | SCI5 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0A8h | SCI5 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0A9h | SCI5 | I ² C Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0AAh | SCI5 | I ² C Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0ABh | SCI5 | I ² C Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0ACh | SCI5 | I ² C Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0ADh | SCI5 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0AEh | SCI5 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0AFh | SCI5 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0AEh | SCI5 | Transmit Data Register HL | TDRHL | 16 | 8, 16 | 2 to 5 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0B0h | SCI5 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0B1h | SCI5 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0B0h | SCI5 | Receive Data Register HL | RDRHL | 16 | 8, 16 | 2 to 5 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0B2h | SCI5 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0B3h | SCI5 | Data Comparison Control Register | DCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0BAh | SCI5 | Comparison Data Register H | CDR.H | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0BBh | SCI5 | Comparison Data Register L | CDR.L | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0BAh | SCI5 | Comparison Data Register | CDR | 16 | 8, 16 | 2 to 5 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0BCh | SCI5 | Serial Port Register | SPTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0C0h | SCI6 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0C0h | SMCI6 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A0C1h | SCI6 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |

Table 4.1 List of I/O Registers (Address Order) (18 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|----------------------------------|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 A0C2h | SCI6 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0C2h | SMCI6 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0C3h | SCI6 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0C4h | SCI6 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0C4h | SMCI6 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0C5h | SCI6 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0C6h | SMCI6 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0C7h | SCI6 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0C8h | SCI6 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0C9h | SCI6 | I ² C Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0CAh | SCI6 | I ² C Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0CBh | SCI6 | I ² C Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0CCh | SCI6 | I ² C Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0CDh | SCI6 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0CEh | SCI6 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0CFh | SCI6 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0CEh | SCI6 | Transmit Data Register HL | TDRHL | 16 | 8, 16 | 2 to 5 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0D0h | SCI6 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0D1h | SCI6 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0D0h | SCI6 | Receive Data Register HL | RDRHL | 16 | 8, 16 | 2 to 5 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0D2h | SCI6 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0D3h | SCI6 | Data Comparison Control Register | DCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0DAh | SCI6 | Comparison Data Register H | CDR.H | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0DBh | SCI6 | Comparison Data Register L | CDR.L | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0DAh | SCI6 | Comparison Data Register | CDR | 16 | 8, 16 | 2 to 5 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A0DCh | SCI6 | Serial Port Register | SPTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A100h | SCI8 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A100h | SMCI8 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A101h | SCI8 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A102h | SCI8 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 A102h | SMCI8 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |

Table 4.1 List of I/O Registers (Address Order) (19 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|----------------------------------|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 A103h | SCI8 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A104h | SCI8 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A104h | SMCI8 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A105h | SCI8 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A106h | SMCI8 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A107h | SCI8 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A108h | SCI8 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A109h | SCI8 | I2C Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A10Ah | SCI8 | I2C Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A10Bh | SCI8 | I2C Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A10Ch | SCI8 | I2C Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A10Dh | SCI8 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A10Eh | SCI8 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A10Fh | SCI8 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A10Eh | SCI8 | Transmit Data Register HL | TDRHL | 16 | 8, 16 | 2 to 5 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A110h | SCI8 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A111h | SCI8 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A110h | SCI8 | Receive Data Register HL | RDRHL | 16 | 8, 16 | 2 to 5 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A112h | SCI8 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A113h | SCI8 | Data Comparison Control Register | DCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A11Ah | SCI8 | Comparison Data Register H | CDR.H | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A11Bh | SCI8 | Comparison Data Register L | CDR.L | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A11Ah | SCI8 | Comparison Data Register | CDR | 16 | 8, 16 | 2 to 5 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A11Ch | SCI8 | Serial Port Register | SPTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A120h | SCI9 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A120h | SMCI9 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A121h | SCI9 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A122h | SCI9 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A122h | SMCI9 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A123h | SCI9 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |
| 0008 A124h | SCI9 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SC1h |

Table 4.1 List of I/O Registers (Address Order) (20 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 A124h | SMCI9 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A125h | SCI9 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A126h | SMCI9 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A127h | SCI9 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A128h | SCI9 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A129h | SCI9 | I2C Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A12Ah | SCI9 | I2C Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A12Bh | SCI9 | I2C Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A12Ch | SCI9 | I2C Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A12Dh | SCI9 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A12Eh | SCI9 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A12Fh | SCI9 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A12Eh | SCI9 | Transmit Data Register HL | TDRHL | 16 | 8, 16 | 2 to 5 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A130h | SCI9 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A131h | SCI9 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A130h | SCI9 | Receive Data Register HL | RDRHL | 16 | 8, 16 | 2 to 5 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A132h | SCI9 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A133h | SCI9 | Data Comparison Control Register | DCCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A13Ah | SCI9 | Comparison Data Register H | CDR.H | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A13Bh | SCI9 | Comparison Data Register L | CDR.L | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A13Ah | SCI9 | Comparison Data Register | CDR | 16 | 8, 16 | 2 to 5 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 A13Ch | SCI9 | Serial Port Register | SPTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCiJ, SCiI, SCiH |
| 0008 B000h | CAC | CAC Control Register 0 | CACR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAC |
| 0008 B001h | CAC | CAC Control Register 1 | CACR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAC |
| 0008 B002h | CAC | CAC Control Register 2 | CACR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAC |
| 0008 B003h | CAC | CAC Interrupt Request Enable Register | CAICR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAC |
| 0008 B004h | CAC | CAC Status Register | CASTR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAC |
| 0008 B006h | CAC | CAC Upper-Limit Value Setting Register | CAULVR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CAC |
| 0008 B008h | CAC | CAC Lower-Limit Value Setting Register | CALLVR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CAC |
| 0008 B00Ah | CAC | CAC Counter Buffer Register | CACNTBR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CAC |
| 0008 B080h | DOC | DOC Control Register | DOCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | DOC |
| 0008 B082h | DOC | DOC Data Input Register | DODIR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | DOC |
| 0008 B084h | DOC | DOC Data Setting Register | DODSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | DOC |
| 0008 B100h | ELC | Event Link Control Register | ELCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B101h | ELC | Event Link Setting Register 0 | ELSR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B104h | ELC | Event Link Setting Register 3 | ELSR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B105h | ELC | Event Link Setting Register 4 | ELSR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |

Table 4.1 List of I/O Registers (Address Order) (21 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 B108h | ELC | Event Link Setting Register 7 | ELSR7 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B10Bh | ELC | Event Link Setting Register 10 | ELSR10 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B10Ch | ELC | Event Link Setting Register 11 | ELSR11 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B10Dh | ELC | Event Link Setting Register 12 | ELSR12 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B10Eh | ELC | Event Link Setting Register 13 | ELSR13 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B110h | ELC | Event Link Setting Register 15 | ELSR15 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B111h | ELC | Event Link Setting Register 16 | ELSR16 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B113h | ELC | Event Link Setting Register 18 | ELSR18 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B114h | ELC | Event Link Setting Register 19 | ELSR19 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B115h | ELC | Event Link Setting Register 20 | ELSR20 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B116h | ELC | Event Link Setting Register 21 | ELSR21 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B117h | ELC | Event Link Setting Register 22 | ELSR22 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B118h | ELC | Event Link Setting Register 23 | ELSR23 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B119h | ELC | Event Link Setting Register 24 | ELSR24 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B11Ah | ELC | Event Link Setting Register 25 | ELSR25 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B11Bh | ELC | Event Link Setting Register 26 | ELSR26 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B11Ch | ELC | Event Link Setting Register 27 | ELSR27 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B11Dh | ELC | Event Link Setting Register 28 | ELSR28 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B11Fh | ELC | Event Link Option Setting Register A | ELOPA | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B120h | ELC | Event Link Option Setting Register B | ELOPB | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B121h | ELC | Event Link Option Setting Register C | ELOPC | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B122h | ELC | Event Link Option Setting Register D | ELOPD | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B123h | ELC | Port Group Setting Register 1 | PGR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B124h | ELC | Port Group Setting Register 2 | PGR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B125h | ELC | Port Group Control Register 1 | PGC1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B126h | ELC | Port Group Control Register 2 | PGC2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B127h | ELC | Port Buffer Register 1 | PDBF1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B128h | ELC | Port Buffer Register 2 | PDBF2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B129h | ELC | Event Link Port Setting Register 0 | PEL0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B12Ah | ELC | Event Link Port Setting Register 1 | PEL1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B12Bh | ELC | Event Link Port Setting Register 2 | PEL2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B12Ch | ELC | Event Link Port Setting Register 3 | PEL3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B12Dh | ELC | Event Link Software Event Generation Register | ELSEGR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B12Eh | ELC | Event Link Setting Register 30 | ELSR30 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B12Fh | ELC | Event Link Setting Register 31 | ELSR31 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B13Dh | ELC | Event Link Setting Register 45 | ELSR45 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B13Eh | ELC | Event Link Option Setting Register E | ELOPE | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B144h | ELC | Event Link Setting Register 46 | ELSR46 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B145h | ELC | Event Link Setting Register 47 | ELSR47 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B146h | ELC | Event Link Setting Register 48 | ELSR48 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B147h | ELC | Event Link Setting Register 49 | ELSR49 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B148h | ELC | Event Link Setting Register 50 | ELSR50 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B149h | ELC | Event Link Setting Register 51 | ELSR51 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B14Ah | ELC | Event Link Setting Register 52 | ELSR52 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B14Bh | ELC | Event Link Setting Register 53 | ELSR53 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B14Ch | ELC | Event Link Setting Register 54 | ELSR54 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B14Dh | ELC | Event Link Setting Register 55 | ELSR55 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B14Eh | ELC | Event Link Setting Register 56 | ELSR56 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B14Fh | ELC | Event Link Setting Register 57 | ELSR57 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |
| 0008 B150h | ELC | Event Link Setting Register 58 | ELSR58 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | ELC |

Table 4.1 List of I/O Registers (Address Order) (22 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 B300h | SCI12 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B300h | SMCI12 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B301h | SCI12 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B302h | SCI12 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B302h | SMCI12 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B303h | SCI12 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B304h | SCI12 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B304h | SMCI12 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B305h | SCI12 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B306h | SMCI12 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B307h | SCI12 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B308h | SCI12 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B309h | SCI12 | I ² C Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B30Ah | SCI12 | I ² C Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B30Bh | SCI12 | I ² C Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B30Ch | SCI12 | I ² C Status Register | SISR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B30Dh | SCI12 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B30Eh | SCI12 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B30Fh | SCI12 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B30Eh | SCI12 | Transmit Data Register HL | TDRHL | 16 | 8, 16 | 2 to 5 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B310h | SCI12 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B311h | SCI12 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B310h | SCI12 | Receive Data Register HL | RDRHL | 16 | 8, 16 | 2 to 5 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B312h | SCI12 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B320h | SCI12 | Extended Serial Module Enable Register | ESMER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B321h | SCI12 | Control Register 0 | CR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B322h | SCI12 | Control Register 1 | CR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B323h | SCI12 | Control Register 2 | CR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B324h | SCI12 | Control Register 3 | CR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B325h | SCI12 | Port Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B326h | SCI12 | Interrupt Control Register | ICR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |

Table 4.1 List of I/O Registers (Address Order) (23 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 B327h | SCI12 | Status Register | STR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B328h | SCI12 | Status Clear Register | STCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B329h | SCI12 | Control Field 0 Data Register | CF0DR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B32Ah | SCI12 | Control Field 0 Compare Enable Register | CF0CR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B32Bh | SCI12 | Control Field 0 Receive Data Register | CF0RR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B32Ch | SCI12 | Primary Control Field 1 Data Register | PCF1DR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B32Dh | SCI12 | Secondary Control Field 1 Data Register | SCF1DR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B32Eh | SCI12 | Control Field 1 Compare Enable Register | CF1CR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B32Fh | SCI12 | Control Field 1 Receive Data Register | CF1RR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B330h | SCI12 | Timer Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B331h | SCI12 | Timer Mode Register | TMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B332h | SCI12 | Timer Prescaler Register | TPRE | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 B333h | SCI12 | Timer Count Register | TCNT | 8 | 8 | 2, 3 PCLKB | 2 ICLK | SCIj, SCli, SClh |
| 0008 C000h | PORT0 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C001h | PORT1 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C002h | PORT2 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C003h | PORT3 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C004h | PORT4 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C005h | PORT5 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C006h | PORT6 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C007h | PORT7 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C008h | PORT8 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C009h | PORT9 | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C00Ah | PORTA | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C00Bh | PORTB | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C00Ch | PORTC | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C00Dh | PORTD | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C00Eh | PORTE | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C00Fh | PORTF | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C010h | PORTG | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C011h | PORTH | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C013h | PORTK | Port Direction Register | PDR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C020h | PORT0 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C021h | PORT1 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C022h | PORT2 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C023h | PORT3 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C024h | PORT4 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C025h | PORT5 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C026h | PORT6 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C027h | PORT7 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C028h | PORT8 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C029h | PORT9 | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |

Table 4.1 List of I/O Registers (Address Order) (24 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|-------------------------------|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C02Ah | PORTA | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C02Bh | PORTB | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C02Ch | PORTC | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C02Dh | PORTD | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C02Eh | PORTE | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C02Fh | PORTF | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C030h | PORTG | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C031h | PORTH | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C033h | PORTK | Port Output Data Register | PODR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C040h | PORT0 | Port Input Register | PIDR | 8 | 8 | 4, 5 PCLKB | 3 ICLK | I/O Ports |
| 0008 C041h | PORT1 | Port Input Register | PIDR | 8 | 8 | 4, 5 PCLKB | 3 ICLK | I/O Ports |
| 0008 C042h | PORT2 | Port Input Register | PIDR | 8 | 8 | 4, 5 PCLKB | 3 ICLK | I/O Ports |
| 0008 C043h | PORT3 | Port Input Register | PIDR | 8 | 8 | 4, 5 PCLKB | 3 ICLK | I/O Ports |
| 0008 C044h | PORT4 | Port Input Register | PIDR | 8 | 8 | 4, 5 PCLKB | 3 ICLK | I/O Ports |
| 0008 C045h | PORT5 | Port Input Register | PIDR | 8 | 8 | 4, 5 PCLKB | 3 ICLK | I/O Ports |
| 0008 C046h | PORT6 | Port Input Register | PIDR | 8 | 8 | 4, 5 PCLKB | 3 ICLK | I/O Ports |
| 0008 C047h | PORT7 | Port Input Register | PIDR | 8 | 8 | 4, 5 PCLKB | 3 ICLK | I/O Ports |
| 0008 C048h | PORT8 | Port Input Register | PIDR | 8 | 8 | 4, 5 PCLKB | 3 ICLK | I/O Ports |
| 0008 C049h | PORT9 | Port Input Register | PIDR | 8 | 8 | 4, 5 PCLKB | 3 ICLK | I/O Ports |
| 0008 C04Ah | PORTA | Port Input Register | PIDR | 8 | 8 | 4, 5 PCLKB | 3 ICLK | I/O Ports |
| 0008 C04Bh | PORTB | Port Input Register | PIDR | 8 | 8 | 4, 5 PCLKB | 3 ICLK | I/O Ports |
| 0008 C04Ch | PORTC | Port Input Register | PIDR | 8 | 8 | 4, 5 PCLKB | 3 ICLK | I/O Ports |
| 0008 C04Dh | PORTD | Port Input Register | PIDR | 8 | 8 | 4, 5 PCLKB | 3 ICLK | I/O Ports |
| 0008 C04Eh | PORTE | Port Input Register | PIDR | 8 | 8 | 4, 5 PCLKB | 3 ICLK | I/O Ports |
| 0008 C04Fh | PORTF | Port Input Register | PIDR | 8 | 8 | 4, 5 PCLKB | 3 ICLK | I/O Ports |
| 0008 C050h | PORTG | Port Input Register | PIDR | 8 | 8 | 4, 5 PCLKB | 3 ICLK | I/O Ports |
| 0008 C051h | PORTH | Port Input Register | PIDR | 8 | 8 | 4, 5 PCLKB | 3 ICLK | I/O Ports |
| 0008 C053h | PORTK | Port Input Register | PIDR | 8 | 8 | 4, 5 PCLKB | 3 ICLK | I/O Ports |
| 0008 C060h | PORT0 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C061h | PORT1 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C062h | PORT2 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C063h | PORT3 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C064h | PORT4 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C065h | PORT5 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C066h | PORT6 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C067h | PORT7 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C068h | PORT8 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C069h | PORT9 | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Ah | PORTA | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Bh | PORTB | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Ch | PORTC | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Dh | PORTD | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Eh | PORTE | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C06Fh | PORTF | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C070h | PORTG | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C071h | PORTH | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C073h | PORTK | Port Mode Register | PMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C080h | PORT0 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C082h | PORT1 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C083h | PORT1 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |

Table 4.1 List of I/O Registers (Address Order) (25 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|-----------------------------------|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C084h | PORT2 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C085h | PORT2 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C086h | PORT3 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C087h | PORT3 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C088h | PORT4 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C089h | PORT4 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Ah | PORT5 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Bh | PORT5 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Ch | PORT6 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Dh | PORT6 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Eh | PORT7 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C08Fh | PORT7 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C090h | PORT8 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C092h | PORT9 | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C093h | PORT9 | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C094h | PORTA | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C095h | PORTA | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C096h | PORTB | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C097h | PORTB | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C098h | PORTC | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C099h | PORTC | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C09Ah | PORTD | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C09Bh | PORTD | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C09Ch | PORTE | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C09Dh | PORTE | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C09Eh | PORTF | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0A0h | PORTG | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0A2h | PORTH | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0A3h | PORTH | Open-Drain Control Register 1 | ODR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0A6h | PORTK | Open-Drain Control Register 0 | ODR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C0h | PORT0 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C1h | PORT1 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C2h | PORT2 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C3h | PORT3 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C4h | PORT4 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C5h | PORT5 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C6h | PORT6 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C7h | PORT7 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C8h | PORT8 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0C9h | PORT9 | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0CAh | PORTA | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0CBh | PORTB | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0CCh | PORTC | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0CDh | PORTD | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0CEh | PORTE | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0CFh | PORTF | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0D0h | PORTG | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0D1h | PORTH | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0D3h | PORTK | Pull-Up Resistor Control Register | PCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0E0h | PORT0 | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |

Table 4.1 List of I/O Registers (Address Order) (26 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|-----------------------------------|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C0E1h | PORT1 | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0E2h | PORT2 | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0E3h | PORT3 | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0E7h | PORT7 | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0E8h | PORT8 | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0E9h | PORT9 | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0EAh | PORTA | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0EBh | PORTB | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0ECh | PORTC | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0EDh | PORTD | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0EEh | PORTE | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0EFh | PORTF | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0F0h | PORTG | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C0F3h | PORTK | Drive Capacity Control Register | DSCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C100h | MPC | CS Output Enable Register | PFCSE | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C102h | MPC | CS Output Pin Select Register 0 | PFCSS0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C104h | MPC | Address Output Enable Register 0 | PFAOE0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C105h | MPC | Address Output Enable Register 1 | PFAOE1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C106h | MPC | External Bus Control Register 0 | PFBCR0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C107h | MPC | External Bus Control Register 1 | PFBCR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C108h | MPC | External Bus Control Register 2 | PFBCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C109h | MPC | External Bus Control Register 3 | PFBCR3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C10Ah | MPC | External Bus Control Register 4 | PFBCR4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C11Fh | MPC | Write-Protect Register | PWPR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C12Fh | PORT7 | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C130h | PORT8 | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C131h | PORT9 | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C133h | PORTB | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C135h | PORTD | Drive Capacity Control Register 2 | DSCR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | I/O Ports |
| 0008 C140h | MPC | P00 Pin Function Control Register | P00PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C141h | MPC | P01 Pin Function Control Register | P01PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C148h | MPC | P10 Pin Function Control Register | P10PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C149h | MPC | P11 Pin Function Control Register | P11PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Ah | MPC | P12 Pin Function Control Register | P12PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Bh | MPC | P13 Pin Function Control Register | P13PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Ch | MPC | P14 Pin Function Control Register | P14PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Dh | MPC | P15 Pin Function Control Register | P15PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Eh | MPC | P16 Pin Function Control Register | P16PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C14Fh | MPC | P17 Pin Function Control Register | P17PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C150h | MPC | P20 Pin Function Control Register | P20PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C151h | MPC | P21 Pin Function Control Register | P21PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C152h | MPC | P22 Pin Function Control Register | P22PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C153h | MPC | P23 Pin Function Control Register | P23PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C154h | MPC | P24 Pin Function Control Register | P24PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C155h | MPC | P25 Pin Function Control Register | P25PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C156h | MPC | P26 Pin Function Control Register | P26PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C157h | MPC | P27 Pin Function Control Register | P27PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C158h | MPC | P30 Pin Function Control Register | P30PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C159h | MPC | P31 Pin Function Control Register | P31PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C15Ah | MPC | P32 Pin Function Control Register | P32PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |

Table 4.1 List of I/O Registers (Address Order) (27 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|-----------------------------------|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C15Bh | MPC | P33 Pin Function Control Register | P33PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C15Ch | MPC | P34 Pin Function Control Register | P34PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C15Dh | MPC | P35 Pin Function Control Register | P35PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C160h | MPC | P40 Pin Function Control Register | P40PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C161h | MPC | P41 Pin Function Control Register | P41PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C162h | MPC | P42 Pin Function Control Register | P42PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C163h | MPC | P43 Pin Function Control Register | P43PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C164h | MPC | P44 Pin Function Control Register | P44PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C165h | MPC | P45 Pin Function Control Register | P45PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C166h | MPC | P46 Pin Function Control Register | P46PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C167h | MPC | P47 Pin Function Control Register | P47PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C168h | MPC | P50 Pin Function Control Register | P50PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C169h | MPC | P51 Pin Function Control Register | P51PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C16Ah | MPC | P52 Pin Function Control Register | P52PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C16Bh | MPC | P53 Pin Function Control Register | P53PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C16Ch | MPC | P54 Pin Function Control Register | P54PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C16Dh | MPC | P55 Pin Function Control Register | P55PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C170h | MPC | P60 Pin Function Control Register | P60PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C171h | MPC | P61 Pin Function Control Register | P61PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C172h | MPC | P62 Pin Function Control Register | P62PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C173h | MPC | P61 Pin Function Control Register | P63PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C174h | MPC | P61 Pin Function Control Register | P64PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C175h | MPC | P61 Pin Function Control Register | P65PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C178h | MPC | P70 Pin Function Control Register | P70PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C179h | MPC | P71 Pin Function Control Register | P71PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C17Ah | MPC | P72 Pin Function Control Register | P72PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C17Bh | MPC | P73 Pin Function Control Register | P73PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C17Ch | MPC | P74 Pin Function Control Register | P74PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C17Dh | MPC | P75 Pin Function Control Register | P75PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C17Eh | MPC | P76 Pin Function Control Register | P76PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C180h | MPC | P80 Pin Function Control Register | P80PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C181h | MPC | P81 Pin Function Control Register | P81PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C182h | MPC | P82 Pin Function Control Register | P82PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C188h | MPC | P90 Pin Function Control Register | P90PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C189h | MPC | P91 Pin Function Control Register | P91PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C18Ah | MPC | P92 Pin Function Control Register | P92PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C18Bh | MPC | P93 Pin Function Control Register | P93PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C18Ch | MPC | P94 Pin Function Control Register | P94PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C18Dh | MPC | P95 Pin Function Control Register | P95PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C18Eh | MPC | P96 Pin Function Control Register | P96PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C190h | MPC | PA0 Pin Function Control Register | PA0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C191h | MPC | PA1 Pin Function Control Register | PA1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C192h | MPC | PA2 Pin Function Control Register | PA2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C193h | MPC | PA3 Pin Function Control Register | PA3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C194h | MPC | PA4 Pin Function Control Register | PA4PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C195h | MPC | PA5 Pin Function Control Register | PA5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C196h | MPC | PA6 Pin Function Control Register | PA6PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C197h | MPC | PA7 Pin Function Control Register | PA7PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C198h | MPC | PB0 Pin Function Control Register | PB0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C199h | MPC | PB1 Pin Function Control Register | PB1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |

Table 4.1 List of I/O Registers (Address Order) (28 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|-----------------------------------|-----------------|----------------|-------------|-------------------------|-------------|-----------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C19Ah | MPC | PB2 Pin Function Control Register | PB2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C19Bh | MPC | PB3 Pin Function Control Register | PB3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C19Ch | MPC | PB4 Pin Function Control Register | PB4PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C19Dh | MPC | PB5 Pin Function Control Register | PB5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C19Eh | MPC | PB6 Pin Function Control Register | PB6PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C19Fh | MPC | PB7 Pin Function Control Register | PB7PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1A0h | MPC | PC0 Pin Function Control Register | PC0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1A1h | MPC | PC1 Pin Function Control Register | PC1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1A2h | MPC | PC2 Pin Function Control Register | PC2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1A3h | MPC | PC3 Pin Function Control Register | PC3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1A4h | MPC | PC4 Pin Function Control Register | PC4PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1A5h | MPC | PC5 Pin Function Control Register | PC5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1A6h | MPC | PC6 Pin Function Control Register | PC6PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1A8h | MPC | PD0 Pin Function Control Register | PD0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1A9h | MPC | PD1 Pin Function Control Register | PD1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1AAh | MPC | PD2 Pin Function Control Register | PD2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1ABh | MPC | PD3 Pin Function Control Register | PD3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1ACh | MPC | PD4 Pin Function Control Register | PD4PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1ADh | MPC | PD5 Pin Function Control Register | PD5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1AEh | MPC | PD6 Pin Function Control Register | PD6PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1AFh | MPC | PD7 Pin Function Control Register | PD7PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B0h | MPC | PE0 Pin Function Control Register | PE0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B1h | MPC | PE1 Pin Function Control Register | PE1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B2h | MPC | PE2 Pin Function Control Register | PE2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B3h | MPC | PE3 Pin Function Control Register | PE3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B4h | MPC | PE4 Pin Function Control Register | PE4PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B5h | MPC | PE5 Pin Function Control Register | PE5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B6h | MPC | PE6 Pin Function Control Register | PE6PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B8h | MPC | PF0 Pin Function Control Register | PF0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1B9h | MPC | PF1 Pin Function Control Register | PF1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1BAh | MPC | PF2 Pin Function Control Register | PF2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1BBh | MPC | PF3 Pin Function Control Register | PF3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1C0h | MPC | PG0 Pin Function Control Register | PG0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1C1h | MPC | PG1 Pin Function Control Register | PG1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1C2h | MPC | PG2 Pin Function Control Register | PG2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1C8h | MPC | PH0 Pin Function Control Register | PH0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1C9h | MPC | PH1 Pin Function Control Register | PH1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1CAh | MPC | PH2 Pin Function Control Register | PH2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1CBh | MPC | PH3 Pin Function Control Register | PH3PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1CCh | MPC | PH4 Pin Function Control Register | PH4PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1CDh | MPC | PH5 Pin Function Control Register | PH5PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1CEh | MPC | PH6 Pin Function Control Register | PH6PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1CFh | MPC | PH7 Pin Function Control Register | PH7PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1D8h | MPC | PK0 Pin Function Control Register | PK0PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1D9h | MPC | PK1 Pin Function Control Register | PK1PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C1DAh | MPC | PK2 Pin Function Control Register | PK2PFS | 8 | 8 | 2, 3 PCLKB | 2 ICLK | MPC |
| 0008 C280h | SYSTEM | Deep Standby Control Register | DPSBYCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |

Table 4.1 List of I/O Registers (Address Order) (29 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|--------------------------|---------------|---|---------------------|----------------|-------------|-------------------------|-------------|--------------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0008 C282h | SYSTEM | Deep Standby Interrupt Enable Register 0 | DPSIER0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C283h | SYSTEM | Deep Standby Interrupt Enable Register 1 | DPSIER1 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C284h | SYSTEM | Deep Standby Interrupt Enable Register 2 | DPSIER2 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C286h | SYSTEM | Deep Standby Interrupt Flag Register 0 | DPSIFR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C287h | SYSTEM | Deep Standby Interrupt Flag Register 1 | DPSIFR1 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C288h | SYSTEM | Deep Standby Interrupt Flag Register 2 | DPSIFR2 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C28Ah | SYSTEM | Deep Standby Interrupt Edge Register 0 | DPSIEGR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C28Bh | SYSTEM | Deep Standby Interrupt Edge Register 1 | DPSIEGR1 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C28Ch | SYSTEM | Deep Standby Interrupt Edge Register 2 | DPSIEGR2 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0008 C290h | SYSTEM | Reset Status Register 0 | RSTSR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Resets |
| 0008 C291h | SYSTEM | Reset Status Register 1 | RSTSR1 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Resets |
| 0008 C293h | SYSTEM | Main Clock Oscillator Function Control Register | MOFCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Clock Generation Circuit |
| 0008 C294h | SYSTEM | High-Speed On-Chip Oscillator Power Supply Control Register | HOCOPCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Clock Generation Circuit |
| 0008 C295h | SYSTEM | Voltage Level Setting Register | VOLSR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Operating Modes |
| 0008 C296h | FLASH | Flash P/E Protect Register | FWEPROR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Flash |
| 0008 C297h | SYSTEM | Voltage Monitoring Circuit Control Register | LVCMPCR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | LVDA |
| 0008 C298h | SYSTEM | Voltage Detection Level Select Register | LVDLVLR | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | LVDA |
| 0008 C29Ah | SYSTEM | Voltage Monitoring 1 Circuit Control Register 0 | LVD1CR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | LVDA |
| 0008 C29Bh | SYSTEM | Voltage Monitoring 2 Circuit Control Register 0 | LVD2CR0 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | LVDA |
| 0008 C2A0h to 0008 C2BFh | SYSTEM | Deep Standby Backup Register 0 to Deep Standby Backup Register 31 | DPSBKR0 to DPSBKR31 | 8 | 8 | 4, 5 PCLKB | 2, 3 ICLK | Low Power Consumption |
| 0009 0200h to 0009 03FFh | CAN0 | Mailbox Register 0 to Mailbox Register 31 | MB0 to MB31 | 128 | 8, 16, 32*2 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0400h to 0009 041Fh | CAN0 | Mask Register 0 to Mask Register 7 | MKR0 to MKR7 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0420h | CAN0 | FIFO Received ID Compare Register 0 | FIDCR0 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0424h | CAN0 | FIFO Received ID Compare Register 1 | FIDCR1 | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0428h | CAN0 | Mask Invalid Register | MKIVLR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |

Table 4.1 List of I/O Registers (Address Order) (30 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|--------------------------|---------------|--|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0009 042Ch | CAN0 | Mailbox Interrupt Enable Register | MIER | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0820h to 0009 083Fh | CAN0 | Message Control Register 0 to Message Control Register 31 | MCTL0 to MCTL31 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0840h | CAN0 | Control Register | CTLR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0842h | CAN0 | Status Register | STR | 16 | 8, 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0844h | CAN0 | Bit Configuration Register | BCR | 32 | 8, 16, 32 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0848h | CAN0 | Receive FIFO Control Register | RFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0849h | CAN0 | Receive FIFO Pointer Control Register | RFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 084Ah | CAN0 | Transmit FIFO Control Register | TFCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 084Bh | CAN0 | Transmit FIFO Pointer Control Register | TFPCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 084Ch | CAN0 | Error Interrupt Enable Register | EIER | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 084Dh | CAN0 | Error Interrupt Factor Judge Register | EIFR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 084Eh | CAN0 | Receive Error Count Register | RECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 084Fh | CAN0 | Transmit Error Count Register | TECR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0850h | CAN0 | Error Code Store Register | ECSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0851h | CAN0 | Channel Search Support Register | CSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0852h | CAN0 | Mailbox Search Status Register | MSSR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0853h | CAN0 | Mailbox Search Mode Register | MSMR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0854h | CAN0 | Time Stamp Register | TSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0856h | CAN0 | Acceptance Filter Support Register | AFSR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 0858h | CAN0 | Test Control Register | TCR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | CAN |
| 0009 E000h | POEG | POEG Group A Setting Register | POEGGA | 32 | 32 | 2, 3 PCLKB | 2 ICLK | POEG |
| 0009 E040h | POEG | GPTW Output Negate Control Group A writing Protection Register | GTONCWPA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POEG |
| 0009 E044h | POEG | GPTW Output Negate Control Group A Controlling Register | GTONCCRA | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POEG |
| 0009 E100h | POEG | POEG Group B Setting Register | POEGGB | 32 | 32 | 2, 3 PCLKB | 2 ICLK | POEG |
| 0009 E140h | POEG | GPTW Output Negate Control Group B writing Protection Register | GTONCWPB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POEG |
| 0009 E144h | POEG | GPTW Output Negate Control Group B Controlling Register | GTONCCRB | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POEG |
| 0009 E200h | POEG | POEG Group C Setting Register | POEGGC | 32 | 32 | 2, 3 PCLKB | 2 ICLK | POEG |
| 0009 E240h | POEG | GPTW Output Negate Control Group C writing Protection Register | GTONCWPC | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POEG |
| 0009 E244h | POEG | GPTW Output Negate Control Group C Controlling Register | GTONCCRC | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POEG |
| 0009 E300h | POEG | POEG Group D Setting Register | POEGGD | 32 | 32 | 2, 3 PCLKB | 2 ICLK | POEG |
| 0009 E340h | POEG | GPTW Output Negate Control Group D writing Protection Register | GTONCWPD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POEG |
| 0009 E344h | POEG | GPTW Output Negate Control Group D Controlling Register | GTONCCRD | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POEG |
| 0009 E400h | POE | Input Level Control/Status Register 1 | ICSR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E402h | POE | Output Level Control/Status Register 1 | OCSR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E404h | POE | Input Level Control/Status Register 2 | ICSR2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E406h | POE | Output Level Control/Status Register 2 | OCSR2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E408h | POE | Input Level Control/Status Register 3 | ICSR3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E40Bh | POE | Port Output Enable Control Register 1 | POECR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E40Ch | POE | Port Output Enable Control Register 2 | POECR2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E40Eh | POE | Port Output Enable Control Register 3 | POECR3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E410h | POE | Port Output Enable Control Register 4 | POECR4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E412h | POE | Port Output Enable Control Register 5 | POECR5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E414h | POE | Port Output Enable Control Register 6 | POECR6 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E416h | POE | Input Level Control/Status Register 4 | ICSR4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E418h | POE | Input Level Control/Status Register 5 | ICSR5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |

Table 4.1 List of I/O Registers (Address Order) (31 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0009 E41Ah | POE | Active Level Setting Register 1 | ALR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E41Ch | POE | Input Level Control/Status Register 6 | ICSR6 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E41Eh | POE | Active Level Setting Register 2 | ALR2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E420h | POE | Input Level Control/Status Register 7 | ICSR7 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E422h | POE | Port Output Enable Control Register 7 | POECR7 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E424h | POE | Port Output Enable Control Register 8 | POECR8 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E426h | POE | Port Output Enable Comparator Detection Flag Register | POECMPFR | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E428h | POE | Port Output Enable Comparator Request Select Register | POECMPSEL | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E42Ah | POE | Output Level Control/Status Register 3 | OCSR3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E42Ch | POE | Active Level Setting Register 3 | ALR3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E42Eh | POE | Software Port Output Enable Register | SPOER | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E430h | POE | Port Mode Mask Control Register 0 | PMMCR0 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E432h | POE | Port Mode Mask Control Register 1 | PMMCR1 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E434h | POE | Port Mode Mask Control Register 2 | PMMCR2 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E436h | POE | Port Mode Mask Control Register 3 | PMMCR3 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E438h | POE | Port Output Enable Comparator Request Extended Select Register 0 | POECMPX0 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E439h | POE | Port Output Enable Comparator Request Extended Select Register 1 | POECMPX1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E43Ah | POE | Port Output Enable Comparator Request Extended Select Register 2 | POECMPX2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E43Bh | POE | Port Output Enable Comparator Request Extended Select Register 3 | POECMPX3 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E43Ch | POE | Port Output Enable Comparator Request Extended Select Register 4 | POECMPX4 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E43Dh | POE | Port Output Enable Comparator Request Extended Select Register 5 | POECMPX5 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E440h | POE | Input Level Control/Status Register 8 | ICSR8 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E442h | POE | Input Level Control/Status Register 9 | ICSR9 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E444h | POE | Input Level Control/Status Register 10 | ICSR10 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E446h | POE | Output Level Control/Status Register 4 | OCSR4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E448h | POE | Output Level Control/Status Register 5 | OCSR5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E44Ah | POE | Active Level Setting Register 4 | ALR4 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E44Ch | POE | Active Level Setting Register 5 | ALR5 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E44Eh | POE | Port Output Enable Control Register 4B | POECR4B | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E450h | POE | Port Output Enable Control Register 6B | POECR6B | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E452h | POE | Port Output Enable Control Register 9 | POECR9 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E454h | POE | Port Output Enable Control Register 10 | POECR10 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E456h | POE | Port Output Enable Control Register 11 | POECR11 | 16 | 16 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E458h | POE | Port Output Enable Comparator Request Extended Select Register 6 | POECMPX6 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E459h | POE | Port Output Enable Comparator Request Extended Select Register 7 | POECMPX7 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E45Ah | POE | Port Output Enable Comparator Request Extended Select Register 8 | POECMPX8 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E460h | POE | MTU0 Pin Select Register 1 | M0SELR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E461h | POE | MTU0 Pin Select Register 2 | M0SELR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E462h | POE | MTU3 Pin Select Register | M3SELR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E463h | POE | MTU4 Pin Select Register 1 | M4SELR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E464h | POE | MTU4 Pin Select Register 2 | M4SELR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E465h | POE | MTU6 Pin Select Register | M6SELR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E466h | POE | MTU7 Pin Select Register 1 | M7SELR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E467h | POE | MTU7 Pin Select Register 2 | M7SELR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E468h | POE | MTU9 Pin Select Register 1 | M9SELR1 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |

Table 4.1 List of I/O Registers (Address Order) (32 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|---|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 0009 E469h | POE | MTU9 Pin Select Register 2 | M9SELR2 | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E46Ah | POE | GPTW0 Pin Select Register | G0SELR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E46Bh | POE | GPTW1 Pin Select Register | G1SELR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E46Ch | POE | GPTW2 Pin Select Register | G2SELR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E46Dh | POE | GPTW3 Pin Select Register | G3SELR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E46Eh | POE | GPTW4 Pin Select Register | G4SELR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E46Fh | POE | GPTW5 Pin Select Register | G5SELR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E470h | POE | GPTW6 Pin Select Register | G6SELR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E471h | POE | GPTW7 Pin Select Register | G7SELR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E472h | POE | GPTW8 Pin Select Register | G8SELR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 0009 E473h | POE | GPTW9 Pin Select Register | G9SELR | 8 | 8 | 2, 3 PCLKB | 2 ICLK | POE3B |
| 000A 0000h | USB0 | System Configuration Control Register | SYSCFG | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0004h | USB0 | System Configuration Status Register 0 | SYSSTS0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^{*1}$ | USBb |
| 000A 0008h | USB0 | Device State Control Register 0 | DVSTCTR0 | 16 | 16 | 9 PCLKB or more | Rounded up to the nearest integer greater than $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^{*1}$ | USBb |
| 000A 0014h | USB0 | CFIFO Port Register | CFIFO | 16 | 8, 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0018h | USB0 | D0FIFO Port Register | D0FIFO | 16 | 8, 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 001Ch | USB0 | D1FIFO Port Register | D1FIFO | 16 | 8, 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0020h | USB0 | CFIFO Port Select Register | CFIFOSEL | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0022h | USB0 | CFIFO Port Control Register | CFIFOCTR | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0028h | USB0 | D0FIFO Port Select Register | D0FIFOSEL | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 002Ah | USB0 | D0FIFO Port Control Register | D0FIFOCTR | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 002Ch | USB0 | D1FIFO Port Select Register | D1FIFOSEL | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 002Eh | USB0 | D1FIFO Port Control Register | D1FIFOCTR | 16 | 16 | 3, 4 PCLKB | 2 ICLK | USBb |
| 000A 0030h | USB0 | Interrupt Enable Register 0 | INTENB0 | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^{*1}$ | USBb |
| 000A 0032h | USB0 | Interrupt Enable Register 1 | INTENB1 | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^{*1}$ | USBb |
| 000A 0036h | USB0 | BRDY Interrupt Enable Register | BRDYENB | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^{*1}$ | USBb |
| 000A 0038h | USB0 | NRDY Interrupt Enable Register | NRDYENB | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^{*1}$ | USBb |
| 000A 003Ah | USB0 | BEMP Interrupt Enable Register | BEMPENB | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^{*1}$ | USBb |
| 000A 003Ch | USB0 | SOF Output Configuration Register | SOFCFG | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times (\text{frequency ratio of ICLK/PCLKB})^{*1}$ | USBb |

Table 4.1 List of I/O Registers (Address Order) (33 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|----------------------------------|-----------------|----------------|-------------|-------------------------|--|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000A 0040h | USB0 | Interrupt Status Register 0 | INTSTS0 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0042h | USB0 | Interrupt Status Register 1 | INTSTS1 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0046h | USB0 | BRDY Interrupt Status Register | BRDYSTS | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0048h | USB0 | NRDY Interrupt Status Register | NRDYSTS | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 004Ah | USB0 | BEMP Interrupt Status Register | BEMPSTS | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 004Ch | USB0 | Frame Number Register | FRMNUM | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0054h | USB0 | USB Request Type Register | USBREQ | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0056h | USB0 | USB Request Value Register | USBVAL | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0058h | USB0 | USB Request Index Register | USBINDX | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 005Ah | USB0 | USB Request Length Register | USBLENG | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 005Ch | USB0 | DCP Configuration Register | DCPCFG | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 005Eh | USB0 | DCP Maximum Packet Size Register | DCPMAXP | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0060h | USB0 | DCP Control Register | DCPCTR | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0064h | USB0 | Pipe Window Select Register | PIPESEL | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0068h | USB0 | Pipe Configuration Register | PIPECFG | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |

Table 4.1 List of I/O Registers (Address Order) (34 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|---|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000A 006Ch | USB0 | Pipe Maximum Packet Size Register | PIPEMAXP | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 006Eh | USB0 | Pipe Cycle Control Register | PIPEPERI | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0070h | USB0 | PIPE1 Control Register | PIPE1CTR | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0072h | USB0 | PIPE2 Control Register | PIPE2CTR | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0074h | USB0 | PIPE3 Control Register | PIPE3CTR | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0076h | USB0 | PIPE4 Control Register | PIPE4CTR | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0078h | USB0 | PIPE5 Control Register | PIPE5CTR | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 007Ah | USB0 | PIPE6 Control Register | PIPE6CTR | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 007Ch | USB0 | PIPE7 Control Register | PIPE7CTR | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 007Eh | USB0 | PIPE8 Control Register | PIPE8CTR | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0080h | USB0 | PIPE9 Control Register | PIPE9CTR | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0090h | USB0 | Pipe1 Transaction Counter Enable Register | PIPE1TRE | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0092h | USB0 | Pipe1 Transaction Counter Register | PIPE1TRN | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0094h | USB0 | Pipe2 Transaction Counter Enable Register | PIPE2TRE | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0096h | USB0 | Pipe2 Transaction Counter Register | PIPE2TRN | 16 | 16 | 9 PCLKB or more | Frequency with $1 + 9 \times$ (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |

Table 4.1 List of I/O Registers (Address Order) (35 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|--|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000A 0098h | USB0 | Pipe3 Transaction Counter Enable Register | PIPE3TRE | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 009Ah | USB0 | Pipe3 Transaction Counter Register | PIPE3TRN | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 009Ch | USB0 | Pipe4 Transaction Counter Enable Register | PIPE4TRE | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 009Eh | USB0 | Pipe4 Transaction Counter Register | PIPE4TRN | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 00A0h | USB0 | Pipe5 Transaction Counter Enable Register | PIPE5TRE | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 00A2h | USB0 | Pipe5 Transaction Counter Register | PIPE5TRN | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 00D0h | USB0 | Device Address 0 Configuration Register | DEVADD0 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 00D2h | USB0 | Device Address 1 Configuration Register | DEVADD1 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 00D4h | USB0 | Device Address 2 Configuration Register | DEVADD2 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 00D6h | USB0 | Device Address 3 Configuration Register | DEVADD3 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 00D8h | USB0 | Device Address 4 Configuration Register | DEVADD4 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 00DAh | USB0 | Device Address 5 Configuration Register | DEVADD5 | 16 | 16 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 00F0h | USB0 | PHY Cross Point Adjustment Register | PHYSLEW | 32 | 32 | 9 PCLKB or more | Frequency with 1 + 9 × (frequency ratio of ICLK/PCLKB) ^{*1} | USBb |
| 000A 0C80h | CMPC0 | Comparator Control Register | CMPCTL | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0C84h | CMPC0 | Comparator Input Select Register | CMPSEL0 | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0C88h | CMPC0 | Comparator Reference Voltage Select Register | CMPSEL1 | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0C8Ch | CMPC0 | Comparator Output Monitor Register | CMPMON | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0C90h | CMPC0 | Comparator External Output Enable Register | CMPIOC | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0CA0h | CMPC1 | Comparator Control Register | CMPCTL | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0CA4h | CMPC1 | Comparator Input Select Register | CMPSEL0 | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |

Table 4.1 List of I/O Registers (Address Order) (36 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000A 0CA8h | CMPC1 | Comparator Reference Voltage Select Register | CMPSEL1 | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0CACh | CMPC1 | Comparator Output Monitor Register | CMPMON | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0CB0h | CMPC1 | Comparator External Output Enable Register | CMPIOC | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0CC0h | CMPC2 | Comparator Control Register | CMPCTL | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0CC4h | CMPC2 | Comparator Input Select Register | CMPSEL0 | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0CC8h | CMPC2 | Comparator Reference Voltage Select Register | CMPSEL1 | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0CCCh | CMPC2 | Comparator Output Monitor Register | CMPMON | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0CD0h | CMPC2 | Comparator External Output Enable Register | CMPIOC | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0CE0h | CMPC3 | Comparator Control Register | CMPCTL | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0CE4h | CMPC3 | Comparator Input Select Register | CMPSEL0 | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0CE8h | CMPC3 | Comparator Reference Voltage Select Register | CMPSEL1 | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0CECh | CMPC3 | Comparator Output Monitor Register | CMPMON | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0CF0h | CMPC3 | Comparator External Output Enable Register | CMPIOC | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0D00h | CMPC4 | Comparator Control Register | CMPCTL | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0D04h | CMPC4 | Comparator Input Select Register | CMPSEL0 | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0D08h | CMPC4 | Comparator Reference Voltage Select Register | CMPSEL1 | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0D0Ch | CMPC4 | Comparator Output Monitor Register | CMPMON | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0D10h | CMPC4 | Comparator External Output Enable Register | CMPIOC | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0D20h | CMPC5 | Comparator Control Register | CMPCTL | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0D24h | CMPC5 | Comparator Input Select Register | CMPSEL0 | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0D28h | CMPC5 | Comparator Reference Voltage Select Register | CMPSEL1 | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0D2Ch | CMPC5 | Comparator Output Monitor Register | CMPMON | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000A 0D30h | CMPC5 | Comparator External Output Enable Register | CMPIOC | 8 | 8 | 1, 2 PCLKB | 1, 2 ICLK | CMPC |
| 000C 1200h | MTU3 | Timer Control Register | TCR | 8 | 8, 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1201h | MTU4 | Timer Control Register | TCR | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1202h | MTU3 | Timer Mode Register 1 | TMDR1 | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1203h | MTU4 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1204h | MTU3 | Timer I/O Control Register H | TIORH | 8 | 8, 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1205h | MTU3 | Timer I/O Control Register L | TIORL | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1206h | MTU4 | Timer I/O Control Register H | TIORH | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1207h | MTU4 | Timer I/O Control Register L | TIORL | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1208h | MTU3 | Timer Interrupt Enable Register | TIER | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1209h | MTU4 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 120Ah | MTU | Timer Output Master Enable Register A | TOERA | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 120Dh | MTU | Timer Gate Control Register A | TGCRA | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 120Eh | MTU | Timer Output Control Register 1A | TOCR1A | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 120Fh | MTU | Timer Output Control Register 2A | TOCR2A | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1210h | MTU3 | Timer Counter | TCNT | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1212h | MTU4 | Timer Counter | TCNT | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1214h | MTU | Timer Cycle Data Register A | TCDRA | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1216h | MTU | Timer Dead Time Data Register A | TDDRA | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1218h | MTU3 | Timer General Register A | TGRA | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 121Ah | MTU3 | Timer General Register B | TGRB | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 121Ch | MTU4 | Timer General Register A | TGRA | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 121Eh | MTU4 | Timer General Register B | TGRB | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1220h | MTU | Timer Subcounter A | TCNTSA | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1222h | MTU | Timer Cycle Buffer Register A | TCBRA | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1224h | MTU3 | Timer General Register C | TGRC | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1226h | MTU3 | Timer General Register D | TGRD | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1228h | MTU4 | Timer General Register C | TGRC | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |

Table 4.1 List of I/O Registers (Address Order) (37 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 122Ah | MTU4 | Timer General Register D | TGRD | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 122Ch | MTU3 | Timer Status Register | TSR | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 122Dh | MTU4 | Timer Status Register | TSR | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1230h | MTU | Timer Interrupt Skipping Set Register 1A | TITCR1A | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1231h | MTU | Timer Interrupt Skipping Counter 1A | TITCNT1A | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1232h | MTU | Timer Buffer Transfer Set Register A | TBTERA | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1234h | MTU | Timer Dead Time Enable Register A | TDERA | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1236h | MTU | Timer Output Level Buffer Register A | TOLBRA | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1238h | MTU3 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1239h | MTU4 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 123Ah | MTU | Timer Interrupt Skipping Mode Register A | TITMRA | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 123Bh | MTU | Timer Interrupt Skipping Set Register 2A | TITCR2A | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 123Ch | MTU | Timer Interrupt Skipping Counter 2A | TITCNT2A | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1240h | MTU4 | Timer A/D Converter Start Request Control Register | TADCR | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1244h | MTU4 | Timer A/D Converter Start Request Cycle Set Register A | TADCORA | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1246h | MTU4 | Timer A/D Converter Start Request Cycle Set Register B | TADCORB | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1248h | MTU4 | Timer A/D Converter Start Request Cycle Set Buffer Register A | TADCOBRA | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 124Ah | MTU4 | Timer A/D Converter Start Request Cycle Set Buffer Register B | TADCOBRB | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 124Ch | MTU3 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 124Dh | MTU4 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1260h | MTU | Timer Waveform Control Register A | TWCRA | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1270h | MTU | Timer Mode Register 2A | TMDR2A | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1272h | MTU3 | Timer General Register E | TGRE | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1274h | MTU4 | Timer General Register E | TGRE | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1276h | MTU4 | Timer General Register F | TGRF | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1280h | MTU | Timer Start Register A | TSTRA | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1281h | MTU | Timer Synchronous Register A | TSYRA | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1282h | MTU | Timer Counter Synchronous Start Register | TCSYSTR | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1284h | MTU | Timer Read/Write Enable Register A | TRWERA | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1290h | MTU0 | Noise Filter Control Register 0 | NFCR0 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1291h | MTU1 | Noise Filter Control Register 1 | NFCR1 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1292h | MTU2 | Noise Filter Control Register 2 | NFCR2 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1293h | MTU3 | Noise Filter Control Register 3 | NFCR3 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1294h | MTU4 | Noise Filter Control Register 4 | NFCR4 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1296h | MTU9 | Noise Filter Control Register 9 | NFCR9 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1299h | MTU0 | Noise Filter Control Register C | NFCRC | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1300h | MTU0 | Timer Control Register | TCR | 8 | 8, 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1301h | MTU0 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1302h | MTU0 | Timer I/O Control Register H | TIORH | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1303h | MTU0 | Timer I/O Control Register L | TIORL | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1304h | MTU0 | Timer Interrupt Enable Register | TIER | 8 | 8, 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1306h | MTU0 | Timer Counter | TCNT | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1308h | MTU0 | Timer General Register A | TGRA | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 130Ah | MTU0 | Timer General Register B | TGRB | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 130Ch | MTU0 | Timer General Register C | TGRC | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 130Eh | MTU0 | Timer General Register D | TGRD | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1320h | MTU0 | Timer General Register E | TGRE | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1322h | MTU0 | Timer General Register F | TGRF | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1324h | MTU0 | Timer Interrupt Enable Register 2 | TIER2 | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |

Table 4.1 List of I/O Registers (Address Order) (38 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 1326h | MTU0 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1328h | MTU0 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1380h | MTU1 | Timer Control Register | TCR | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1381h | MTU1 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1382h | MTU1 | Timer I/O Control Register | TIOR | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1384h | MTU1 | Timer Interrupt Enable Register | TIER | 8 | 8, 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1385h | MTU1 | Timer Status Register | TSR | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1386h | MTU1 | Timer Counter | TCNT | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1388h | MTU1 | Timer General Register A | TGRA | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 138Ah | MTU1 | Timer General Register B | TGRB | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1390h | MTU1 | Timer Input Capture Control Register | TICCR | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1391h | MTU1 | Timer Mode Register 3 | TMDR3 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1394h | MTU1 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 13A0h | MTU1 | Timer Longword Counter | TCNTLW | 32 | 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 13A4h | MTU1 | Timer Longword General Register | TGRALW | 32 | 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 13A8h | MTU1 | Timer Longword General Register | TGRBLW | 32 | 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1400h | MTU2 | Timer Control Register | TCR | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1401h | MTU2 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1402h | MTU2 | Timer I/O Control Register | TIOR | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1404h | MTU2 | Timer Interrupt Enable Register | TIER | 8 | 8, 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1405h | MTU2 | Timer Status Register | TSR | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1406h | MTU2 | Timer Counter | TCNT | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1408h | MTU2 | Timer General Register A | TGRA | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 140Ah | MTU2 | Timer General Register B | TGRB | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 140Ch | MTU2 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1580h | MTU9 | Timer Control Register | TCR | 8 | 8, 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1581h | MTU9 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1582h | MTU9 | Timer I/O Control Register H | TIORH | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1583h | MTU9 | Timer I/O Control Register L | TIORL | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1584h | MTU9 | Timer Interrupt Enable Register | TIER | 8 | 8, 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1586h | MTU9 | Timer Counter | TCNT | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1588h | MTU9 | Timer General Register A | TGRA | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 158Ah | MTU9 | Timer General Register B | TGRB | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 158Ch | MTU9 | Timer General Register C | TGRC | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 158Eh | MTU9 | Timer General Register D | TGRD | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 15A0h | MTU9 | Timer General Register E | TGRE | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 15A2h | MTU9 | Timer General Register F | TGRF | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 15A4h | MTU9 | Timer Interrupt Enable Register 2 | TIER2 | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 15A6h | MTU9 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 15A8h | MTU9 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A00h | MTU6 | Timer Control Register | TCR | 8 | 8, 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A01h | MTU7 | Timer Control Register | TCR | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A02h | MTU6 | Timer Mode Register 1 | TMDR1 | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A03h | MTU7 | Timer Mode Register 1 | TMDR1 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A04h | MTU6 | Timer I/O Control Register H | TIORH | 8 | 8, 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A05h | MTU6 | Timer I/O Control Register L | TIORL | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A06h | MTU7 | Timer I/O Control Register H | TIORH | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A07h | MTU7 | Timer I/O Control Register L | TIORL | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A08h | MTU6 | Timer Interrupt Enable Register | TIER | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A09h | MTU7 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |

Table 4.1 List of I/O Registers (Address Order) (39 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 1A0Ah | MTU | Timer Output Master Enable Register B | TOERB | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A0Dh | MTU | Timer Gate Control Register B | TGCRB | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A0Eh | MTU | Timer Output Control Register 1B | TOCR1B | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A0Fh | MTU | Timer Output Control Register 2B | TOCR2B | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A10h | MTU6 | Timer Counter | TCNT | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A12h | MTU7 | Timer Counter | TCNT | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A14h | MTU | Timer Cycle Data Register B | TCDRB | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A16h | MTU | Timer Dead Time Data Register B | TDDR | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A18h | MTU6 | Timer General Register A | TGRA | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A1Ah | MTU6 | Timer General Register B | TGRB | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A1Ch | MTU7 | Timer General Register A | TGRA | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A1Eh | MTU7 | Timer General Register B | TGRB | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A20h | MTU | Timer Subcounter B | TCNTSB | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A22h | MTU | Timer Cycle Buffer Register B | TCTBRB | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A24h | MTU6 | Timer General Register C | TGRC | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A26h | MTU6 | Timer General Register D | TGRD | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A28h | MTU7 | Timer General Register C | TGRC | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A2Ah | MTU7 | Timer General Register D | TGRD | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A2Ch | MTU6 | Timer Status Register | TSR | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A2Dh | MTU7 | Timer Status Register | TSR | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A30h | MTU | Timer Interrupt Skipping Set Register 1B | TITCR1B | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A31h | MTU | Timer Interrupt Skipping Counter 1B | TITCNT1B | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A32h | MTU | Timer Buffer Transfer Set Register B | TBTERB | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A34h | MTU | Timer Dead Time Enable Register B | TDERB | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A36h | MTU | Timer Output Level Buffer Register B | TOLBRB | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A38h | MTU6 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A39h | MTU7 | Timer Buffer Operation Transfer Mode Register | TBTM | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A3Ah | MTU | Timer Interrupt Skipping Mode Register B | TITMRB | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A3Bh | MTU | Timer Interrupt Skipping Set Register 2B | TITCR2B | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A3Ch | MTU | Timer Interrupt Skipping Counter 2B | TITCNT2B | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A40h | MTU7 | Timer A/D Converter Start Request Control Register | TADCR | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A44h | MTU7 | Timer A/D Converter Start Request Cycle Set Register A | TADCORA | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A46h | MTU7 | Timer A/D Converter Start Request Cycle Set Register B | TADCORB | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A48h | MTU7 | Timer A/D Converter Start Request Cycle Set Buffer Register A | TADCOBRA | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A4Ah | MTU7 | Timer A/D Converter Start Request Cycle Set Buffer Register B | TADCOBRB | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A4Ch | MTU6 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A4Dh | MTU7 | Timer Control Register 2 | TCR2 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A50h | MTU6 | Timer Synchronous Clear Register | TSYCR | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A60h | MTU | Timer Waveform Control Register B | TWCRB | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A70h | MTU | Timer Mode Register 2B | TMDR2B | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A72h | MTU6 | Timer General Register E | TGRE | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A74h | MTU7 | Timer General Register E | TGRE | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A76h | MTU7 | Timer General Register F | TGRF | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A80h | MTU | Timer Start Register B | TSTRB | 8 | 8, 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A81h | MTU | Timer Synchronous Register B | TSYRB | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A84h | MTU | Timer Read/Write Enable Register B | TRWERB | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A93h | MTU6 | Noise Filter Control Register 6 | NFCR6 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A94h | MTU7 | Noise Filter Control Register 7 | NFCR7 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1A95h | MTU5 | Noise Filter Control Register 5 | NFCR5 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |

Table 4.1 List of I/O Registers (Address Order) (40 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 1C80h | MTU5 | Timer Counter U | TCNTU | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1C82h | MTU5 | Timer General Register U | TGRU | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1C84h | MTU5 | Timer Control Register U | TCRU | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1C85h | MTU5 | Timer Control Register 2U | TCR2U | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1C86h | MTU5 | Timer I/O Control Register U | TIORU | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1C90h | MTU5 | Timer Counter V | TCNTV | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1C92h | MTU5 | Timer General Register V | TGRV | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1C94h | MTU5 | Timer Control Register V | TCRV | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1C95h | MTU5 | Timer Control Register 2V | TCR2V | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1C96h | MTU5 | Timer I/O Control Register V | TIORV | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1CA0h | MTU5 | Timer Counter W | TCNTW | 16 | 16, 32 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1CA2h | MTU5 | Timer General Register W | TGRW | 16 | 16 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1CA4h | MTU5 | Timer Control Register W | TCRW | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1CA5h | MTU5 | Timer Control Register 2W | TCR2W | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1CA6h | MTU5 | Timer I/O Control Register W | TIORW | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1CB2h | MTU5 | Timer Interrupt Enable Register | TIER | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1CB4h | MTU5 | Timer Start Register | TSTR | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1CB6h | MTU5 | Timer Compare Match Clear Register | TCNTCMPCLR | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1D30h | MTU | A/D Conversion Start Request Select Register 0 | TADSTRGR0 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 1D32h | MTU | A/D Conversion Start Request Select Register 1 | TADSTRGR1 | 8 | 8 | 4 to 7 PCLKA | 2 to 4 ICLK | MTU3d |
| 000C 2000h | GPTW0 | General PWM Timer Write-Protection Register | GTWP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2004h | GPTW0 | General PWM Timer Software Start Register | GTSTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2008h | GPTW0 | General PWM Timer Software Stop Register | GTSTP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 200Ch | GPTW0 | General PWM Timer Software Clear Register | GTCLR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2010h | GPTW0 | General PWM Timer Start Source Select Register | GTSSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2014h | GPTW0 | General PWM Timer Stop Source Select Register | GTSPSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2018h | GPTW0 | General PWM Timer Clear Source Select Register | GTCSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 201Ch | GPTW0 | General PWM Timer Count-Up Source Select Register | GTUPSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2020h | GPTW0 | General PWM Timer Count-Down Source Select Register | GTDNSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2024h | GPTW0 | General PWM Timer Input Capture Source Select Register A | GTICASR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2028h | GPTW0 | General PWM Timer Input Capture Source Select Register B | GTICBSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 202Ch | GPTW0 | General PWM Timer Control Register | GTCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2030h | GPTW0 | General PWM Timer Count Direction and Duty Setting Register | GTUDDTYC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2034h | GPTW0 | General PWM Timer I/O Control Register | GTIOR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2038h | GPTW0 | General PWM Timer Interrupt Output Setting Register | GTINTAD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 203Ch | GPTW0 | General PWM Timer Status Register | GTST | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2040h | GPTW0 | General PWM Timer Buffer Enable Register | GTBER | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2044h | GPTW0 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register | GTITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2048h | GPTW0 | General PWM Timer Counter | GTCNT | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 204Ch | GPTW0 | General PWM Timer Compare Capture Register A | GTCCRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2050h | GPTW0 | General PWM Timer Compare Capture Register B | GTCCRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2054h | GPTW0 | General PWM Timer Compare Capture Register C | GTCCRC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2058h | GPTW0 | General PWM Timer Compare Capture Register E | GTCCRE | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 205Ch | GPTW0 | General PWM Timer Compare Capture Register D | GTCCRD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2060h | GPTW0 | General PWM Timer Compare Capture Register F | GTCCRF | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2064h | GPTW0 | General PWM Timer Period Setting Register | GTPR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2068h | GPTW0 | General PWM Timer Period Setting Buffer Register | GTPBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |

Table 4.1 List of I/O Registers (Address Order) (41 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 206Ch | GPTW0 | General PWM Timer Period Setting Double-Buffer Register | GTPDBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2070h | GPTW0 | A/D Converter Start Request Timing Register A | GTADTRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2074h | GPTW0 | A/D Converter Start Request Timing Buffer Register A | GTADTBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2078h | GPTW0 | A/D Converter Start Request Timing Double-Buffer Register A | GTADTDBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 207Ch | GPTW0 | A/D Converter Start Request Timing Register B | GTADTRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2080h | GPTW0 | A/D Converter Start Request Timing Buffer Register B | GTADTBRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2084h | GPTW0 | A/D Converter Start Request Timing Double-Buffer Register B | GTADTDBRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2088h | GPTW0 | General PWM Timer Dead Time Control Register | GTDTCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 208Ch | GPTW0 | General PWM Timer Dead Time Value Register U | GTDVU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2090h | GPTW0 | General PWM Timer Dead Time Value Register D | GTDVD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2094h | GPTW0 | General PWM Timer Dead Time Buffer Register U | GTDBU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2098h | GPTW0 | General PWM Timer Dead Time Buffer Register D | GTDBD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 209Ch | GPTW0 | General PWM Timer Output Protection Function Status Register | GTSOS | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 20A0h | GPTW0 | General PWM Timer Output Protection Function Temporary Release Register | GTSOTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 20A4h | GPTW0 | General PWM Timer A/D Converter Start Request Signal Monitoring Register | GTADSMR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 20A8h | GPTW0 | General PWM Timer Extended Interrupt Skipping Counter Control Register | GTEITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 20ACh | GPTW0 | General PWM Timer Extended Interrupt Skipping Setting Register 1 | GTEITLI1 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 20B0h | GPTW0 | General PWM Timer Extended Interrupt Skipping Setting Register 2 | GTEITLI2 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 20B4h | GPTW0 | General PWM Timer Extended Buffer Transfer Skipping Setting Register | GTEITLB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 20D0h | GPTW0 | General PWM Timer Operation Enable Bit Simultaneous Control Channel Select Register | GTSECSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 20D4h | GPTW0 | General PWM Timer Operation Enable Bit Simultaneous Control Register | GTSECR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2100h | GPTW1 | General PWM Timer Write-Protection Register | GTWP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2104h | GPTW1 | General PWM Timer Software Start Register | GTSTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2108h | GPTW1 | General PWM Timer Software Stop Register | GTSTP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 210Ch | GPTW1 | General PWM Timer Software Clear Register | GTCLR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2110h | GPTW1 | General PWM Timer Start Source Select Register | GTSSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2114h | GPTW1 | General PWM Timer Stop Source Select Register | GTSPSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2118h | GPTW1 | General PWM Timer Clear Source Select Register | GTCSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 211Ch | GPTW1 | General PWM Timer Count-Up Source Select Register | GTUPSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2120h | GPTW1 | General PWM Timer Count-Down Source Select Register | GTNSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2124h | GPTW1 | General PWM Timer Input Capture Source Select Register A | GTICASR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2128h | GPTW1 | General PWM Timer Input Capture Source Select Register B | GTICBSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 212Ch | GPTW1 | General PWM Timer Control Register | GTCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2130h | GPTW1 | General PWM Timer Count Direction and Duty Setting Register | GTUDDTYC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2134h | GPTW1 | General PWM Timer I/O Control Register | GTIOR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2138h | GPTW1 | General PWM Timer Interrupt Output Setting Register | GTINTAD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 213Ch | GPTW1 | General PWM Timer Status Register | GTST | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2140h | GPTW1 | General PWM Timer Buffer Enable Register | GTBER | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2144h | GPTW1 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register | GTITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2148h | GPTW1 | General PWM Timer Counter | GTCNT | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 214Ch | GPTW1 | General PWM Timer Compare Capture Register A | GTCCRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |

Table 4.1 List of I/O Registers (Address Order) (42 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 2150h | GPTW1 | General PWM Timer Compare Capture Register B | GTCCRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2154h | GPTW1 | General PWM Timer Compare Capture Register C | GTCCRC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2158h | GPTW1 | General PWM Timer Compare Capture Register E | GTCCRE | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 215Ch | GPTW1 | General PWM Timer Compare Capture Register D | GTCCRD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2160h | GPTW1 | General PWM Timer Compare Capture Register F | GTCCRF | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2164h | GPTW1 | General PWM Timer Period Setting Register | GTPR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2168h | GPTW1 | General PWM Timer Period Setting Buffer Register | GTPBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 216Ch | GPTW1 | General PWM Timer Period Setting Double-Buffer Register | GTPDBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2170h | GPTW1 | A/D Converter Start Request Timing Register A | GTADTRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2174h | GPTW1 | A/D Converter Start Request Timing Buffer Register A | GTADTBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2178h | GPTW1 | A/D Converter Start Request Timing Double-Buffer Register A | GTADTDBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 217Ch | GPTW1 | A/D Converter Start Request Timing Register B | GTADTRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2180h | GPTW1 | A/D Converter Start Request Timing Buffer Register B | GTADTBRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2184h | GPTW1 | A/D Converter Start Request Timing Double-Buffer Register B | GTADTDBRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2188h | GPTW1 | General PWM Timer Dead Time Control Register | GTDTCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 218Ch | GPTW1 | General PWM Timer Dead Time Value Register U | GTDVU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2190h | GPTW1 | General PWM Timer Dead Time Value Register D | GTDVD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2194h | GPTW1 | General PWM Timer Dead Time Buffer Register U | GTDBU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2198h | GPTW1 | General PWM Timer Dead Time Buffer Register D | GTDBD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 219Ch | GPTW1 | General PWM Timer Output Protection Function Status Register | GTSOS | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 21A0h | GPTW1 | General PWM Timer Output Protection Function Temporary Release Register | GTSOTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 21A4h | GPTW1 | General PWM Timer A/D Converter Start Request Signal Monitoring Register | GTADSMR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 21A8h | GPTW1 | General PWM Timer Extended Interrupt Skipping Counter Control Register | GTEITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 21ACh | GPTW1 | General PWM Timer Extended Interrupt Skipping Setting Register 1 | GTEITLI1 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 21B0h | GPTW1 | General PWM Timer Extended Interrupt Skipping Setting Register 2 | GTEITLI2 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 21B4h | GPTW1 | General PWM Timer Extended Buffer Transfer Skipping Setting Register | GTEITLB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 21D0h | GPTW1 | General PWM Timer Operation Enable Bit Simultaneous Control Channel Select Register | GTSECSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 21D4h | GPTW1 | General PWM Timer Operation Enable Bit Simultaneous Control Register | GTSECR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2200h | GPTW2 | General PWM Timer Write-Protection Register | GTWP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2204h | GPTW2 | General PWM Timer Software Start Register | GTSTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2208h | GPTW2 | General PWM Timer Software Stop Register | GTSTP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 220Ch | GPTW2 | General PWM Timer Software Clear Register | GTCLR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2210h | GPTW2 | General PWM Timer Start Source Select Register | GTSSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2214h | GPTW2 | General PWM Timer Stop Source Select Register | GTPSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2218h | GPTW2 | General PWM Timer Clear Source Select Register | GTCSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 221Ch | GPTW2 | General PWM Timer Count-Up Source Select Register | GTUPSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2220h | GPTW2 | General PWM Timer Count-Down Source Select Register | GTNSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2224h | GPTW2 | General PWM Timer Input Capture Source Select Register A | GTICASR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2228h | GPTW2 | General PWM Timer Input Capture Source Select Register B | GTICBSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 222Ch | GPTW2 | General PWM Timer Control Register | GTCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2230h | GPTW2 | General PWM Timer Count Direction and Duty Setting Register | GTUDDTYC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |

Table 4.1 List of I/O Registers (Address Order) (43 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 2234h | GPTW2 | General PWM Timer I/O Control Register | GTIOR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2238h | GPTW2 | General PWM Timer Interrupt Output Setting Register | GTINTAD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 223Ch | GPTW2 | General PWM Timer Status Register | GTST | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2240h | GPTW2 | General PWM Timer Buffer Enable Register | GTBER | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2244h | GPTW2 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register | GTITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2248h | GPTW2 | General PWM Timer Counter | GT CNT | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 224Ch | GPTW2 | General PWM Timer Compare Capture Register A | GTCCRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2250h | GPTW2 | General PWM Timer Compare Capture Register B | GTCCRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2254h | GPTW2 | General PWM Timer Compare Capture Register C | GTCCRC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2258h | GPTW2 | General PWM Timer Compare Capture Register E | GTCCRE | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 225Ch | GPTW2 | General PWM Timer Compare Capture Register D | GTCCRD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2260h | GPTW2 | General PWM Timer Compare Capture Register F | GTCCRF | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2264h | GPTW2 | General PWM Timer Period Setting Register | GT PR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2268h | GPTW2 | General PWM Timer Period Setting Buffer Register | GT PBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 226Ch | GPTW2 | General PWM Timer Period Setting Double-Buffer Register | GT PDBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2270h | GPTW2 | A/D Converter Start Request Timing Register A | GTADTRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2274h | GPTW2 | A/D Converter Start Request Timing Buffer Register A | GTADTBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2278h | GPTW2 | A/D Converter Start Request Timing Double-Buffer Register A | GTADTBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 227Ch | GPTW2 | A/D Converter Start Request Timing Register B | GTADTRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2280h | GPTW2 | A/D Converter Start Request Timing Buffer Register B | GTADTRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2284h | GPTW2 | A/D Converter Start Request Timing Double-Buffer Register B | GTADTRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2288h | GPTW2 | General PWM Timer Dead Time Control Register | GTDT CR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 228Ch | GPTW2 | General PWM Timer Dead Time Value Register U | GT DVU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2290h | GPTW2 | General PWM Timer Dead Time Value Register D | GT DVD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2294h | GPTW2 | General PWM Timer Dead Time Buffer Register U | GT DBU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2298h | GPTW2 | General PWM Timer Dead Time Buffer Register D | GT DBD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 229Ch | GPTW2 | General PWM Timer Output Protection Function Status Register | GT SOS | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 22A0h | GPTW2 | General PWM Timer Output Protection Function Temporary Release Register | GT SOTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 22A4h | GPTW2 | General PWM Timer A/D Converter Start Request Signal Monitoring Register | GT ADSMR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 22A8h | GPTW2 | General PWM Timer Extended Interrupt Skipping Counter Control Register | GT EITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 22ACh | GPTW2 | General PWM Timer Extended Interrupt Skipping Setting Register 1 | GT EITL1 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 22B0h | GPTW2 | General PWM Timer Extended Interrupt Skipping Setting Register 2 | GT EITL2 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 22B4h | GPTW2 | General PWM Timer Extended Buffer Transfer Skipping Setting Register | GT EITLB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 22D0h | GPTW2 | General PWM Timer Operation Enable Bit Simultaneous Control Channel Select Register | GT SECSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 22D4h | GPTW2 | General PWM Timer Operation Enable Bit Simultaneous Control Register | GT SECR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2300h | GPTW3 | General PWM Timer Write-Protection Register | GT WP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2304h | GPTW3 | General PWM Timer Software Start Register | GT STR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2308h | GPTW3 | General PWM Timer Software Stop Register | GT STP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 230Ch | GPTW3 | General PWM Timer Software Clear Register | GT CLR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2310h | GPTW3 | General PWM Timer Start Source Select Register | GT SSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2314h | GPTW3 | General PWM Timer Stop Source Select Register | GT PSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2318h | GPTW3 | General PWM Timer Clear Source Select Register | GT CSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |

Table 4.1 List of I/O Registers (Address Order) (44 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 231Ch | GPTW3 | General PWM Timer Count-Up Source Select Register | GTUPSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2320h | GPTW3 | General PWM Timer Count-Down Source Select Register | GTDNSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2324h | GPTW3 | General PWM Timer Input Capture Source Select Register A | GTICASR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2328h | GPTW3 | General PWM Timer Input Capture Source Select Register B | GTICBSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 232Ch | GPTW3 | General PWM Timer Control Register | GTCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2330h | GPTW3 | General PWM Timer Count Direction and Duty Setting Register | GTUDDTYC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2334h | GPTW3 | General PWM Timer I/O Control Register | GTIOR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2338h | GPTW3 | General PWM Timer Interrupt Output Setting Register | GTINTAD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 233Ch | GPTW3 | General PWM Timer Status Register | GTST | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2340h | GPTW3 | General PWM Timer Buffer Enable Register | GTBER | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2344h | GPTW3 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register | GTITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2348h | GPTW3 | General PWM Timer Counter | GTCNT | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 234Ch | GPTW3 | General PWM Timer Compare Capture Register A | GTCCRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2350h | GPTW3 | General PWM Timer Compare Capture Register B | GTCCRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2354h | GPTW3 | General PWM Timer Compare Capture Register C | GTCCRC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2358h | GPTW3 | General PWM Timer Compare Capture Register E | GTCCRE | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 235Ch | GPTW3 | General PWM Timer Compare Capture Register D | GTCCRD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2360h | GPTW3 | General PWM Timer Compare Capture Register F | GTCCRF | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2364h | GPTW3 | General PWM Timer Period Setting Register | GTPR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2368h | GPTW3 | General PWM Timer Period Setting Buffer Register | GTPBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 236Ch | GPTW3 | General PWM Timer Period Setting Double-Buffer Register | GTPDBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2370h | GPTW3 | A/D Converter Start Request Timing Register A | GTADTRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2374h | GPTW3 | A/D Converter Start Request Timing Buffer Register A | GTADTBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2378h | GPTW3 | A/D Converter Start Request Timing Double-Buffer Register A | GTADTDBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 237Ch | GPTW3 | A/D Converter Start Request Timing Register B | GTADTRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2380h | GPTW3 | A/D Converter Start Request Timing Buffer Register B | GTADTBRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2384h | GPTW3 | A/D Converter Start Request Timing Double-Buffer Register B | GTADTDBRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2388h | GPTW3 | General PWM Timer Dead Time Control Register | GTDTCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 238Ch | GPTW3 | General PWM Timer Dead Time Value Register U | GTDVU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2390h | GPTW3 | General PWM Timer Dead Time Value Register D | GTDVD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2394h | GPTW3 | General PWM Timer Dead Time Buffer Register U | GTDBU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2398h | GPTW3 | General PWM Timer Dead Time Buffer Register D | GTDBD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 239Ch | GPTW3 | General PWM Timer Output Protection Function Status Register | GTSOS | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 23A0h | GPTW3 | General PWM Timer Output Protection Function Temporary Release Register | GTSOTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 23A4h | GPTW3 | General PWM Timer A/D Converter Start Request Signal Monitoring Register | GTADSMR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 23A8h | GPTW3 | General PWM Timer Extended Interrupt Skipping Counter Control Register | GTEITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 23ACh | GPTW3 | General PWM Timer Extended Interrupt Skipping Setting Register 1 | GTEITLI1 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 23B0h | GPTW3 | General PWM Timer Extended Interrupt Skipping Setting Register 2 | GTEITLI2 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 23B4h | GPTW3 | General PWM Timer Extended Buffer Transfer Skipping Setting Register | GTEITLB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 23D0h | GPTW3 | General PWM Timer Operation Enable Bit Simultaneous Control Channel Select Register | GTSECSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 23D4h | GPTW3 | General PWM Timer Operation Enable Bit Simultaneous Control Register | GTSECR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |

Table 4.1 List of I/O Registers (Address Order) (45 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 2400h | GPTW4 | General PWM Timer Write-Protection Register | GTWP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2404h | GPTW4 | General PWM Timer Software Start Register | GTSTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2408h | GPTW4 | General PWM Timer Software Stop Register | GTSTP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 240Ch | GPTW4 | General PWM Timer Software Clear Register | GTCLR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2410h | GPTW4 | General PWM Timer Start Source Select Register | GTSSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2414h | GPTW4 | General PWM Timer Stop Source Select Register | GTPSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2418h | GPTW4 | General PWM Timer Clear Source Select Register | GTCSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 241Ch | GPTW4 | General PWM Timer Count-Up Source Select Register | GTUPSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2420h | GPTW4 | General PWM Timer Count-Down Source Select Register | GTNSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2424h | GPTW4 | General PWM Timer Input Capture Source Select Register A | GTICASR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2428h | GPTW4 | General PWM Timer Input Capture Source Select Register B | GTICBSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 242Ch | GPTW4 | General PWM Timer Control Register | GTCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2430h | GPTW4 | General PWM Timer Count Direction and Duty Setting Register | GTUDDTYC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2434h | GPTW4 | General PWM Timer I/O Control Register | GTIOR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2438h | GPTW4 | General PWM Timer Interrupt Output Setting Register | GTINTAD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 243Ch | GPTW4 | General PWM Timer Status Register | GTST | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2440h | GPTW4 | General PWM Timer Buffer Enable Register | GTBER | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2444h | GPTW4 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register | GTITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2448h | GPTW4 | General PWM Timer Counter | GT CNT | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 244Ch | GPTW4 | General PWM Timer Compare Capture Register A | GTCCRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2450h | GPTW4 | General PWM Timer Compare Capture Register B | GTCCRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2454h | GPTW4 | General PWM Timer Compare Capture Register C | GTCCRC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2458h | GPTW4 | General PWM Timer Compare Capture Register E | GTCCRE | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 245Ch | GPTW4 | General PWM Timer Compare Capture Register D | GTCCRD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2460h | GPTW4 | General PWM Timer Compare Capture Register F | GTCCRF | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2464h | GPTW4 | General PWM Timer Period Setting Register | GT PR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2468h | GPTW4 | General PWM Timer Period Setting Buffer Register | GTPBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 246Ch | GPTW4 | General PWM Timer Period Setting Double-Buffer Register | GTPDBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2470h | GPTW4 | A/D Converter Start Request Timing Register A | GTADTRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2474h | GPTW4 | A/D Converter Start Request Timing Buffer Register A | GTADTBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2478h | GPTW4 | A/D Converter Start Request Timing Double-Buffer Register A | GTADTDBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 247Ch | GPTW4 | A/D Converter Start Request Timing Register B | GTADTRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2480h | GPTW4 | A/D Converter Start Request Timing Buffer Register B | GTADTBRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2484h | GPTW4 | A/D Converter Start Request Timing Double-Buffer Register B | GTADTDBRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2488h | GPTW4 | General PWM Timer Dead Time Control Register | GTDT CR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 248Ch | GPTW4 | General PWM Timer Dead Time Value Register U | GT DVU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2490h | GPTW4 | General PWM Timer Dead Time Value Register D | GT DVD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2494h | GPTW4 | General PWM Timer Dead Time Buffer Register U | GT DBU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2498h | GPTW4 | General PWM Timer Dead Time Buffer Register D | GT DBD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 249Ch | GPTW4 | General PWM Timer Output Protection Function Status Register | GTSOS | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 24A0h | GPTW4 | General PWM Timer Output Protection Function Temporary Release Register | GTSOTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 24A4h | GPTW4 | General PWM Timer A/D Converter Start Request Signal Monitoring Register | GTADSMR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 24A8h | GPTW4 | General PWM Timer Extended Interrupt Skipping Counter Control Register | GTEITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |

Table 4.1 List of I/O Registers (Address Order) (46 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 24ACh | GPTW4 | General PWM Timer Extended Interrupt Skipping Setting Register 1 | GTEITLI1 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 24B0h | GPTW4 | General PWM Timer Extended Interrupt Skipping Setting Register 2 | GTEITLI2 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 24B4h | GPTW4 | General PWM Timer Extended Buffer Transfer Skipping Setting Register | GTEITLB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 24D0h | GPTW4 | General PWM Timer Operation Enable Bit Simultaneous Control Channel Select Register | GTSECSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 24D4h | GPTW4 | General PWM Timer Operation Enable Bit Simultaneous Control Register | GTSECR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2500h | GPTW5 | General PWM Timer Write-Protection Register | GTWP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2504h | GPTW5 | General PWM Timer Software Start Register | GTSTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2508h | GPTW5 | General PWM Timer Software Stop Register | GTSTP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 250Ch | GPTW5 | General PWM Timer Software Clear Register | GTCLR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2510h | GPTW5 | General PWM Timer Start Source Select Register | GTSSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2514h | GPTW5 | General PWM Timer Stop Source Select Register | GTCSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2518h | GPTW5 | General PWM Timer Clear Source Select Register | GTCSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 251Ch | GPTW5 | General PWM Timer Count-Up Source Select Register | GTUPSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2520h | GPTW5 | General PWM Timer Count-Down Source Select Register | GTDNSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2524h | GPTW5 | General PWM Timer Input Capture Source Select Register A | GTICASR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2528h | GPTW5 | General PWM Timer Input Capture Source Select Register B | GTICBSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 252Ch | GPTW5 | General PWM Timer Control Register | GTCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2530h | GPTW5 | General PWM Timer Count Direction and Duty Setting Register | GTUDDTYC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2534h | GPTW5 | General PWM Timer I/O Control Register | GTIOR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2538h | GPTW5 | General PWM Timer Interrupt Output Setting Register | GTINTAD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 253Ch | GPTW5 | General PWM Timer Status Register | GTST | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2540h | GPTW5 | General PWM Timer Buffer Enable Register | GTBER | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2544h | GPTW5 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register | GTITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2548h | GPTW5 | General PWM Timer Counter | GTCNT | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 254Ch | GPTW5 | General PWM Timer Compare Capture Register A | GTCCRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2550h | GPTW5 | General PWM Timer Compare Capture Register B | GTCCRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2554h | GPTW5 | General PWM Timer Compare Capture Register C | GTCCRC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2558h | GPTW5 | General PWM Timer Compare Capture Register E | GTCCRE | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 255Ch | GPTW5 | General PWM Timer Compare Capture Register D | GTCCRD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2560h | GPTW5 | General PWM Timer Compare Capture Register F | GTCCRF | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2564h | GPTW5 | General PWM Timer Period Setting Register | GTPR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2568h | GPTW5 | General PWM Timer Period Setting Buffer Register | GTPBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 256Ch | GPTW5 | General PWM Timer Period Setting Double-Buffer Register | GTPDBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2570h | GPTW5 | A/D Converter Start Request Timing Register A | GTADTRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2574h | GPTW5 | A/D Converter Start Request Timing Buffer Register A | GTADTBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2578h | GPTW5 | A/D Converter Start Request Timing Double-Buffer Register A | GTADTBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 257Ch | GPTW5 | A/D Converter Start Request Timing Register B | GTADTRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2580h | GPTW5 | A/D Converter Start Request Timing Buffer Register B | GTADTBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2584h | GPTW5 | A/D Converter Start Request Timing Double-Buffer Register B | GTADTBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2588h | GPTW5 | General PWM Timer Dead Time Control Register | GTDTCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 258Ch | GPTW5 | General PWM Timer Dead Time Value Register U | GTDVU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2590h | GPTW5 | General PWM Timer Dead Time Value Register D | GTDVD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2594h | GPTW5 | General PWM Timer Dead Time Buffer Register U | GTDBU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |

Table 4.1 List of I/O Registers (Address Order) (47 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 2598h | GPTW5 | General PWM Timer Dead Time Buffer Register D | GTDBD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 259Ch | GPTW5 | General PWM Timer Output Protection Function Status Register | GTSOS | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 25A0h | GPTW5 | General PWM Timer Output Protection Function Temporary Release Register | GTSOTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 25A4h | GPTW5 | General PWM Timer A/D Converter Start Request Signal Monitoring Register | GTADSMR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 25A8h | GPTW5 | General PWM Timer Extended Interrupt Skipping Counter Control Register | GTEITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 25ACh | GPTW5 | General PWM Timer Extended Interrupt Skipping Setting Register 1 | GTEITLI1 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 25B0h | GPTW5 | General PWM Timer Extended Interrupt Skipping Setting Register 2 | GTEITLI2 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 25B4h | GPTW5 | General PWM Timer Extended Buffer Transfer Skipping Setting Register | GTEITLB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 25D0h | GPTW5 | General PWM Timer Operation Enable Bit Simultaneous Control Channel Select Register | GTSECSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 25D4h | GPTW5 | General PWM Timer Operation Enable Bit Simultaneous Control Register | GTSECR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2600h | GPTW6 | General PWM Timer Write-Protection Register | GTWP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2604h | GPTW6 | General PWM Timer Software Start Register | GTSTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2608h | GPTW6 | General PWM Timer Software Stop Register | GTSTP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 260Ch | GPTW6 | General PWM Timer Software Clear Register | GTCLR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2610h | GPTW6 | General PWM Timer Start Source Select Register | GTSSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2614h | GPTW6 | General PWM Timer Stop Source Select Register | GTPSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2618h | GPTW6 | General PWM Timer Clear Source Select Register | GTCSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 261Ch | GPTW6 | General PWM Timer Count-Up Source Select Register | GTUPSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2620h | GPTW6 | General PWM Timer Count-Down Source Select Register | GTDNSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2624h | GPTW6 | General PWM Timer Input Capture Source Select Register A | GTICASR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2628h | GPTW6 | General PWM Timer Input Capture Source Select Register B | GTICBSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 262Ch | GPTW6 | General PWM Timer Control Register | GTCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2630h | GPTW6 | General PWM Timer Count Direction and Duty Setting Register | GTUDDTYC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2634h | GPTW6 | General PWM Timer I/O Control Register | GTIOR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2638h | GPTW6 | General PWM Timer Interrupt Output Setting Register | GTINTAD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 263Ch | GPTW6 | General PWM Timer Status Register | GTST | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2640h | GPTW6 | General PWM Timer Buffer Enable Register | GTBER | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2644h | GPTW6 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register | GTITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2648h | GPTW6 | General PWM Timer Counter | GTCNT | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 264Ch | GPTW6 | General PWM Timer Compare Capture Register A | GTCCRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2650h | GPTW6 | General PWM Timer Compare Capture Register B | GTCCRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2654h | GPTW6 | General PWM Timer Compare Capture Register C | GTCCRC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2658h | GPTW6 | General PWM Timer Compare Capture Register E | GTCCRE | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 265Ch | GPTW6 | General PWM Timer Compare Capture Register D | GTCCRD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2660h | GPTW6 | General PWM Timer Compare Capture Register F | GTCCRF | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2664h | GPTW6 | General PWM Timer Period Setting Register | GTPR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2668h | GPTW6 | General PWM Timer Period Setting Buffer Register | GTPBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 266Ch | GPTW6 | General PWM Timer Period Setting Double-Buffer Register | GTPDBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2670h | GPTW6 | A/D Converter Start Request Timing Register A | GTADTRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2674h | GPTW6 | A/D Converter Start Request Timing Buffer Register A | GTADTBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2678h | GPTW6 | A/D Converter Start Request Timing Double-Buffer Register A | GTADTDBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |

Table 4.1 List of I/O Registers (Address Order) (48 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 267Ch | GPTW6 | A/D Converter Start Request Timing Register B | GTADTRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2680h | GPTW6 | A/D Converter Start Request Timing Buffer Register B | GTADTRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2684h | GPTW6 | A/D Converter Start Request Timing Double-Buffer Register B | GTADTDBRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2688h | GPTW6 | General PWM Timer Dead Time Control Register | GTDTCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 268Ch | GPTW6 | General PWM Timer Dead Time Value Register U | GTDVU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2690h | GPTW6 | General PWM Timer Dead Time Value Register D | GTDVD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2694h | GPTW6 | General PWM Timer Dead Time Buffer Register U | GTDBU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2698h | GPTW6 | General PWM Timer Dead Time Buffer Register D | GTDBD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 269Ch | GPTW6 | General PWM Timer Output Protection Function Status Register | GTSOS | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 26A0h | GPTW6 | General PWM Timer Output Protection Function Temporary Release Register | GTSOTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 26A4h | GPTW6 | General PWM Timer A/D Converter Start Request Signal Monitoring Register | GTADSMR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 26A8h | GPTW6 | General PWM Timer Extended Interrupt Skipping Counter Control Register | GTEITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 26ACh | GPTW6 | General PWM Timer Extended Interrupt Skipping Setting Register 1 | GTEITL1 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 26B0h | GPTW6 | General PWM Timer Extended Interrupt Skipping Setting Register 2 | GTEITL2 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 26B4h | GPTW6 | General PWM Timer Extended Buffer Transfer Skipping Setting Register | GTEITLB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 26D0h | GPTW6 | General PWM Timer Operation Enable Bit Simultaneous Control Channel Select Register | GTSECSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 26D4h | GPTW6 | General PWM Timer Operation Enable Bit Simultaneous Control Register | GTSECR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2700h | GPTW7 | General PWM Timer Write-Protection Register | GTWP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2704h | GPTW7 | General PWM Timer Software Start Register | GTSTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2708h | GPTW7 | General PWM Timer Software Stop Register | GTSTP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 270Ch | GPTW7 | General PWM Timer Software Clear Register | GTCLR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2710h | GPTW7 | General PWM Timer Start Source Select Register | GTSSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2714h | GPTW7 | General PWM Timer Stop Source Select Register | GTSPSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2718h | GPTW7 | General PWM Timer Clear Source Select Register | GTCSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 271Ch | GPTW7 | General PWM Timer Count-Up Source Select Register | GTUPSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2720h | GPTW7 | General PWM Timer Count-Down Source Select Register | GTDNSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2724h | GPTW7 | General PWM Timer Input Capture Source Select Register A | GTICASR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2728h | GPTW7 | General PWM Timer Input Capture Source Select Register B | GTICBSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 272Ch | GPTW7 | General PWM Timer Control Register | GTCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2730h | GPTW7 | General PWM Timer Count Direction and Duty Setting Register | GTUDDTYC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2734h | GPTW7 | General PWM Timer I/O Control Register | GTIOR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2738h | GPTW7 | General PWM Timer Interrupt Output Setting Register | GTINTAD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 273Ch | GPTW7 | General PWM Timer Status Register | GTST | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2740h | GPTW7 | General PWM Timer Buffer Enable Register | GTBER | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2744h | GPTW7 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register | GTITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2748h | GPTW7 | General PWM Timer Counter | GTCNT | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 274Ch | GPTW7 | General PWM Timer Compare Capture Register A | GTCCRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2750h | GPTW7 | General PWM Timer Compare Capture Register B | GTCCRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2754h | GPTW7 | General PWM Timer Compare Capture Register C | GTCCRC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2758h | GPTW7 | General PWM Timer Compare Capture Register E | GTCCRE | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 275Ch | GPTW7 | General PWM Timer Compare Capture Register D | GTCCRD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2760h | GPTW7 | General PWM Timer Compare Capture Register F | GTCCRF | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |

Table 4.1 List of I/O Registers (Address Order) (49 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 2764h | GPTW7 | General PWM Timer Period Setting Register | GTPR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2768h | GPTW7 | General PWM Timer Period Setting Buffer Register | GTPBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 276Ch | GPTW7 | General PWM Timer Period Setting Double-Buffer Register | GTPDBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2770h | GPTW7 | A/D Converter Start Request Timing Register A | GTADTRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2774h | GPTW7 | A/D Converter Start Request Timing Buffer Register A | GTADTBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2778h | GPTW7 | A/D Converter Start Request Timing Double-Buffer Register A | GTADTBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 277Ch | GPTW7 | A/D Converter Start Request Timing Register B | GTADTRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2780h | GPTW7 | A/D Converter Start Request Timing Buffer Register B | GTADTRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2784h | GPTW7 | A/D Converter Start Request Timing Double-Buffer Register B | GTADTRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2788h | GPTW7 | General PWM Timer Dead Time Control Register | GTDTCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 278Ch | GPTW7 | General PWM Timer Dead Time Value Register U | GTDVU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2790h | GPTW7 | General PWM Timer Dead Time Value Register D | GTDVD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2794h | GPTW7 | General PWM Timer Dead Time Buffer Register U | GTDBU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2798h | GPTW7 | General PWM Timer Dead Time Buffer Register D | GTDBD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 279Ch | GPTW7 | General PWM Timer Output Protection Function Status Register | GTSOS | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 27A0h | GPTW7 | General PWM Timer Output Protection Function Temporary Release Register | GTSOTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 27A4h | GPTW7 | General PWM Timer A/D Converter Start Request Signal Monitoring Register | GTADSMR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 27A8h | GPTW7 | General PWM Timer Extended Interrupt Skipping Counter Control Register | GTEITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 27ACh | GPTW7 | General PWM Timer Extended Interrupt Skipping Setting Register 1 | GTEITL1 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 27B0h | GPTW7 | General PWM Timer Extended Interrupt Skipping Setting Register 2 | GTEITL2 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 27B4h | GPTW7 | General PWM Timer Extended Buffer Transfer Skipping Setting Register | GTEITLB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 27D0h | GPTW7 | General PWM Timer Operation Enable Bit Simultaneous Control Channel Select Register | GTSECSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 27D4h | GPTW7 | General PWM Timer Operation Enable Bit Simultaneous Control Register | GTSECR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2800h | GPTW8 | General PWM Timer Write-Protection Register | GTWP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2804h | GPTW8 | General PWM Timer Software Start Register | GTSTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2808h | GPTW8 | General PWM Timer Software Stop Register | GTSTP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 280Ch | GPTW8 | General PWM Timer Software Clear Register | GTCLR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2810h | GPTW8 | General PWM Timer Start Source Select Register | GTSSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2814h | GPTW8 | General PWM Timer Stop Source Select Register | GTSPSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2818h | GPTW8 | General PWM Timer Clear Source Select Register | GTCSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 281Ch | GPTW8 | General PWM Timer Count-Up Source Select Register | GTUPSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2820h | GPTW8 | General PWM Timer Count-Down Source Select Register | GTDNSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2824h | GPTW8 | General PWM Timer Input Capture Source Select Register A | GTICASR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2828h | GPTW8 | General PWM Timer Input Capture Source Select Register B | GTICBSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 282Ch | GPTW8 | General PWM Timer Control Register | GTCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2830h | GPTW8 | General PWM Timer Count Direction and Duty Setting Register | GTUDDTYC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2834h | GPTW8 | General PWM Timer I/O Control Register | GTIOR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2838h | GPTW8 | General PWM Timer Interrupt Output Setting Register | GTINTAD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 283Ch | GPTW8 | General PWM Timer Status Register | GTST | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2840h | GPTW8 | General PWM Timer Buffer Enable Register | GTBER | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2844h | GPTW8 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register | GTITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |

Table 4.1 List of I/O Registers (Address Order) (50 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 2848h | GPTW8 | General PWM Timer Counter | GT CNT | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 284Ch | GPTW8 | General PWM Timer Compare Capture Register A | GTCCRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2850h | GPTW8 | General PWM Timer Compare Capture Register B | GTCCRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2854h | GPTW8 | General PWM Timer Compare Capture Register C | GTCCRC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2858h | GPTW8 | General PWM Timer Compare Capture Register E | GTCCRE | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 285Ch | GPTW8 | General PWM Timer Compare Capture Register D | GTCCRD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2860h | GPTW8 | General PWM Timer Compare Capture Register F | GTCCRF | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2864h | GPTW8 | General PWM Timer Period Setting Register | GT PR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2868h | GPTW8 | General PWM Timer Period Setting Buffer Register | GT PBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 286Ch | GPTW8 | General PWM Timer Period Setting Double-Buffer Register | GT PDBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2870h | GPTW8 | A/D Converter Start Request Timing Register A | GTADTRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2874h | GPTW8 | A/D Converter Start Request Timing Buffer Register A | GTADTBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2878h | GPTW8 | A/D Converter Start Request Timing Double-Buffer Register A | GTADTDBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 287Ch | GPTW8 | A/D Converter Start Request Timing Register B | GTADTRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2880h | GPTW8 | A/D Converter Start Request Timing Buffer Register B | GTADTRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2884h | GPTW8 | A/D Converter Start Request Timing Double-Buffer Register B | GTADTDBRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2888h | GPTW8 | General PWM Timer Dead Time Control Register | GT DTCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 288Ch | GPTW8 | General PWM Timer Dead Time Value Register U | GT DVU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2890h | GPTW8 | General PWM Timer Dead Time Value Register D | GT DVD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2894h | GPTW8 | General PWM Timer Dead Time Buffer Register U | GT DBU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2898h | GPTW8 | General PWM Timer Dead Time Buffer Register D | GT DBD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 289Ch | GPTW8 | General PWM Timer Output Protection Function Status Register | GT SOS | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 28A0h | GPTW8 | General PWM Timer Output Protection Function Temporary Release Register | GT SOTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 28A4h | GPTW8 | General PWM Timer A/D Converter Start Request Signal Monitoring Register | GT ADSMR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 28A8h | GPTW8 | General PWM Timer Extended Interrupt Skipping Counter Control Register | GT EITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 28ACh | GPTW8 | General PWM Timer Extended Interrupt Skipping Setting Register 1 | GT EITL1 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 28B0h | GPTW8 | General PWM Timer Extended Interrupt Skipping Setting Register 2 | GT EITL2 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 28B4h | GPTW8 | General PWM Timer Extended Buffer Transfer Skipping Setting Register | GT EITLB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 28D0h | GPTW8 | General PWM Timer Operation Enable Bit Simultaneous Control Channel Select Register | GT SECSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 28D4h | GPTW8 | General PWM Timer Operation Enable Bit Simultaneous Control Register | GT SECR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2900h | GPTW9 | General PWM Timer Write-Protection Register | GT WP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2904h | GPTW9 | General PWM Timer Software Start Register | GT STR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2908h | GPTW9 | General PWM Timer Software Stop Register | GT STP | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 290Ch | GPTW9 | General PWM Timer Software Clear Register | GT CLR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2910h | GPTW9 | General PWM Timer Start Source Select Register | GT SSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2914h | GPTW9 | General PWM Timer Stop Source Select Register | GT PSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2918h | GPTW9 | General PWM Timer Clear Source Select Register | GT CSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 291Ch | GPTW9 | General PWM Timer Count-Up Source Select Register | GT UCSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2920h | GPTW9 | General PWM Timer Count-Down Source Select Register | GT DCSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2924h | GPTW9 | General PWM Timer Input Capture Source Select Register A | GT ICASR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2928h | GPTW9 | General PWM Timer Input Capture Source Select Register B | GT ICBSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 292Ch | GPTW9 | General PWM Timer Control Register | GT CR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |

Table 4.1 List of I/O Registers (Address Order) (51 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 2930h | GPTW9 | General PWM Timer Count Direction and Duty Setting Register | GTUDDTYC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2934h | GPTW9 | General PWM Timer I/O Control Register | GTIOR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2938h | GPTW9 | General PWM Timer Interrupt Output Setting Register | GTINTAD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 293Ch | GPTW9 | General PWM Timer Status Register | GTST | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2940h | GPTW9 | General PWM Timer Buffer Enable Register | GTBER | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2944h | GPTW9 | General PWM Timer Interrupt and A/D Converter Start Request Skipping Setting Register | GTITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2948h | GPTW9 | General PWM Timer Counter | GT CNT | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 294Ch | GPTW9 | General PWM Timer Compare Capture Register A | GTCCRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2950h | GPTW9 | General PWM Timer Compare Capture Register B | GTCCRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2954h | GPTW9 | General PWM Timer Compare Capture Register C | GTCCRC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2958h | GPTW9 | General PWM Timer Compare Capture Register E | GTCCRE | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 295Ch | GPTW9 | General PWM Timer Compare Capture Register D | GTCCRD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2960h | GPTW9 | General PWM Timer Compare Capture Register F | GTCCRF | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2964h | GPTW9 | General PWM Timer Period Setting Register | GT PR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2968h | GPTW9 | General PWM Timer Period Setting Buffer Register | GT PBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 296Ch | GPTW9 | General PWM Timer Period Setting Double-Buffer Register | GT PDBR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2970h | GPTW9 | A/D Converter Start Request Timing Register A | GTADTRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2974h | GPTW9 | A/D Converter Start Request Timing Buffer Register A | GTADTBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2978h | GPTW9 | A/D Converter Start Request Timing Double-Buffer Register A | GTADTDBRA | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 297Ch | GPTW9 | A/D Converter Start Request Timing Register B | GTADTRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2980h | GPTW9 | A/D Converter Start Request Timing Buffer Register B | GTADTBRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2984h | GPTW9 | A/D Converter Start Request Timing Double-Buffer Register B | GTADTDBRB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2988h | GPTW9 | General PWM Timer Dead Time Control Register | GT DTCR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 298Ch | GPTW9 | General PWM Timer Dead Time Value Register U | GT DVU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2990h | GPTW9 | General PWM Timer Dead Time Value Register D | GT DVD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2994h | GPTW9 | General PWM Timer Dead Time Buffer Register U | GT DBU | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2998h | GPTW9 | General PWM Timer Dead Time Buffer Register D | GT DBD | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 299Ch | GPTW9 | General PWM Timer Output Protection Function Status Register | GT SOS | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 29A0h | GPTW9 | General PWM Timer Output Protection Function Temporary Release Register | GT SOTR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 29A4h | GPTW9 | General PWM Timer A/D Converter Start Request Signal Monitoring Register | GT ADSMR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 29A8h | GPTW9 | General PWM Timer Extended Interrupt Skipping Counter Control Register | GT EITC | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 29ACh | GPTW9 | General PWM Timer Extended Interrupt Skipping Setting Register 1 | GT EITLI1 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 29B0h | GPTW9 | General PWM Timer Extended Interrupt Skipping Setting Register 2 | GT EITLI2 | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 29B4h | GPTW9 | General PWM Timer Extended Buffer Transfer Skipping Setting Register | GT EITLB | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 29D0h | GPTW9 | General PWM Timer Operation Enable Bit Simultaneous Control Channel Select Register | GT SECSR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 29D4h | GPTW9 | General PWM Timer Operation Enable Bit Simultaneous Control Register | GT SECR | 32 | 32 | 4, 5 PCLKA | 2, 3 ICLK | GPTW |
| 000C 2A00h | HRPWM | HRPWM Operation Control Register | HT OCR | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | HRPWM |
| 000C 2A02h | HRPWM | HRPWM Operation Control Register 2 | HT OCR2 | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | HRPWM |
| 000C 2A18h | HRPWM | GTIOC0A Pin Rising Edge Adjustment Register | HT REAR0A | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | HRPWM |
| 000C 2A1Ah | HRPWM | GTIOC0B Pin Rising Edge Adjustment Register | HT REAR0B | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | HRPWM |
| 000C 2A1Ch | HRPWM | GTIOC1A Pin Rising Edge Adjustment Register | HT REAR1A | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | HRPWM |
| 000C 2A1Eh | HRPWM | GTIOC1B Pin Rising Edge Adjustment Register | HT REAR1B | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | HRPWM |

Table 4.1 List of I/O Registers (Address Order) (52 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000C 2A20h | HRPWM | GTIOC2A Pin Rising Edge Adjustment Register | HRREAR2A | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | HRPWM |
| 000C 2A22h | HRPWM | GTIOC2B Pin Rising Edge Adjustment Register | HRREAR2B | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | HRPWM |
| 000C 2A24h | HRPWM | GTIOC3A Pin Rising Edge Adjustment Register | HRREAR3A | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | HRPWM |
| 000C 2A26h | HRPWM | GTIOC3B Pin Rising Edge Adjustment Register | HRREAR3B | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | HRPWM |
| 000C 2A28h | HRPWM | GTIOC0A Pin Falling Edge Adjustment Register | HRFEAR0A | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | HRPWM |
| 000C 2A2Ah | HRPWM | GTIOC0B Pin Falling Edge Adjustment Register | HRFEAR0B | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | HRPWM |
| 000C 2A2Ch | HRPWM | GTIOC1A Pin Falling Edge Adjustment Register | HRFEAR1A | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | HRPWM |
| 000C 2A2Eh | HRPWM | GTIOC1B Pin Falling Edge Adjustment Register | HRFEAR1B | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | HRPWM |
| 000C 2A30h | HRPWM | GTIOC2A Pin Falling Edge Adjustment Register | HRFEAR2A | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | HRPWM |
| 000C 2A32h | HRPWM | GTIOC2B Pin Falling Edge Adjustment Register | HRFEAR2B | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | HRPWM |
| 000C 2A34h | HRPWM | GTIOC3A Pin Falling Edge Adjustment Register | HRFEAR3A | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | HRPWM |
| 000C 2A36h | HRPWM | GTIOC3B Pin Falling Edge Adjustment Register | HRFEAR3B | 16 | 16 | 4, 5 PCLKA | 2, 3 ICLK | HRPWM |
| 000D 0000h | SCI11 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0000h | SMCI11 | Serial Mode Register | SMR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0001h | SCI11 | Bit Rate Register | BRR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0002h | SCI11 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0002h | SMCI11 | Serial Control Register | SCR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0003h | SCI11 | Transmit Data Register | TDR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0004h | SCI11 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0004h | SMCI11 | Serial Status Register | SSR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0004h | SCI11 | Serial Status Register | SSRFIFO | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0005h | SCI11 | Receive Data Register | RDR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0006h | SMCI11 | Smart Card Mode Register | SCMR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0007h | SCI11 | Serial Extended Mode Register | SEMR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0008h | SCI11 | Noise Filter Setting Register | SNFR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0009h | SCI11 | I2C Mode Register 1 | SIMR1 | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 000Ah | SCI11 | I2C Mode Register 2 | SIMR2 | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 000Bh | SCI11 | I2C Mode Register 3 | SIMR3 | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 000Ch | SCI11 | I2C Status Register | SISR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 000Dh | SCI11 | SPI Mode Register | SPMR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 000Eh | SCI11 | Transmit Data Register H | TDRH | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 000Fh | SCI11 | Transmit Data Register L | TDRL | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 000Eh | SCI11 | Transmit Data Register HL | TDRHL | 16 | 8, 16 | 2 to 5 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 000Eh | SCI11 | Transmit FIFO Data Register H | FTDR.H | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 000Fh | SCI11 | Transmit FIFO Data Register L | FTDR.L | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 000Eh | SCI11 | Transmit FIFO Data Register | FTDR | 16 | 8, 16 | 2 to 5 PCLKA | 2 ICLK | SCIj, SCli, SClh |

Table 4.1 List of I/O Registers (Address Order) (53 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|---|-----------------|----------------|-------------|-------------------------|-------------|------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000D 0010h | SCI11 | Receive Data Register H | RDRH | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0011h | SCI11 | Receive Data Register L | RDRL | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0010h | SCI11 | Receive Data Register | RDRHL | 16 | 8, 16 | 2 to 5 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0010h | SCI11 | Receive FIFO Data Register H | FRDR.H | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0011h | SCI11 | Receive FIFO Data Register L | FRDR.L | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0010h | SCI11 | Receive FIFO Data Register HL | FRDR | 16 | 8, 16 | 2 to 5 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0012h | SCI11 | Modulation Duty Register | MDDR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0013h | SCI11 | Data Comparison Control Register | DCCR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0014h | SCI11 | FIFO Control Register H | FCR.H | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0015h | SCI11 | FIFO Control Register L | FCR.L | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0014h | SCI11 | FIFO Control Register | FCR | 16 | 8, 16 | 2 to 5 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0016h | SCI11 | FIFO Data Count Register H | FDR.H | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0017h | SCI11 | FIFO Data Count Register L | FDR.L | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0016h | SCI11 | FIFO Data Count Register | FDR | 16 | 8, 16 | 2 to 5 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0018h | SCI11 | Line Status Register H | LSR.H | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0019h | SCI11 | Line Status Register L | LSR.L | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0018h | SCI11 | Line Status Register | LSR | 16 | 8, 16 | 2 to 5 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 001Ah | SCI11 | Comparison Data Register H | CDR.H | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 001Bh | SCI11 | Comparison Data Register L | CDR.L | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 001Ah | SCI11 | Comparison Data Register | CDR | 16 | 8, 16 | 2 to 5 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 001Ch | SCI11 | Serial Port Register | SPTR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | SCIj, SCli, SClh |
| 000D 0100h | RSPI0 | RSPI Control Register | SPCR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | RSPIc |
| 000D 0101h | RSPI0 | RSPI Slave Select Polarity Register | SSLP | 8 | 8 | 2, 3 PCLKA | 2 ICLK | RSPIc |
| 000D 0102h | RSPI0 | RSPI Pin Control Register | SPPCR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | RSPIc |
| 000D 0103h | RSPI0 | RSPI Status Register | SPSR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | RSPIc |
| 000D 0104h | RSPI0 | RSPI Data Register | SPDR | 32 | 8, 16, 32 | 2, 3 PCLKA | 2 ICLK | RSPIc |
| 000D 0108h | RSPI0 | RSPI Sequence Control Register | SPSCR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | RSPIc |
| 000D 0109h | RSPI0 | RSPI Sequence Status Register | SPSSR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | RSPIc |
| 000D 010Ah | RSPI0 | RSPI Bit Rate Register | SPBR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | RSPIc |
| 000D 010Bh | RSPI0 | RSPI Data Control Register | SPDCR | 8 | 8 | 2, 3 PCLKA | 2 ICLK | RSPIc |
| 000D 010Ch | RSPI0 | RSPI Clock Delay Register | SPCKD | 8 | 8 | 2, 3 PCLKA | 2 ICLK | RSPIc |
| 000D 010Dh | RSPI0 | RSPI Slave Select Negation Delay Register | SSLND | 8 | 8 | 2, 3 PCLKA | 2 ICLK | RSPIc |
| 000D 010Eh | RSPI0 | RSPI Next-Access Delay Register | SPND | 8 | 8 | 2, 3 PCLKA | 2 ICLK | RSPIc |
| 000D 010Fh | RSPI0 | RSPI Control Register 2 | SPCR2 | 8 | 8 | 2, 3 PCLKA | 2 ICLK | RSPIc |
| 000D 0110h | RSPI0 | RSPI Command Register 0 | SPCMD0 | 16 | 16 | 2, 3 PCLKA | 2 ICLK | RSPIc |
| 000D 0112h | RSPI0 | RSPI Command Register 1 | SPCMD1 | 16 | 16 | 2, 3 PCLKA | 2 ICLK | RSPIc |
| 000D 0114h | RSPI0 | RSPI Command Register 2 | SPCMD2 | 16 | 16 | 2, 3 PCLKA | 2 ICLK | RSPIc |
| 000D 0116h | RSPI0 | RSPI Command Register 3 | SPCMD3 | 16 | 16 | 2, 3 PCLKA | 2 ICLK | RSPIc |

Table 4.1 List of I/O Registers (Address Order) (54 / 54)

| Address | Module Symbol | Register Name | Register Symbol | Number of Bits | Access Size | Number of Access Cycles | | Related Function |
|------------|---------------|--|-----------------|----------------|-------------|-------------------------|-------------|-----------------------|
| | | | | | | ICLK ≥ PCLK | ICLK < PCLK | |
| 000D 0118h | RSPI0 | RSPI Command Register 4 | SPCMD4 | 16 | 16 | 2, 3 PCLKA | 2 ICLK | RSPIC |
| 000D 011Ah | RSPI0 | RSPI Command Register 5 | SPCMD5 | 16 | 16 | 2, 3 PCLKA | 2 ICLK | RSPIC |
| 000D 011Ch | RSPI0 | RSPI Command Register 6 | SPCMD6 | 16 | 16 | 2, 3 PCLKA | 2 ICLK | RSPIC |
| 000D 011Eh | RSPI0 | RSPI Command Register 7 | SPCMD7 | 16 | 16 | 2, 3 PCLKA | 2 ICLK | RSPIC |
| 000D 0120h | RSPI0 | RSPI Data Control Register 2 | SPDCR2 | 8 | 8 | 2, 3 PCLKA | 2 ICLK | RSPIC |
| 0012 0040h | OFSM | Serial Programmer Command Control Register | SPCC | 32 | 32 | 8 FCLK | | Option-Setting Memory |
| 0012 0048h | OFSM | TM Enable Flag Register | TMEF | 32 | 32 | 8 FCLK | | Option-Setting Memory |
| 0012 0050h | OFSM | OCD/Serial Programmer ID Setting Register | OSIS | 128 | 32 | 8 FCLK | | Option-Setting Memory |
| 0012 0060h | OFSM | TM Identification Data Register | TMINF | 32 | 32 | 8 FCLK | | Option-Setting Memory |
| 0012 0064h | OFSM | Endian Select Register | MDE | 32 | 32 | 8 FCLK | | Option-Setting Memory |
| 0012 0068h | OFSM | Option Function Select Register 0 | OFS0 | 32 | 32 | 8 FCLK | | Option-Setting Memory |
| 0012 006Ch | OFSM | Option Function Select Register 1 | OFS1 | 32 | 32 | 8 FCLK | | Option-Setting Memory |
| 0012 007Ch | OFSM | ROM Code Protection Register | ROMCODE | 32 | 32 | 8 FCLK | | Option-Setting Memory |
| 007F B174h | FLASH | Unique ID Register 0 | UIDR0 | 32 | 32 | 3 to 5 FCLK | 3, 4 ICLK | Flash |
| 007F B17Ch | TEMPS | Temperature Sensor Calibration Data Register | TSCDR | 32 | 32 | 3 to 5 FCLK | 3, 4 ICLK | TEMPS |
| 007F B1E4h | FLASH | Unique ID Register 1 | UIDR1 | 32 | 32 | 3 to 5 FCLK | 3, 4 ICLK | Flash |
| 007F B1E8h | FLASH | Unique ID Register 2 | UIDR2 | 32 | 32 | 3 to 5 FCLK | 3, 4 ICLK | Flash |
| 007F E010h | FLASH | Flash Access Status Register | FASTAT | 8 | 8 | 2 to 4 FCLK | 2, 3 ICLK | Flash |
| 007F E014h | FLASH | Flash Access Error Interrupt Enable Register | FAEINT | 8 | 8 | 2 to 4 FCLK | 2, 3 ICLK | Flash |
| 007F E018h | FLASH | Flash Ready Interrupt Enable Register | FRDYIE | 8 | 8 | 2 to 4 FCLK | 2, 3 ICLK | Flash |
| 007F E030h | FLASH | FACI Command Processing Start Address Register | FSADDR | 32 | 32 | 2 to 4 FCLK | 2, 3 ICLK | Flash |
| 007F E034h | FLASH | FACI Command Processing End Address Register | FEADDR | 32 | 32 | 2 to 4 FCLK | 2, 3 ICLK | Flash |
| 007F E080h | FLASH | Flash Status Register | FSTATR | 32 | 32 | 2 to 4 FCLK | 2, 3 ICLK | Flash |
| 007F E084h | FLASH | Flash P/E Mode Entry Register | FENTRYR | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | Flash |
| 007F E088h | FLASH | Flash Protection Register | FPROTR | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | Flash |
| 007F E08Ch | FLASH | Flash Sequencer Set-Up Initialization Register | FSUINITR | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | Flash |
| 007F E090h | FLASH | Lock Bit Status Register | FLKSTAT | 8 | 8 | 2 to 4 FCLK | 2, 3 ICLK | Flash |
| 007F E0A0h | FLASH | FACI Command Register | FCMDR | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | Flash |
| 007F E0C0h | FLASH | Flash P/E Status Register | FPESTAT | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | Flash |
| 007F E0D0h | FLASH | Data Flash Blank Check Control Register | FBCCNT | 8 | 8 | 2 to 4 FCLK | 2, 3 ICLK | Flash |
| 007F E0D4h | FLASH | Data Flash Blank Check Status Register | FBCSTAT | 8 | 8 | 2 to 4 FCLK | 2, 3 ICLK | Flash |
| 007F E0D8h | FLASH | Data Flash Programming Start Address Register | FPSADDR | 32 | 32 | 2 to 4 FCLK | 2, 3 ICLK | Flash |
| 007F E0E0h | FLASH | Flash Sequencer Processing Switching Register | FCPSR | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | Flash |
| 007F E0E4h | FLASH | Flash Sequencer Processing Clock Frequency Notification Register | FPCKAR | 16 | 16 | 2 to 4 FCLK | 2, 3 ICLK | Flash |

Note 1. When the register is accessed while the USB is operating, a delay may be generated in accessing.

Note 2. The address must end with 0h, 4h, 8h, or Ch when access is made in 32-bit units. The address must end with 0h, 2h, 4h, 6h, 8h, Ah, Ch, or Eh when access is made in 16-bit units.

5. Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Rating

Conditions: $V_{SS} = V_{SS_USB} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0V$

| Item | | Symbol | Value | Unit |
|-------------------------------|---|----------------------------------|--------------|-----------------------------------|
| Power supply voltage*1 | | VCC | -0.3 to +6.5 | V |
| USB power supply voltage*1 | | VCC_USB | -0.3 to +6.5 | |
| Analog power supply voltage*1 | | AVCC0, AVCC1, AVCC2 | -0.3 to +6.5 | |
| Input voltage | PB1, PB2, PC0*2, and PD2*2 | | V_{in} | -0.3 to +6.5 |
| | P40 to P42, P44 to P46, PH0, and PH4 | With negative input enabled*3 | V_{in} | -1.0 to AVCC1 + 0.3 (up to 6.5) |
| | | With negative input disabled | | -0.3 to AVCC1 + 0.3 (up to 6.5) |
| | P43, P47, PH1 to PH3, and PH5 to PH7 | | | -0.3 to AVCC1 + 0.3 (up to 6.5) |
| | P50 to P55, and P60 to P65 | | | -0.3 to AVCC2 + 0.3 (up to 6.5) |
| | USB0_DP, USB0_DM | | | -0.3 to VCC_USB + 0.3 (up to 6.5) |
| | Other than above | | | -0.3 to VCC + 0.3 (up to 6.5) |
| Junction temperature | D version | T_j | | -40 to +105 |
| | G version | | -40 to +125 | |
| Storage temperature | | T_{stg} | -55 to +125 | |

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

Note 1. Insert capacitors with good frequency characteristics between each power supply pin and the ground. Specifically, place capacitors with a value around 0.1 μF as close as possible to every power supply pin, and use the shortest and thickest possible traces.

Note 2. This is only available for products with 128 Kbytes of RAM.

Note 3. When VOLS.R.PGAVLS = 0 and ADPGADCR0.PxDEN = 1 (x = 000, 001, 002, 100, 101, 102).

5.2 Recommended operating conditions

Table 5.2 Recommended operating conditions (1)

| Item | | Symbol | Min. | Typ. | Max. | Unit | |
|-------------------------------|--------------------------------------|-------------------------------|-----------------|------------------|------|---------------|--|
| Power supply voltage | | VCC*1 | 2.7 | — | 5.5 | V | |
| | | VSS | — | 0 | — | | |
| USB power supply voltage*2 | When USB in use | VCC_USB*1 | 3.0 | — | 3.6 | | |
| | | VSS_USB | — | 0 | — | | |
| | When USB not in use | VCC_USB | — | VCC | — | | |
| | | VSS_USB | — | VSS | — | | |
| Analog power supply voltage*3 | | AVCC0, AVCC1, AVCC2*1 | 3.0 | — | 5.5 | | |
| | | AVSS0, AVSS1, AVSS2 | — | 0 | — | | |
| Input voltage | PB1, PB2, PC0*4, and PD2*4 | | V _{in} | -0.3 | — | 5.8 | |
| | P40 to P42, and P44 to P46 | With negative input enabled*5 | | -1.0 | — | AVCC1 + 0.3 | |
| | | With negative input disabled | | -0.3 | — | | |
| | PH0, PH4 | With negative input enabled*5 | | -0.5 | — | AVCC1 + 0.3 | |
| | | With negative input disabled | | -0.3 | — | | |
| | P43, P47, PH1 to PH3, and PH5 to PH7 | | | -0.3 | — | AVCC1 + 0.3 | |
| | P50 to P55, and P60 to P65 | | | -0.3 | — | AVCC2 + 0.3 | |
| | USB0_DP, USB0_DM | | | -0.3 | — | VCC_USB + 0.3 | |
| | Other than above | | | -0.3 | — | VCC + 0.3 | |
| | Operating temperature | D version | | T _{opr} | -40 | — | |
| G version | | -40 | — | | 105 | | |

Note 1. Comply with the following voltage condition: $VCC_USB \leq VCC \leq AVCC0 = AVCC1 = AVCC2$

Note 2. When the USB interface is not to be used, connect VCC_USB to VCC and VSS_USB to VSS, and set VOLSR.USBVON=0.

Note 3. When not using any of the 12-bit A/D converter (unit 0 to 2), 12-bit D/A converter, comparator C, or temperature sensor, connect AVCC0, AVCC1, and AVCC2 to VCC, and AVSS0, AVSS1, and AVSS2 to VSS, respectively. For details, refer to section 38.6.10, Voltage Range of Analog Power Supply Pins in the User's Manual: Hardware.

Note 4. This is only available for products with 128 Kbytes of RAM.

Note 5. When VOLSR.PGAVLS = 0 and ADPGADCR0.PxDEN = 1 (x = 000, 001, 002, 100, 101, 102).

Table 5.3 Recommended operating conditions (2)

| Item | Symbol | Value |
|--|------------------|-----------------|
| Decoupling capacitance to stabilize the internal voltage | C _{VCL} | 0.47 μF ± 30%*1 |

Note 1. Use a multilayer ceramic capacitor whose nominal capacitance is 0.47 μF and a capacitance tolerance is ±30% or better.

5.3 DC Characteristics

Table 5.4 DC Characteristics (1)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
 $T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|--|--------------------|---------------------|--------------------|--------------------|------|-----------------|
| Schmitt trigger input voltage | CAN input pin | V_{IH} | $0.8 \times VCC$ | — | — | V | |
| | MTU input pin | V_{IL} | — | — | $0.2 \times VCC$ | | |
| | GPTW input pin | ΔV_T | $0.06 \times VCC$ | — | — | | |
| | POE input pin | | | | | | |
| | POEG input pin | | | | | | |
| | TMR input pin | | | | | | |
| | SCI input pin | | | | | | |
| | ADTRG# input pin | | | | | | |
| | RES#, NMI | | | | | | |
| | IRQ input pin (except for P52 to P55, and P60 to P65) | V_{IH} | $0.8 \times VCC$ | — | — | | |
| | | V_{IL} | — | — | $0.2 \times VCC$ | | |
| | | ΔV_T | $0.06 \times VCC$ | — | — | | |
| | IRQ input pin (P52 to P55, and P60 to P65) | V_{IH} | $0.8 \times AVCC2$ | — | — | | |
| | | V_{IL} | — | — | $0.2 \times AVCC2$ | | |
| | | ΔV_T | $0.06 \times AVCC2$ | — | — | | |
| | RIIC input pin (except for SMBus) | V_{IH} | $0.7 \times VCC$ | — | — | | |
| | | V_{IL} | — | — | $0.3 \times VCC$ | | |
| | | ΔV_T | $0.06 \times VCC$ | — | — | | |
| | Pins for 5 V tolerant (PB1, PB2, PC0*1, and PD2*1) | V_{IH} | $0.8 \times VCC$ | — | — | | |
| | | V_{IL} | — | — | $0.2 \times VCC$ | | |
| Analog input pins (P40 to P47, and PH0 to PH7) | V_{IH} | $0.8 \times AVCC1$ | — | — | | | |
| | V_{IL} | — | — | $0.2 \times AVCC1$ | | | |
| Analog input pins (P50 to P55, and P60 to P65) | V_{IH} | $0.8 \times AVCC2$ | — | — | | | |
| | V_{IL} | — | — | $0.2 \times AVCC2$ | | | |
| Other input pins (pins other than those above) | V_{IH} | $0.8 \times VCC$ | — | — | | | |
| | V_{IL} | — | — | $0.2 \times VCC$ | | | |
| High-level input voltage (except for Schmitt trigger input pin) | MD pin, EMLE | V_{IH} | $0.9 \times VCC$ | — | — | V | |
| | EXTAL, WAIT#, RSPI input pin | | $0.8 \times VCC$ | — | — | | |
| | D0 to D15 | | $0.7 \times VCC$ | — | — | | |
| | RIIC (SMBus) | | 2.1 | — | — | | |
| Low-level input voltage (except for Schmitt trigger input pin) | MD pin, EMLE | V_{IL} | — | — | $0.1 \times VCC$ | V | |
| | EXTAL, WAIT#, RSPI input pin | | — | — | $0.2 \times VCC$ | | |
| | D0 to D15 | | — | — | $0.3 \times VCC$ | | |
| | RIIC (SMBus) | | — | — | 0.8 | | |

Note 1. This is only available for products with 128 Kbytes of RAM.

Table 5.5 DC Characteristics (2)

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V,
 $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|--|----------------|------|------|---------|--|
| High-level output voltage | P43, P47, PH1 to PH3, and PH5 to PH7 | $AVCC1 - 0.5$ | — | — | V | $I_{OH} = -1.0$ mA |
| | P50 to P55, and P60 to P65 | $AVCC2 - 0.5$ | — | — | | $I_{OH} = -1.0$ mA |
| | P90 to P95, P71 to P76, P81, PB5, and PD3 | $V_{CC} - 1.0$ | — | — | | $I_{OH} = -5.0$ mA (when the large current output is set) |
| | Other than above | $V_{CC} - 0.5$ | — | — | | $I_{OH} = -1.0$ mA |
| Low-level output voltage | P43, P47, PH1 to PH3, and PH5 to PH7 | — | — | 0.5 | | $I_{OL} = 1.0$ mA |
| | P50 to P55, and P60 to P65 | — | — | 0.5 | | $I_{OL} = 1.0$ mA |
| | P90 to P95, P71 to P76, P81, PB5, and PD3 | — | — | 1.0 | | $I_{OL} = 15$ mA (when the large current output is set) |
| | RIIC pins | — | — | 0.4 | | $I_{OL} = 3.0$ mA |
| | | — | — | 0.6 | | $I_{OL} = 6.0$ mA |
| | Other than above | — | — | 0.5 | | $I_{OL} = 1.0$ mA |
| Input leakage current | RES#, MD pin, PE2, and EMLE*1 | — | — | 1.0 | μ A | $V_{in} = 0$ V $V_{in} = V_{CC}$ |
| | P40 to P42, and P44 to P46 | — | — | 1.0 | | $V_{in} = 0$ V $V_{in} = AVCC1$ |
| | PH0 and PH4 | — | — | 1.0 | | $V_{in} = 0$ V $V_{in} = AVCC1$ VOLSR.PGAVLS = 1 |
| Three-state leakage current (off state) | RIIC pins | — | — | 5.0 | | $V_{in} = 0$ V $V_{in} = V_{CC}$ |
| | Other than above | — | — | 1.0 | | |
| Input pull-up resistors current | P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65 | -300 | — | -10 | | $AVCC1 = AVCC2 = 3.0$ to 5.5 V $V_{in} = 0$ V |
| | Pins other than those above and PE2 | -300 | — | -10 | | $V_{CC} = 2.7$ to 5.5 V $V_{in} = 0$ V |
| Input pull-down resistors current | EMLE | 10 | — | 300 | | $V_{in} = V_{CC} = AVCC$ |
| Input capacitance | RIIC pins, PH0, and PH4 | — | — | 16 | pF | $V_{bias} = 0$ V $V_{amp} = 20$ mV $f = 1$ MHz $T_a = 25^\circ$ C |
| | USB0_DP, and USB0_DM pins | — | — | 16 | | |
| | Other than above | — | — | 8 | | |
| Output voltage of the VCL pin | V_{CL} | — | 1.25 | — | V | |

Note 1. The input leakage current value at the EMLE pin is only when $V_{in} = 0$ V.

Table 5.6 DC Characteristics (3) (Products with 64 Kbytes of RAM, D version)

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V,
 $T_a = T_{opr}$

| Item | Symbol | D version | | | Unit | Test Conditions | | | | |
|------------------|---------------|----------------------------|---|---|------|-----------------|--|------------------|-----|----|
| | | Min. | Typ. | Max. | | | | | | |
| Supply current*1 | I_{CC}^{*3} | Normal operating mode | Full operation*2 | | 75 | mA | ICLK = 160 MHz PCLKA = 80 MHz PCLKB = 40 MHz PCLKC = 160 MHz PCLKD = 40 MHz FCLK = 40 MHz BCLK = 40 MHz BCLK pin = 40 MHz | | | |
| | | | Normal operation | Peripheral module clocks are supplied*4 | | | | — | 21 | — |
| | | | | Peripheral module clocks are stopped*4, *5 | | | | — | 12 | — |
| | | | CoreMark | Peripheral module clocks are stopped*4, *5 | | | | — | 21 | — |
| | | | | Sleep mode: Peripheral module clocks are supplied*4 | | | | — | 18 | 37 |
| | | | All module clock stop mode (reference value) | | — | | | 9.4 | 23 | |
| | | | Increase current by BGO operation*6 | | — | | | 13 | — | |
| | | | Increase current by operating Trusted Secure IP | | — | | | 3.9 | 5.0 | |
| | | | Software standby mode | | — | | | 0.9 | 7.0 | |
| | | Deep software standby mode | | — | 14 | 20 | μ A | VOLSR.PGAVLS = 1 | | |

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.

Note 2. Peripheral module clocks are supplied. This does not include operations as BGO (background operations).

Note 3. I_{CC} depends on f (ICLK) as follows.

(when ICLK : PCLKA : PCLKB : PCLKC : PCLKD : BCLK : BCLK pin = 4 : 2 : 1 : 4 : 1 : 1 : 1 and EXTAL = 16 MHz)

• D version product

I_{CC} Max. = $0.375 \times f + 15$ (full operation in high-speed operating mode)

I_{CC} Typ. = $0.099 \times f + 5$ (normal operation in high-speed operating mode)

I_{CC} Max. = $0.135 \times f + 15$ (sleep mode)

Note 4. This does not include operations as BGO (background operations). Whether the peripheral module clocks are supplied or stopped is controlled only by the bit settings in the module stop control registers A to D.

Note 5. When peripheral module clocks are stopped, each clock frequency is set for division by 64, and the frequencies of FCLK, BCLK, PCLKA, PCLKB, PCLKC, PCLKD, and the BCLK pin are the same.

Note 6. This is an increase caused by program/erase operation to the code flash memory or data flash memory during executing the user program.

Table 5.7 DC Characteristics (3) (Products with 64 Kbytes of RAM, G version)

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V,
 $T_a = T_{opr}$

| Supply current*1 | Item | | Symbol | G version | | | Unit | Test Conditions |
|-----------------------|---|--|---------------|-----------|------|------|------------------|--|
| | | | | Min. | Typ. | Max. | | |
| Normal operating mode | Full operation*2 | | I_{CC}^{*3} | — | — | 82 | mA | ICLK = 160 MHz PCLKA = 80 MHz PCLKB = 40 MHz PCLKC = 160 MHz PCLKD = 40 MHz FCLK = 40 MHz BCLK = 40 MHz BCLK pin = 40 MHz |
| | Normal operation | Peripheral module clocks are supplied*4 | | — | 21 | — | | |
| | | Peripheral module clocks are stopped*4, *5 | | — | 12 | — | | |
| | CoreMark | Peripheral module clocks are stopped*4, *5 | | — | 21 | — | | |
| | Sleep mode: Peripheral module clocks are supplied*4 | | | — | 18 | 42 | | |
| | All module clock stop mode (reference value) | | | — | 9.4 | 28 | | |
| | Increase current by BGO operation*6 | | | — | 13 | — | | |
| | Increase current by operating Trusted Secure IP | | | — | 3.9 | 5.0 | | |
| | Software standby mode | | | — | 0.9 | 11.2 | | |
| | Deep software standby mode | | | — | 14 | 26 | VOLSR.PGAVLS = 1 | |

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.

Note 2. Peripheral module clocks are supplied. This does not include operations as BGO (background operations).

Note 3. I_{CC} depends on f (ICLK) as follows.

(when ICLK : PCLKA : PCLKB : PCLKC : PCLKD : BCLK : BCLK pin = 4 : 2 : 1 : 4 : 1 : 1 : 1 and EXTAL = 16 MHz)

• G version product

I_{CC} Max. = $0.394 \times f + 19$ (full operation in high-speed operating mode)

I_{CC} Typ. = $0.099 \times f + 5$ (normal operation in high-speed operating mode)

I_{CC} Max. = $0.144 \times f + 19$ (sleep mode)

Note 4. This does not include operations as BGO (background operations). Whether the peripheral module clocks are supplied or stopped is controlled only by the bit settings in the module stop control registers A to D.

Note 5. When peripheral module clocks are stopped, each clock frequency is set for division by 64, and the frequencies of FCLK, BCLK, PCLKA, PCLKB, PCLKC, PCLKD, and the BCLK pin are the same.

Note 6. This is an increase caused by program/erase operation to the code flash memory or data flash memory during executing the user program.

Table 5.8 DC Characteristics (3) (Products with 128 Kbytes of RAM, D version)

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V,
 $T_a = T_{opr}$

| Supply current*1 | Item | | Symbol | D version | | | Unit | Test Conditions |
|-----------------------|---|--|---------------|-----------|------|------|------------------------|--|
| | | | | Min. | Typ. | Max. | | |
| Normal operating mode | Full operation*2 | | I_{CC}^{*3} | — | — | 96 | mA | ICLK = 160 MHz PCLKA = 80 MHz PCLKB = 40 MHz PCLKC = 160 MHz PCLKD = 40 MHz FCLK = 40 MHz BCLK = 40 MHz BCLK pin = 40 MHz |
| | Normal operation | Peripheral module clocks are supplied*4 | | — | 23 | — | | |
| | | Peripheral module clocks are stopped*4, *5 | | — | 14 | — | | |
| | CoreMark | Peripheral module clocks are stopped*4, *5 | | — | 23 | — | | |
| | Sleep mode: Peripheral module clocks are supplied*4 | | | — | 20 | 45 | | |
| | All module clock stop mode (reference value) | | | — | 9.8 | 33 | | |
| | Increase current by BGO operation*6 | | | — | 14 | — | | |
| | Increase current by operating Trusted Secure IP | | | — | 3.9 | 5.3 | | |
| | Software standby mode | | | — | 0.9 | 13.9 | | |
| | Deep software standby mode | | | — | 15 | 21 | μA VOLSR.PGAVLS = 1 | |

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.

Note 2. Peripheral module clocks are supplied. This does not include operations as BGO (background operations).

Note 3. I_{CC} depends on f (ICLK) as follows.

(when ICLK : PCLKA : PCLKB : PCLKC : PCLKD : BCLK : BCLK pin = 4 : 2 : 1 : 4 : 1 : 1 : 1 and EXTAL = 16 MHz)

• D version product

I_{CC} Max. = $0.469 \times f + 21$ (full operation in high-speed operating mode)

I_{CC} Typ. = $0.112 \times f + 5$ (normal operation in high-speed operating mode)

I_{CC} Max. = $0.15 \times f + 21$ (sleep mode)

Note 4. This does not include operations as BGO (background operations). Whether the peripheral module clocks are supplied or stopped is controlled only by the bit settings in the module stop control registers A to D.

Note 5. When peripheral module clocks are stopped, each clock frequency is set for division by 64, and the frequencies of FCLK, BCLK, PCLKA, PCLKB, PCLKC, PCLKD, and the BCLK pin are the same.

Note 6. This is an increase caused by program/erase operation to the code flash memory or data flash memory during executing the user program.

Table 5.9 DC Characteristics (3) (Products with 128 Kbytes of RAM, G version)

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V,
 $T_a = T_{opr}$

| Supply current*1 | Item | | Symbol | G version | | | Unit | Test Conditions |
|-----------------------|---|--|---------------|-----------|------|------|------------------------|--|
| | | | | Min. | Typ. | Max. | | |
| Normal operating mode | Full operation*2 | | I_{CC}^{*3} | — | — | 109 | mA | ICLK = 160 MHz PCLKA = 80 MHz PCLKB = 40 MHz PCLKC = 160 MHz PCLKD = 40 MHz FCLK = 40 MHz BCLK = 40 MHz BCLK pin = 40 MHz |
| | Normal operation | Peripheral module clocks are supplied*4 | | — | 23 | — | | |
| | | Peripheral module clocks are stopped*4, *5 | | — | 14 | — | | |
| | CoreMark | Peripheral module clocks are stopped*4, *5 | | — | 23 | — | | |
| | Sleep mode: Peripheral module clocks are supplied*4 | | | — | 20 | 57 | | |
| | All module clock stop mode (reference value) | | | — | 9.8 | 45 | | |
| | Increase current by BGO operation*6 | | | — | 14 | — | | |
| | Increase current by operating Trusted Secure IP | | | — | 3.9 | 5.3 | | |
| | Software standby mode | | | — | 0.9 | 22.1 | | |
| | Deep software standby mode | | | — | 15 | 28 | μA VOLSR.PGAVLS = 1 | |

Note 1. Supply current values are measured when all output pins are unloaded and all input pull-up resistors are disabled.

Note 2. Peripheral module clocks are supplied. This does not include operations as BGO (background operations).

Note 3. I_{CC} depends on f (ICLK) as follows.

(when ICLK : PCLKA : PCLKB : PCLKC : PCLKD : BCLK : BCLK pin = 4 : 2 : 1 : 4 : 1 : 1 : 1 and EXTAL = 16 MHz)

• G version product

I_{CC} Max. = $0.50 \times f + 29$ (full operation in high-speed operating mode)

I_{CC} Typ. = $0.112 \times f + 5$ (normal operation in high-speed operating mode)

I_{CC} Max. = $0.175 \times f + 29$ (sleep mode)

Note 4. This does not include operations as BGO (background operations). Whether the peripheral module clocks are supplied or stopped is controlled only by the bit settings in the module stop control registers A to D.

Note 5. When peripheral module clocks are stopped, each clock frequency is set for division by 64, and the frequencies of FCLK, BCLK, PCLKA, PCLKB, PCLKC, PCLKD, and the BCLK pin are the same.

Note 6. This is an increase caused by program/erase operation to the code flash memory or data flash memory during executing the user program.

Table 5.10 DC Characteristics (4)

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V,
 $T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|-----------------------------|--|---|---------------|------|------|--------------------------------|---|
| Analog power supply current | Unit 0 | During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: operation for all channels; PGA: enabled for all channels) | — | 2.9 | 5.1 | mA | IAVCC0_AD + SH + PGA |
| | | During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: operation for all channels; PGA: disabled for all channels) | — | 1.9 | 2.9 | | IAVCC0_AD + SH |
| | | During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: stopping of all channels; PGA: enabled for all channels) | — | 2.0 | 4.0 | | IAVCC0_AD + PGA |
| | | During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: stopping of all channels; PGA: disabled for all channels) | — | 1.0 | 1.5 | | IAVCC0_AD |
| | Unit 1 | During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: operation for all channels; PGA: enabled for all channels) | — | 2.9 | 5.1 | mA | IAVCC1_AD + SH + PGA |
| | | During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: operation for all channels; PGA: disabled for all channels) | — | 1.9 | 2.9 | | IAVCC1_AD + SH |
| | | During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: stopping of all channels; PGA: enabled for all channels) | — | 2.0 | 4.0 | | IAVCC1_AD + PGA |
| | | During 12-bit A/D conversion (Channel-dedicated sample-and-hold circuits: stopping of all channels; PGA: disabled for all channels) | — | 1.0 | 1.5 | | IAVCC1_AD |
| | Unit 2 | During 12-bit A/D conversion with the temperature sensor operating | — | 0.9 | 1.5 | mA | IAVCC2_AD + TEMP |
| | | During 12-bit A/D conversion with the temperature sensor stopped | — | 0.9 | 1.5 | | IAVCC2_AD |
| | Comparator (6 channels) | | — | 0.5 | 0.6 | mA | IAVCC2_CMP |
| | During 12-bit D/A conversion (2 channels) | | — | 0.6 | 0.8 | | IAVCC2_DA |
| | Waiting for 12-bit A/D, 12-bit D/A, Comparator C, and temperature sensor conversion (all units) | | — | 0.1 | 0.4 | | IAVCC0_AD + IAVCC1_AD + IAVCC2_AD + IAVCC2_DA |
| | 12-bit A/D, 12-bit D/A, Comparator C, and temperature sensor are in module stop status (all units) | | — | 0.2 | 14.8 | | μA |
| | USB operating current | Low speed | $I_{CCUSBLS}$ | — | 3.6 | 6.5 | mA |
| Full speed | | $I_{CCUSBFS}$ | — | 4.1 | 10 | $V_{CC_USB} = 3.0$ to 3.6 V | |
| RAM retention voltage | | V_{RAM} | 2.7 | — | — | V | |

Table 5.11 DC Characteristics (5)

Conditions: $VCC = 2.7$ to 5.5 V, $VCC_USB = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0$ V,
 $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|------------------------------------|---|-------|------|------|------|--|
| VCC ramp rate at power-on | At normal startup | SrVCC | 0.02 | — | 8 | ms/V |
| | Voltage monitoring 0 reset enabled at startup*1, *2 | | 0.02 | — | 20 | |
| VCC ramp rate at power fluctuation | dt/dVCC | 1.0 | — | — | | When VCC change exceeds $VCC \pm 10\%$ |

Note 1. When OFS1.LVDAS = 0.

Note 2. Settings of the OFS1 register are not read in boot mode or user boot mode, so turn on the power supply voltage with a ramp rate at normal startup.

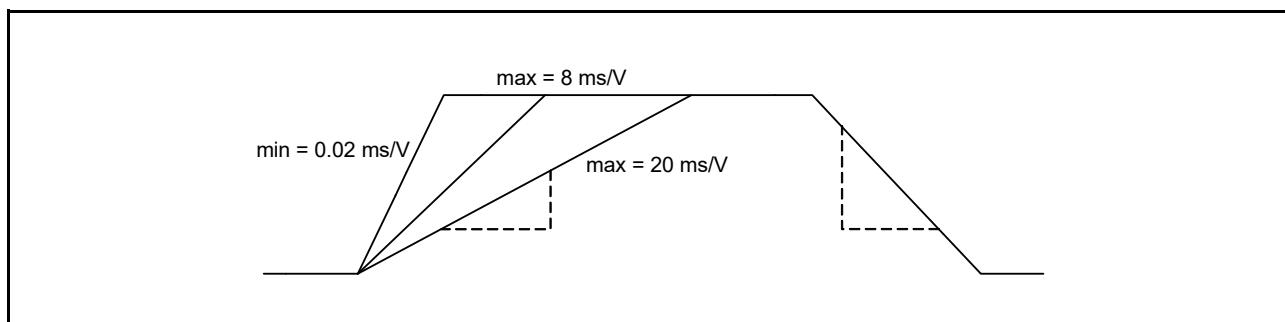


Figure 5.1 VCC Ramp Rate at Power-On

Table 5.12 Permissible Output Currents

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V,
 $T_a = T_{opr}$

| Item | | Symbol | Min. | Typ. | Max. | Unit |
|---|--|---|-----------------|------|----------------|------|
| Permissible low-level output current (average value per pin) | All output pins (except for RIIC pins, P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65) | Normal drive*1 | — | — | 2.0 | mA |
| | | High drive*2 | | | 2.0 | |
| | | Large current output*3 | | | 15.0 | |
| | RIIC pins | Standard mode | | | 3 | |
| | | Fast mode | | | 6 | |
| | P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65 | | | | 2.0 | |
| Permissible low-level output current (max. value per pin) | All output pins (except for RIIC pins, P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65) | Normal drive*1 | — | — | 4.0 | |
| | | High drive*2 | — | — | 4.0 | |
| | | Large current output*3 | — | — | 15.0 | |
| | RIIC pins | Standard mode | — | — | 3 | |
| | | Fast mode | — | — | 6 | |
| | P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65 | | — | — | 4.0 | |
| Permissible low-level output current (total) | Total of all output pins | ΣI_{OL} | — | — | 110 | |
| Permissible high-level output current (average value per pin) | All output pins (except for P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65) | Normal drive*1 | — | — | -2.0 | |
| | | High drive*2 | | | -2.0 | |
| | | Large current output*3 | | | -5.0 | |
| | P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65 | | | | -2.0 | |
| | | | | | | |
| | Permissible high-level output current (max. value per pin) | All output pins (except for P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65) | | | Normal drive*1 | |
| High drive*2 | | | — | — | -4.0 | |
| Large current output*3 | | | — | — | -5.0 | |
| P43, P47, PH1 to PH3, PH5 to PH7, P50 to P55, and P60 to P65 | | | — | — | -4.0 | |
| | | | | | | |
| Permissible high-level output current (total) | | Total of all output pins | ΣI_{OH} | — | — | -35 |

Caution: To protect the LSI's reliability, the output current values should not exceed the values in this table.

Note 1. This is the value when normal driving ability is set with a pin for which normal driving ability is selectable.

Note 2. This is the value when high driving ability is set with a pin for which normal driving ability is selectable or the value of the pin to which high driving ability is fixed.

Note 3. This is the value when large current output is set with a pin for which large current output ability is selectable.

Table 5.13 Thermal Resistance Value (Reference)Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AV_{CC0} = AV_{CC1} = AV_{CC2} = 3.0$ to 5.5 V, $V_{SS} = V_{SS_USB} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0$ V, $T_a = T_{opr}$

| Item | Package | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|--------------------|------------------------------|---------------|------|------|------|------|------------------------------------|
| Thermal resistance | 144-pin LFQFP (PLQP0144KA-B) | θ_{ja} | — | — | 32.4 | °C/W | JESD51-2 and JESD51-7 compliant |
| | 112-pin LQFP (PLQP0112JA-B) | | — | — | 33.8 | | |
| | 100-pin LFQFP (PLQP0100KB-B) | | — | — | 35.0 | | |
| | 80-pin LFQFP (PLQP0080KB-B) | | — | — | 36.3 | | |
| | 80-pin LQFP (PLQP0080JA-A) | | — | — | 35.7 | | |
| | 64-pin LFQFP (PLQP0064KB-C) | | — | — | 37.9 | | |
| | 144-pin LFQFP (PLQP0144KA-B) | Ψ_{jt} | — | — | 0.6 | | |
| | 112-pin LQFP (PLQP0112JA-B) | | — | — | 0.6 | | |
| | 100-pin LFQFP (PLQP0100KB-B) | | — | — | 0.8 | | |
| | 80-pin LFQFP (PLQP0080KB-B) | | — | — | 0.8 | | |
| | 80-pin LQFP (PLQP0080JA-A) | | — | — | 0.8 | | |
| | 64-pin LFQFP (PLQP0064KB-C) | | — | — | 0.8 | | |

Note: The values are reference values when the 4-layer printed circuit board is used. Thermal resistance depends on the number of layers and size of the board. For details, refer to the JEDEC standards.

5.4 AC Characteristics

Table 5.14 Operating Frequency

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
 VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
 $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max.*3 | Unit | Test Conditions |
|---------------------------------|--------|------|------|--------|------|---|
| System clock (ICLK) | f | — | — | 160 | MHz | |
| Peripheral module clock (PCLKA) | | — | — | 120 | | |
| Peripheral module clock (PCLKB) | | — | — | 60 | | |
| Peripheral module clock (PCLKC) | | — | — | 160 | | |
| Peripheral module clock (PCLKD) | | 8*1 | — | 60 | | AVCC0 = AVCC1 = AVCC2 ≥ 4.5 V |
| | | 8*1 | — | 40 | | AVCC0 = AVCC1 = AVCC2 < 4.5 V |
| Flash-IF clock (FCLK) | | 4*2 | — | 60 | | |
| External bus clock (BCLK) | | — | — | 60 | | |
| BCLK pin output | | — | — | 40 | | VCC ≥ 4.5 V, High-drive output is selected in the driving ability control register. |
| | | — | — | 32 | | |
| USB clock (UCLK) | — | 48 | — | | | |

Note 1. This restriction is only applied when a 12-bit A/D converter is to be used.

Note 2. This restriction is only applied when flash memory is to be programmed or erased.

Note 3. The maximum frequencies of each clock based on the frequency of ICLK are listed below.

ICLK = 160 MHz, PCLKA = 80 MHz, PCLKB = 40 MHz, PCLKC = 160 MHz, PCLKD = 40 MHz, FCLK = 40 MHz, BCLK = 40 MHz, BCLK pin output = 40 MHz

ICLK = 120 MHz, PCLKA = 120 MHz, PCLKB = 60 MHz, PCLKC = 120 MHz, PCLKD = 60 MHz, FCLK = 60 MHz,

BCLK = 60 MHz, BCLK pin output = 30 MHz

5.4.1 Reset Timing

Table 5.15 Reset Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
 VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
 T_a = T_{opr}

| Item | | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|--|---|--------------------|------|------|------|-------------------|-----------------|
| RES# pulse width | Power-on | t _{RESWP} | 2.0 | — | — | ms | Figure 5.2 |
| | Deep software standby mode | t _{RESWD} | 0.6 | — | — | | Figure 5.3 |
| | Software standby mode | t _{RESWS} | 0.3 | — | — | | |
| | Programming or erasure of the code flash memory, or programming, erasure or blank checking of the data flash memory | t _{RESWF} | 200 | — | — | μs | |
| | Other than above | t _{RESW} | 200 | — | — | | |
| Waiting time after release from the RES# pin reset | | t _{RESWT} | 62 | — | 63 | t _{Lcyc} | Figure 5.2 |
| Internal reset time (independent watchdog timer reset, watchdog timer reset, software reset) | | t _{RESW2} | 108 | — | 116 | | |

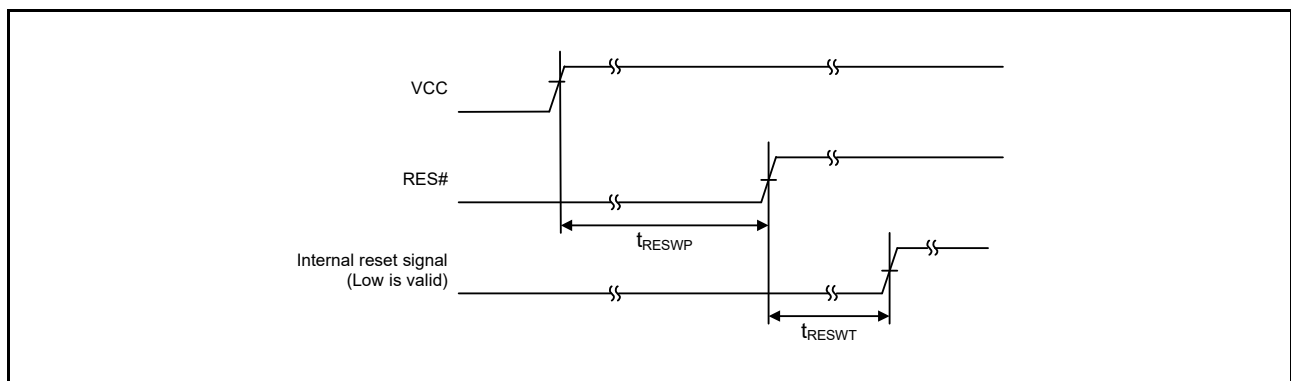


Figure 5.2 Reset Input Timing at Power-On

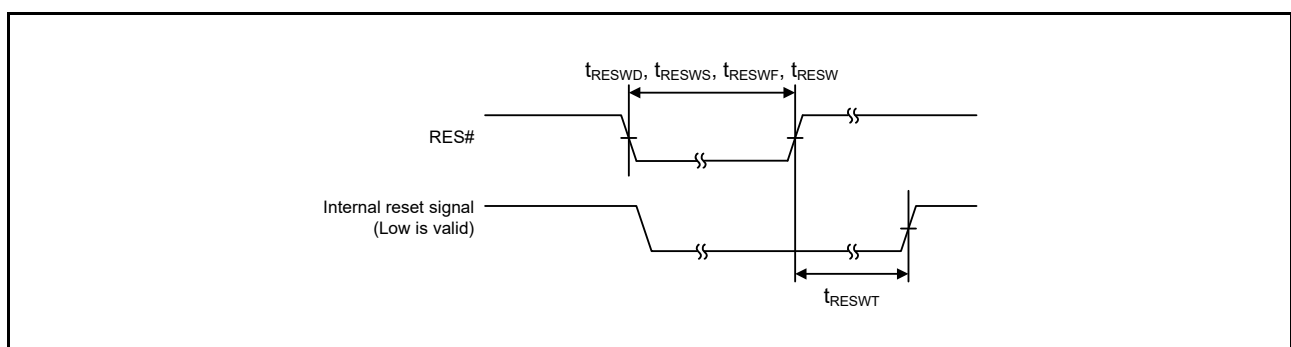


Figure 5.3 Reset Input Timing

5.4.2 Clock Timing

Table 5.16 BCLK Pin Output Clock Timing (1)

Conditions: $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, $V_{CC_USB} = 2.7\text{ to }5.5\text{ V}$, $AV_{CC0} = AV_{CC1} = AV_{CC2} = 3.0\text{ to }5.5\text{ V}$,
 $V_{SS} = V_{SS_USB} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0\text{ V}$,
 $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|----------------------------------|------------|------|------|------|------|-----------------|
| BCLK pin output cycle time | t_{Bcyc} | 25 | — | — | ns | Figure 5.4 |
| BCLK pin output high pulse width | t_{CH} | 7.5 | — | — | | |
| BCLK pin output low pulse width | t_{CL} | 7.5 | — | — | | |
| BCLK pin output rising time | t_{Cr} | — | — | 5 | | |
| BCLK pin output falling time | t_{Cf} | — | — | 5 | | |

Table 5.17 BCLK Pin Output Clock Timing (2)

Conditions: $2.7\text{ V} \leq V_{CC} < 4.5\text{ V}$, $V_{CC_USB} = 2.7\text{ to }5.5\text{ V}$, $AV_{CC0} = AV_{CC1} = AV_{CC2} = 3.0\text{ to }5.5\text{ V}$,
 $V_{SS} = V_{SS_USB} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0\text{ V}$,
 $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|----------------------------------|------------|--------|------|------|------|-----------------|
| BCLK pin output cycle time | t_{Bcyc} | 31.25 | — | — | ns | Figure 5.4 |
| BCLK pin output high pulse width | t_{CH} | 10.625 | — | — | | |
| BCLK pin output low pulse width | t_{CL} | 10.625 | — | — | | |
| BCLK pin output rising time | t_{Cr} | — | — | 5 | | |
| BCLK pin output falling time | t_{Cf} | — | — | 5 | | |

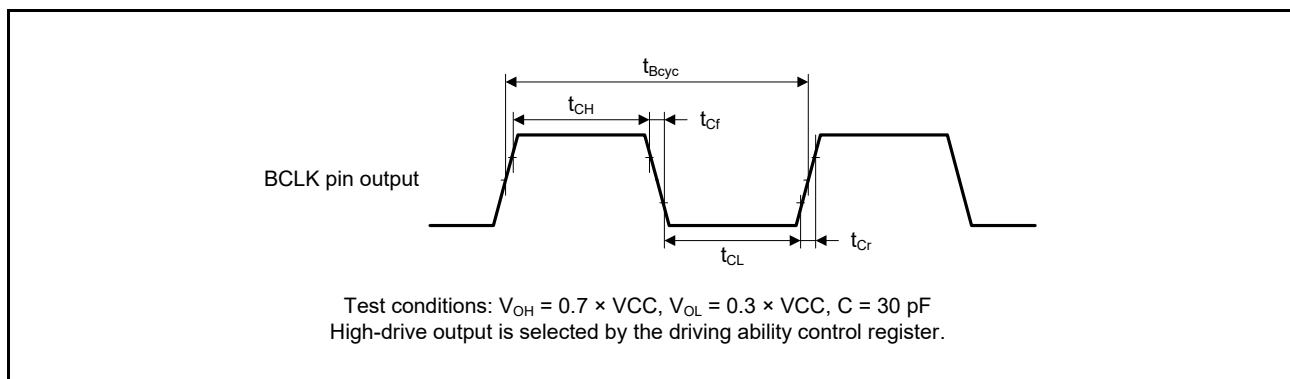
**Figure 5.4 BCLK Pin Output Timing**

Table 5.18 EXTAL Clock Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
 VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
 T_a = T_{opr}

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---------------------|-------|------|------|------|-----------------|
| EXTAL external clock input cycle time | t _{EXcyc} | 41.66 | — | — | ns | Figure 5.5 |
| EXTAL external clock input frequency | f _{EXMAIN} | — | — | 24 | MHz | |
| EXTAL external clock input high pulse width | t _{EXH} | 15.83 | — | — | ns | |
| EXTAL external clock input low pulse width | t _{EXL} | 15.83 | — | — | | |
| EXTAL external clock rising time | t _{EXr} | — | — | 5 | ns | |
| EXTAL external clock falling time | t _{EXf} | — | — | 5 | | |

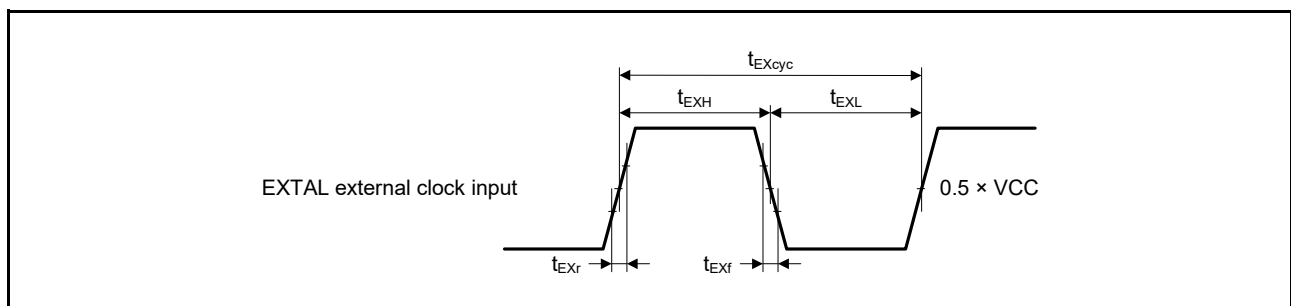


Figure 5.5 EXTAL External Clock Input Timing

Table 5.19 Main Clock Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
 VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
 T_a = T_{opr}

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|------------------------|------|------|------|------|-----------------|
| Main clock oscillation frequency | f _{MAIN} | 8 | — | 24 | MHz | Figure 5.6 |
| Main clock oscillator stabilization time (crystal) | t _{MAINOSC} | — | — | —*1 | ms | |
| Main clock oscillator stabilization wait time (crystal) | t _{MAINOSCWT} | — | — | —*2 | | |

Note 1. When using a main clock, ask the manufacturer of the oscillator to evaluate its oscillation. Refer to the results of evaluation provided by the manufacturer for the oscillation stabilization time.

Note 2. The number of cycles selected by the value of the MOSCWTCR.MSTS[7:0] bits determines the main clock oscillation stabilization wait time in accord with the formula below.

$$t_{\text{MAINOSCWT}} = [(MSTS[7:0] \text{ bits} \times 32) + 7] / f_{\text{LOCO}}$$

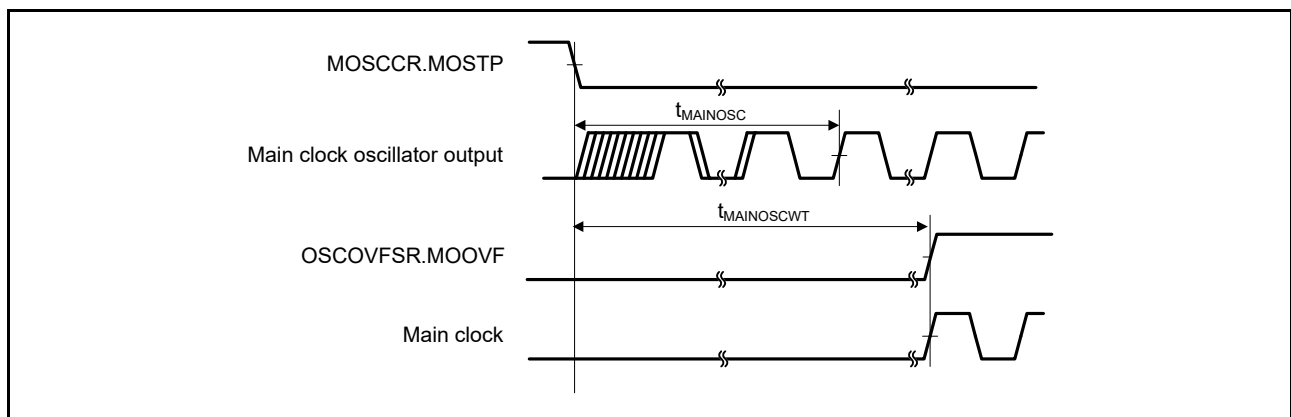


Figure 5.6 Main Clock Oscillation Start Timing

Table 5.20 LOCO and IWDT-Dedicated Low-Speed Clock Timing

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V,
 $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|--|---------------|------|------|------|---------|-----------------|
| LOCO clock cycle time | t_{Lcyc} | 3.78 | 4.16 | 4.63 | μ s | |
| LOCO clock oscillation frequency | f_{LOCO} | 216 | 240 | 264 | kHz | |
| LOCO clock oscillation stabilization time | t_{LOCOWT} | — | — | 44 | μ s | Figure 5.7 |
| IWDT-dedicated low-speed clock cycle time | t_{iLcyc} | 7.57 | 8.33 | 9.26 | | |
| IWDT-dedicated low-speed clock oscillation frequency | f_{iLOCO} | 108 | 120 | 132 | kHz | |
| IWDT-dedicated low-speed clock oscillation stabilization wait time | $t_{iLOCOWT}$ | — | 142 | 190 | μ s | Figure 5.8 |

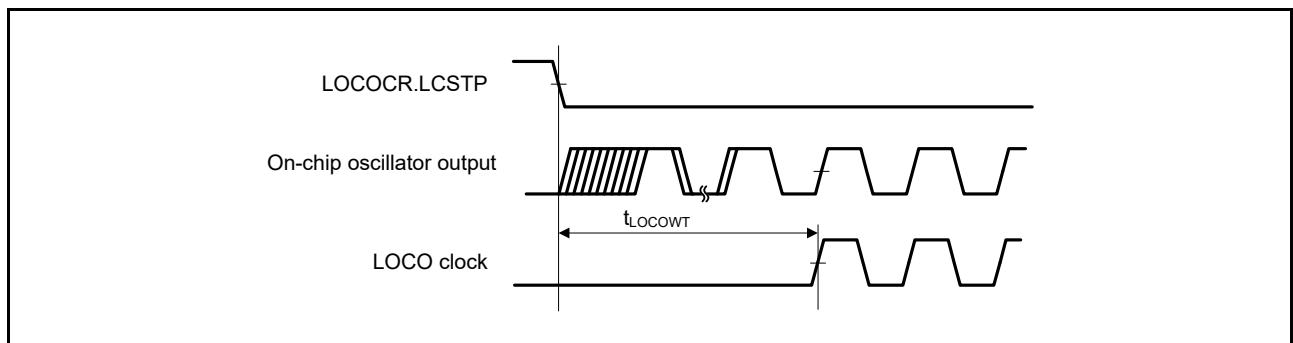


Figure 5.7 LOCO Clock Oscillation Start Timing

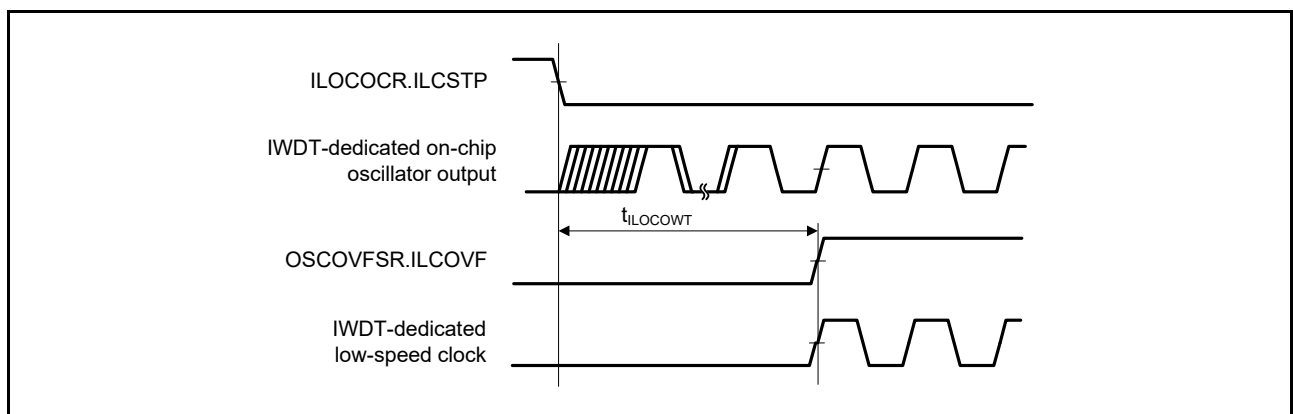


Figure 5.8 IWDT-dedicated Low-Speed Clock Oscillation Start Timing

Table 5.21 HOCO Clock Timing

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V,
 $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|--|--------------|-------|------|-------|---------------|---|
| HOCO clock oscillation frequency | f_{HOCO} | 15.61 | 16 | 16.39 | MHz | $-20^{\circ}\text{C} \leq T_a \leq 105^{\circ}\text{C}$ |
| | | 17.56 | 18 | 18.44 | | |
| | | 19.52 | 20 | 20.48 | | |
| | | 15.52 | 16 | 16.48 | | $-40^{\circ}\text{C} \leq T_a < -20^{\circ}\text{C}$ |
| | | 17.46 | 18 | 18.54 | | |
| | | 19.40 | 20 | 20.60 | | |
| HOCO clock oscillation stabilization wait time | t_{HOCOWT} | — | 105 | 149 | μs | Figure 5.9 |
| HOCO clock power supply stabilization time | t_{HOCOP} | — | — | 150 | | Figure 5.10 |

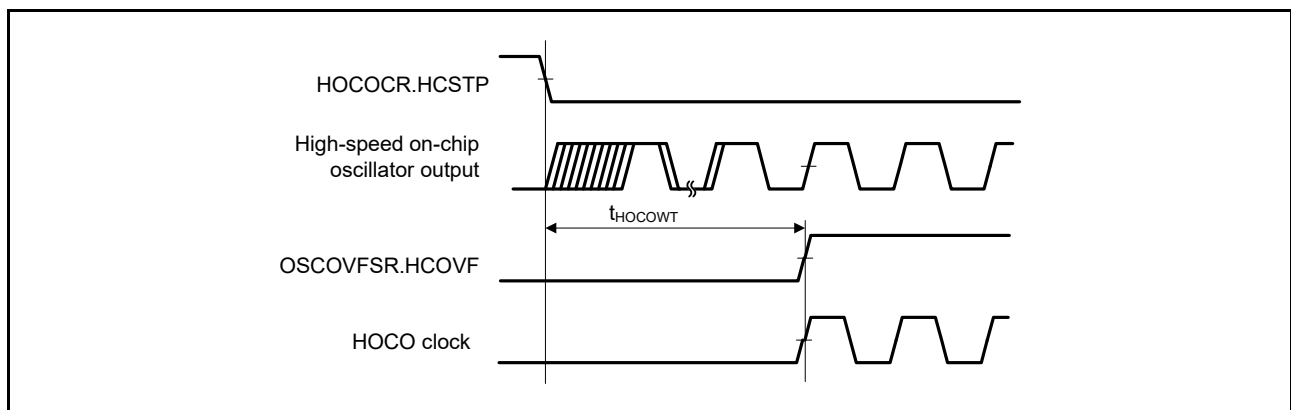


Figure 5.9 HOCO Clock Oscillation Start Timing (Oscillation is Started by Setting the HOCO CR.HCSTP Bit)

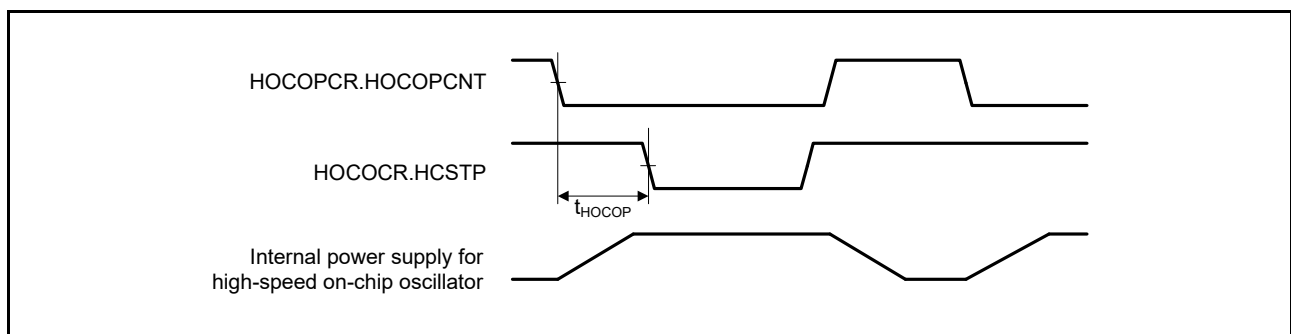


Figure 5.10 High-Speed On-Chip Oscillator Power Supply Control Timing

Table 5.22 PLL Clock Timing

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AV_{CC0} = AV_{CC1} = AV_{CC2} = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0$ V,
 $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|-------------|------|------|------|---------|-----------------|
| PLL clock oscillation frequency | f_{PLL} | 120 | — | 240 | MHz | |
| PLL clock oscillation stabilization wait time | t_{PLLWT} | — | 259 | 320 | μ s | Figure 5.11 |

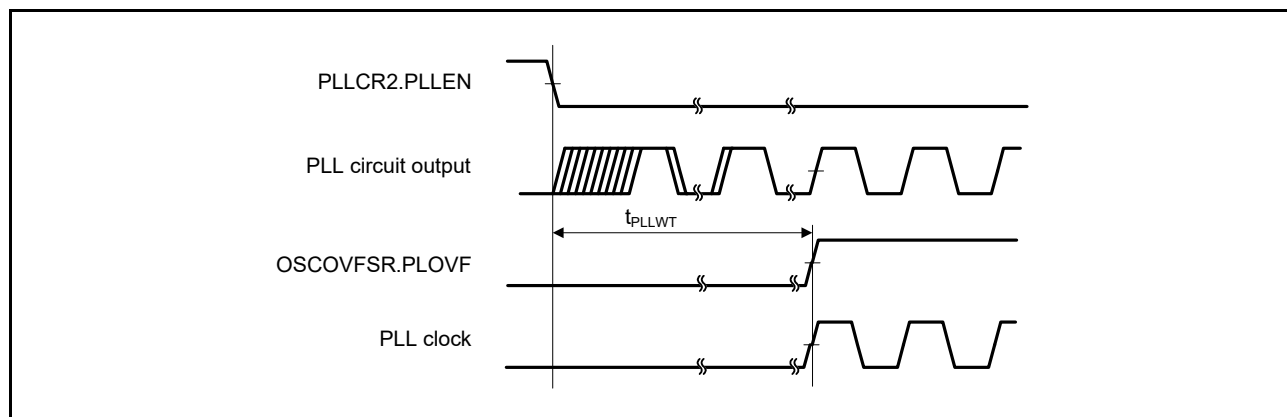


Figure 5.11 PLL Clock Oscillation Start Timing

5.4.3 Timing of Recovery from Low Power Consumption Modes

Table 5.23 Timing of Recovery from Low Power Consumption Modes (1)

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
T_a = T_{opr}

| Item | Symbol | Min. | Typ. | Max. | | Unit | Test Conditions | | |
|---|--|---|--------------------|--------------------------|------------------------|--|--|----|-------------|
| | | | | t _{SBYOSCWT} *2 | t _{SBYSEQ} *3 | | | | |
| Recovery time after cancellation of software standby mode*1 | Crystal resonator connected to main clock oscillator | Main clock oscillator operating | t _{SBYMC} | — | — | $\{(MSTS[7:0] \text{ bits} \times 32) + 76\} / 0.216$ | $100 + 7 / f_{ICLK} + 2n / f_{MAIN}$ | μs | Figure 5.12 |
| | | Main clock oscillator and PLL circuit operating | t _{SBYPC} | — | — | $\{(MSTS[7:0] \text{ bits} \times 32) + 138\} / 0.216$ | $100 + 7 / f_{ICLK} + 2n / f_{PLL}$ | | |
| | External clock input to main clock oscillator | Main clock oscillator operating | t _{SBYEX} | — | — | 352 | $100 + 7 / f_{ICLK} + 2n / f_{EXMAIN}$ | | |
| | | Main clock oscillator and PLL circuit operating | t _{SBYPE} | — | — | 639 | $100 + 7 / f_{ICLK} + 2n / f_{PLL}$ | | |
| | High-speed on-chip oscillator operating | High-speed on-chip oscillator operating | t _{SBYHO} | — | — | 454 | $100 + 7 / f_{ICLK} + 2n / f_{HOCO}$ | | |
| | | High-speed on-chip oscillator operating and PLL circuit operating | t _{SBYPH} | — | — | 741 | $100 + 7 / f_{ICLK} + 2n / f_{PLL}$ | | |
| | Low-speed on-chip oscillator operating*4 | t _{SBYLO} | — | — | — | 338 | $100 + 7 / f_{ICLK} + 2n / f_{LOCO}$ | | |

Note 1. The time for return after release from software standby is determined by the value obtained by adding the oscillation stabilization waiting time (t_{SBYOSCWT}) and the time required for operations by the software standby release sequencer (t_{SBYSEQ}).

Note 2. When several oscillators were running before the transition to software standby, the greatest value of the oscillation stabilization waiting time t_{SBYOSCWT} is selected.

Note 3. For n, the greatest value is selected from among the internal clock division settings.

Note 4. This condition applies when f_{ICLK} : f_{FCLK} = 1 : 1, 2 : 1, or 4 : 1.

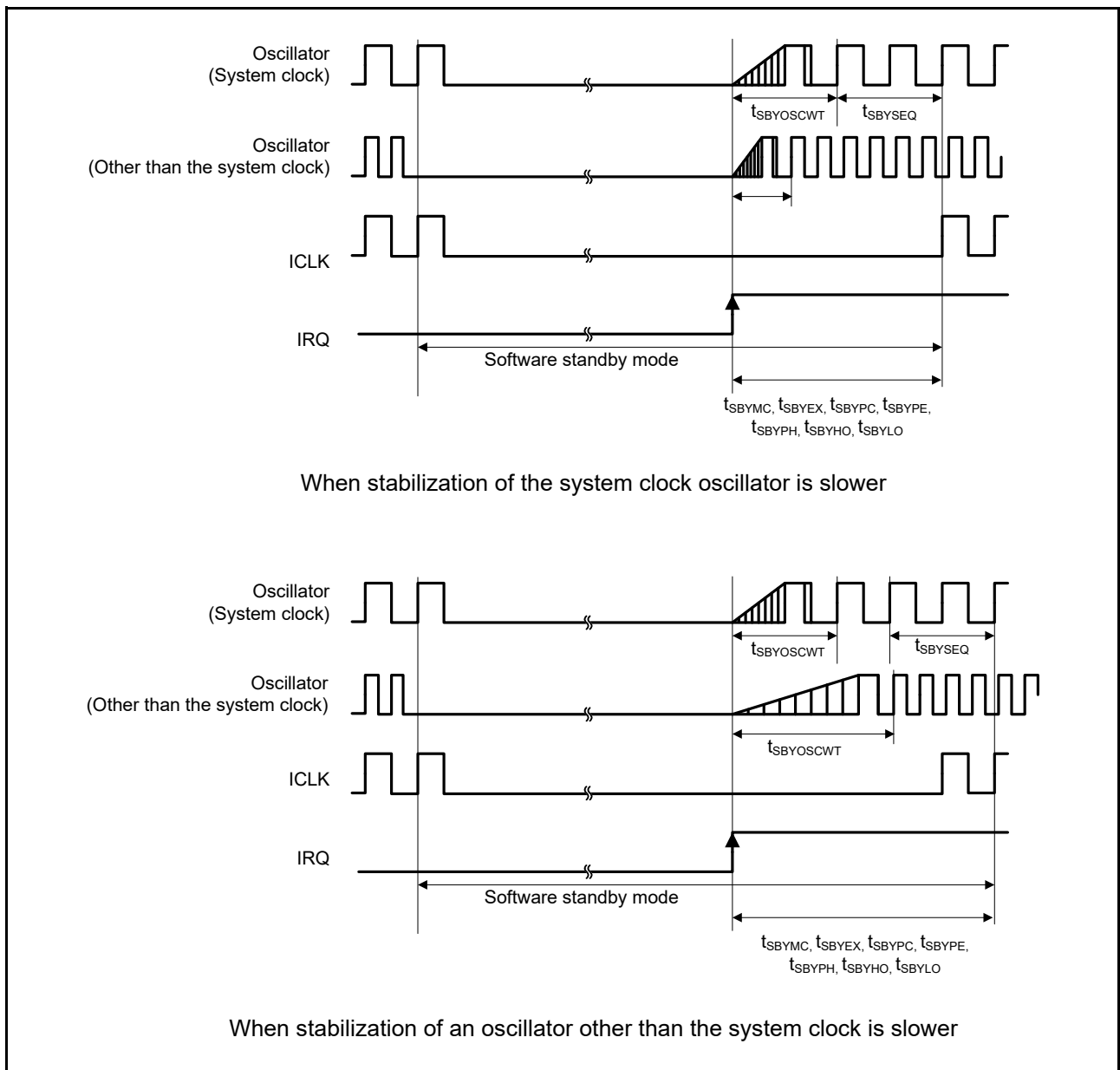


Figure 5.12 Software Standby Mode Cancellation Timing

Table 5.24 Timing of Recovery from Low Power Consumption Modes (2)

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AV_{CC0} = AV_{CC1} = AV_{CC2} = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0$ V,
 $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|--|--------------|------|------|------|------------|-----------------|
| Recovery time after cancellation of deep software standby mode | t_{DSBY} | — | — | 0.9 | ms | Figure 5.13 |
| Wait time after cancellation of deep software standby mode | t_{DSBYWT} | 31 | — | 32 | t_{Lcyc} | |

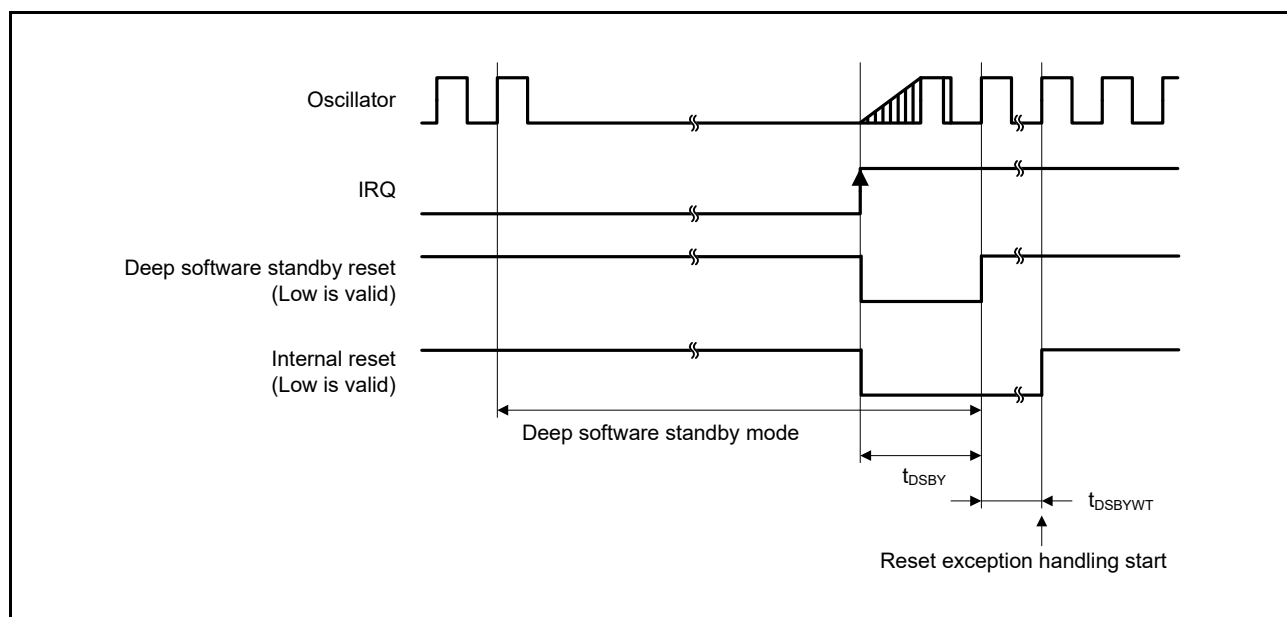


Figure 5.13 Deep Software Standby Mode Cancellation Timing

5.4.4 Control Signal Timing

Table 5.25 Control Signal Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5 V,
 VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
 T_a = T_{opr}

| Item | Symbol | Min.*1 | Typ. | Max. | Unit | Test Conditions*1 |
|-----------------|-------------------|------------------------|------|------|------|--|
| NMI pulse width | t _{NMIW} | 200 | — | — | ns | 2 × t _{PBcyc} ≤ 200 ns, Figure 5.14 |
| | | 2 × t _{PBcyc} | — | — | | 2 × t _{PBcyc} > 200 ns, Figure 5.14 |
| IRQ pulse width | t _{IRQW} | 200 | — | — | | 2 × t _{PBcyc} ≤ 200 ns, Figure 5.15 |
| | | 2 × t _{PBcyc} | — | — | | 2 × t _{PBcyc} > 200 ns, Figure 5.15 |

Note 1. t_{PBcyc}: PCLKB cycle

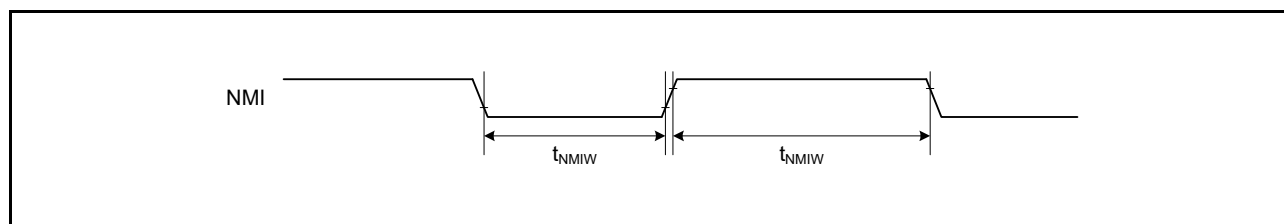


Figure 5.14 NMI Interrupt Input Timing

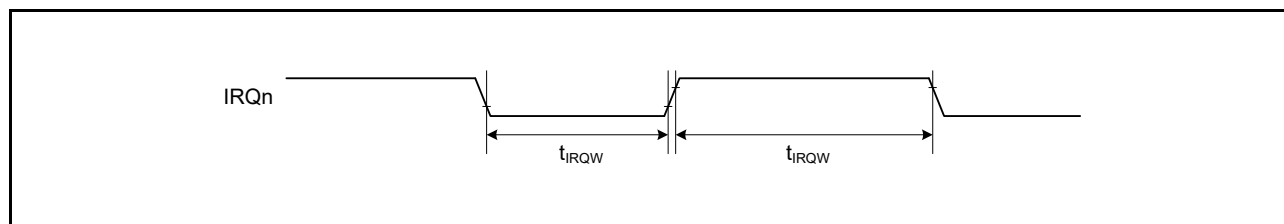


Figure 5.15 IRQ Interrupt Input Timing

5.4.5 Bus Timing

Table 5.26 Bus Timing (1)

Conditions: $4.5\text{ V} \leq V_{CC} \leq 5.5\text{ V}$, $V_{CC_USB} = 2.7\text{ to }5.5\text{ V}$, $AVCC0 = AVCC1 = AVCC2 = 3.0\text{ to }5.5\text{ V}$,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0\text{ V}$, $T_a = T_{opr}$,
 $ICLK = 8\text{ to }160\text{ MHz}$, $PCLKA = 8\text{ to }120\text{ MHz}$, $PCLKB = 8\text{ to }60\text{ MHz}$, $PCLKC = 8\text{ to }160\text{ MHz}$, $BCLK = 8\text{ to }60\text{ MHz}$,
 Output load conditions: $V_{OH} = 0.5 \times V_{CC}$, $V_{OL} = 0.5 \times V_{CC}$, $C = 30\text{ pF}$,
 High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|-------------------------|------------|------|------|------|------|-------------------------------|
| Address delay time | t_{AD} | — | — | 12.5 | ns | Figure 5.16 to Figure 5.21 |
| Byte control delay time | t_{BCD} | — | — | 12.5 | | |
| CS# delay time | t_{CSD} | — | — | 12.5 | | |
| ALE delay time | t_{ALED} | — | — | 12.5 | | |
| RD# delay time | t_{RSD} | — | — | 12.5 | | |
| Read data setup time | t_{RDS} | 12.5 | — | — | | |
| Read data hold time | t_{RDH} | 0 | — | — | | |
| WR# delay time | t_{WRD} | — | — | 12.5 | | |
| Write data delay time | t_{WDD} | — | — | 12.5 | | |
| Write data hold time | t_{WDH} | 0 | — | — | | |
| WAIT# setup time | t_{WTS} | 12.5 | — | — | | |
| WAIT# hold time | t_{WTH} | 0 | — | — | | |

Table 5.27 Bus Timing (2)

Conditions: $2.7\text{ V} \leq V_{CC} < 4.5\text{ V}$, $V_{CC_USB} = 2.7\text{ to }5.5\text{ V}$, $AVCC0 = AVCC1 = AVCC2 = 3.0\text{ to }5.5\text{ V}$,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0\text{ V}$, $T_a = T_{opr}$,
 $ICLK = 8\text{ to }160\text{ MHz}$, $PCLKA = 8\text{ to }120\text{ MHz}$, $PCLKB = 8\text{ to }60\text{ MHz}$, $PCLKC = 8\text{ to }160\text{ MHz}$, $BCLK = 8\text{ to }60\text{ MHz}$,
 Output load conditions: $V_{OH} = 0.5 \times V_{CC}$, $V_{OL} = 0.5 \times V_{CC}$, $C = 30\text{ pF}$,
 High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|-------------------------|------------|------|------|------|------|-------------------------------|
| Address delay time | t_{AD} | — | — | 25 | ns | Figure 5.16 to Figure 5.21 |
| Byte control delay time | t_{BCD} | — | — | 25 | | |
| CS# delay time | t_{CSD} | — | — | 25 | | |
| ALE delay time | t_{ALED} | — | — | 25 | | |
| RD# delay time | t_{RSD} | — | — | 25 | | |
| Read data setup time | t_{RDS} | 25 | — | — | | |
| Read data hold time | t_{RDH} | 0 | — | — | | |
| WR# delay time | t_{WRD} | — | — | 25 | | |
| Write data delay time | t_{WDD} | — | — | 25 | | |
| Write data hold time | t_{WDH} | 0 | — | — | | |
| WAIT# setup time | t_{WTS} | 25 | — | — | | |
| WAIT# hold time | t_{WTH} | 0 | — | — | | |

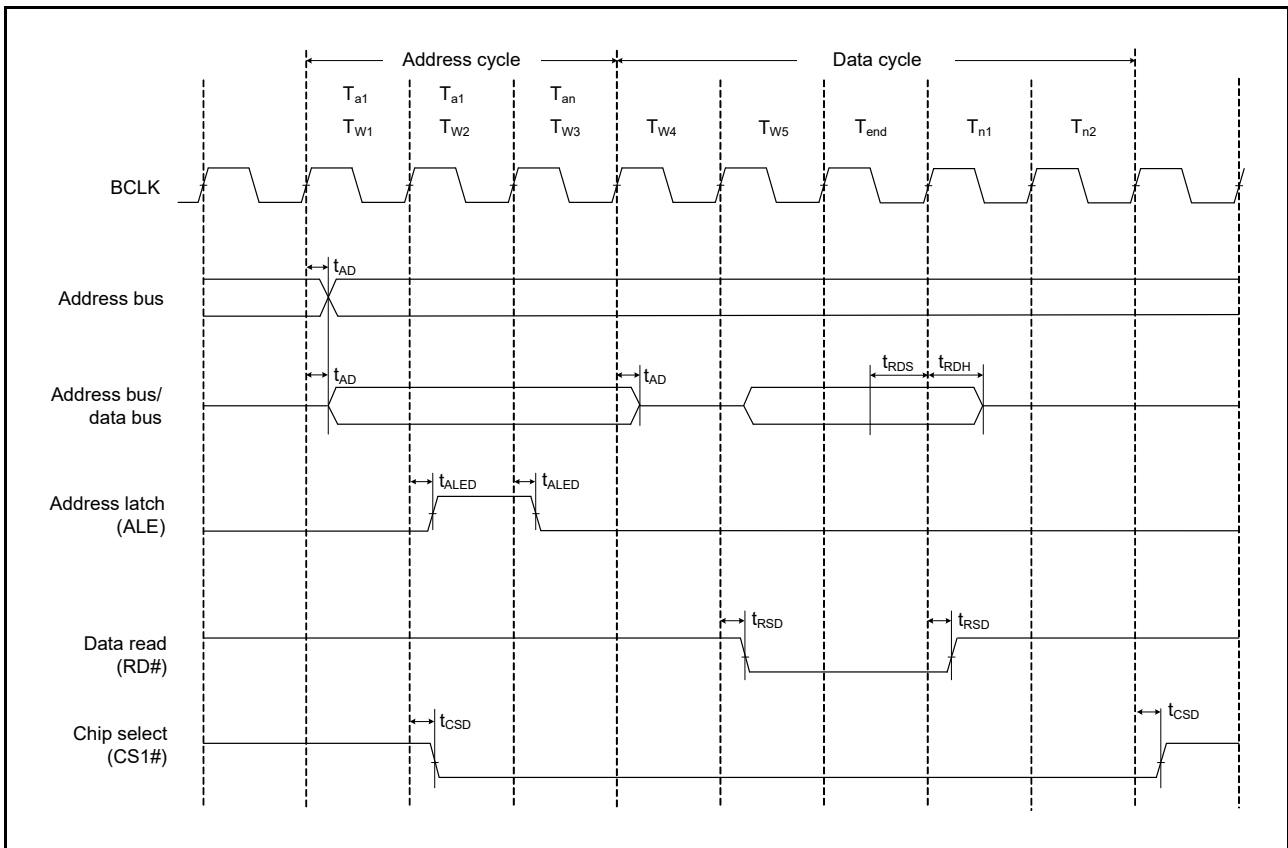


Figure 5.16 Address/Data Multiplexed Bus Read Access Timing

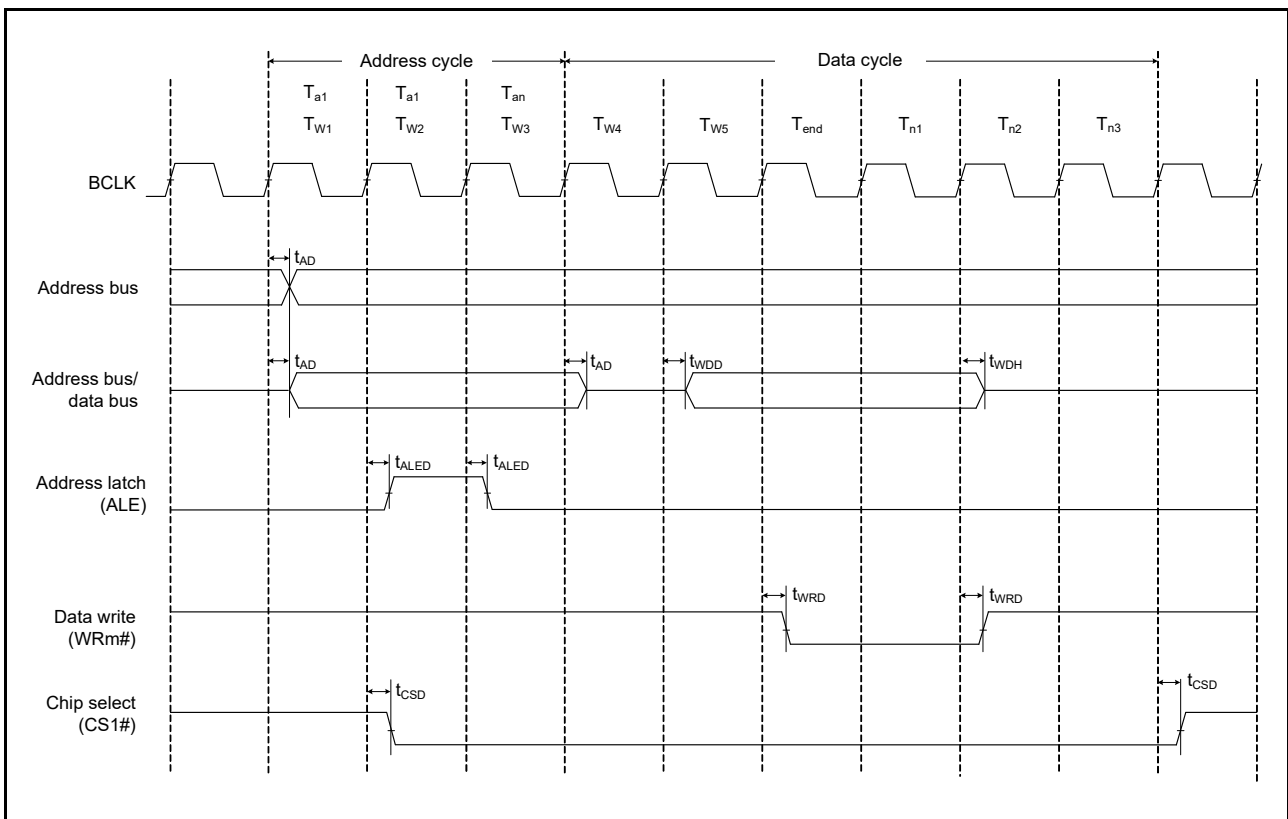


Figure 5.17 Address/Data Multiplexed Bus Write Access Timing

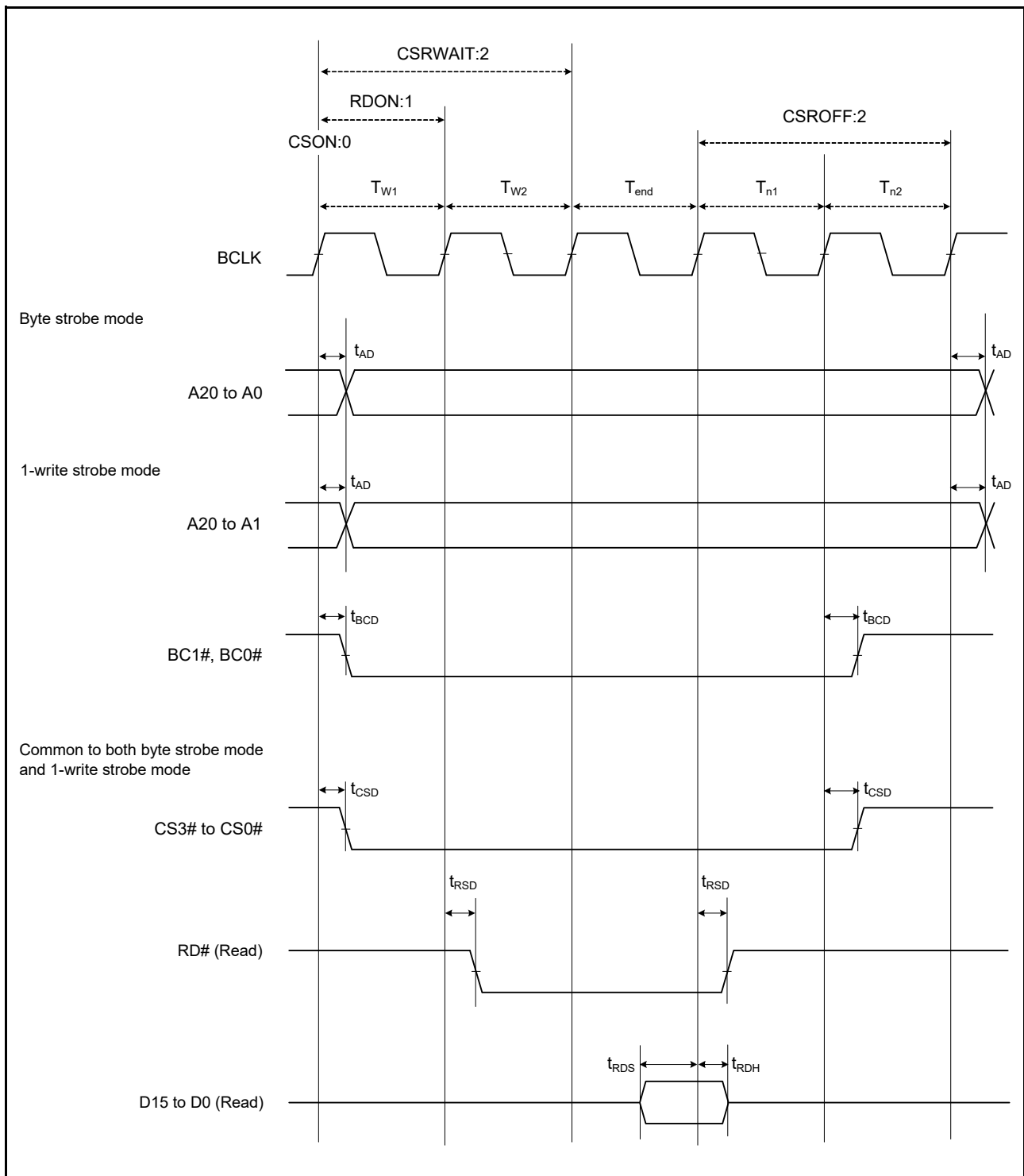


Figure 5.18 External Bus Timing/Normal Read Cycle (Bus Clock Synchronized)

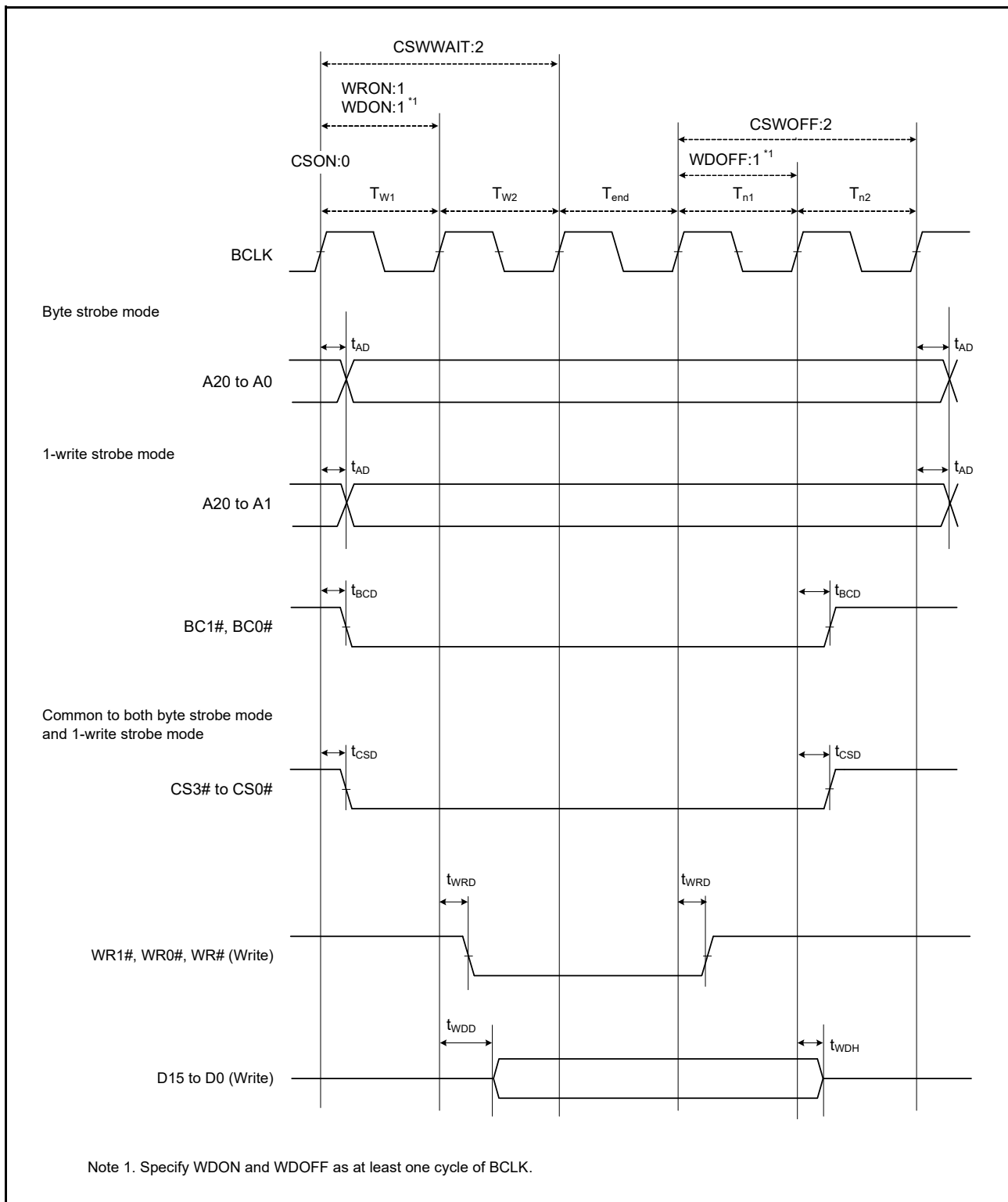


Figure 5.19 External Bus Timing/Normal Write Cycle (Bus Clock Synchronized)

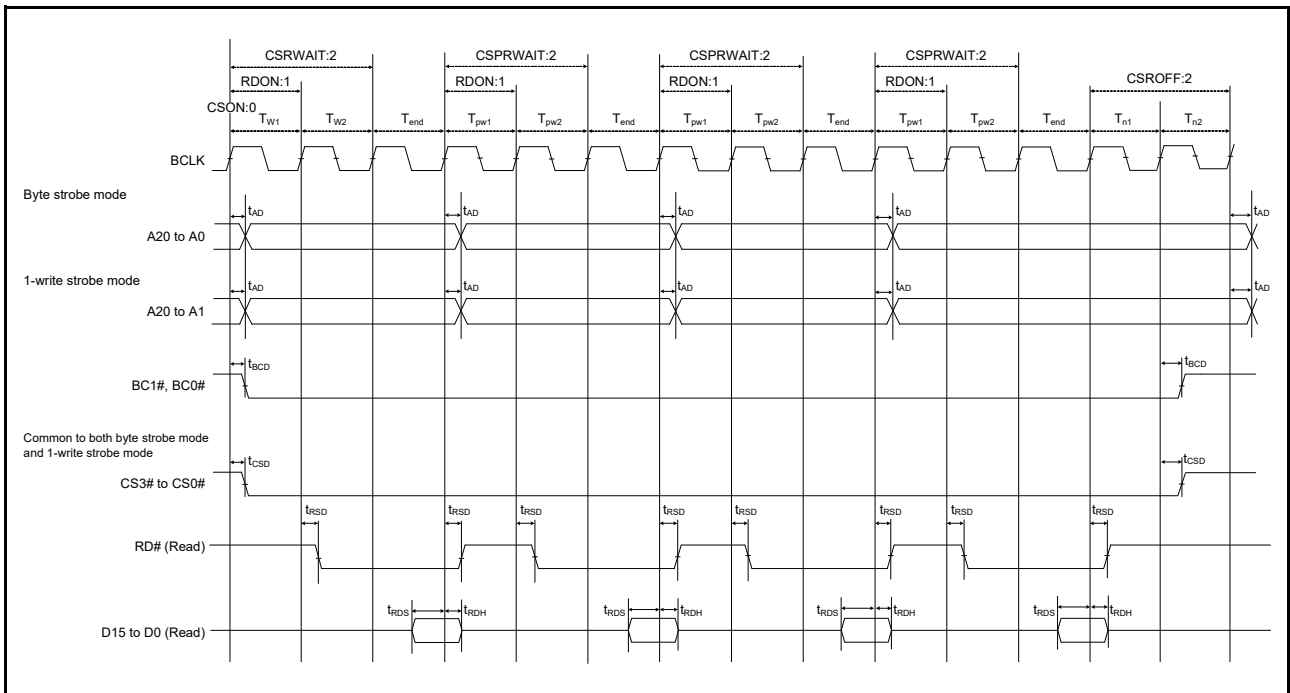


Figure 5.20 External Bus Timing/Page Read Cycle (Bus Clock Synchronized)

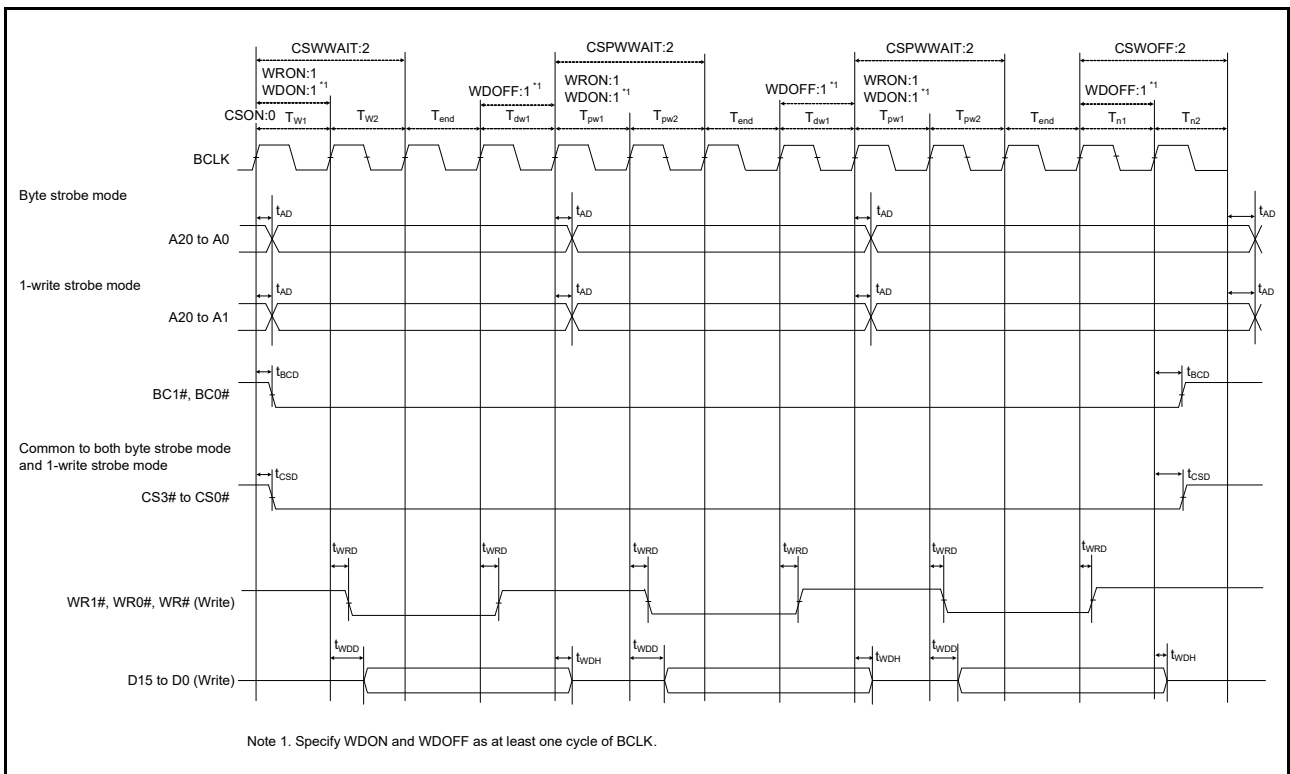


Figure 5.21 External Bus Timing/Page Write Cycle (Bus Clock Synchronized)

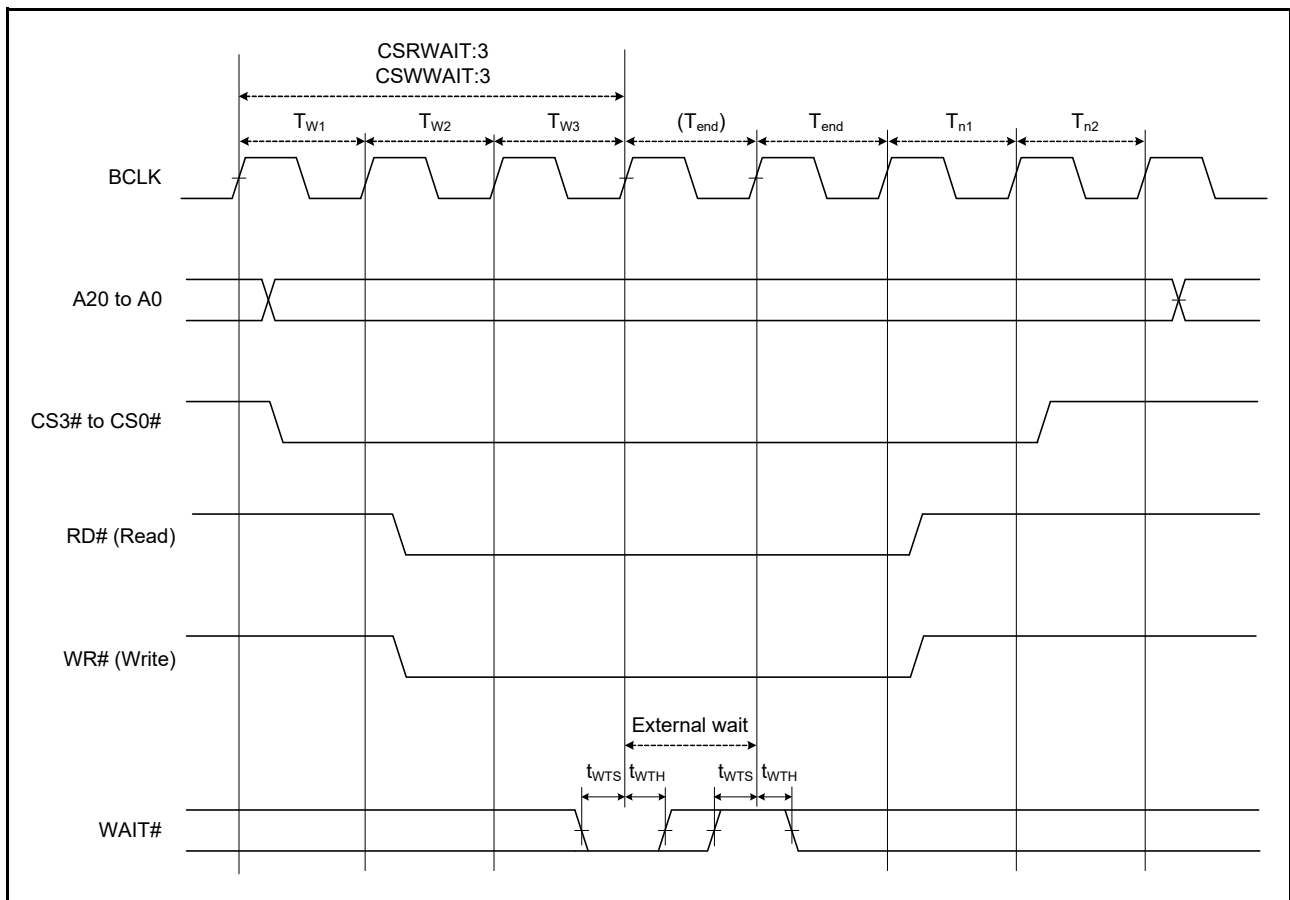


Figure 5.22 External Bus Timing/External Wait Control

5.4.6 Timing of On-Chip Peripheral Modules

Table 5.28 I/O Port Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
 VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = T_{opr},
 ICLK = 8 to 160 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 160 MHz, BCLK = 8 to 60 MHz,
 Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
 High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|-----------|------------------------|------------------|------|------|--------------------|-----------------|
| I/O ports | Input data pulse width | t _{PRW} | 1.5 | — | t _{PBcyc} | Figure 5.23 |

Note 1. t_{PBcyc}: PCLKB cycle

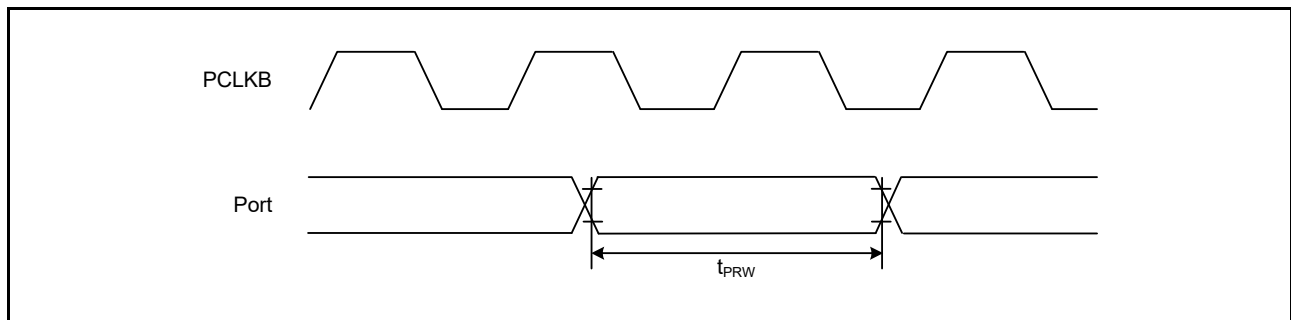


Figure 5.23 I/O Port Input Timing

Table 5.29 TMR Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
 VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = T_{opr},
 ICLK = 8 to 160 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 160 MHz, BCLK = 8 to 60 MHz,
 Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
 High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions | |
|------|-------------------------|---------------------|--|------|--------|--------------------|-------------|
| TMR | Timer clock pulse width | Single-edge setting | t _{TMCWH} , t _{TMCWL} | 1.5 | — | t _{PBcyc} | Figure 5.24 |
| | | Both-edge setting | | 2.5 | — | | |

Note 1. t_{PBcyc}: PCLKB cycle

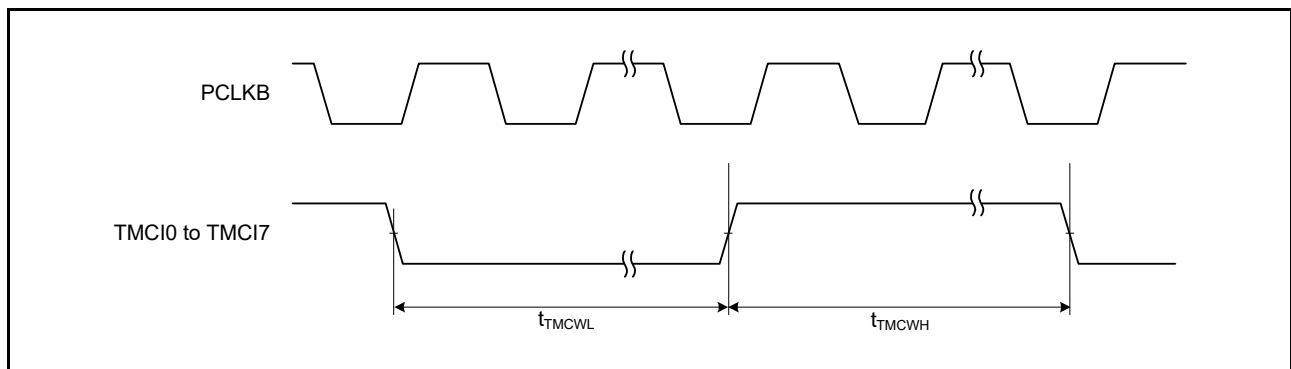


Figure 5.24 TMR Clock Input Timing

Table 5.30 MTU Timing

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V, $T_a = T_{opr}$,
 $ICLK = 8$ to 160 MHz, $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $PCLKC = 8$ to 160 MHz, $BCLK = 8$ to 60 MHz,
 Output load conditions: $V_{OH} = 0.5 \times V_{CC}$, $V_{OL} = 0.5 \times V_{CC}$, $C = 30$ pF,
 High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions | |
|------|---------------------------------|---------------------|--------------------------------|------|-------------|-----------------|-------------|
| MTU | Input capture input pulse width | Single-edge setting | 1.5 | — | t_{PCcyc} | Figure 5.25 | |
| | | Both-edge setting | 2.5 | — | | | |
| | Timer clock pulse width | Single-edge setting | t_{MTCKWH} , t_{MTCKWL} | 1.5 | — | | t_{PCcyc} |
| | | Both-edge setting | | 2.5 | — | | |
| | | Phase counting mode | | 2.5 | — | | |

Note 1. t_{PCcyc} : PCLKC cycle

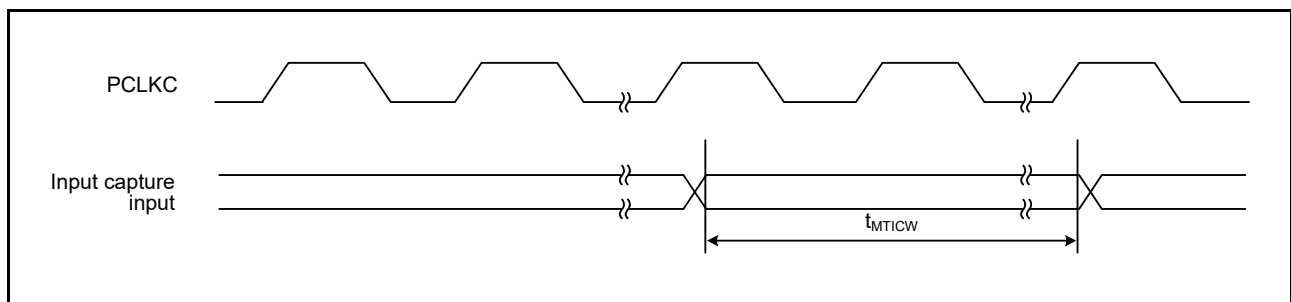


Figure 5.25 MTU Input Capture Input Timing

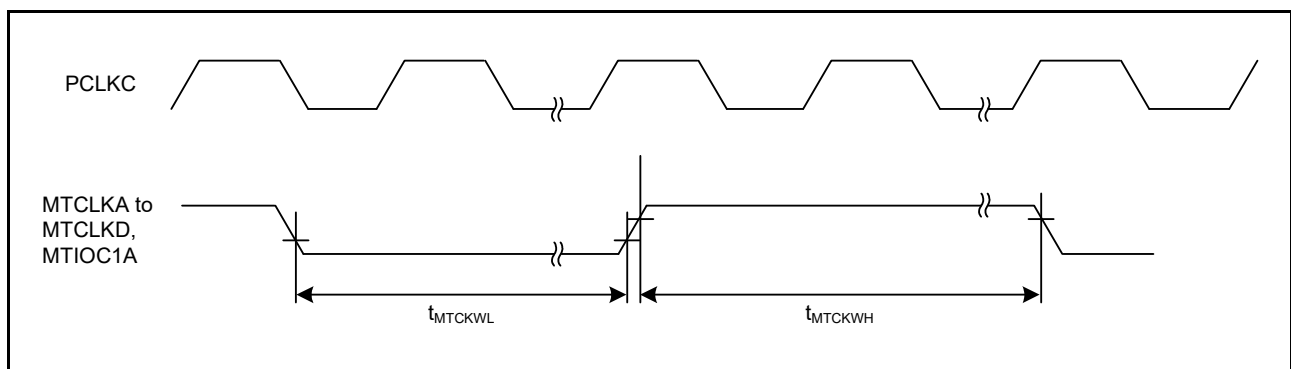


Figure 5.26 MTU Clock Input Timing

Table 5.31 POE and POEG Timing

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V, $T_a = T_{opr}$,
 $ICLK = 8$ to 160 MHz, $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $PCLKC = 8$ to 160 MHz, $BCLK = 8$ to 60 MHz,
Output load conditions: $V_{OH} = 0.5 \times V_{CC}$, $V_{OL} = 0.5 \times V_{CC}$, $C = 30$ pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | | Symbol | Min. | Typ. | Max. | Unit*1 | Test Conditions | |
|------|---|--|---------------|------|------|--|-----------------|---|
| POE | POEn# input pulse width (n = 0, 4, and 8 to 14) | t_{POEW} | 1.5 | — | — | t_{PBcyc} | Figure 5.27 | |
| | Output disable time | Transition of the POEn# signal level | t_{POEDI} | — | — | $5 \text{ PCLKB} + 0.24$ | μs | Figure 5.28 When detecting falling edges (ICSRM.POEnM[3:0] = 0000 (m = 1 to 5, 7 to 9, n = 0, 4, 8 to 14)) |
| | | Simultaneous conduction of output pins | t_{POEDO} | — | — | $3 \text{ PCLKB} + 0.2$ | μs | Figure 5.29 |
| | | Detection of comparator outputs | t_{POEDC} | — | — | $5 \text{ PCLKB} + 0.2$ | μs | Figure 5.30 The time is that when the noise filter for comparator C is not in use (CMPCTL.CDFS[1:0] = 00) and excludes the time for detection by comparator C. |
| | | Register setting | t_{POEDS} | — | — | $1 \text{ PCLKB} + 0.2$ | μs | Figure 5.31 Time for access to the register is not included. |
| | | Oscillation stop detection | t_{POEDOS} | — | — | 21 | μs | Figure 5.32 |
| POEG | GTETRn input pulse width (n = A to D) | t_{POEGW} | 1.5 | — | — | t_{PBcyc} | Figure 5.33 | |
| | Output disable time | Input level detection of the GTETRn pin (via flag) | t_{POEGDI} | — | — | $3 \text{ PCLKB} + 0.34$ | μs | Figure 5.34 When the digital noise filter is not in use (POEGn.NFEN = 0 (n = A to D)) |
| | | Detection of the output stopping signal from GPTW (deadtime error, simultaneous high output, or simultaneous low output) | t_{POEGDE} | — | — | 0.5 | μs | Figure 5.35 |
| | | Edge detection signal from a comparator | t_{POEGDC} | — | — | $4 \text{ PCLKB} + 0.5$ | μs | Figure 5.36 The time is that when the noise filter for comparator C is not in use (CMPCTL.CDFS[1:0] = 00) and excludes the time for detection by comparator C. |
| | | Register setting | t_{POEGDS} | — | — | $1 \text{ PCLKB} + 0.3$ | μs | Figure 5.37 Time for access to the register is not included. |
| | | Oscillation stop detection | $t_{POEGDOS}$ | — | — | 21 | μs | Figure 5.38 |
| | | Input level detection of the GTETRn pin (direct path) | $t_{POEGDDI}$ | — | — | $2 \text{ PCLKB} + 1 \text{ PCLKC} + 0.34$ | μs | Figure 5.39 |
| | | Level detection signal from a comparator | $t_{POEGDDC}$ | — | — | $3 \text{ PCLKB} + 0.3$ | μs | Figure 5.40 The time is that when the noise filter for comparator C is not in use (CMPCTL.CDFS[1:0] = 00) and excludes the time for detection by comparator C. |

Note 1. t_{PBcyc} : PCLKB cycle

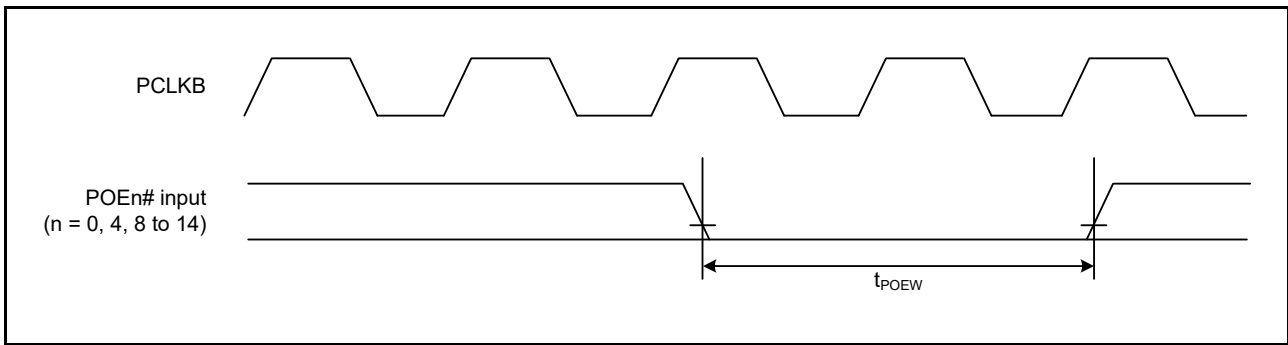


Figure 5.27 POE Input Timing

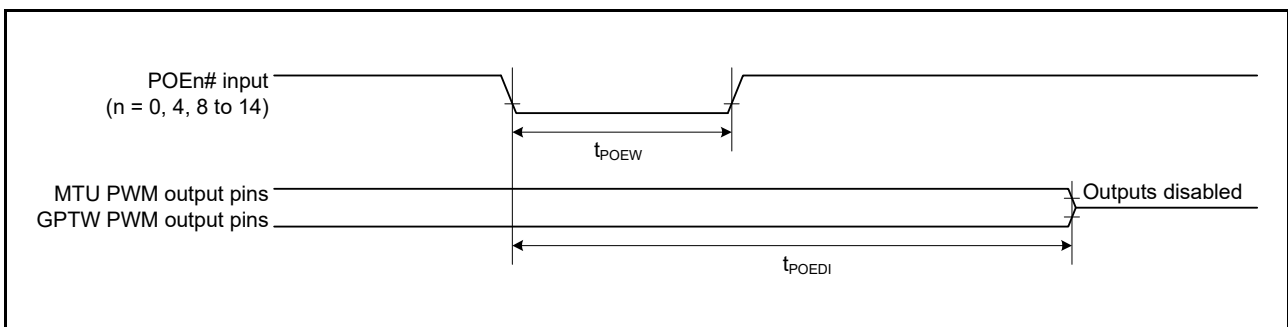


Figure 5.28 Output Disable Time for POE in Response to Transition of the POEn# Signal Level

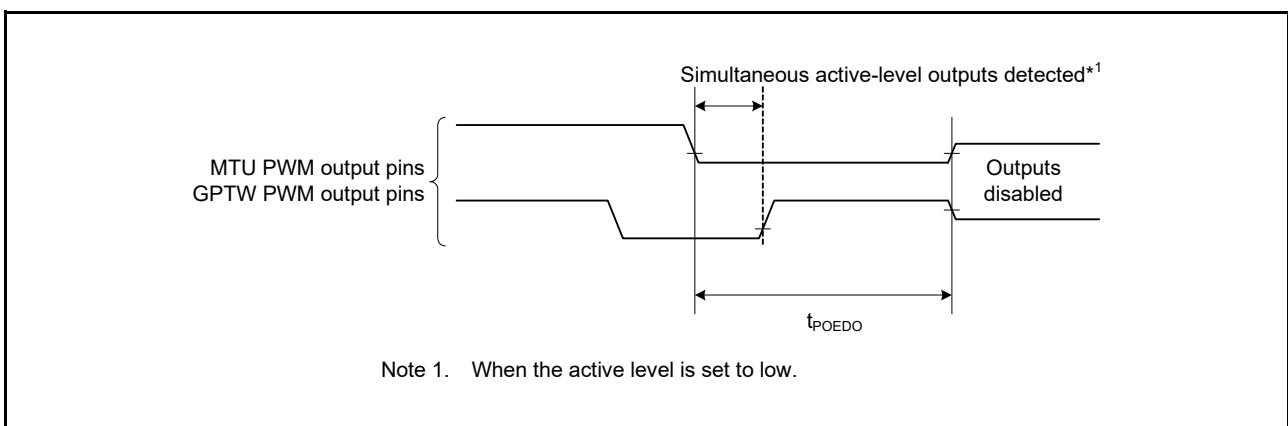


Figure 5.29 Output Disable Time for POE in Response to the Simultaneous Conduction of Output Pins

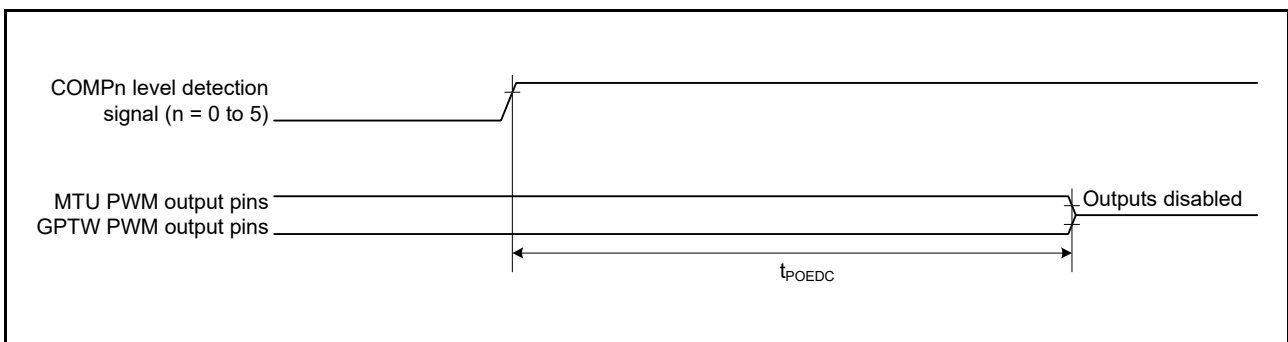


Figure 5.30 Output Disable Time for POE in Response to Detection of the Comparator Outputs

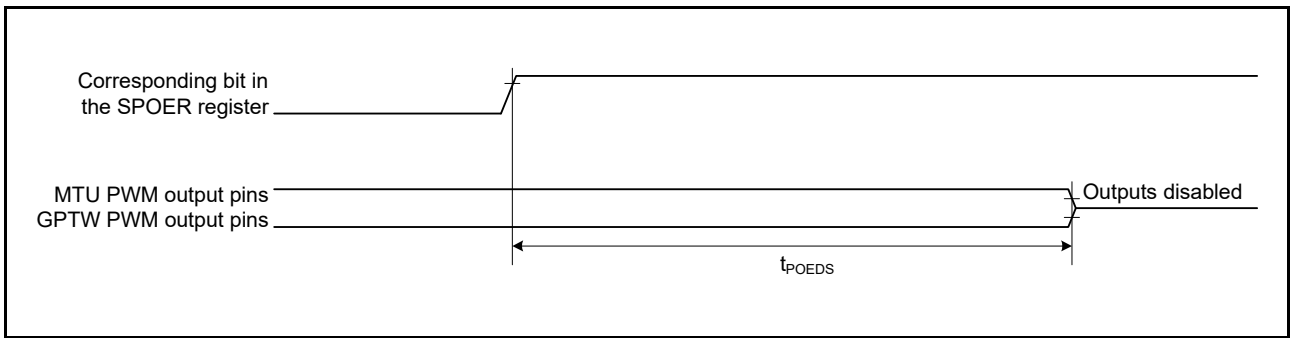


Figure 5.31 Output Disable Time for POE in Response to the Register Setting

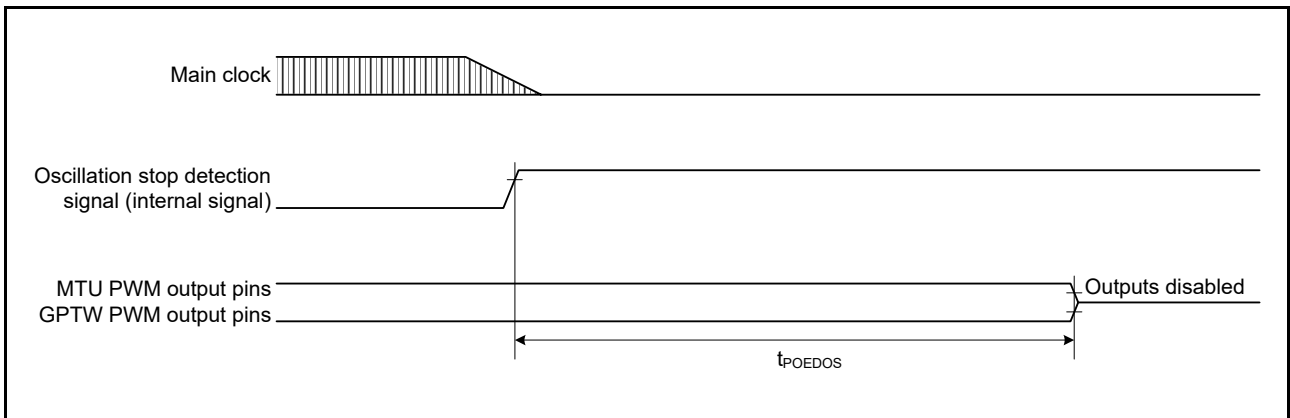


Figure 5.32 Output Disable Time for POE in Response to the Oscillation Stop Detection

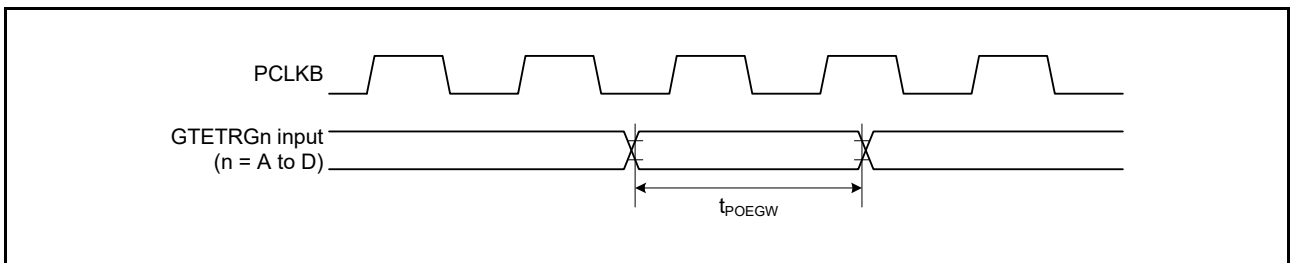


Figure 5.33 POEG Input Timing

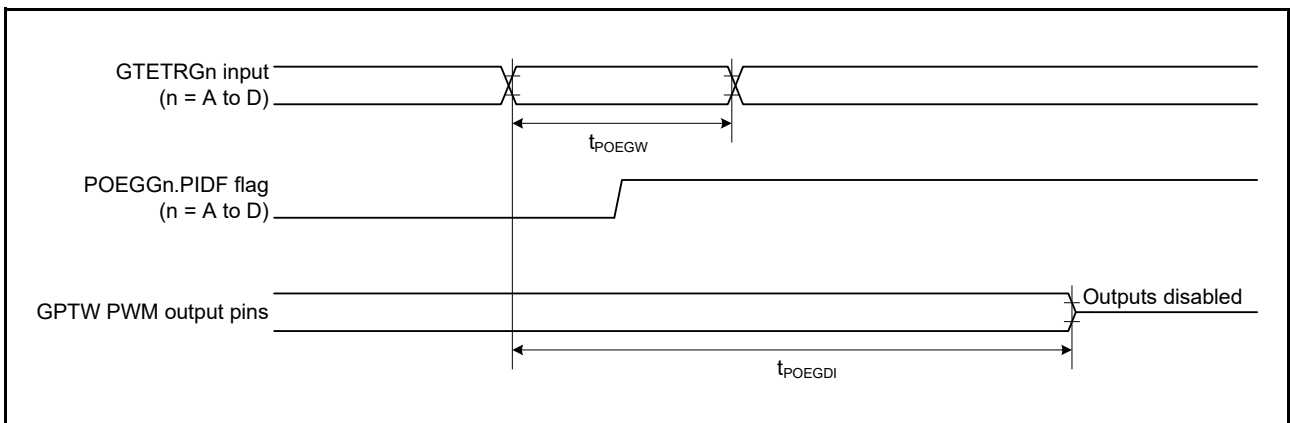


Figure 5.34 Output Disable Time for POEG via Detection Flag in Response to the Input Level Detection of the GTETRn pin

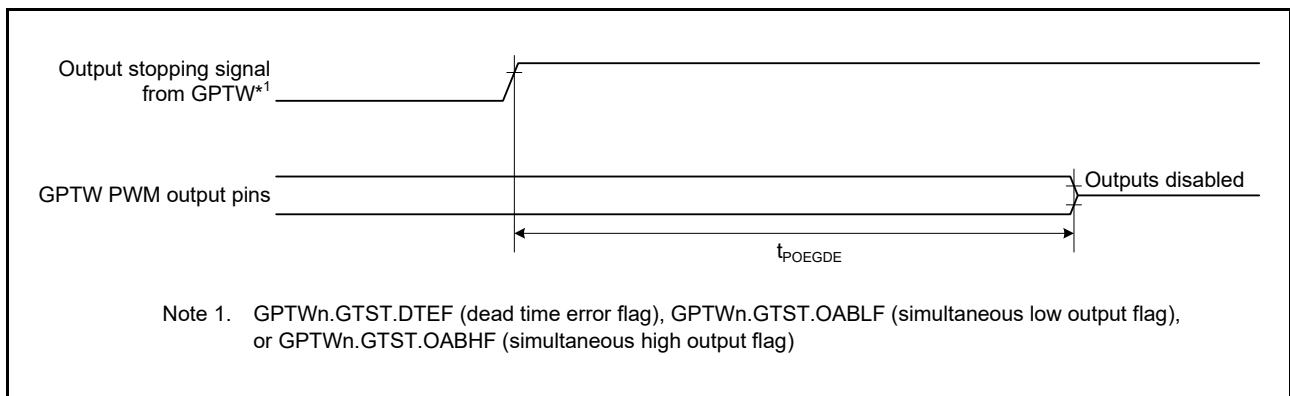


Figure 5.35 Output Disable Time for POEG in Response to Detection of the Output Stopping Signal from GPTW

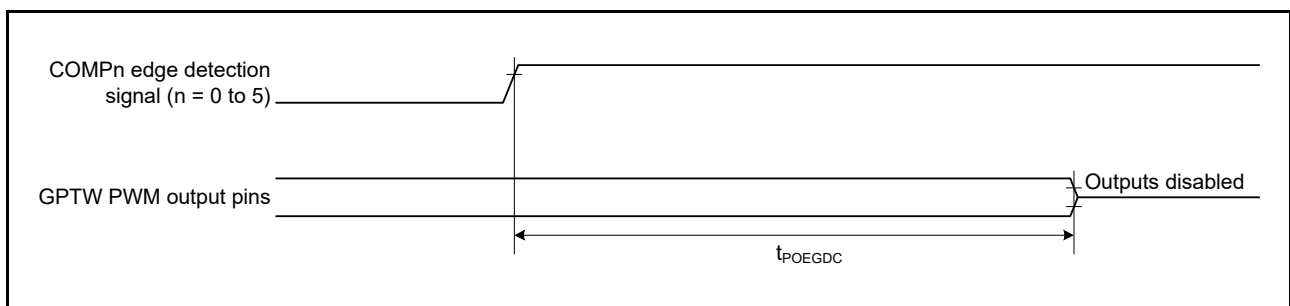


Figure 5.36 Output Disable Time for POEG in Response to Edge Detection Signal from a Comparator

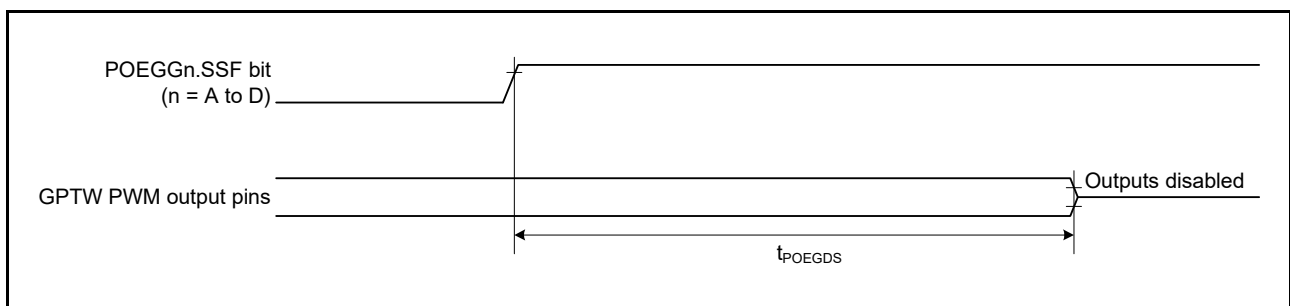


Figure 5.37 Output Disable Time for POEG in Response to the Register Setting

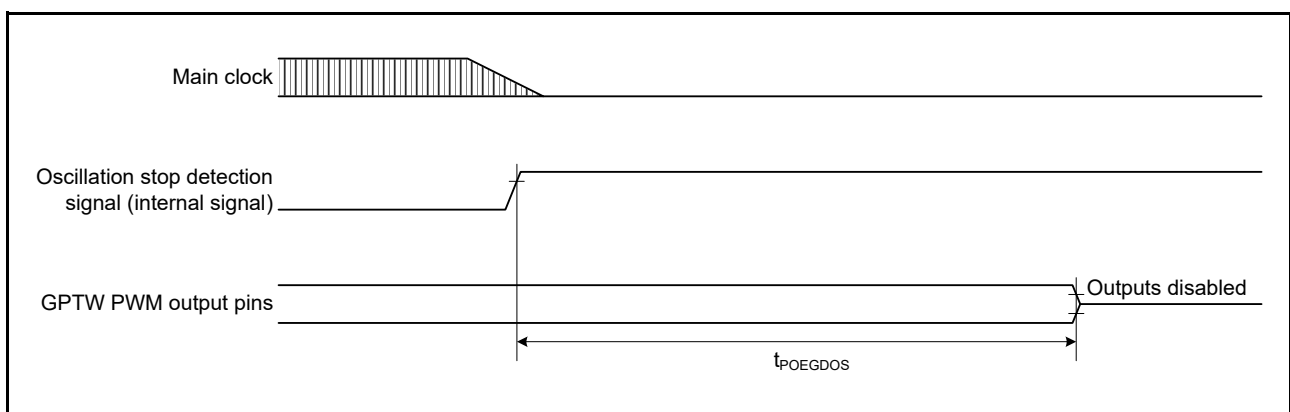


Figure 5.38 Output Disable Time of POEG in Response to the Oscillation Stop Detection

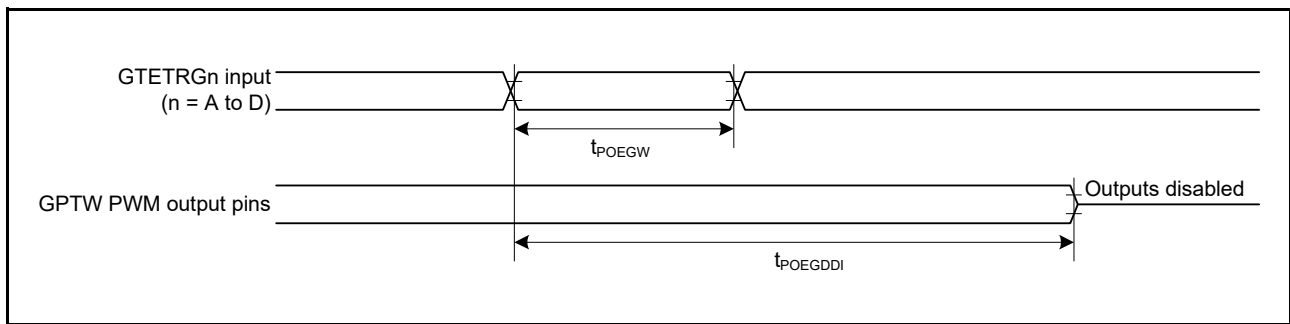


Figure 5.39 Output Disable Time for POEG in Direct Response to the Input Level Detection of the GTETRn pin

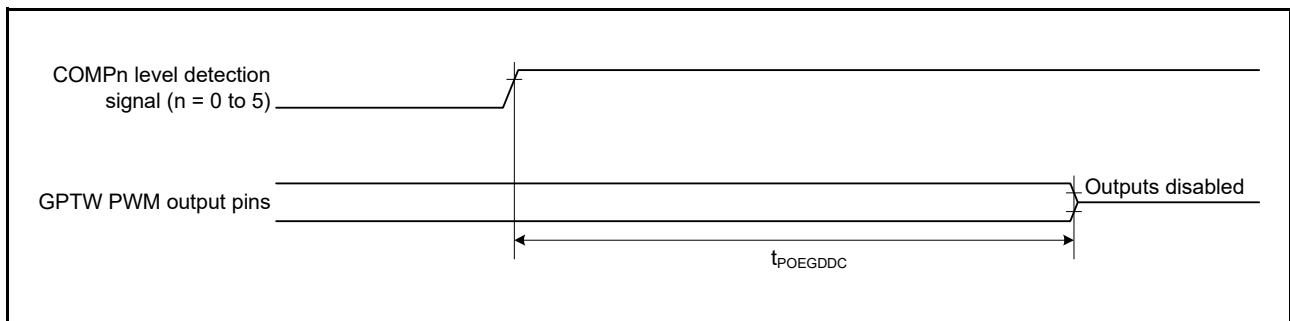


Figure 5.40 Output Disable Time for POEG in Response to Level Detection Signal from a Comparator

Table 5.32 GPTW Timing

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
 VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = T_{opr},
 ICLK = 8 to 160 MHz, PCLKA = 8 to 120 MHz, PCLKB = 8 to 60 MHz, PCLKC = 8 to 160 MHz, BCLK = 8 to 60 MHz,
 Output load conditions: V_{OH} = 0.5 × VCC, V_{OL} = 0.5 × VCC, C = 30 pF,
 High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | | Symbol | Min. | Max. | Unit*1, *2 | Test Conditions |
|-------------------------|------------------------------------|---------------------|------|------|-------------------|-----------------|
| GPTW | Input capture input pulse width | Single-edge setting | 1.5 | — | t _{PCyc} | Figure 5.41 |
| | | Both-edge setting | 2.5 | — | | |
| | External trigger input pulse width | Single-edge setting | 1.5 | — | t _{BCyc} | |
| | | Both-edge setting | 2.5 | — | | |
| Timer clock pulse width | | t _{GTCKWH} | 1.5 | — | t _{BCyc} | |
| | | t _{GTCKWL} | | | | |

Note 1. t_{PCyc}: PCLKC cycle

Note 2. t_{BCyc}: PCLKB cycle

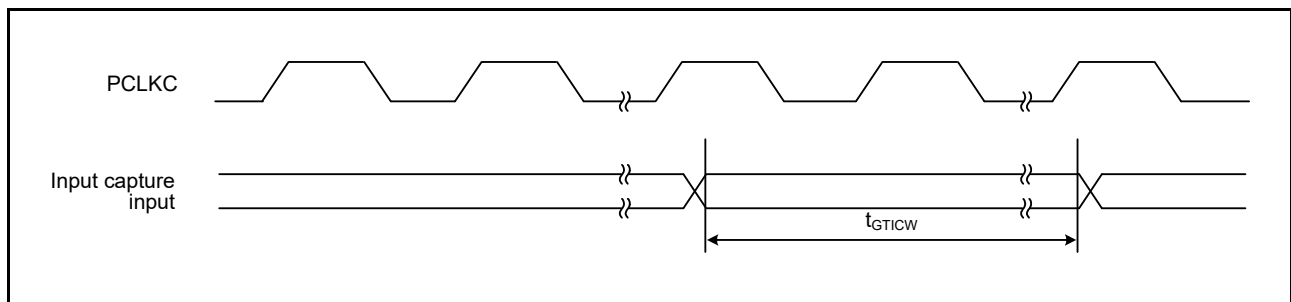


Figure 5.41 GPTW Input Capture Input Timing

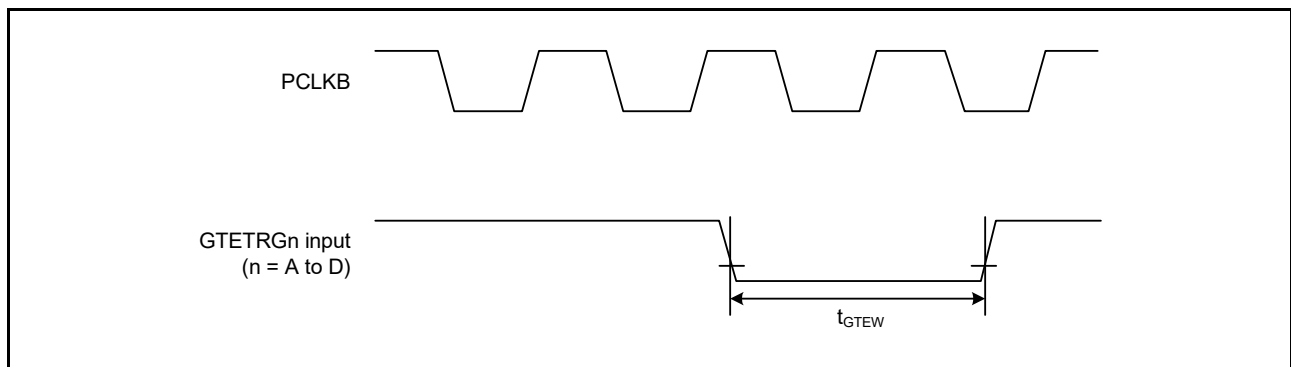


Figure 5.42 GPTW External Trigger Input Timing

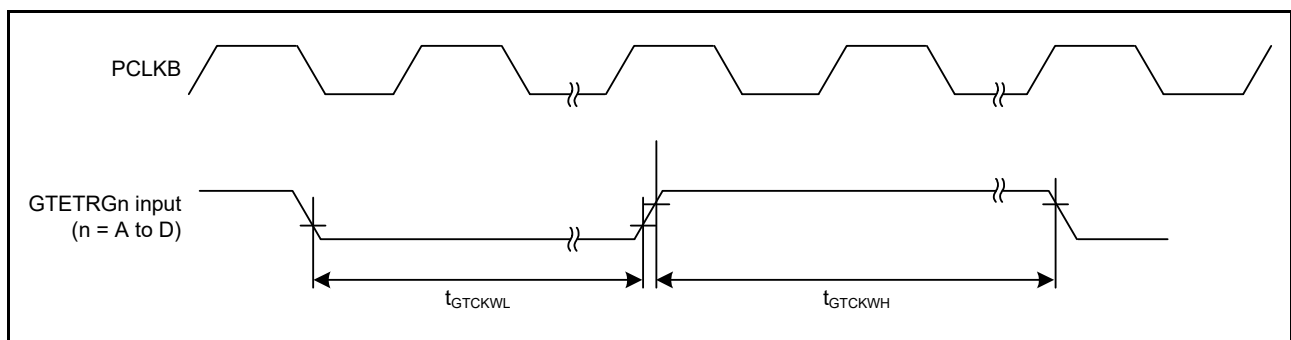


Figure 5.43 GPTW Clock Input Timing

Table 5.33 A/D Converter Trigger Timing

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V, $T_a = T_{opr}$,
 $ICLK = 8$ to 160 MHz, $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $PCLKC = 8$ to 160 MHz, $BCLK = 8$ to 60 MHz,
 Output load conditions: $V_{OH} = 0.5 \times V_{CC}$, $V_{OL} = 0.5 \times V_{CC}$, $C = 30$ pF,
 High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|---------------|---|------------|------|------|-------------|-----------------|
| A/D converter | A/D converter trigger input pulse width | t_{TRGW} | 1.5 | — | t_{PBcyc} | Figure 5.44 |

Note 1. t_{PBcyc} : PCLKB cycle

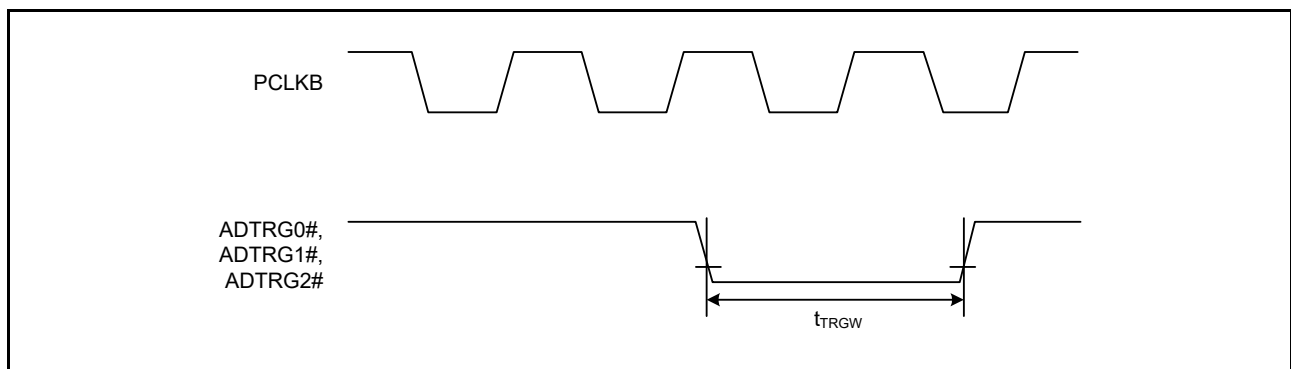


Figure 5.44 A/D Converter Trigger Input Timing

Table 5.34 CAC Timing

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V, $T_a = T_{opr}$,
 $ICLK = 8$ to 160 MHz, $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $PCLKC = 8$ to 160 MHz, $BCLK = 8$ to 60 MHz,
 Output load conditions: $V_{OH} = 0.5 \times V_{CC}$, $V_{OL} = 0.5 \times V_{CC}$, $C = 30$ pF,
 High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item*1, *2 | | Symbol | Min.*1, *2 | Max. | Unit | Test Conditions |
|------------|--------------------------|--------------------------|--------------|-----------------------------|-----------------------------|-----------------|
| CAC | CACREF input pulse width | $t_{PBcyc} \leq t_{cac}$ | t_{CACREF} | $4.5 t_{cac} + 3 t_{PBcyc}$ | — | ns |
| | | | | $t_{PBcyc} > t_{cac}$ | $5 t_{cac} + 6.5 t_{PBcyc}$ | |

Note 1. t_{PBcyc} : PCLKB cycle

Note 2. t_{cac} : CAC count clock source cycle

Table 5.35 SCJ, SCJh, and SCJi Timing

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V, $T_a = T_{opr}$,
 $ICLK = 8$ to 160 MHz, $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $PCLKC = 8$ to 160 MHz, $BCLK = 8$ to 60 MHz,
 Output load conditions: $V_{OH} = 0.5 \times V_{CC}$, $V_{OL} = 0.5 \times V_{CC}$, $C = 30$ pF,
 High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions | | | |
|-------------------------|--------------------------|-------------------|------------|------|------------------|---------------------|-------------|---------------------|-------------|
| SCJ, SCJh | Input clock cycle | Asynchronous | t_{Scyc} | 4 | — | t_{PBcyc} | Figure 5.45 | | |
| | | Clock synchronous | | 6 | — | | | | |
| | Input clock pulse width | | t_{SCKW} | 0.4 | 0.6 | t_{Scyc} | | | |
| | Input clock rise time | | t_{SCKr} | — | 5 | ns | | | |
| | Input clock fall time | | t_{SCKf} | — | 5 | ns | | | |
| | Output clock cycle | Asynchronous*2 | t_{Scyc} | 8 | — | t_{PBcyc} | | | |
| | | Clock synchronous | | 4 | — | | | | |
| | Output clock pulse width | | t_{SCKW} | 0.4 | 0.6 | t_{Scyc} | | | |
| | Output clock rise time | | t_{SCKr} | — | 5 | ns | | | |
| | Output clock fall time | | t_{SCKf} | — | 5 | ns | | | |
| | Transmit data delay time | Clock synchronous | t_{TXD} | — | 28 | ns | | $V_{CC} \geq 4.5$ V | Figure 5.46 |
| | | | | — | 33 | | | $V_{CC} < 4.5$ V | |
| | Receive data setup time | Clock synchronous | t_{RXS} | 15 | — | ns | | $V_{CC} \geq 4.5$ V | Figure 5.46 |
| 20 | | | | — | $V_{CC} < 4.5$ V | | | | |
| Receive data hold time | Clock synchronous | t_{RXH} | 5 | — | ns | Figure 5.46 | | | |
| SCJi | Input clock cycle | Asynchronous | t_{Scyc} | 4 | — | t_{PAcyc} | Figure 5.45 | | |
| | | Clock synchronous | | 6 | — | | | | |
| | Input clock pulse width | | t_{SCKW} | 0.4 | 0.6 | t_{Scyc} | | | |
| | Input clock rise time | | t_{SCKr} | — | 5 | ns | | | |
| | Input clock fall time | | t_{SCKf} | — | 5 | ns | | | |
| | Output clock cycle | Asynchronous*2 | t_{Scyc} | 6 | — | t_{PAcyc} | | | |
| | | Clock synchronous | | 4 | — | | | | |
| | Output clock pulse width | | t_{SCKW} | 0.4 | 0.6 | t_{Scyc} | | | |
| | Output clock rise time | | t_{SCKr} | — | 5 | ns | | | |
| | Output clock fall time | | t_{SCKf} | — | 5 | ns | | | |
| | Transmit data delay time | Master | t_{TXD} | — | 15 | ns | | $V_{CC} \geq 4.5$ V | Figure 5.46 |
| | | Slave | | — | 28 | | | | |
| | | Master | | — | 20 | | | $V_{CC} < 4.5$ V | |
| Slave | | — | | 33 | | | | | |
| Receive data setup time | Clock synchronous | t_{RXS} | 15 | — | ns | $V_{CC} \geq 4.5$ V | Figure 5.46 | | |
| | | | 20 | — | | $V_{CC} < 4.5$ V | | | |
| Receive data hold time | Clock synchronous | t_{RXH} | 5 | — | ns | Figure 5.46 | | | |

Note 1. t_{PBcyc} : PCLKB cycle; t_{PAcyc} : PCLKA cycle

Note 2. When the SEMR.ABCS and SEMR.BGDM bits are set to 1

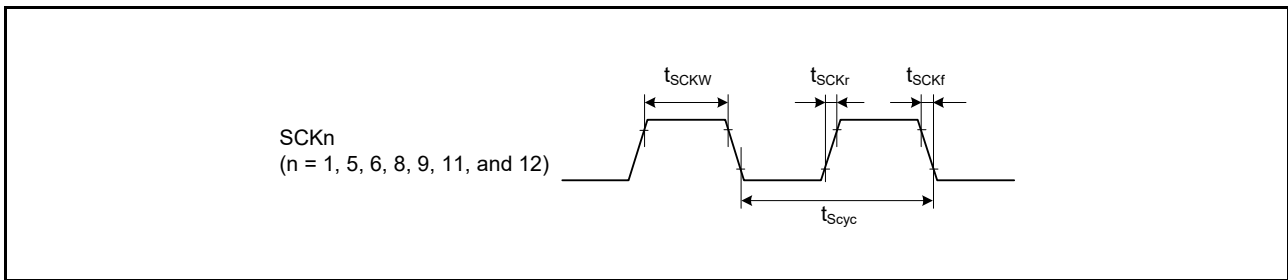


Figure 5.45 SCK Clock Input Timing

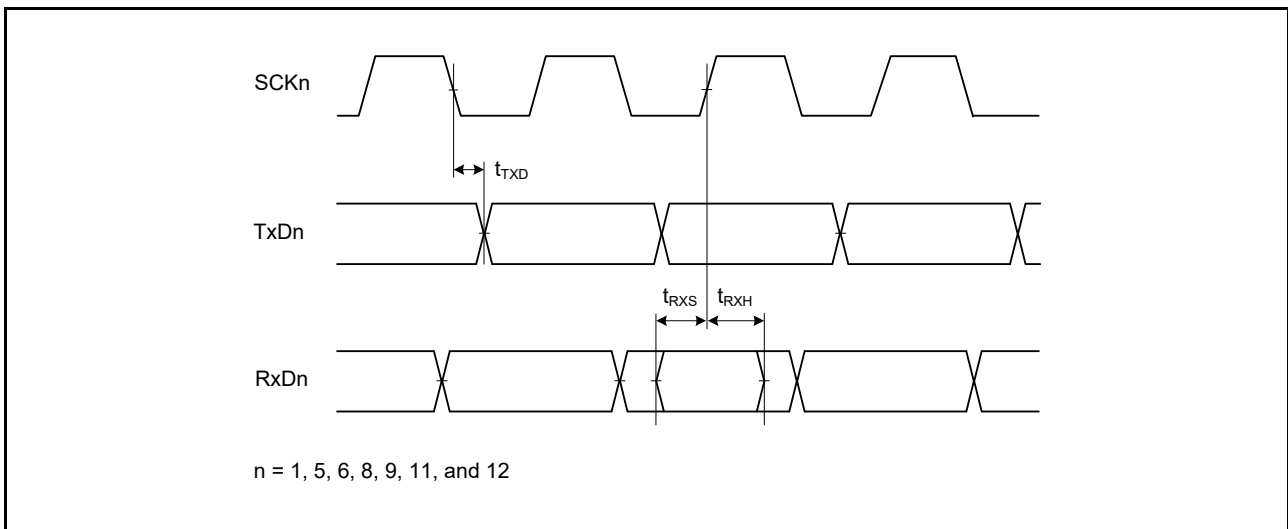


Figure 5.46 SCI Input/Output Timing: Clock Synchronous Mode

Table 5.36 RSPI Timing

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V, $T_a = T_{opr}$,
 $ICLK = 8$ to 160 MHz, $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $PCLKC = 8$ to 160 MHz, $BCLK = 8$ to 60 MHz,
Output load conditions: $V_{OH} = 0.5 \times V_{CC}$, $V_{OL} = 0.5 \times V_{CC}$, $C = 30$ pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | | Symbol | Min.*1 | Max.*1 | Unit*1 | Test Conditions | | | | | | | | | |
|------------------------------------|------------------------------|----------------------------|--|---|-------------|------------------|-------------|--|---|---|----------------------------|----------------|--|-----------------------------|-------------------------------|
| RSPI | RSPCK clock cycle | Master | t_{SPcyc} | 2 | 4096 | t_{PAcyc} | Figure 5.47 | | | | | | | | |
| | | Slave | | 4 | — | | | | | | | | | | |
| | RSPCK clock high pulse width | Master | t_{SPCKWH} | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | — | ns | | | | | | | | | |
| | | Slave | | | | | | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$ | — | ns | | | | |
| | RSPCK clock low pulse width | Master | t_{SPCKWL} | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2 - 3$ | — | ns | | | | | | | | | |
| | | Slave | | | | | | | | $(t_{SPcyc} - t_{SPCKr} - t_{SPCKf}) / 2$ | — | ns | | | |
| | RSPCK clock rise/fall time | Output | t_{SPCKr} , t_{SPCKf} | — | 5 | ns | | | | | | | | | |
| | | Input | | — | 1 | μ s | | | | | | | | | |
| | Data input setup time | Master | t_{SU} | 6 | — | ns | | | | | $V_{CC} \geq 4.5$ V | Figure 5.48 to | | | |
| | | | | 11 | — | | | | | | $V_{CC} < 4.5$ V | Figure 5.53 | | | |
| | | Slave | | 8.3 | — | ns | | | | | Figure 5.48 to Figure 5.53 | | | | |
| | Data input hold time | Master | PCLKA division ratio set to 1/2 | t_{HF} | 0 | ns | | | | | | | | | |
| | | | PCLKA division ratio set to a value other than 1/2 | t_H | t_{PAcyc} | | | | | | | — | | | |
| | | Slave | | | 8.3 | — | | | | | | | | | |
| | SSL setup time | Master | t_{LEAD} | 1 | 8 | t_{SPcyc} | | | | | | | | | |
| | | Slave | | 6 | — | t_{PAcyc} | | | | | | | | | |
| | SSL hold time | Master | t_{LAG} | 1 | 8 | t_{SPcyc} | | | | | | | | | |
| | | Slave | | 6 | — | t_{PAcyc} | | | | | | | | | |
| | Data output delay time | Master | t_{OD} | — | 6.3 | ns | | | | | | | | $V_{CC} \geq 4.5$ V | Figure 5.48 to Figure 5.53 |
| | | Slave | | — | 28 | | | | | | | | | | |
| Master | | — | | 11.3 | ns | $V_{CC} < 4.5$ V | | | | | | | | | |
| Slave | | — | | 33 | | | | | | | | | | | |
| Data output hold time | Master | t_{OH} | 0 | — | ns | | | | | | | | | | |
| | Slave | | 0 | — | | | | | | | | | | | |
| Successive transmission delay time | Master | t_{TD} | $t_{SPcyc} + 2 \times t_{PAcyc}$ | $8 \times t_{SPcyc} + 2 \times t_{PAcyc}$ | ns | | | | | | | | | | |
| | Slave | | $6 \times t_{PAcyc}$ | — | | | | | | | | | | | |
| MOSI and MISO rise/fall time | Output | t_{Dr} , t_{Df} | — | 5 | ns | | | | | | | | | | |
| | Input | | — | 1 | | | | | μ s | | | | | | |
| SSL rise/fall time | Output | t_{SSLr} , t_{SSLf} | — | 5 | ns | | | | | | | | | | |
| | Input | | — | 1 | | | | | | μ s | | | | | |
| Slave access time | | t_{SA} | — | $2 \times t_{PAcyc} + 28$ | ns | | | | | $V_{CC} \geq 4.5$ V | | | | Figure 5.52, Figure 5.53 | |
| | | | — | $2 \times t_{PAcyc} + 33$ | | | | | | $V_{CC} < 4.5$ V | | | | | |
| Slave output release time | | t_{REL} | — | $2 \times t_{PAcyc} + 28$ | ns | | | | | $V_{CC} \geq 4.5$ V | | | | | |
| | | | — | $2 \times t_{PAcyc} + 33$ | | | | | | $V_{CC} < 4.5$ V | | | | | |

Note 1. t_{PAcyc} : PCLKA cycle

Table 5.37 Simple SPI Timing

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V, $T_a = T_{opr}$,
 $ICLK = 8$ to 160 MHz, $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $PCLKC = 8$ to 160 MHz, $BCLK = 8$ to 60 MHz,
Output load conditions: $V_{OH} = 0.5 \times V_{CC}$, $V_{OL} = 0.5 \times V_{CC}$, $C = 30$ pF,
High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | | Symbol | Min. | Max. | Unit*1 | Test Conditions |
|--|---------------------------------|---------------------------|------|-------|-------------|----------------------------|
| Simple SPI (SCI11) | SCK clock cycle output (master) | t_{SPcyc} | 4 | 65536 | t_{PAcyc} | Figure 5.47 |
| | SCK clock cycle input (slave) | | 8 | — | | |
| | SCK clock high pulse width | t_{SPCKWH} | 0.4 | 0.6 | t_{SPcyc} | |
| | SCK clock low pulse width | t_{SPCKWL} | 0.4 | 0.6 | t_{SPcyc} | |
| | SCK clock rise/fall time | t_{SPCKr} , t_{SPCKf} | — | 20 | ns | |
| | Data input setup time | t_{SU} | 33.3 | — | ns | Figure 5.48 to Figure 5.53 |
| | Data input hold time | t_H | 33.3 | — | ns | |
| | SS input setup time | t_{LEAD} | 1 | — | t_{SPcyc} | |
| | SS input hold time | t_{LAG} | 1 | — | t_{SPcyc} | |
| | Data output delay time | t_{OD} | — | 33.3 | ns | |
| | Data output hold time | t_{OH} | -10 | — | ns | |
| | Data rise/fall time | t_{Dr} , t_{Df} | — | 16.6 | ns | |
| | SS input rise/fall time | t_{SSLr} , t_{SSLf} | — | 16.6 | ns | |
| | Slave access time | t_{SA} | — | 7 | t_{PAcyc} | Figure 5.52, Figure 5.53 |
| | Slave output release time | t_{REL} | — | 7 | t_{PAcyc} | |
| Simple SPI (SCI1, SCI5, SCI6, SCI8, SCI9, SCI12) | SCK clock cycle output (master) | t_{SPcyc} | 4 | 65536 | t_{PBcyc} | Figure 5.47 |
| | SCK clock cycle input (slave) | | 8 | — | | |
| | SCK clock high pulse width | t_{SPCKWH} | 0.4 | 0.6 | t_{SPcyc} | |
| | SCK clock low pulse width | t_{SPCKWL} | 0.4 | 0.6 | t_{SPcyc} | |
| | SCK clock rise/fall time | t_{SPCKr} , t_{SPCKf} | — | 20 | ns | |
| | Data input setup time | t_{SU} | 33.3 | — | ns | Figure 5.48 to Figure 5.53 |
| | Data input hold time | t_H | 33.3 | — | ns | |
| | SS input setup time | t_{LEAD} | 1 | — | t_{SPcyc} | |
| | SS input hold time | t_{LAG} | 1 | — | t_{SPcyc} | |
| | Data output delay time | t_{OD} | — | 33.3 | ns | |
| | Data output hold time | t_{OH} | -10 | — | ns | |
| | Data rise/fall time | t_{Dr} , t_{Df} | — | 16.6 | ns | |
| | SS input rise/fall time | t_{SSLr} , t_{SSLf} | — | 16.6 | ns | |
| | Slave access time | t_{SA} | — | 7 | t_{PBcyc} | Figure 5.52, Figure 5.53 |
| | Slave output release time | t_{REL} | — | 7 | t_{PBcyc} | |

Note 1. t_{PAcyc} : PCLKA cycle, t_{PBcyc} : PCLKB cycle

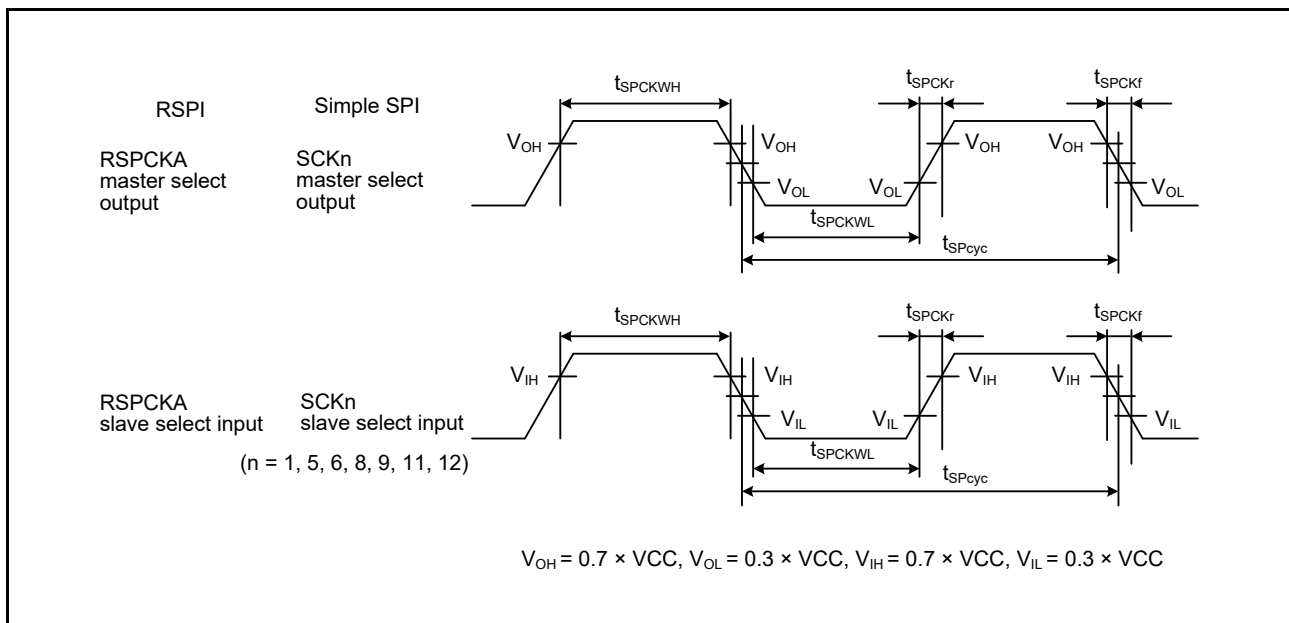


Figure 5.47 RSPI Clock Timing and Simple SPI Clock Timing

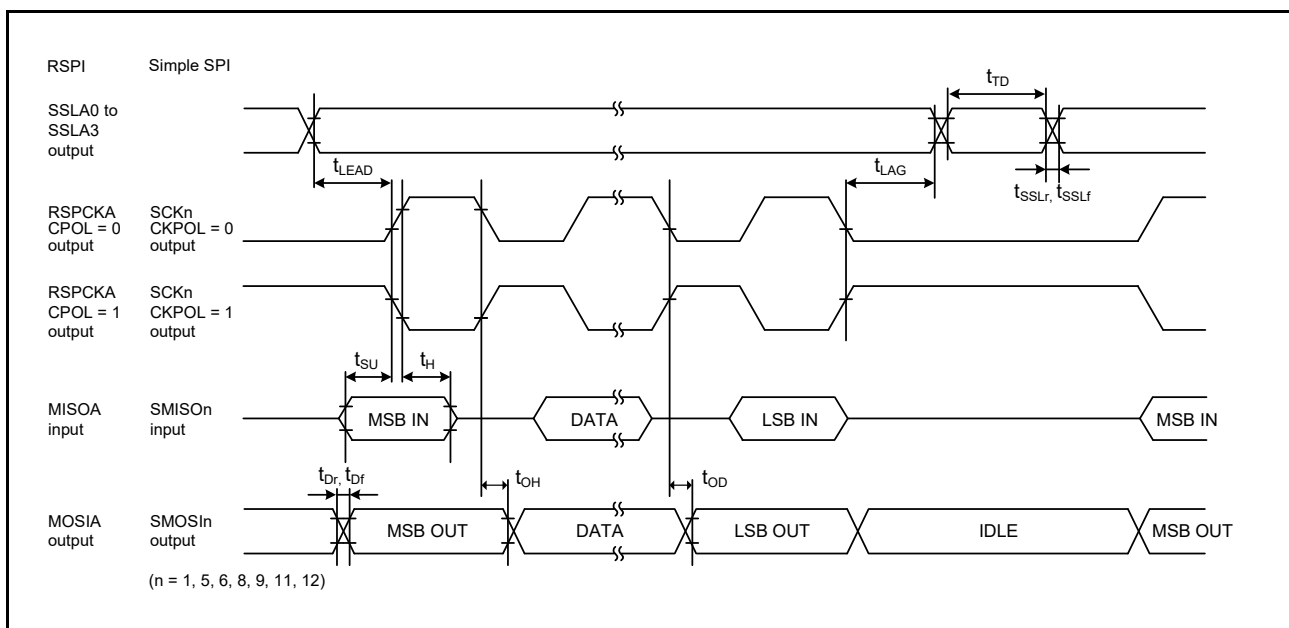


Figure 5.48 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 1)

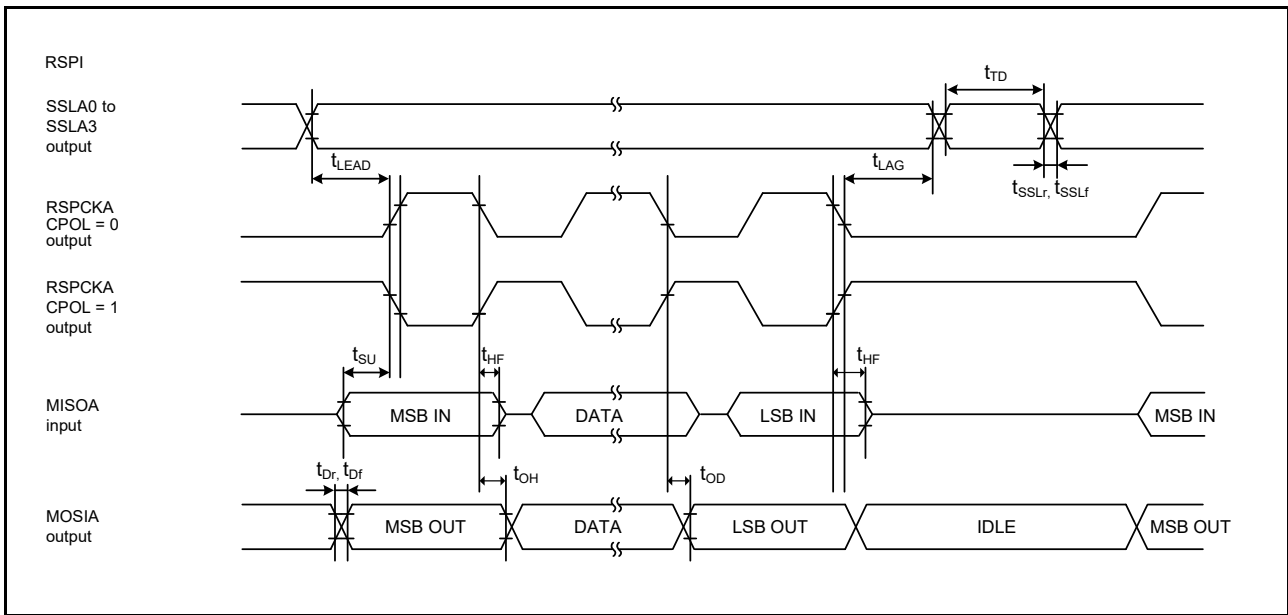


Figure 5.49 RSPI Timing (Master, CPHA = 0) (Bit Rate: PCLKA Division Ratio Set to 1/2)

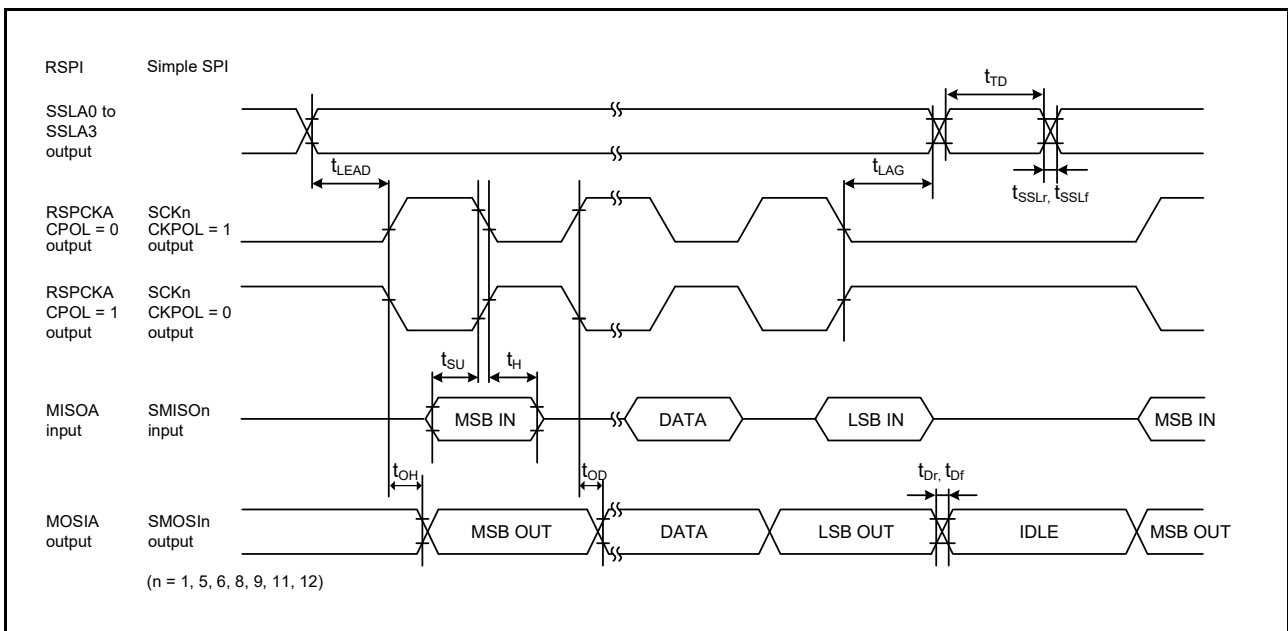


Figure 5.50 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to a Value Other Than 1/2) and Simple SPI Timing (Master, CKPH = 0)

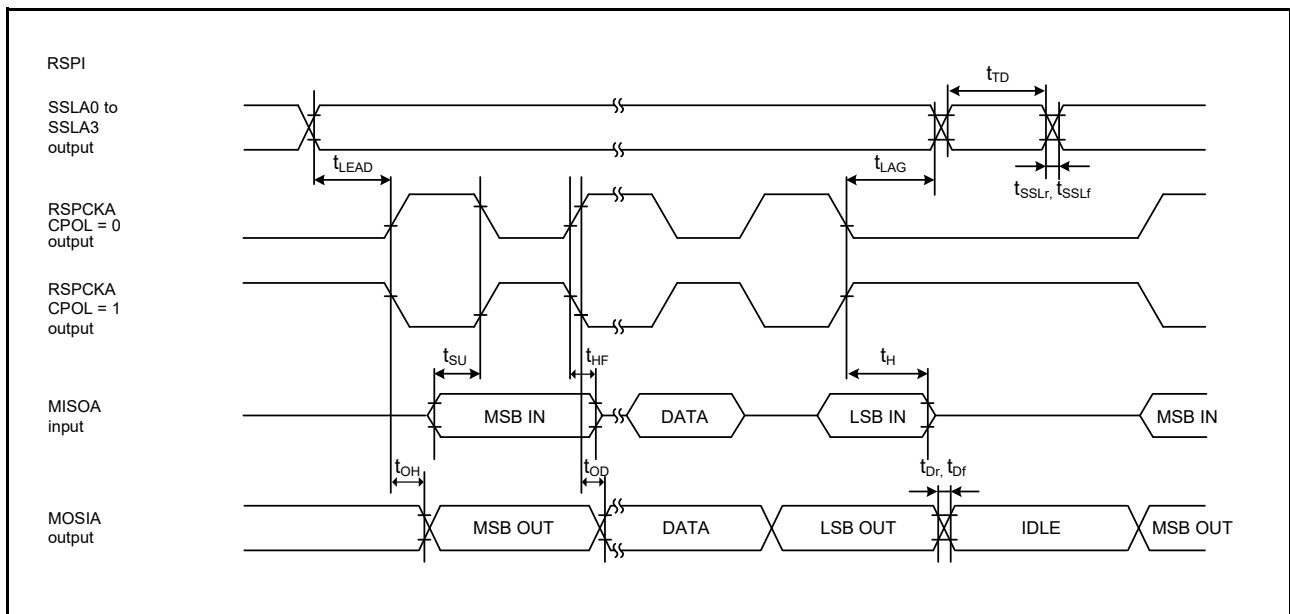


Figure 5.51 RSPI Timing (Master, CPHA = 1) (Bit Rate: PCLKA Division Ratio Set to 1/2)

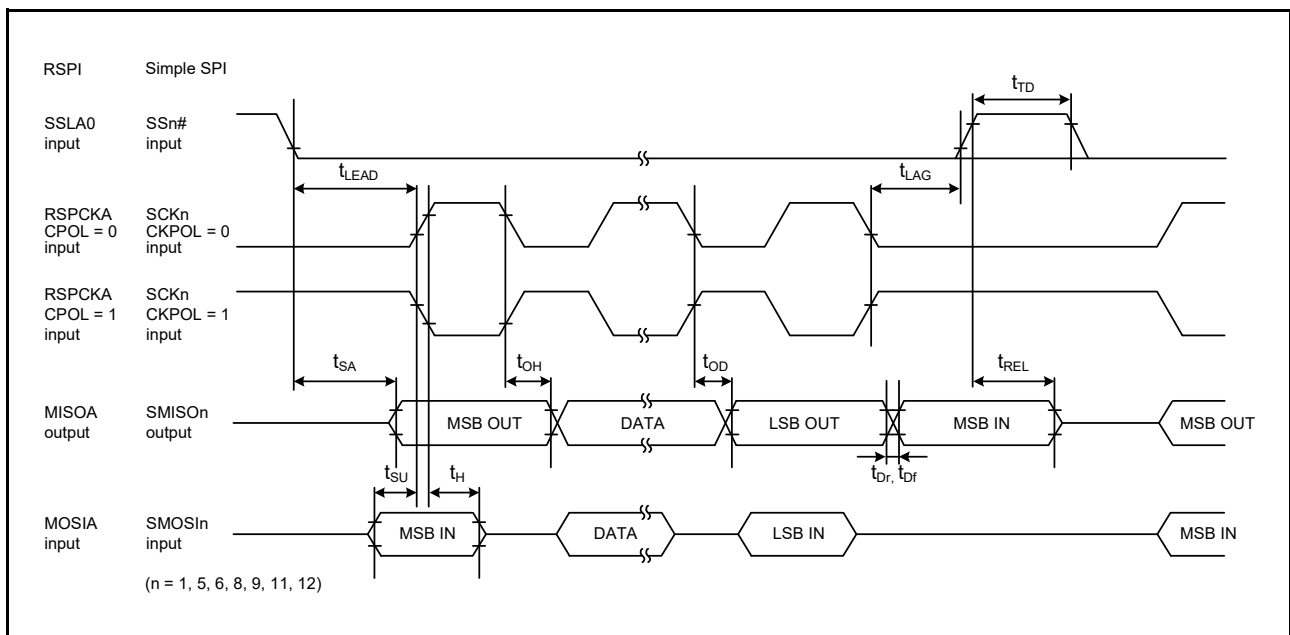


Figure 5.52 RSPI Timing (Slave, CPHA = 0) and Simple SPI Timing (Slave, CKPH = 1)

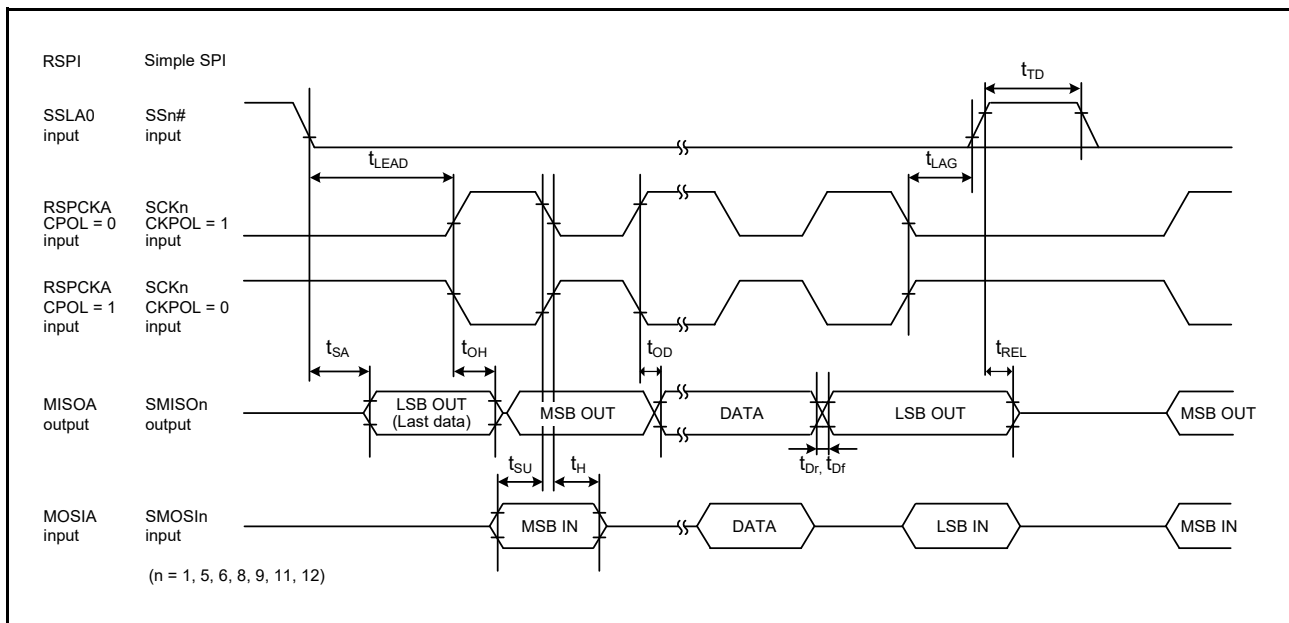


Figure 5.53 RSPI Timing (Slave, CPHA = 1) and Simple SPI Timing (Slave, CKPH = 0)

Table 5.38 RIIC Timing

Conditions: $VCC = 2.7$ to 5.5 V, $VCC_USB = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0$ V, $T_a = T_{opr}$,
 $ICLK = 8$ to 160 MHz, $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $PCLKC = 8$ to 160 MHz, $BCLK = 8$ to 60 MHz,
 High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | | Symbol *2 | Min.*1 | Max.*1 | Unit | Test Conditions*3 |
|-----------------------------------|---|--------------|--|--------------------------|------|----------------------|
| RIIC (Standard-mode, SMBus) | SCL input cycle time | t_{SCL} | $6(12) \times t_{IICcyc} + 1300$ | — | ns | Figure 5.54 |
| | SCL input high pulse width | t_{SCLH} | $3(6) \times t_{IICcyc} + 300$ | — | | |
| | SCL input low pulse width | t_{SCLL} | $3(6) \times t_{IICcyc} + 300$ | — | | |
| | SCL, SDA input rise time | t_{Sr} | — | 1000 | | |
| | SCL, SDA input fall time | t_{Sf} | — | 300 | | |
| | SCL, SDA input spike pulse removal time | t_{SP} | 0 | $1(4) \times t_{IICcyc}$ | | |
| | SDA input bus free time | t_{BUF} | $3(6) \times t_{IICcyc} + 300$ | — | | |
| | Start condition input hold time | t_{STAH} | $t_{IICcyc} + 300$ | — | | |
| | Restart condition input setup time | t_{STAS} | 1000 | — | | |
| | Stop condition input setup time | t_{STOS} | 1000 | — | | |
| | Data input setup time | t_{SDAS} | $t_{IICcyc} + 50$ | — | | |
| | Data input hold time | t_{SDAH} | 0 | — | | |
| | SCL, SDA capacitive load | C_b | — | 400 | pF | |
| RIIC (Fast-mode) | SCL input cycle time | t_{SCL} | $6(12) \times t_{IICcyc} + 600$ | — | ns | |
| | SCL input high pulse width | t_{SCLH} | $3(6) \times t_{IICcyc} + 300$ | — | | |
| | SCL input low pulse width | t_{SCLL} | $3(6) \times t_{IICcyc} + 300$ | — | | |
| | SCL, SDA input rise time | t_{Sr} | $20 \times (\text{External pull-up voltage}/5.5V)$ | 300 | | |
| | SCL, SDA input fall time | t_{Sf} | $20 \times (\text{External pull-up voltage}/5.5V)$ | 300 | | |
| | SCL, SDA input spike pulse removal time | t_{SP} | 0 | $1(4) \times t_{IICcyc}$ | | |
| | SDA input bus free time | t_{BUF} | $3(6) \times t_{IICcyc} + 300$ | — | | |
| | Start condition input hold time | t_{STAH} | $t_{IICcyc} + 300$ | — | | |
| | Restart condition input setup time | t_{STAS} | 300 | — | | |
| | Stop condition input setup time | t_{STOS} | 300 | — | | |
| | Data input setup time | t_{SDAS} | $t_{IICcyc} + 50$ | — | | |
| | Data input hold time | t_{SDAH} | 0 | — | | |
| | SCL, SDA capacitive load | C_b | — | 400 | pF | |

Note: t_{IICcyc} : RIIC internal reference clock (IIC ϕ) cycle

Note 1. The value within parentheses is applicable when the value of the ICMR3.NF[1:0] bits is 11b while the digital filter is enabled by the setting ICFER.NFE = 1.

Note 2. C_b is the total capacitance of the bus lines.

Note 3. When $VCC \geq 4.5V$, VOLSR.RICVLS = 0
 When $VCC < 4.5V$, VOLSR.RICVLS = 1

Table 5.39 Simple IIC Timing

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V, $T_a = T_{opr}$,
 $ICLK = 8$ to 160 MHz, $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $PCLKC = 8$ to 160 MHz, $BCLK = 8$ to 60 MHz,
 High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | | Symbol*1 | Min. | Max.*2 | Unit | Test Conditions |
|-------------------------------|---|------------|------|---------------------|------|-----------------|
| Simple IIC (Standard-mode) | SSDA input rise time | t_{Sr} | — | 1000 | ns | Figure 5.54 |
| | SSDA input fall time | t_{Sf} | — | 300 | | |
| | SSCL, SSDA input spike pulse removal time | t_{SP} | 0 | $4 \times t_{Pcyc}$ | | |
| | Data input setup time | t_{SDAS} | 250 | — | | |
| | Data input hold time | t_{SDAH} | 0 | — | | |
| | SSCL, SSDA capacitive load | C_b | — | 400 | pF | |
| Simple IIC (Fast-mode) | SSDA input rise time | t_{Sr} | — | 300 | ns | Figure 5.54 |
| | SSDA input fall time | t_{Sf} | — | 300 | | |
| | SSCL, SSDA input spike pulse removal time | t_{SP} | 0 | $4 \times t_{Pcyc}$ | | |
| | Data input setup time | t_{SDAS} | 100 | — | | |
| | Data input hold time | t_{SDAH} | 0 | — | | |
| | SSCL, SSDA capacitive load | C_b | — | 400 | pF | |

Note 1. C_b is the total capacitance of the bus lines.

Note 2. t_{Pcyc} : For SCI11, this is the period of PCLKA, and for SCI1, 5, 6, 8, 9, and 12, this is the period of PCLKB.

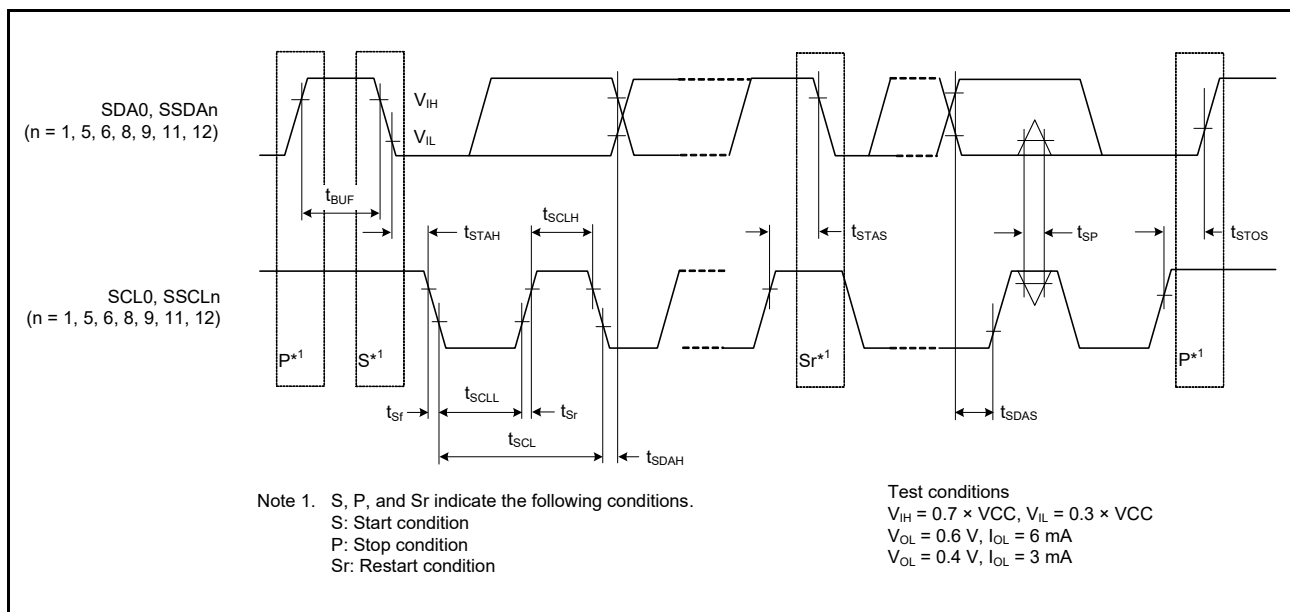


Figure 5.54 RIIC Bus Interface Input/Output Timing and Simple IIC Bus Interface Input/Output Timing

Table 5.40 HRPWM Timing

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,

$V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V, $T_a = T_{opr}$,

$ICLK = 8$ to 160 MHz, $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz, $PCLKC = 8$ to 160 MHz, $BCLK = 8$ to 60 MHz,

Output load conditions: $V_{OH} = 0.5 \times V_{CC}$, $V_{OL} = 0.5 \times V_{CC}$, $C = 30$ pF,

High-drive output is selected by the driving ability control register (other than for P53 to P55 and P60 to P65).

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|------------------------------|------|-----------|------|------|--------------------|
| Input frequency (f_{IN}) | 80 | — | 160 | MHz | |
| Resolution | — | 195 | — | ps | $f_{IN} = 160$ MHz |
| DNL*1 | — | ± 2.0 | — | LSB | |

Note 1. The value is that difference from code to code normalized by the resolution (1 LSB).

5.5 USB Characteristics

Table 5.41 On-Chip USB Low Speed (Host Only) Characteristics (DP and DM Pin Characteristics)

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 3.0$ to 3.6 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V, $T_a = T_{opr}$,
 $UCLK = 48$ MHz, $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz

| Item | Symbol | Min. | Max. | Unit | Test Conditions | |
|---------------------------|--|-------------------|-------|-------|-----------------|-----------------------|
| Input characteristics | Input high-level voltage | V_{IH} | 2.0 | — | V | |
| | Input low-level voltage | V_{IL} | — | 0.8 | V | |
| | Differential input sensitivity | V_{DI} | 0.2 | — | V | DP – DM |
| | Differential common mode range | V_{CM} | 0.8 | 2.5 | V | |
| Output characteristics | Output high-level voltage | V_{OH} | 2.8 | 3.6 | V | $I_{OH} = -200 \mu A$ |
| | Output low-level voltage | V_{OL} | 0.0 | 0.3 | V | $I_{OL} = 2$ mA |
| | Cross-over voltage | V_{CRS} | 1.3 | 2.0 | V | Figure 5.55 |
| | Rise time | t_{LR} | 75 | 300 | ns | t_{LR} / t_{LF} |
| | Fall time | t_{LF} | 75 | 300 | ns | |
| | Rise/fall time ratio | t_{LR} / t_{LF} | 80 | 125 | % | |
| Pull-down characteristics | DP/DM pull-down resistance (when the host controller function is selected) | R_{pd} | 14.25 | 24.80 | k Ω | |

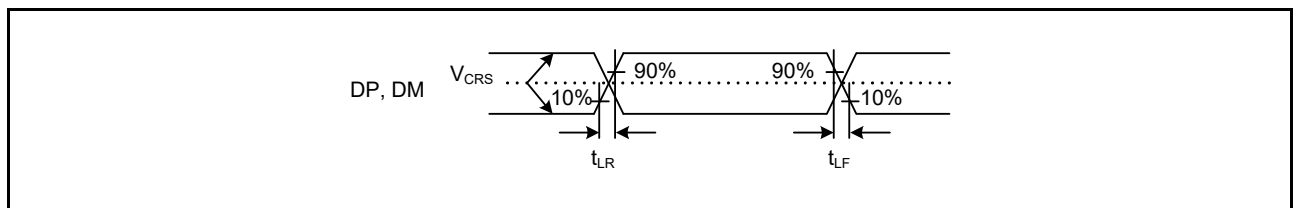


Figure 5.55 DP and DM Output Timing (Low Speed)

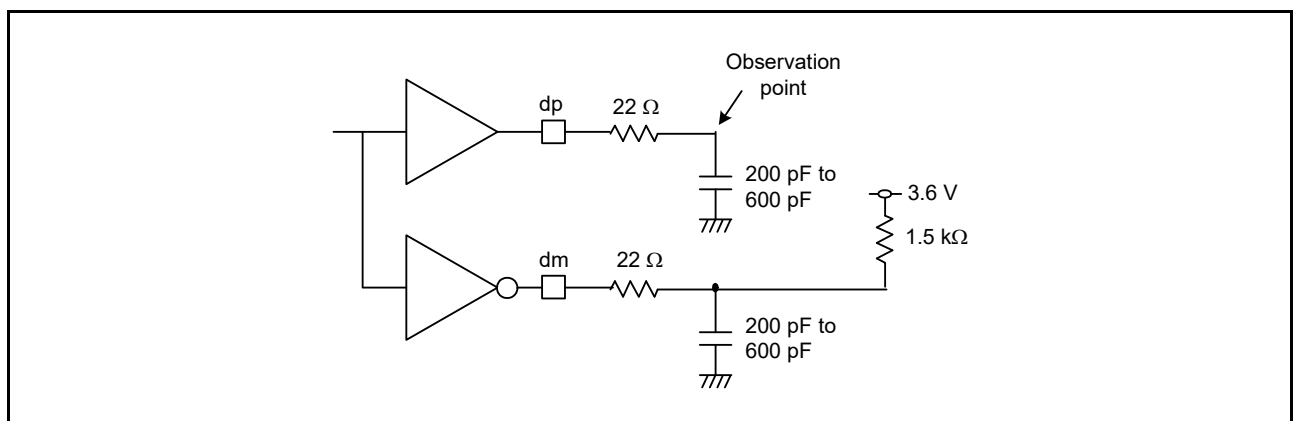


Figure 5.56 Test Circuit (Low Speed)

Table 5.42 On-Chip USB Full-Speed Characteristics (DP and DM Pin Characteristics)

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 3.0$ to 3.6 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V, $T_a = T_{opr}$,
 $UCLK = 48$ MHz, $PCLKA = 8$ to 120 MHz, $PCLKB = 8$ to 60 MHz

| | Item | Symbol | Min. | Max. | Unit | Test Conditions |
|---------------------------------------|---|-------------------|-------|--------|------------|-------------------------------|
| Input characteristics | Input high-level voltage | V_{IH} | 2.0 | — | V | |
| | Input low-level voltage | V_{IL} | — | 0.8 | V | |
| | Differential input sensitivity | V_{DI} | 0.2 | — | V | DP – DM |
| | Differential common mode range | V_{CM} | 0.8 | 2.5 | V | |
| Output characteristics | Output high-level voltage | V_{OH} | 2.8 | 3.6 | V | $I_{OH} = -200 \mu A$ |
| | Output low-level voltage | V_{OL} | 0.0 | 0.3 | V | $I_{OL} = 2$ mA |
| | Cross-over voltage | V_{CRS} | 1.3 | 2.0 | V | Figure 5.57 |
| | Rise time | t_{FR} | 4 | 20 | ns | |
| | Fall time | t_{FF} | 4 | 20 | ns | |
| | Rise/fall time ratio | t_{FR} / t_{FF} | 90 | 111.11 | % | t_{FR} / t_{FF} |
| | Output resistance | Z_{DRV} | 28 | 44 | Ω | $R_s = 22 \Omega$ included |
| Pull-up and pull-down characteristics | DP pull-up resistance (when the function controller function is selected) | R_{pu} | 0.900 | 1.575 | k Ω | Idle state |
| | | | 1.425 | 3.090 | k Ω | At transmission and reception |
| | DP/DM pull-down resistance (when the host controller function is selected) | R_{pd} | 14.25 | 24.80 | k Ω | |

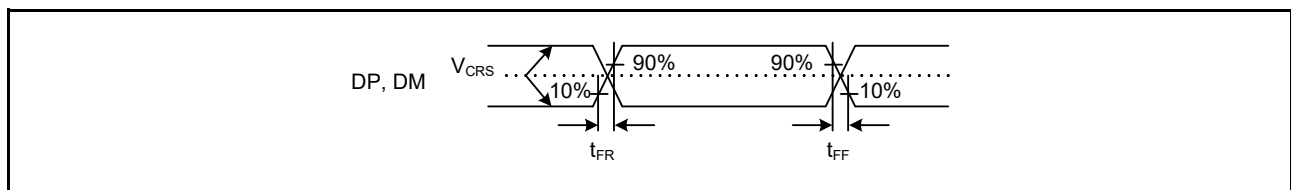


Figure 5.57 DP and DM Output Timing (Full-Speed)

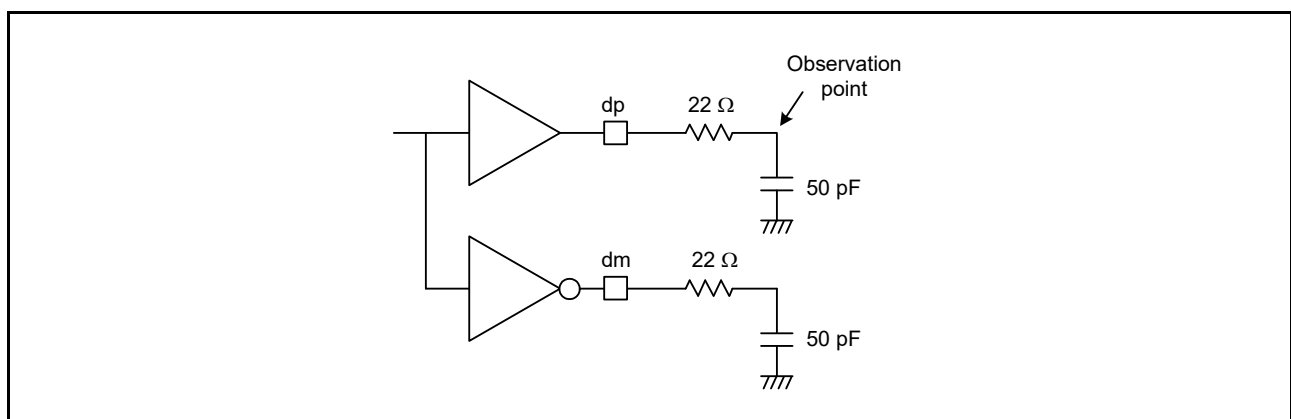


Figure 5.58 Test Circuit (Full-Speed)

5.6 A/D Conversion Characteristics

Table 5.43 12-Bit A/D (Unit 0, 1, 2) Conversion Characteristics (1)

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, 4.5 V \leq AVCC0 = AVCC1 = AVCC2 \leq 5.5V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V, $T_a = T_{opr}$, PCLKB = PCLKD = 8 to 60 MHz*1,
 Source impedance = 1.0 k Ω

| Item | | | | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---|---|----------------------------------|-----------|----------------|---------------------------|--|---|
| Resolution | | | | 12 | 12 | 12 | Bit | |
| Analog input capacitance | | | | — | — | 30 | pF | |
| Conversion time*2 (Operation at PCLKD = 60 MHz) | AN000 to AN002, AN100 to AN102 | Channel-dedicated sample-and-hold circuits in use | Constant sampling enabled | 1.00 | — | — | μ s | • Sampling time: 24 PCLKD |
| | | | Constant sampling disabled | 1.40 | — | — | | • Sampling time of channel-dedicated sample-and-hold circuits: 24 PCLKD • Sampling time: 24 PCLKD |
| | | Channel-dedicated sample-and- hold circuits not in use | | 0.90 | — | — | | • Sampling time: 30 PCLKD |
| | AN003 to AN006, AN103 to AN106 | | 0.90 | — | — | • Sampling time: 30 PCLKD | | |
| | AN007, AN107, AN200 to AN211 | | 0.95 | — | — | • Sampling time: 33 PCLKD | | |
| | AN216 to AN217 | | 1.05 | — | — | • Sampling time: 39 PCLKD | | |
| Offset error | Channel-dedicated sample-and- hold circuits in use | | — | \pm 1.5 | \pm 6.0 | LSB | AN000 to AN002, AN100 to AN102 = 0.2 V | |
| | Channel-dedicated sample-and- hold circuits not in use | | — | \pm 1.5 | \pm 5.0 | | | |
| Full-scale error | Channel-dedicated sample-and- hold circuits in use | | — | \pm 1.5 | \pm 5.5 | | AN000 to AN002 = AVCC0 – 0.2 V AN100 to AN102 = AVCC1 – 0.2 V | |
| | Channel-dedicated sample-and- hold circuits not in use | | — | \pm 1.5 | \pm 4.5 | | | |
| Quantization error | Channel-dedicated sample-and- hold circuits in use | | — | \pm 0.5 | — | | | |
| | Channel-dedicated sample-and- hold circuits not in use | | — | \pm 0.5 | — | | | |
| Absolute accuracy | AN000 to AN002, AN100 to AN102 | Channel-dedicated sample-and- hold circuits in use | — | \pm 3.0 | \pm 6.0 | | | |
| | | Channel-dedicated sample-and- hold circuits not in use | — | \pm 2.5 | \pm 5.5 | | | |
| | AN003 to AN007, AN103 to AN107 | | — | \pm 2.5 | \pm 5.5 | | | |
| | AN200 to AN211 | | — | \pm 2.5 | \pm 5.5 | | | |
| AN216 to AN217 | | — | \pm 2.5 | \pm 6.5 | | | | |
| DNL differential nonlinearity error | Channel-dedicated sample-and- hold circuits in use | | — | \pm 1.0 | \pm 2.5 | | | |
| | Channel-dedicated sample-and- hold circuits not in use | | — | \pm 1.0 | \pm 1.5 | | | |
| INL integral nonlinearity error | Channel-dedicated sample-and- hold circuits in use | | — | \pm 1.5 | \pm 4.0 | | | |
| | Channel-dedicated sample-and- hold circuits not in use | | — | \pm 1.5 | \pm 2.5 | | | |
| Holding time of the channel-dedicated sample-and-hold circuit | | | | — | — | 20 | μ s | |
| Dynamic range | AN000 to AN002 | Channel-dedicated sample-and- hold circuits in use | 0.2 | — | AVCC0 – 0.2 | V | | |
| | AN100 to AN102 | Channel-dedicated sample-and- hold circuits in use | 0.2 | — | AVCC1 – 0.2 | | | |

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.

Note 1. When PCLKD was higher than 40 MHz, capacitors with the following values were placed in parallel with the 0.1- μ F capacitors between AVCC0 and AVSS0, AVCC1 and AVSS1, and AVCC2 and AVSS2 for measurement of the A/D conversion characteristics.

- Products with 64 Kbytes of RAM: 1000 pF
- Products with 128 Kbytes of RAM: 0.01 μ F

Note 2. The conversion time is the sum of the sampling time and the comparison time. The numbers of sampling-clock cycles are indicated as the test conditions.

Table 5.44 12-Bit A/D (Unit 0, 1, 2) Conversion Characteristics (2)

Conditions: $V_{CC} = 2.7$ to 4.5 V, $V_{CC_USB} = 2.7$ to 4.5 V, 3.0 V \leq $AV_{CC0} = AV_{CC1} = AV_{CC2} < 4.5$ V,
 $V_{SS} = V_{SS_USB} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0$ V, $T_a = T_{opr}$, $PCLKB = PCLKD = 8$ to 40 MHz,
 Source impedance = 1.0 k Ω

| Item | | | | Min. | Typ. | Max. | Unit | Test Conditions |
|--|-----------------------------------|---|----------------------------------|-----------|------------------|---------------------------|--|---|
| Resolution | | | | 12 | 12 | 12 | Bit | |
| Analog input capacitance | | | | — | — | 30 | pF | |
| Conversion time*1 (Operation at PCLKD = 40 MHz) | AN000 to AN002, AN100 to AN102 | Channel-dedicated sample-and-hold circuits in use | Constant sampling enabled | 1.35 | — | — | μ s | • Sampling time: 18 PCLKD |
| | | | Constant sampling disabled | 1.80 | — | — | | • Sampling time of channel-dedicated sample-and-hold circuits: 18 PCLKD • Sampling time: 18 PCLKD |
| | | Channel-dedicated sample-and- hold circuits not in use | | 1.13 | — | — | | • Sampling time: 21 PCLKD |
| | AN003 to AN006, AN103 to AN106 | | 1.13 | — | — | • Sampling time: 21 PCLKD | | |
| | AN007, AN107, AN200 to AN211 | | 1.20 | — | — | • Sampling time: 24 PCLKD | | |
| | AN216 to AN217 | | 1.28 | — | — | • Sampling time: 27 PCLKD | | |
| Offset error | | Channel-dedicated sample-and- hold circuits in use | — | ± 1.5 | ± 7.5 | LSB | AN000 to AN002, AN100 to AN102 = 0.2 V | |
| | | Channel-dedicated sample-and- hold circuits not in use | — | ± 1.5 | ± 6.5 | | | |
| Full-scale error | | Channel-dedicated sample-and- hold circuits in use | — | ± 1.5 | ± 7.5 | | AN000 to AN002 = $AV_{CC0} - 0.2$ V AN100 to AN102 = $AV_{CC1} - 0.2$ V | |
| | | Channel-dedicated sample-and- hold circuits not in use | — | ± 1.5 | ± 6.5 | | | |
| Quantization error | | Channel-dedicated sample-and- hold circuits in use | — | ± 0.5 | — | | | |
| | | Channel-dedicated sample-and- hold circuits not in use | — | ± 0.5 | — | | | |
| Absolute accuracy | AN000 to AN002, AN100 to AN102 | Channel-dedicated sample-and- hold circuits in use | — | ± 4.0 | ± 8.0 | | | |
| | | Channel-dedicated sample-and- hold circuits not in use | — | ± 2.5 | ± 7.0 | | | |
| | AN003 to AN007, AN103 to AN107 | | — | ± 2.5 | ± 7.0 | | | |
| | AN200 to AN211 | | — | ± 2.5 | ± 7.0 | | | |
| | AN216 to AN217 | | — | ± 2.5 | ± 8.0 | | | |
| DNL differential nonlinearity error | | Channel-dedicated sample-and- hold circuits in use | — | ± 1.0 | ± 4.5 | | | |
| | | Channel-dedicated sample-and- hold circuits not in use | — | ± 1.0 | ± 3.5 | | | |
| INL integral nonlinearity error | | Channel-dedicated sample-and- hold circuits in use | — | ± 2.0 | ± 5.0 | | | |
| | | Channel-dedicated sample-and- hold circuits not in use | — | ± 1.5 | ± 3.5 | | | |
| Channel-dedicated sample-and-hold characteristics of hold circuits | | | | — | — | 20 | μ s | |
| Dynamic range | AN000 to AN002 | Channel-dedicated sample-and- hold circuits in use | 0.2 | — | $AV_{CC0} - 0.2$ | V | | |
| | AN100 to AN102 | Channel-dedicated sample-and- hold circuits in use | 0.2 | — | $AV_{CC1} - 0.2$ | | | |

Note: The above specification values apply when there is no access to the external bus during A/D conversion. If access proceeds during A/D conversion, values may not fall within the above ranges.

Note 1. The conversion time is the sum of the sampling time and the comparison time. The numbers of sampling-clock cycles are indicated as the test conditions.

Table 5.45 A/D Internal Reference Voltage Characteristics

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V, $T_a = T_{opr}$, $PCLKB = PCLKD = 8$ to 60 MHz

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|--------------------------------|------|------|------|------|-----------------|
| A/D internal reference voltage | 1.20 | 1.25 | 1.30 | V | |

Note: The above specification values apply during normal operations.

5.7 Programmable Gain Amplifier Characteristics

Table 5.46 Programmable Gain Amplifier Characteristics (single-ended input)

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V, $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|----------------------------------|-------------|-------------------------|------------|-------------------------|-------------|---------------------|
| Input offset voltage | V_{IO} | — | 3 | 8 | mV | |
| Single-ended input voltage range | V_{ISR} | $V_{OSR}(\text{min})/G$ | — | $V_{OSR}(\text{min})/G$ | V | |
| Output voltage range | V_{OR} | $0.10 \times AVCCn$ | — | $0.90 \times AVCCn$ | | G = 2.000 to 3.636 |
| | | $0.15 \times AVCCn$ | — | $0.85 \times AVCCn$ | | G = 4.000 to 6.667 |
| | | $0.20 \times AVCCn$ | — | $0.80 \times AVCCn$ | | G = 8.000 to 20.000 |
| Gain | G | 2.000 | — | 20.000 | Linear gain | |
| Gain error | E_G | — | ± 0.5 | ± 2.0 | % | G = 2.000 |
| | | — | ± 0.5 | ± 2.0 | | G = 2.500 |
| | | — | ± 0.5 | ± 2.0 | | G = 3.077 |
| | | — | ± 0.5 | ± 2.0 | | G = 3.636 |
| | | — | ± 0.6 | ± 2.0 | | G = 4.000 |
| | | — | ± 0.6 | ± 2.0 | | G = 4.444 |
| | | — | ± 0.7 | ± 2.0 | | G = 5.000 |
| | | — | ± 0.7 | ± 3.0 | | G = 6.667 |
| | | — | ± 0.7 | ± 3.0 | | G = 8.000 |
| | | — | ± 0.7 | ± 4.0 | | G = 10.000 |
| | | — | ± 1.1 | ± 4.0 | | G = 13.333 |
| — | ± 1.3 | ± 4.0 | G = 20.000 | | | |
| Slew rate | SR | 10 | — | — | V/ μ s | |
| Operation stabilization time | t_{start} | — | — | 5 | μ s | |

n = 0 and 1

Table 5.47 Programmable Gain Amplifier Characteristics (pseudo-differential input)

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V, $T_a = T_{opr}$

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions*1 |
|----------------------------------|-----------------|--------------------------|-----------|-------------------------|------------|-------------------|
| Input offset voltage | V_{IO} | — | 10 | 20 | mV | |
| Differential input voltage range | V_{IDR} | $-0.28 \times AVCCn / G$ | — | $0.28 \times AVCCn / G$ | V | |
| Output voltage range | V_{OR} | $0.22 \times AVCC$ | — | $0.78 \times AVCC$ | | |
| Input voltage range (PGAVSS) | $V_{I(PGAVSS)}$ | -0.5 | — | 0.3 | | |
| Gain error | E_G | — | ± 0.5 | ± 2.0 | % | G = 1.500 |
| | | — | ± 0.5 | ± 2.0 | | G = 4.000 |
| | | — | ± 0.8 | ± 3.0 | | G = 7.000 |
| | | — | ± 1.2 | ± 4.0 | | G = 12.333 |
| Slew rate | SR | 10 | — | — | V/ μ s | |
| Operation stabilization time | t_{start} | — | — | 5 | μ s | |

n = 0 and 1

Note 1. When $AVCC0 = AVCC1 = AVCC2 \geq 4.0$ V, $VOLSR.PGAVLS = 0$
 When $AVCC0 = AVCC1 = AVCC2 < 4.0$ V, $VOLSR.PGAVLS = 1$

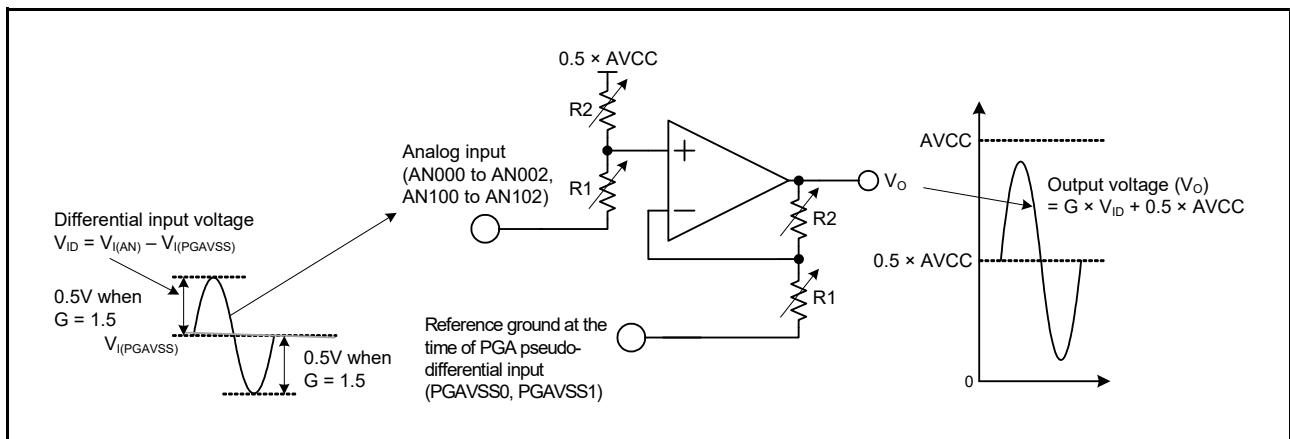


Figure 5.59 Input and Output Signal Levels with the PGA's Pseudo-Differential Setting

5.8 Comparator Characteristics

Table 5.48 Comparator Characteristics

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
 VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = T_{opr}

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|---|---------------------|------|------|-------|------|----------------------------------|
| Input offset voltage | V _{IO} | — | 8 | 40 | mV | |
| Reference input voltage range | V _{ref} | 0 | — | AVCC1 | V | CMPSEL1.CVRS[3:0] = 0100b, 1000b |
| | | 0 | — | AVCC2 | | CMPSEL1.CVRS[3:0] = 0001b, 0010b |
| Response time | t _{tot(r)} | — | — | 200 | ns | VOD = 100 mV CMPCTL.CDFS = 0 |
| | t _{tot(f)} | — | — | 200 | | |
| Waiting time for stabilization following switching of the input | t _{cwait} | 300 | — | — | | |
| Operation stabilization time | t _{cmp} | — | — | 1 | μs | |

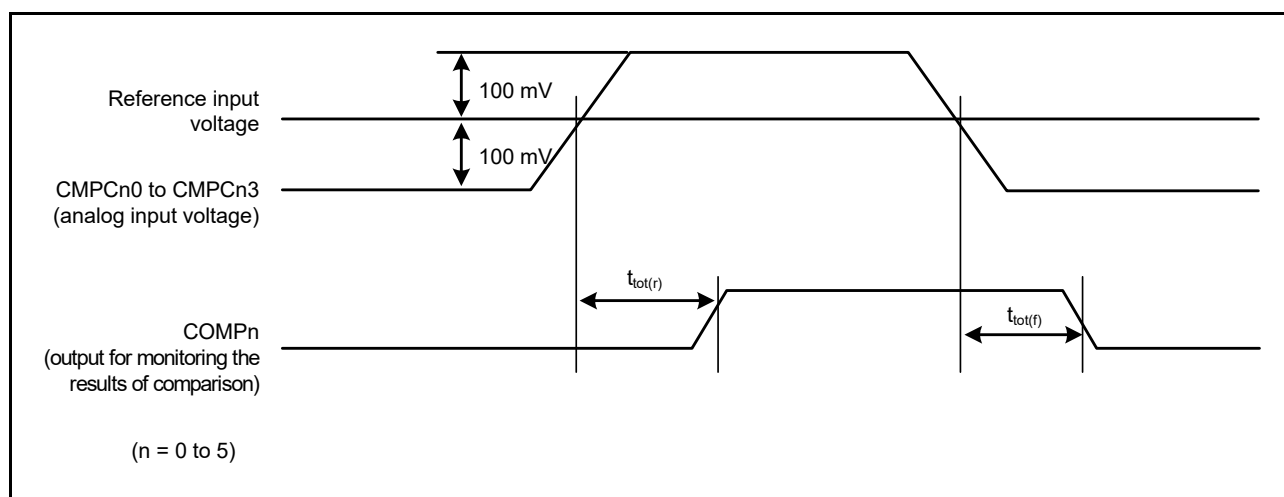


Figure 5.60 Comparator Response Time

5.9 D/A Conversion Characteristics

Table 5.49 D/A Conversion Characteristics

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V, $T_a = T_{opr}$

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|---------------------------------------|------|------|------|------------|--|
| Resolution | 12 | 12 | 12 | Bit | |
| Absolute accuracy | — | — | ±6.0 | LSB | 2-M Ω resistive load, 10-bit conversion |
| Differential nonlinearity error (DNL) | — | ±1.0 | ±2.0 | LSB | 2-M Ω resistive load |
| Output resistance (R_o) | — | 5.7 | — | k Ω | |
| Conversion time | — | — | 3 | μ s | 20-pF capacitive load |

5.10 Temperature Sensor Characteristics

Table 5.50 Temperature Sensor Characteristics

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AVCC0 = AVCC1 = AVCC2 = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AVSS0 = AVSS1 = AVSS2 = 0$ V, $T_a = T_{opr}$,
 $PCLKB = PCLKD = 8$ to 60 MHz

| Item | Min. | Typ. | Max. | Unit | Test Conditions |
|-------------------------------|------|------|------|---------|--------------------------|
| Relative accuracy | — | ±1.0 | — | °C | |
| Temperature slope | — | -2.0 | — | mV/°C | |
| Output voltage | — | 0.63 | — | V | $T_a = 25^\circ\text{C}$ |
| Temperature sensor start time | — | — | 200 | μ s | |
| Sampling time*1 | 3 | — | — | μ s | |

Note 1. Set the S12AD2.ADSSTR register such that the sampling time of the 12-bit A/D converter satisfies this specification.

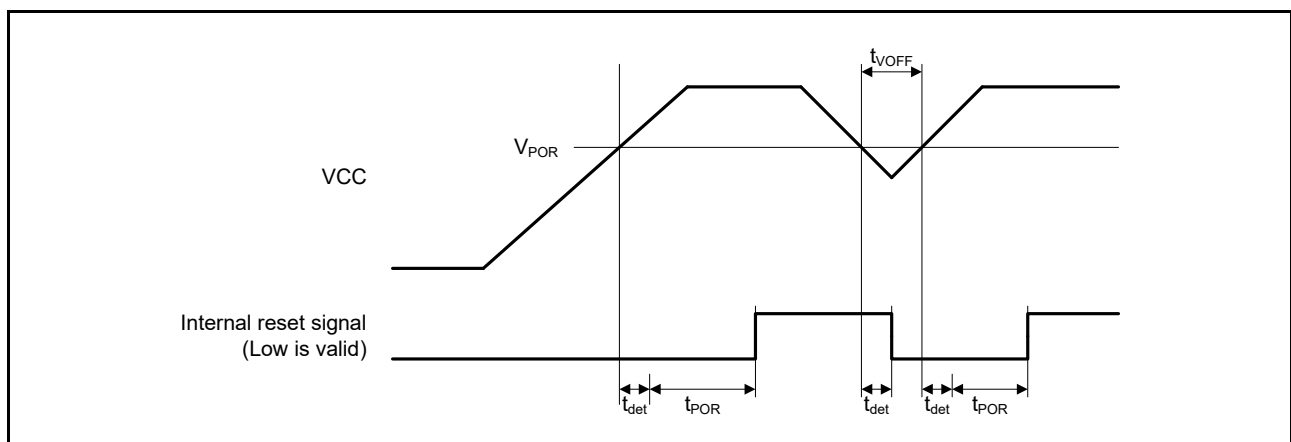
5.11 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Table 5.51 Power-on Reset Circuit and Voltage Detection Circuit Characteristics

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AV_{CC0} = AV_{CC1} = AV_{CC2} = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0$ V, $T_a = T_{opr}$

| | Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions | | |
|---|----------------------------------|---------------------|------------|------|------|-------------|-------------------------------|----|-------------|
| Voltage detection level | Power-on reset (POR) | V_{POR} | 2.46 | 2.58 | 2.70 | V | Figure 5.61 | | |
| | Voltage detection circuit (LVD0) | V_{det0_1} | 4.04 | 4.22 | 4.40 | | Figure 5.62 | | |
| | | V_{det0_2} | 2.71 | 2.83 | 2.95 | | | | |
| | Voltage detection circuit (LVD1) | V_{det1_0} | 4.39 | 4.57 | 4.75 | | Figure 5.63 | | |
| | | V_{det1_1} | 4.29 | 4.47 | 4.65 | | | | |
| | | V_{det1_2} | 4.14 | 4.32 | 4.50 | | | | |
| | | V_{det1_3} | 2.81 | 2.93 | 3.05 | | | | |
| | | V_{det1_4} | 2.76 | 2.88 | 3.00 | | | | |
| | Voltage detection circuit (LVD2) | V_{det2_0} | 4.39 | 4.57 | 4.75 | | Figure 5.64 | | |
| | | V_{det2_1} | 4.29 | 4.47 | 4.65 | | | | |
| | | V_{det2_2} | 4.14 | 4.32 | 4.50 | | | | |
| | | V_{det2_3} | 2.81 | 2.93 | 3.05 | | | | |
| | | V_{det2_4} | 2.76 | 2.88 | 3.00 | | | | |
| | Internal reset time | Power-on reset time | t_{POR} | — | 13.7 | | — | ms | Figure 5.61 |
| | | LVD0 reset time | t_{LVD0} | — | 0.70 | | — | | Figure 5.62 |
| LVD1 reset time | | t_{LVD1} | — | 0.57 | — | Figure 5.63 | | | |
| LVD2 reset time | | t_{LVD2} | — | 0.57 | — | Figure 5.64 | | | |
| Minimum VCC down time | | t_{VOFF} | 200 | — | — | μ s | Figure 5.61, Figure 5.62 | | |
| Response delay time | | t_{det} | — | — | 200 | μ s | Figure 5.61 to Figure 5.64 | | |
| LVD operation stabilization time (after LVD is enabled) | | $T_{d(E-A)}$ | — | — | 20 | μ s | Figure 5.63, Figure 5.64 | | |
| Hysteresis width (LVD1 and LVD2) | | V_{LVH} | — | 80 | — | mV | | | |

Note: The minimum VCC down time indicates the time when VCC is below the minimum value of voltage detection levels V_{POR} , V_{det1} , and V_{det2} for the POR/ LVD.

**Figure 5.61 Power-on Reset Timing**

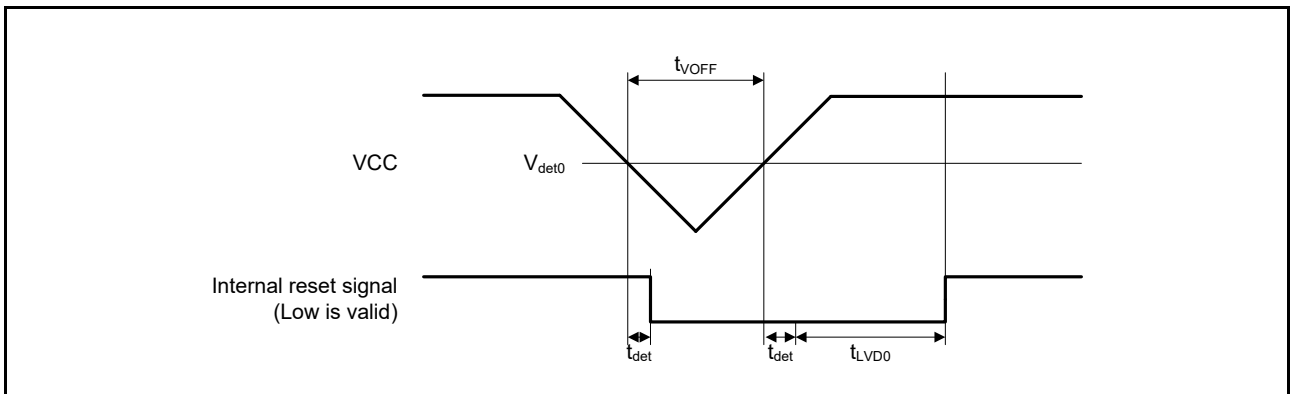


Figure 5.62 Voltage Detection Circuit Timing (V_{det0})

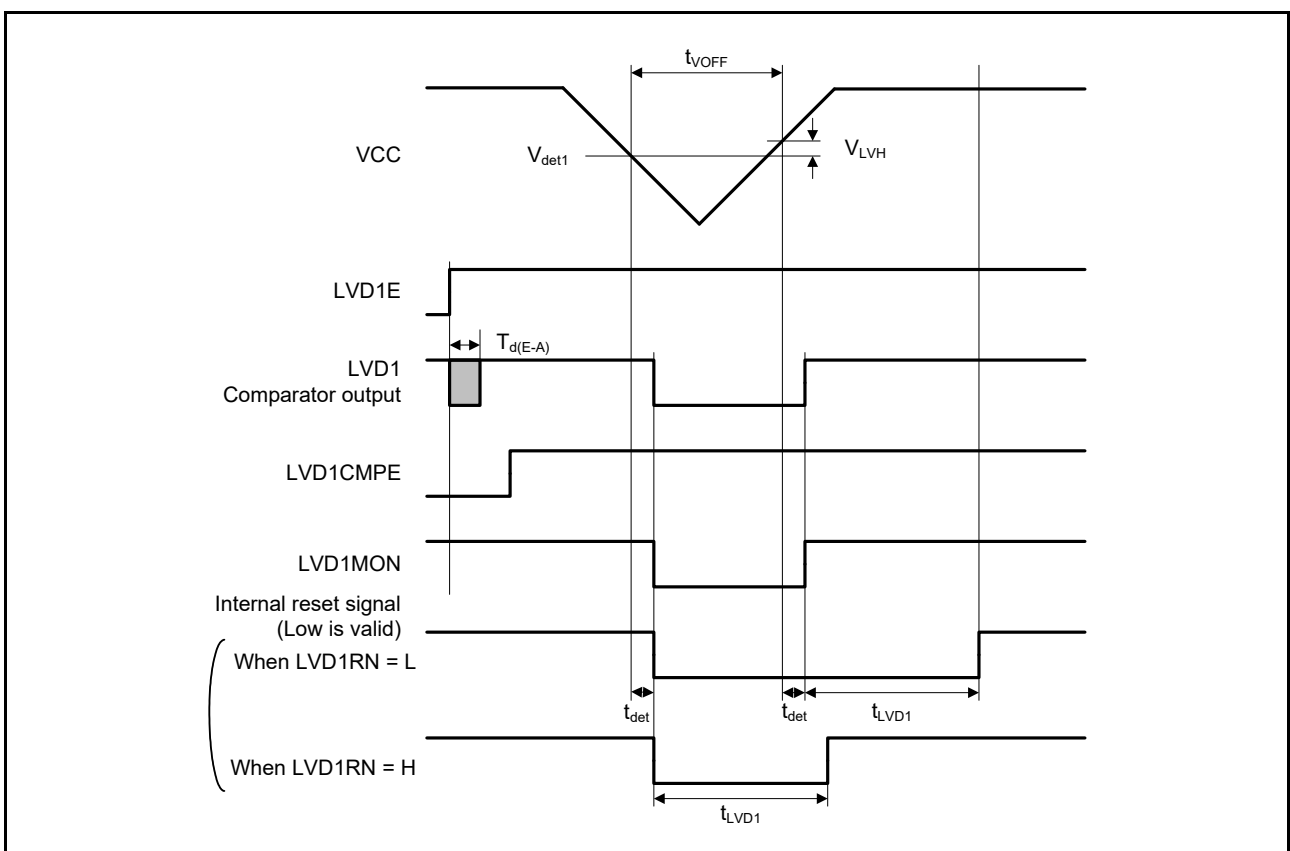


Figure 5.63 Voltage Detection Circuit Timing (V_{det1})

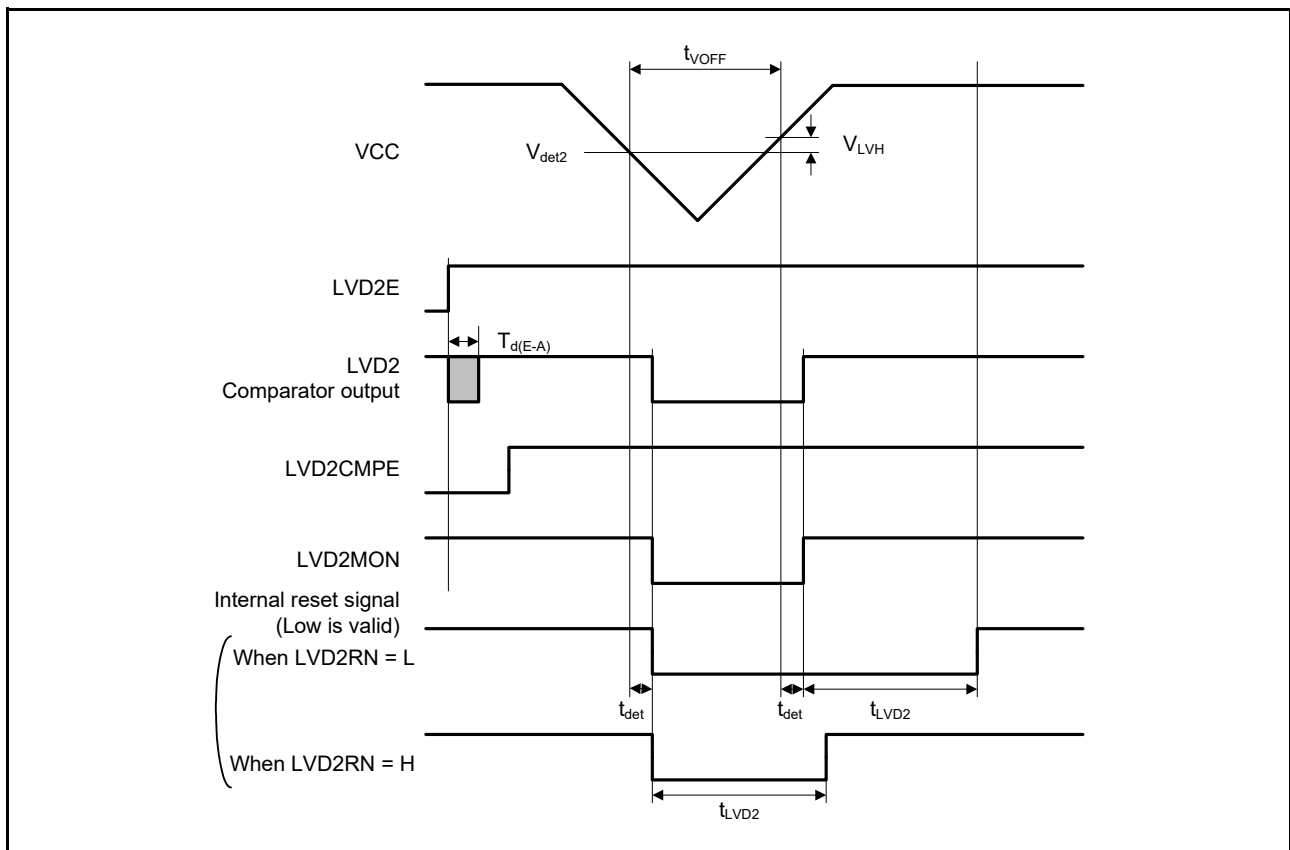


Figure 5.64 Voltage Detection Circuit Timing (V_{det2})

5.12 Oscillation Stop Detection Timing

Table 5.52 Oscillation Stop Detection Circuit Characteristics

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
 VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V, T_a = T_{opr}

| Item | Symbol | Min. | Typ. | Max. | Unit | Test Conditions |
|----------------|-----------------|------|------|------|------|-----------------|
| Detection time | t _{dr} | — | — | 1 | ms | Figure 5.65 |

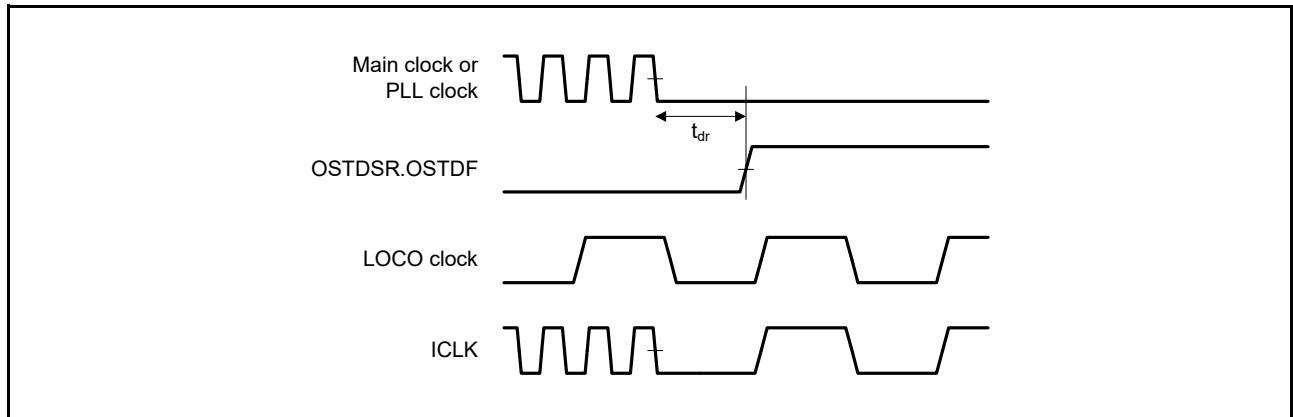


Figure 5.65 Oscillation Stop Detection Timing

5.13 Flash Memory Characteristics

Table 5.53 Code Flash Memory Characteristics

Conditions: VCC = 2.7 to 5.5 V, VCC_USB = 2.7 to 5.5 V, AVCC0 = AVCC1 = AVCC2 = 3.0 to 5.5V,
VSS = VSS_USB = AVSS0 = AVSS1 = AVSS2 = 0 V,
Temperature range for program/erase: T_a = T_{opr}

| Item | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 60 MHz | | | Unit | |
|--|--------------------|-------------------|------|------|------------------------|------|------|--------|----|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Program time (N _{PEC} ≤ 100 cycles) | 256 bytes | t _{P256} | — | 0.9 | 13.2 | — | 0.4 | 6 | ms |
| | 8 Kbytes | t _{P8K} | — | 29 | 176 | — | 13 | 80 | |
| | 32 Kbytes | t _{P32K} | — | 116 | 704 | — | 52 | 320 | |
| Program time (N _{PEC} > 100 cycles) | 256 bytes | t _{P256} | — | 1.1 | 15.8 | — | 0.5 | 7.2 | |
| | 8 Kbytes | t _{P8K} | — | 35 | 212 | — | 16 | 96 | |
| | 32 Kbytes | t _{P32K} | — | 140 | 848 | — | 64 | 384 | |
| Erase time (N _{PEC} ≤ 100 cycles) | 8 Kbytes | t _{E8K} | — | 71 | 216 | — | 39 | 120 | |
| | 32 Kbytes | t _{E32K} | — | 254 | 864 | — | 141 | 480 | |
| Erase time (N _{PEC} > 100 cycles) | 8 Kbytes | t _{E8K} | — | 85 | 260 | — | 47 | 144 | |
| | 32 Kbytes | t _{E32K} | — | 304 | 1040 | — | 169 | 576 | |
| Program/erase cycles*1 | N _{PEC} | 1000*2 | — | — | 1000*2 | — | — | Cycles | |
| Program suspend latency | t _{SPD} | — | — | 264 | — | — | 120 | μs | |
| Primary erase suspend latency in suspend priority mode | t _{SESD1} | — | — | 216 | — | — | 120 | | |
| Secondary erase suspend latency in suspend priority mode | t _{SESD2} | — | — | 1.7 | — | — | 1.7 | ms | |
| Erase suspend latency in erase priority mode | t _{SEED} | — | — | 1.7 | — | — | 1.7 | | |
| Forced stop command | t _{FD} | — | — | 32 | — | — | 20 | μs | |
| Data retention*3 | t _{DRP} | 10 | — | — | 10 | — | — | Year | |

Note 1. Definition of program/erase cycle:

The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 256-byte program is performed 32 times for different addresses in 8-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).

Note 2. Characteristics are degraded as the number of program/erase increases. This is the minimum value of program/erase cycles to guarantee all characteristics listed in this table.

Note 3. This shows the characteristic when the program/erase cycle does not exceed the specified value.

Table 5.54 Data Flash Memory Characteristics

Conditions: $V_{CC} = 2.7$ to 5.5 V, $V_{CC_USB} = 2.7$ to 5.5 V, $AV_{CC0} = AV_{CC1} = AV_{CC2} = 3.0$ to 5.5 V,
 $V_{SS} = V_{SS_USB} = AV_{SS0} = AV_{SS1} = AV_{SS2} = 0$ V,
 Temperature range for program/erase: $T_a = T_{opr}$

| Item | Symbol | FCLK = 4 MHz | | | 20 MHz ≤ FCLK ≤ 60 MHz | | | Unit | |
|--|----------|--------------|----------|------|------------------------|----------|------|------|--------|
| | | Min. | Typ. | Max. | Min. | Typ. | Max. | | |
| Program time | 4 bytes | t_{DP4} | — | 0.36 | 3.8 | — | 0.16 | 1.7 | ms |
| Erase time | 64 bytes | t_{DE64} | — | 3.1 | 18 | — | 1.7 | 10 | |
| Blank check time | 4 bytes | t_{DBC4} | — | — | 84 | — | — | 30 | μs |
| | 64 bytes | t_{DBC64} | — | — | 280 | — | — | 100 | |
| | 2 Kbytes | t_{DBC2K} | — | — | 6160 | — | — | 2200 | |
| Program/erase cycles*1 | | N_{DPEC} | 100000*2 | — | — | 100000*2 | — | — | Cycles |
| Program suspend latency | | t_{DSPD} | — | — | 264 | — | — | 120 | μs |
| Primary erase suspend latency in suspend priority mode | | t_{DSESD1} | — | — | 216 | — | — | 120 | |
| Secondary erase suspend latency in suspend priority mode | | t_{DSESD2} | — | — | 300 | — | — | 300 | |
| Erase suspend latency in erase priority mode | | t_{DSEED} | — | — | 300 | — | — | 300 | |
| Forced stop command | | t_{FD} | — | — | 32 | — | — | 20 | |
| Data retention*3 | | t_{DDRP} | 10 | — | — | 10 | — | — | Year |

Note 1. Definition of program/erase cycle:

The program/erase cycle is the number of erasing for each block. When the number of program/erase cycles is n, each block can be erased n times. For instance, when 4-byte program is performed 512 times for different addresses in 2-Kbyte block and then the block is erased, the program/erase cycle is counted as one. However, the same address cannot be programmed more than once before the next erase cycle (overwriting is prohibited).

Note 2. Characteristics are degraded as the number of program/erase increases. This is the minimum value of program/erase cycles to guarantee all characteristics listed in this table.

Note 3. This shows the characteristic when the program/erase cycle does not exceed the specified value.

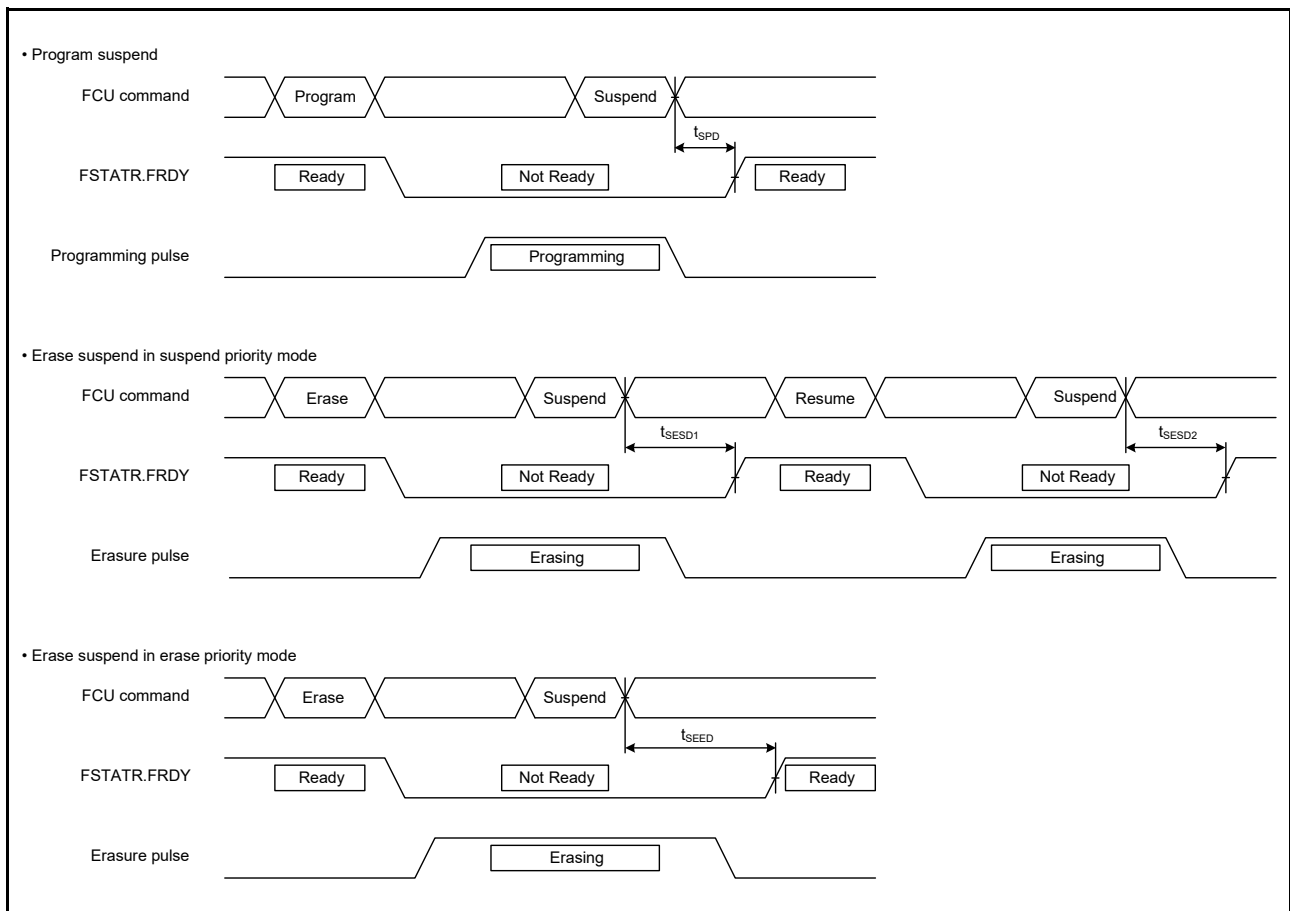


Figure 5.66 Flash Memory Program/Erase Suspend Timing

Appendix 1. Package Dimensions

Information on the latest version of the package dimensions or mountings has been displayed in “Packages” on Renesas Electronics Corporation website.

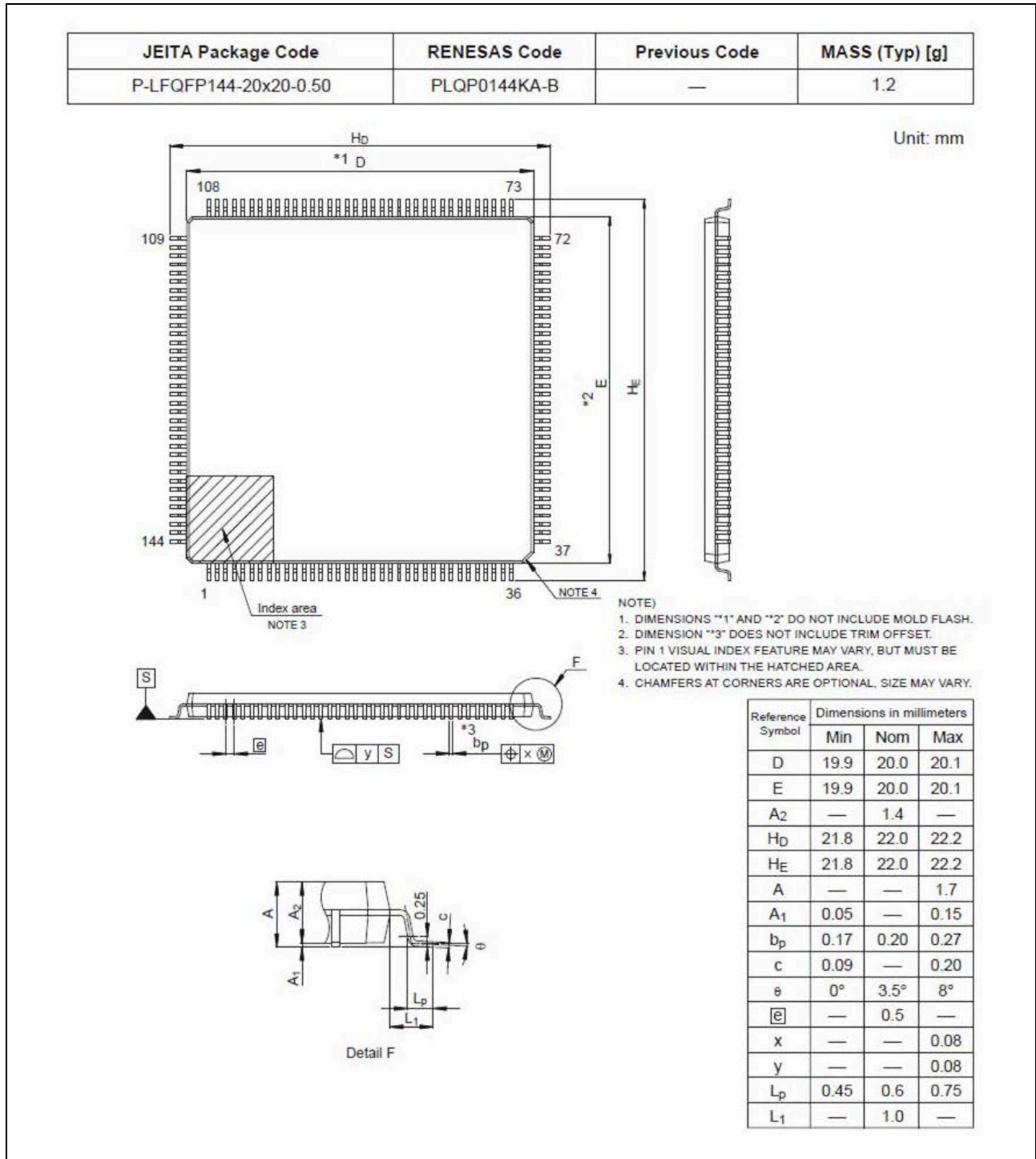


Figure A 144-Pin LFQFP (PLQP0144KA-B)

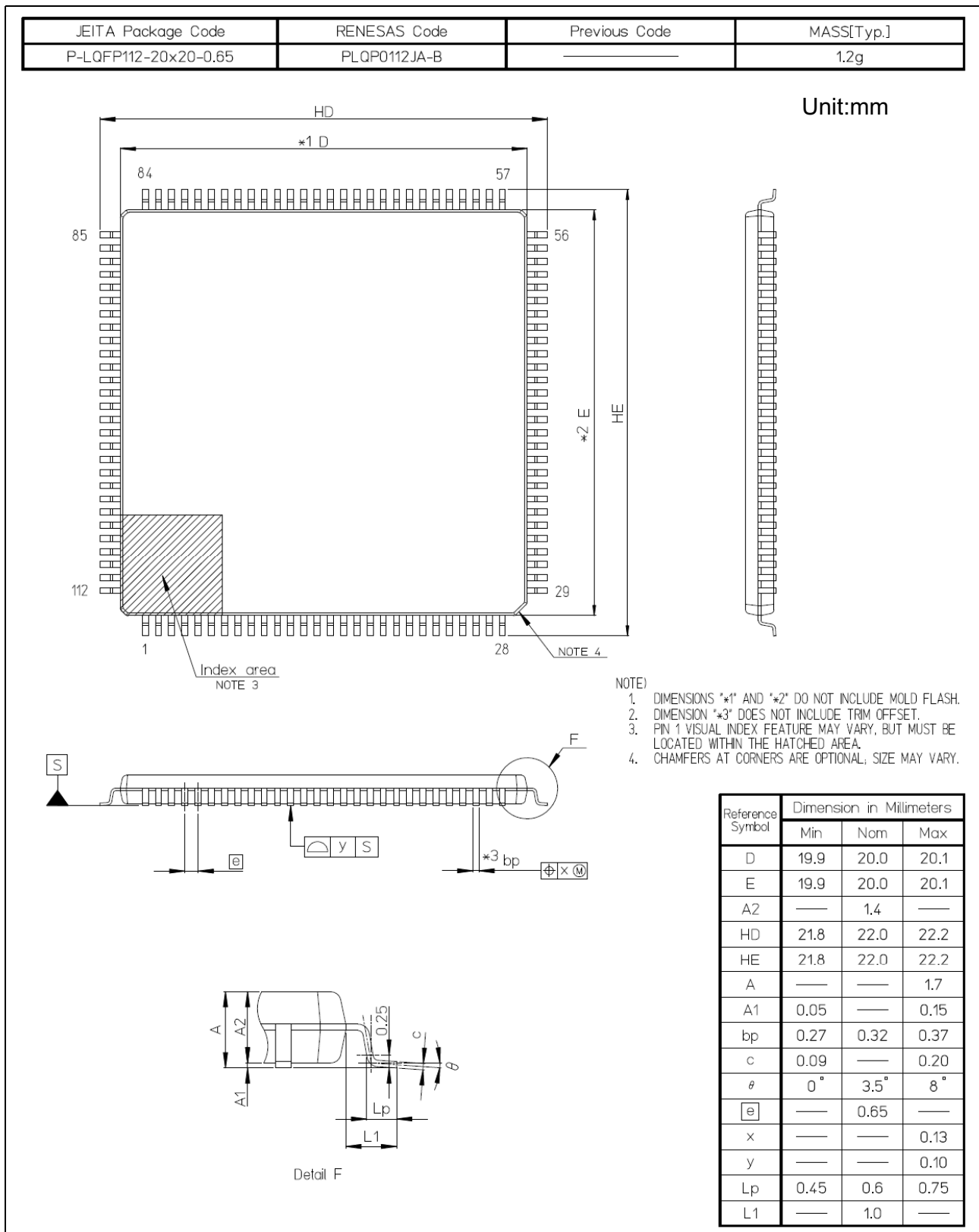
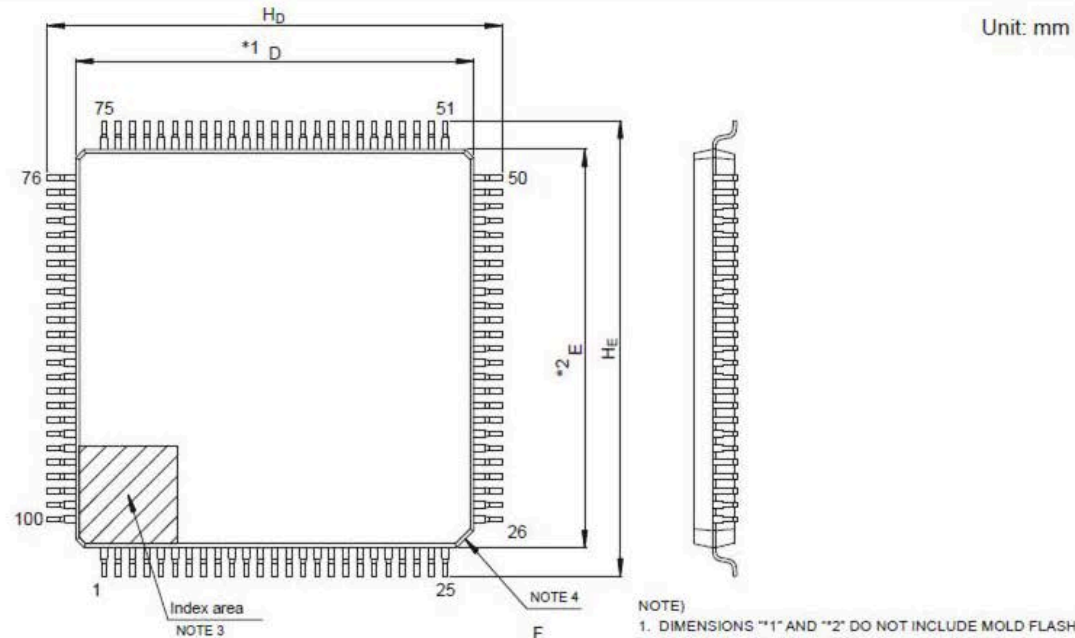
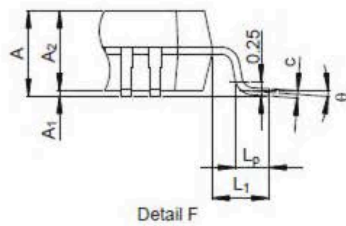
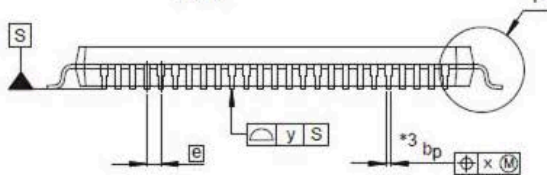


Figure B 112-Pin LQFP (PLQP0112JA-B)

| JEITA Package Code | RENESAS Code | Previous Code | MASS (Typ) [g] |
|-----------------------|--------------|---------------|----------------|
| P-LFQFP100-14x14-0.50 | PLQP0100KB-B | — | 0.6 |



- NOTE)
1. DIMENSIONS **1" AND **2" DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION **3" DOES NOT INCLUDE TRIM OFFSET.
 3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
 4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.



| Reference Symbol | Dimensions in millimeters | | |
|------------------|---------------------------|------|------|
| | Min | Nom | Max |
| D | 13.9 | 14.0 | 14.1 |
| E | 13.9 | 14.0 | 14.1 |
| A ₂ | — | 1.4 | — |
| H _D | 15.8 | 16.0 | 16.2 |
| H _E | 15.8 | 16.0 | 16.2 |
| A | — | — | 1.7 |
| A ₁ | 0.05 | — | 0.15 |
| b _p | 0.15 | 0.20 | 0.27 |
| c | 0.09 | — | 0.20 |
| θ | 0° | 3.5° | 8° |
| e | — | 0.5 | — |
| x | — | — | 0.08 |
| y | — | — | 0.08 |
| L _p | 0.45 | 0.6 | 0.75 |
| L ₁ | — | 1.0 | — |

Figure C 100-Pin LFQFP (PLQP0100KB-B)

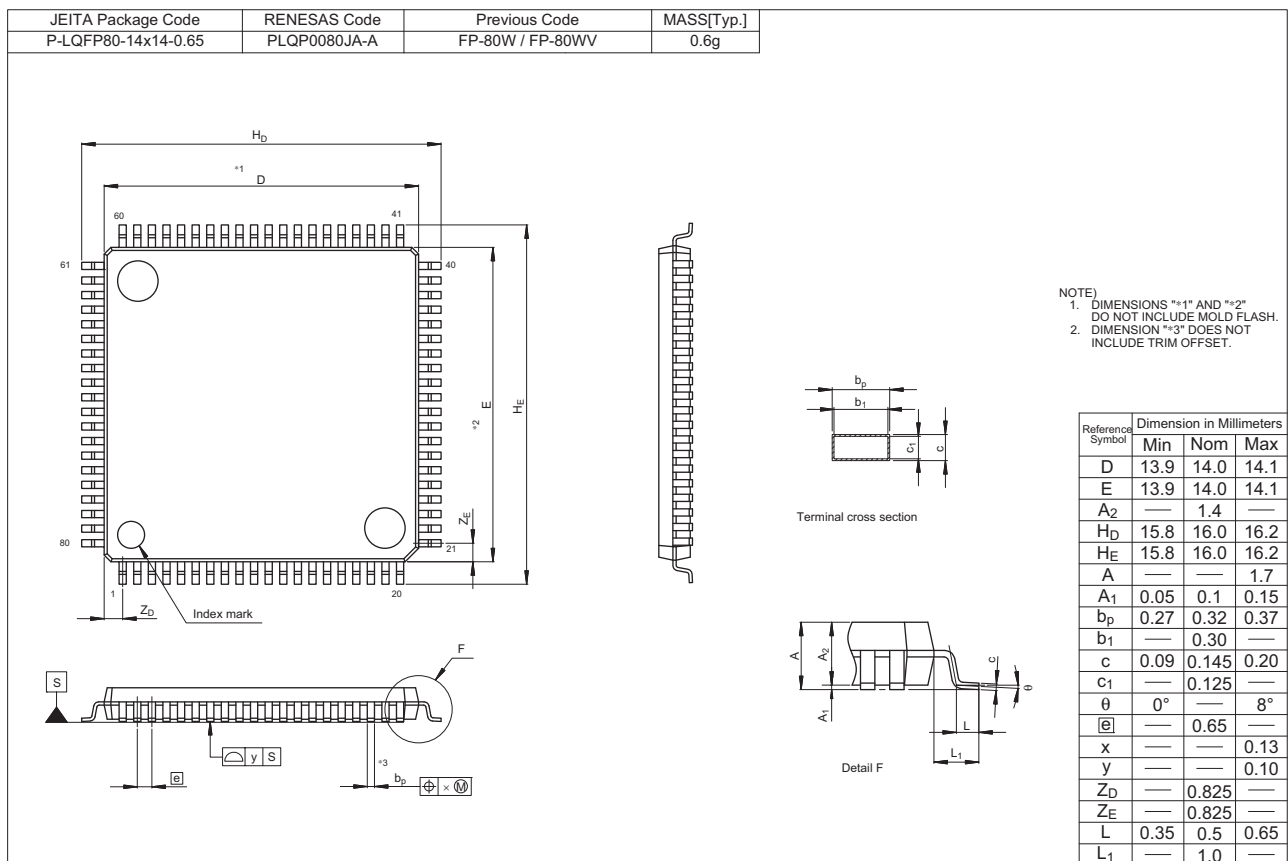


Figure D 80-Pin LQFP (PLQP0080JA-A)

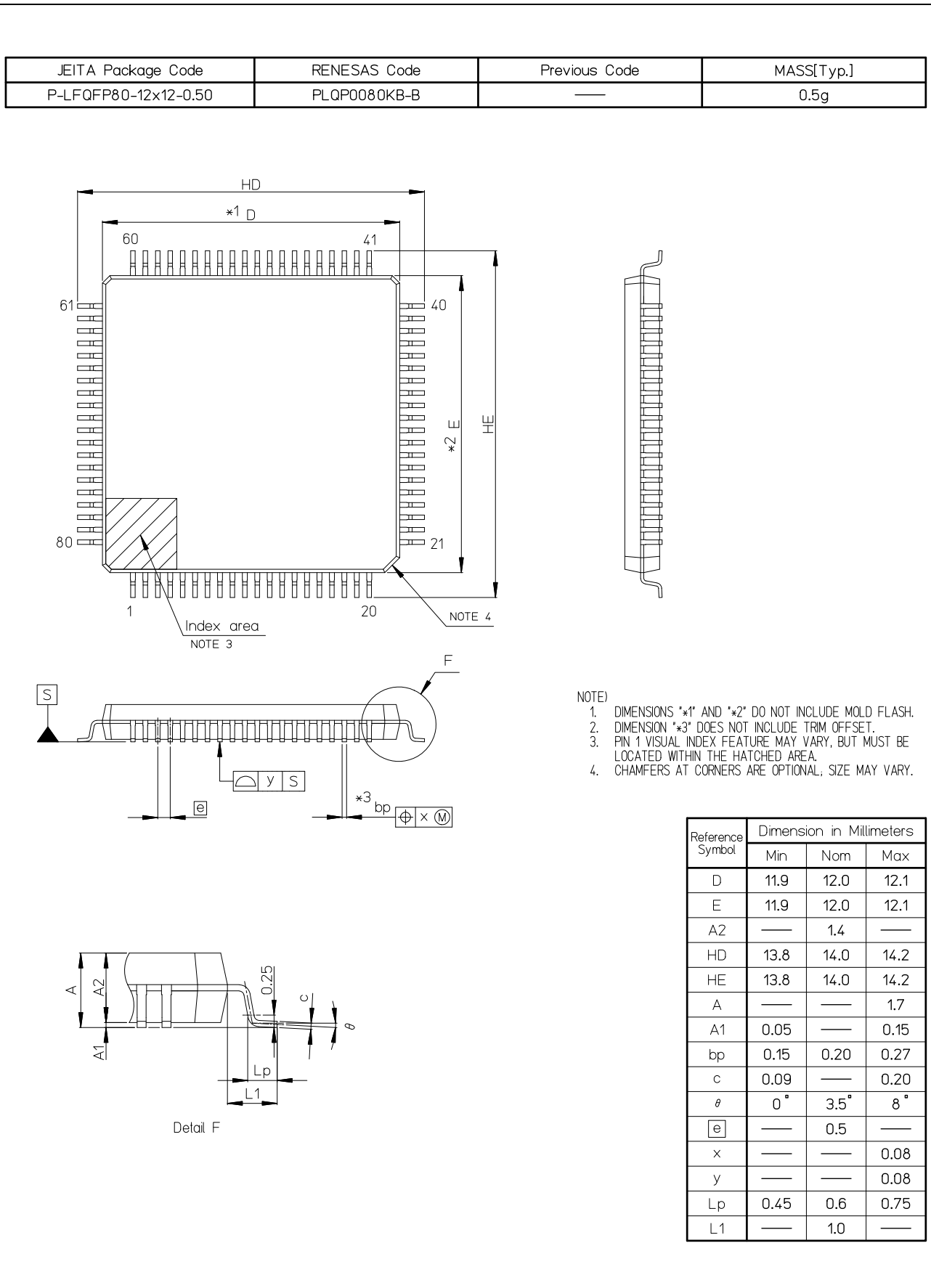


Figure E 80-Pin LQFP (PLQP0080KB-B)

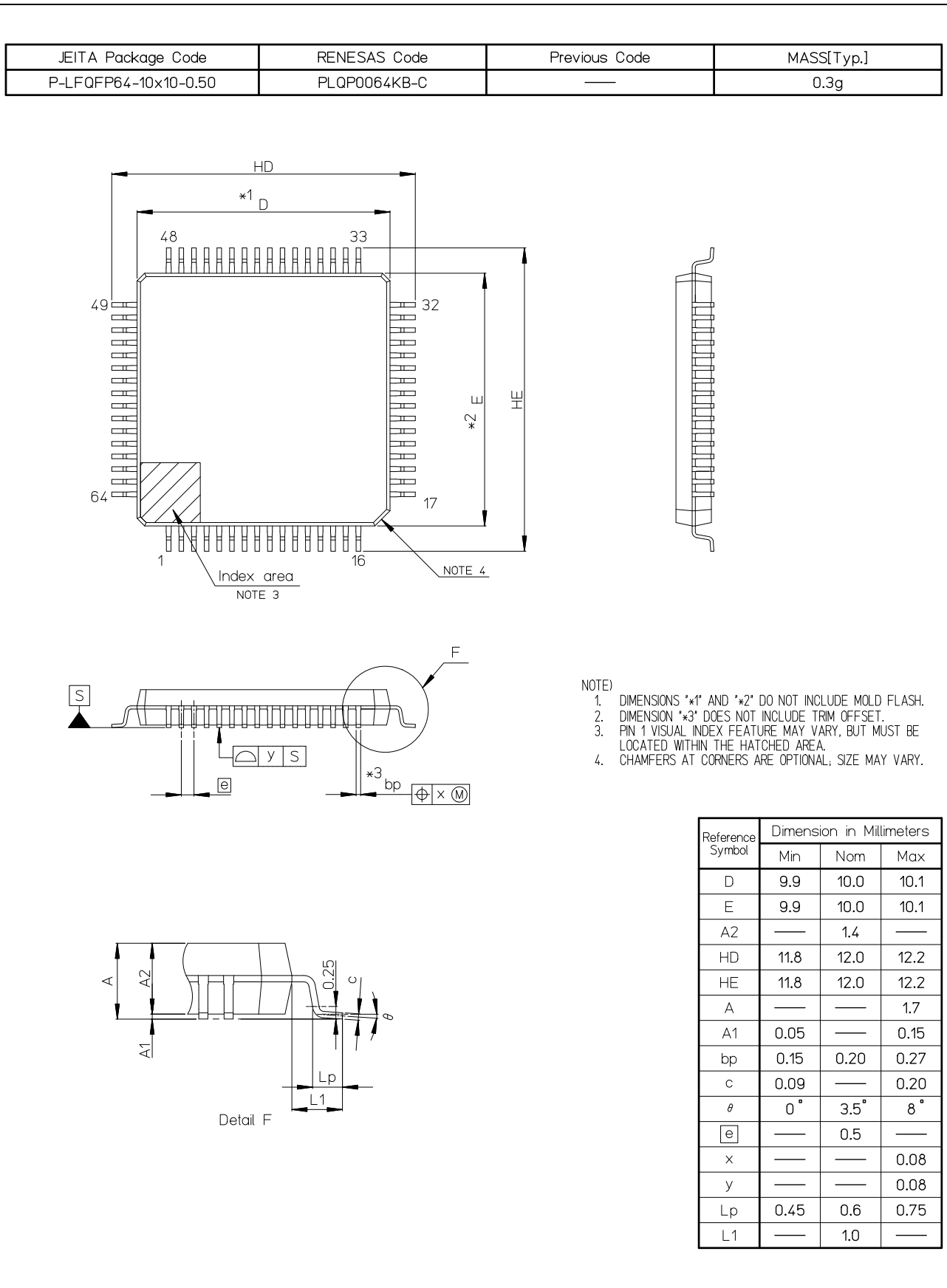


Figure F 64-Pin LFQFP (PLQP0064KB-C)

| | |
|------------------|-----------------------|
| REVISION HISTORY | RX66T Group Datasheet |
|------------------|-----------------------|

Classifications

- Items with Technical Update document number: Changes according to the corresponding issued Technical Update
- Items without Technical Update document number: Minor changes that do not require Technical Update to be issued

| Rev. | Date | Description | | Classification |
|------|--|-------------------------------|--|-----------------|
| | | Page | Summary | |
| 1.00 | Jul 30, 2018 | — | First edition, issued | |
| 1.10 | Feb 08, 2019 | All | G-version products, added 144-pin products, added Products with 128 Kbytes of RAM, added | |
| | | Features | | |
| | | 1 | Features, changed | TN-RX*-A0205A/E |
| | | 1. Overview | | |
| | | 23 | Table 1.4 Pin Functions: Note added | |
| | | 3. Address Space | | |
| | | 70 | Figure 3.1 Memory Map in Each Operating Mode, changed | |
| | | 71 | Figure 3.2 Correspondence between External Address Spaces and CS Areas (In On-Chip ROM Disabled Extended Mode), changed | |
| | | 5. Electrical Characteristics | | |
| | | 129 | Table 5.3 Recommended operating conditions (2), added | TN-RX*-A0205A/E |
| | | 131 | Table 5.5 DC Characteristics (2), changed | |
| | | 138 | Table 5.12 Permissible Output Currents, changed | |
| | | 150 | Figure 5.14 NMI Interrupt Input Timing, Figure 5.15 IRQ Interrupt Input Timing, changed | |
| | | 159 | Table 5.31 POE and POEG Timing, changed | |
| | | 160, 161 | Figure 5.28 Output Disable Time for POE in Response to Transition of the POEn# Signal Level to Figure 5.32 Output Disable Time for POE in Response to the Oscillation Stop Detection, changed | |
| | | 161 | Figure 5.33 POEG Input Timing, changed | |
| | | 161 to 163 | Figure 5.34 Output Disable Time for POEG via Detection Flag in Response to the Input Level Detection of the GTETRn pin to Figure 5.40 Output Disable Time for POEG in Response to Level Detection Signal from a Comparator, changed | TN-RX*-A0205A/E |
| | | 168 | Table 5.36 RSPI Timing, changed | |
| | | 174 | Table 5.38 RIIC Timing, changed | |
| | | 175 | Table 5.39 Simple IIC Timing, changed | |
| 179 | Table 5.43 12-Bit A/D (Unit 0, 1, 2) Conversion Characteristics (1), changed | | | |
| 180 | Table 5.44 12-Bit A/D (Unit 0, 1, 2) Conversion Characteristics (2), changed | | | |
| 182 | Table 5.46 Programmable Gain Amplifier Characteristics (single-ended input), Table 5.47 Programmable Gain Amplifier Characteristics (pseudo-differential input), changed | | | |

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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems.

The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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