R5H30313XB08
for USB Type-C™ Authentication

Renesas Microcomputer

R01DS0314EJ0110
Rev.1.10
Feb 28, 2019

Overview

This LSI is a microcomputer which offers the authentication function for PD products to USB Power Delivery Controller R9A02G011. The authentication function which offered by the LSI is based on the Universal Serial Bus Type-C™ Authentication Specification Revision 1.0.

Applications

USB Type-C™ Authentication supported devices (AC Adapter, Power outlet, USB PD Hub, PC, Tablet, Smartphone, Docking Station, PC Peripheral Device (Monitor, Printer, Router, External HDD), Consumer Electronics (DTV, STB, Home Gateway), USB Type-C™ Cable etc.)

Table 1 Features

Classification	Description
Authentication function	• Based on the Universal Serial Bus Type-C™ Authentication Specification Revision 1.0 Works as Authentication Initiator Note 1 or Authentication Responder Note 1. And private keys, Certificate Chain Note 1, Root Certificate Note 1 and Certificate Chain digests are managed. Authentication Initiator caches Authentication Responder's Certificate Chains (cache size: 16 Certificate Chains).
Hardware Security	• Security error detecting functions • Current control functions
On-chip memory	• EEPROM Private keys, Certificate Chain, Root Certificate and Certificate Chain digests used for authentication are stored. Data retention time: 10 years
Power-down modes	• Power-Down States is entered by a request of R9A02G011
CPU operating clock	• Internal clock
Communication interface	• I^2C bus interface is used.
Power-on reset circuit	• Incorporated
Power supply	• Single-voltage power supply • 1.8 V to 3.6 V
Operating peripheral temperature (°C)	• –40°C to +90°C

Notes: 1. Unique names in this paragraph are defined in the Universal Serial Bus Type-C™ Authentication Specification Revision 1.0.

Ordering Information

Table 2 is an ordering information.

Table 2 Ordering Information

Part No.	Application	Package
R5H30313XB08NAxx Note	Universal Serial Bus Type-C™ Authentication	UQFN0404-20

Note xx is determined by internal code for each customer's product. Please contact a Renesas Sales Representative or Distributor in your area.

Pin Assignment and Functions

Pin Assignment

Figure 1 shows the pin arrangement of this LSI.

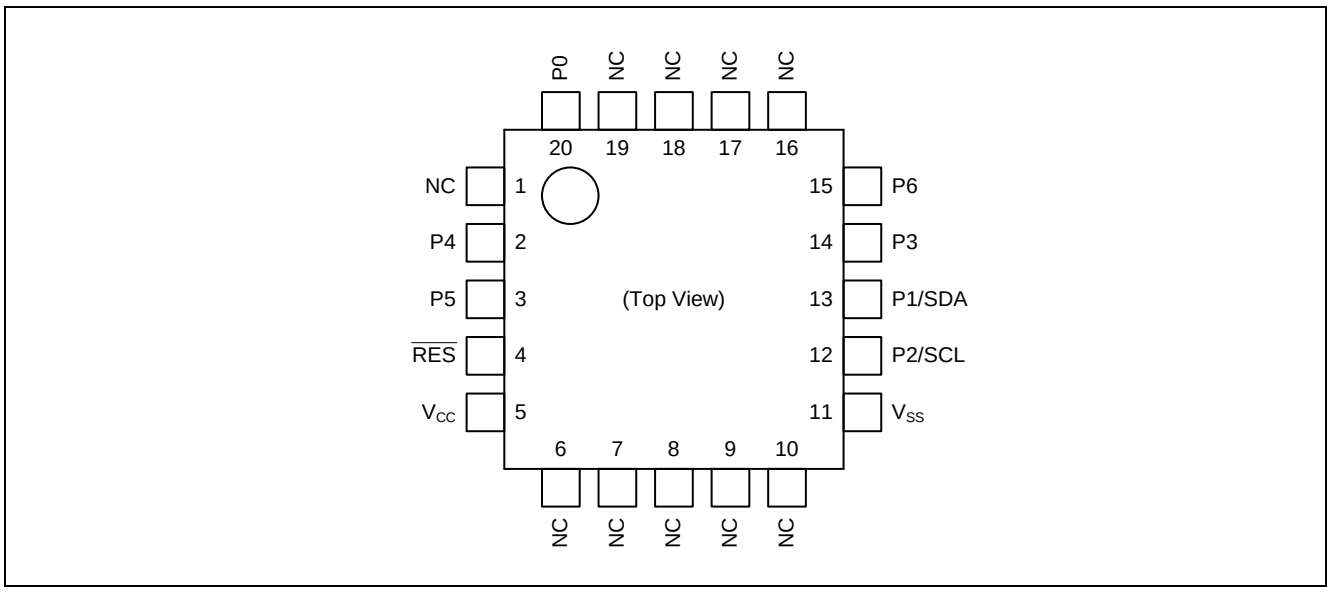


Figure 1 Pin Assignment

Pin Functions

Table 3 lists the pin functions of this LSI.

Table 3 Pin Functions

Pin No.	Pin Name	I/O	Function
2	P4	Input	Unused pin. Connect this pin to V_{SS} via a pull-down resistor.
3	P5	Input	Unused pin. Connect this pin to V_{SS} via a pull-down resistor.
4	$\overline{RES}$	Input	Reset pin. Low-level input resets the chip.
5	V_{CC}	Input	Power supply. Connected to the power supply of the system.
11	V_{SS}	Input	Ground. Connected to the power supply (0 V) of the system.
12	P2/SCL	I/O	Clock input/output pin for the I^2C bus interface. It's also the input pin from which software standby mode and deep software standby mode is canceled.
13	P1/SDA	I/O	Data input/output pin for the I^2C bus interface. It's also the input pin from which software standby mode and deep software standby mode is canceled.
14	P3	Input	Unused pin. Connect this pin to V_{SS} via a pull-down resistor.
15	P6	Output	Unused pin. Leave this pin open.
20	P0	Input	Unused pin. Connect this pin to V_{SS} via a pull-down resistor.

Absolute Maximum Ratings

Table 4 Absolute Maximum Ratings

Item	Symbol		Rating	Unit
Power supply voltage	V_{CC}	V_{CC}	–0.3 to +7.0	V
Input voltage	V_{in}	$\overline{RES}$, P1/SDA, P2/SCL	–0.3 to V_{CC} + 0.3	V
Operating temperature	T_{opr}		–40 to +90	°C
Storage temperature	T_{stg}		–55 to +90	°C

Note: Permanent damage may occur to the chip if maximum ratings are exceeded. Normal operation should be under the recommended operating conditions. Exceeding these conditions could affect the reliability of the chip.

DC Characteristics

Table 5 DC Characteristics

Conditions: V_{CC} = 1.8 V to 3.6 V, V_{SS} = 0 V, Ta = –40°C to +90°C, unless otherwise specified.

Item		Sym.	Test Conditions	Min.	Typ.	Max.	Unit
Input high voltage	$\overline{RES}$, P1/SDA, P2/SCL	V_{IH}	V_{CC} = 1.8 to 2.2 V	$V_{CC} \times 0.85$	—	V_{CC} + 0.3	V
			V_{CC} = 2.2 to 3.6 V	$V_{CC} \times 0.7$	—	V_{CC} + 0.3	V
Input low voltage	$\overline{RES}$, P1/SDA, P2/SCL	V_{IL}	V_{CC} = 1.8 to 2.2 V	–0.3	—	0.2	V
			V_{CC} = 2.2 to 3.6 V	–0.3	—	$V_{CC} \times 0.2$	V
Output low voltage	P1/SDA, P2/SCL	V_{OL}	I_{OL} = 1 mA	0	—	0.4	V
Input leakage current	P1/SDA, P2/SCL	$\|I_{in}\|$	V_{in} = 0.5 to V_{CC} – 0.5V	—	—	10	µA
Input pull-up MOSFET current	$\overline{RES}$ Note 1	$-I_p$	V_{in} = 0 V	—	—	150	µA
	P1/SDA, P2/SCL Note 3						
Supply current	Authentication operation	I_{CC}	Note 2	—	—	15	mA
	With software standby mode Note 1			—	—	200	µA
	With deep software standby mode Note 1 Note 3			—	5	10	µA
Pin capacitance		C_p	V_{in} = 0V, f = 1MHz, T_a = 25°C	—	—	15	pF

Notes: 1. A pull-up MOSFET is connected to the $\overline{RES}$ pin, and thus the pull-up function is always enabled even in deep software standby mode.
2. Supply current is determined assuming that all the input pins are set to $V_{IH} = V_{CC}$ or V_{IL} = 0 V, all the output pins are unloaded, and pull-up resistors are disabled.
3. A pull-up MOSFET is connected to the P1/SDA and P2/SCL pins, and thus the pull-up function is enabled in deep software standby mode.

AC Characteristics

Table 6 AC Characteristics

Conditions: V_{CC} = 1.8 V to 3.6 V, V_{SS} = 0 V, Ta = –40°C to +90°C, unless otherwise specified.

Item	Sym.	Test Conditions	Min.	Typ.	Max.	Unit
$\overline{RES}$ fall time	t_{rf}	Figure 2	—	—	400 Note 1	µs
$\overline{RES}$ rise time	t_{rr}	Figure 2	—	—	400 Note 1	µs

Notes: 1. It is assumed that there is no noise on the $\overline{RES}$ pin, and the rise and fall of $\overline{RES}$ are straightforward.

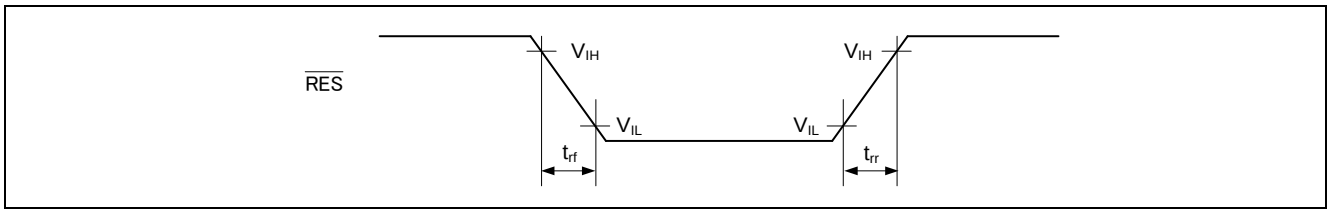


Figure 2 $\overline{RES}$ Input Waveform

Reset Circuit Characteristics

Table 7 Reset Circuit Characteristics

Conditions: V_{CC} = 1.8 V to 3.6 V, V_{SS} = 0 V, Ta = –40°C to +90°C, unless otherwise specified.

Item	Sym.	Test Conditions	Min.	Typ.	Max.	Unit
Power-on reset effective voltage	V_{POR1}	Figure 3	—	—	0.4	V
Power-on reset release voltage rise time	t_{PWON1}	Figure 3 $t_{POR1} \geq 500\mu s$ Note 1	—	—	500	µs
Power-on reset release time	t_{PRST}	Figure 3	—	—	500	µs

Notes: 1. t_{POR1} is the time necessary to enable the power-on reset by keeping the external power supply V_{CC} to lower than the effective voltage (V_{POR1}). The external power supply V_{CC} should be stable. The LSI may be reset by the rapid change of V_{CC}.

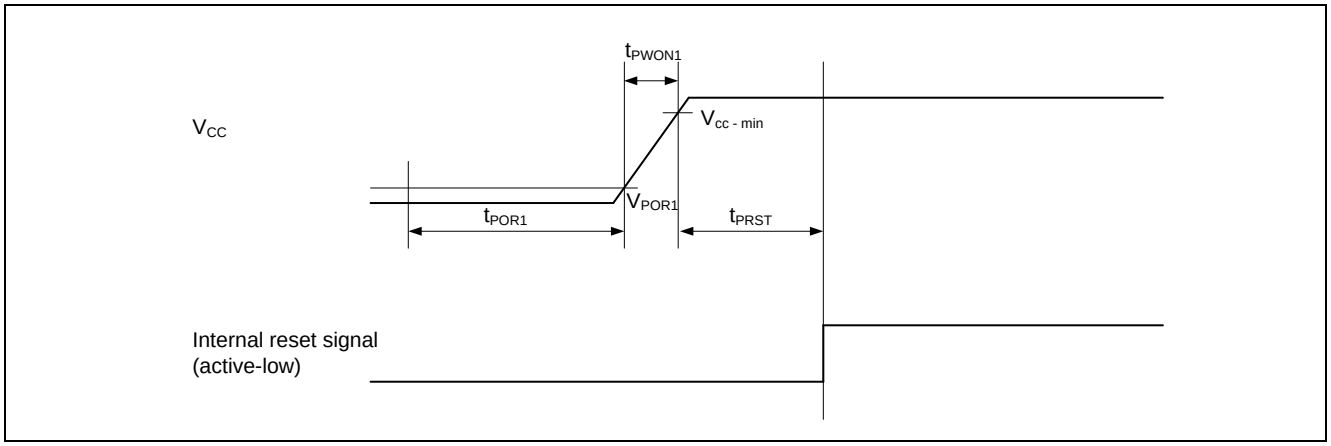


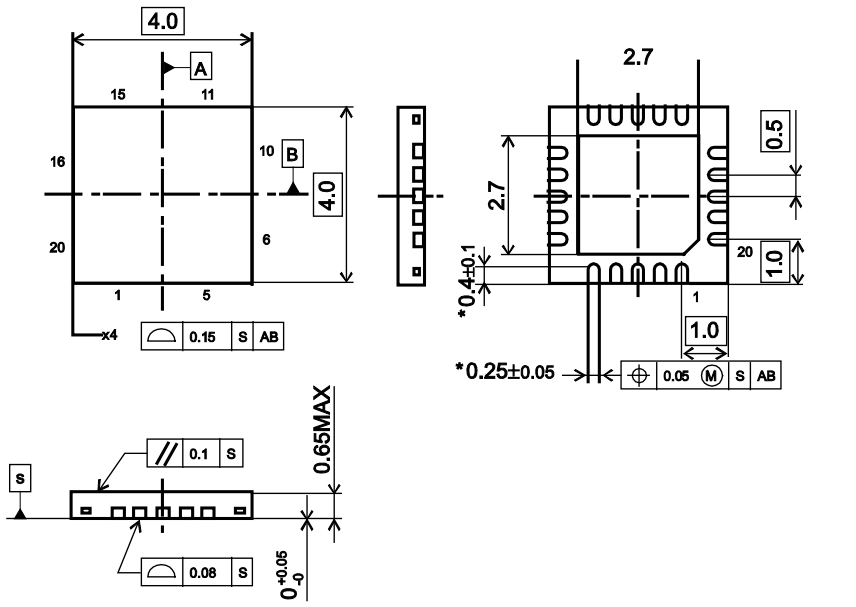
Figure 3 Power-On Reset Timing

Notes on Noise

Notes: 1. Inserting a Bypass Capacitor between V_{CC} and V_{SS} Pins as a Countermeasure against Noise and Latch-up
Connect a bypass capacitor (with a value of about 0.1 μF) using the shortest and thickest wiring runs possible.

Package Dimensions

unit : mm



* Pd plating

Package CODE	PUQN0020KA-A
EIAJ CODE	–
JEDEC CODE	–
MASS	0.033

Revision History	R5H30313XB08 for USB Type-C™ Authentication Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	Apr 17, 2017	—	First edition issued
1.10	Feb 28, 2019	2	Updated Ordering Information

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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