# RAA210030

5V, 3A Step-Down DC/DC Mini Module with Integrated Inductor

The RAA210030 power module is a compact, single-channel, synchronous step-down, non-isolated complete power supply, capable of delivering up to 3A of continuous current. By operating from a single 2.7V to 5.5V input power rail and integrating the controller, gate driver, power inductor, and MOSFETs, the RAA210030 is optimized for space constrained applications.

Based on a peak current mode control scheme, the RAA210030 provides fast transient response and excellent loop stability. The output voltage can be set as low as 0.6V, with setpoint accuracy better than ±1.5% over line, load, and temperature. The operating frequency has a 2MHz default setting, however it can also be set from 500kHz to 4MHz by an external resistor. The external synchronization is also supported with an external clock signal up to 4MHz. The RAA210030 supports 100% duty cycle operation to minimize switching losses with typically 300mV dropout voltage. A dedicated enable pin and power-good flag allow for easy system power rails sequencing.

The RAA210030 can be configured for pulsed frequency modulation (PFM) or forced pulse width modulation (FPWM) at light load. FPWM reduces noise and RF interference, while PFM provides higher efficiency by reducing switching losses at light loads.

An array of protection features, including input Undervoltage Lockout (UVLO), Overcurrent Protection (OCP), output Overvoltage Protection (OVP), and Over-Temperature Protection (OTP), ensures safe operations under abnormal operating conditions.

The RAA210030 is available in a compact RoHS compliant 3mm×3mm×1.08mm (1.15mm MAX) dual flat embedded laminate package.

## Features

- 3A complete power supply
  - Integrates controller, gate driver, MOSFETs, and inductor
- 2.7V to 5.5V input voltage range
- Adjustable output voltage
  - As low as 0.6V with ±1.5% accuracy over line, load, and temperature
  - Up to 95% efficiency
- Default 2MHz current mode control operation
  - 500kHz to 4MHz resistor adjustable
  - External synchronization up to 4MHz
  - 100% duty cycle
- Dedicated enable pin and power-good flag
- Internal 1ms soft-start time
- Selectable PFM or FPWM mode
- Soft-stop output discharge
- UVLO, OCP, negative OCP, OVP, and OTP
  - OCP/Short-Circuit Protection (SCP) hiccup mode
- Compact RoHS compliant 3mm×3mm×1.08mm (1.15mm Max) 10 lead dual flat embedded laminate package

## Applications

- Telecom, Industrial, optical, and medical equipment
- Point-of-load conversions
- MCU, MPU, DSP, and FPGA

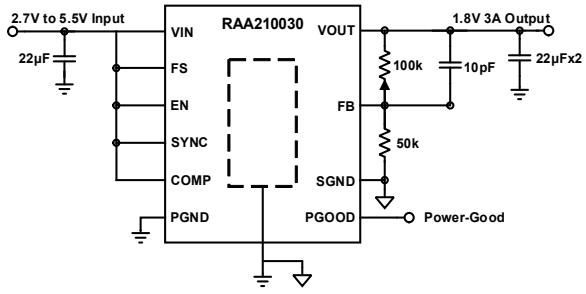



**Figure 1. Typical Application Circuit**

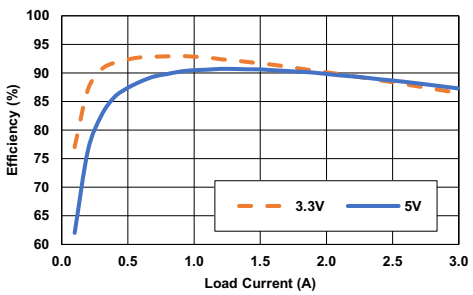



**Figure 2. Efficiency $V_{OUT}$ = 1.8V, PWM Mode**

# Contents

# 1. Overview

## 1.1 Typical Application Circuits

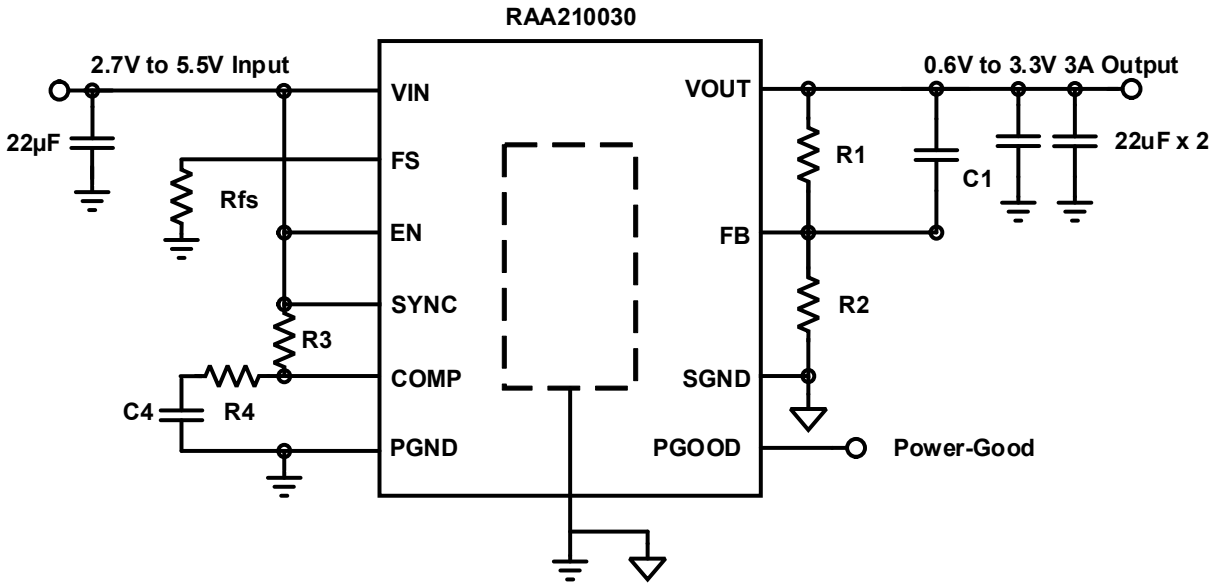



**Figure 3. Typical Application Circuit for $V_{IN}$ = 2.7V to 5.5V and $V_{OUT}$ = 0.6V to 3.3V**

## 1.2 Block Diagram

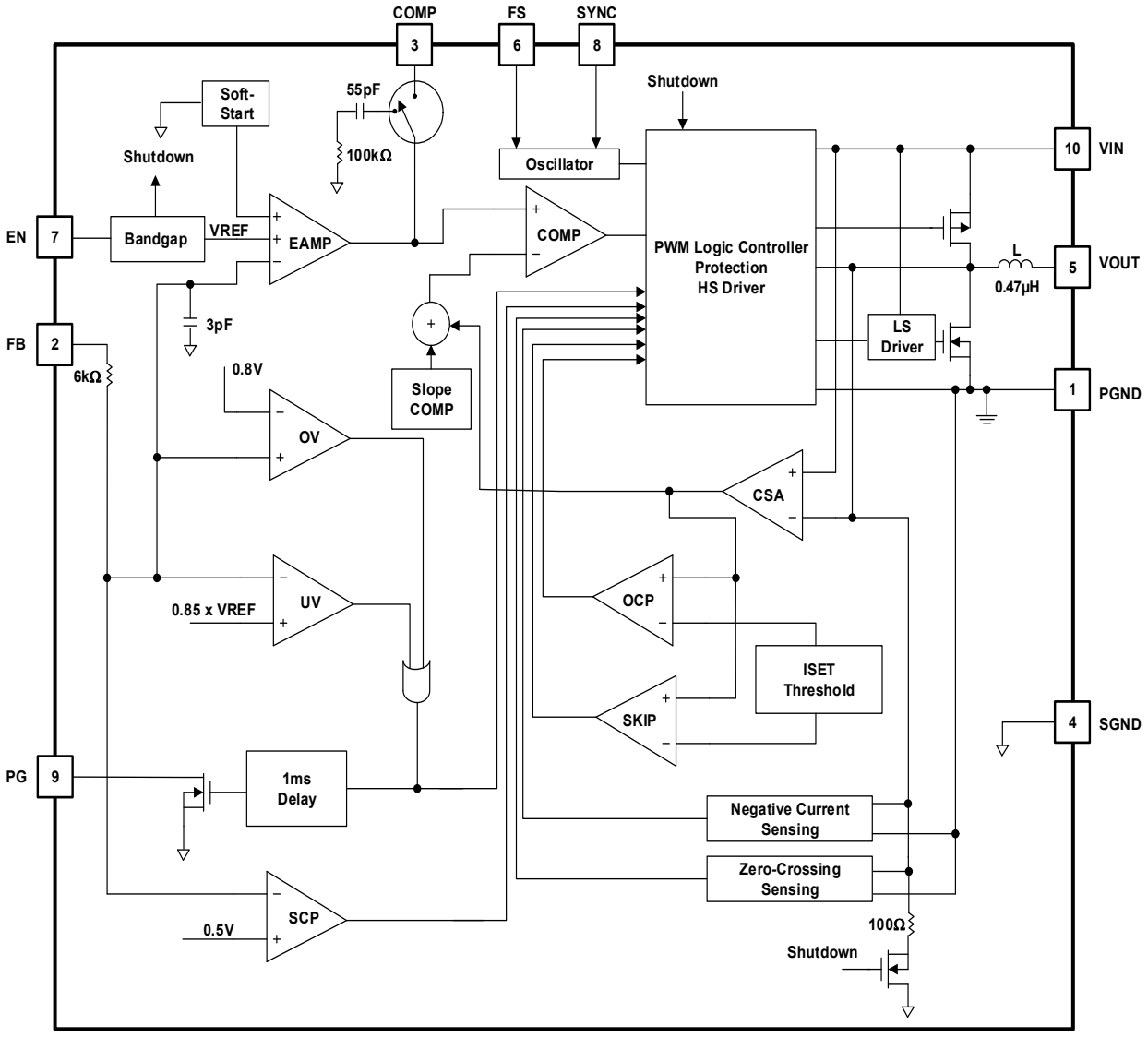
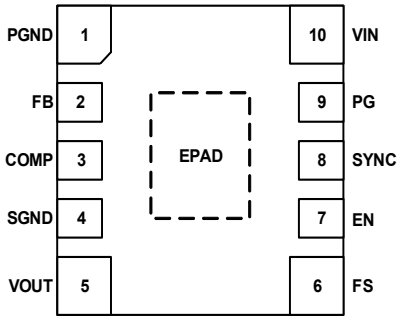


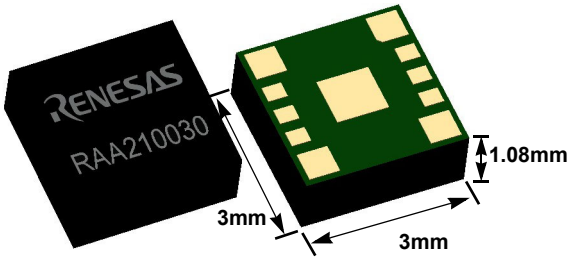

**Figure 4. Block Diagram**

# 2. Pin Information

## 2.1 Pin Assignments




Top View




## 2.2 Pin Descriptions

| Pin Number | Pin Name | Function |
|---|---|---|
| 1 | PGND | Power ground. Connect it close to the (-) terminals of the external input capacitors and output capacitors. |
| 2 | FB | Voltage setting pin. The module output voltage is set by an external resistor divider connected to FB. With a properly selected divider, the output voltage is set to any voltage between 0.6V and 5V. Renesas also recommends placing a ceramic capacitor in parallel to ensure system stability at extreme operation conditions. Table 1 lists for the resistor and capacitor values for various typical output voltages. |
| 3 | COMP | Compensation pin. COMP is the output of the transconductance error amplifier. For most applications, directly connect COMP to VIN to select internal compensation to stabilize the system and achieve an optimal transient response. For applications where external compensation is required, connect COMP to SGND with an external compensation network. |
| 4 | SGND | Signal ground. Must connect it to EPAD for proper electrical performance. See Layout Guidelines for more information. |
| 5 | VOUT | Power output of the module. Place the output capacitors as close as possible to the module output. See Layout Guidelines for more information. |
| 6 | FS | Frequency selection pin. This pin sets the module switching frequency by connecting a resistor to SGND. The frequency of operation can be programmed between 500kHz to 4MHz. The default frequency is 2MHz if FS is connected to VIN. |
| 7 | EN | Module enable pin. Enable the module by driving EN high. Shuts down the module and discharge the output capacitor when driven low. Typically tied to VIN directly. **Note:** Do not leave this pin floating. |
| 8 | SYNC | Mode Selection pin. Connect to logic high or input voltage VIN for FPWM mode. Connect to logic low or ground for PFM mode. Drive with a 500kHz to 4MHz square wave for external synchronization. There is an internal 1MΩ pull-down resistor to prevent an undefined logic state in case of SYNC pin float. |
| 9 | PG | Power-good pin. Power-good is an open-drain output. Use a 10kΩ to 100kΩ pull-up resistor connected between VIN and PG. During power-up or EN start-up, the PG rising edge is delayed by 1ms after the output is in regulation. |
| 10 | VIN | Power input of the module. Tie directly to the input rail between 2.7V~5.5V. **Note:** You must place minimum total 22µF input ceramic capacitors as close as possible to the module input. Add additional capacitance if possible. See Layout Guidelines for more information |
| - | EPAD | Power ground. Must connect it to SGND for proper electrical performance. Place as many vias as possible under the EPAD for optimal thermal performance. |

**Table 1. RAA210030 Design Guide Matrix (See Figure 3)**

| Case | $V_{IN}$ (V) | $V_{OUT}$ (V) | $R_1$ (kΩ) | $R_2$ (kΩ) | $R_3$ (kΩ) | $R_4$ (kΩ) | Freq (MHz) | $R_{FS}$ (kΩ) | $C_1$ (pF) | $C_4$ (pF) |
|---|---|---|---|---|---|---|---|---|---|---|
| 1 | 3.3 | 0.6 | 0.1 | Open | Open | 33 | 1 | 206 | Open | 680 |
| 2 | 3.3 | 0.8 | 33.2 | 100 | Open | 33 | 1.4 | 143 | Open | 680 |
| 3 | 3.3 | 0.9 | 50 | 100 | Open | 33 | 1.5 | 133 | Open | 680 |
| 4 | 3.3 | 1 | 66.5 | 100 | Open | 33 | 1.7 | 115 | Open | 680 |
| 5 | 3.3 | 1.2 | 100 | 100 | Open | 33 | 2 | 96 | Open | 680 |
| 6 | 3.3 | 1.5 | 100 | 66.5 | 0 | Open | 2 | 96 | 10 | Open |
| 7 | 3.3 | 1.8 | 100 | 50 | 0 | Open | 2 | 96 | 10 | Open |
| 8 | 3.3 | 2.5 | 100 | 31.6 | 0 | Open | 2 | 96 | Open | Open |
| 9 | 5 | 1 | 66.5 | 100 | Open | 33 | 1 | 206 | Open | 680 |
| 10 | 5 | 1.2 | 100 | 100 | Open | 33 | 1.4 | 143 | Open | 680 |
| 11 | 5 | 1.5 | 100 | 66.5 | 0 | Open | 1.7 | 115 | 10 | Open |
| 12 | 5 | 1.8 | 100 | 50 | 0 | Open | 2 | 96 | 10 | Open |
| 13 | 5 | 2.5 | 100 | 31.6 | 0 | Open | 2 | 96 | Open | Open |
| 14 | 5 | 3.3 | 100 | 22.1 | 0 | Open | 2 | 96 | Open | Open |

**Table 2. Recommended Input/Output Capacitor**

| Name | Vendor | Value | Part Number | Number |
|---|---|---|---|---|
| Input Capacitor | Murata | 22µF, 10V, 0603, X5R | GRM188R61A226ME15D | 1 |
| | TDK | 22µF, 10V, 0603, X5R | C1608X5R1A226M080AC | 1 |
| Output Capacitor | Murata | 22µF, 6.3V, 0402, X5R | GRM158R60J226ME01D | 2 |
| | TDK | 22µF, 10V, 0603, X5R | C1608X5R1A226M080AC | 2 |

# 3. Specifications

## 3.1 Absolute Maximum Ratings

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| VIN to PGND | -0.3 | +5.8 (DC) or +7V (20ms) | V |
| EN, FS, PG, FB, SYNC, COMP to SGND | -0.3 | $V_{IN}$ + 0.3 | V |
| VOUT to PGND | -0.3 | $V_{IN}$ + 0.3 | V |
| Maximum Storage Temperature Range | -65 | +150 | °C |
| Human Body Model (Tested per JS-001-2017) | - | 3.5 | kV |
| Charged Device Model (Tested per JS-002-2018) | - | 2 | kV |
| Latch-Up (Tested per JESD78E; Class 2, Level A, +125°C) | - | 100 | mA |

## 3.2 Thermal Information

| Parameter | Package | Symbol | Conditions | Typical Value | Unit |
|---|---|---|---|---|---|
| Thermal Resistance | 10 Ld Dual Flat Embedded Laminate Package | $\theta_{JA}$[1] | Junction to air | 33.84 | °C/W |
| | | $\theta_{JC}$[2] | Junction to case | 16.4 | °C/W |

1. $\theta_{JA}$ is measured in free air with the module mounted on a 4-layer thermal test board 3x4.5 inch in size with significant coverage of 2oz Cu on both top and bottom layers, and 1oz Cu on internal layers, with numerous vias.
2. For $\theta_{JC}$, the case temperature location is the center of the exposed metal pad on the package underside.

## 3.3 Recommended Operating Conditions

| Parameter | Minimum | Maximum | Unit |
|---|---|---|---|
| VIN to GND | 2.7 | 5.5 | V |
| Output Voltage, $V_{OUT}$ | 0.6 | 5 | V |
| Output Current, $I_{OUT}$ | 0 | 3 | A |
| Junction Temperature Range, $T_J$ | -40 | +125 | °C |

## 3.4 Electrical Specifications

Unless otherwise noted, all parameter limits are established across the recommended operating conditions and the specification limits are measured at the following conditions: $T_A$= -40°C to +125°C**,** $V_{IN}$ = 3.6V, $V_{OUT}$ = 1.2V, unless otherwise noted. Typical specifications are measured at $T_A$= +25°C. **Boldface limits apply across the internal junction temperature range, -40°C to +125°C.**

| Parameter | Symbol | Test Conditions | Min[1] | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|
| **Module Input Supply** | | | | | | |
| Input Voltage Range | $V_{IN}$ | | **2.7** | | **5.5** | V |
| $V_{IN}$ Undervoltage Lockout Threshold | $V_{UVLO}$ | Rising, no load | | 2.5 | 2.7 | V |
| | | Falling, no load | 2.2 | 2.45 | | V |
| Quiescent Supply Current | $I_{VIN}$ | SYNC = $V_{IN}$ = 3.6V, $f_{SW}$ = 2MHz, EN = high, $I_{OUT}$ = 0A | | 19 | 25 | mA |
| | | SYNC = $V_{IN}$= 5V, $f_{SW}$ = 2MHz, EN = high, $I_{OUT}$ = 0A | | 23 | 30 | mA |
| Shutdown Supply Current | $I_{SD}$ | SYNC = $V_{IN}$ = 5.5V, EN = low | | 4.5 | 10 | µA |
| **Output Regulation** | | | | | | |
| Output Continuous Current Range[2] | $I_{OUT}$ | | **0** | | **3** | A |
| Output Voltage Range[2] | $V_{OUT\_RANGE}$ | | **0.6** | | **5** | V |
| Output Voltage Accuracy[2] | $V_{OUT\_ACCY}$ | Total variation with line, load, and temperature (-40°C ≤ $T_J$ ≤ +125°C) | **-1.5** | | **1.5** | % |
| Line Regulation[2] | $\Delta V_{OUT}$/ $V_{OUT\_SET}$ | $V_{IN}$ from 2.7V to 5.5V, $I_{OUT}$ = 0A | **-1** | | **1** | % |
| Load Regulation[2] | $\Delta V_{OUT}$/ $V_{OUT\_SET}$ | From 0A to 3A, $V_{IN}$ = 5V | **-1** | | **1** | % |
| Output Ripple Voltage | $V_{OUT(AC)}$ | $V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 3A, $f_{SW}$ = 2MHz, 22µF×2 ceramic capacitor | | 8 | | $mV_{P-P}$ |
| **Dynamic Characteristics** | | | | | | |
| Voltage Change of Positive Load Step | $V_{OUT\_DP}$ | Current slew rate = 2.5A/µs, $V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 0A to 3A, 22µF×2 ceramic capacitor | | 63 | | mV |
| Voltage Change of Negative Load Step | $V_{OUT\_DN}$ | Current slew rate = 2.5A/µs, $V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 0A to 3A, 22µF×2 ceramic capacitor | | 63 | | mV |
| **Current Protection** | | | | | | |
| Current Limit Blanking Time | $t_{OCON}$ | | | 17 | | clock pulses |
| Hiccup Time | $t_{HICCUP}$ | | | 8 | | ms |
| Positive Peak Current Limit | $I_{PLIMIT}$ | | 3.7 | 4.9 | 6.6 | A |
| Skip Current Limit | $I_{SKIP}$ | See Figure 34 for more detail. | 0.6 | 0.9 | 1.3 | |
| Negative Current Limit | $I_{NLIMIT}$ | | -6 | -3 | -0.6 | A |

| Parameter | Symbol | Test Conditions | Min[1] | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|
| **EN Threshold** | | | | | | |
| Logic Input Low | | | | | **0.4** | V |
| Logic Input High | | | **0.9** | | | V |
| EN Logic Input Leakage Current | | Pulled up to 3.6V | | 0.1 | **1** | µA |
| **Default Internal Soft-Starting** | | | | | | |
| Default Internal Output Ramping Time | $t_{SS}$ | SS = SGND | | 1 | | ms |
| **Power-Good** | | | | | | |
| Output Low Voltage | | $I_{PG}$ = 1mA | | | **0.3** | V |
| PG Delay Time (Rising Edge) | $t_{PGR}$ | Time from $V_{OUT}$ reached regulation | **0.5** | 1 | **2** | ms |
| PG Delay Time (Falling Edge) | $t_{PGF}$ | | | 6.5 | | µs |
| PG Leakage Current | $I_{PGLKG}$ | PG = 3.6V | | 10 | **100** | nA |
| OVP PG Rising Threshold | $V_{PGR\_OVP}$ | | | 0.8 | | V |
| UVP PG Rising Threshold | $V_{PGR\_UVP}$ | | **80** | 86 | **90** | % |
| UVP PG Hysteresis | | | | 5.4 | | % |
| **Reference Section** | | | | | | |
| Internal Reference Voltage | $V_{REF}$ | | | 0.600 | | V |
| FB Bias Current | $I_{FBLKG}$ | FB = 0.75V | | 0.1 | | µA |
| **Compensation** | | | | | | |
| Error Amplifier Transconductance | | Internal Compensation | | 126 | | µA/V |
| | | External Compensation | | 132 | | µA/V |
| Current Sense Gain | | | **0.145** | 0.2 | **0.25** | Ω |
| **PWM Regulator** | | | | | | |
| Maximum Duty Cycle | $d_{MAX}$ | | | 100 | | % |
| Minimum On-Time | $t_{ON\_MIN}$ | SYNC = high | | | **105** | ns |
| **Oscillator** | | | | | | |
| Switching Frequency | $f_{SW}$ | $f_{SW}$ = 2MHz | **1.6** | 2 | **2.4** | MHz |
| | | $R_{FS}$ = 402kΩ | | 0.5 | | MHz |
| | | $R_{FS}$ = 42.2kΩ | | 4 | | MHz |
| **Synchronization** | | | | | | |
| SYNC Synchronization Range | $f_{SYNC}$ | | **0.5** | | **4** | MHz |
| SYNC Logic Low-to-High Transition Range | | | 0.67 | 0.76 | 0.84 | V |
| SYNC Hysteresis | | | | 0.17 | | V |
| SYNC Logic Input Leakage Current | | $V_{IN}$ = 3.6V | | 4 | 5 | µA |

| Parameter | Symbol | Test Conditions | Min[1] | Typ | Max[1] | Unit |
|---|---|---|---|---|---|---|
| **Over-Temperature** | | | | | | |
| Over-Temperature Shutdown | $T_{OT-TH}$ | | | 150 | | °C |
| Over-Temperature Hysteresis | $T_{OT-HYS}$ | | | 25 | | °C |

1. Compliance to datasheet limit is assured by one or more methods: production test, characterization, and/or design.
2. Compliance to limits is assured by characterization and design.

# 4. Typical Performance Curves

## 4.1 Efficiency Performance

Operating condition: $T_A$ = +25°C, no air flow. Typical values are used unless otherwise noted.

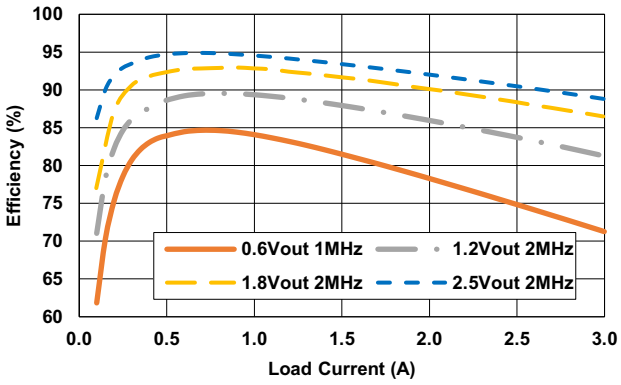



**Figure 5. $V_{IN}$ = 3.3V, FPWM**

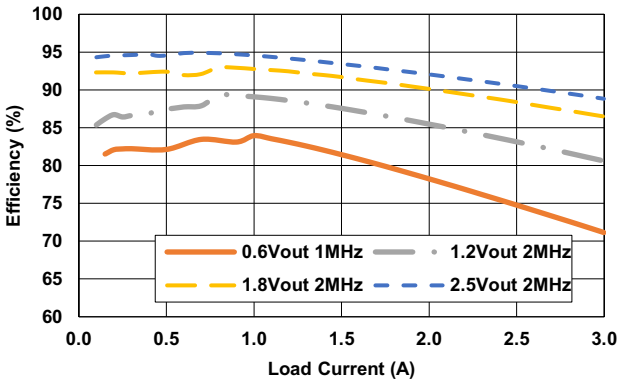



**Figure 6. $V_{IN}$ = 3.3V, PFM**

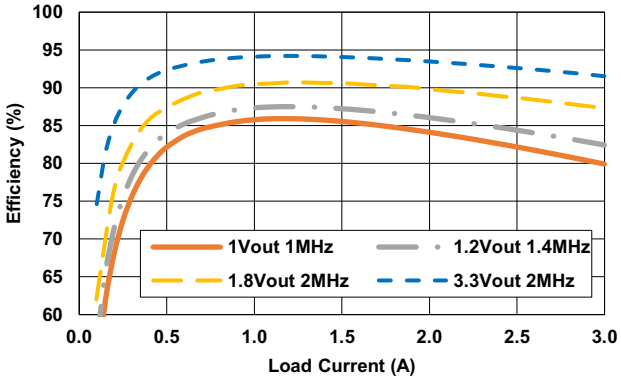



**Figure 7. $V_{IN}$ = 5V, FPWM**

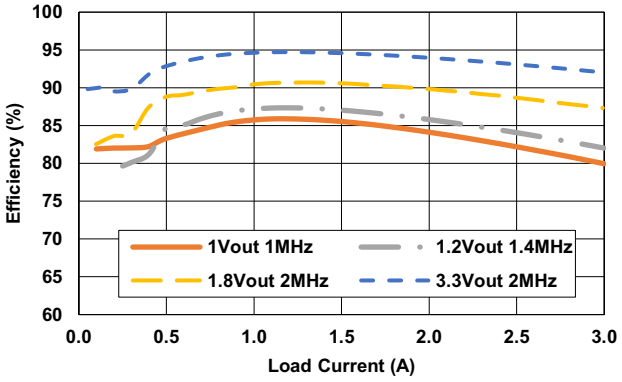



**Figure 8. $V_{IN}$ = 5V, PFM**

## 4.2 Output Voltage Ripple

Operating condition: $T_A$ = +25°C, no air flow, FPWM mode. Typical values are used unless otherwise noted.

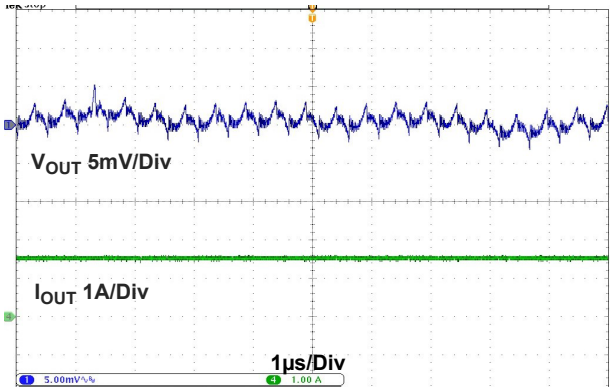



**Figure 9. Output Ripple, $V_{IN}$ = 3.3V, $V_{OUT}$ = 1.8V, $f_{SW}$ = 2MHz, Half Load, $C_{OUT}$ = 22µFx2 Ceramic**

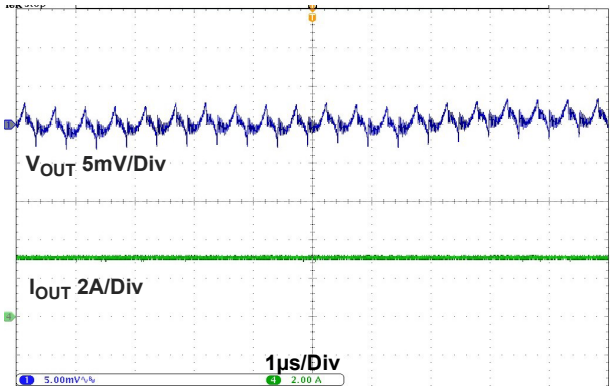



**Figure 10. Output Ripple, $V_{IN}$ = 3.3V, $V_{OUT}$ = 1.8V, $f_{SW}$ = 2MHz, Full Load, $C_{OUT}$ = 22µFx2 Ceramic**

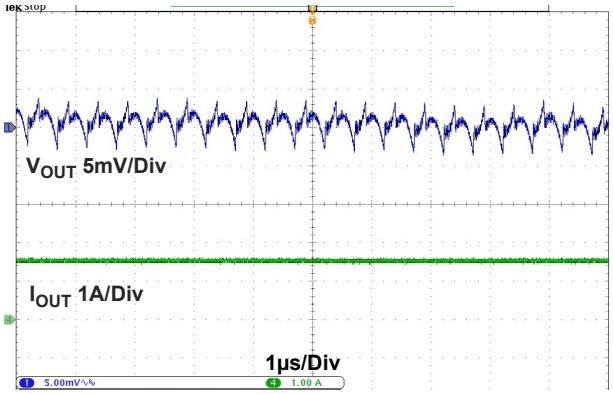



**Figure 11. Output Ripple, $V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $f_{SW}$ = 2MHz, Half Load, $C_{OUT}$ = 22µFx2 Ceramic**

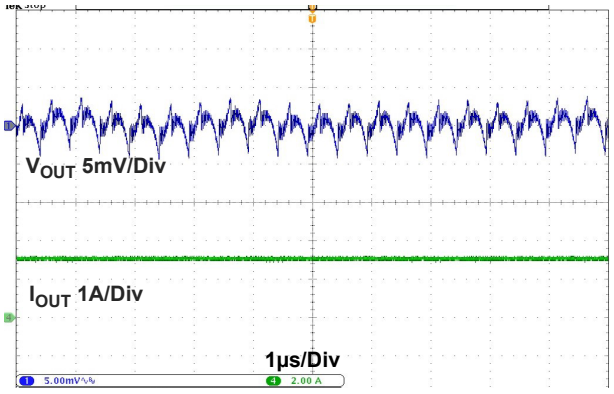



**Figure 12. Output Ripple, $V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $f_{SW}$ = 2MHz, Full Load, $C_{OUT}$ = 22µFx2 Ceramic**

## 4.3 Load Transient Response Performance

Operating condition: $T_A$ = +25°C, no air flow, $C_{OUT}$ = 2×22µF, 2.5A/µs step load. Typical values are used unless otherwise noted.

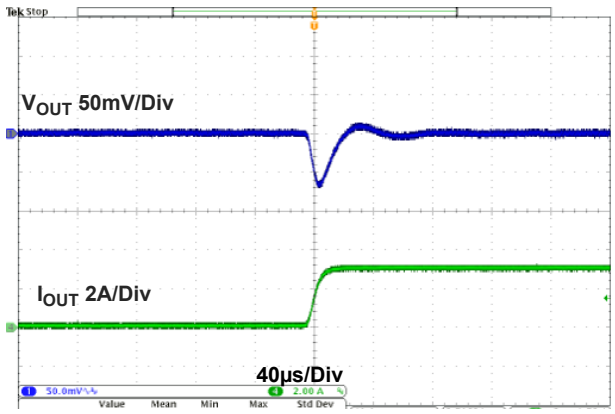



**Figure 13. $V_{IN}$ = 3.3V, $V_{OUT}$ = 1.8V, $f_{SW}$ = 2MHz, 0A⟶3A, FPWM**

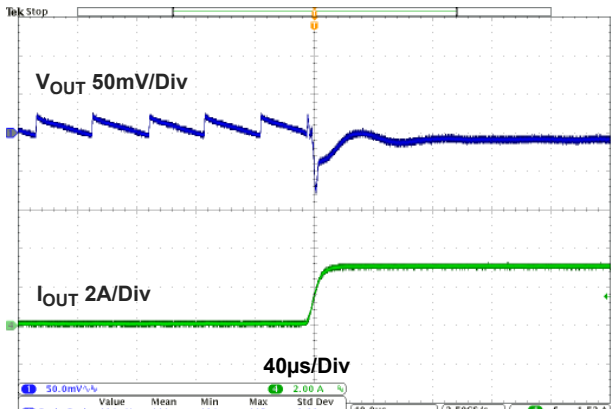



**Figure 14. $V_{IN}$ = 3.3V, $V_{OUT}$ = 1.8V, $f_{SW}$ = 2MHz, 0A⟶3A, PFM**

Operating condition: $T_A$ = +25°C, no air flow, $C_{OUT}$ = 2×22µF, 2.5A/µs step load. Typical values are used unless otherwise noted.

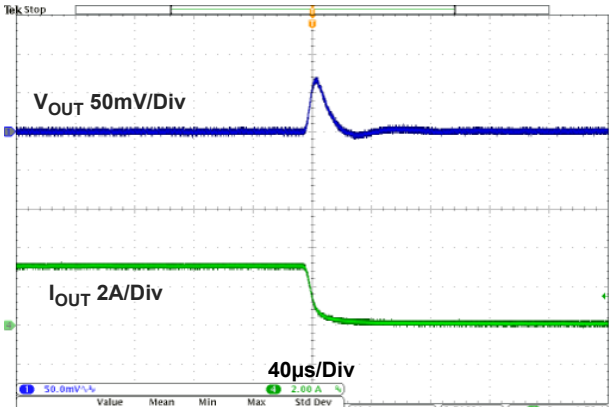



**Figure 15. $V_{IN}$ = 3.3V, $V_{OUT}$ = 1.8V, $f_{SW}$ = 2MHz, 3A⟶0A, FPWM**

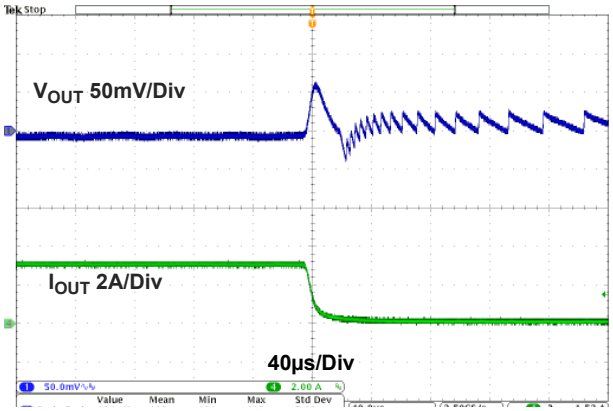



**Figure 16. $V_{IN}$ = 3.3V, $V_{OUT}$ = 1.8V, $f_{SW}$ = 2MHz, 3A⟶0A, PFM**

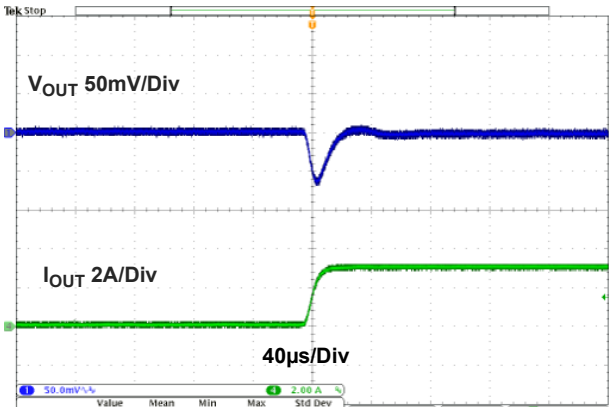



**Figure 17. $V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $f_{SW}$ = 2MHz, 0A⟶3A, FPWM**

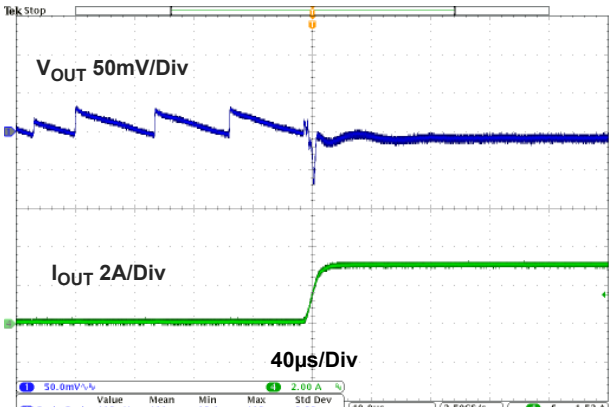



**Figure 18. $V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $f_{SW}$ = 2MHz, 0A⟶3A, PFM**

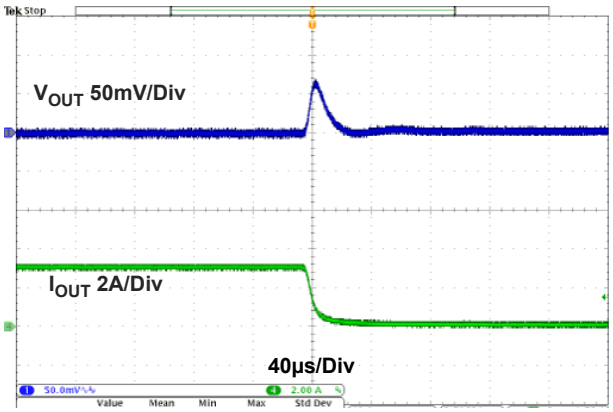



**Figure 19. $V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $f_{SW}$ = 2MHz, 3A⟶0A, FPWM**

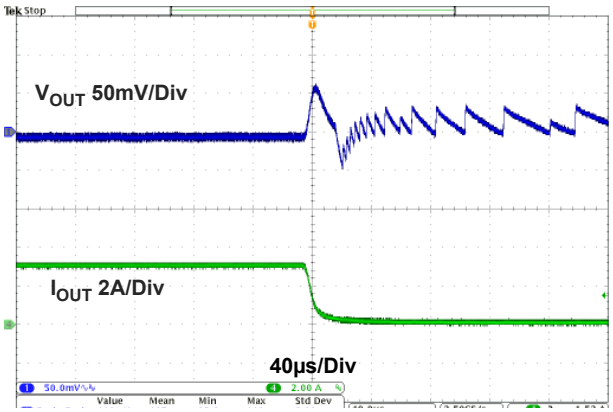



**Figure 20. $V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $f_{SW}$ = 2MHz, 3A⟶0A, PFM**

## 4.4 Start-Up and Shutdown Waveforms

Operating condition: $T_A$ = +25°C,FPWM mode, no air flow. Typical values are used unless otherwise noted.

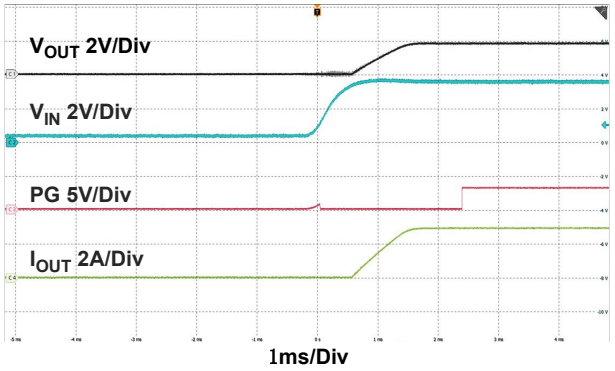



**Figure 21. $V_{IN}$ Start-Up Waveforms; $V_{IN}$ = 3.3V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 3A**

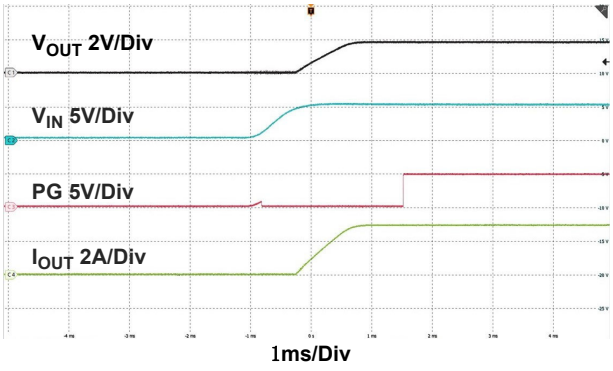



**Figure 22. $V_{IN}$ Start-up Waveforms; $V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 3A**

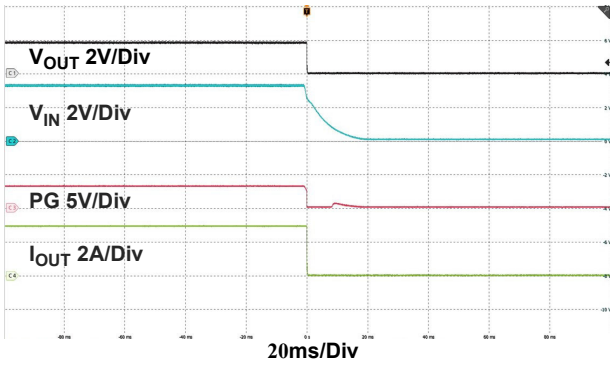



**Figure 23. VIN Shutdown Waveforms; $V_{IN}$ = 3.3V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 3A**

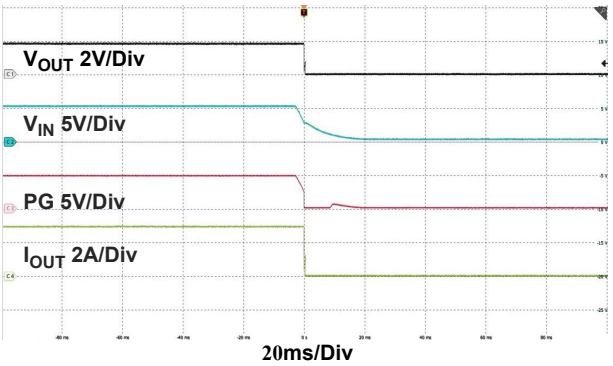



**Figure 24. VIN Shutdown Waveforms; $V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 3A**

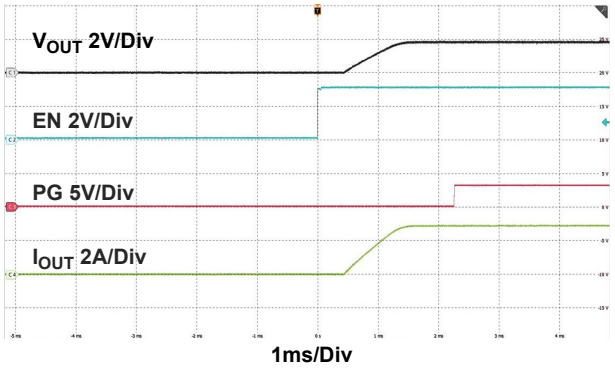



**Figure 25. EN Start-Up Waveforms; $V_{IN}$ = 3.3V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 3A**

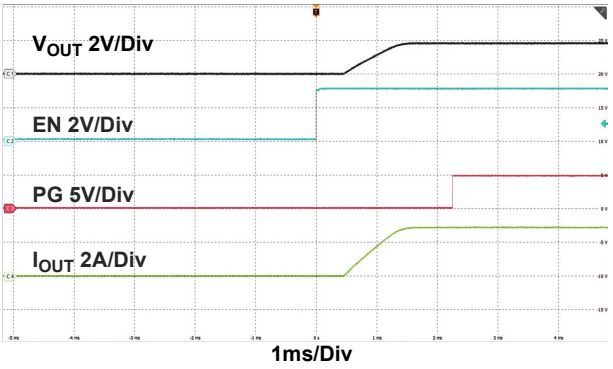



**Figure 26. EN Start-up Waveforms; $V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 3A**

Operating condition: $T_A$ = +25°C,FPWM mode, no air flow. Typical values are used unless otherwise noted. (Cont.)

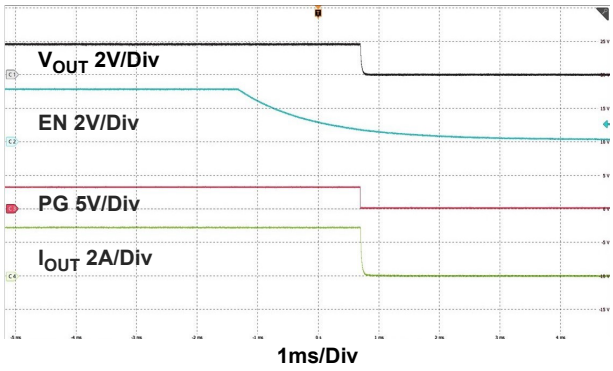



**Figure 27. EN Shutdown Waveforms; $V_{IN}$ = 3.3V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 3A**

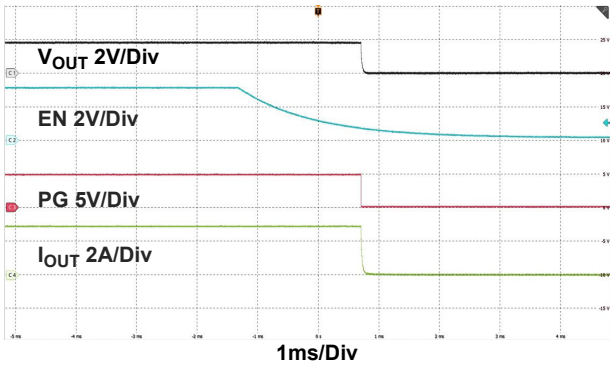



**Figure 28. EN Shutdown Waveforms; $V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $I_{OUT}$ = 3A**

## 4.5 Derating

FPWM operation. All of the following curves were plotted at $T_J$ = +120°C.

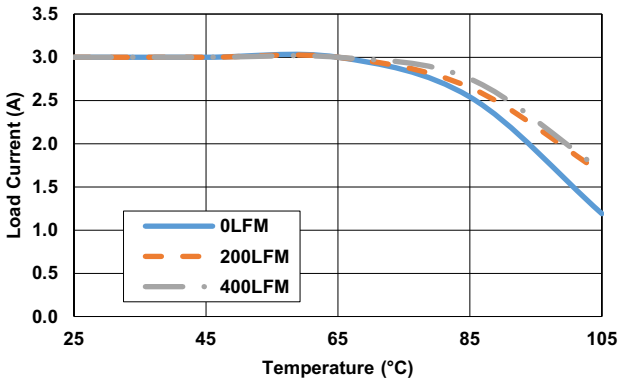



**Figure 29. $V_{IN}$ = 3.3V, $V_{OUT}$ = 1.2V, $f_{SW}$ = 2MHz**

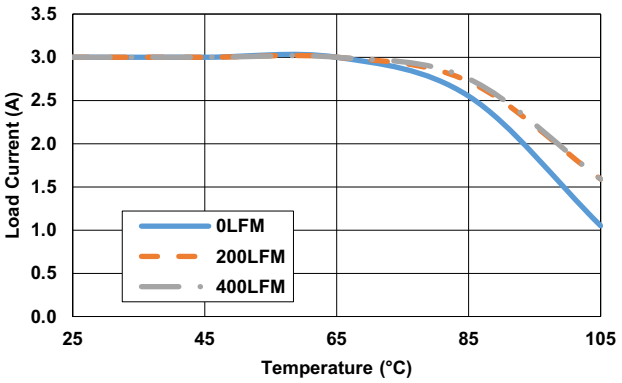



**Figure 30. $V_{IN}$ = 5V, $V_{OUT}$ = 1.2V, $f_{SW}$ = 1.4MHz**

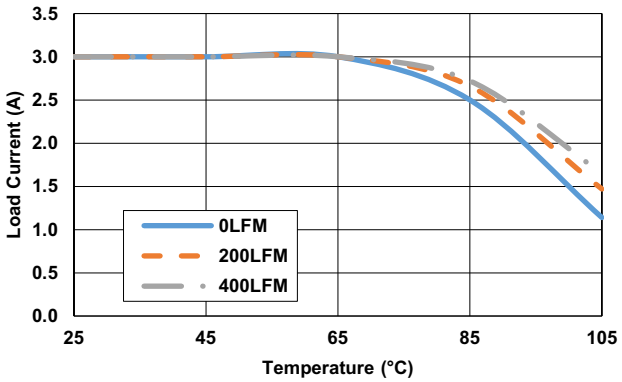



**Figure 31. $V_{IN}$ = 3.3V, $V_{OUT}$ = 1.8V, $f_{SW}$ = 2MHz**

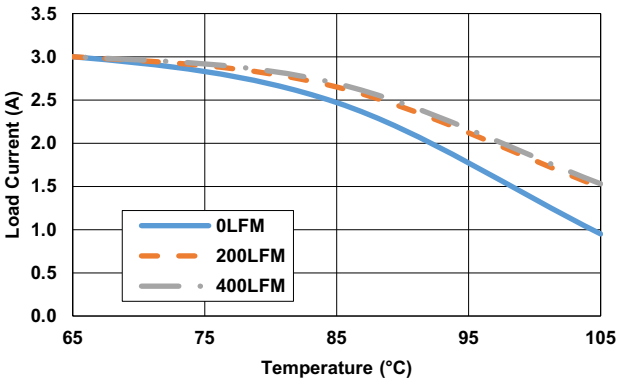



**Figure 32. $V_{IN}$ = 5V, $V_{OUT}$ = 1.8V, $f_{SW}$ = 2MHz**

# 5. Functional Description

The RAA210030 is a compact 3A step-down high efficiency power module optimized for space constrained applications. The module switches at 2MHz by default when the FS pin is shorted to VIN. The switching frequency is also adjustable from 500kHz to 4MHz through a resistor, $R_{FS}$, from FS to SGND. Peak current mode control scheme is implemented for a fast transient response. By shorting the COMP pin to VIN, the module uses internal compensation to stabilize the system and optimize transient response. Other features include soft-stop output discharge, external synchronization, 100% duty cycle operation, and low quiescent current.The supply current is typically only 4.5µA when the module is shut down.

## 5.1 PWM Control Scheme

The RAA210030 employs peak current-mode Pulse-Width Modulation (PWM) for fast transient response and pulse-by-pulse current limiting. Pulling the SYNC pin high (>0.8V) forces the module into FPWM mode. As shown in Figure 4, the current loop consists of the oscillator, PWM comparator, a current-sensing circuit, and slope compensation for the current loop stability. The slope compensation is 440mV/Ts, which changes with frequency. The gain for the current-sensing circuit is typically 200mV/A. The control reference for the current loops comes from the output of the Error Amplifier (EAMP).

The PWM operation is initialized by the clock from the oscillator. The P-channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the Current-Sense Amplifier (CSA) and the slope compensation reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-channel MOSFET and turn on the N-channel MOSFET. The N-channel MOSFET stays on until the end of the PWM cycle. Figure 33 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the slope compensation ramp and the output of the CSA.

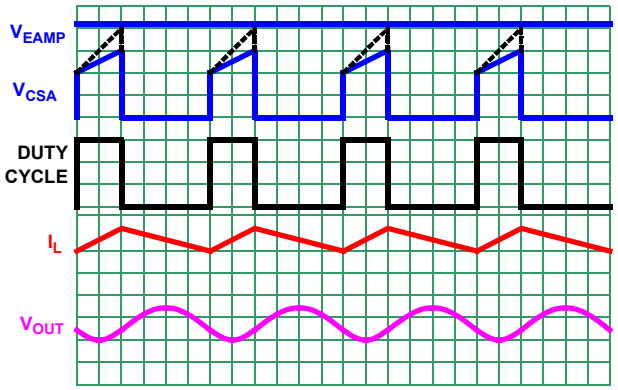



**Figure 33. PWM Operation Waveforms**

The output voltage is regulated by controlling the $V_{EAMP}$ voltage to the current loop. The band-gap circuit outputs a 0.6V reference voltage to the voltage loop. The feedback signal comes from the FB pin. The soft-start block only affects the operation during start-up and is discussed separately, see Soft Start-Up. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. When the COMP is tied to VIN, the voltage loop is internally compensated with the 55pF and 100kΩ RC network.

## 5.2 SKIP MODE

Pulling the SYNC pin low(<0.4V) forces the converter into PFM mode. The RAA210030 enters a pulse-skipping mode at light load to minimize the switching loss by reducing the switching frequency. Figure 34 illustrates the skip-mode operation. A zero-cross sensing circuit shown in Figure 4 monitors the N-channel MOSFET current for zero crossing. When 16 consecutive cycles are detected, the regulator enters the skip mode. During the sixteen detecting cycles, the current in the inductor is allowed to become negative. The counter is reset to zero when the current in any cycle does not cross zero. When the skip mode is entered, the pulse modulation starts being

controlled by the SKIP comparator shown in Figure 4. Each pulse cycle is still synchronized by the PWM clock. The P-channel MOSFET is turned on at the rising edge of the clock and turned off when the output is higher than 2% of the nominal regulation or when its current reaches the peak Skip current limit value. Then, the inductor current stays at zero (the internal clock is disabled), and the output voltage reduces gradually because of the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the P-channel MOSFET is turned on again at the rising edge of the internal clock as it repeats the previous operations. The regulator resumes normal FPWM mode operation when the output voltage drops 2% below the nominal voltage.

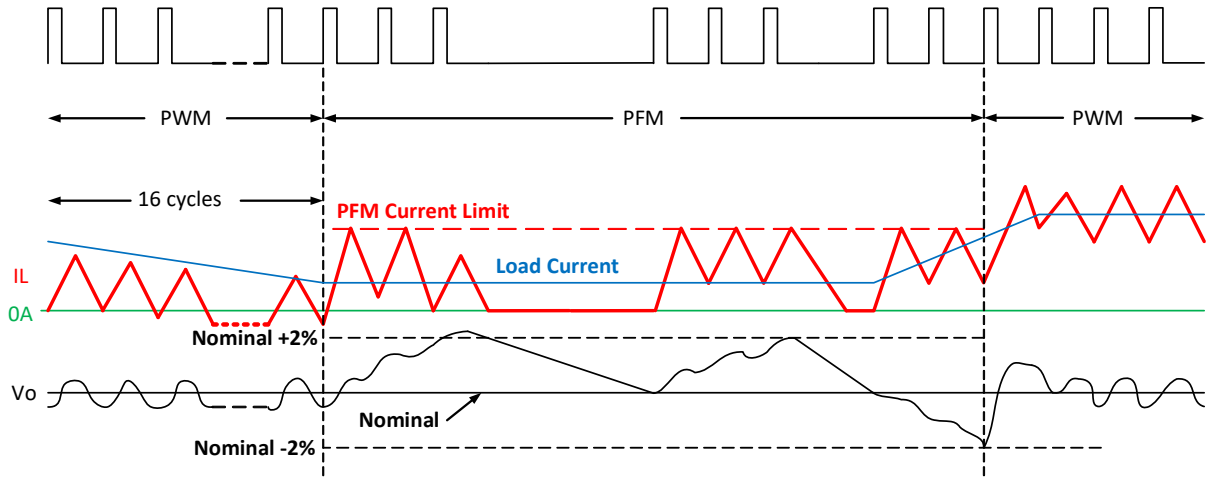



**Figure 34. Skip Mode Operation Waveforms**

## 5.3 Frequency Adjustment

The switching frequency of RAA210030 is adjustable ranging from 500kHz to 4MHz using a simple resistor $R_{FS}$ across FS to SGND. The switching frequency setting is based on Equation 1:

**(EQ. 1)** $$R_{FS}[k\Omega] = \frac{220 \cdot 10^3}{f_{OSC}[kHz]} - 14$$

When the FS pin is directly tied to VIN, the frequency of operation is fixed at 2MHz. See Table 1 to help with the selection of switching frequency for typical operation conditions. More detailed information on recommended switching frequency is provided in the Switching Frequency Selection section.

## 5.4 Overcurrent Protection (OCP)

The overcurrent protection is implemented by monitoring the CSA output with the OCP comparator, as shown in Figure 4. The current-sensing circuit has a gain of 200mV/A, from the P-channel MOSFET current to the CSA output. When the CSA output reaches the threshold, the OCP comparator is tripped and turns off the P-channel MOSFET immediately. The overcurrent function protects the module from a shorted output by monitoring the current flowing through the P-channel MOSFET.

With the detection of an overcurrent condition, the P-channel MOSFET is immediately turned off and is not turned on again until the next switching cycle. With the detection of the initial overcurrent condition, the overcurrent fault counter is set to 1. During the subsequent cycle, if another overcurrent condition is detected, the OC fault counter is incremented. If there are 17 sequential OC fault detections, the module shuts down under an overcurrent fault condition. An overcurrent fault condition results in the module attempting to restart in Hiccup mode within the delay of eight soft-start periods. At the end of the eighth soft-start wait period, the fault counters are reset and soft-start is attempted again. If the overcurrent condition goes away during the delay of eight soft-start periods, the output resumes back into regulation after the Hiccup mode expires as shown in Figure 35.

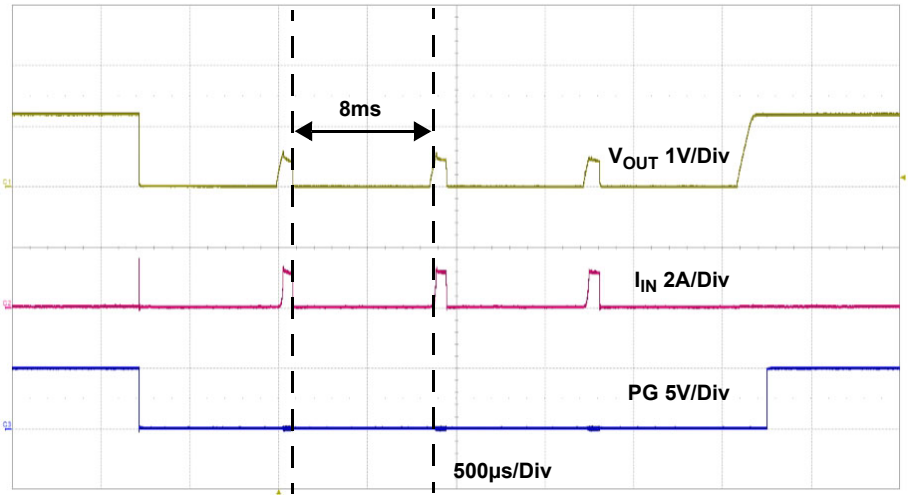



**Figure 35. OCP Response: Output Short-Circuited from No Load to Ground and Released, $V_{OUT}$ = 1.2V**

## 5.5 Negative Current Protection

Similar to overcurrent, the negative current protection is realized by monitoring the current across the low-side N-channel MOSFET, as shown in Figure 4. When the valley point of the inductor current reaches -3A for four consecutive cycles, both P-channel MOSFET and N-channel MOSFET are turned off. The 100Ω in parallel to the N-channel MOSFET activates discharging the output into regulation. The control begins to switch when output is within regulation.

## 5.6 Power-Good

Power-Good (PG) is the open-drain output of a window comparator that continuously monitors the module output voltage. PG is actively held low when EN is low and during the module soft-start period. After the 1ms delay of the soft-start period, PG becomes high impedance as long as the output voltage is within the nominal regulation voltage set by $V_{FB}$. During an output overvoltage fault condition (output voltage is 33% higher than nominal value) or an output undervoltage fault condition (output voltage is 15% lower than nominal value), PG is pulled low. Any fault condition forces PG low until the fault condition is cleared during soft-start. For logic level output voltages, connect an external pull-up resistor between PG and VIN. A 100kΩ resistor works well in most applications.

## 5.7 Undervoltage Lockout (UVLO)

When the input voltage is below the Undervoltage Lockout (UVLO) threshold, the module is disabled.

## 5.8 Soft Start-Up

The soft start-up reduces the inrush current during start-up. The soft-start block outputs a ramp reference to the input of the error amplifier. This voltage ramp limits the inductor current and the output voltage rise time so that the output voltage rises in a controlled fashion. When VFB is less than 0.1V at the beginning of the soft-start, the switching frequency is reduced to 200kHz, so that the output can start-up smoothly at light load condition. The RAA210030 supports pre-biased output condition during soft start-up. The default soft start-up period is approximately 1ms.

## 5.9 External Synchronization Control

The operating frequency can be synchronized up to 4MHz by an external signal applied to the SYNC pin. The rising edge of SYNC signal triggers the rising edge of PWM ON pulse. To ensure proper operation, Renesas recommends using an external SYNC frequency within ±25% of the switching frequency set by the FS pin.

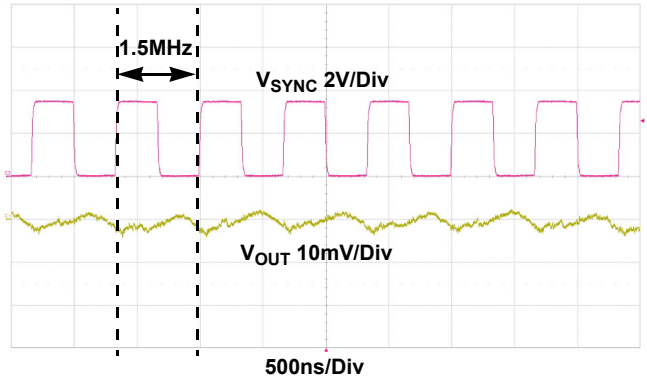



**Figure 36. External Frequency Synchronization Waveform, $V_{IN}$ = 5V, $V_{OUT}$ = 1.2V, $f_{SYNC}$ = 1.5MHz, $I_{OUT}$ = 0A**

## 5.10 Enable

The enable (EN) input allows you to control the turning on or off of the module for purposes such as power-up sequencing. When the module is enabled, there is typically a 600µs delay for waking up the band-gap reference and then the soft start-up begins. EN should be held below the logic input low until $V_{IN}$ exceeds $V_{UVLO}$ rising threshold.

## 5.11 Discharge Mode (Soft-Stop)

When a transition to shutdown mode occurs or the $V_{IN}$ UVLO is set, the discharge function is to ensure a defined down-ramp of the output voltage and keep the output voltage close to 0V. The output voltage is discharged to SGND through an internal 100Ω switch.

## 5.12 100% Duty Cycle

The RAA210030 features a 100% duty cycle operation to minimize switching loss. When the input voltage drops to a level that the RAA210030 can no longer maintain the regulation at the output, the module completely turns on the P-channel MOSFET. This is particularly useful in battery-powered applications to make full use of the battery voltage and maximize the operation time.

## 5.13 Thermal Shutdown

The RAA210030 has built-in thermal protection. When the internal temperature reaches +150°C, the module shuts down. Both MOSFETs are turned off and PG goes low. As the temperature drops to +125°C, the RAA210030 resumes operation by stepping through the soft-start.

# 6. Application Information

## 6.1 Output Voltage Programming

The output voltage of the module is programmed by an external resistor divider, $R_1$ and $R_2$ in Figure 3. $R_2$ combined with the internal 100kΩ 0.5% resistor connected from FB to VSENSE forms a resistor divider that sets the output voltage. The output voltage is governed by Equation 2.

**(EQ. 2)** $$V_{OUT} = V_{REF} \cdot \frac{R_2 + R_1}{R_2}$$

**Note:** The output voltage accuracy is also dependent on the resistor accuracy of $R_1$ and $R_2$. You need to select high accuracy resistors to achieve the overall output accuracy.

**Table 3. Output Voltage Resistor Settings**

| $V_{OUT}$ (V) | $R_1$ (kΩ) | $R_2$ (kΩ) |
|---|---|---|
| 0.6 | 0.1 | Open |
| 0.8 | 33.2 | 100 |
| 0.9 | 50 | 100 |
| 1.0 | 66.5 | 100 |
| 1.2 | 100 | 100 |
| 1.5 | 100 | 66.5 |
| 1.8 | 100 | 50 |
| 2.5 | 100 | 31.6 |
| 3.3 | 100 | 22.1 |

## 6.2 Switching Frequency Selection

With varieties of input and output voltage combinations, you must choose wisely on which frequency to operate at according to the specific applications. The selection of switching frequency for each $V_{IN}$ and $V_{OUT}$ combination needs to take into account a few trade-offs. Typically, lower switching frequency leads to higher efficiency at the cost of higher output voltage ripple. Do not decrease the switching frequency too low because of the negative current protection limit. Do not increase the switching frequency too high because of the minimum on-time limit, especially at low $V_{OUT}$. Moreover, when the output voltage is relatively high, low switching frequency results in more sub-harmonic oscillation. Therefore, operating frequency needs to be kept relatively high under high $V_{OUT}$ conditions. However, to ensure better thermal performance, limit any increase to the switching frequency.

## 6.3 Input Capacitor Selection

The selection of the input filter capacitor is based on how much ripple the supply can tolerate on the DC input line. The larger the capacitor, the less ripple expected, however, you need to consider the higher surge current during power-up. The RAA210030 provides a soft-start function that controls and limits the current surge. The total capacitance of the input capacitor is calculated using Equation 3:

**(EQ. 3)** $$C_{IN(MIN)} = \frac{I_O \bullet D(1-D)}{V_{P-P} \bullet f_{SW}}$$

where:

- $C_{IN(MIN)}$ is the minimum required input capacitance (µF)
- $I_O$ is the output current (A)
- D is the duty cycle
- $V_{P-P}$ is the allowable peak-to-peak voltage (V)
- $f_{SW}$ is the switching frequency (Hz)

Renesas recommends placing a low Equivalent Series Resistance (ESR) ceramic capacitor as close as possible to the module input. This input capacitor reduces voltage ringing created by the switching current across parasitic circuit elements. It also reduces the input noise seen by the module. Moreover, you need to consider the estimated RMS ripple current in choosing ceramic capacitors. The RMS ripple current is calculated using Equation 4.

**(EQ. 4)** $$I_{IN(RMS)} = \frac{Io\sqrt{D(1-D)}}{\eta}$$

See the capacitor datasheet for the RMS current ratings.

Based on the previous considerations, a minimum total input capacitance of 22µF is required for the RAA210030. Add additional capacitance if possible. Use ceramic capacitors. The placement of the input ceramic capacitors should be as close as possible to the module input. See PCB Layout Pattern Design for more information. A bulk input capacitance may also be needed if the input source does not have enough output capacitance. The typical value of bulk input capacitor is 47µF. In such conditions, this bulk input capacitance can supply the current during output load transient conditions.

## 6.4 Output Capacitor Selection

Ceramic capacitors with low ESR are typically used as the output capacitors for the RAA210030. To keep the low resistance up to high frequencies and to get narrow capacitance variations with the temperatures, Renesas recommends using dielectric X5R or better. See Table 2 for recommended output capacitor values. Bulk output capacitors that have adequately low ESR, such as low ESR polymer capacitors or a low ESR tantalum capacitor, can also be used in combination with the ceramic capacitors, depending on the output voltage ripple and transient requirements.

# 7. Layout Guidelines

Careful attention to layout requirements is necessary for successful implementation of the RAA210030 power module. The RAA210030 operates at high switching frequencies. Therefore, an optimized layout can minimize the impacts of high di/dt and dv/dt. Conversely, a poor layout can lead to poor regulation (both line and load), degraded efficiency, increased EMI radiation, noise sensitivity, and thermal stress.

## 7.1 Layout Considerations

The following are the layout considerations.

- Place the input ceramic capacitors as close as possible to the module input. These ceramic capacitors minimize the high frequency noise by reducing the parasitic inductance of the power loop. Proper placement of these capacitors not only leads to less PHASE node spikes and ringing, but also minimizes the switching noise coupled to the module. Renesas recommends using dielectric X5R or better with a minimum total capacitance of 22µF at the module input. A layout example is shown in Figure 37 and Figure 38.
- Use large copper planes to minimize conduction loss and thermal stress for VIN, VOUT, and PGND. Use multiple vias to connect the power planes in different layers.
- Use a separate SGND plane for components that are connected to SGND. Connect SGND and PGND at a single point on the top layer as shown in Figure 39.
- Use a remote-sensing trace to connect to the point-of-load and achieve tight output voltage regulation. Route the remote-sensing trace underneath the PGND layer and avoid routing it near noisy planes. Place a 2Ω resistor close to the output voltage resistor divider and FB pin to damp the noise on the trace.

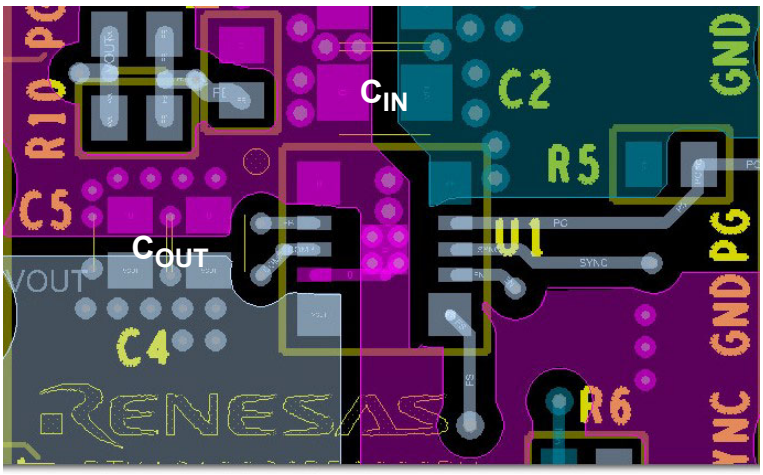



**Figure 37. Layout Example - Top Layer**

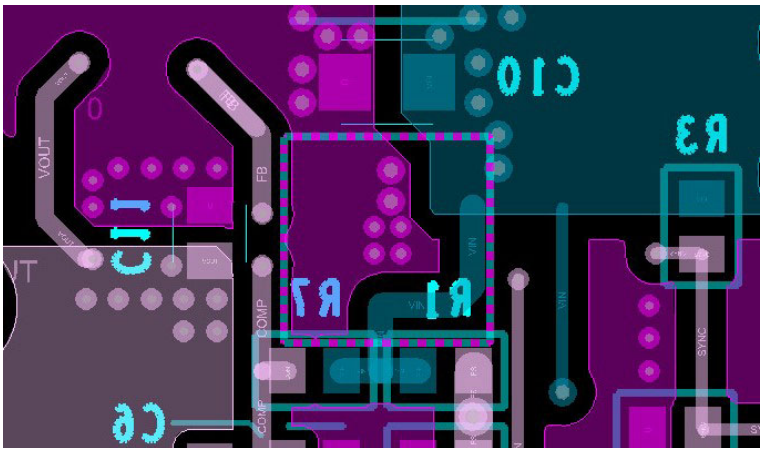



**Figure 38. Layout Example - Bottom Layer**

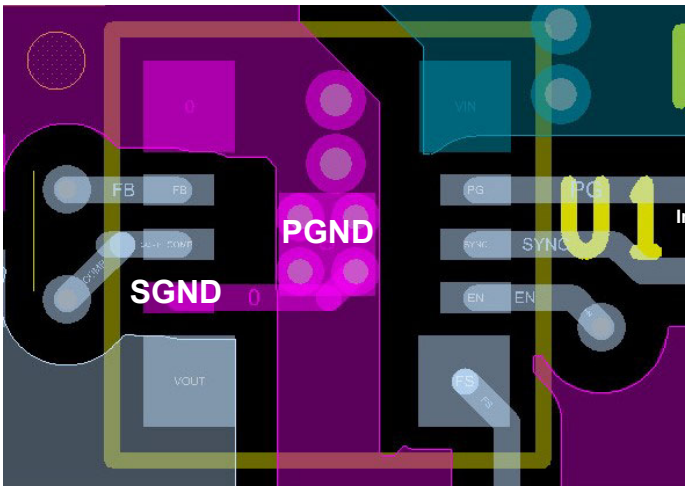



**Figure 39. Layout Example - SGND is Connected to PGND at Single Point**

## 7.2 Thermal Considerations

Experimental power loss curves, along with $\theta_{JA}$ from thermal modeling analysis, can evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +120°C. In applications in which the system parameters and layout are different from the evaluation board, the customer can adjust the margin of safety. All derating curves are obtained from tests on a 4-layer thermal test board 4.5x3 inches in size with 2oz copper on both top and bottom layers and 1oz copper on internal layers. See TB379 for more details. In the actual application, other heat sources and design margins should be considered.

# 8. Package Description

The RAA210030 is integrated into a 10 Lead Dual Flat Embedded Laminate Package with exposed copper thermal pads. This package has such advantages as good thermal and electrical conductivity, low weight, and small size. The package is applicable for surface mounting technology and is becoming more common in the industry. The embedded laminate substrate and inductor are overmolded with a polymer mold compound to protect these devices.

The package outline, typical PCB layout pattern, and typical stencil pattern design are shown in the Package Outline Drawing. *R70TB0004EU: PCB Design and Assembly Recommendations for Renesas Power Modules* shows the typical reflow profile parameters. These guidelines are general design rules. You can modify parameters according to your specific application.

## 8.1 PCB Layout Pattern Design

The bottom of RAA210030 is an embedded laminate substrate, which is attached to the PCB by surface mounting. The PCB layout pattern is in the Y10.3x3A Package Outline Drawing. The PCB layout pattern is essentially 1:1 with the package exposed pad and the I/O termination dimensions, except that the PCB lands are slightly longer than the dual flat embedded laminate package terminations by about 0.3mm. This extension allows for solder filleting around the package periphery and ensures a more complete and inspectable solder joint. The thermal lands on the PCB layout should match 1:1 with the package exposed die pads.

## 8.2 Thermal Vias

Place a grid of 1.0mm to 1.2mm pitched thermal vias, which drops down and connects to buried copper planes under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter, with the barrel plated to about 2.0 ounce copper. Although adding more vias (by decreasing pitch) improves thermal performance, it also diminishes results as more vias are added. Use only as many vias as needed for the thermal land size and as your board design rules allow.

## 8.3 Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2 mil to 3 mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joins. The stencil aperture size to land size ratio should typically be 1:1. Reduce the aperture width slightly to help prevent solder bridging between adjacent I/O lands.

Renesas recommends using an array of smaller apertures instead of one large aperture to reduce the solder paste volume on larger thermal lands. The stencil printing area should cover 50% to 80% of the PCB layout pattern. Consider the symmetry of the whole stencil pattern when designing the pads.

Renesas recommends using a laser-cut, stainless-steel stencil with electropolished trapezoidal walls. Electropolishing smooths the aperture walls, resulting in reduced surface friction and better paste release, which reduces voids. Using a Trapezoidal Section Aperture (TSA) also promotes paste release and forms a brick-like paste deposit, which assists in firm component placement.

## 8.4 Reflow Parameters

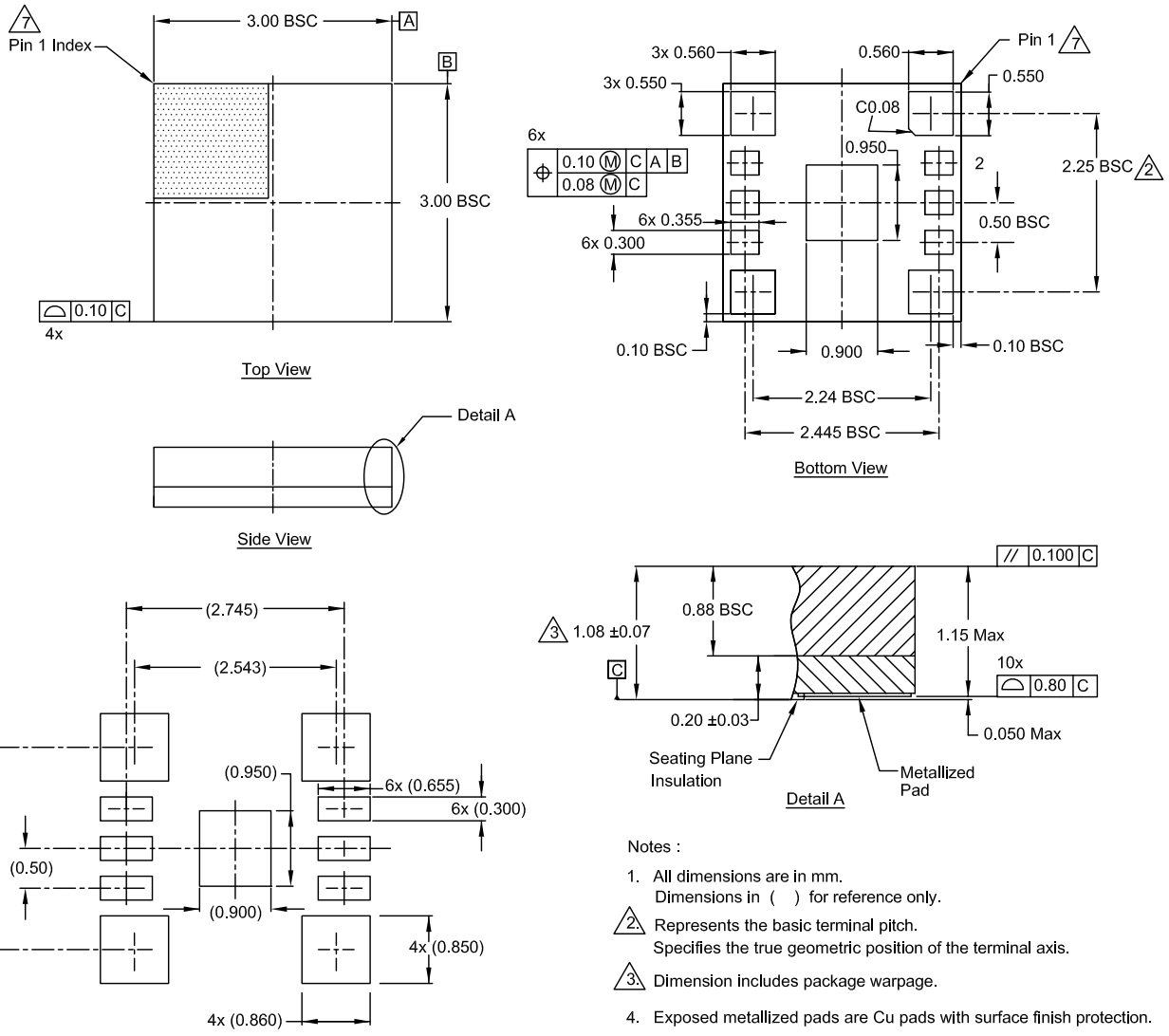
Renesas recommends using a No Clean Type 3 solder paste, per ANSI/J-STD-005 because of the low mount height of the package. Nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board; therefore, it is not practical to define a specific soldering profile just for the package. The profile given in R70TB0004EU is provided as a guideline to customize for varying manufacturing practices and applications.

# 9. Package Outline Drawing

For the most package drawing, see Y10.3X3A.

Y10.3x3A

10 Lead Dual Flat Embedded Laminate Package
Rev 1, 1/2022




Notes :

1. All dimensions are in mm.
   Dimensions in ( ) for reference only.
2. Represents the basic terminal pitch.
   Specifies the true geometric position of the terminal axis.
3. Dimension includes package warpage.
4. Exposed metallized pads are Cu pads with surface finish protection.
5. Package dimensions refer to JEDEC MO-208 rev.c.
6. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
   Unless otherwise specified, tolerance: Decimal ±0.05
7. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier is either a mold or mark feature.

# 10. Ordering Information

| Part Number[1][2] | Part Marking | Package Description[3] (RoHS Compliant) | Pkg. Dwg. # | Carrier Type[4] | Junction Temperature |
|---|---|---|---|---|---|
| RAA210030GLG#HD0 | 0030 | 10 Lead Dual Flat Embedded Laminate Package | Y10.3X3A | Reel, 3k | -40 to +125 |
| RTKA210030DR0000BU | Demonstration Board | | | | |

1. These Pb-free plastic packaged products are RoHS compliant by EU exemption 7C-I and 7A. They employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA210030 device page. For information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, refer to R70TB0004EU.
4. See TB347 for details about reel specifications.

# 11. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.01 | Jun 15, 2023 | Changed all references for TB493 to R70TB0004EU.<br>Updated the package description throughout document. |
| 1.00 | Jun 15, 2022 | Initial release. |

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