RAA210850

Pin-Configurable 50A DC/DC Power Module with PMBus Interface

FN9346
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The RAA210850 is a pin-strap configurable 50A step-down PMBus-compliant DC/DC power supply module that integrates a digital PWM controller, synchronous MOSFETs, power inductor, and passive components. Only input and output capacitors are needed to finish the design. Because of its thermally enhanced HDA packaging technology, the module can deliver up to 50A of continuous output current without the need for airflow or additional heat sinking. The RAA210850 simplifies configuration and control of Renesas digital power technology while offering an upgrade path to full PMBus configuration through the pin-compatible ISL8272M.

The RAA210850 operates with the ChargeMode™ control architecture, which responds to a transient load within a single switching cycle. The RAA210850 can be easily programmed with pin-strap resistors to set the output voltage, switching frequency, input UVLO, soft-start/stop, and device addresses. PMBus can be used to monitor voltages, currents, temperatures, and fault status. The RAA210850 is supported by PowerNavigator™ software, a Graphical User Interface (GUI), that can configure modules for desired solutions.

The RAA210850 is available in a low profile, compact, (18mmx23mmx7.5mm) fully encapsulated, thermally enhanced HDA package, suitable for automated assembly by standard surface mount equipment.

Related Literature

For a full list of related documents, visit our website:

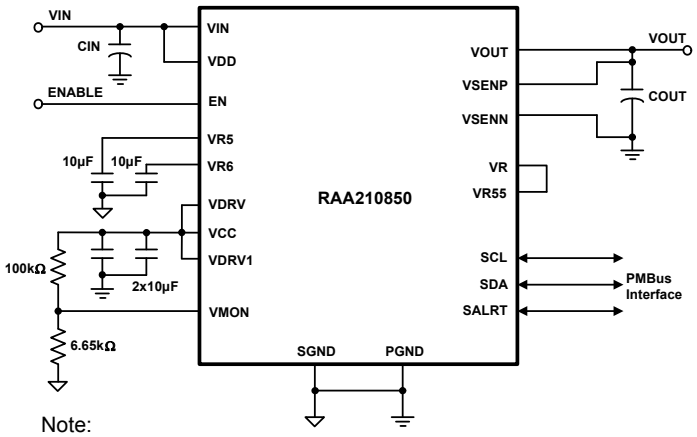
- RAA210850 product page

Features

- Wide input voltage range: 4.5V to 14V
- Up to 96% efficiency
- Programmable output voltage
  - 0.6V to 5V output voltage settings
  - ±1.2% V_{OUT} accuracy over line, load, and temperature
- PMBus compliant communication interface
- Pin-strap mode for standard settings
  - V_{OUT}, switching frequency, input UVLO, soft-start/stop, and external synchronization
- Real-time telemetry for V_{IN}, V_{OUT}, I_{OUT}, temperature, duty cycle, and switching frequency
- Complete overvoltage, undervoltage, current and temperature protections with fault logging
- PowerNavigator supported
- Thermally enhanced HDA package

Applications

- Server, telecom, storage, and datacom
- Industrial/ATE and networking equipment
- General purpose power for ASIC, FPGA, DSP, and memory



Note:

1. Figure 1 represents a typical implementation of the RAA210850. Renesas recommends tying the enable pin (EN) to SGND for

Figure 1. 50A Application Circuit

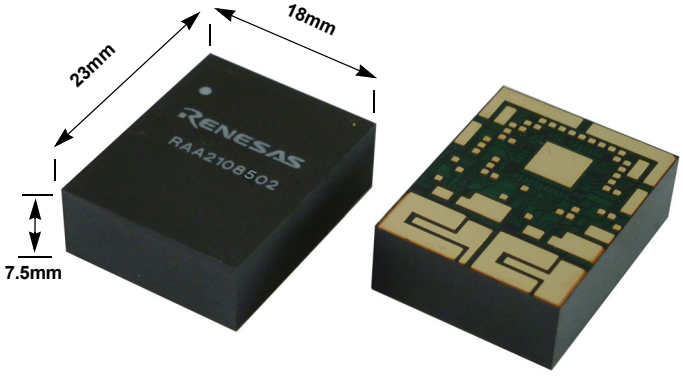


Figure 2. A Small Package for High Power Density

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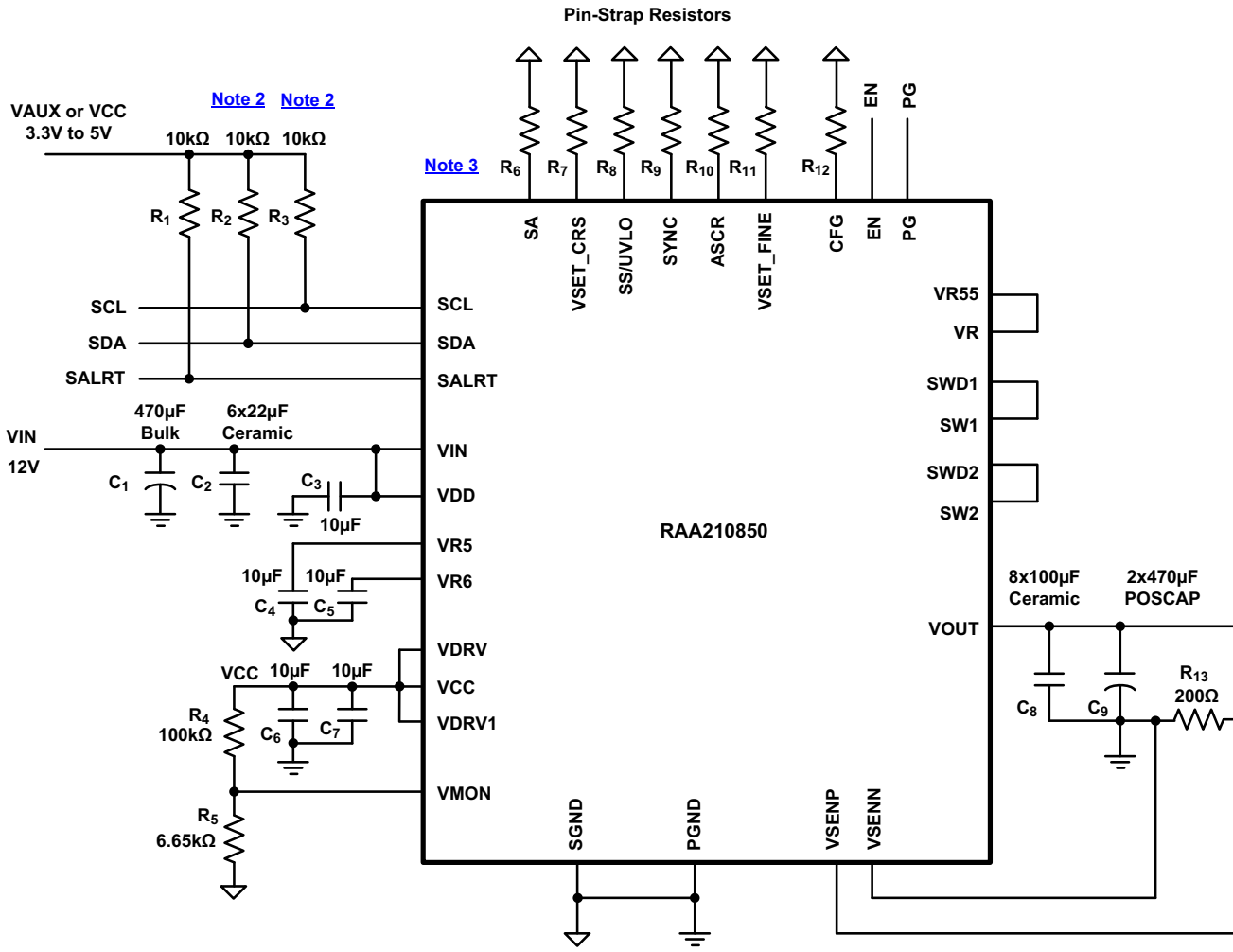
1. Overview

1.1 Typical Application Module



Notes:

2. R_2 and R_3 are not required if the PMBus host already has I^2C pull-up resistors.
3. R_6 through R_{11} can be selected according to the tables for the pin-strap resistor setting in this document.
4. V25, VR, and VR55 do not need external capacitors. V25 can be no connection.

Figure 3. Typical Application Circuit - Single Module

Table 1. RAA210850 Design Guide Matrix and Output Voltage Response

V_{IN} (V)	V_{OUT} (V)	C_{OUT} (Bulk) (µF)	C_{OUT} (Ceramic) (µF)	ASCR Residual (Note 6)	ASCR Gain (Note 6)	P-P Deviation (mV)	Recovery Time (µs)	Load Step (A) (Note 7)	Frequency (kHz)
12	0.7	5x470	12 x100	90	280	64.39	12.8	0 - 25	364
12	0.7	4x470	8 x100	90	600	61.25	10.23	0 – 25	615
5	0.7	5x470	12 x100	90	280	62.36	12.26	0 – 25	364
5	0.7	4x470	8 x100	90	500	61.32	7.47	0 – 25	640
12	0.8	5x470	10 x100	90	250	72.59	14.7	0 – 25	364
12	0.8	3x470	10 x100	100	450	70.76	9.83	0 – 25	615
5	0.8	5x470	10 x100	90	250	65.88	11.86	0 – 25	364
5	0.8	3x470	10 x100	90	450	65.29	8.66	0 – 25	615
12	0.9	4x470	12 x100	90	230	80	12.8	0 – 25	364
12	0.9	3x470	8 x100	90	320	81.85	10.58	0 – 25	615
5	0.9	4x470	12 x100	90	230	73.84	12.26	0 – 25	364
5	0.9	3x470	8 x100	90	320	78.73	9.06	0 – 25	615
12	1	3x470	10 x100	90	250	91.65	10.8	0 – 25	421
12	1	2x470	9 x100	100	320	92.06	11.38	0 – 25	615
5	1	3x470	10 x100	90	220	84.2	12.65	0 – 25	421
5	1	2x470	9 x100	100	320	85.83	11.46	0 – 25	727
12	1.2	2x470	11 x100	100	240	107.16	10.41	0 – 25	471
12	1.2	2x470	8 x100	90	320	103.49	8.22	0 – 25	727
5	1.2	2x470	11 x100	100	240	98.35	15	0 – 25	471
5	1.2	2x470	8 x100	90	320	99.77	8.62	0 – 25	727
12	1.5	2x470	6 x100	90	160	137.69	10.4	0 – 25	471
12	1.5	1x470	8 x100	100	240	131.45	9.71	0 – 25	727
5	1.5	2x470	6 x100	90	160	133.77	17	0 – 25	471
5	1.5	1x470	8 x100	100	240	140.51	12.61	0 – 25	727
12	1.8	1x470	12 x100	100	160	151.12	12.61	0 – 25	471
12	1.8	1x470	6 x100	100	200	159.72	9.46	0 – 25	727
5	1.8	1x470	12 x100	100	160	150.77	22.98	0 – 25	471
5	1.8	1x470	6 x100	100	200	159.62	17.39	0 – 25	727
12	2.5	1x470	9 x100	100	160	174.37	9.81	0 – 25	533
5	2.5	1x470	9 x100	100	160	168.41	29.37	0 – 25	533
12	3.3	1x470	7 x100	90	120	218.11	8.62	0 – 25	533
12	5	1x470	9 x100	90	120	224.44	5.03	0 – 2	571

Notes:

5. 1 x 470µF input bulk (EEE1EA471P) and 6x22µF input ceramic (CRM32ER71C226KE18L) capacitors are used to evaluate all test conditions above. The C_{IN} bulk capacitor is optional only for energy buffer from the long input power supply cable.
6. ASCR gain and residual are selected to ensure phase margin higher than 60° and gain margin higher than 8dB at room temperature.
7. Output voltage response is tested with 0 to 50% load step and slew rate at 15A/µs.

Table 2. Recommended Input/Output Capacitors

Vendors	Value	Part Number
Murata, Input Ceramic	47µF, 16V, 1210	GRM32ER61C476ME15L
Murata, Input Ceramic	22µF, 25V, 1210	GRM32ER61E226KE15L
Murata, Input Ceramic	22µF, 16V, 1210	GRM32ER71C226KE18L
Murata, Output Ceramic	100µF, 6.3V, 1206	GRM31CR60J107ME39L
TDK, Output Ceramic	100µF, 6.3V, 1206	C3216X5R0J107M160AB
Panasonic, Output Bulk	470µF, 4V, 2917	4TPE470MCL
Panasonic, Output Bulk	470µF, 6.3V, 2917	6TPF470MAH
Panasonic, Input Bulk	470µF, 25V	EEE1EA471P

1.2 Internal Block Diagram

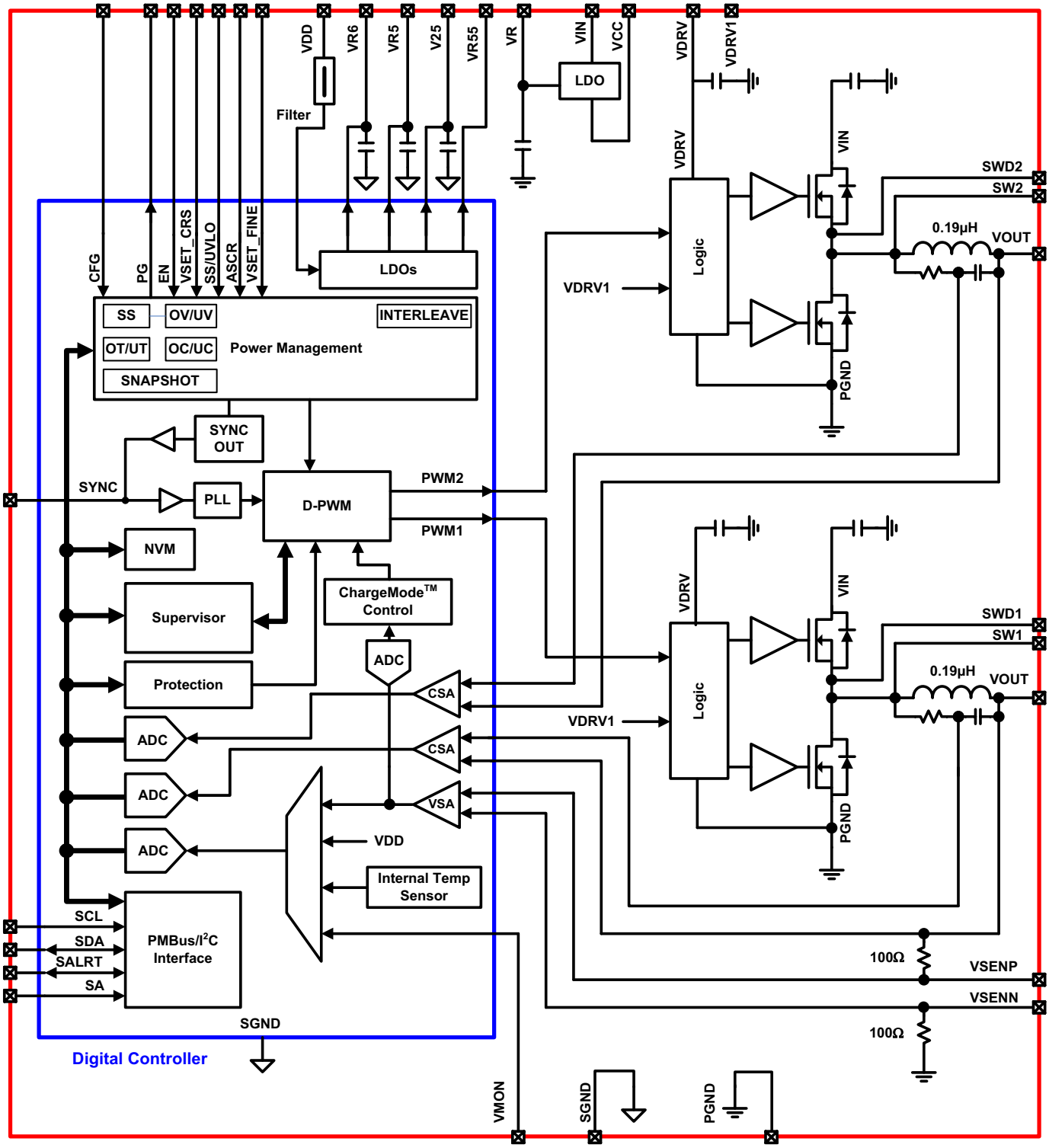


Figure 4. Internal Block Diagram

1.3 Ordering Information

Part Number (Notes 9, 10)	Part Marking	Temp Range (°c)	Tape and Reel (Units) (Note 8)	Package (RoHS Compliant)	Pkg. Dwg. #
RAA2108502GLG#AG0	RAA2108502	-40 to +85	-	58 Ld 18x23 HDA	Y58.18x23
RAA2108502GLG#HG0	RAA2108502	-40 to +85	100	58 Ld 18x23 HDA	Y58.18x23
RTKA2108502H00000BU	Single-Module Evaluation Board				

Notes:

8. Refer to TB347 for details about reel specifications.
9. These Pb-free plastic packaged products are RoHS compliant by EU exemption 7C-I and 7A. They employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
10. For Moisture Sensitivity Level (MSL), refer to the RAA210850 device. For more information about MSL, refer to TB363.

Table 3. Key Differences between Family of Parts

Part Number	Description	V_{IN} Range (V)	V_{OUT} Range (V)	I_{OUT} (A)
RAA210850	50A DC/DC single channel power module	4.5 - 14	0.6 - 5	50
RAA210833	33A DC/DC single channel power module	4.5 - 14	0.6 - 5	33
RAA210825	25A DC/DC single channel power module	4.5 - 14	0.6 - 5	25
RAA210870	70A DC/DC single channel power module	4.5 - 14	0.6 - 2.5	70
RAA210925	25A/25A DC/DC dual channel power module	4.5 - 14	0.6 - 5	25/25

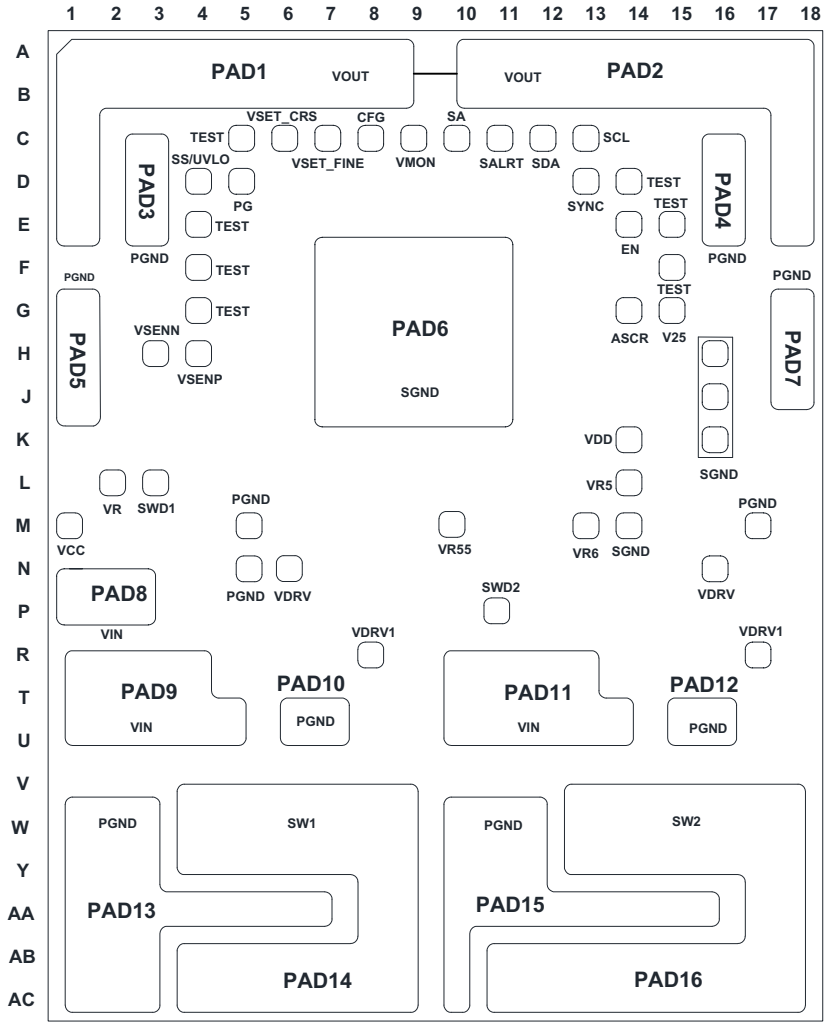
Table 4. Comparison of Simple Digital and Full Digital Parts

	ISL8272M	RAA210850
V_{IN} (V)	4.5 - 14	4.5 - 14
V_{OUT} (V)	0.6 - 5	0.6 - 5
I_{OUT} (Max) (A)	50	50
f_{SW} (kHz)	296 - 1067	296 - 1067
Digital PMBus Programmablility for Configuration of Modules	All PMBus commands. NVM access to store module configuration	Configuration of modules supported by pin-strap resistors. Digital programmability supports configuration changes during run-time operation with a subset of PMBus commands. No NVM access to store module configuration
Power Navigator Support	Yes	Yes
SYNC Capability	Yes	Yes
Current Sharing Multi-Modules	Yes	No
DDC Pin (Inter-Device Communication)	Yes	No

Note: For a full comparison of all the RAA210XXX and ISL827XM product offerings, please visit the simple-digital module family page.

1.4 Pin Configuration

58 Ld HDA
Top View



1.5 Pin Descriptions

Pin	Label	Type	Description
PAD1, 2	VOUT	PWR	Power supply output voltage. Output voltage from 0.6V to 5V. Tie these two pads together to achieve a single output. For higher output voltage, refer to the derating curves starting on page 17 to set the maximum output current from these pads.
PAD3, 4, 5, 7, 10, 12, 13, 15	PGND	PWR	Power ground. Refer to "Layout Guidelines" on page 29 for the PGND pad connections and I/O capacitor placement.
PAD6	SGND	PWR	Signal ground. Refer to "Layout Guidelines" on page 29 for the SGND pad connections.
PAD8, 9, 11	VIN	PWR	Input power supply voltage to power the module. The input voltage range is 4.5V to 14V.
PAD14, 16	SW1, SW2	PWR	Switching node pads. The SW pads dissipate heat and provide good thermal performance. Refer to "Layout Guidelines" on page 29 for the SW pad connections.
C6	VSET_CRS	I	Output voltage selection pin. Used to set the V_{OUT} set point. Use VSET_FINE for fine-tuning.
C7	VSET_FINE	I	Output voltage fine-tuning. Provides increased V_{OUT} resolution based on the programmed VSET_CRS value.

Pin	Label	Type	Description
C8	CFG	I	Clock source configuration pin. If the clock source is set to be internal, the internal frequency is set according to the SYNC pin resistor settings. If the clock source is set to external, the internal frequency is set according to the CFG pin resistor. Refer to "Switching Frequency and PLL" on page 22 for more information.
C9	VMON	I	Driver voltage monitoring. Use this pin to monitor VDRV through an external 16:1 resistor divider.
C10	SA	I	Serial address selection pin. Assigns a unique address for each individual device and enables certain management features.
C11	SALRT	O	Serial alert. Connect to an external host if desired. SALRT is asserted low upon a fault event and deasserted when the fault is cleared. A pull-up resistor is required.
C12	SDA	I/O	Serial data. Connect to an external host and/or to other Digital-DC™ devices. A pull-up resistor is required.
C13	SCL	I/O	Serial clock. Connect to an external host and/or to other Digital-DC devices. A pull-up resistor is required.
D4	SS/ UVLO	I	Soft-start/stop and undervoltage lockout selection pin. Sets the turn on/off delay and ramp time and the input UVLO threshold levels.
D5	PG	O	Power-good output. The power-good is configured as an open-drain output.
D13	SYNC	I/O	Clock synchronization input. Sets the frequency of the internal switch clock, or synchronizes to an external clock.
E14	EN	I	Enable pin. Logic high to enable the module output.
C5, D14, E4, E15, F4, F15, G4	TEST	-	Test pins. Do not connect these pins.
G14	ASCR	I	ChargeMode™ control ASCR parameters selection pin. Sets ASCR gain and residual values.
G15	V25	PWR	Internal 2.5V reference that powers internal circuitry. No external capacitor is required for this pin.
H3	VSENN	I	Differential output voltage sense feedback. Connect to the negative output regulation point.
H4	VSENP	I	Differential output voltage sense feedback. Connect to the positive output regulation point.
H16, J16, K16, M14	SGND	PWR	Signal grounds. Use multiple vias to connect the SGND pins to the internal SGND layer.
K14	VDD	PWR	Input supply voltage for the controller. Connect the VDD pad to the V_{IN} supply.
L2	VR	PWR	Internal LDO bias pin. Tie VR directly to VR55 with a short loop trace.
L3, P11	SWD1, SWD2	PWR	Switching node driving pins. Directly connect to the SW1 and SW2 pads with short loop wires.
L14	VR5	PWR	Internal 5V reference that powers internal circuitry. Place a 10µF decoupling capacitor for this pin.
M1	VCC	PWR	Internal LDO output. Connect VCC to VDRV for internal LDO driving.
M5, M17, N5	PGND	PWR	Power grounds. Use multiple vias to connect the PGND pins to the internal PGND layer.
M10	VR55	PWR	Internal 5.5V bias voltage for internal LDO use only. Tie VR55 directly to the VR pin.
M13	VR6	PWR	Internal 6V reference used to power internal circuitry. Place a 10µF decoupling capacitor for this pin.
N6, N16	VDRV	PWR	Power supply for internal FET drivers. Connect a 10µF bypass capacitor to each of these pins. These pins can be driven by the internal LDO through VCC pin or by the external power supply directly. Keep the driving voltage between 4.5V and 5.5V. For 5V input applications, use an external supply or connect this pin to VIN.
R8, R17	VDRV1	I	Bias pin of the internal FET drivers. Always tie to VDRV.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Input Supply Voltage, VIN Pin	-0.3	+17	V
Input Supply Voltage for Controller, VDD Pin	-0.3	+17	V
MOSFET Switch Node Voltage, SW1/2, SWD1/2	-0.3	+17	V
MOSFET Driver Supply Voltage, VDRV, VDRV1 Pin	-0.3	+6.0	V
Output Voltage, VOUT pin	-0.3	+6.0	V
Internal Reference Supply Voltage, VR6 Pin	-0.3	+6.6	V
Internal Reference Supply Voltage, VR, VR5, VR55 Pin	-0.3	+6.5	V
Internal Reference Supply Voltage, V25 Pin	-0.3	+3	V
Logic I/O Voltage for EN, CFG, PG, ASCR, VSET_FINE, SA, SCL, SDA, SALRT, SYNC, SS/UVLO, VMON, VSET_CRS	-0.3	+6.0	V
Analog Input Voltages			
VSENP	-0.3	+6.0	V
VSENN	-0.3	+0.3	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	2		kV
Machine Model (Tested per JESD22-A115C)	200		V
Charged Device Model (Tested per JS-002-2014)	750		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
58 Ld HDA Package (Notes 11, 12)	5.3	1.1

Notes:

11. θ_{JA} is measured in free air with the module mounted on an 8-layer evaluation board 4.7x4.8inch in size with 2oz Cu on all layers and multiple via interconnects as specified in the RTKA2108502H00000BU evaluation board user guide.
12. For θ_{JC}, the “case temp” location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature (Plastic Package)		+125	°C
Storage Temperature Range	-55	+150	°C
Pb-Free Reflow Profile	See Figure 29 on page 31		

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Input Supply Voltage Range, V_{IN}	4.5	14	V
Input Supply Voltage Range for Controller, V_{DD}	4.5	14	V
Output Voltage Range, V_{OUT}	0.6	5	V

Parameter	Minimum	Maximum	Unit
Output Current Range, $I_{OUT(DC)}$ (Note 15)	0	50	A
Operating Junction Temperature Range, T_J	-40	+125	°C

2.4 Electrical Specifications

V_{IN} = V_{DD}= 12V, f_{SW} = 533kHz, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

Parameter	Symbol	Test Conditions	Min (Note 13)	Typ	Max (Note 13)	Unit
Input And Supply Characteristics						
Input Supply Current for Controller	I_{DD}	V_{IN} = V_{DD} = 12V, V_{OUT} = 0V, module not enabled		40	**50**	mA
6V Internal Reference Supply Voltage	V_{R6}		**5.5**	6.1	**6.6**	V
5V Internal Reference Supply	V_{R5}	I_{VR5} <5mA	**4.5**	5.2	**5.5**	V
2.5V Internal Reference Supply	V_{25}		**2.25**	2.5	**2.75**	V
Internal LDO Output Voltage	Vcc			5.3		V
Internal LDO Output Current	I_{VCC}	V_{IN} = V_{DD} = 12V, V_{CC} connected to VDRV, module enabled	**50**			mA
Input Supply Voltage for Controller Read Back Resolution	$V_{DD\_READ\_RES}$			±20		mV
Input Supply Voltage for Controller Read Back Total Error (Note 16)	$V_{DD\_READ\_ERR}$	PMBus Read		±2		%FS
Output Characteristics						
Output Voltage Adjustment Range	V_{OUT_RANGE}	V_{IN} > V_{OUT} + 1.8V	**0.54**		**5.5**	V
Output Voltage Set-Point Range	V_{OUT_RES}	Configured using PMBus		±0.025		%
Output Voltage Set-Point Accuracy (Note 14, 16)	V_{OUT_ACCY}	Includes line, load, and temperature (-20°C ≤ T_A ≤ +85°C)	**-1.2**		**1.2**	%FS
Output Voltage Read Back Resolution	$V_{OUT\_READ\_RES}$			±0.15		%FS
Output Voltage Read Back Total Error (Note 16)	$V_{OUT\_READ\_ERR}$	PMBus read	**-2**		**2**	%FS
Output Current Read Back Resolution	$I_{OUT\_READ\_RES}$			0.2		A
Output Current Range (Note 15)	I_{OUT_RANGE}				**50**	A
Output Current Read back Total Error	$I_{OUT\_READ\_ERR}$	PMBus read at max load. V_{OUT} = 1.5V		±3		A
Soft-Start and Sequencing						
Delay Time From Enable to V_{OUT} Rise	t_{ON_DELAY}	Configured using pin-strap resistors or PMBus	**2**		**300**	ms
t_{ON_DELAY} Accuracy	$t_{ON\_DELAY\_ACCY}$			±2		ms
Output Voltage Ramp-Up Time	t_{ON_RISE}	Configured using pin-strap resistors or PMBus	**0.5**		**120**	ms
Output Voltage Ramp-Up Time Accuracy	$t_{ON\_RISE\_ACCY}$			±250		µs

V_{IN} = V_{DD}= 12V, f_{SW} = 533kHz, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 13)	Typ	Max (Note 13)	Unit
Delay Time From Disable to V_{OUT} Fall	t_{OFF_DELAY}	Configured using pin-strap resistors or PMBus	**2**		**300**	ms
t_{OFF_DELAY} Accuracy	$t_{OFF\_DELAY\_ACCY}$			±2		ms
Output Voltage Fall Time	t_{OFF_FALL}	Configured using pin-strap resistors or PMBus	**0.5**		**120**	ms
Output Voltage Fall Time Accuracy	$t_{ON\_FALL\_ACCY}$			±250		µs
Power-Good						
Power-Good Delay	V_{PG_DELAY}			3		ms
Temperature Sense						
Temperature Sense Range	T_{SENSE_RANGE}	Configurable using PMBus	**-50**		**150**	°C
Internal Temperature Sensor Accuracy	INT_TEMP_{ACCY}	Tested at +100°C	-5		5	°C
Fault Protection						
V_{DD} Undervoltage Threshold Range	$V_{DD\_UVLO\_RANGE}$	Measured internally	**4.18**		**16**	V
V_{DD} Undervoltage Threshold Accuracy (Note 16)	$V_{DD\_UVLO\_ACCY}$			±2		%FS
V_{DD} Undervoltage Response Time	$V_{DD\_UVLO\_DELAY}$			10		µs
V_{OUT} Overvoltage Threshold Range	$V_{OUT\_OV\_RANGE}$	Factory default		$1.15V_{OUT}$		V
		Configured using PMBus	**$1.05V_{OUT}$**		**V_{OUT_MAX}**	V
V_{OUT} Undervoltage Threshold Range	$V_{OUT\_UV\_RANGE}$	Factory default		$0.85V_{OUT}$		V
		Configured using PMBus	**0**		**$0.95V_{OUT}$**	V
V_{OUT} OV/UV Threshold Accuracy (Note 14)	V_{OUT_OV/UV_ACCY}		**-2**		**2**	%
V_{OUT} OV/UV Response Time	V_{OUT_OV/UV_DELAY}			10		µs
Output Current Limit Set-Point Accuracy (Note 16)	I_{LIMIT_ACCY}	Tested at I_{OUT}_OC_FAULT_LIMIT = 50A		±10		% FS
Output Current Fault Response Time (Note 17)	I_{LIMIT_DELAY}	Factory default		3		t_{SW}
Over-Temperature Protection Threshold (Controller Junction Temperature)	$T_{JUNCTION}$	Factory default		115		°C
		Configured using PMBus	**-40**		**125**	°C
Thermal Protection Hysteresis	$T_{JUNCTION\_HYS}$			15		°C

V_{IN} = V_{DD}= 12V, f_{SW} = 533kHz, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 13)	Typ	Max (Note 13)	Unit
Oscillator and Switching Characteristics						
Switching Frequency Range	f_{SW_RANGE}		**296**		**1067**	kHz
Switching Frequency Set-Point Accuracy	f_{SW_ACCY}		**-5**		**5**	%
Minimum Pulse Width Required from External SYNC Clock	EXT_SYNC_{PW}	Measured at 50% amplitude	**150**			ns
Drift Tolerance for External SYNC Clock	EXT_SYNC_{DRIFT}	External SYNC Clock equal to 500kHz is not supported	**-10**		**10**	%
Logic Input/Output Characteristics						
Bias Current at the Logic Input Pins	I_{LOGIC_BIAS}	EN, CFG, PG, SA, SCL, SDA, SALRT, SYNC, UVLO, V_{MON}, V_{SET_CRS}	**-100**		**100**	nA
Logic Input Low Threshold Voltage	$V_{LOGIC\_IN\_LOW}$				**0.8**	V
Logic Input High Threshold Voltage	$V_{LOGIC\_IN\_HIGH}$		**2.0**			V
Logic Output Low Threshold Voltage	$V_{LOGIC\_OUT\_LOW}$	2mA sinking			**0.5**	V
Logic Output High Threshold Voltage	$V_{LOGIC\_OUT\_HIGH}$	2mA sourcing	**2.25**			V
PMBus Interface Timing Characteristic						
PMBus Operating Frequency	f_{SMB}		**100**		**400**	kHz

Notes:

13. Compliance to datasheet limits is assured by one or more methods: Production test, characterization and/or design. Controller is independently tested before module assembly.
14. V_{OUT} measured at the termination of the VSENP and VSENN sense points.
15. The MAX load current is determined by the thermal "Derating Curves" on page 17.
16. "FS" stands for full scale of recommended maximum operation range.
17. "t_{SW}" stands for time period of operation switching frequency.

3. Typical Performance Curves

3.1 Efficiency Performance

Operating condition: T_A = +25°C, no air flow. C_{OUT} = 6x470µF POSCAP + 12X100µF Ceramic. Typical values used unless otherwise noted.

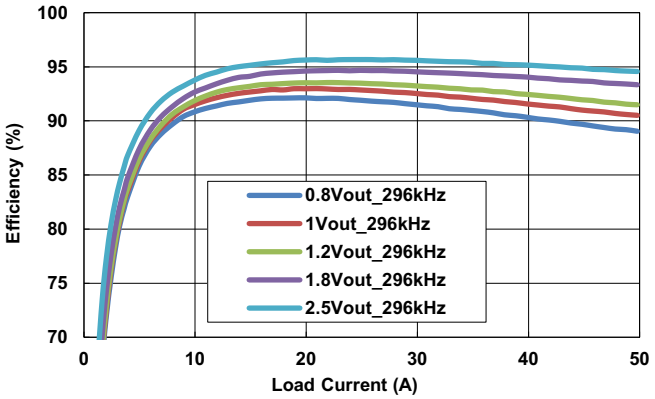


Figure 5. Efficiency vs Output Current at V_{IN} = 5V for Various Output Voltages

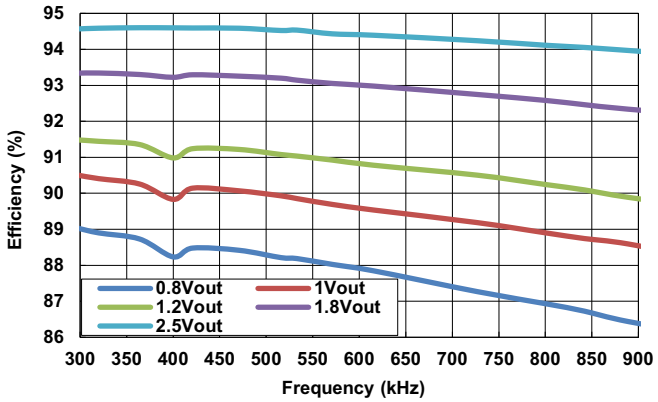


Figure 6. Efficiency vs Switching Frequency at V_{IN} = 5V, I_{OUT} = 50A for Various Output Voltages

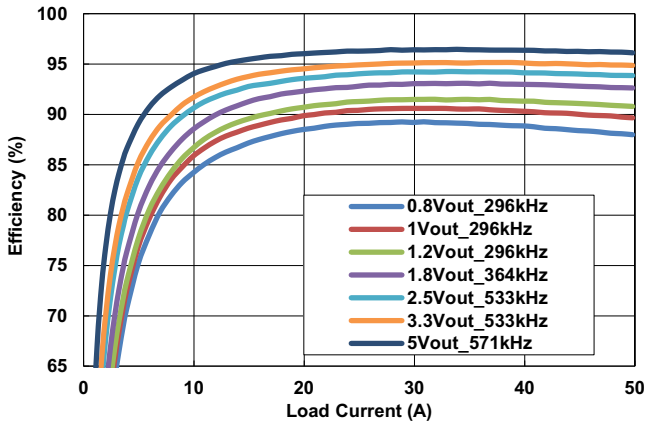


Figure 7. Efficiency vs Output Current at V_{IN} = 9V for Various Output Voltages

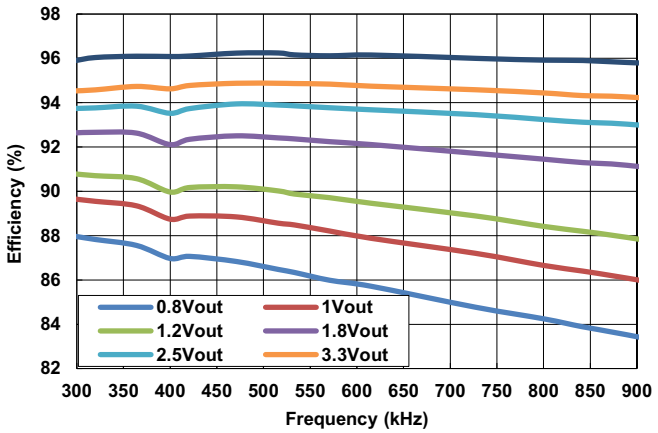


Figure 8. Efficiency vs Switching Frequency at V_{IN} = 9V, I_{OUT} = 50A for Various Output Voltages

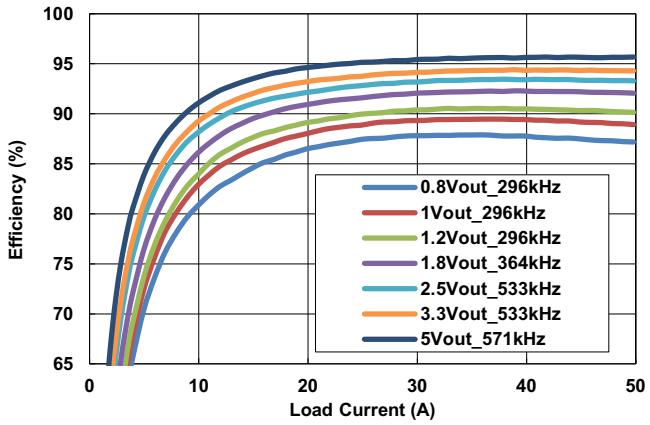


Figure 9. Efficiency vs Output Current at V_{IN} = 12V for Various Output Voltages

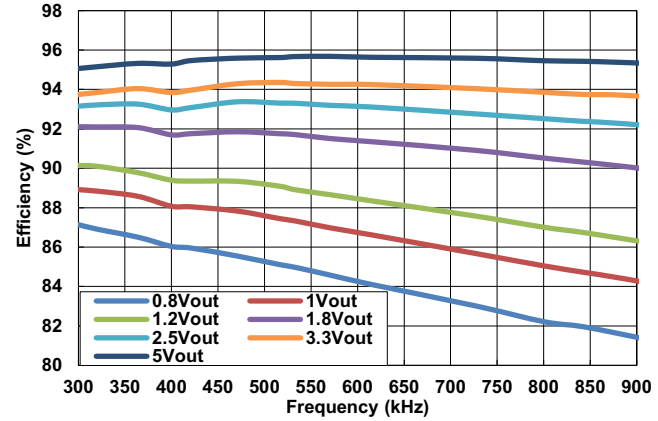


Figure 10. Efficiency vs Switching Frequency at V_{IN} = 12V, I_{OUT} = 50A for Various Output Voltages

3.2 Transient Response Performance

Operating conditions: V_{IN} = 12V, f_{SW} = 533kHz, I_{OUT} = 0A/25A, I_{OUT} slew rate = 15A/µs, T_A = +25°C, no air flow. Typical values are used unless otherwise noted.

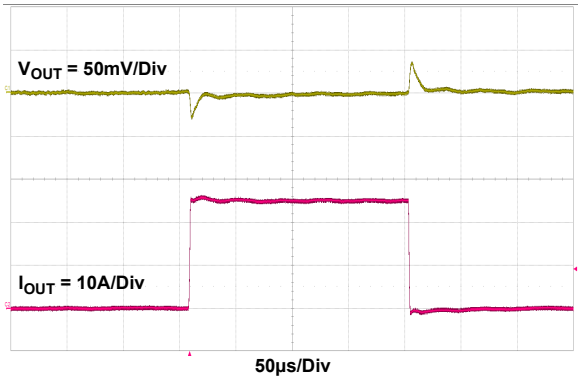


Figure 11. $5V_{IN}$ to $0.8V_{OUT}$ Transient Response, f_{SW} = 615kHz, C_{OUT} = 10x100µF Ceramic + 3x470µF POSCAP, ACSR Residual = 90, ASCR Gain = 450

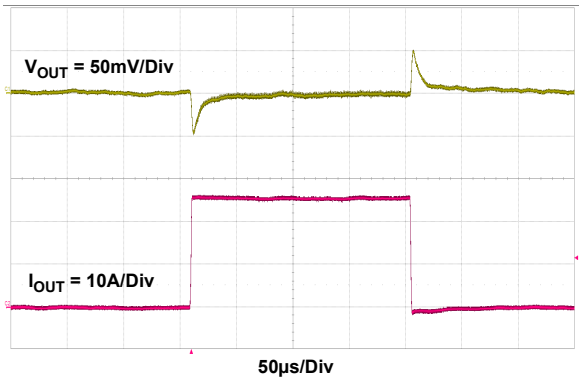


Figure 12. $5V_{IN}$ to $1.2V_{OUT}$ Transient Response, f_{SW} = 727kHz, C_{OUT} = 8x100µF Ceramic + 2x470µF POSCAP, ACSR Residual = 90, ASCR Gain = 320

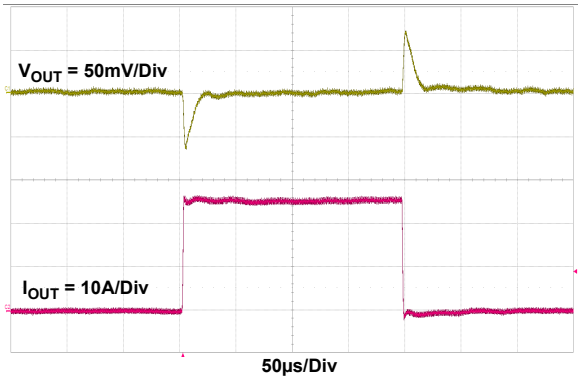


Figure 13. $12V_{IN}$ to $1.5V_{OUT}$ Transient Response, f_{SW} = 471kHz, C_{OUT} = 6x100µF Ceramic + 2x470µF POSCAP, ACSR Residual = 90, ASCR Gain = 160

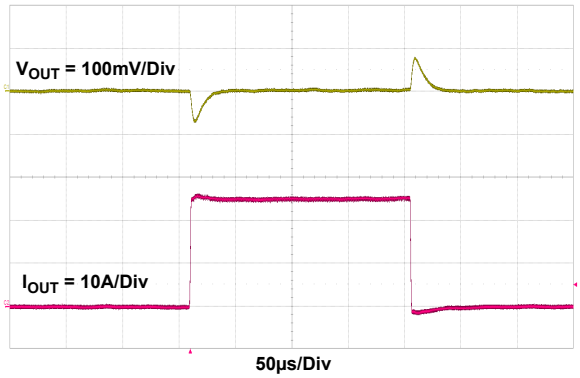


Figure 14. $12V_{IN}$ to $1.8V_{OUT}$ Transient Response, f_{SW} = 471kHz, C_{OUT} = 12x100µF Ceramic + 1x470µF POSCAP, ACSR Residual = 100, ASCR Gain = 160

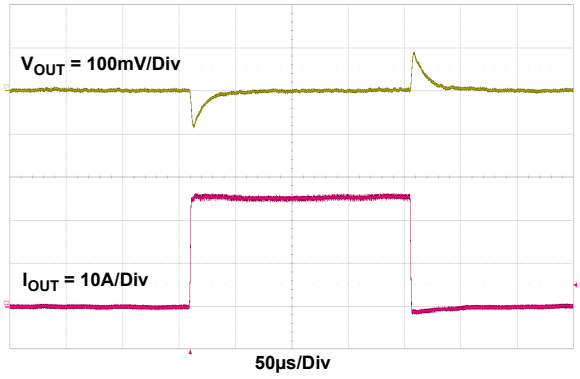


Figure 15. $12V_{IN}$ to $2.5V_{OUT}$ Transient Response, f_{SW} = 533kHz, C_{OUT} = 9x100µF Ceramic + 1x470µF POSCAP, ACSR Residual = 100, ASCR Gain = 160

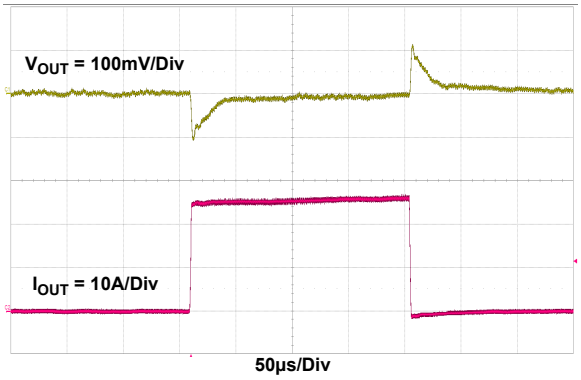


Figure 16. $12V_{IN}$ to $5V_{OUT}$ Transient Response, f_{SW} = 571kHz, C_{OUT} = 9x100µF Ceramic + 1x470µF POSCAP, ACSR Residual = 90, ASCR Gain = 120

3.3 Derating Curves

All of the following curves were plotted at T_J = +120°C.

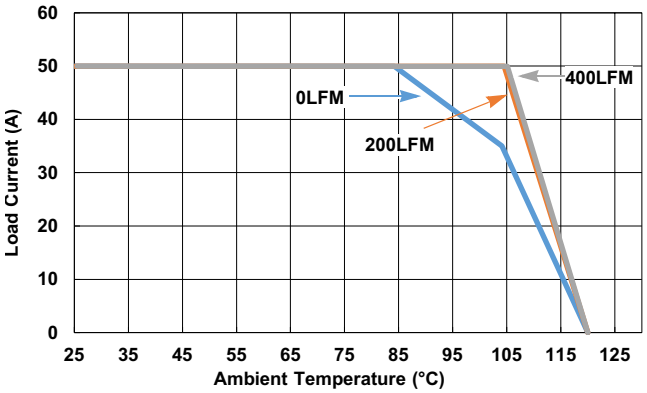


Figure 17. $12V_{IN}$ to $1V_{OUT}$, f_{SW} = 364kHz

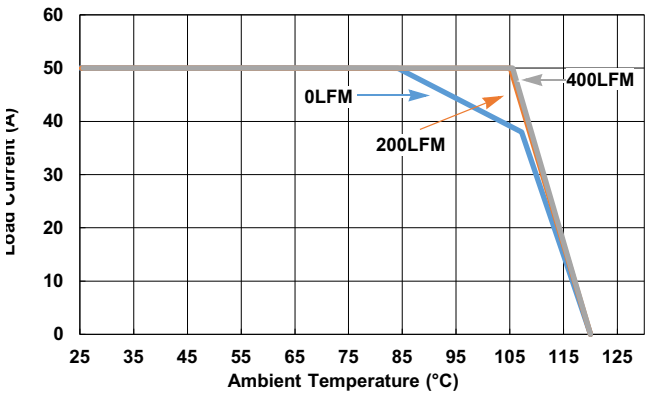


Figure 18. $5V_{IN}$ to $1V_{OUT}$, f_{SW} = 364kHz

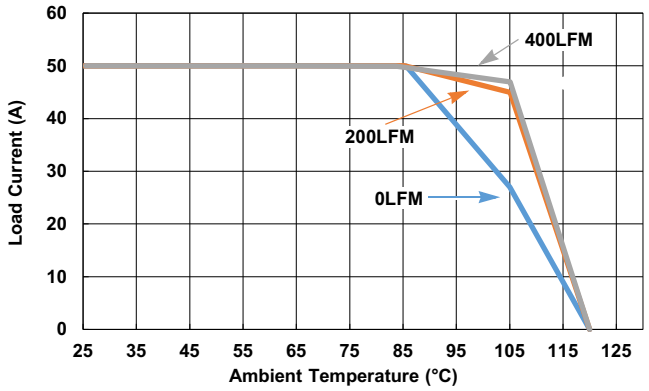


Figure 19. $12V_{IN}$ to $1.5V_{OUT}$, f_{SW} = 471kHz

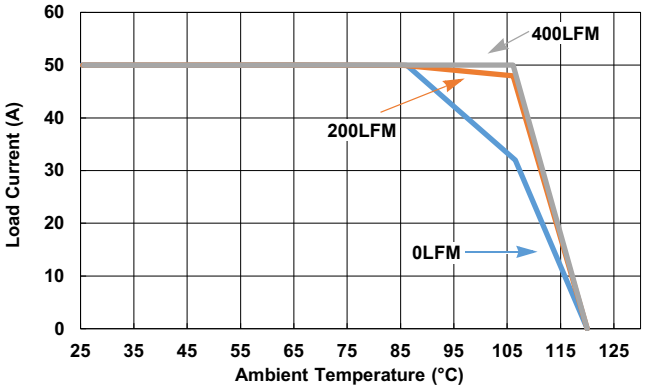


Figure 20. $5V_{IN}$ to $1.5V_{OUT}$, f_{SW} = 471kHz

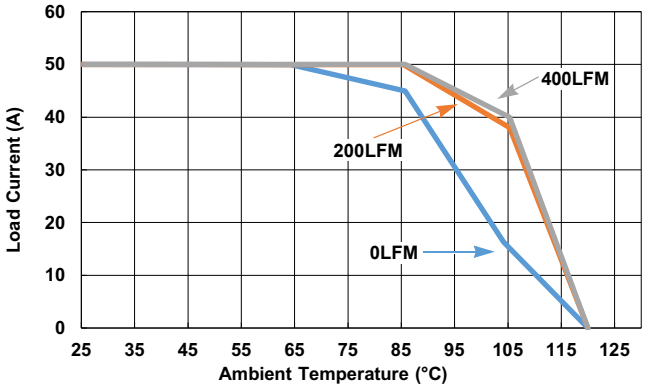


Figure 21. $12V_{IN}$ to $1.8V_{OUT}$, f_{SW} = 727kHz

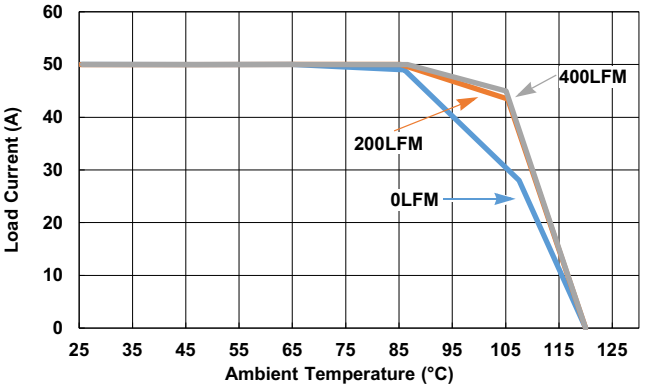


Figure 22. $5V_{IN}$ to $1.8V_{OUT}$, f_{SW} = 727kHz

All of the following curves were plotted at T_J = +120°C. **(Continued)**

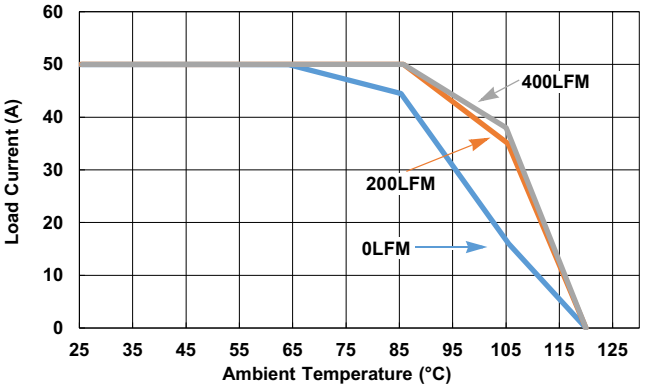


Figure 23. $12V_{IN}$ to $2.5V_{OUT}$, f_{SW} = 533kHz

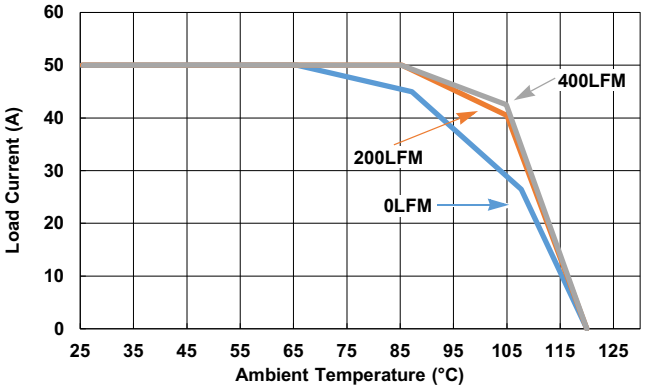


Figure 24. $5V_{IN}$ to $2.5V_{OUT}$, f_{SW} = 533kHz

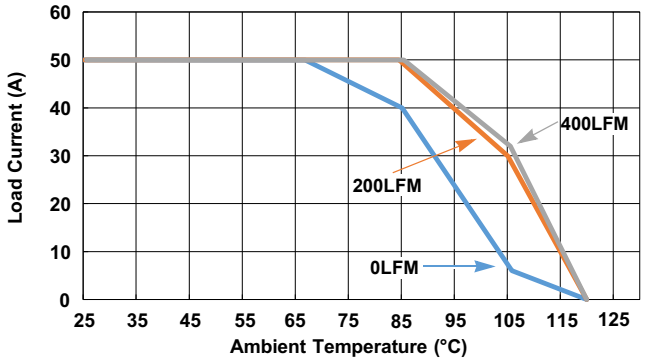


Figure 25. $12V_{IN}$ to $3.3V_{OUT}$, f_{SW} = 533kHz

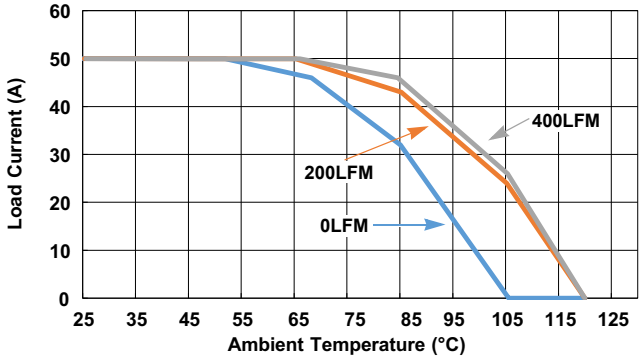


Figure 26. $12V_{IN}$ to $5V_{OUT}$, f_{SW} = 571kHz

4. Functional Description

4.1 SMBus Communications

The RAA210850 provides a SMBus digital interface that enables configuration of the module and monitors the input and output parameters. The RAA210850 can be used with any SMBus host device. The module is compatible with PMBus Power System Management Protocol Specification Parts I and II version 1.2. The RAA210850 accepts most standard PMBus commands. Renesas recommends tying the enable pin to SGND when PMBus commands are issued.

The SMBus device address is the only parameter that must be set by external pins.

4.2 Output Voltage Selection

The output voltage can be set to a voltage between 0.6V and 5V if the input voltage is higher than the desired output voltage by an amount sufficient to maintain regulation.

The VSET_CRS (VOUT Coarse) and VSET_FINE (VOUT Fine) pins set the output voltage. A resistor placed between the VSET_CRS pin and SGND programs the VOUT_CRS (VOUT Coarse) voltage according to the levels shown in Table 5. A standard 1% resistor is required.

Table 5. Output Voltage (Coarse) Resistor Settings

VOUT_CRS (V)	R_{SET} (kΩ)
0.600	10
0.675	11
0.700	12.1
0.720	13.3
0.750	14.7
0.800	16.2
0.850	17.8
0.900	19.6
0.930	21.5
0.950	23.7
0.980	26.1
1.000	Connect to SGND
1.030	28.7
1.050	31.6
1.100	34.8
1.120	38.3
1.150	42.2
1.200	OPEN
1.250	46.4
1.300	51.1
1.350	56.2
1.400	61.9
1.500	68.1
1.650	75
1.800	82.5
1.850	90.9

Table 5. Output Voltage (Coarse) Resistor Settings

VOUT_CRS (V)	R_{SET} (kΩ)
2.000	100
2.400	110
2.500	Connect to V25
2.800	121
3.000	133
3.300	147
3.600	162
5.000	178

If higher resolution is desired, the VSET_FINE pin can be used to fine-tune the output voltage settings according to the command set below:

$$\text{Output voltage} = \begin{cases} \text{VOUT\_CRS} + 5\text{mV} \bullet \text{N}, & \text{if } 0.6\text{V} \le \text{VOUT\_CRS} \le 1.4\text{V} \\ \text{VOUT\_CRS} + 10\text{mV} \bullet \text{N}, & \text{if } 1.5\text{V} \le \text{VOUT\_CRS} \le 1.85\text{V} \\ \text{VOUT\_CRS} + 50\text{ mV} \bullet \text{N}, & \text{if } 2\text{V} \le \text{VOUT\_CRS} \le 3.3\text{V} \\ \text{VOUT\_CRS} + 100\text{ mV} \bullet \text{N}, & \text{if } 3.6\text{V} \le \text{VOUT\_CRS} < 5\text{V} \\ \text{VOUT\_CRS}, & \text{if VOUT\_CRS} = 5\text{V} \end{cases}$$

Use the resistors values from Table 6 to set the appropriate value of N for calculating the final output voltage.

Table 6. VSET_FINE Resistor Settings

N	R_{SET} (kΩ)
0	10, or OPEN
1	11
2	12.1
3	13.3
4	14.7
5	16.2
6	17.8
7	19.6
8	21.5
9	23.7, or connect to SGND
10	26.1
11	28.7
12	31.6
13	34.8
14	38.3
15	42.2
16	46.4
17	51.1
18	56.2
19	61.9
20	68.1, or connect to V25

The output voltage can be set to any value between 0.6V and 5V using the pin-strap settings provided in Tables 5 and 6.

By default, V_{OUT_MAX} is set 110% higher than V_{OUT} set by the pin-strap resistor, which can be changed to any value up to 5.5V with the PMBus command VOUT_MAX.

4.3 Soft-Start/Stop Delay and Ramp Times

The RAA210850 follows an internal start-up procedure after power is applied to the VDD pin. The module requires approximately 60ms to 70ms to check for specific values stored in its internal memory and is programmed by pin-strap resistors. When this process is complete, the device is ready to accept commands from the PMBus interface and the module is ready to be enabled. If the module is synchronizing to an external clock source, the clock frequency must be stable before asserting the EN pin.

It may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period expires. These features can be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The RAA210850 has several options for precisely and independently controlling both the delay and ramp time periods. The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires.

The soft-start delay and ramp up time can be programmed to custom values with the PMBus commands TON_DELAY and TON_RISE. When the delay time is set to 0ms, the device begins its ramp-up after the internal circuitry has initialized (approximately 2ms). When the soft-start ramp period is set to 0ms, the output ramps up as quickly as the output load capacitance and loop settings allow. In general, set the soft-start ramp to a value greater than 1ms to prevent inadvertent fault conditions due to excessive in-rush current.

Similar to the soft-start delay and ramp up time, the delay and ramp down time for soft-stop/off can be programmed with the PMBus commands TOFF_DELAY and TOFF_FALL. In addition, the module can be configured as “immediate off” with the command ON_OFF_CONFIG, so that the FETs are turned off immediately after the delay time expires.

The SS/UVLO pin can program the soft start/stop delay time and ramp time to some typical values as shown in Table 7. A standard 1% resistor is required.

Table 7. UVLO and Soft-Start/Stop Resistor Settings

Resistor (kΩ)	UVLO (V)	Delay Time (ms)	Ramp Time (ms)
10	4.5	5	2
11	4.5	5	2
12.1	4.5	5	2
13.3	4.5	5	2
14.7	4.5	5	2
16.2	4.5	5	2
17.8	4.5	5	2
19.6	4.5	5	2
21.5	4.5	10	2
23.7	4.5	5	5
26.1	4.5	10	5
28.7	4.5	20	5
31.6	4.5	5	10
34.8	4.5	10	10
38.3	4.5	20	10
42.2	10.8	5	2

Table 7. UVLO and Soft-Start/Stop Resistor Settings (Continued)

Resistor (kΩ)	UVLO (V)	Delay Time (ms)	Ramp Time (ms)
46.4	10.8	10	2
51.1	10.8	5	5
56.2	10.8	10	5
61.9	10.8	20	5
68.1	10.8	5	10
75	10.8	10	10
82.5	10.8	20	10
Connect to SGND	4.5	5	2
OPEN	4.2	5	5
Connect to V25	4.5	10	10

4.4 Input Undervoltage Lockout (UVLO)

The input undervoltage lockout (UVLO) prevents the RAA210850 from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The UVLO threshold (V_{UVLO}) can be set between 4.18V and 16V by using the PMBus command VIN_UV_FAULT_LIMIT. Use the pin-strap method (SS/UVLO pin) shown in Table 7 to set the V_{UVLO} to three typical values. A standard 1% resistor is required.

The module shuts down immediately when it falls below the UVLO threshold. The fault must be cleared before the module can restart.

4.5 Power-Good

The RAA210850 provides a Power-Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin asserts if the output is within 10% of the target voltage. This limit can be changed using the PMBus command POWER_GOOD_ON.

A PG delay period is defined as the time from when all conditions within the RAA210850 for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. A fixed PG delay of 3ms is programmed for the RAA210850.

4.6 Switching Frequency and PLL

The device's switching frequency is configurable between 296kHz to 1067kHz using the pin-strap method shown in Table 8, or by using the PMBus command FREQUENCY_SWITCH.

Table 8. Switching Frequency Resistor Settings

f_{SW} (kHz)	R_{SET} (kΩ)
296	14.7, or connect to SGND
300	16.2
320	17.8
364	19.6
400	21.5
421	23.7, or OPEN
471	26.1
533	28.7
571	31.6
615	34.8, or connect to V25

Table 8. Switching Frequency Resistor Settings (Continued)

f_{SW} (kHz)	R_{SET} (kΩ)
727	38.3
800	42.2
842	46.4
889	51.1
1067	56.2

The RAA210850 incorporates an internal Phase-Locked Loop (PLL) to clock the internal circuitry. The PLL can also be driven by an external clock source connected to the SYNC pin. Set this configuration by connecting a resistor to the CFG pin. If the clock source is internal, the internal frequency is set according to the SYNC pin resistor settings shown in Table 8. If clock source is external, the internal frequency is set according to the resistor connected to the CFG pin as shown in Table 9. The external clock frequency should be within ±10% of the listed options.

Table 9. External Frequency Sync Settings

Clock Source	Internal FREQUENCY_SWITCH (kHz)	R_{SET} (kΩ)
Internal	Determined by SYNC resistor	10, or OPEN
External	296	11
External	340	12.1
External	390	13.3
External	444	14.7
External	516	16.2, or connect to SGND
External	593	17.8
External	696	19.6
External	800	21.5
External	941	23.7
External	1067	26.1, or connect to V25

The incoming clock signal must be stable when the enable pin is asserted. The external clock signal must not vary more than 10% from its initial value and should have a minimum pulse width of 150ns. A standard 1% resistor is required.

4.7 Loop Compensation

The module loop response is programmable using the pin-strap method or by using the PMBus command ASCR_CONFIG according to Table 10. A standard 1% resistor is required. The RAA210850 uses the ChargeMode control algorithm that responds to output current changes within a single PWM switching cycle, achieving a smaller total output voltage variation with less output capacitance than traditional PWM controllers.

Table 10. ASCR Resistor Settings

ASCR Gain	ASCR Residual	R_{SET} (kΩ)
80	90	10
100	90	11
110	90	12.1
120	90	Connect to SGND
160	90	13.3

Table 10. ASCR Resistor Settings (Continued)

ASCR Gain	ASCR Residual	R_{SET} (kΩ)
200	90	OPEN
220	90	14.7
230	90	16.2
250	90	17.8
280	90	19.6
320	90	21.5
360	90	23.7
400	90	26.1
450	90	28.7
500	90	31.6
550	90	34.8
600	90	38.3
700	90	42.2
800	90	46.4
80	100	51.1
120	100	56.2
160	100	61.9
200	100	68.1
240	100	75
280	100	82.5
320	100	90.9
360	100	100
400	100	110
450	100	121
500	100	Connect to V25
550	100	133
600	100	147
700	100	162
800	100	178

4.8 SMBus Module Address Selection

Each module must have its own unique serial address to distinguish between other devices on the bus. The module address is set by connecting a resistor between the SA pin and SGND. Table 11 lists the available module addresses. A standard 1% resistor is required.

Table 11. SMBus Address Resistor Selection

R_{SA} (kΩ)	SMBus Address
10	19h
11	1Ah
12.1	1Bh
13.3	1Ch

Table 11. SMBus Address Resistor Selection (Continued)

R_{SA} (kΩ)	SMBus Address
14.7	1Dh
16.2	1Eh
17.8	1Fh
19.6	20h
21.5	21h
23.7	22h
26.1	23h
28.7	24h
31.6	25h
34.8, or connect to SGND	26h
38.3	27h
42.2, or Open	28h
46.4	29h
51.1	2Ah
56.2	2Bh
61.9	2Ch
68.1	2Dh
75	2Eh
82.5	2Fh
90.9	30h
100	31h
110	32h
121	33h
133	34h
147	35h
162	36h
178	37h

4.9 Output Overvoltage Protection

The RAA210850 has an internal output overvoltage protection circuit that can protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator compares the actual output voltage (seen at the VSENP and VSENN pins) to a threshold set to 15% higher than the target output voltage. The fault threshold can be programmed to a desired level with the PMBus command VOUT_OV_FAULT_LIMIT. If the VSENP - VSENN voltage exceeds this threshold, the module initiates an immediate shutdown without retry.

Internal to the module, two 100Ω resistors are populated from V_{OUT} to VSENP and SGND to VSENN to protect from overvoltage conditions in case of open at voltage sensing pins and differential remote sense traces due to assembly error. If the differential remote sense traces have low resistance, V_{OUT} regulation accuracy is not sacrificed.

4.10 Output Prebias Protection

An output prebias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start-up if a prebias condition exists at the output. The RAA210850 provides prebias protection by sampling the output voltage before initiating an output ramp.

If a prebias voltage lower than the target voltage exists after the preconfigured delay period has expired, the target voltage is set to match the existing prebias voltage and both drivers are enabled. The output voltage is then ramped to the final regulation value at the preconfigured ramp rate.

The actual time the output takes to ramp from the prebias voltage to the target voltage varies depending on the prebias voltage; however, the total time elapsed from when the delay period expires to when the output reaches its target value matches the preconfigured ramp time (see Figure 27).

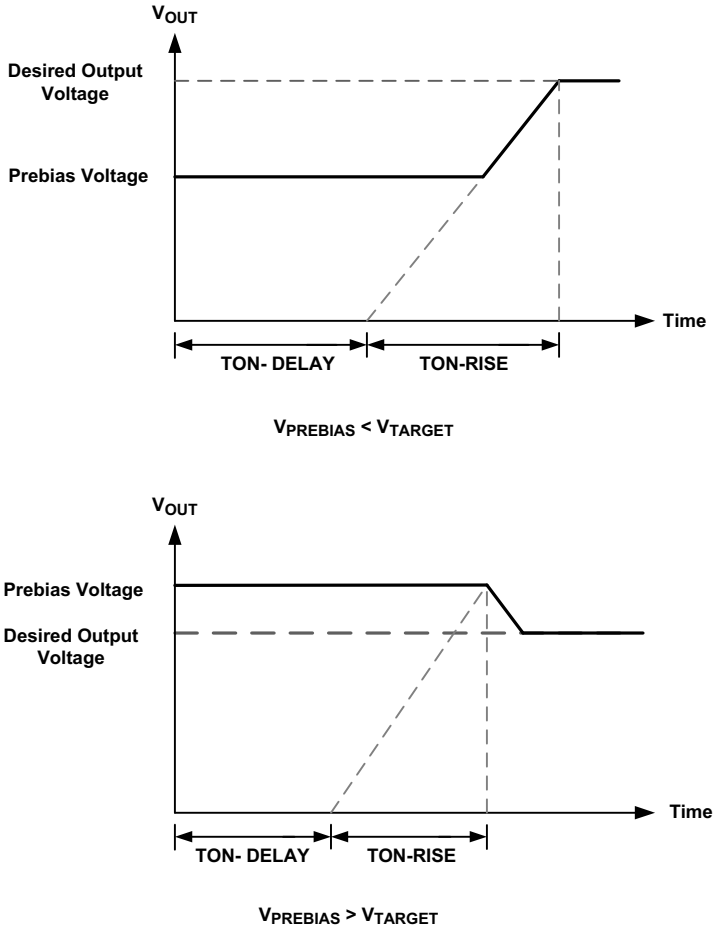


Figure 27. Output Responses to Prebias Voltages

If a prebias voltage is higher than the target voltage after the preconfigured delay period has expired, the target voltage is set to match the existing prebias voltage and both drivers are enabled with a PWM duty cycle that ideally creates the prebias voltage.

When the preconfigured soft-start ramp period expires, the PG pin is asserted (assuming the prebias voltage is not higher than the overvoltage limit). The PWM then adjusts its duty cycle to match the original target voltage and the output ramps down to the preconfigured output voltage.

If a prebias voltage is higher than the overvoltage limit, the device does not initiate a turn-on sequence and declares an overvoltage fault condition.

4.11 Output Overcurrent Protection

The RAA210850 can protect the power supply from damage if the output is shorted to ground or if an overload condition is imposed on the output. Average output overcurrent fault threshold can be programmed with the PMBus command IOUT_OC_FAULT_LIMIT. The module automatically programs the peak inductor current fault threshold by calculating the inductor ripple current from the input voltage, switching frequency, and the VOUT_COMMAND.

The response from an overcurrent fault is an immediate shutdown with 70ms retry.

4.12 Thermal Overload Protection

The RAA210850 includes a thermal sensor that continuously measures the internal temperature of the module and shuts down the controller when the temperature exceeds the preset limit. The default temperature limit is set to +115°C in the factory, but can be changed with PMBus command OT_FAULT_LIMIT.

The response from an over-temperature fault is an immediate shutdown without retry.

4.13 Phase Spreading

When multiple point-of-load converters share a common DC input supply, adjust the clock phase offset of each device so that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Because the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced and the power losses proportional to the I_{RMS}^2 are reduced dramatically.

To enable phase spreading, all converters must be synchronized to the same switching clock.

The phase offset between devices will be determined from the lower 4 bits of the SMBus address of each interleaved device. The phase offset of each device can be set to any value between 0˚ and 360˚ in 22.5˚ increments. The internal two phase of the module always maintain a phase difference of 180˚.

This functionality can also be accessed using the PMBus command INTERLEAVE.

Table 12. Interleave

SMBus Address	SMBus Address in Binary	Low 4-Bits	INTERLEAVE	Phase Shift in ˚	Rail ID
19h	00011001	1001	9	202.5	25
1Ah	00011010	1010	10	225	26
1Bh	00011011	1011	11	247.5	27
1Ch	00011100	1100	12	270	28
1Dh	00011101	1101	13	292.5	29
1Eh	00011110	1110	14	315	30
1Fh	00011111	1111	15	337.5	31
20h	00100000	0000	0	0	0
21h	00100001	0001	1	22.5	1
22h	00100010	0010	2	45	2
23h	00100011	0011	3	67.5	3
24h	00100100	0100	4	90	4
25h	00100101	0101	5	112.5	5
26h	00100110	0110	6	135	6
27h	00100111	0111	7	157.5	7
28h	00101000	1000	8	180	8
29h	00101001	1001	9	202.5	9

Table 12. Interleave (Continued)

SMBus Address	SMBus Address in Binary	Low 4-Bits	INTERLEAVE	Phase Shift in °	Rail ID
2Ah	00101010	1010	10	225	10
2Bh	00101011	1011	11	247.5	11
2Ch	00101100	1100	12	270	12
2Dh	00101101	1101	13	292.5	13
2Eh	00101110	1110	14	315	14
2Fh	00101111	1111	15	337.5	15
30h	00110000	0000	0	0	16
31h	00110001	0001	1	22.5	17
32h	00110010	0010	2	45	18
33h	00110011	0011	3	67.5	19
34h	00110100	0100	4	90	20
35h	00110101	0101	5	112.5	21
36h	00110110	0110	6	135	22
37h	00110111	0111	7	157.5	23

4.14 Monitoring with SMBus

The RAA210850 can monitor a wide variety of system parameters with the following PMBus commands:

- READ_VIN
- READ_VOUT
- READ_IOUT
- READ_INTERNAL_TEMP
- READ_DUTY_CYCLE
- READ_FREQUENCY
- READ_VMON

4.15 Snapshot Parameter Capture

The RAA210850's snapshot feature captures parametric data and some fault status following a fault. A detailed description is provided in the "SNAPSHOT (EAh)" and "SNAPSHOT_CONTROL (F3h)" sections of "PMBus Commands Description" on page 35.

5. Layout Guidelines

To achieve stable operation, low losses, and good thermal performance, proper layout (Figure 28) is important.

- Establish separate SGND plane and PGND planes, then connect SGND to the PGND plane on the middle layer and underneath PAD6 with a single point connection. For SGND and PGND pin connections, such as small pins H16, J16, M5, and M17..., use multiple vias for each pin to connect to the inner SGND or PGND layer.
- Place enough ceramic capacitors between VIN and PGND, VOUT and PGND, and bypass capacitors between VDD, VDRV, and the ground plane, as close to the module as possible to minimize high frequency noise. It is critical to place the output ceramic capacitors as close to the center of the two VOUT pads as possible, to create a low impedance path for the high frequency inductor ripple current.
- Use large copper areas for power path (VIN, PGND, VOUT) to minimize conduction loss and thermal stress. Also, use multiple vias to connect the power planes in different layers. Renesas recommends enlarging PAD11 and PAD15 and placing more vias on these pads. The ceramic caps CIN can be put on the bottom layer under these two pads.
- Connect remote sensed traces to the regulation points to achieve a tight output voltage regulation and keep them in parallel. Route a trace from VSENN and VSENP to the point of load where the tight output voltage is desired. Avoid routing any sensitive signal traces, such as the VSENN, VSENP sensing point near the SW pins.
- The SW1 and SW2 pads are noisy pads, but they are beneficial for thermal dissipation. If the noise issue is critical for the application, Renesas recommends using the top layer only for SW pads. For better thermal performance, use multiple vias on these pads to connect into SW inner and bottom layer. However, be very careful when placing limited SW planes in any layer. The SW planes should avoid the sensing signals and should be surrounded by the PGND layer to avoid noise coupling.
- For pins SWD1 (L3) and SWD2 (P10), it is recommended to connect to the related SW1 and SW2 pads with short loop wires. The wire width should be greater than 20 mils.

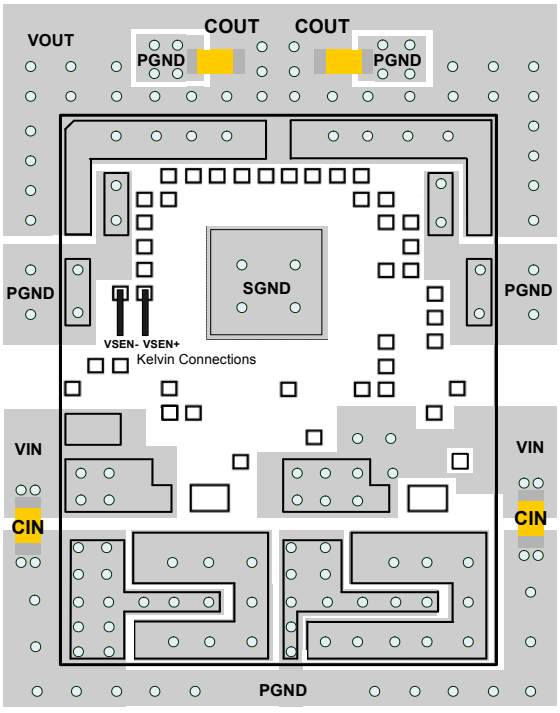


Figure 28. Recommended Layout

5.1 Thermal Considerations

Experimental power loss curves along with θ_{JA} from thermal modeling analysis can be used to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +125°C. In actual applications, other heat sources and design margins should be considered.

5.2 Package Description

The RAA210850 uses the High Density Array No-lead package (HDA). This package offers good thermal and electrical conductivity, low weight, and small size. The HDA package is applicable for surface mounting technology and is being more readily used in the industry. The RAA210850 contains several types of devices, including resistors, capacitors, inductors, and control ICs. The RAA210850 is a copper lead-frame based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper lead frame and multi component assembly is overmolded with polymer mold compound to protect these devices.

The package outline and typical PCB layout pattern design and typical stencil pattern design are shown in the "Package Outline Drawing" starting on page 51. The module has a small size of 18mmx23mmx7.5mm.

5.3 PCB Layout Pattern Design

The bottom of the RAA210850 is a lead-frame footprint, which is attached to the PCB by a surface mounting process. The PCB layout pattern is shown on pages 55 to 57. The PCB layout pattern is an array of solder mask defined PCB lands which align with the perimeters of the HDA exposed pads and I/O termination dimensions. The thermal lands on the PCB layout also feature an array of solder mask defined lands and should match 1:1 with the package exposed die pad perimeters. The exposed solder mask defined PCB land area should be 50-80% of the available module I/O area.

5.4 Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 ounce copper. Although adding more vias (by decreasing via pitch) improves the thermal performance, diminishing returns are seen as the number of vias increases. Use as many vias as practical for the thermal land size and your board design rules allow.

5.5 Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2mil to 3mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joints. The stencil aperture size to solder mask defined PCB land size ratio should typically be 1:1. The aperture width can be reduced slightly to help prevent solder bridging between adjacent I/O lands. A typical solder stencil pattern is shown in the "Package Outline Drawing" starting on page 51. The gap width between pad to pad is 0.6mm. Consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing "smooths" the aperture walls, resulting in reduced surface friction and better paste release which reduces voids. Using a Trapezoidal Section Aperture (TSA) also promotes paste release and forms a brick-like paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch HDA.

5.6 Reflow Parameters

Due to the HDA's low mount height, "No Clean" Type 3 solder paste per ANSI/J-STD-005 is recommended. Nitrogen purge is recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the HDA. The profile in Figure 29 is a guideline to be customized for varying manufacturing practices and applications.

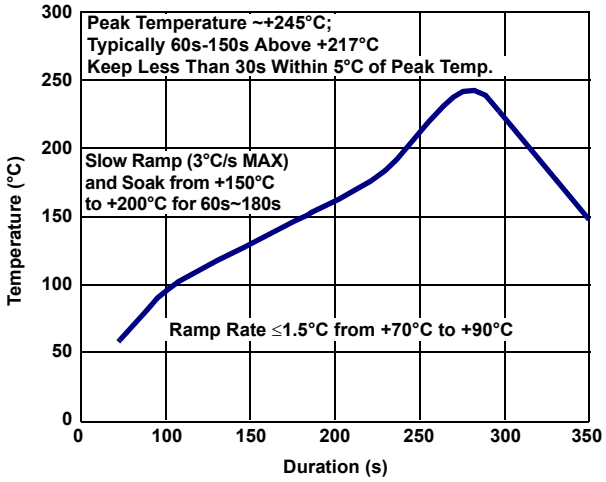


Figure 29. Typical Reflow Profile

6. PMBus Command Summary

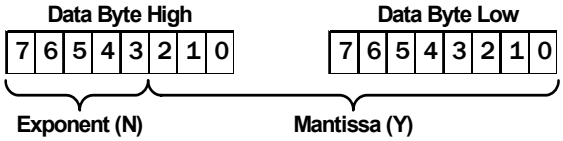
Command Code	Command Name	Description	Type	Data Format	Default Value	Default Setting	Page
01h	OPERATION	Sets the Enable and Disable settings.	R/W Byte	Bit			35
02h	ON_OFF_CONFIG	Configures the EN pin and PMBus commands to turn the unit ON/OFF	R/W Byte	Bit	16h	Hardware Enable, Soft Off	35
03h	CLEAR_FAULTS	Clears fault indications.	Send Byte				35
21h	VOUT_COMMAND	Sets the nominal value of the output voltage.	R/W Word	L16u		V_{OUT} Pin-Strap (set based on VSET_CRS and VSET_FINE)	36
24h	VOUT_MAX	Sets the maximum possible value of V_{OUT}. 110% of pin-strap V_{OUT}.	R/W Word	L16u		1.1 x V_{OUT} Pin-Strap	36
33h	FREQUENCY_SWITCH	Sets the switching frequency.	R/W Word	L11		Pin-Strap	36
37h	INTERLEAVE	Configures a phase offset between devices sharing a SYNC clock.	R/W Word	Bit	Pin-Strap (set based on SMBus address)		37
40h	VOUT_OV_FAULT_LIMIT	Sets the V_{OUT} overvoltage fault threshold.	R/W Word	L16u		1.15 x V_{OUT} Pin-Strap	37
44h	VOUT_UV_FAULT_LIMIT	Sets the V_{OUT} undervoltage fault threshold.	R/W Word	L16u		0.85 x V_{OUT} Pin-Strap	37
46h	IOUT_OC_FAULT_LIMIT	Sets the I_{OUT} average overcurrent fault threshold.	R/W Word	L11	E3C0h	60A	37
4Bh	IOUT_UC_FAULT_LIMIT	Sets the I_{OUT} average undercurrent fault threshold.	R/W Word	L11	E440h	-60A	38
4Fh	OT_FAULT_LIMIT	Sets the over-temperature fault threshold.	R/W Word	L11	EB98h	+115°C	38
53h	UT_FAULT_LIMIT	Sets the under-temperature fault threshold.	R/W Word	L11	E530h	-45°C	38
55h	VIN_OV_FAULT_LIMIT	Sets the V_{IN} overvoltage fault threshold.	R/W Word	L11	D3A0h	14.5V	38
59h	VIN_UV_FAULT_LIMIT	Sets the V_{IN} undervoltage fault threshold.	R/W Word	L11		Pin-Strap	39
5Eh	POWER_GOOD_ON	Sets the voltage threshold for Power-Good indication.	R/W Word	L16u		0.9 x V_{OUT} Pin-Strap	39
60h	TON_DELAY	Sets the delay time from ENABLE to start of V_{OUT} rise.	R/W Word	L11		Pin-Strap	39
61h	TON_RISE	Sets the rise time of V_{OUT} after ENABLE and TON_DELAY.	R/W Word	L11		Pin-Strap	39
64h	TOFF_DELAY	Sets the delay time from DISABLE to start of V_{OUT} fall.	R/W Word	L11		Pin-Strap	40
65h	TOFF_FALL	Sets the fall time for V_{OUT} after DISABLE and TOFF_DELAY.	R/W Word	L11		Pin-Strap	40

Command Code	Command Name	Description	Type	Data Format	Default Value	Default Setting	Page
78h	STATUS_BYTE	Returns an abbreviated status for fast reads.	Read Byte	Bit	00h	No Faults	40
79h	STATUS_WORD	Returns information with a summary of the unit's fault condition.	Read Word	Bit	0000h	No Faults	41
7Ah	STATUS_VOUT	Returns the V_{OUT} specific status.	Read Byte	Bit	00h	No Faults	42
7Bh	STATUS_IOUT	Returns the I_{OUT} specific status.	Read Byte	Bit	00h	No Faults	42
7Ch	STATUS_INPUT	Returns specific status specific to the input.	Read Byte	Bit	00h	No Faults	43
7Dh	STATUS_TEMPERATURE	Returns the temperature specific status.	Read Byte	Bit	00h	No Faults	43
7Eh	STATUS_CML	Returns the Communication, Logic, and Memory specific status.	Read Byte	Bit	00h	No Faults	44
80h	STATUS_MFR_SPECIFIC	Returns the VMON and External Sync clock specific status.	Read Byte	Bit	00h	No Faults	44
88h	READ_VIN	Returns the input voltage reading.	Read Word	L11			44
8Bh	READ_VOUT	Returns the output voltage reading.	Read Word	L16u			45
8Ch	READ_IOUT	Returns the output current reading.	Read Word	L11			45
8Dh	READ_INTERNAL_TEMP	Returns the temperature reading internal to the device.	Read Word	L11			45
94h	READ_DUTY_CYCLE	Returns the duty cycle reading during the ENABLE state.	Read Word	L11			45
95h	READ_FREQUENCY	Returns the measured operating switch frequency.	Read Word	L11			45
96h	READ_IOUT_0	Returns phase 1 current reading.	Read Word	L11			45
97h	READ_IOUT_1	Returns phase 2 current reading.	Read Word	L11			46
DFh	ASCR_CONFIG	Configures ASCR control loop.	R/W Block	CUS		Pin-Strap	46
E4h	DEVICE_ID	Returns the 16-byte (character) device identifier string.	Read Block	ASC		Reads Device Version	46
E5h	MFR_IOUT_OC_FAULT_RESPONSE	Configures the I_{OUT} overcurrent fault response.	R/W Byte	Bit	B9h	Disable and 70ms Continuous Retry	47
E6h	MFR_IOUT_UC_FAULT_RESPONSE	Configures the I_{OUT} undercurrent fault response.	R/W Byte	Bit	B9h	Disable and 70ms Continuous Retry	47

Command Code	Command Name	Description	Type	Data Format	Default Value	Default Setting	Page
EAh	SNAPSHOT	Returns 32-byte read-back of parametric and status values.	Read Block	Bit			48
F3h	SNAPSHOT_CONTROL	Snapshot feature control command.	R/W Byte	Bit			48
F5h	MFR_VMON_OV_FAULT_LIMIT	Returns the VMON overvoltage threshold.	Read Word	L11	CB00h	6V	49
F6h	MFR_VMON_UV_FAULT_LIMIT	Returns the VMON undervoltage threshold.	Read Word	L11	CA00h	4V	49
F7h	MFR_READ_VMON	Returns the VMON voltage reading.	Read Word	L11			49

6.1 PMBus Data Formats

- **Linear-11 (L11)** - The L11 data format uses 5-bit two's complement exponent (N) and 11-bit two's complement mantissa (Y) to represent real world decimal value (X). The relation between real world decimal value (X), N and Y is: $X = Y \cdot 2^{N}$.



- **Linear-16 Unsigned (L16u) -** The L16u data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit unsigned integer mantissa (Y) to represent the real world decimal value (X). The relation between the real world decimal value (X), N and Y is: $X = Y \cdot 2^{-13}$.
- **Linear-16 Signed (L16s)** - The L16s data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit two's complement mantissa (Y) to represent the real world decimal value (X).
  The relation between the real world decimal value (X), N and Y is: $X = Y \cdot 2^{-13}$.
- **Bit Field (BIT) -** An explanation of the Bit Field is provided in "PMBus Commands Description" on page 35.
- **Custom (CUS) -** An explanation of the Custom data format is provided in "PMBus Commands Description" on page 35. A combination of Bit Field and integer are common type of Custom data format.
- **ASCII (ASC) -** A variable length string of text characters that uses the ASCII data format.

6.2 PMBus Use Guidelines

The PMBus is a powerful tool that allows the user to optimize circuit performance by configuring devices for their application. When configuring a device in a circuit, the device should be disabled whenever most settings are changed with PMBus commands. Some exceptions to this recommendation are OPERATION, ON_OFF_CONFIG, CLEAR_FAULTS, VOUT_COMMAND, and ASCR_CONFIG. While the device is enabled any command can be read. Many commands do not take effect until after the device has been re-enabled, hence the recommendation that commands that change device settings are written while the device is disabled.

In addition, there should be a 2ms delay between repeated READ commands sent to the same device. When sending any other command, a 5ms delay is recommended between repeated commands sent to the same device. Commands not listed in the PMBus command summary are not allowed for customer use, and are reserved for factory use only. Issuing reserved commands may result in unexpected operation.

7. PMBus Commands Description

OPERATION (01h)

Definition: Sets the Enable and Disable settings.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value:

Units: N/A

Settings	Actions
00h	Immediate off
40h	Soft off
80h	On

ON_OFF_CONFIG (02h)

Definition: Configures the interpretation and coordination of the OPERATION command and the ENABLE pin (EN).

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 16h (Device starts from ENABLE pin with soft off)

Units: N/A

Settings	Actions
16h	Device starts from ENABLE pin with soft off.
17h	Device starts from ENABLE pin with immediate off.
1Ah	Device starts from OPERATION command with soft off.
1Bh	Device starts from OPERATION command with immediate off.

CLEAR_FAULTS (03h)

Definition: Clears all fault bits in all registers and releases the SALRT pin (if asserted) simultaneously. If a fault condition still exists, the bit reasserts immediately. This command does not restart a device if it has shut down, it will clears the faults.

Data Length in Bytes: 0 Byte

Data Format: N/A

Type: Write only

Default Value: N/A

Units: N/A

Reference: N/A

VOUT_COMMAND (21h)

Definition: Sets or reports the target output voltage. This command cannot set a value higher than either VOUT_MAX or 110% of the pin-strap V_{OUT} setting.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: Pin-strap setting (set based on VSET_CRS and VSET_FINE)

Units: Volts

Range: 0V to VOUT_MAX

VOUT_MAX (24h)

Definition: Sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output overprotection. The default value can be changed using PMBus.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 1.10 x V_{OUT} pin-strap setting

Units: Volts

Range: 0V to 5.5V

FREQUENCY_SWITCH (33h)

Definition: Sets the switching frequency of the device. The initial default value is defined by a pin-strap and this value can be overridden by writing this command using PMBus. The output must be disabled when writing this command.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: kHz

Range: 296kHz to 1067kHz

INTERLEAVE (37h)

Definition: Configures the phase offset of a device that is sharing a common SYNC clock with other devices. The phase offset of each device can be set to any value between 0° and 360° in 22.5° increments. The internal two phases of the module always maintain a phase difference of 180°.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W

Default Value: Pin-strap (set based on SMBus address)

Units: N/A

Bits	Purpose	Value	Description
15:8	Reserved	0	These bits are reserved.
7:4	Group Number	0 to 15	Sets the group number. A value of 0 is interpreted as 16.
3:0	Position in Group	0 to 15	Sets position of the device's rail within the group.

VOUT_OV_FAULT_LIMIT (40h)

Definition: Sets the V_{OUT} overvoltage fault threshold.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 1.15 x V_{OUT} pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_UV_FAULT_LIMIT (44h)

Definition: Sets the V_{OUT} undervoltage fault threshold. This fault is masked during ramp or when disabled.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 0.85xV_{OUT} pin-strap setting

Units: V

Range: 0V to VOUT_MAX

IOUT_OC_FAULT_LIMIT (46h)

Definition: Sets the I_{OUT} average overcurrent fault threshold. The device automatically calculates the peak inductor overcurrent fault limit for each phase based on the equation:
$I_{OUT(PEAK\ OC\ LIMIT)} = (0.5 * IOUT\_OC\_FAULT\_LIMIT + 0.5 * I_{RIPPLE(P-P)}) * 120\%$. A hard bound of 42A is applied to the peak overcurrent fault limit per phase.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: E3C0h (60A)

Units: A

Range: -100A to 100A

IOUT_UC_FAULT_LIMIT (4Bh)

Definition: Sets the I_{OUT} average undercurrent fault threshold. The device automatically calculates the valley inductor undercurrent fault limit for each phase based on the equation: $I_{OUT(VALLEY\ UC\ LIMIT)}$ = (0.5 * IOUT_UC_FAULT_LIMIT - 0.5 * $I_{RIPPLE(P-P)}$) * 120%. A hard bound of -42A is applied to the valley undercurrent fault limit per phase.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: -60A

Units: A

Range: -100A to 100A

OT_FAULT_LIMIT (4Fh)

Definition: Sets the temperature at which the device should indicate an over-temperature fault. Note that the temperature must drop below the fault limit to clear this fault.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: EB98h (+115˚C)

Units: Celsius

Range: 0°C to +150°C

UT_FAULT_LIMIT (53h)

Definition: Sets the temperature, in degrees Celsius, of the unit where it should indicate an under-temperature fault.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: E530h (-45°C)

Units: Celsius

Range: -55°C to +25°C

VIN_OV_FAULT_LIMIT (55h)

Definition: Sets the V_{IN} overvoltage fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: D3A0h (14.5V)

Units: V

Range: 0V to 16V

VIN_UV_FAULT_LIMIT (59h)

Definition: Sets the V_{IN} undervoltage fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: V

Range: 0V to 12V

POWER_GOOD_ON (5Eh)

Definition: Sets the voltage threshold for Power-good indication. Power-good asserts after the output voltage exceeds POWER_GOOD_ON. Renesas recommends setting POWER_GOOD_ON higher than VOUT_UV_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 0.9 x V_{OUT} pin-strap setting

Units: V

TON_DELAY (60h)

Definition: Sets the delay time from when the device is enabled to the start of V_{OUT} rise.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: ms

Range: 2 to 300ms

TON_RISE (61h)

Definition: Sets the rise time of V_{OUT} after ENABLE and TON_DELAY.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: ms

Range: 0 to 120ms

TOFF_DELAY (64h)

Definition: Sets the delay time from DISABLE to the start of V_{OUT} fall.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: ms

Range: 2 to 300ms

TOFF_FALL (65h)

Definition: Sets the soft-off fall time for V_{OUT} after DISABLE and TOFF_DELAY.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: ms

Range: 0 to 120ms

STATUS_BYTE (78h)

Definition: Returns one byte of information with a summary of the most critical faults.

Data Length in Bytes: 1

Data Format: BIT

Type: Read-only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault has occurred.
1	CML	A communications, memory or logic fault has occurred.
0	None of the Above	A fault not listed in Bits 7:1 has occurred.

STATUS_WORD (79h)

Definition: Returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (78h) command.

Data Length in Bytes: 2

Data Format: BIT

Type: Read-only

Default Value: 0000h

Units: N/A

Bit Number	Status Bit Name	Meaning
15	VOUT	An output voltage fault has occurred.
14	IOUT/POUT	An output current or output power fault has occurred.
13	INPUT	An input voltage, input current, or input power fault has occurred.
12	MFG_SPECIFIC	A manufacturer specific fault has occurred.
11	POWER_GOOD#	The POWER_GOOD signal, if present, is negated.
10	Reserved	This bit is reserved.
9	OTHER	A bit in STATUS_OTHER is set.
8	UNKNOWN	A fault type not given in bits 15:1 of the STATUS_WORD has been detected.
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault has occurred.
1	CML	A communications, memory, or logic fault has occurred.
0	None of the Above	A fault not listed in Bits 7:1 has occurred.

STATUS_VOUT (7Ah)

Definition: Returns one data byte with the status of the output voltage.

Data Length in Bytes: 1

Data Format: BIT

Type: Read-only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	VOUT_OV_FAULT	Indicates an output overvoltage fault.
6:5	Reserved	These bits are reserved.
4	VOUT_UV_FAULT	Indicates an output undervoltage fault.
3:0	N/A	These bits are not used.

STATUS_IOUT (7Bh)

Definition: Returns one data byte with the status of the output current.

Data Length in Bytes: 1

Data Format: BIT

Type: Read-only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	IOUT_OC_FAULT	An output overcurrent fault has occurred.
6:5	Reserved	These bits are reserved.
4	IOUT_UC_FAULT	An output undercurrent fault has occurred.
3:0	N/A	These bits are not used.

STATUS_INPUT (7Ch)

Definition: Returns input voltage and input current status information.

Data Length in Bytes: 1

Data Format: BIT

Type: Read-only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	VIN_OV_FAULT	An input overvoltage fault has occurred.
6:5	Reserved	These bits are reserved.
4	VIN_UV_FAULT	An input undervoltage fault has occurred.
3:0	N/A	These bits are not used.

STATUS_TEMPERATURE (7Dh)

Definition: Returns one byte of information with a summary of any temperature related faults.

Data Length in Bytes: 1

Data Format: BIT

Type: Read-only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	OT_FAULT	An over-temperature fault has occurred.
6:5	Reserved	These bits are reserved.
4	UT_FAULT	An under-temperature fault has occurred.
3:0	N/A	These bits are not used.

STATUS_CML (7Eh)

Definition: Returns one byte of information with a summary of any communications, logic, and/or memory errors.

Data Length in Bytes: 1

Data Format: BIT

Type: Read-only

Default Value: 00h

Units: N/A

Bit Number	Meaning
7	Invalid or unsupported PMBus command was received.
6	The PMBus command was sent with invalid or unsupported data.
5	Packet error was detected in the PMBus command.
4	Memory/logic fault.
3:2	These bits are reserved.
1	A PMBus command tried to write to a read-only or protected command, or a communication fault other than the ones listed in this table has occurred.
0	This bit is reserved.

STATUS_MFR_SPECIFIC (80h)

Definition: Returns one byte of information providing the status of the device's voltage monitoring and clock synchronization faults.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default Value: 00h

Units: N/A

Bit Number	Field Name	Meaning
7:4	Reserved	These bits are reserved.
3	External Switching Period Fault	Loss of external clock synchronization has occurred.
2	Reserved	This bit is reserved.
1	VMON UV Fault	The voltage on the VMON pin has dropped below the level set by VMON_UV_FAULT_LIMIT.
0	VMON OV Fault	The voltage on the VMON pin has risen above the level set by VMON_OV_FAULT_LIMIT.

READ_VIN (88h)

Definition: Returns the input voltage reading.

Data Length in Bytes: 2

Data Format: L11

Type: Read-only

Units: V

READ_VOUT (8Bh)

Definition: Returns the output voltage reading.

Data Length in Bytes: 2

Data Format: L16u

Type: Read-only

Units: V

READ_IOUT (8Ch)

Definition: Returns the output current reading.

Data Length in Bytes: 2

Data Format: L11

Type: Read-only

Default Value: N/A

Units: A

READ_INTERNAL_TEMP (8Dh)

Definition: Returns the controller junction temperature reading from internal temperature sensor.

Data Length in Bytes: 2

Data Format: L11

Type: Read-only

Units: °C

READ_DUTY_CYCLE (94h)

Definition: Reports the actual duty cycle of the converter during the enable state.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Units: %

READ_FREQUENCY (95h)

Definition: Reports the actual switching frequency of the converter during the enable state.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Units: kHz

READ_IOUT_0 (96h)

Definition: Returns the Phase 1 current reading.

Data Length in Bytes: 2

Data Format: L11

Type: Read-only

Default Value: N/A

Units: A

READ_IOUT_1 (97h)

Definition: Returns the Phase 2 current reading.

Data Length in Bytes: 2

Data Format: L11

Type: Read-only

Default Value: N/A

Units: A

ASCR_CONFIG (DFh)

Definition: Allows user configuration of ASCR settings. ASCR Gain is analogous to bandwidth and ASCR Residual is analogous to damping. To improve load transient response performance, increase ASCR Gain. To lower transient response overshoot, increase ASCR Residual. Increasing ASCR gain can result in increased PWM jitter and should be evaluated in the application circuit. Excessive ASCR gain can lead to excessive output voltage ripple. Increasing ASCR Residual to improve transient response damping can result in slower recovery times, but does not affect the peak output voltage deviation. Typical ASCR Gain settings range from 50 to 1000 and ASCR Residual settings range from 10 to 100.

Data Length in Bytes: 4

Data Format: CUS

Type: R/W

Default Value: Pin-strap setting

Bit	Purpose	Data Format	Value	Description
31:25	Unused		0000000h	Unused
24	Reserved			This bit is reserved
23:16	ASCR Residual Setting	Integer		ASCR residual
15:0	ASCR Gain Setting	Integer		ASCR gain

DEVICE_ID (E4h)

Definition: Returns the 16-byte (character) device identifier string.

Data Length in Bytes: 16

Data Format: ASCII

Type: Block Read

Default Value: Part number/Die revision/Firmware revision

MFR_IOUT_OC_FAULT_RESPONSE (E5h)

Definition: Configures the I_{OUT} overcurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the overcurrent status bit in STATUS_IOUT.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: B9h (Disable and 70ms continuous retry)

Units: N/A

Settings	Actions
80h	Disable with no retry.
B9h	Disable and continuous retry with 70ms delay.

MFR_IOUT_UC_FAULT_RESPONSE (E6h)

Definition: Configures the I_{OUT} undercurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the undercurrent status bit in STATUS_IOUT.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: B9h (Disable and 70ms continuous retry)

Units: N/A

Settings	Actions
80h	Disable with no retry.
B9h	Disable and continuous retry with 70ms delay.

SNAPSHOT (EAh)

Definition: A 32-byte read-back of parametric and status values. It allows monitoring and status data to be stored to flash following a fault condition. In case of a fault, the last updated values are stored to the flash memory. When the SNAPSHOT STATUS bit is set stored, the device will no longer automatically capture parametric and status values following fault until stored data are erased. Use the SNAPSHOT_CONTROL command to erase store data and clear the status bit before next ramp up. Data erased is not allowed when the module is enabled.

Data Length in Bytes: 32

Data Format: Bit field

Type: Block Read

Byte Number	Value	PMBus Command	Format
31:23	Reserved	These bits are reserved	00h
22	Flash Memory Status Byte FF - Not Stored 00 - Stored	N/A	BIT
21	Manufacturer Specific Status Byte	STATUS_MFR_SPECIFIC (80h)	Byte
20	CML Status Byte	STATUS_CML (7Eh)	Byte
19	Temperature Status Byte	STATUS_TEMPERATURE (7Dh)	Byte
18	Input Status Byte	STATUS_INPUT (7Ch)	Byte
17	I_{OUT} Status Byte	STATUS_IOUT (7Bh)	Byte
16	V_{OUT} Status Byte	STATUS_VOUT (7Ah)	Byte
15:14	Switching Frequency	READ_FREQUENCY (95h)	L11
13:12	Reserved	These bits are reserved	00h
11:10	Internal Temperature	READ_INTERNAL_TEMP (8Dh)	L11
9:8	Duty Cycle	READ_DUTY_CYCLE (94h)	L11
7:6	Reserved	These bits are reserved	L11
5:4	Output Current	READ_IOUT (8Ch)	L11
3:2	Output Voltage	READ_VOUT (8Bh)	L16u
1:0	Input Voltage	READ_VIN (88h)	L11

SNAPSHOT_CONTROL (F3h)

Definition: Writing a 01h causes the device to copy the current SNAPSHOT values from NVRAM to the 32-byte SNAPSHOT command parameter. Writing a 02h causes the device to write the current SNAPSHOT values to NVRAM, and writing a 03h erases all SNAPSHOT values from NVRAM. Write (02h) and Erase (03h) can only be used when the device is disabled. All other values are ignored.

Data Length in Bytes: 1

Data Format: Bit field

Type: R/W byte

Value	Description
01h	Read SNAPSHOT values from NVRAM
02h	Write SNAPSHOT values to NVRAM
03h	Erase SNAPSHOT values stored in NVRAM.

MFR_VMON_OV_FAULT_LIMIT (F5h)

Definition: Reads the VMON OV fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Default Value: CB00h (6V)

Units: V

Range: 4V to 6V

MFR_VMON_UV_FAULT_LIMIT (F6h)

Definition: Reads the VMON UV fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Default Value: CA00h (4V)

Units: V

Range: 4V to 6V

MFR_READ_VMON (F7h)

Definition: Reads the VMON voltage.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Default Value: N/A

Units: V

Range: 4V to 6V

8. Revision History

8.1 Firmware

Firmware Revision Code	Change Description	Note
RAA210850--G0100	Initial Release	Recommended for new designs.

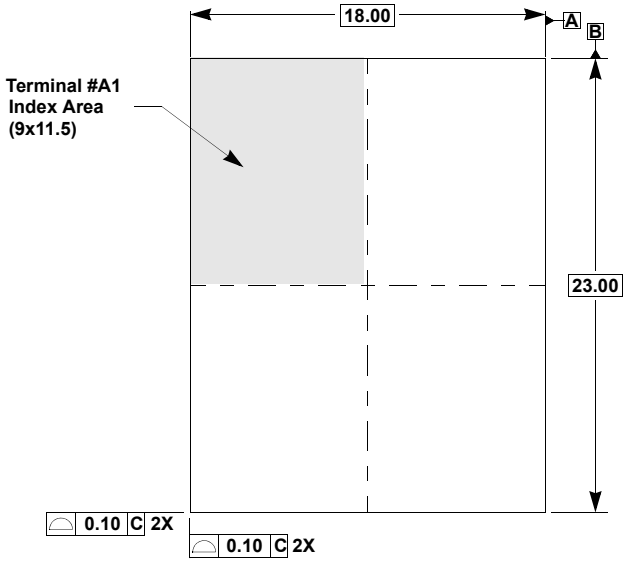
8.2 Datasheet

Rev	Date	Change
1.00	Mar 15, 2019	Updated pin configuration to show correct location for M5, N5, and N6. Updated description for pin D5. Changed PMBus to SMBus in the SMBus Communications section. Changed On-Nominal to On in the table under the OPERATION section on page 35. Updated Disclaimer.
0.00	Sep 12, 2018	Initial release.

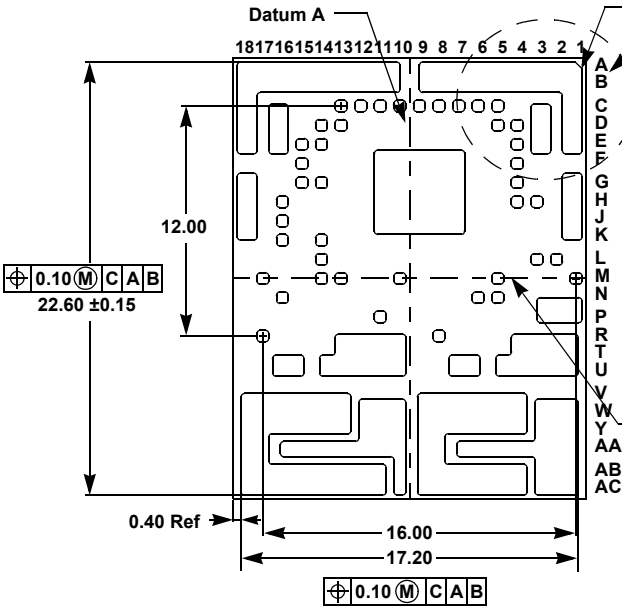
9. Package Outline Drawing

For the most recent package outline

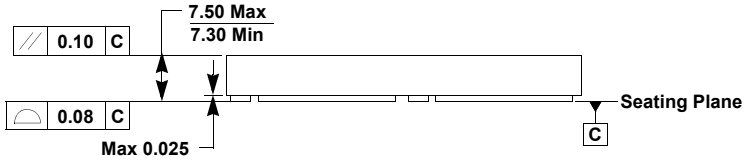
Y58.18x23
58 I/O 18mmx23mmx7.5mm Custom HDA Module
Rev 4, 4/18



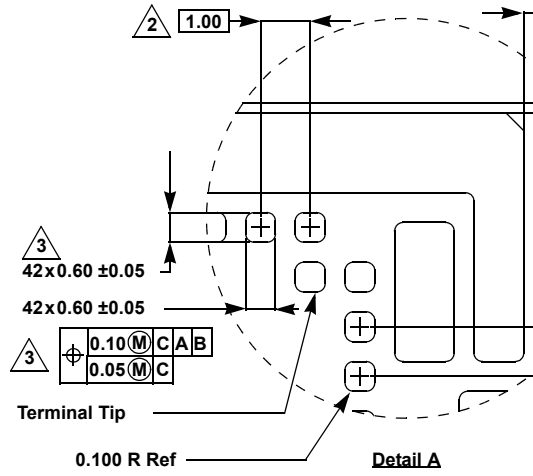
Top View



Bottom View



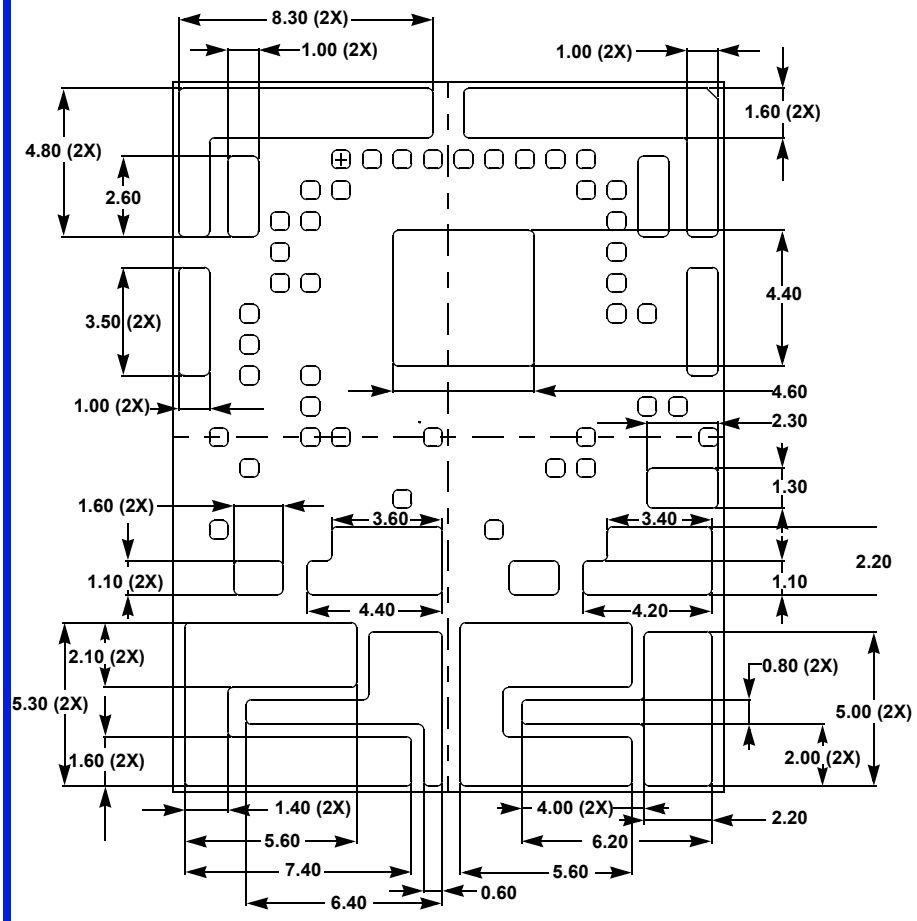
Side View



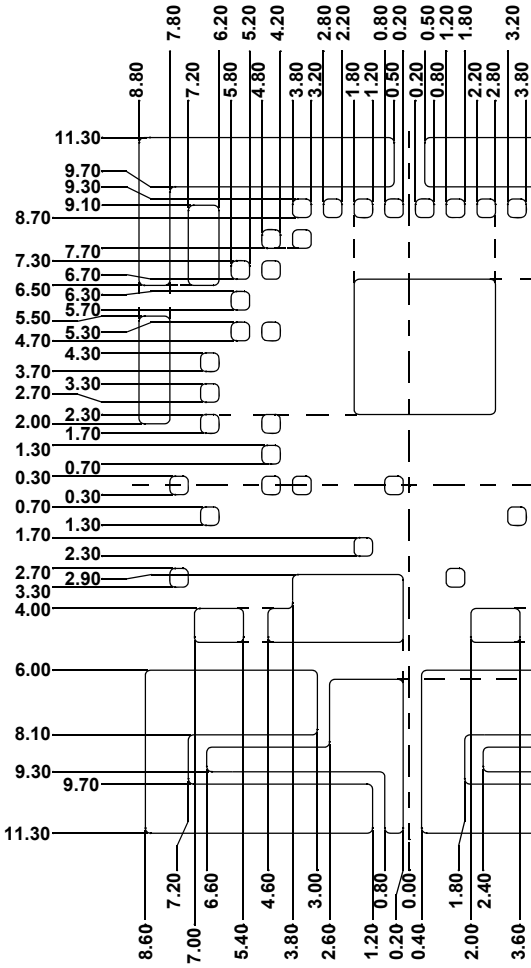
Detail A

Notes:

1. All dimensions are in millimeters.
2. Represents the basic land grid pitch.
3. These 42 I/Os are centered in a fixed row and column matrix at 1.0mm pitch BSC.
4. Dimensioning and tolerancing per ASME Y14.5-2009.
5. Tolerance for exposed PAD edge location dimension on page 3 is ±0.1mm.

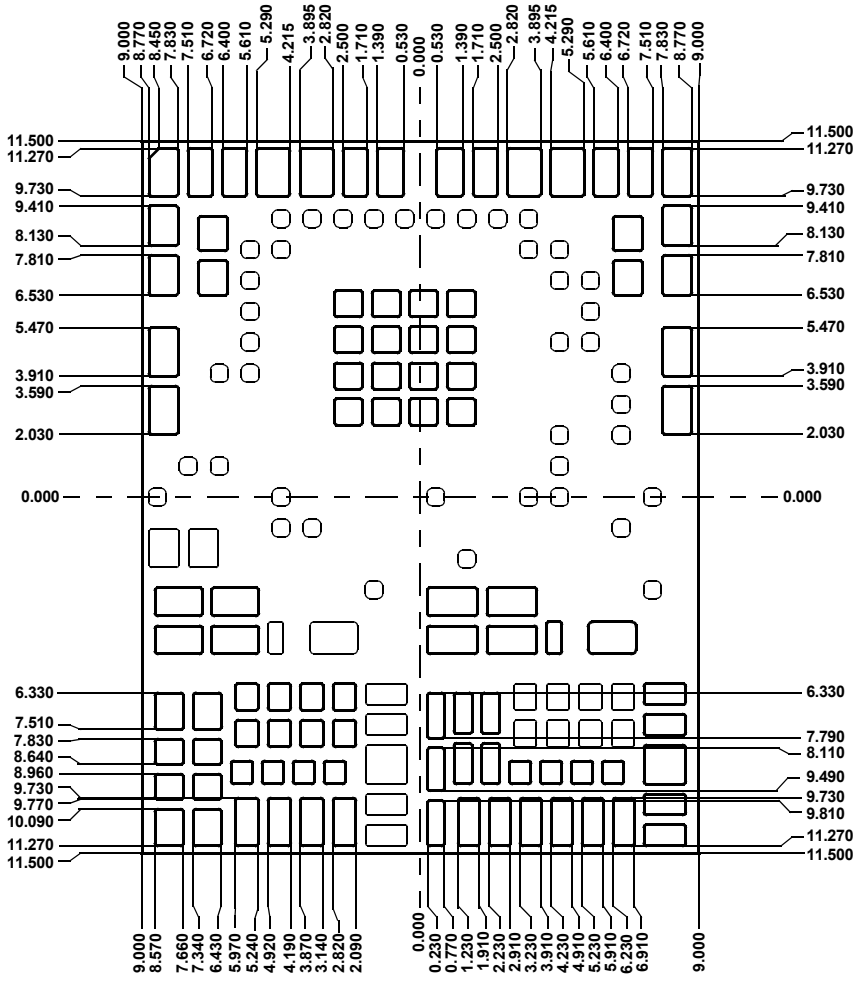


SIZE DETAILS FOR THE 16 EXPOSED PADS

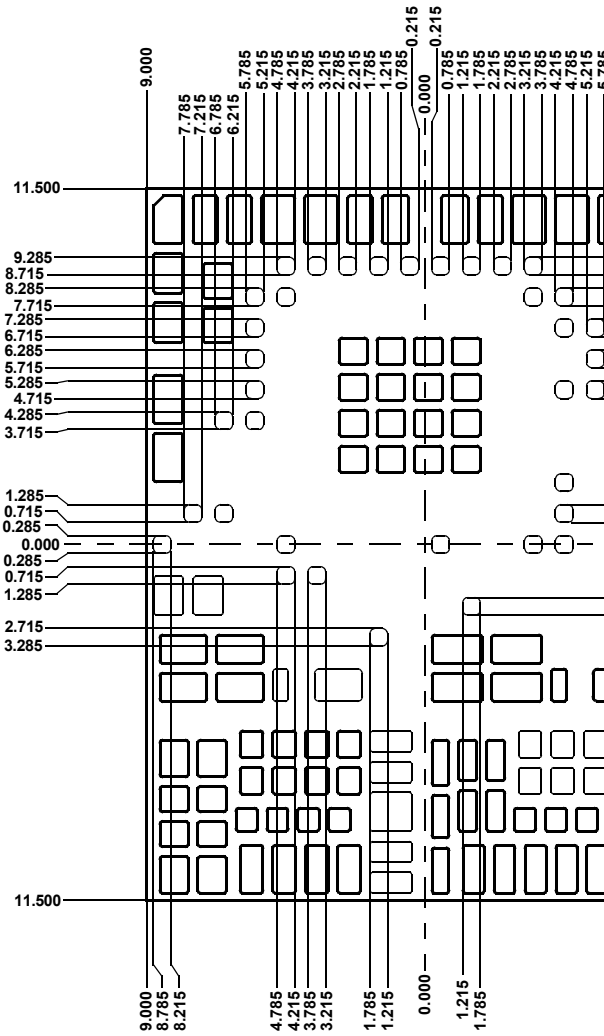


TERMINAL AND PAD EDGE DET

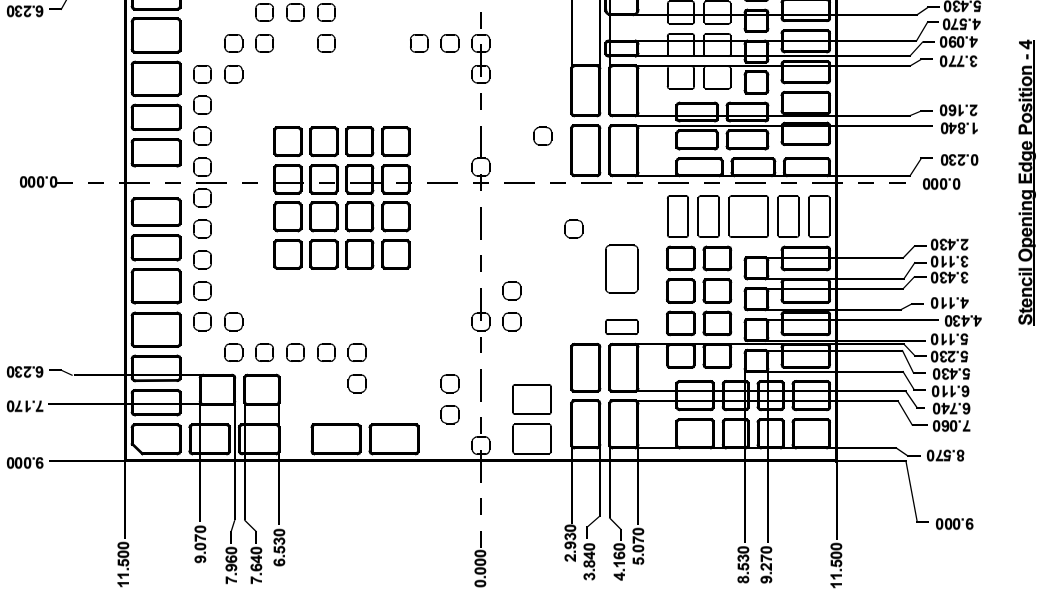
BOTTOM VIEW

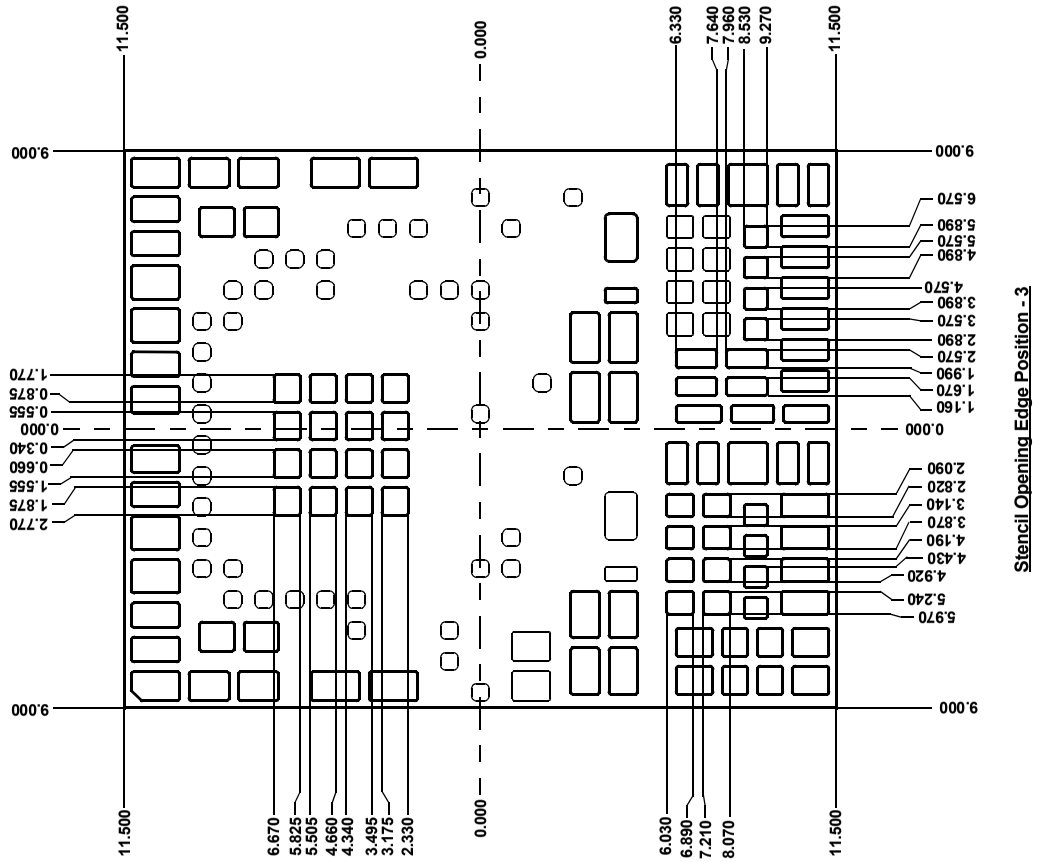


Stencil Opening Edge Position - 1



Stencil Opening Edge Position - 2


Stencil Opening Edge Position - 4
11.500
9.070
7.960
7.640
6.530
0.000
2.930
3.840
4.160
5.070
8.530
9.270
11.500
9.000
7.170
6.230
0.000
6.230
5.430
5.230
5.110
4.430
4.110
3.430
3.110
2.430
0.230
1.840
2.160
3.770
4.090
4.570
5.430


Stencil Opening Edge Position - 3
11.500
6.670
5.825
5.505
4.660
4.340
3.495
3.175
2.330
0.000
6.030
6.890
7.210
8.070
11.500
9.000
2.770
1.875
1.555
0.660
0.340
0.000
0.555
0.875
1.770
1.160
1.670
1.990
2.570
2.890
3.570
3.890
4.570
4.890
5.570
5.890
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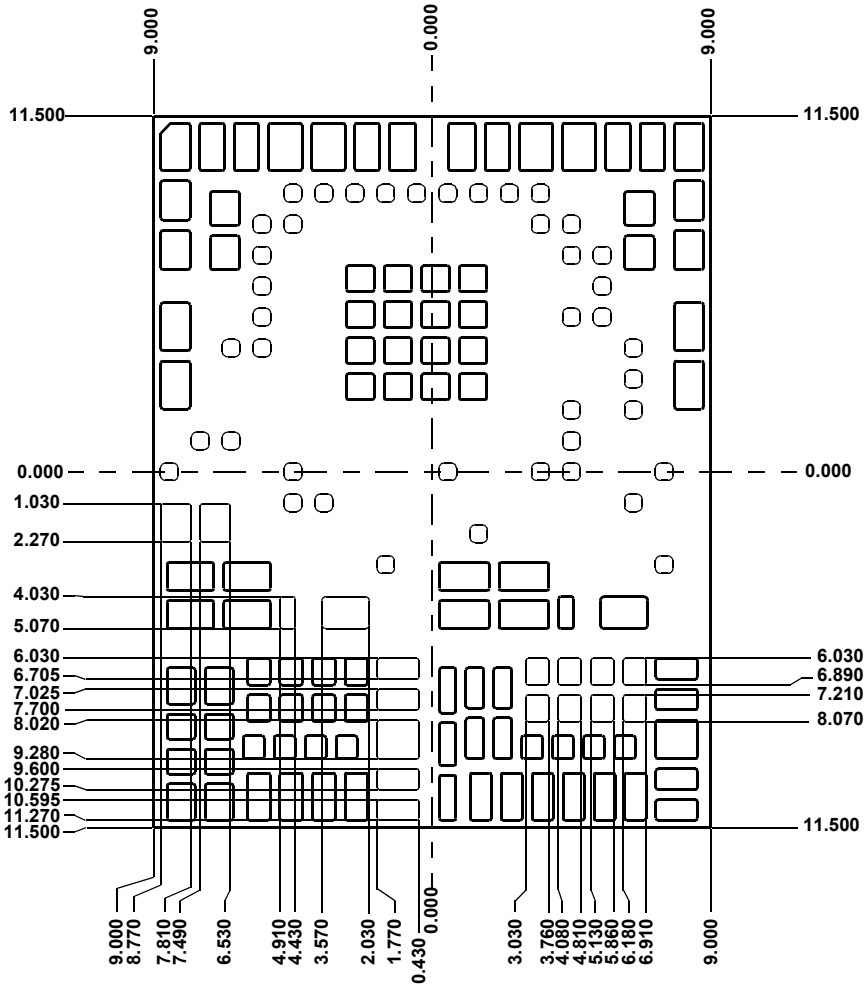
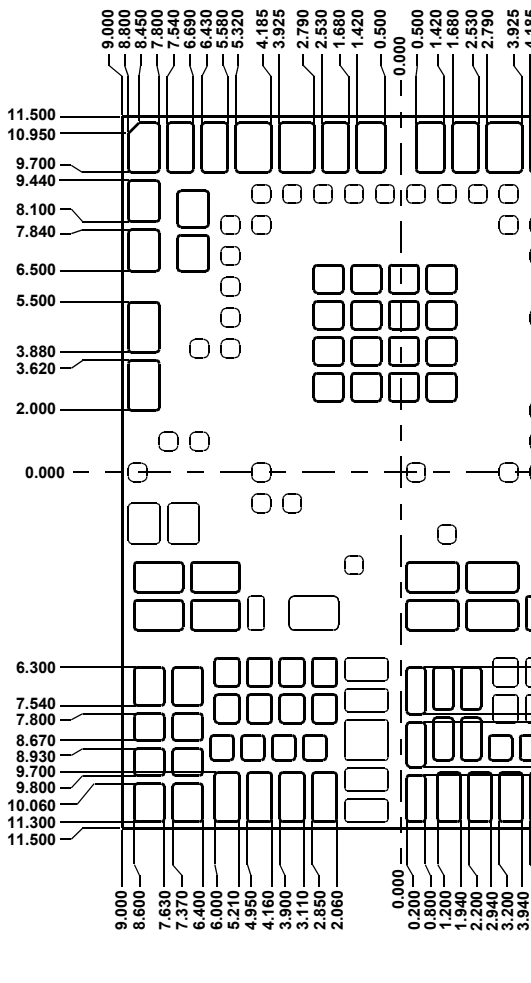
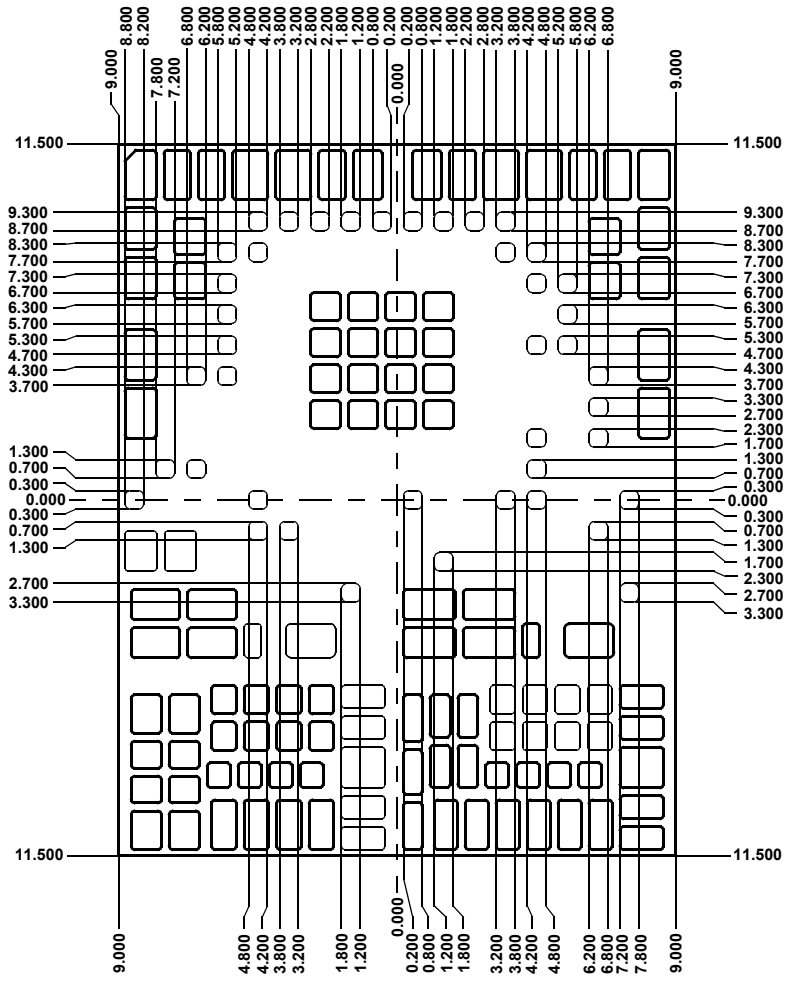
7.640
7.960
8.530
9.270
11.500
9.000



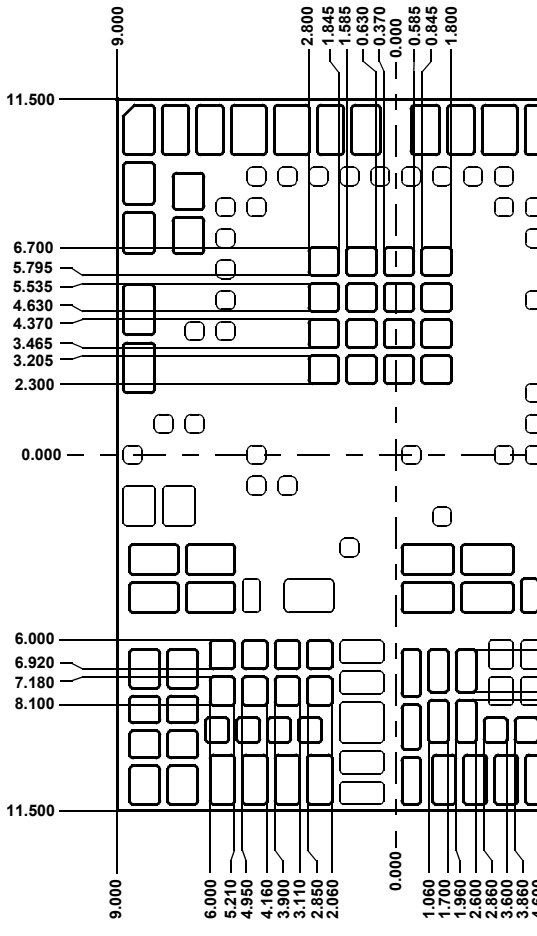
STENCIL OPENING EDGE POSITION - 5



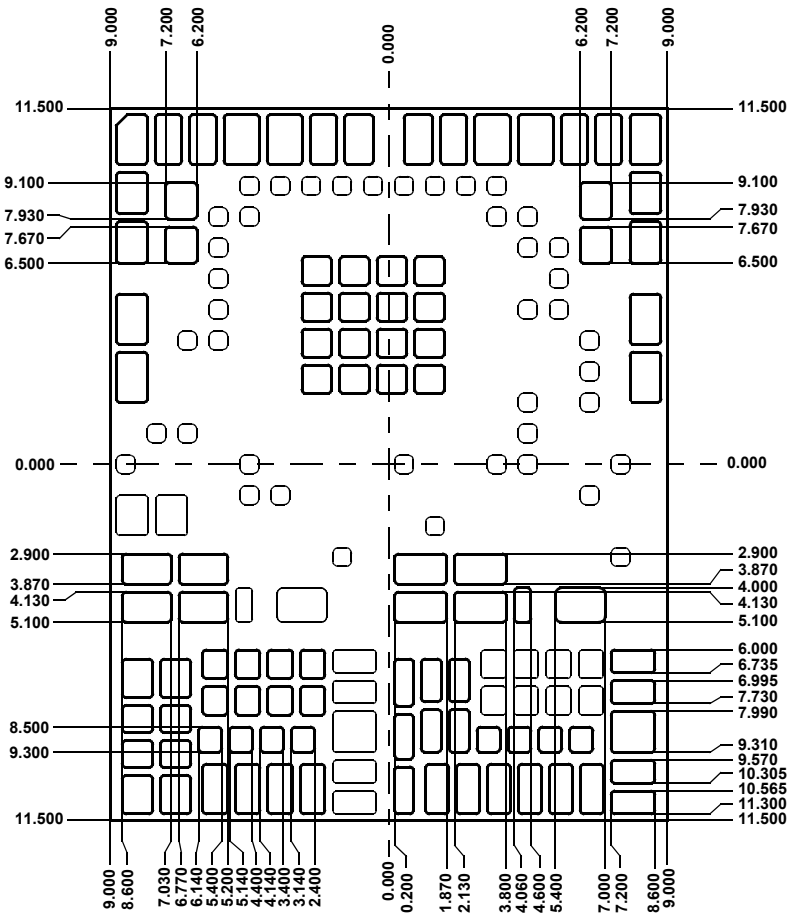
PCB LAND PATTERN - 1 (FOR REFER



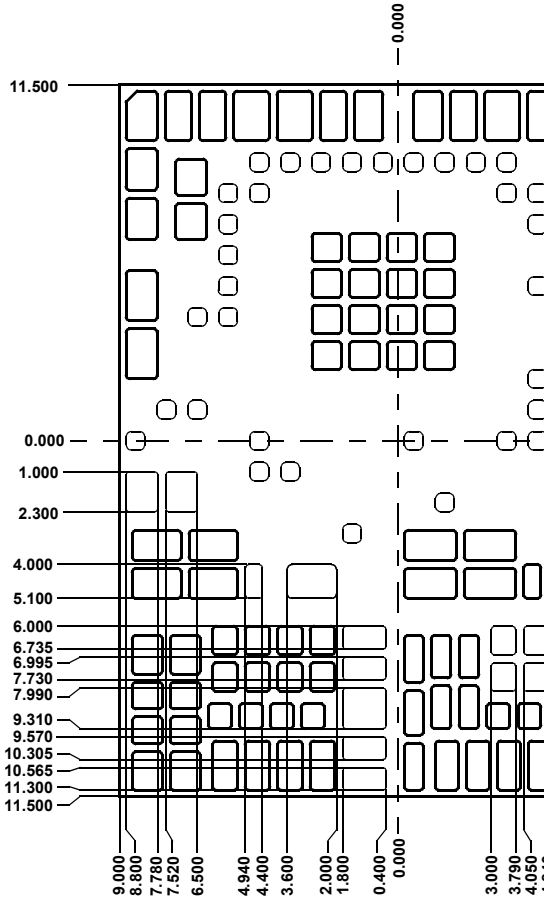
PCB LAND PATTERN - 2 (FOR REFERENCE)



PCB LAND PATTERN - 3 (FOR REFERE



PCB LAND PATTERN - 4 (FOR REFERENCE)



PCB LAND PATTERN - 5 (FOR REFERE

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