RAA210925

Pin-Configurable Dual 25A DC/DC Power Module with PMBus Interface

FN9352
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The RAA210925 is a pin-strap configurable dual 25A step-down PMBus-compliant DC/DC power supply module that integrates a digital PWM controller, synchronous MOSFETs, power inductor, and passive components. Only input and output capacitors are needed to finish the design. Because of its thermally-enhanced HDA packaging technology, the module can deliver up to 25A of continuous output current without the need for airflow or additional heat sinking. The RAA210925 simplifies configuration and control of Renesas digital power technology while offering an upgrade to full PMBus configuration through the pin-compatible ISL8274M.

Operating across an input voltage range of 4.5V to 14V, the RAA210925 offers adjustable output voltages down to 0.6V and achieves up to 95.5% conversion efficiencies. A unique ChargeMode™ control architecture provides a single clock cycle response to an output load step and can support switching frequencies up to 1067kHz. The power module integrates all power and most passive components and requires only a few external components to operate. The RAA210925 comes with a preprogrammed configuration for operating in Pin-strap mode. Output voltage, switching frequency, input UVLO, soft-start/stop delay and ramp times, tracking function, and the device SMBus address can be programmed with external pin-strap resistors. A standard PMBus interface addresses fault management, as well as real-time full telemetry and point-of-load monitoring. The RAA210925 is supported by PowerNavigator™ software, a Graphical User Interface (GUI), that can configure modules for desired solutions.

The RAA210925 is available in a low profile, compact 18mmx23mmx7.5mm fully encapsulated, thermally enhanced HDA package.

Related Literature

For a full list of related documents, visit our website:

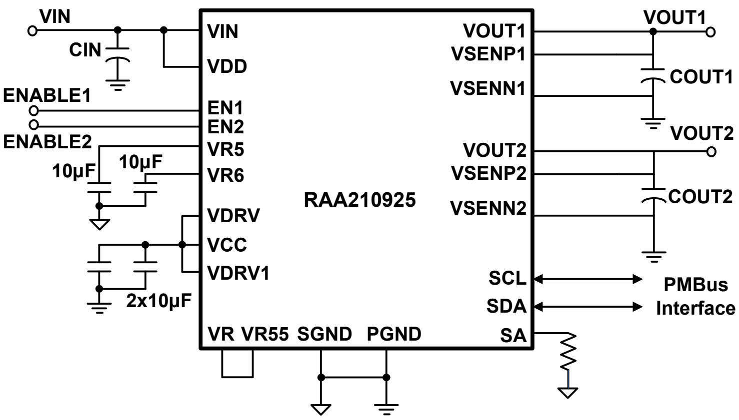
- RAA210925 device page

Features

- 25A/25A dual-channel output current
  - 4.5V to 14V single rail input voltage
  - Up to 95.5% efficiency
- Programmable output voltage
  - 0.6V to 5V output voltage settings
  - ±1.2% accuracy over line/load/temperature
- ChargeMode control loop architecture
  - 296kHz to 1067kHz fixed switching frequency operations
  - No compensation required
  - Fast single clock cycle transient response
- PMBus interface and/or pin-strap mode
  - Programmable through PMBus
  - Pin-strap mode for standard settings
  - Real-time telemetry for V_{IN}, V_{OUT}, I_{OUT}, temperature, duty cycle, and f_{SW}
- Complete over/undervoltage, current, and temperature protections with fault logging
- PowerNavigator supported
- Thermally enhanced 18mmx23mmx7.5mm HDA package

Applications

- Server, telecom, storage, and datacom
- Industrial/ATE and networking equipment
- General purpose power for ASIC, FPGA, DSP, and memory



Note: This figure represents a typical implementation of the RAA210925. For PMBus operation, it is recommended to tie the enable pin (EN) to SGND.

Figure 1. Application Circuit

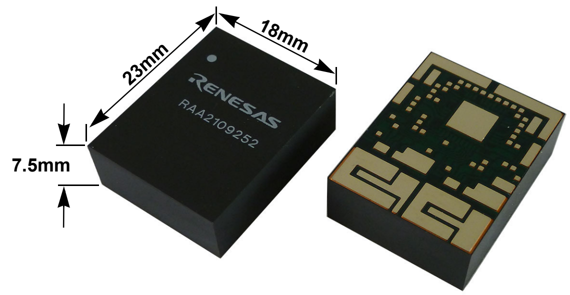
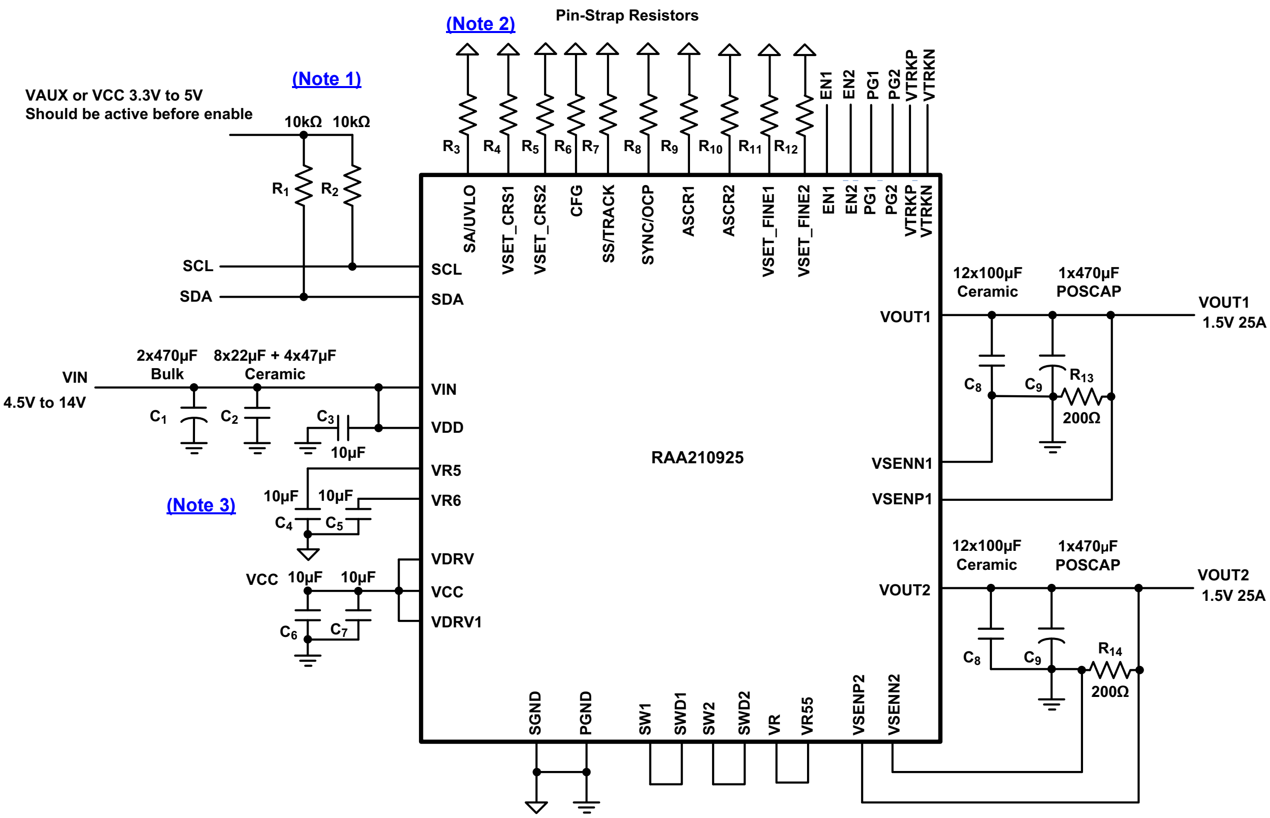


Figure 2. Small Package for High Power Density

Contents

1. Overview

1.1 Typical Application Circuit



Notes:
1. R_1 and R_2 are not required if the PMBus host already has I^2C pull-up resistors.
2. R_3 through R_{11} can be selected according to the tables for the pin-strap resistor setting in this document.
3. V25, VR, and VR55 do not need external capacitors. V25 can be no connection.

Figure 3. RAA210925 Digital PMBus Module Dual 25A/25A Application with Pin-Strap Settings

Table 1. RAA210925 Design Guide Matrix and Output Voltage Response

V_{IN} (V)	V_{OUT} (V)	f_{SW} (kHz)	I_{OUT} (A)	Avg OCP (A)	C_{IN} (µF)	Cout_Bulk (µF) (Note 4)	Cout_Ceramic (µF) (Note 4)	ASCR Gain (Note 6)
12	5	1067	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	6*100	275
12	5	615	20	25	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	6*100	175
12	3.3	800	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	8*100	300
12	3.3	571	20	25	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	8*100	175
12	2.5	1067	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	9*100	600
12	2.5	615	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	9*100	275
12	2.5	471	20	25	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	9*100	175
12	1.8	889	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	12*100	600
12	1.8	421	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	12*100	225
12	1.8	364	20	25	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	12*100	175
12	1.5	889	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	12*100	525
12	1.5	421	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	12*100	225
12	1.5	320	20	25	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	12*100	140
12	1.2	727	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	12*100	600
12	1.2	296	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	4*470	12*100	225
12	1	615	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	12*100	450
12	1	296	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	5*470	12*100	250
12	0.6	296	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	7*470	12*100	300
5	2.5	1067	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	9*100	600
5	2.5	615	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	9*100	275
5	2.5	471	20	25	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	9*100	175
5	1.8	889	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	12*100	600
5	1.8	421	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	12*100	250
5	1.8	364	20	25	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	12*100	200
5	1.5	889	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	12*100	525
5	1.5	421	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	12*100	250
5	1.5	320	20	25	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	12*100	140
5	1.2	727	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	12*100	600

Table 1. RAA210925 Design Guide Matrix and Output Voltage Response (Continued)

V_{IN} (V)	V_{OUT} (V)	f_{SW} (kHz)	I_{OUT} (A)	Avg OCP (A)	C_{IN} (µF)	Cout_Bulk (µF) (Note 4)	Cout_Ceramic (µF) (Note 4)	ASCR Gain (Note 6)
5	1.2	296	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	4*470	12*100	250
5	1	615	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	1*470	12*100	450
5	1	296	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	5*470	12*100	250
5	0.6	296	25	30	2*470µF POS + (8*22µF + 4*47µF) ceramic	7*470	12*100	300

Notes:

4. 100µF (GRM31CD80J107ME39L) ceramic and 470µF (6TPF470MAH) are selected for output capacitor in the evaluation board.
5. Peak-to-peak V_{OUT} deviation is measured under 0%-60% load transient with 15A/µs load step slew rate.
6. ASCR gain and residual was designed to achieve 50° phase margin at room temperature.
7. Frequency is selected to achieve the highest efficiency at full load as well as avoid saturation of the inductor. For instance, select 615kHz instead of 296k avoid inductor saturation. Although better efficiency is obtained at 296kHz supporting 1V, 25A, higher frequency can be selected because less output ca meet the transient response specification.

1.2 RAA210925 Internal Block Diagram

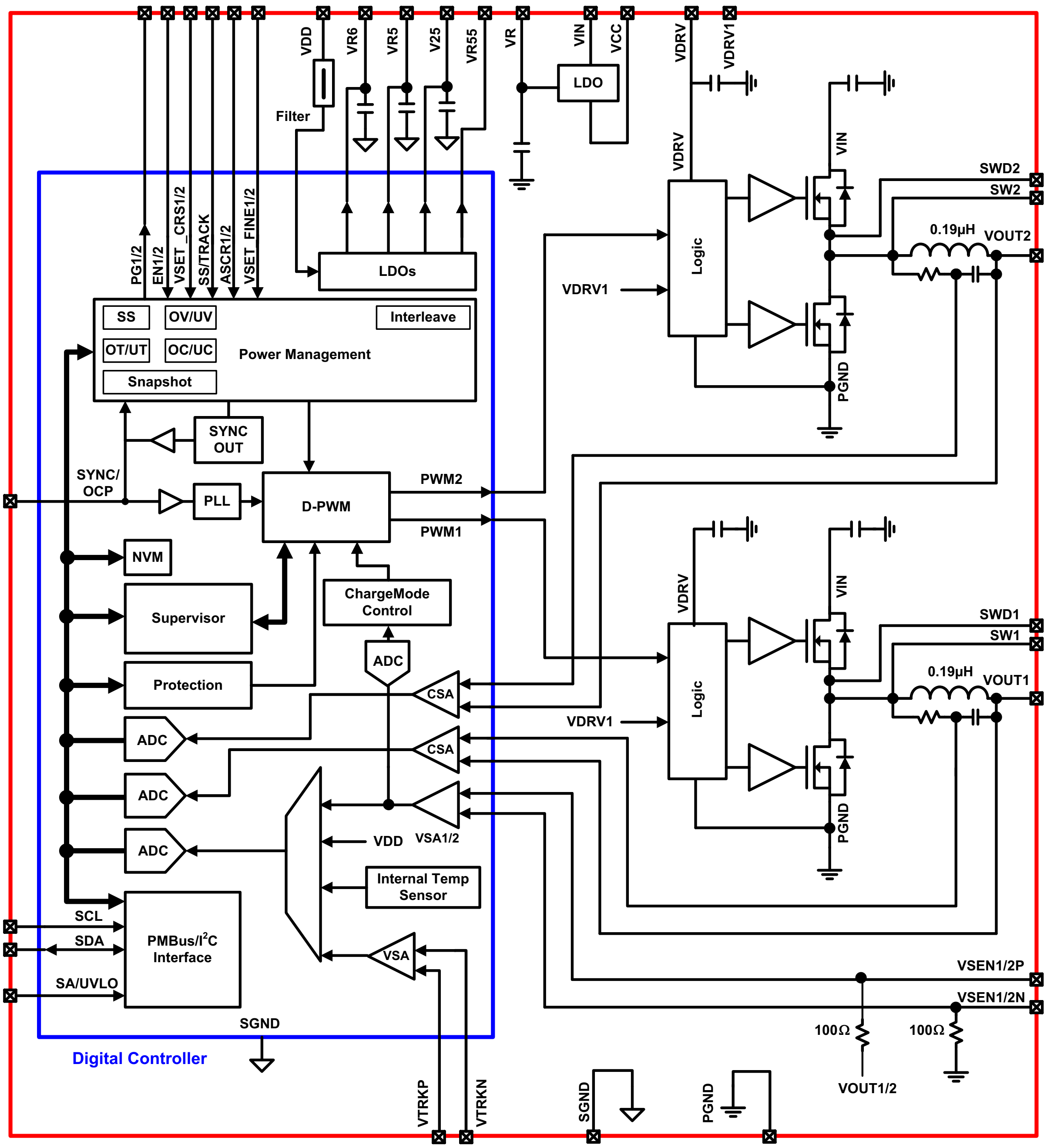


Figure 4. Internal Block Diagram

1.3 Ordering Information

Part Number (Notes 9, 10)	Part Marking	Temp Range (°C)	Tape and Reel (Units) (Note 8)	Package (RoHS Compliant)	Pkg. Dwg. #
RAA2109252GLG#AG0	RAA2109252	-40 to +85	-	58 Ld 18x23 HDA Module	Y58.18x23
RAA2109252GLG#HG0	RAA2109252	-40 to +85	100	58 Ld 18x23 HDA Module	Y58.18x23
RTKA2109252H00000BU	Evaluation Board				

Notes:

8. Refer to TB347 for details about reel specifications.
9. These Pb-free plastic packaged products are RoHS compliant by EU exemption 7C-I and 7A. They employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate-e4 termination finish, which is compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
10. For Moisture Sensitivity Level (MSL), see the RAA210925 device page. For more information about MSL, see TB363.

Table 2. Key Differences Between Family of Parts

Part Number	Description	V_{IN} Range (V)	V_{OUT} Range (V)	I_{OUT} (A)
RAA210925	25A/25A DC/DC dual channel Power Module	4.5 - 14	0.6 - 5	25/25
RAA210825	25A DC/DC single channel Power Module	4.5 - 14	0.6 - 5	25
RAA210833	33A DC/DC single channel Power Module	4.5 - 14	0.6 - 5	33
RAA210850	50A DC/DC single channel Power Module	4.5 - 14	0.6 - 5	50
RAA210870	70A DC/DC single channel Power Module	4.5 - 14	0.6 - 2.5	70

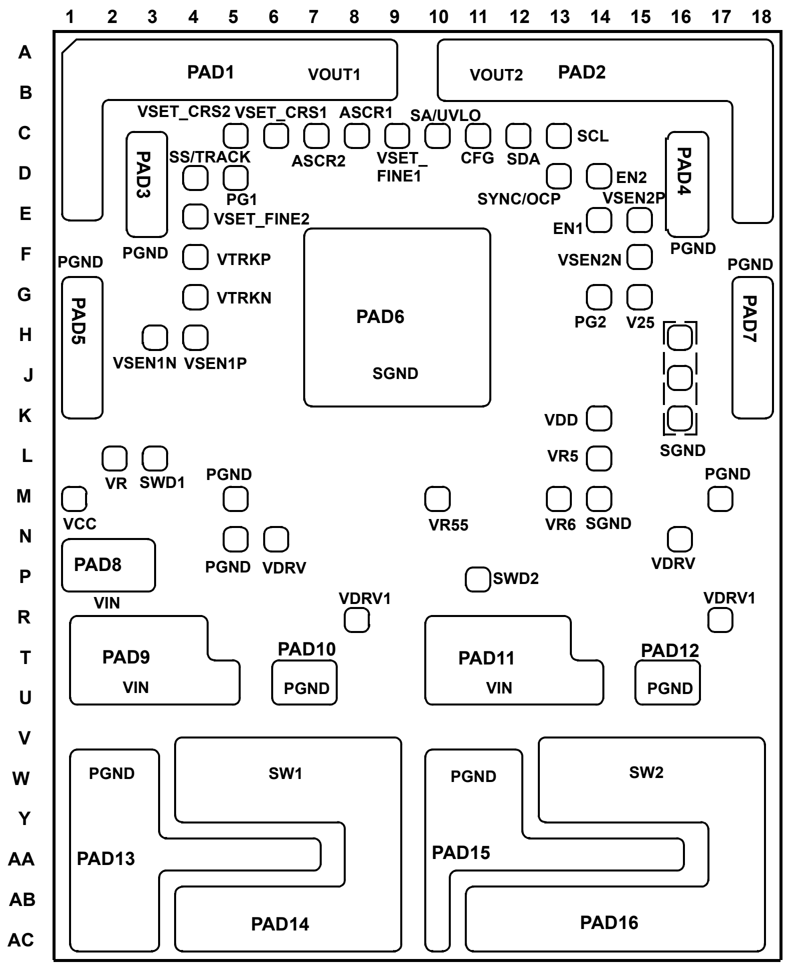
Table 3. Comparison of Simple Digital and Full Digital Parts

	ISL8274M	RAA210925
V_{IN} (V)	4.5 - 14	4.5 - 14
V_{OUT} (V)	0.6 - 5	0.6 - 5
I_{OUT} (Max) (A)	30/30	25/25
f_{SW} (kHz)	296 - 1067	296 - 1067
Digital PMBus Programmability for Configuration of Modules	All PMBus commands. NVM access to store module configuration	Configuration of modules supported by pin-strap resistors. Digital programmability supports configuration changes during run-time operation with a subset of PMBus commands. No NVM access to store module configuration
Power Navigator Support	Yes	Yes
SYNC Capability	Yes	Yes
Current Sharing Multi-Modules	No	No
DDC Pin (Inter-Device Communication)	Yes	No

Note: For a full comparison of all the RAA210XXX and ISL827XM product offerings please visit the simple-digital module family page.

1.4 Pin Configuration

58 Ld HDA
Top View



1.5 Pin Descriptions

Pin Number	Pin Name	Type	Description
PAD1	VOUT1	PWR	Power supply output voltage. Channel 1 provides an output voltage from 0.6V to 5V. Refer to the “Functional Description” on page 22 to set the maximum output current from these pads.
PAD2	VOUT2	PWR	Power supply output voltage. Channel 2 provides an output voltage from 0.6V to 5V. Refer to the “Functional Description” on page 22 to set the maximum output current from these pads.
PAD3, PAD4, PAD5, PAD7, PAD10, PAD12, PAD13, PAD15	PGND	PWR	Power ground. Refer to the “Layout Guide” on page 35 for the PGND pad connections and I/O capacitor placement.
PAD6	SGND	PWR	Signal ground. Refer to “Layout Guide” on page 35 for the SGND pad connections.
PAD8, PAD9, PAD11	VIN	PWR	Input power supply voltage to power the module. Input voltage ranges from 4.5V to 14V.
PAD14	SW1	PWR	Switching node pads for Channel 1. The SW1 pad dissipates the heat and provides good thermal performance. Refer to “Layout Guide” on page 35 for the SW1 pad connections.
PAD16	SW2	PWR	Switching node pads for Channel 2. The SW2 pad dissipates the heat and provides good thermal performance. Refer to “Layout Guide” on page 35 for the SW2 pad connections.
C5	VSET_CRS2	I	Output voltage selection pin for Channel 2. Sets the VOUT2 set point and VOUT2 max. Use VSET_FINE2 for fine-tuning.
C6	VSET_CRS1	I	Output voltage selection pin for Channel 1. Sets the VOUT1 set point and VOUT1 max. Use VSET_FINE1 for fine-tuning.
C7	ASCR2	I	ChargeMode control ASCR parameters selection pin for Channel 2. Sets ASCR gain and residual values.
C8	ASCR1	I	ChargeMode control ASCR parameters selection pin for Channel 1. Sets ASCR gain and residual values.
C9	VSET_FINE1	I	Output voltage fine-tuning. Provides increased VOUT1 resolution based on programmed VSET_CRS1 value.
C10	SA/UVLO	I	Serial address selection pin. Assigns unique address for each individual device or enables certain management features. This pin also sets the UVLO level.
C11	CFG	O	Clock source configuration. If the clock source is internal, set the internal FREQUENCY_SWITCH according to the SYNC pin resistor setting. If the clock source is external, the internal FREQUENCY_SWITCH is set according to the CFG pin resistor.
C12	SDA	I/O	Serial data. Connect to external host and/or to other Digital-DC™ devices. A pull-up resistor is required.
C13	SCL	I/O	Serial clock. Connect to external host and/or to other Digital-DC devices. A pull-up resistor is required.
D4	SS/ TRACK	I	Soft-start/stop selection pin. Sets the turn on/off delay and ramp time as well as tracking configuration.
D5	PG1	O	Power-good output for Channel 1. Power-good is configured as an open-drain output.
D13	SYNC/ OCP	I/O	Clock synchronization input and OCP setting pin. Sets the frequency of the internal switch clock, synchronizes to an external clock, or an output internal clock. If using external synchronization, the external clock must be active before enable. Different OCP levels can be set with this pin.
D14	EN2	I	Enable pin for Channel 2. Logic high to enable the module output.
E14	EN1	I	Enable pin for Channel 1. Logic high to enable the module output.
E4	VSET_FINE2	I/O	Output voltage fine-tuning. Provides increased VOUT2 resolution based on programmed VSET_CRS2 value.
E15	VSEN2P	I	Differential output voltage sense feedback for Channel 2. Connect to positive output regulation point.

Pin Number	Pin Name	Type	Description
F4	VTRKP	I	Tracking sense positive input. Tracks an external voltage source.
F15	VSEN2N	I	Differential output voltage sense feedback for Channel 2. Connect to negative output regulation point.
G4	VTRKN	I	Tracking sense negative input (return).
G14	PG2	O	Power-good output for Channel 2. Power-good is configured as an open-drain output.
G15	V25	PWR	Internal 2.5V reference that powers internal circuitry. No external capacitor required for this pin. Not recommended to power external circuits.
H3	VSEN1N	I	Differential output voltage sense feedback for Channel 1. Connect to a negative output regulation point.
H4	VSEN1P	I	Differential output voltage sense feedback for Channel 1. Connect to a positive output regulation point.
H16, J16, K16, M14	SGND	PWR	Signal grounds. Use multiple vias to connect the SGND pins to the internal SGND layer.
K14	VDD	PWR	Input supply voltage for controller. Connect VDD pad to VIN supply.
L2	VR	PWR	Internal LDO bias pin. Tie VR to VR55 directly with a short loop trace. Not recommended to power external circuits.
L3	SWD1	PWR	Switching node driving pins for Channel 1. Directly connect to the SW1 pad with short loop wires.
P11	SWD2	PWR	Switching node driving pins for Channel 2. Directly connect to the SW2 pad with short loop wires.
L14	VR5	PWR	Internal 5V reference that powers internal circuitry. Place a 10µF decoupling capacitor for this pin. Maximum external loading current is 5mA.
M1	VCC	PWR	Internal LDO output. Connect VCC to VDRV for internal LDO driving.
M5, M17, N5	PGND	PWR	Power grounds. Using multiple vias to connect the PGND pins to the internal PGND layer.
M10	VR55	PWR	Internal 5.5V bias voltage for internal LDO use only. Tie VR55 pin directly to the VR pin. Not recommended to power external circuits.
M13	VR6	PWR	Internal 6V reference that powers internal circuitry. Place a 10µF decoupling capacitor for this pin. Not recommended to power external circuits.
N6, N16	VDRV	PWR	Power supply for internal FET drivers. Connect a 10µF bypass capacitor to each of these pins. These pins can be driven by the internal LDO through the VCC pin or by the external power supply directly. Keep the driving voltage between 4.5V and 5.5V. For 5V input application, use external supply or connect this pin to VIN.
R8, R17	VDRV1	I	Bias pin of the internal FET drivers. Always tie to VDRV.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Input Supply Voltage, VIN Pin	-0.3	17	V
Input Supply Voltage for Controller, VDD Pin	-0.3	17	V
MOSFET Switch Node Voltage, SW1/2, SWD1/2 (Note 11)	-0.3	25	V
MOSFET Driver Supply Voltage, VDRV, VDRV1 Pin	-0.3	6.0	V
Output Voltage, VOUT1/2 Pin	-0.3	6.0	V
Internal Reference Supply Voltage			
VR6 Pin	-0.3	6.6	V
VR, VR5, VR55 Pin	-0.3	6.5	V
V25 Pin	-0.3	3	V
Logic I/O Voltage for EN1/2, PG1/2, ASCR1/2, SA/UVLO, SCL, SDA, SYNC/OCP, SS/TRACK, VSET_CRS1/2, VSET_FINE1/2	-0.3	6.0	V
Analog Input Voltages			
VSEN1P, VSEN2P, VTRKP	-0.3	6.0	V
VSEN1N, VSEN2N, VTRKN	-0.3	0.3	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2017)	2		kV
Machine Model (Tested per JESD22-A115C)	200		V
Charged Device Model (Tested per JS-002-2014)	750		V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100		mA

Note:

11. Do not apply DC voltage higher than 17V to the pins.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
58 Ld HDA Package (Notes 12, 13)	5.3	1.1

Notes:

12. θ_{JA} is defined by simulation in free air with the module mounted on an 8-layer evaluation board 4.7x4.8inch in size with 2oz Cu on all layers.
13. For θ_{JC}, the “case temp” location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature (Plastic Package)		+125	°C
Storage Temperature Range	-55	+150	°C
Pb-Free Reflow Profile	see Figure 33		

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Input Supply Voltage Range, V_{IN}	4.5	14	V
Input Supply Voltage Range for Controller, V_{DD}	4.5	14	V
Output Voltage Range, V_{OUT}	0.6	5	V
Output Current Range, $I_{OUT(DC)}$ Per Channel (Note 16)	0	25	A
Operating Junction Temperature Range, T_J	-40	+125	°C

2.4 Electrical Specifications

V_{IN} = V_{DD} = 12V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C.**

Parameter	Symbol	Test Conditions	Min (Note 14)	Typ	Max (Note 14)	Unit
Input and Supply Characteristics						
Input Supply Current for Controller	I_{DD}	V_{IN} = V_{DD} = 12V, V_{OUT} = 0V, module not enabled		40	**50**	mA
6V Internal Reference Supply Voltage	V_{R6}		**5.5**	6.1	**6.6**	V
5V Internal Reference Supply	V_{R5}	I_{VR5} < 5mA	**4.5**	5.2	**5.5**	V
2.5V Internal Reference Supply	V_{25}		**2.25**	2.5	**2.75**	V
Internal LDO Output Voltage	V_{CC}			5.3		V
Internal LDO Output Current	I_{VCC}	V_{IN} = V_{DD} = 12V, V_{CC} connected to VDRV, module enabled	**50**			mA
Input Supply Voltage for Controller Read Back Resolution	$V_{DD\_READ\_RES}$			±20		mV
Input Supply Voltage for Controller Read Back Total Error (Note 17)	$V_{DD\_READ\_ERR}$	PMBus read		±2		% FS
Output Characteristics						
Output Voltage Adjustment Range	V_{OUT_RANGE}		**0.54**		**5.5**	V
Output Voltage Set-Point Resolution	V_{OUT_RES}	Configured using PMBus		±0.025		$\%V_{OUT}$
Output Voltage Set-Point Accuracy (Notes 15, 17)	V_{OUT_ACCY}	Includes line, load, and temperature (-20°C ≤ T_A ≤ +85°C)	**-1.2**		**1.2**	%
Output Voltage Read Back Resolution	$V_{OUT\_READ\_RES}$			±0.15		% FS
Output Voltage Read Back Total Error (Note 17)	$V_{OUT\_READ\_ERR}$	PMBus read	**-2**		**2**	% FS
Output Current Range (Note 16)	I_{OUT_RANGE}	Per channel			**25**	A
Output Current Read Back Total Error	$I_{OUT\_READ\_ERR}$	PMBus read at max load V_{OUT} = 1.5V		±3		A
Soft-Start and Sequencing						
Delay Time from Enable to V_{OUT} Rise	t_{ON_DELAY}	Configured using pin-strap resistor or PMBus	**2**		**300**	ms
t_{ON_DELAY} Accuracy	$t_{ON\_DELAY\_ACCY}$			±2		ms

V_{IN} = V_{DD} = 12V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 14)	Typ	Max (Note 14)	Unit
Output Voltage Ramp-Up Time	t_{ON_RISE}	Configured using pin-strap resistor or PMBus	**0.5**		**120**	ms
Output Voltage Ramp-Up Time Accuracy	$t_{ON\_RISE\_ACCY}$			±250		µs
Delay Time from Disable to V_{OUT} Fall	t_{OFF_DELAY}	Configured using pin-strap resistor or PMBus	**2**		**300**	ms
t_{OFF_DELAY} Accuracy	$t_{OFF\_DELAY\_ACCY}$			±2		ms
Output Voltage Fall Time	t_{OFF_FALL}	Configured using pin-strap resistor or PMBus	**0.5**		**120**	ms
Output Voltage Fall Time Accuracy	$t_{ON\_FALL\_ACCY}$			±250		µs
Power-Good						
Power-Good Delay	V_{PG_DELAY}			3		ms
Temperature Sense						
Temperature Sense Range	T_{SENSE_RANGE}		**-50**		**150**	°C
Internal Temperature Sensor Accuracy	INT_TEMP_{ACCY}	Tested at +100°C	-5		5	°C
Fault Protection						
V_{DD} Undervoltage Threshold Range	$V_{DD\_UVLO\_RANGE}$	Measured internally	**4.18**		**16**	V
V_{DD} Undervoltage Threshold Accuracy (Note 17)	$V_{DD\_UVLO\_ACCY}$			±2		%FS
V_{DD} Undervoltage Response Time	$V_{DD\_UVLO\_DELAY}$			10		µs
V_{OUT} Overvoltage Threshold Range	$V_{OUT\_OV\_RANGE}$	Factory default		$1.15V_{OUT}$		V
		Configured using pin-strap resistor or PMBus	**$1.05V_{OUT}$**		**V_{OUT_MAX}**	V
V_{OUT} Undervoltage Threshold Range	$V_{OUT\_UV\_RANGE}$	Factory default		$0.85V_{OUT}$		V
		Configured using pin-strap resistor or PMBus	**0**		**$0.95V_{OUT}$**	V
V_{OUT} OV/UV Threshold Accuracy (Note 15)	V_{OUT_OV/UV_ACCY}		**-2**		**2**	%
V_{OUT} OV/UV Response Time	V_{OUT_OV/UV_DELAY}			10		µs
Output Current Limit Set-Point Accuracy (Note 17)	I_{LIMIT_ACCY}	Tested at IOUT_AVG_OC_FAULT_LIMIT = 35A		±10		% FS
Over-temperature Protection Threshold (Controller Junction Temperature)	$T_{JUNCTION}$	Factory default		115		°C
		Configured using PMBus	**-40**		**115**	°C
Thermal Protection Hysteresis	$T_{JUNCTION\_HYS}$			15		°C
Oscillator and Switching Characteristics						
Switching Frequency Range	f_{SW_RANGE}		**296**		**1067**	kHz
Switching Frequency Set-Point Accuracy	f_{SW_ACCY}		**-5**		**5**	%

V_{IN} = V_{DD} = 12V, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +85°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 14)	Typ	Max (Note 14)	Unit
Minimum Pulse Width Required from External SYNC Clock	EXT_SYNC_{PW}	Measured at 50% amplitude	**150**			ns
Drift Tolerance for External SYNC Clock	EXT_SYNC_{DRIFT}	External SYNC clock equal to 500kHz is not supported	**-10**		**10**	%
Logic Input/Output Characteristics						
Bias Current at the Logic Input Pins	I_{LOGIC_BIAS}	EN1/2, PG1/2, SA/UVLO, SCL, SDA, ASCR1/2, SS/TRACK, SYNC/OCP, VSET_CRS1/2, VSET_FINE1/2	**-100**		**+100**	nA
Logic Input Low Threshold Voltage	$V_{LOGIC\_IN\_LOW}$				**0.8**	V
Logic Input High Threshold Voltage	$V_{LOGIC\_IN\_HIGH}$		**2.0**			V
Logic Output Low Threshold Voltage	$V_{LOGIC\_OUT\_LOW}$	2mA sinking			**0.5**	V
Logic Output High Threshold Voltage	$V_{LOGIC\_OUT\_HIGH}$	2mA sourcing	**2.25**			V
PMBus Interface Timing Characteristic						
PMBus Operating Frequency	f_{SMB}		**100**		**400**	kHz

Notes:

14. Compliance to datasheet limits is assured by one or more methods: Production test, characterization, and/or design. Controller is independently tested before module assembly.
15. V_{OUT} measured at the termination of the VSEN1/2P and VSEN1/2N sense points.
16. The MAX load current is determined by the thermal "Derating Curves" on page 19.
17. "FS" stands for full scale of recommended maximum operation range.

3. Typical Performance Curves

3.1 Efficiency Performance

Operating condition: T_A = +25°C, no air flow. C_{OUT} = 1 x 470µF POSCAP + 12 x 100µF Ceramic. Typical values are used unless otherwise noted. The efficiency curves were measured on the evaluation board. For test conditions, refer to Table 1 on page 6.

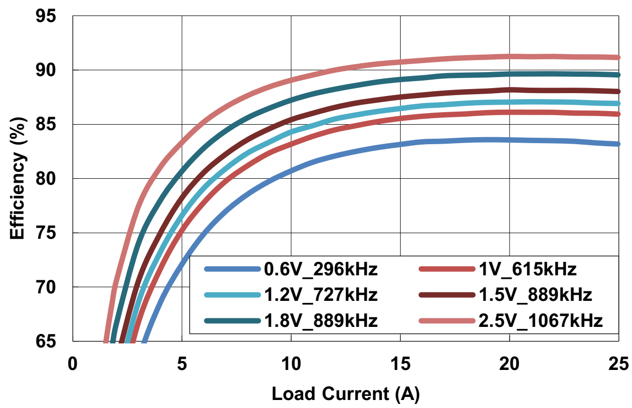


Figure 5. Single Channel Efficiency vs Output Current

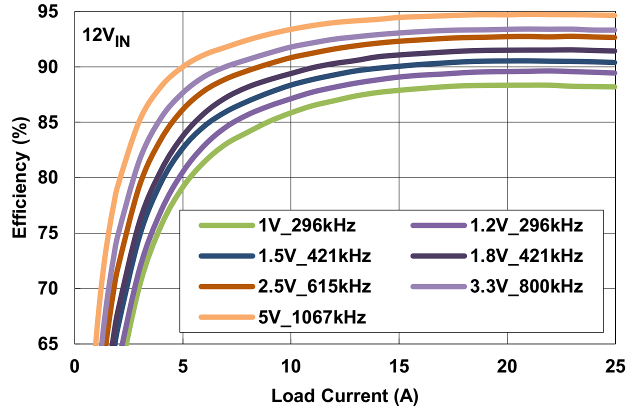


Figure 6. Single Channel Efficiency vs Output Current

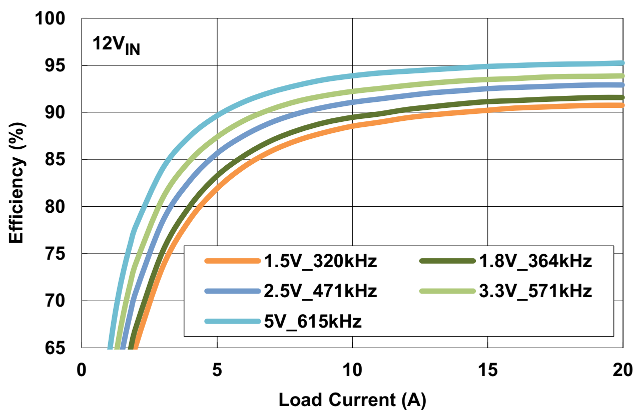


Figure 7. Single Channel Efficiency vs Output Current

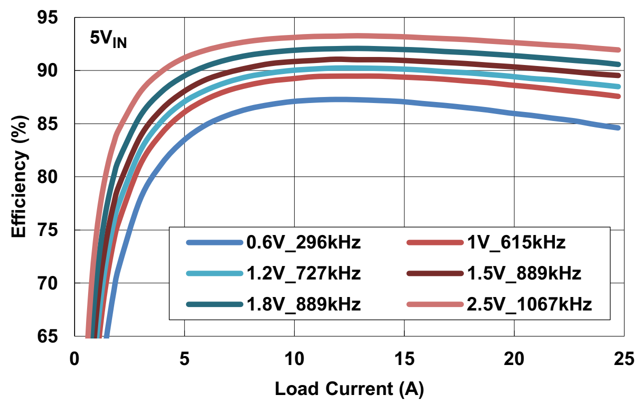


Figure 8. Single Channel Efficiency vs Output Current

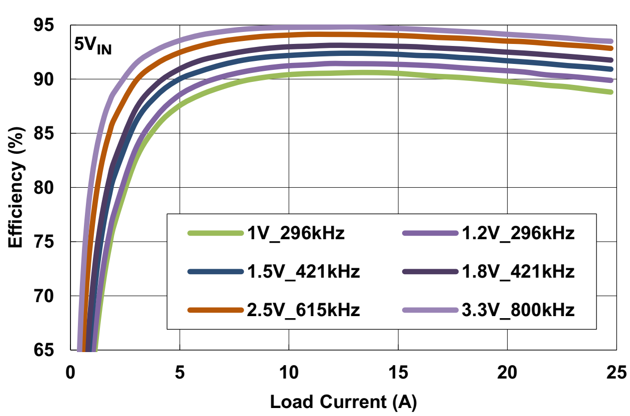


Figure 9. Single Channel Efficiency vs Output Current

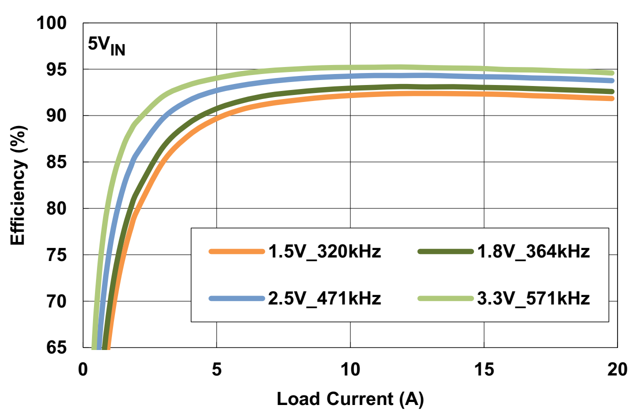


Figure 10. Single Channel Efficiency vs Output Current

3.2 Startup and Shutdown

Operating condition: T_A = +25°C, no air flow. C_{OUT} = 1 x 470µF POSCAP + 12 x 100µF Ceramic. Typical values are used unless otherwise noted.

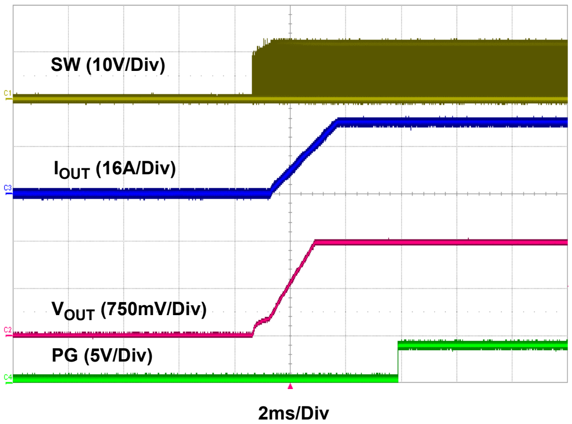


Figure 11. Single Channel Startup 12V_{IN}, 1.5V_{OUT}, 25A

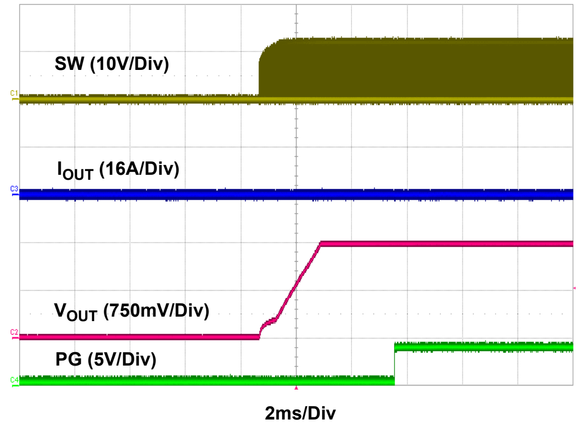


Figure 12. Single Channel Startup 12V_{IN}, 1.5V_{OUT}, 0A

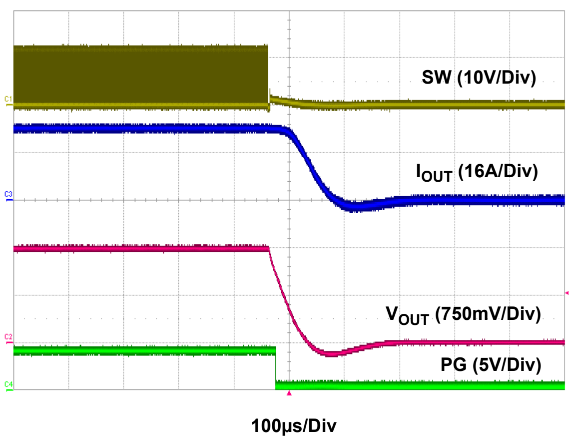


Figure 13. Single Channel Shutdown 12V_{IN}, 1.5V_{OUT}, 25A

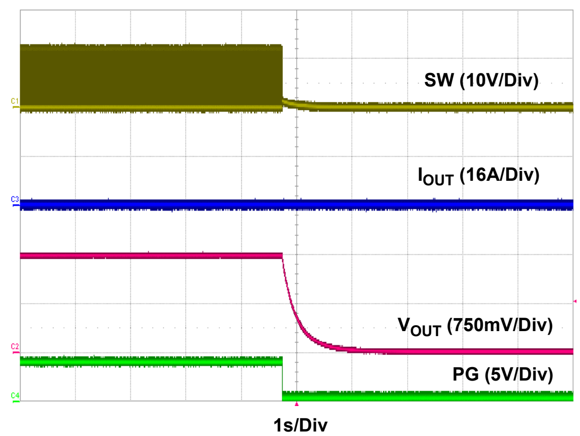


Figure 14. Single Channel Shutdown 12V_{IN}, 1.5V_{OUT}, 0A

3.3 Derating Curves

All of the following curves were plotted at T_J = +125°C. The derating curves were measured on the evaluation board. For test conditions, refer to Table 1 on page 6. Load current is applied per channel, two channels are operating at the same time.

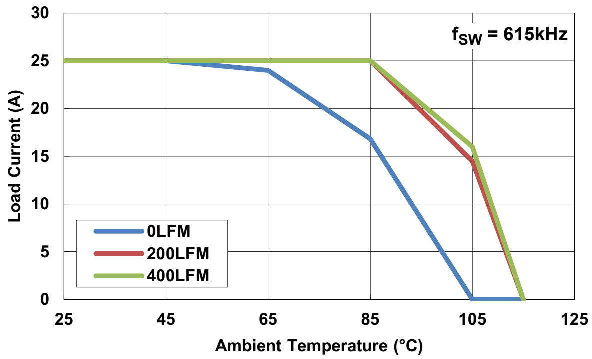


Figure 15. 12V_{IN} to 1V_{OUT}

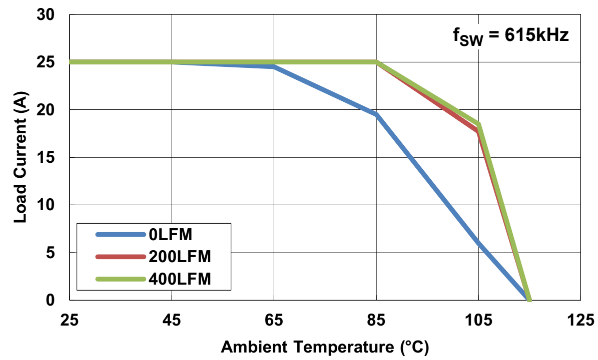


Figure 16. 5V_{IN} to 1V_{OUT}

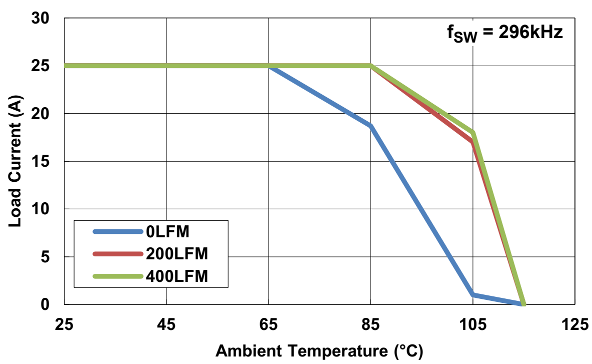


Figure 17. 12V_{IN} to 1V_{OUT}

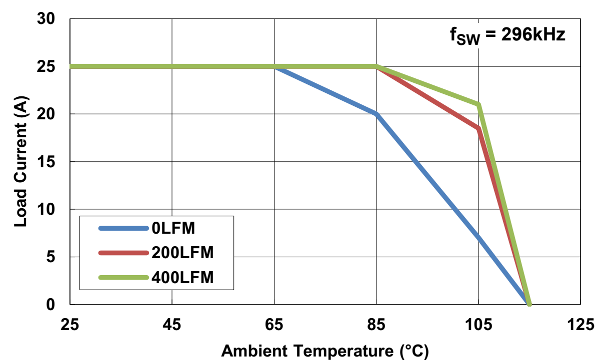


Figure 18. 5V_{IN} to 1V_{OUT}

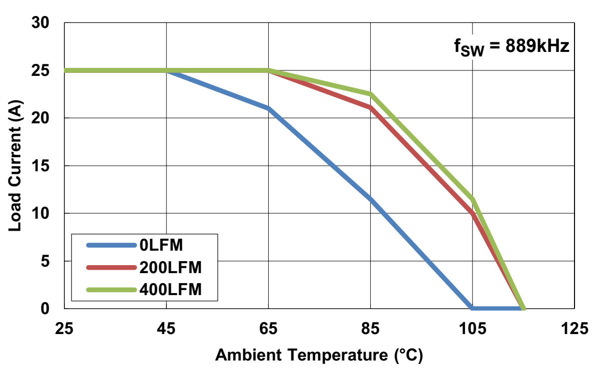


Figure 19. 12V_{IN} to 1.5V_{OUT}

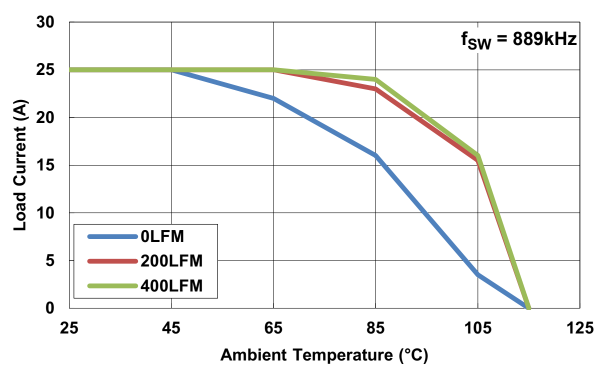


Figure 20. 5V_{IN} to 1.5V_{OUT}

All of the following curves were plotted at T_J = +125°C. The derating curves were measured on the evaluation board. For test conditions, refer to Table 1 on page 6. Load current is applied per channel, two channels are operating at the same time. **(Continued)**

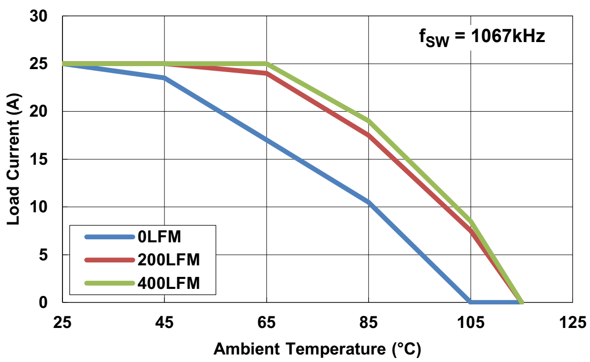


Figure 21. $12V_{IN}$ to $2.5V_{OUT}$

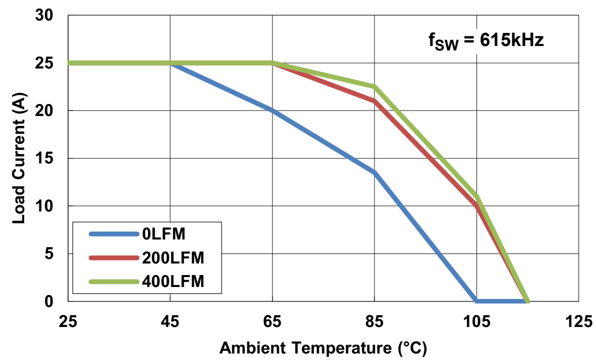


Figure 22. $5V_{IN}$ to $2.5V_{OUT}$

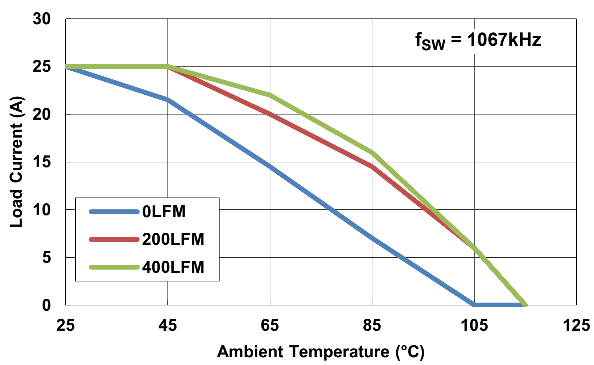


Figure 23. $12V_{IN}$ to $5V_{OUT}$

3.4 Transient Response Performance

Operating condition: T_A = +25°C, no air flow. Refer to Table 1 on page 6 for output capacitor and ASCR settings. Typical values are used unless otherwise noted.

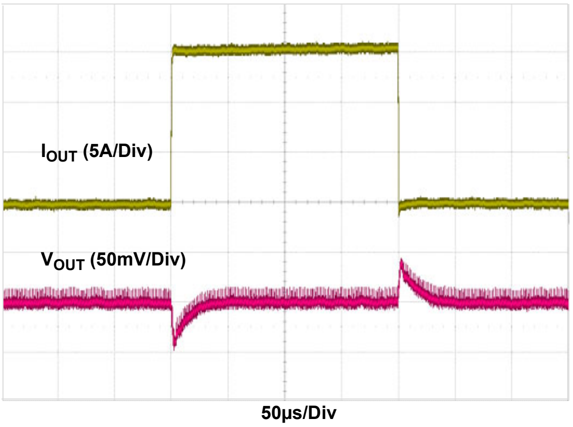


Figure 24. 0A-15A, 15A/µs, $12V_{IN}$,$1V_{OUT}$, 615kHz

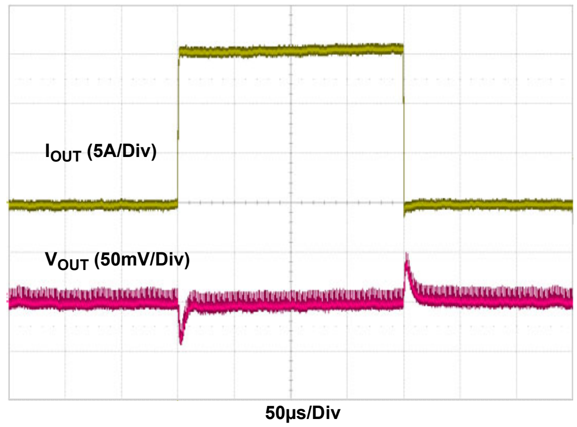


Figure 25. 0A-15A, 15A/µs, $12V_{IN}$,$1.5V_{OUT}$, 889kHz

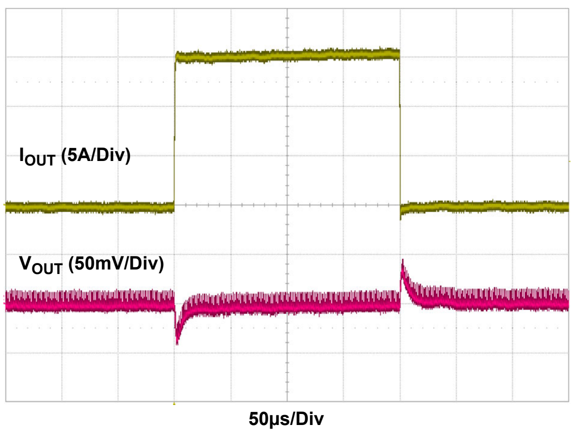


Figure 26. 0A-15A, 15A/µs, $12V_{IN}$,$1.8V_{OUT}$, 889kHz

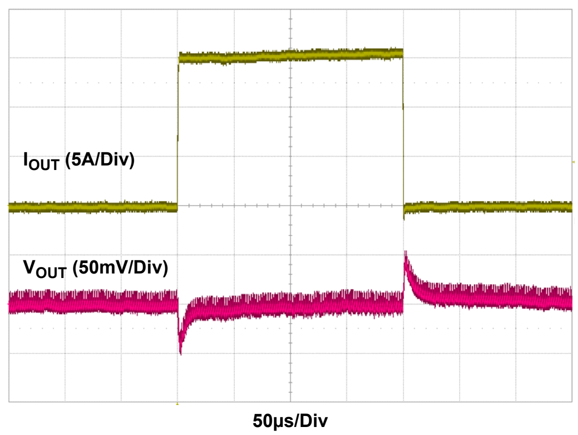


Figure 27. 0A-15A, 15A/µs, $12V_{IN}$, $2.5V_{OUT}$, 1067kHz

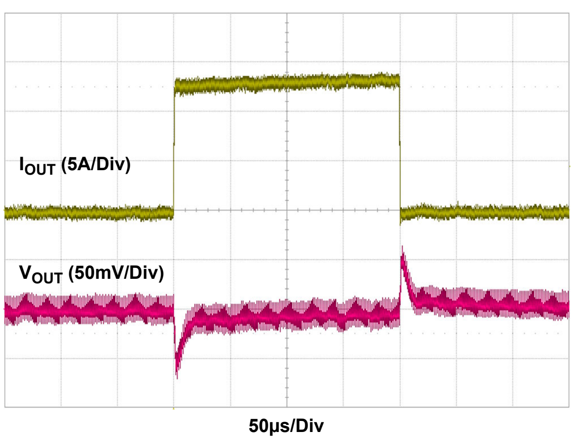


Figure 28. 0A-12.5A, 15A/µs, $12V_{IN}$, $3.3V_{OUT}$, 800kHz

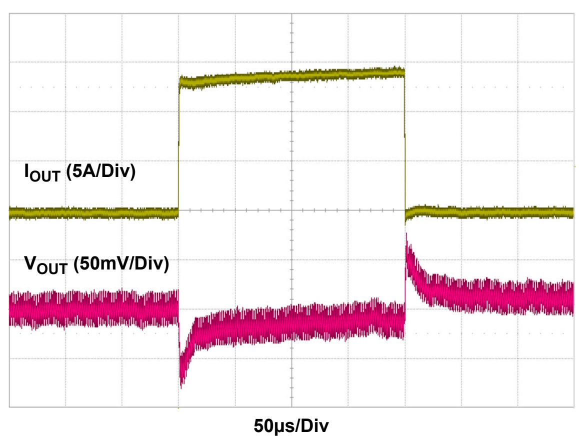


Figure 29. 0A-12.5A, 15A/µs, $12V_{IN}$, $5V_{OUT}$, 1067kHz

4. Functional Description

4.1 SMBus Communications

The RAA210925 provides a SMBus digital interface that enables the user to configure the module operation as well as monitor the input and output parameters. The RAA210925 can be used with any SMBus host device. In addition, the module is compatible with PMBus Power System Management Protocol Specification Parts I and II version 1.2. The RAA210925 accepts most standard PMBus commands. When configuring the device using PMBus commands, it is recommended that the enable pin is tied to SGND.

The SMBus device address is the only parameter that must be set by the external pins.

The RAA210925 can operate without the PMBus in pin-strap mode with configurations programmed by pin-strap resistors, such as output voltage, ASCR setting, switching frequency, OCP limit, device SMBus address, input UVLO, soft-start/stop, and tracking.

4.2 Output Voltage Selection

The output voltages of both channels may be set to a voltage between 0.6V and 5V if the input voltage is higher than the desired output voltage by an amount sufficient to maintain regulation.

The VSET_CRS1/2 (V_{OUT} Coarse) and VSET_FINE1/2 (V_{OUT} Fine) pins set the output voltage. A standard 1% resistor is required. Placing a resistor between VCRS1/2 and SGND based on Table 4 determines the VCRS value.

If higher resolution is desired, the VSET_FINE pin can be used to fine-tune the output voltage settings according to the following command set:

$$\text{VOUT\_COMMAND} = \begin{cases} \text{VOUT\_CRS} + 5\text{mV} \cdot \text{N, if } 0.6\text{V} \le \text{VOUT\_CRS} < 1.4\text{V} \\ \text{VOUT\_CRS} + 10\text{mV} \cdot \text{N, if } 1.4\text{V} \le \text{VOUT\_CRS} < 2\text{V} \\ \text{VOUT\_CRS} + 50\text{mV} \cdot \text{N, if } 2\text{V} \le \text{VOUT\_CRS} < 3.6\text{V} \\ \text{VOUT\_CRS} + 100\text{mV} \cdot \text{N, if } 3.6\text{V} \le \text{VOUT\_CRS} < 5\text{V} \\ \text{VOUT\_CRS, if VOUT\_CRS} = 5\text{V} \end{cases}$$

Use the resistors values from Table 5 on page 23 to set the appropriate value of N for calculating the final output voltage.

Table 4. Output Voltage Resistor Settings

VOUT_CRS1/2 (V)	RSET1/2 (kΩ)
1	LOW
1.5	OPEN
3.3	HIGH
0.6	10
0.675	11
0.7	12.1
0.72	13.3
0.75	14.7
0.8	16.2
0.85	17.8
0.9	19.6
0.93	21.5
0.95	23.7
0.98	26.1
1.03	28.7

Table 4. Output Voltage Resistor Settings (Continued)

VOUT_CRS1/2 (V)	RSET1/2 (kΩ)
1.05	31.6
1.1	34.8
1.12	38.3
1.15	42.2
1.2	46.4
1.25	51.1
1.3	56.2
1.35	61.9
1.4	68.1
1.65	75
1.8	82.5
1.85	90.9
2	100
2.4	110
2.5	121
2.8	133
3	147
3.6	162
5	178

Table 5. VSET_FINE Settings

N	RSET1/2 (kΩ)
0	10, or OPEN
1	11
2	12.1
3	13.3
4	14.7
5	16.2
6	17.8
7	19.6
8	21.5
9	23.7, or connect to SGND
10	26.1
11	28.7
12	31.6
13	34.8
14	38.3
15	42.2
16	46.4
17	51.1
18	56.2

Table 5. VSET_FINE Settings (Continued)

N	RSET1/2 (kΩ)
19	61.9
20	68.1, or connect to V25

The output voltage may also be set to any value between 0.6V and 5V using the PMBus command VOUT_COMMAND.

By default, V_{OUT_MAX} is set to 110% of V_{OUT} set by the pin-strap resistor, which can be changed to any value up to 5.5V by the PMBus Command VOUT_MAX.

4.3 Soft-Start, Stop Delay, and Ramp Times

The RAA210925 follows an internal start-up procedure after power is applied to the VDD pin. The module requires approximately 60ms to 70ms to check for specific values stored in its internal memory and programmed by pin-strap resistors. When this process is completed, the device is ready to accept commands through the PMBus interface and the module is ready to be enabled. If the module is to be synchronized to an external clock source, the clock frequency must be stable before asserting the EN pin.

It may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features can be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The RAA210925 gives the system designer several options for precisely and independently controlling both the delay and ramp time periods. The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires.

The soft-start delay (TON_DELAY) and ramp-up time (TON_RISE) can be set to custom values with pin-strap resistors or PMBus. When the delay time is set to 0ms, the device begins its ramp-up after the internal circuitry has initialized (approximately 2ms). When the soft-start ramp period is set to 0ms, the output ramps up as quickly as the output load capacitance and loop settings allow. It is generally recommended to set the soft-start ramp to a value greater than 2ms to prevent inadvertent fault conditions due to excessive inrush current.

Similar to the soft-start delay and ramp-up time, the delay (TOFF_DELAY) and ramp-down time (TOFF_FALL) for soft-stop/off can be set to custom values with pin-strap resistors or PMBus. In addition, the module can be configured as “immediate off” using the command ON_OFF_CONFIG, so that the internal MOSFETs are turned off immediately after the delay time expires.

The SS/TRACK pin can be used to program the soft-start/stop delay time and ramp time to some typical values as well as enable/disable the tracking function shown in Table 6 on page 24.

Table 6. Soft-Start/Stop and Tracking Resistor Settings

TON_DELAY TOFF_DELAY (ms)		TON_RISE TOFF_FALL (ms)		Tracking		R (kΩ)
Ch1	Ch2	Ch1	Ch2	Ch1	Ch2	
5	5	2	2	No	No	LOW
5	5	2	5	No	No	OPEN
5	5	5	2	No	No	HIGH
5	5	5	5	No	No	10
5	10	2	2	No	No	11
5	10	2	5	No	No	12.1
5	10	5	2	No	No	13.3
5	10	5	5	No	No	14.7
10	5	2	2	No	No	16.2

Table 6. Soft-Start/Stop and Tracking Resistor Settings (Continued)

TON_DELAY TOFF_DELAY (ms)		TON_RISE TOFF_FALL (ms)		Tracking		
Ch1	Ch2	Ch1	Ch2	Ch1	Ch2	R (kΩ)
10	5	2	5	No	No	17.8
10	5	5	2	No	No	19.6
10	5	5	5	No	No	21.5
20	5	2	2	No	No	23.7
20	5	5	5	No	No	26.1
5	20	2	2	No	No	28.7
5	20	2	5	No	No	31.6
5	20	5	2	No	No	34.8
5	20	5	5	No	No	38.3
5	N/A	2	N/A	No	Track 100%	42.2
5	N/A	2	N/A	No	Track 50%	46.4
5	N/A	5	N/A	No	Track 100%	51.1
5	N/A	5	N/A	No	Track 50%	56.2
10	N/A	2	N/A	No	Track 100%	61.9
10	N/A	2	N/A	No	Track 50%	68.1
10	N/A	5	N/A	No	Track 100%	75
10	N/A	5	N/A	No	Track 50%	82.5
N/A	5	N/A	2	Track 100%	No	90.9
N/A	5	N/A	2	Track 50%	No	100
N/A	5	N/A	5	Track 100%	No	110
N/A	5	N/A	5	Track 50%	No	121
N/A	10	N/A	2	Track 100%	No	133
N/A	10	N/A	2	Track 50%	No	147
N/A	10	N/A	5	Track 100%	No	162
N/A	10	N/A	5	Track 50%	No	178

4.4 Voltage Tracking

Numerous high performance systems place stringent demands on the order in which the power supply voltages are turned on. This is particularly true when powering FPGAs, ASICs, and other advanced processor devices that require multiple supply voltages to power a single die. In most cases, the I/O interface operates at a higher voltage than the core and therefore, the core supply voltage must not exceed the I/O supply voltage according to the manufacturers' specifications.

The RAA210925 integrates a tracking scheme that allows one of its outputs (Channel 1 or Channel 2) to track a voltage that is applied to the VTRKP and VTRKN pins with no external components required. The VTRKP and VTRKN pins are analog inputs that, when the tracking mode is enabled, configure the voltage applied to the VTRKP and VTRKN pins to act as a reference for the device's output regulation.

Figure 30 illustrates the typical connection and the two tracking modes:

- Coincident - This mode configures the RAA210925 to ramp its output voltage at the same rate as the voltage applied to the VTRK pin until it reaches its desired output voltage. The device that is tracking another output voltage (slave) must be set to its desired steady-state output voltage.
- Ratiometric - This mode configures the RAA210925 to ramp its output voltage at a rate that is a percentage of the voltage applied to the VTRKP and VTRKN pins. The device that is tracking another output voltage (slave) must be set to its desired steady-state output voltage.

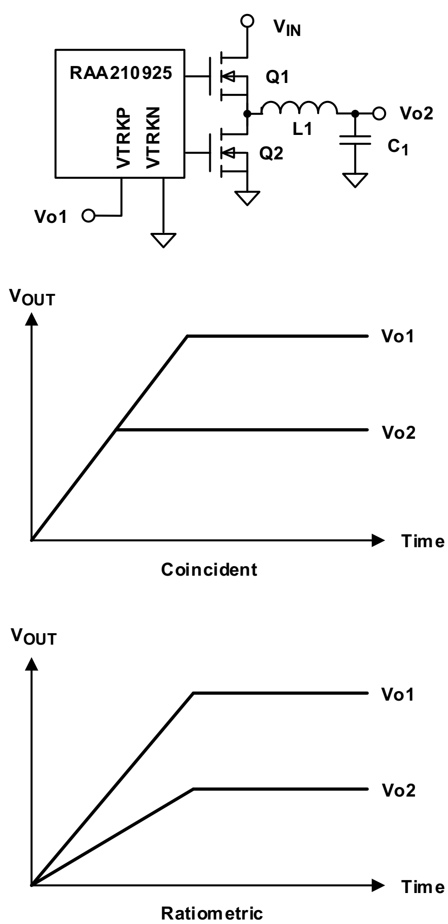


Figure 30. Tracking Modes

The master RAA210925 device in a tracking group is defined as the device that has the highest target output voltage within the group. This master device controls the ramp rate of all tracking devices and is not configured for tracking mode. The maximum tracking rise time is 1V/ms. The slave device must be enabled before the master.

Any device that is configured for tracking mode ignores its TON_DELAY and TON_RISE settings and its output takes on the turn-on/turn-off characteristics of the reference voltage present at the VTRKP and VTRKN pins.

The VOUT_COMMAND needs to be set the same as the target tracking voltage when tracking is enabled. For example, the VOUT_COMMAND of the Page1 (VOUT2 which enables the tracking) needs to set to 1V if tracking 100% is selected and a ramp of 1V is applied to VTRKP and VTRKN. The VOUT_COMMAND of Page 1 (VOUT2 which enables the tracking) needs to set to 1V if tracking 50% is selected and a ramp of 2V is applied to VTRKP and VTRKN. In Tracking mode, the minimum voltage that can be tracked is ~200mV.

4.5 Power-Good

The RAA210925 provides a Power-Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin asserts if the output is within 10% of the target voltage. This limit may be changed using the PMBus command POWER_GOOD_ON.

A PG delay period is defined as the time from when all conditions within the RAA210925 for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. A fixed PG delay of 3ms is programmed for the RAA210925.

4.6 Switching Frequency and PLL

The device’s switching frequency is set from 296kHz to 1067kHz using the pin-strap method (combined with the average OCP limit setting) as shown in Table 7, or by using the PMBus command FREQUENCY_SWITCH.

Table 7. Switching Frequency and OCP Limit Resistor Setting

Switching Frequency		OCP Avg	
R (kΩ)	f_{SW} (kHz)	Ch1 (A)	Ch2 (A)
LOW	296	35	35
OPEN	889	35	35
HIGH	1067	35	35
10	296	30	35
11	296	30	30
12.1	296	25	35
13.3	296	25	30
14.7	296	25	25
16.2	320	25	35
17.8	320	25	30
19.6	320	25	25
21.5	320	20	30
23.7	320	20	25
26.1	364	25	35
28.7	364	25	30
31.6	364	20	30
34.8	421	30	35
38.3	421	30	30
42.2	471	25	35
46.4	471	25	30
51.1	471	20	35
56.2	571	25	35

Table 7. Switching Frequency and OCP Limit Resistor Setting (Continued)

Switching Frequency		OCP Avg	
R (kΩ)	f_{SW} (kHz)	Ch1 (A)	Ch2 (A)
61.9	571	25	30
68.1	571	20	35
75	571	20	30
82.5	615	35	35
90.9	615	35	30
100	615	30	30
110	615	25	35
121	615	25	30
133	615	25	25
147	727	35	35
162	800	30	35
178	800	30	30

The RAA210925 incorporates an internal Phase-Locked Loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. This configuration can be achieved by connecting a resistor to the CFG pin. If the clock source is set to internal, the internal frequency is set according to the SYNC pin resistor settings. If the clock source is programmed to external, the internal frequency is set according to the resistor connected to the CFG pin as shown in Table 8. The external clock signal must not vary more than 10% from its initial value and should have a minimum pulse width of 150ns. For the external clock source, OCP AVG is 25A for CH1 and CH2, which is not adjustable.

Table 8. External Frequency SYNC Settings

Clock Source	Internal FREQUENCY_SWITCH (kHz)	R_{SET} (kΩ)
Internal	Determined by SYNC resistor	10, or OPEN
External	296	11
External	340	12.1
External	390	13.3
External	444	14.7
External	516	16.2, or connect to SGND
External	593	17.8
External	696	19.6
External	800	21.5
External	941	23.7
External	1067	26.1, or connect to V25

4.7 Output Overcurrent Protection

The RAA210925 is protected from damage if the output is shorted to ground or if an overload condition is imposed on the output. Average output overcurrent fault threshold can be programmed by the PMBus command IOUT_AVG_OC_FAULT_LIMIT while the peak output overcurrent fault threshold can be programmed by the PMBus command IOUT_OC_FAULT_LIMIT. The default response from an average overcurrent fault is an immediate shutdown with a continuous retry of 70ms delay. A hard bound of 50A is applied to the peak overcurrent limit.

The average OCP limit can be set by the SYNC/OCP pin strap. Refer to Table 7 on page 27 for more information.

4.8 Loop Compensation

The module loop response can be set by using the pin-strap method (ASCR1/2 pins) according to Table 9 or through the PMBus command ASCR_CONFIG. The RAA210925 uses the ChargeMode control algorithm that responds to the output current changes within a single PWM switching cycle, achieving a smaller total output voltage variation with less output capacitance than traditional PWM controllers.

Table 9. ASCR Resistor Setting

ASCR Gain	ASCR Residual	R (kΩ)
350	110	LOW
525	90	OPEN
475	80	HIGH
100	90	10
100	100	11
120	90	12.1
120	100	13.3
140	90	14.7
140	100	16.2
140	110	17.8
150	90	19.6
150	100	21.5
160	70	23.7
160	90	26.1
175	80	28.7
175	90	31.6
200	90	34.8
200	100	38.3
200	110	42.2
225	80	46.4
225	90	51.1
250	80	56.2
250	100	61.9
275	90	68.1
275	100	75
300	70	82.5
300	90	90.9
350	100	100

Table 9. ASCR Resistor Setting (Continued)

ASCR Gain	ASCR Residual	R (kΩ)
450	100	110
450	110	121
500	70	133
500	90	147
600	100	162
600	110	178

4.9 SMBus Module Address Selection

Each module must have its own unique serial address to distinguish between other devices on the bus. The module address is set by connecting a resistor between pins SA/UVLO and SGND. The SA/UVLO pin also defines the input undervoltage lockout limit. The input Undervoltge Lockout (UVLO) prevents the RAA210925 from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The UVLO threshold (V_{UVLO}) can be set between 4.18V and 16V by using the PMBus command VIN_UV_FAULT_LIMIT.

Table 10 lists the available module addresses. A standard 1% resistor is required. When the UVLO threshold is hit, the module shuts down immediately. The fault needs to be cleared for the module to restart.

Table 10. SMBus Address and UVLO Resistor Setting

PMBus Address	UVLO (V)	R (kΩ)
26h	4.2	LOW
28h	4.5	OPEN
19h	10.8	10
1Ah	10.8	11
1Bh	10.8	12.1
1Ch	10.8	13.3
1Dh	10.8	14.7
1Eh	10.8	16.2
1Fh	10.8	17.8
20h	4.2	19.6
21h	4.2	21.5
22h	4.2	23.7
23h	4.2	26.1
24h	4.2	28.7
25h	4.2	31.6
26h	4.2	34.8
27h	4.2	38.3
28h	4.5	42.2
29h	4.5	46.4
2Ah	4.5	51.1
2Bh	4.5	56.2
2Ch	4.5	61.9
2Dh	4.5	68.1
2Eh	4.5	75

Table 10. SMBus Address and UVLO Resistor Setting (Continued)

PMBus Address	UVLO (V)	R (kΩ)
2Fh	4.5	82.5
30h	10.8	90.9
31h	10.8	100
32h	10.8	110
33h	10.8	121
34h	10.8	133
35h	10.8	147
36h	10.8	162
37h	10.8	178

4.10 Output Overvoltage Protection

The RAA210925 offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator compares the actual output voltage (seen at pins VSEN1/2P, VSEN1/2N) to a threshold set to 15% higher than the target output voltage (default setting). The fault threshold can be set to a desired level by the PMBus command VOUT_OV_FAULT_LIMIT. If the VSEN1/2P, VSEN1/2N voltage exceeds this threshold, the module initiates an immediate shutdown without retry.

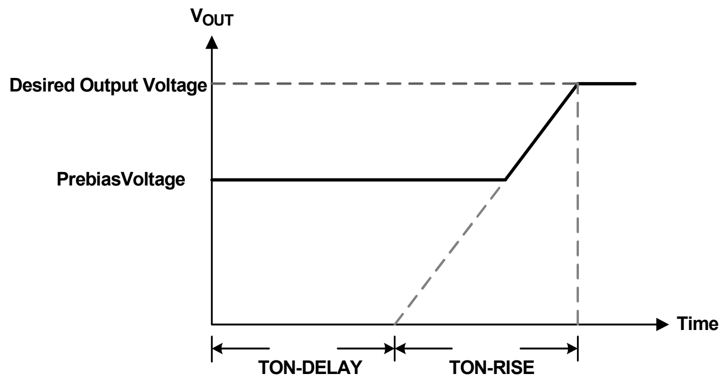
Internal to the module, two 100Ω resistors are populated from V_{OUT} to VSEN1/2P and SGND to VSEN1/2N to protect the module from overvoltage conditions in case of open at the voltage sensing pins and differential remote sense traces due to assembly error. As long as differential remote sense traces have low resistance, V_{OUT} regulation accuracy is not compromised.

4.11 Output Prebias Protection

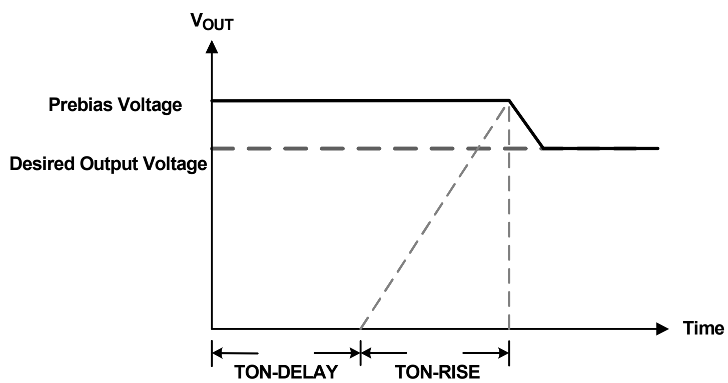
An output prebias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start-up if a prebias condition exists at the output. The RAA210925 provides prebias protection by sampling the output voltage before initiating an output ramp.

If a prebias voltage lower than the target voltage exists after the preconfigured delay period has expired, the target voltage is set to match the existing prebias voltage and both drivers are enabled. The output voltage is then ramped to the final regulation value at the preconfigured ramp rate.

The actual time the output takes to ramp from the prebias voltage to the target voltage varies, depending on the prebias voltage. However, the total time elapsed from when the delay period expires to when the output reaches its target value matches the preconfigured ramp time (see Figure 31 on page 32).



$V_{PREBIAS} < V_{TARGET}$



$V_{PREBIAS} > V_{TARGET}$

Figure 31. Output Responses to Prebias Voltages

If a prebias voltage is higher than the target voltage after the preconfigured delay period has expired, the target voltage is set to match the existing prebias voltage. Thus, both drivers are enabled with a PWM duty cycle that would ideally create the prebias voltage.

When the preconfigured soft-start ramp period has expired, the PG pin is asserted (assuming the prebias voltage is not higher than the overvoltage limit). The PWM then adjusts its duty cycle to match the original target voltage and the output ramps down to the preconfigured output voltage.

If a prebias voltage is higher than the overvoltage limit, the device does not initiate a turn-on sequence and declares an overvoltage fault condition.

4.12 Thermal Overload Protection

The RAA210925 includes a thermal sensor that continuously measures the internal temperature of the module and shuts down the controller when the temperature exceeds the preset limit. The factory default temperature limit is set to +115°C, and can be changed using the PMBus command OT_FAULT_LIMIT. Note that the temperature reading from the PMBus command is the temperature of the internal controller, which is lower than the junction temperature of the module.

The default response from an over-temperature fault is an immediate shutdown without retry.

4.13 Phase Spreading

When multiple point-of-load converters share a common DC input supply, adjust the clock phase offset of each device so that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Because the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced, and the power losses proportional to the I_{RMS}^2 are reduced dramatically.

To enable phase spreading, all converters must be synchronized to the same switching clock. The phase offset of each device can also be set to any value between 0° and 360° in 22.5° increments by setting the device address appropriately as shown in Table 11. This functionality can also be accessed using the PMBus command INTERLEAVE. The internal two phases of the module always maintain a phase difference of 180°. The phase offset between devices is determined from the lower four bits of the SMBus address of each interleaved device.

Table 11. INTERLEAVE

SA	UVLO	R (kΩ)	SA in Binary	Low 4-Bits	INTERLEAVE-Ch1	Phase Shift (°)	Rail ID
19h	10.8	10	00011001	1001	9	202.5	25
1Ah	10.8	11	00011010	1010	10	225	26
1Bh	10.8	12.1	00011011	1011	11	247.5	27
1Ch	10.8	13.3	00011100	1100	12	270	28
1Dh	10.8	14.7	00011101	1101	13	292.5	29
1Eh	10.8	16.2	00011110	1110	14	315	30
1Fh	10.8	17.8	00011111	1111	15	337.5	31
20h	4.2	19.6	00100000	0000	0	0	0
21h	4.2	21.5	00100001	0001	1	22.5	1
22h	4.2	23.7	00100010	0010	2	45	2
23h	4.2	26.1	00100011	0011	3	67.5	3
24h	4.2	28.7	00100100	0100	4	90	4
25h	4.2	31.6	00100101	0101	5	112.5	5
26h	4.2	34.8, low	00100110	0110	6	135	6
27h	4.2	38.3	00100111	0111	7	157.5	7
28h	4.5	42.2, open	00101000	1000	8	180	8
29h	4.5	46.4	00101001	1001	9	202.5	9
2Ah	4.5	51.1	00101010	1010	10	225	10
2Bh	4.5	56.2	00101011	1011	11	247.5	11
2Ch	4.5	61.9	00101100	1100	12	270	12
2Dh	4.5	68.1	00101101	1101	13	292.5	13
2Eh	4.5	75	00101110	1110	14	315	14
2Fh	4.5	82.5	00101111	1111	15	337.5	15
30h	10.8	90.9	00110000	0000	0	0	16
31h	10.8	100	00110001	0001	1	22.5	17
32h	10.8	110	00110010	0010	2	45	18
33h	10.8	121	00110011	0011	3	67.5	19
34h	10.8	133	00110100	0100	4	90	20
35h	10.8	147	00110101	0101	5	112.5	21
36h	10.8	162	00110110	0110	6	135	22
37h	10.8	178	00110111	0111	7	157.5	23

4.14 Monitoring Using SMBus

The RAA210925 can monitor a wide variety of different system parameters using the PMBus commands:

- READ_VIN
- READ_VOUT
- READ_IOUT
- READ_INTERNAL_TEMP
- READ_DUTY_CYCLE
- READ_FREQUENCY

4.15 Snapshot Parameter Capture

The RAA210925 offers a special feature to capture parametric data and fault status following a fault. A detailed description is provided in the "PMBus Commands Description" on page 41 under PMBus the commands SNAPSHOT and SNAPSHOT_CONTROL.

5. Layout Guide

To achieve stable operation, low losses, and good thermal performance, some layout considerations are necessary (Figure 32). Refer to the RTKA2109252H00000BU layout design.

- Establish separate SGND plane and PGND planes, then connect SGND to PGND plane on a middle layer and underneath PAD6 with a single point connection. For SGND and PGND pin connections, such as small pins H16, J16, M5 and M17..., use multiple vias for each pin to connect to inner SGND or PGND layers.
- Place enough ceramic capacitors between VIN and PGND, VOUT and PGND and bypass capacitors between VDD, VDRV and the ground plane, as close to the module as possible to minimize high frequency noise. It is very critical to place the output ceramic capacitors close to the VOUT pads and in the direction of the load current path in order to create a low impedance path for the high frequency inductor ripple current.
- Use large copper areas for power paths (VIN, PGND, VOUT) to minimize conduction loss and thermal stress. Also, use multiple vias to connect the power planes in different layers. It is recommended to enlarge PAD11 and PAD9 to place more vias on them. The ceramic capacitors CIN can be placed on the bottom layer under these two pads.
- Connect remote sensing traces to the regulation point to achieve a tight output voltage regulation and place the two traces in parallel. Route a trace from VSEN1/2N and VSEN1/2P to the point of load where the tight output voltage is desired. Avoid routing any sensitive signal traces, such as the VSENN, VSENP sensing lines near the SW pins.
- PAD14 and 16 (SW1 and SW2) are noisy pads, but they are beneficial for thermal dissipation. If the noise issue is critical for the applications, it is recommended to use only the top layer for the SW pads. For better thermal performance, use multiple vias on these pads to connect into the SW inner and bottom layers. However, use caution when placing a limited area of SW planes in any layer. The SW planes should avoid the sensing signals and should be surrounded by the PGND layer to avoid noise coupling.
- For pins SWD1 (L3) and SWD2 (P10), it is recommended to connect to the related SW1 and SW2 pads with short loop traces. The trace width should be more than 20 mils.

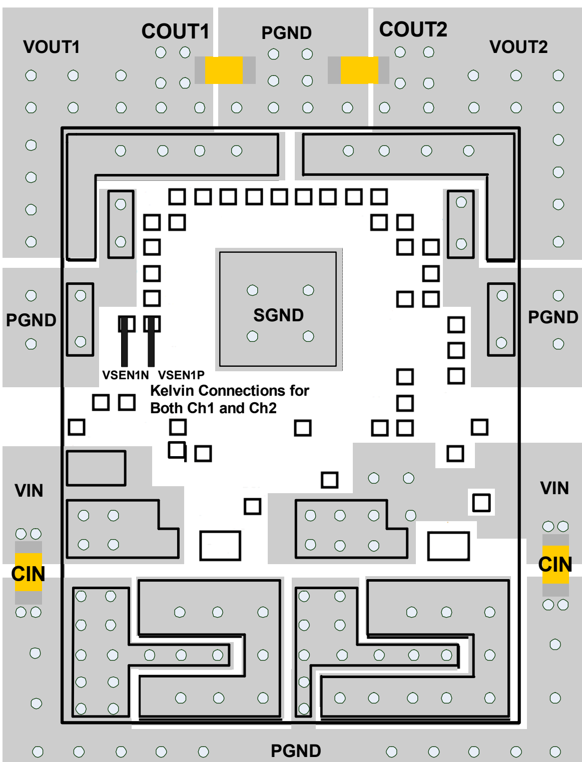


Figure 32. Recommended Layout

5.1 Thermal Considerations

Experimental power loss curves along with θ_{JA} from thermal modeling analysis can be used to evaluate the thermal consideration for the module. The derating curves are derived from the maximum power allowed while maintaining the temperature below the maximum junction temperature of +125°C. The derating curves are derived based on tests of the RTKA2109252H00000BU evaluation board, which is an 8-layer board 4.5x4inch in size with 2oz Cu on the top and bottom layers, 1oz Cu on the inner layers, and multiple via interconnects. In the actual application, other heat sources and design margins should be considered.

5.2 Package Description

The structure of the RAA210925 belongs to the High Density Array (HDA) no-lead package. This kind of package has advantages, such as good thermal and electrical conductivity, low weight, and small size. The HDA package is applicable for surface mounting technology and is being more readily used in the industry. The RAA210925 contains several types of devices, including resistors, capacitors, inductors, and control ICs. The RAA210925 is a copper leadframe based package with exposed copper thermal pads, which have good electrical and thermal conductivity. The copper leadframe and multicomponent assembly is overmolded with a polymer mold compound to protect these devices.

The package outline and typical PCB layout pattern design and typical stencil pattern design are shown on pages 57 through page 63. The module has a small size of 18mm x 23mm x 7.5mm.

5.3 PCB Layout Pattern Design

The bottom of RAA210925 is a leadframe footprint, which is attached to the PCB by the surface mounting process. The PCB layout pattern is shown on pages 61 through 63. The PCB layout pattern is an array of solder mask defined PCB lands which align with the perimeters of the HDA exposed pads and I/O termination dimensions. The thermal lands on the PCB layout also feature an array of solder mask defined lands and should match 1:1 with the package exposed die pads.

5.4 Thermal Vias

A grid of 1.0mm to 1.2mm pitch thermal vias, which drops down and connects to buried copper plane(s), should be placed under the thermal land. The vias should be about 0.3mm to 0.33mm in diameter with the barrel plated to about 1.0 oz. of copper. Although adding more vias (by decreasing via pitch) improves the thermal performance, diminishing returns are seen as the number of vias is increased. Simply use as many vias as practical for the thermal land size and your board design rules allow. All vias should be capped and filled to avoid scavenging solder from the I/O solder joints and creating voids.

5.5 Stencil Pattern Design

Reflowed solder joints on the perimeter I/O lands should have about a 50µm to 75µm (2 mil to 3 mil) standoff height. The solder paste stencil design is the first step in developing optimized, reliable solder joins. Stencil aperture size to solder mask defined PCB land size ratio should typically be 1:1. The aperture width may be reduced slightly to help prevent solder bridging between adjacent I/O lands. To reduce solder paste volume on the larger thermal lands, it is recommended that an array of smaller apertures be used instead of one large aperture. It is recommended that the stencil printing area cover 50% to 80% of the PCB layout pattern. A typical solder stencil pattern is shown on pages 59 through 61. The gap width between pads is 0.6mm. The user should consider the symmetry of the whole stencil pattern when designing its pads. A laser cut, stainless steel stencil with electropolished trapezoidal walls is recommended. Electropolishing "smooths" the aperture walls resulting in reduced surface friction and better paste release, which reduces voids. Using a Trapezoidal Section Aperture (TSA) also promotes paste release and forms a "brick like" paste deposit that assists in firm component placement. A 0.1mm to 0.15mm stencil thickness is recommended for this large pitch (1.3mm) HDA.

5.6 Reflow Parameters

Due to the low mount height of the HDA, “No-Clean” Type 3 solder paste per ANSI/J-STD-005 is recommended. A nitrogen purge is also recommended during reflow. A system board reflow profile depends on the thermal mass of the entire populated board, so it is not practical to define a specific soldering profile just for the HDA. The profile given in Figure 33 is provided as a guideline, which can be customized for varying manufacturing practices and applications.

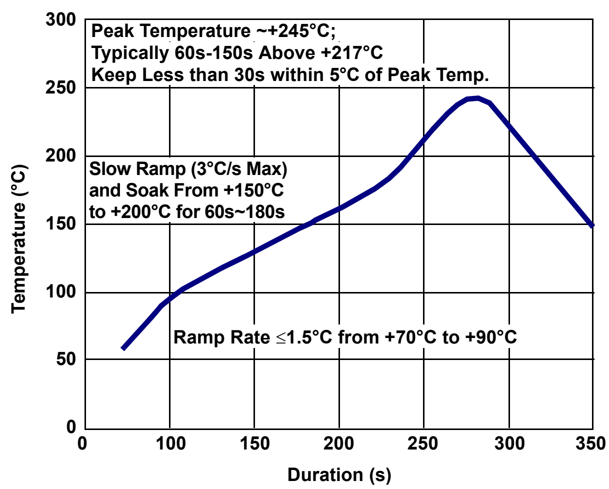


Figure 33. Typical Reflow Profile

6. PMBus Command Summary

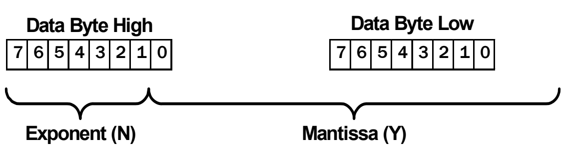
Command Code	Command Name	Description	Type	Data Format	Default Value	Default Setting	Page
00h	PAGE	Selects Controller 0, 1, or both.	R/W Byte	BIT	00h	Channel 1	41
01h	OPERATION	Sets Enable and Disable modes.	R/W Byte	BIT			41
02h	ON_OFF_CONFIG	Configures the EN pin and PMBus commands to turn the unit ON/OFF.	R/W Byte	BIT	16h	Hardware Pin Enable, soft-off	41
03h	CLEAR_FAULTS	Clears fault indications.	SEND Byte				42
21h	VOUT_COMMAND	Sets the nominal value of the output voltage.	R/W Word	L16u		Pin-strap	42
24h	VOUT_MAX	Sets the maximum possible value of V_{OUT}. 110% of pin-strap V_{OUT}.	R/W Word	L16u		1.1 x V_{OUT} Pin-strap	42
33h	FREQUENCY_SWITCH	Sets the switching frequency.	R/W Word	L11		Pin-strap	42
37h	INTERLEAVE	Configures a phase offset between devices sharing a SYNC clock.	R/W Word	BIT	1000h(Ch1)/ 0000h(Ch2)	180° phase shift between Ch1/Ch2	43
40h	VOUT_OV_FAULT_LIMIT	Sets the V_{OUT} overvoltage fault threshold.	R/W Word	L16u		1.15 x V_{OUT} Pin-strap	43
44h	VOUT_UV_FAULT_LIMIT	Sets the V_{OUT} undervoltage fault threshold.	R/W Word	L16u		0.85 x V_{OUT} Pin-strap	43
46h	IOUT_OC_FAULT_LIMIT	Sets the I_{OUT} peak overcurrent fault threshold.	R/W Word	L11	E320h	50A	44
4Bh	IOUT_UC_FAULT_LIMIT	Sets the I_{OUT} valley undercurrent fault threshold.	R/W Word	L11	E4E0h	-50A	44
4Fh	OT_FAULT_LIMIT	Sets the over-temperature fault threshold.	R/W Word	L11	EB98h	+115°C	44
53h	UT_FAULT_LIMIT	Sets the under-temperature fault threshold.	R/W Word	L11	E530h	-45°C	45
55h	VIN_OV_FAULT_LIMIT	Sets the V_{IN} overvoltage fault threshold.	R/W Word	L11	D3A0	14.5V	45
59h	VIN_UV_FAULT_LIMIT	Sets the V_{IN} undervoltage fault threshold.	R/W Word	L11		Pin-strap	45
5Eh	POWER_GOOD_ON	Sets the voltage threshold for power-good indication.	R/W Word	L16u		0.9 x V_{OUT} Pin-strap	45
60h	TON_DELAY	Sets the delay time from ENABLE to start of V_{OUT} rise.	R/W Word	L11		Pin-strap	46

Command Code	Command Name	Description	Type	Data Format	Default Value	Default Setting	Page
61h	TON_RISE	Sets the rise time of V_{OUT} after ENABLE and TON_DELAY.	R/W Word	L11		Pin-strap	46
64h	TOFF_DELAY	Sets the delay time from DISABLE to start of V_{OUT} fall.	R/W Word	L11		Pin-strap	46
65h	TOFF_FALL	Sets the fall time for V_{OUT} after DISABLE and TOFF_DELAY.	R/W Word	L11		Pin-strap	46
78h	STATUS_BYTE	Returns an abbreviated status for fast reads.	Read Byte	BIT	00h	No Faults	47
79h	STATUS_WORD	Returns information with a summary of the units's fault condition.	Read Word	BIT	0000h	No Faults	48
7Ah	STATUS_VOUT	Returns the V_{OUT} specific status.	Read Byte	BIT	00h	No Faults	48
7Bh	STATUS_IOUT	Returns the I_{OUT} specific status.	Read Byte	BIT	00h	No Faults	49
7Ch	STATUS_INPUT	Returns status specific to the input.	Read Byte	BIT	00h	No Faults	49
7Dh	STATUS_TEMP	Returns the temperature specific status.	Read Byte	BIT	00h	No Faults	49
7Eh	STATUS_CML	Returns the communication, logic and memory specific status.	Read Byte	BIT	00h	No Faults	50
80h	STATUS_MFR_SPECIFIC	Returns the external sync clock specific status.	Read Byte	BIT	00h	No Faults	50
88h	READ_VIN	Returns the input voltage reading.	Read Word	L11			50
8Bh	READ_VOUT	Returns the output voltage reading.	Read Word	L16u			51
8Ch	READ_IOUT	Returns the output current reading.	Read Word	L11			51
8Dh	READ_INTERNAL_TEMP	Returns the temperature reading internal to the device.	Read Word	L11			51
94h	READ_DUTY_CYCLE	Returns the duty cycle reading during the ENABLE state.	Read Word	L11			51
95h	READ_FREQUENCY	Returns the measured operating switch frequency.	Read Word	L11			51
DFh	ASCR_CONFIG	Configures ASCR control loop.	R/W Block	CUS		Pin-strap	52
E4h	DEVICE_ID	Returns the 16-byte (character) device identifier string.	Read Block	ASC		Reads Device Version	52
E5h	MFR_IOUT_OC_FAULT_ RESPONSE	Configures the I_{OUT} overcurrent fault response.	R/W Byte	BIT	B9h	Disable and Retry with 70ms delay	52
E6h	MFR_IOUT_UC_FAULT_ RESPONSE	Configures the I_{OUT} undercurrent fault response.	R/W Byte	BIT	B9h	Disable and Retry with 70ms delay	53

Command Code	Command Name	Description	Type	Data Format	Default Value	Default Setting	Page
E7h	IOUT_AVG_OC_FAULT_LIMIT	Sets the I_{OUT} average overcurrent fault threshold.	R/W	L11		Set by SYNC/OCP pin-strap	53
E8h	IOUT_AVG_UC_FAULT_LIMIT	Sets the I_{OUT} average undercurrent fault threshold.	R/W	L11	DC40h	-30A	54
EAh	SNAPSHOT	Returns 32-byte read-back of parametric and status values.	Read Block	BIT			55
F3h	SNAPSHOT_CONTROL	Snapshot feature control command.	R/W Byte	BIT			55

6.1 PMBus Data Formats

- **Linear-11 (L11)** - The L11 data format uses 5-bit two's complement exponent (N) and 11-bit two's complement mantissa (Y) to represent the real world decimal value (X). The relation between the real world decimal value (X), N, and Y is: $X = Y \cdot 2^N$



- **Linear-16 Unsigned (L16u)** - The L16u data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit unsigned integer mantissa (Y) to represent real world decimal value (X). The relation between the real world decimal value (X), N and Y is: $X = Y \cdot 2^{-13}$
- **Linear-16 Signed (L16s)** - The L16s data format uses a fixed exponent (hard-coded to N = -13h) and a 16-bit two's complement mantissa (Y) to represent real world decimal value (X). The relation between the real world decimal value (X), N and Y is: $X = Y \cdot 2^{-13}$
- **Bit Field (BIT)** - An explanation of the Bit Field for each command is provided in "PMBus Commands Description" on page 41.
- **Custom (CUS)** - An explanation of the Custom data format for each command is provided in "PMBus Commands Description" on page 41. A combination of Bit Field and integer are common type of Custom data format.
- **ASCII (ASC)** - A variable length string of text characters uses ASCII data format.

6.2 PMBus Use Guidelines

The PMBus is a powerful tool that allows the user to optimize circuit performance by configuring devices for their application. When configuring a device in a circuit, the device should be disabled whenever most settings are changed with PMBus commands. Some exceptions to this recommendation are OPERATION, ON_OFF_CONFIG, CLEAR_FAULTS, VOUT_COMMAND, and ASCR_CONFIG. While the device is enabled any command can be read. Many commands do not take effect until after the device has been re-enabled, hence the recommendation that commands that change device settings are written while the device is disabled.

In addition, there should be a 2ms delay between repeated READ commands sent to the same device. When sending any other command, a 5ms delay is recommended between repeated commands sent to the same device.

7. PMBus Commands Description

PAGE(00h)

Definition: Select Channel 1, Channel 2 or both channels to receive commands. All commands following this command are received and acted on by the selected channel or channels.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 00h (Page 0)

Units: N/A

Bits 7:4	Bits 3:0	Page
0000	0000	0
0000	0001	1
1111	1111	Both

OPERATION (01h)

Definition: Sets Enable and Disable settings.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value:

Units: N/A

Settings	Actions
00h	Immediate off
40h	Soft off
80h	On

ON_OFF_CONFIG (02h)

Definition: Configures the interpretation and coordination of the OPERATION command and the ENABLE pin (EN).

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: 16h (Device starts from ENABLE pin with soft-off)

Units: N/A

Settings	Actions
16h	Device starts from the ENABLE pin with soft off.
17h	Device starts from the ENABLE pin with immediate off.
1Ah	Device starts from the OPERATION command with soft off.
1Bh	Device starts from the OPERATION command with immediate off.

CLEAR_FAULTS (03h)

Definition: Clears all fault bits in all registers. If a fault condition still exists, the bit reasserts immediately. This command does not restart a device if it has shut down, it only clears the faults.

Data Length in Bytes: 0 Byte

Data Format: N/A

Type: Send byte

Default Value: N/A

Units: N/A

Reference: N/A

VOUT_COMMAND (21h)

Definition: Sets or reports the target output voltage. This command cannot set a value higher than VOUT_MAX.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: Pin-strap setting

Units: Volts

Range: 0V to VOUT_MAX

VOUT_MAX (24h)

Definition: Sets an upper limit on the output voltage the unit can command regardless of any other commands or combinations. The intent of this command is to provide a safeguard against a user accidentally setting the output voltage to a possibly destructive level rather than to be the primary output overprotection. Default value can be changed using PMBus.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 1.10 x V_{OUT} pin-strap setting

Units: Volts

Range: 0V to 5.5V

FREQUENCY_SWITCH (33h)

Definition: Sets the switching frequency of the device. Initial default value is defined by a pin-strap and this value can be overridden by writing this command through the PMBus. If using an external SYNC, set this value as close as possible to the external clock value. The output must be disabled when writing this command.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: kHz

Range: 296kHz to 1067kHz

INTERLEAVE (37h)

Definition: Configures the phase offset of a device that is sharing a common SYNC clock with other devices. The phase offset of each device can be set to any value between 0° and 360° in 22.5° increments. The internal two phases of the module always maintain a phase difference of 180°.

Data Length in Bytes: 2

Data Format: BIT

Type: R/W

Default Value: 1000h (Page0), 0000h (Page1)

Units: N/A

Bits	Purpose	Value	Description
15:8	Reserved	0	Reserved
7:4	Group Number	0 to 15	Sets the group number. A value of 0 is interpreted as 16.
3:0	Position in Group	0 to 15	Sets position of the device's rail within the group.

VOUT_OV_FAULT_LIMIT (40h)

Definition: Sets the V_{OUT} overvoltage fault threshold.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 1.15 x V_{OUT} pin-strap setting

Units: V

Range: 0V to VOUT_MAX

VOUT_UV_FAULT_LIMIT (44h)

Definition: Sets the V_{OUT} undervoltage fault threshold. This fault is masked during ramp or when disabled.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 0.85 x V_{OUT} pin-strap setting

Units: V

Range: 0V to VOUT_MAX

IOUT_OC_FAULT_LIMIT (46h)

Definition: Sets the I_{OUT} peak overcurrent fault threshold. This limit is applied to current measurement samples taken after the Current Sense Blanking Time has expired. A fault occurs after this limit is exceeded. The recommended peak OCP limit is determined by Equation 1.

$$IOUT\_OC\_FAULT\_LIMIT = (IOUT\_AVG\_OC\_FAULT\_LIMIT + 0.5 \bullet IRIPPLE_{P-P}) \bullet 130\% \quad \text{(EQ. 1)}$$

A hard bound of 50A is applied to the command value. This feature shares the OC fault bit operation (in STATUS_IOUT) and OC fault response with the IOUT_AVG_OC_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: E320h (50A)

Units: A

Range: -100A to 100A

IOUT_UC_FAULT_LIMIT (4Bh)

Definition: Sets the I_{OUT} valley undercurrent fault threshold. This limit is applied to current measurement samples taken after the Current Sense Blanking Time has expired. A fault occurs after this limit is exceeded. The recommended valley UCP limit is determined by Equation 2:

$$IOUT\_UC\_FAULT\_LIMIT = (IOUT\_AVG\_UC\_FAULT\_LIMIT - 0.5 \bullet IRIPPLE_{P-P}) \bullet 130\% \quad \text{(EQ. 2)}$$

A hard bound of -50A is applied to the command value. This feature shares the UC fault bit operation (in STATUS_IOUT) and UC fault response with IOUT_AVG_UC_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: E4E0 (-50A)

Units: A

Range: -100A to 100A

OT_FAULT_LIMIT (4Fh)

Definition: Sets the temperature at which the device should indicate an over-temperature fault. Note that the temperature must drop below the fault threshold to clear this fault.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: EB98 (+115°C)

Units: °C

Range: 0°C to +175°C

UT_FAULT_LIMIT (53h)

Definition: Sets the temperature, in degrees Celsius, of the unit where it should indicate an under-temperature fault. Note that the temperature must rise above the fault threshold to clear this fault.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: E530h (-45°C)

Units: °C

Range: -55°C to +25°C

VIN_OV_FAULT_LIMIT (55h)

Definition: Sets the V_{IN} overvoltage fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: D3A0 (14.5V)

Units: V

Range: 0V to 16V

VIN_UV_FAULT_LIMIT (59h)

Definition: Sets the V_{IN} undervoltage fault threshold.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: V

Range: 0V to 12V

POWER_GOOD_ON (5Eh)

Definition: Sets the voltage threshold for power-good indication. Power-good asserts after the output voltage exceeds POWER_GOOD_ON and deasserts when the output voltage is less than VOUT_UV_FAULT_LIMIT. It is recommended to set POWER_GOOD_ON higher than VOUT_UV_FAULT_LIMIT.

Data Length in Bytes: 2

Data Format: L16u

Type: R/W

Default Value: 0.9 x V_{OUT} pin-strap setting

Units: V

TON_DELAY (60h)

Definition: Sets the delay time from when the device is enabled to the start of V_{OUT} rise.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: ms

Range: 2ms to 300ms

TON_RISE (61h)

Definition: Sets the rise time of V_{OUT} after ENABLE and TON_DELAY.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: ms

Range: 1ms to 120ms

TOFF_DELAY (64h)

Definition: Sets the delay time from DISABLE to start of V_{OUT} fall.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: ms

Range: 2ms to 300ms

TOFF_FALL (65h)

Definition: Sets the soft-off fall time for V_{OUT} after DISABLE and TOFF_DELAY.

Data Length in Bytes: 2

Data Format: L11

Type: R/W

Default Value: Pin-strap setting

Units: ms

Range: 0ms to 120ms

STATUS_BYTE (78h)

Definition: Returns one byte of information with a summary of the most critical faults.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault has occurred.
1	CML	A communications, memory, or logic fault has occurred.
0	NONE OF THE ABOVE	A fault not listed in Bits 7:1 has occurred.

STATUS_WORD (79h)

Definition: Returns two bytes of information with a summary of the unit's fault condition. Based on the information in these bytes, the host can get more information by reading the appropriate status registers. The low byte of the STATUS_WORD is the same register as the STATUS_BYTE (78h) command.

Data Length in Bytes: 2

Data Format: BIT

Type: Read Only

Default Value: 0000h

Units: N/A

Bit Number	Status Bit Name	Meaning
15	VOUT	An output voltage fault has occurred.
14	IOUT/POUT	An output current or output power fault has occurred.
13	INPUT	An input voltage, input current, or input power fault has occurred.
12	MFG_SPECIFIC	A manufacturer specific fault has occurred.
11	POWER_GOOD#	The POWER_GOOD signal, if present, is negated.
10	Reserved	Reserved
9	OTHER	A bit in STATUS_OTHER is set.
8	UNKNOWN	A fault type not given in Bits 15:1 of the STATUS_WORD has been detected.
7	BUSY	A fault was declared because the device was busy and unable to respond.
6	OFF	This bit is asserted if the unit is not providing power to the output, regardless of the reason, including simply not being enabled.
5	VOUT_OV_FAULT	An output overvoltage fault has occurred.
4	IOUT_OC_FAULT	An output overcurrent fault has occurred.
3	VIN_UV_FAULT	An input undervoltage fault has occurred.
2	TEMPERATURE	A temperature fault has occurred.
1	CML	A communications, memory, or logic fault has occurred.
0	NONE OF THE ABOVE	A fault not listed in Bits 7:1 has occurred.

STATUS_VOUT (7Ah)

Definition: Returns one data byte with the status of the output voltage.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	VOUT_OV_FAULT	Indicates an output overvoltage fault.
6:5	Reserved	Reserved
4	VOUT_UV_FAULT	Indicates an output undervoltage fault.
3:0	N/A	These bits are not used.

STATUS_IOUT (7Bh)

Definition: Returns one data byte with the status of the output current.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	IOUT_OC_FAULT	An output overcurrent fault has occurred.
6:5	Reserved	Reserved
4	IOUT_UC_FAULT	An output undercurrent fault has occurred.
3:0	N/A	These bits are not used.

STATUS_INPUT (7Ch)

Definition: Returns the input voltage and input current status information.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	VIN_OV_FAULT	An input overvoltage fault has occurred.
6:5	Reserved	Reserved
4	VIN_UV_FAULT	An input undervoltage fault has occurred.
3:0	N/A	These bits are not used.

STATUS_TEMP (7Dh)

Definition: Returns one byte of information with a summary of any temperature related faults.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Only

Default Value: 00h

Units: N/A

Bit Number	Status Bit Name	Meaning
7	OT_FAULT	An over-temperature fault has occurred.
6:5	Reserved	Reserved
4	UT_FAULT	An under-temperature fault has occurred.
3:0	N/A	These bits are not used.

STATUS_CML (7Eh)

Definition: Returns one byte of information with a summary of any communications, logic, and/or memory errors.

Data Length in Bytes: 1

Data Format: BIT

Type: Read Only

Default Value: 00h

Units: N/A

Bit Number	Meaning
7	Invalid or unsupported PMBus command was received.
6	The PMBus command was sent with invalid or unsupported data.
5	Packet error was detected in the PMBus command.
4	Memory/logic fault has occurred.
3:2	Reserved
1	A PMBus command tried to write to a read-only or protected command, or a communication fault other than the ones listed in this table has occurred.
0	Not used

STATUS_MFR_SPECIFIC (80h)

Definition: Returns one byte of information providing the status of the clock synchronization faults.

Data Length in Bytes: 1

Data Format: BIT

Type: Read only

Default value: 00h

Units: N/A

Bit Number	Field Name	Meaning
7:4	Reserved	Reserved
3	External Switching Period Fault	Loss of external clock synchronization has occurred.
2:0	Reserved	Reserved

READ_VIN (88h)

Definition: Returns the input voltage reading.

Data Length in Bytes: 2

Data Format: L11

Type: Read Only

Units: V

READ_VOUT (8Bh)

Definition: Returns the output voltage reading.

Data Length in Bytes: 2

Data Format: L16u

Type: Read Only

Units: V

READ_IOUT (8Ch)

Definition: Returns the output current reading.

Data Length in Bytes: 2

Data Format: L11

Type: Read Only

Default Value: N/A

Units: A

READ_INTERNAL_TEMP (8Dh)

Definition: Returns the controller junction temperature reading from the internal temperature sensor.

Data Length in Bytes: 2

Data Format: L11

Type: Read Only

Units: °C

READ_DUTY_CYCLE (94h)

Definition: Reports the actual duty cycle of the converter during the enable state.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Units: %

READ_FREQUENCY (95h)

Definition: Reports the actual switching frequency of the converter during the enable state.

Data Length in Bytes: 2

Data Format: L11

Type: Read only

Units: kHz

ASCR_CONFIG (DFh)

Definition: Allows user configuration of ASCR settings. ASCR gain is analogous to bandwidth, ASCR residual is analogous to damping. To improve load transient response performance, increase ASCR gain. To lower transient response overshoot, increase ASCR residual. Increasing ASCR gain can result in increased PWM jitter and should be evaluated in the application circuit. Excessive ASCR gain can lead to excessive output voltage ripple. Increasing ASCR residual to improve transient response damping can result in slower recovery times, but does not affect the peak output voltage deviation. Typical ASCR gain settings range from 50 to 1000, and ASCR residual settings range from 10 to 100.

Data Length in Bytes: 4

Data Format: CUS

Type: R/W

Default Value: Pin-strap setting

Bit	Purpose	Data Format	Value	Description
31:25	Unused		0000000h	Unused
24	Reserved			Reserved
23:16	ASCR Residual Setting	Integer		ASCR residual
15:0	ASCR Gain Setting	Integer		ASCR gain

DEVICE_ID (E4h)

Definition: Returns the 16-byte (character) device identifier string.

Data Length in Bytes: 16

Data Format: ASC

Type: Block Read

Default Value: Part number/Die revision/Firmware revision

MFR_IOUT_OC_FAULT_RESPONSE (E5h)

Definition: Configures the I_{OUT} overcurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the overcurrent status bit in STATUS_IOUT.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: B9h (Disable and continuous retry with 70ms delay)

Units: N/A

Field Name	Actions
80h	Disable with no retry.
B9h	Disable and continuous retry with 70ms delay

MFR_IOUT_UC_FAULT_RESPONSE (E6h)

Definition: Configures the I_{OUT} undercurrent fault response as defined by the following table. The command format is the same as the PMBus standard fault responses except that it sets the undercurrent status bit in STATUS_IOUT.

Data Length in Bytes: 1

Data Format: BIT

Type: R/W

Default Value: B9h (Disable and continuous retry with 70ms delay)

Units: N/A

Field Name	Actions
80h	Disable with no retry.
B9h	Disable and continuous retry with 70ms delay

IOUT_AVG_OC_FAULT_LIMIT (E7h)

Definition: Sets the I_{OUT} average overcurrent fault threshold. For down-slope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the current sense blanking time (which occurs at the beginning of the 1-D interval). For up-slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the current sense blanking time (which occurs at the beginning of the D interval). This feature shares the OC fault bit operation (in STATUS_IOUT) and OC fault response with IOUT_OC_FAULT_LIMIT.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: SYNC/OCP pin-strap setting

Units: A

Range: -100A to 100A

IOUT_AVG_UC_FAULT_LIMIT (E8h)

Definition: Sets the I_{OUT} average undercurrent fault threshold. For down-slope sensing, this corresponds to the average of all the current samples taken during the (1-D) time interval, excluding the current sense blanking time (which occurs at the beginning of the 1-D interval). For up-slope sensing, this corresponds to the average of all the current samples taken during the D time interval, excluding the current sense blanking time (which occurs at the beginning of the D interval). This feature shares the UC fault bit operation (in STATUS_IOUT) and UC fault response with IOUT_ UC_FAULT_LIMIT.

Paged or Global: Paged

Data Length in Bytes: 2

Data Format: Linear-11

Type: R/W

Protectable: Yes

Default Value: DC40h (-30A)

Units: A

Range: -100A to 100A

SNAPSHOT (EAh)

Definition: A 32-byte read-back of parametric and status values. It allows monitoring and status data to be stored to flash following a fault condition. In case of a fault, last updated values are stored to the flash memory. When the SNAPSHOT STATUS bit is set stored, the device no longer automatically captures parametric and status values following fault until stored data are erased. Use the SNAPSHOT_CONTROL command to erase store data and clear the status bit before next ramp up. Data erased is not allowed when module is enabled.

Data Length in Bytes: 32

Data Format: Bit field

Type: Block Read

Byte Number	Value	PMBus Command	Format
31:23	Reserved	Reserved	00h
22	Flash Memory Status Byte FF - Not Stored 00 - Stored	NVM Status Byte	BIT
21	Manufacturer Specific Status Byte	STATUS_MFR_SPECIFIC (80h)	Byte
20	CML Status Byte	STATUS_CML (7Eh)	Byte
19	Temperature Status Byte	STATUS_TEMPERATURE (7Dh)	Byte
18	Input Status Byte	STATUS_INPUT (7Ch)	Byte
17	I_{OUT} Status Byte	STATUS_IOUT (7Bh)	Byte
16	V_{OUT} Status Byte	STATUS_VOUT (7Ah)	Byte
15:14	Switching Frequency	READ_FREQUENCY (95h)	L11
13:12	Reserved	Reserved	00h
11:10	Internal Temperature	READ_INTERNAL_TEMP (8Dh)	L11
9:8	Duty Cycle	READ_DUTY_CYCLE (94h)	L11
7:6	Reserved	Reserved	L11
5:4	Output Current	READ_IOUT (8Ch)	L11
3:2	Output Voltage	READ_VOUT (8Bh)	L16u
1:0	Input Voltage	READ_VIN (88h)	L11

SNAPSHOT_CONTROL (F3h)

Definition: Writing a 01h causes the device to copy the current Snapshot values from NVRAM to the 32-byte Snapshot command parameter. Writing a 02h causes the device to write the current Snapshot values to NVRAM. Writing a 03h erases all Snapshot values from NVRAM. Write (02h) and Erase (03h) can only be used when the device is disabled. All other values are ignored.

Data Length in Bytes: 1

Data Format: Bit field

Type: R/W byte

Value	Description
01h	Read Snapshot values from NV RAM
02h	Write Snapshot values to NV RAM
03h	Erase Snapshot values stored in NV RAM.

8. Revision History

8.1 Firmware

Table 12. RAA210925 Nomenclature Guide

Firmware Revision Code	Change Description	Note
RAA210925-0-G0100	Initial Release	Recommended for new designs

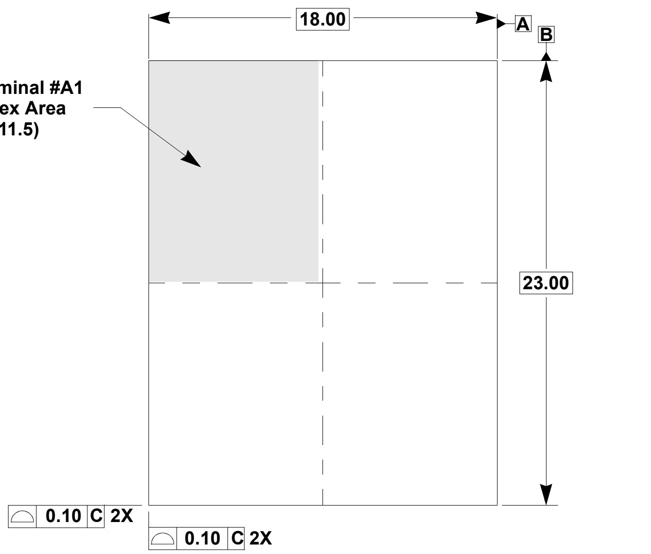
8.2 Datasheet

Rev.	Date	Description
1.00	May 31, 2019	Pin Description table on page 11 and 12 - updated Description for D5 and G14. Page 22, SMBus Communications 1st sentence: Changed PMBus to SMBus page 41 OPERATION (01h) table, 80h removed Nominal from Actions column.
0.00	Sep 12, 2018	Initial release

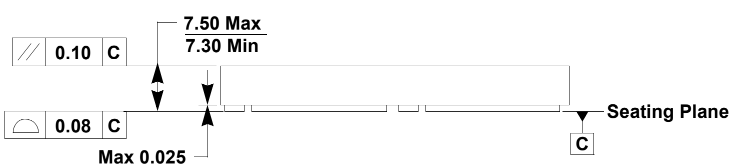
9. Package Outline Drawing

For the most recent package outli

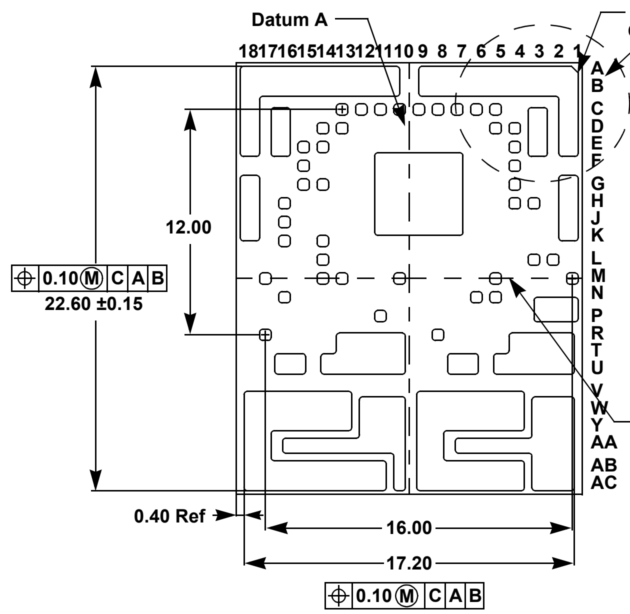
Y58.18x23
58 I/O 18mmx23mmx7.5mm Custom HDA Module
Rev 4, 4/18



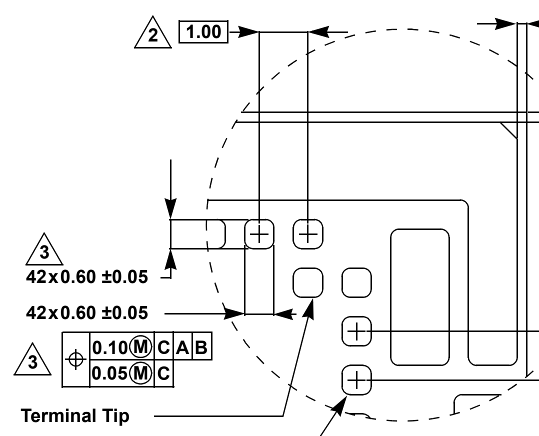
Top View



Side View



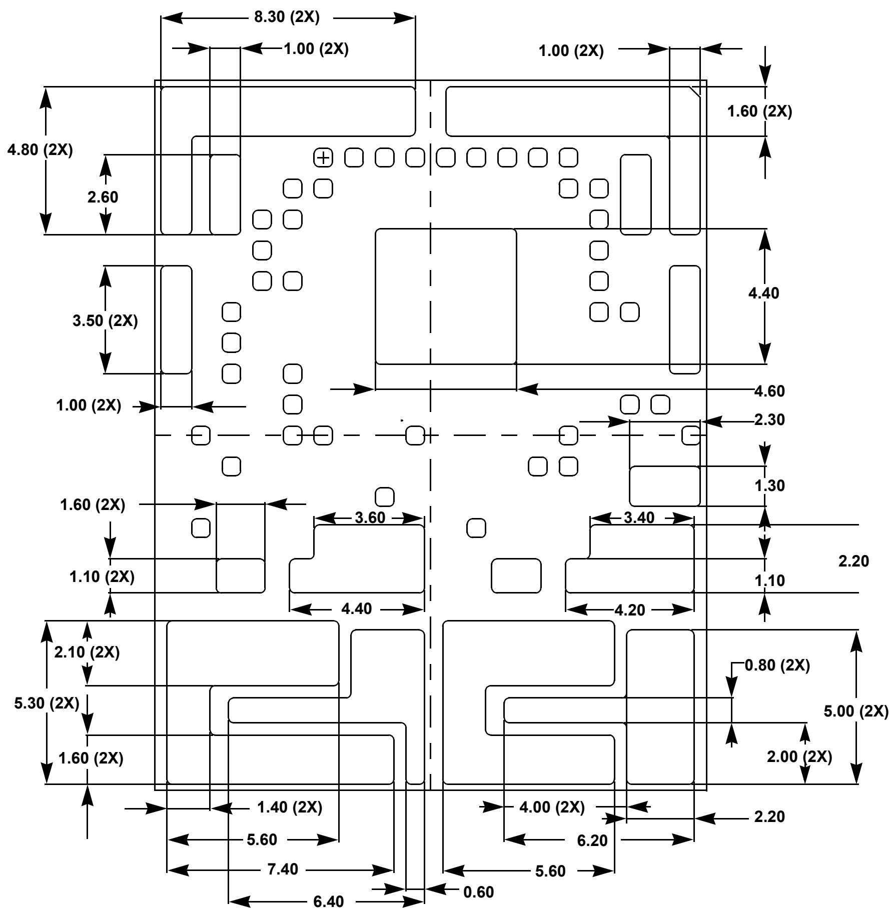
Bottom View



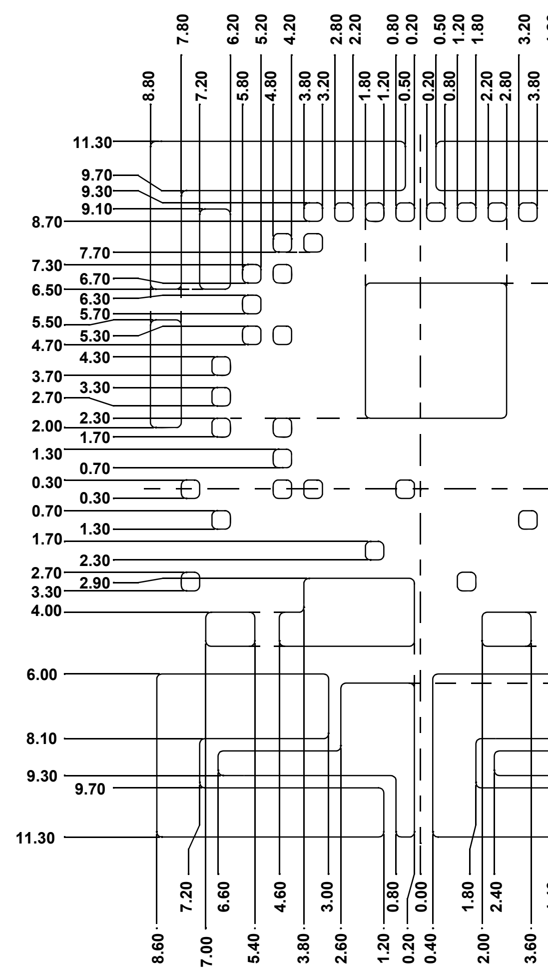
Detail A

Notes:

1. All dimensions are in millimeters.
2. Represents the basic land grid pitch.
3. These 42 I/Os are centered in a fixed row and column matrix at 1.0mm pitch BSC.
4. Dimensioning and tolerancing per ASME Y14.5-2009.
5. Tolerance for exposed PAD edge location dimension on page 3 is ±0.1mm.

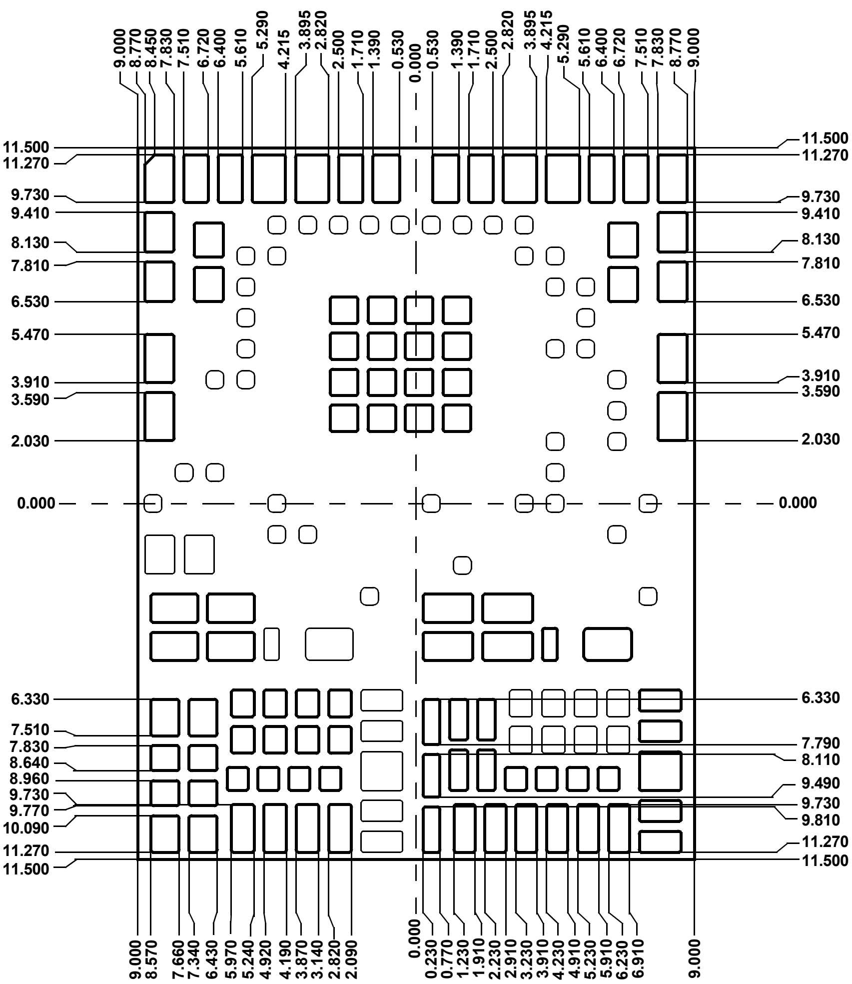


Size Details for the 16 Exposed Pads

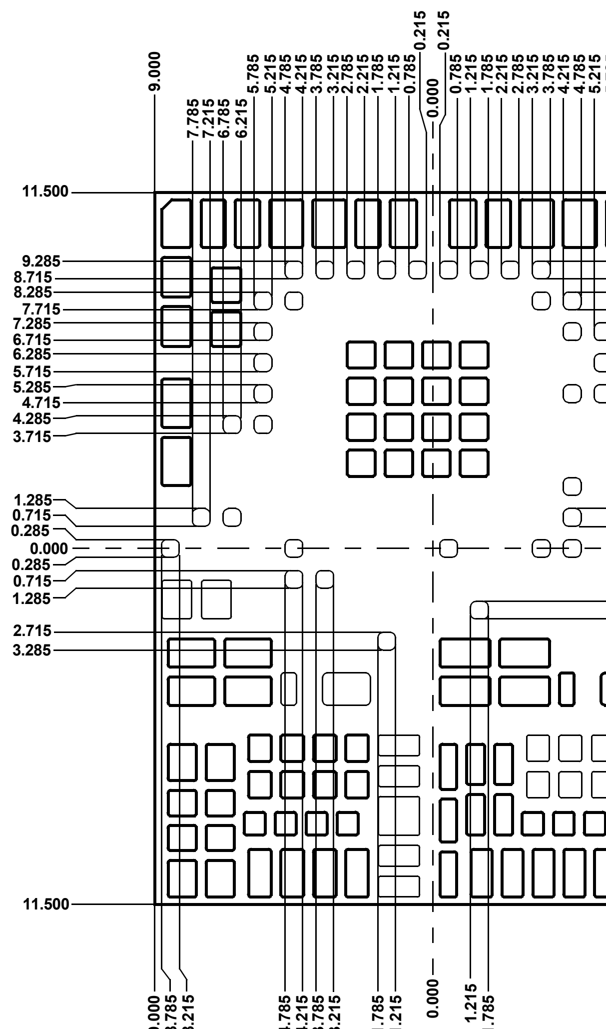


Terminal and Pad Edge Details

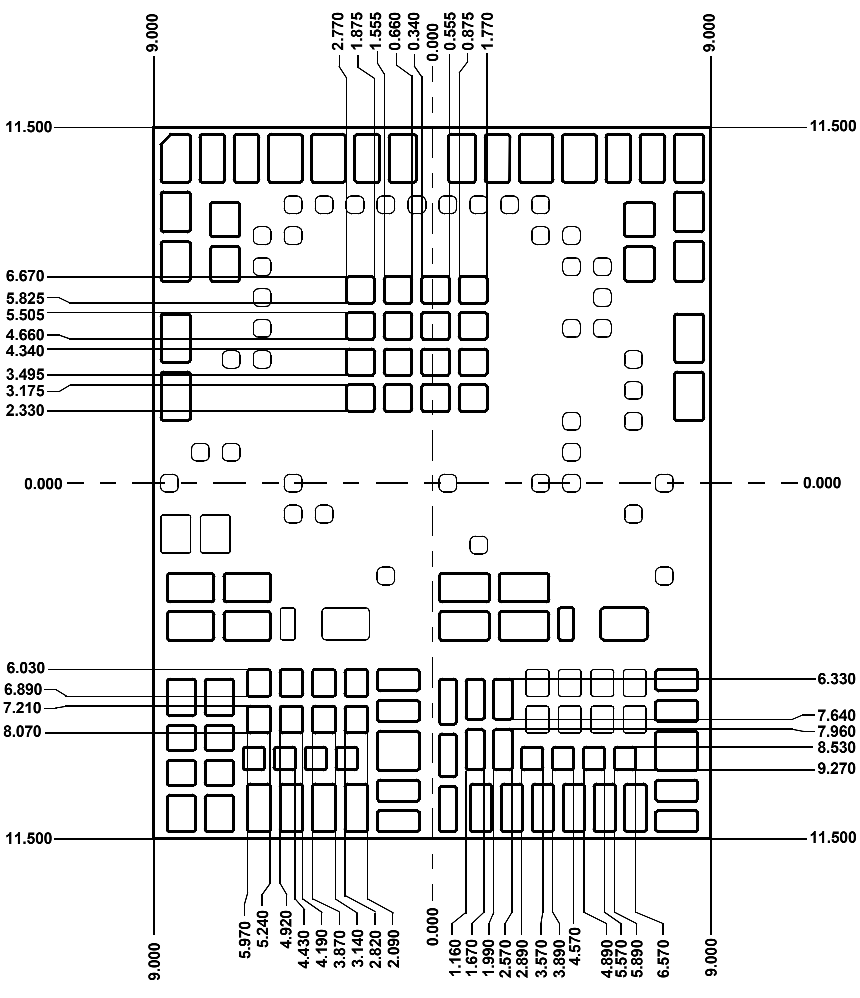
Bottom View



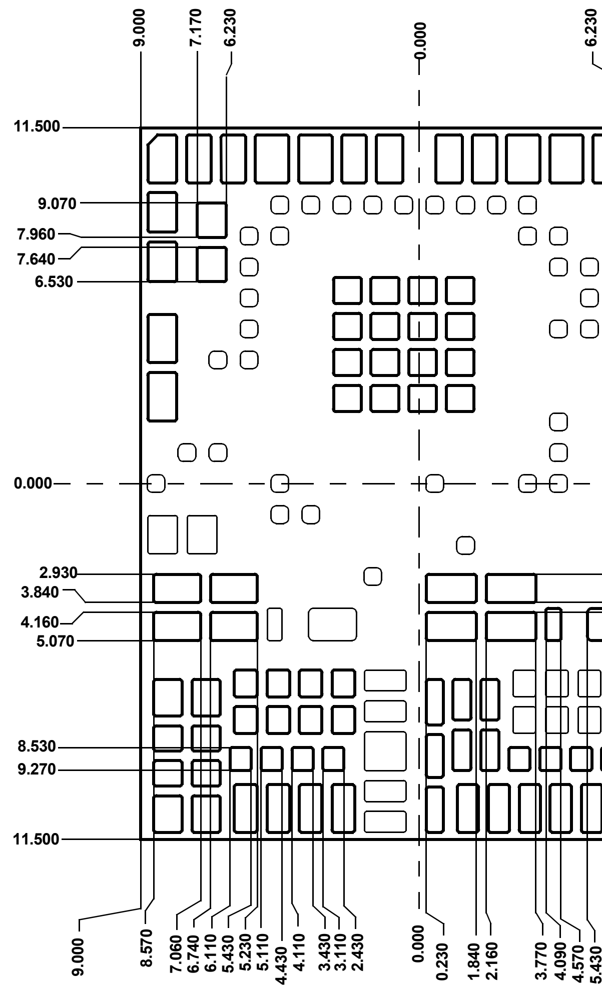
Stencil Opening Edge Position - 1



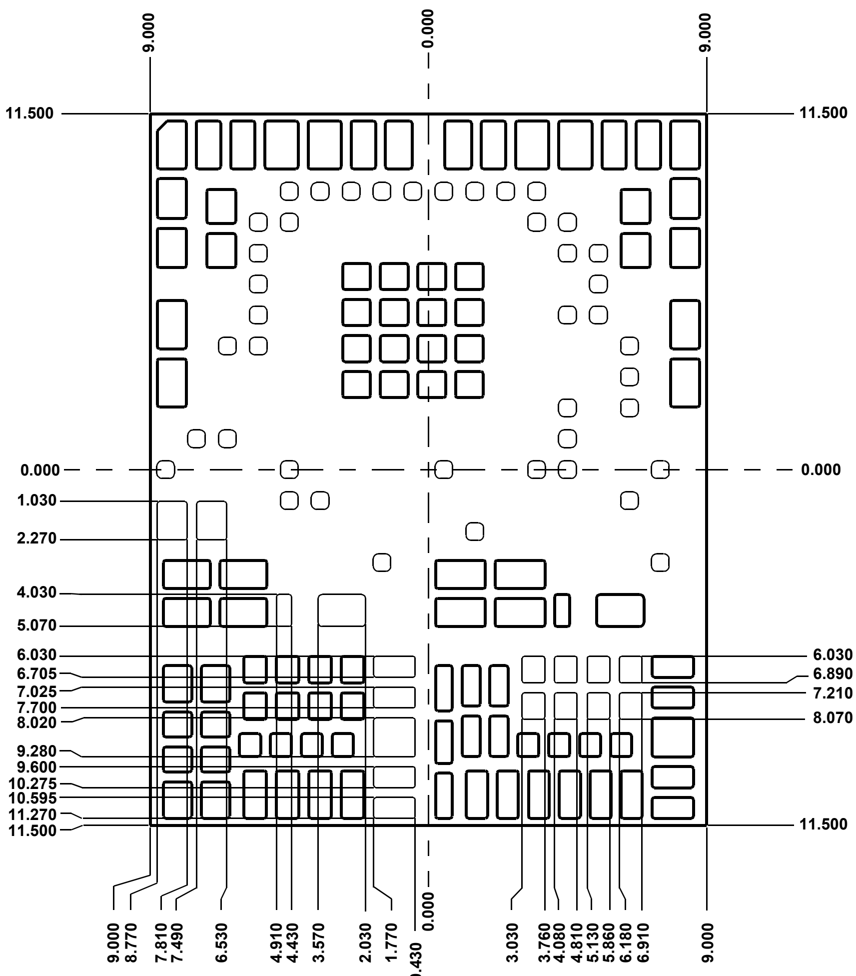
Stencil Opening Edge Position - 2



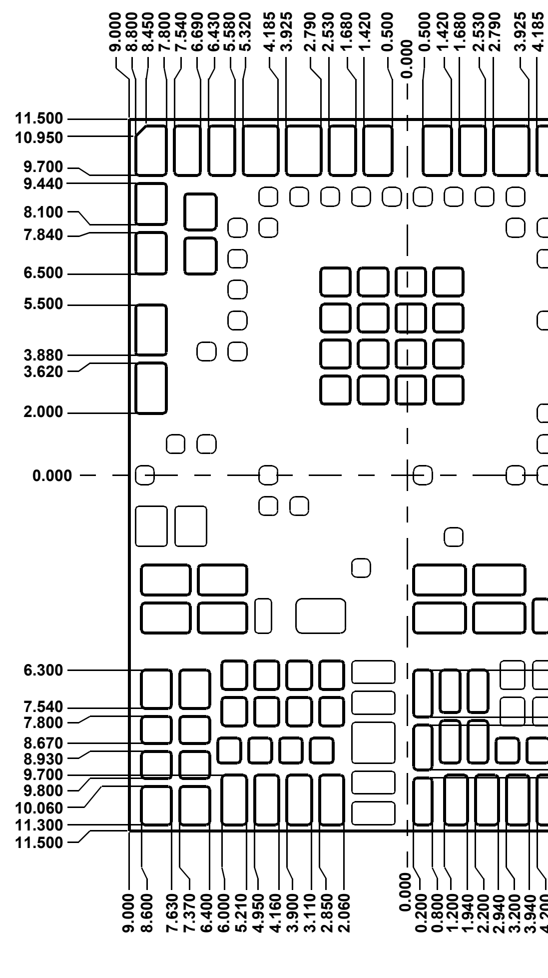
Stencil Opening Edge Position - 3



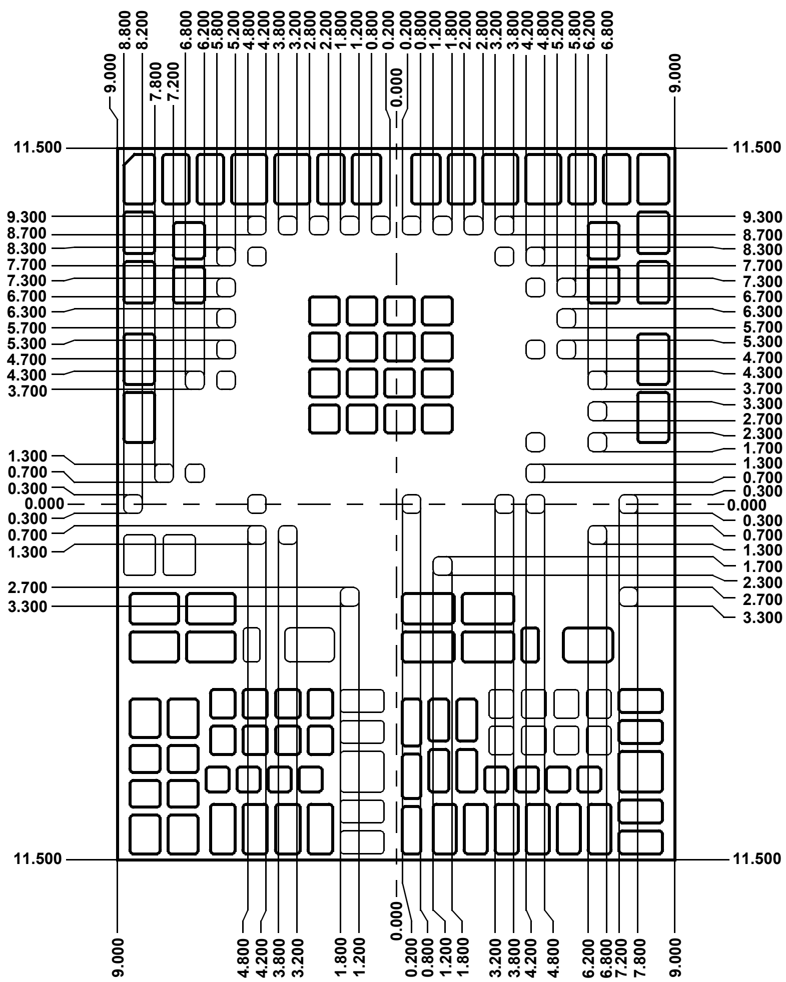
Stencil Opening Edge Position - 4



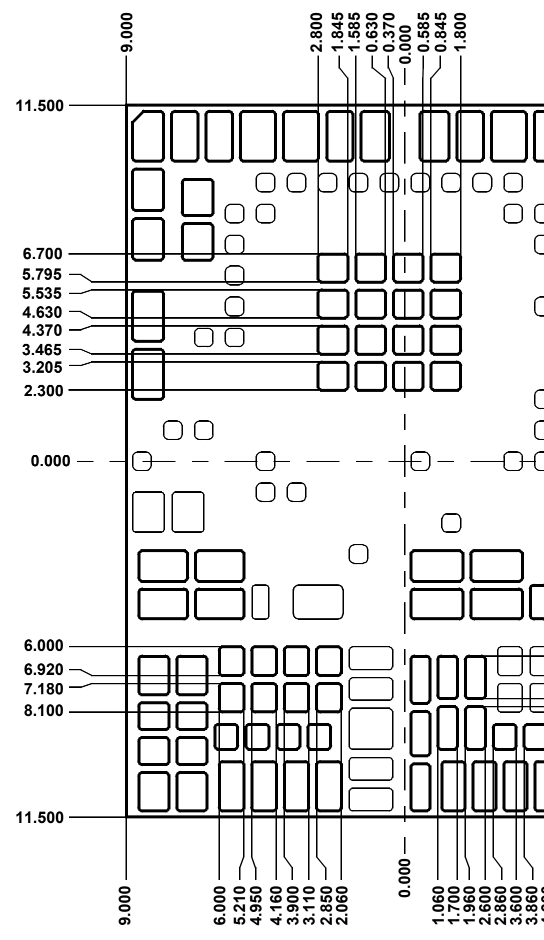
Stencil Opening Edge Position - 5



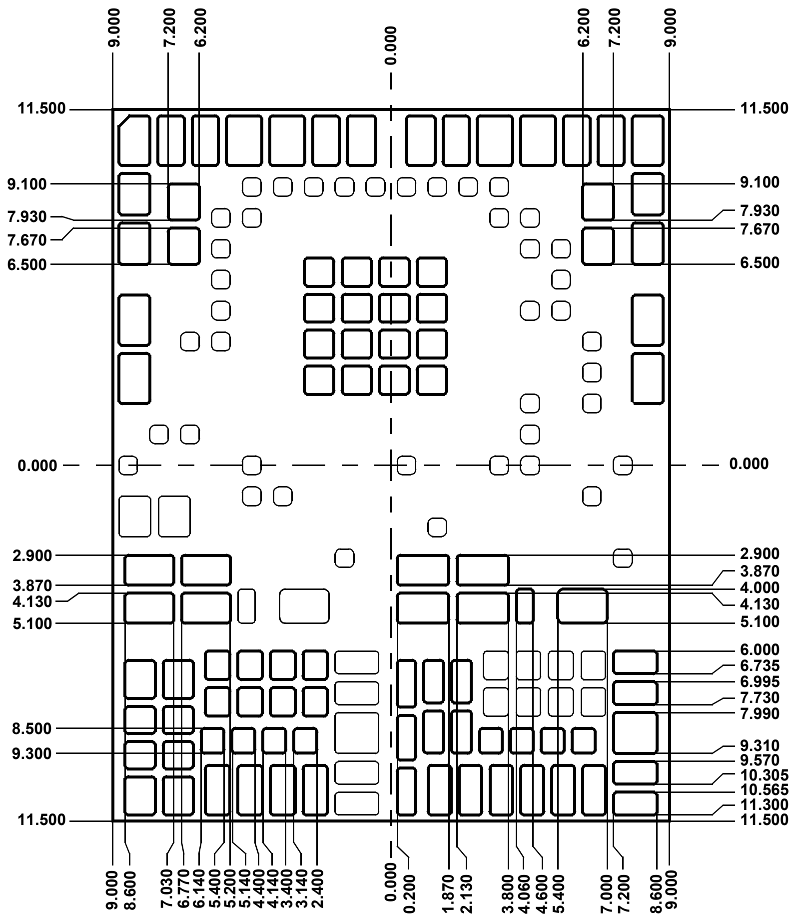
PCB Land Pattern - 1 (for Referenc



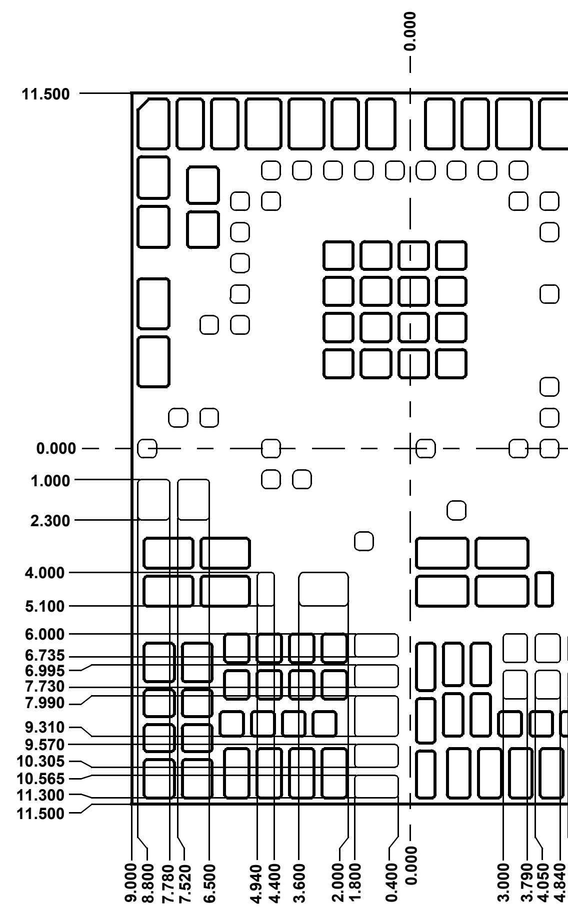
PCB Land Pattern - 2 (for Reference)



PCB Land Pattern - 3 (for Reference)



PCB Land Pattern - 4 (for Reference)



PCB Land Pattern - 5 (for Reference)

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