RAA7884QT

Quad, ±16.5kV ESD Protected, 3.0V to 5.5V, Low Power, RS-422 Transmitter

The RAA7884QT is a ±16.5kV IEC61000-4-2 ESD protected, 3.0V to 5.5V powered, Quad transmitter designed for balanced communication using the RS-422 standard. With low output leakage currents (±10µA), the driver presents a low load to the RS-422 bus.

The driver (Tx) outputs are tri-statable and incorporate a hot plug feature to keep them disabled during power-up and power-down. The RAA7884QT has a common EN/$\overline{EN}$ (see Table 1).

Related Literature

For a full list of related documents, visit our website:

- RAA7884QT device page

Applications

- Telecom equipment
- Motor controllers/encoders
- Programmable logic controllers
- Industrial/process control networks

Features

- IEC61000 ESD protection on RS-422 outputs: ±16.5kV
  - Class 3 ESD level on all other pins: 12kV HBM
  - High machine model ESD level on all pins: 700V
- Wide supply range: 3.0V to 5.5V
- Specified for +125°C operation
- Available in industry standard pinout
- Hot plug Tx outputs remain tri-stated during power-up and power-down
- Low Tx leakage allows > 256 devices on the bus
- High data rate of 50Mbps minimum
- Low quiescent supply current: 0.8mA (maximum)
  - Low shutdown supply current: 60µA
- Current limiting and thermal shutdown for driver overload protection
- Tri-statable Tx outputs
- 5V tolerant logic inputs when V_{CC} = 3.3V
- Pb-free (RoHS compliant)

Table 1. Summary of Features

Part Number	Function	Data Rate (Mbps)	Slew Rate Limited?	Hot Plug?	V_L Pin?	TX Enable Type	Quiescent I_{CC} (mA)	Low Power Shutdown?	Pin Count
RAA7884QT	4 Tx	50	No	Yes	No	EN, $\overline{EN}$	<1	No	16

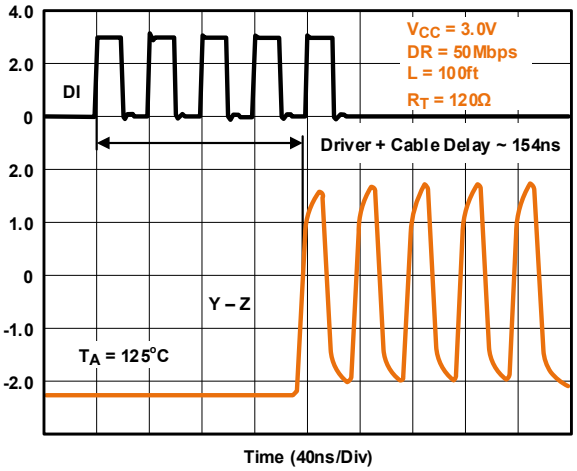


Figure 1. Data Rate Performance at 3.0V

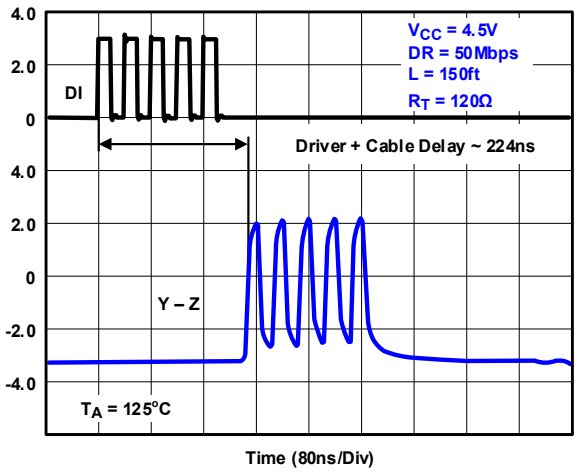


Figure 2. Data Rate Performance at 4.5V

1. Overview

1.1 Typical Operating Circuits (1 of 4 Channels Shown)

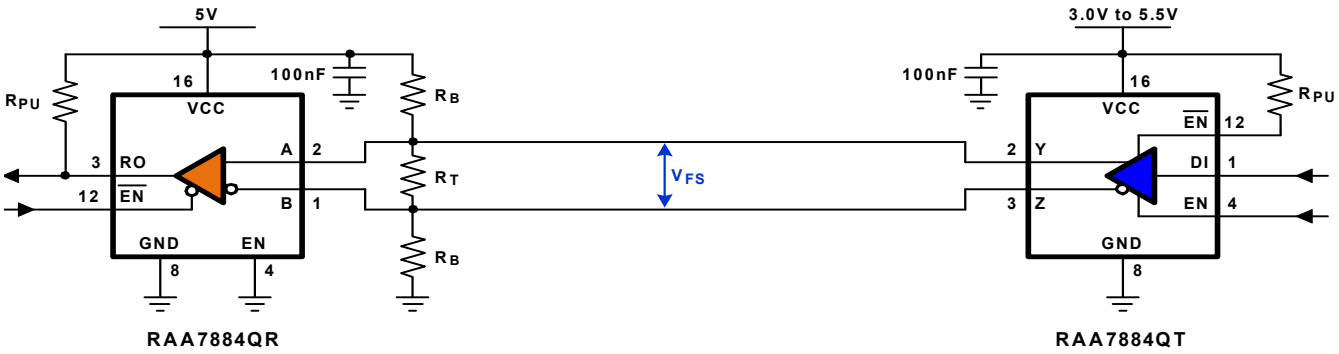


Figure 3. Network Using Group Enables

Note: To calculate the resistor values, see TB509.

1.2 Ordering Information

Part Number (Notes 2, 3)	Part Marking	Temp. Range (°C)	Tape and Reel (Units) (Note 1)	Package (RoHS Compliant)	Pkg. Dwg. #
RAA7884QT4GSP#AB0	RAA7884 QT4GSP	-40 to +125	-	16 Ld SOIC	M16.15
RAA7884QT4GSP#HB0	RAA7884 QT4GSP	-40 to +125	2.5k	16 Ld SOIC	M16.15

Notes:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
3. For Moisture Sensitivity Level (MSL), see the RAA7884QT device pages. For more information about MSL, see TB363.

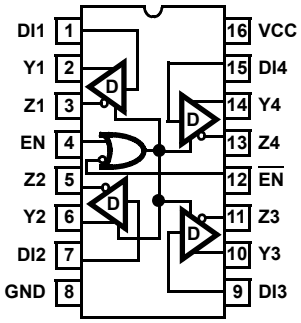
1.3 Truth Tables

RAA7884QT				
Inputs			Outputs	
EN	EN	DIX	ZX	YX
X	0	1/0	0/1	1/0
1	X	0/1	1/0	0/1
0	1	X	Z	Z

Note: Z = Tri-state

1.4 Pin Configuration

(16 Ld N-SOIC)
Top View



1.5 Pin Descriptions

Pin	Function
EN, $\overline{EN}$	Group Driver Output Enables that are internally pulled high to VCC. All driver outputs, Y and Z, are enabled by driving EN high or $\overline{EN}$ low. The outputs are high impedance when EN is low and $\overline{EN}$ is high (for example, if using only the active high EN, connect $\overline{EN}$ directly to VCC; if using only the active low $\overline{EN}$, connect EN directly to GND). If the Group Driver Enable function is not required (see Note 4), connect $\overline{EN}$ to GND.
DIx	Driver input. A low on DI forces the corresponding channel's output Y low and output Z high. A high on DI forces output Y high and output Z low.
GND	Ground connection.
Yx	±16.5kV IEC61000-4-2 ESD protected RS-422 level and a non-inverting transmitter output.
Zx	±16.5kV IEC61000-4-2 ESD protected RS-422 level and an inverting transmitter output.
VCC	System power supply input (3.0V to 5.5V).

Note:
4. Tie unused EN pins with a 1k resistor to VCC.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
VCC to GND		7	V
Input Voltages DI, EN (All varieties)	-0.3	7	V
Output Voltages Y, Z	-0.5	7	V
Output Current Y, Z (per output, continuous, $T_J \leq 125°C$)		100	mA
ESD Rating	**See** **"ESD Performance" on page 5**		

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
16 Ld SOIC Package (Notes 5, 6)	71	32

Notes:

5. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
6. For θ_{JC}, the case temperature location is taken at the package top center.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature (Plastic Package)		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

2.3 Recommended Operation Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage, V_{CC}	3.0	5.5	V
Ambient Temperature	-40	+125	°C

2.4 Electrical Specifications

Test Conditions: V_{CC} = 3.0V to 3.6V and 4.5V to 5.5V; Typicals are at V_{CC} = 3.3V or V_{CC} = 5V, T_A = +25°C unless otherwise specified (Notes 7, 11).

Parameter	Symbol	Test Conditions		Temp (°C)	Min (Note 10)	Typ	Max (Note 10)	Unit
DC Characteristics								
Differential V_{OUT}	V_{OD}	No load		Full	2.5	-	V_{CC}	V
		R_L = 100Ω (RS-422) (see Figure 4)	V_{CC} ≥ 3V	Full	2	2.6	-	V
			V_{CC} ≥ 4.5V	Full	3	4	-	V
Single-Ended V_{OUT} (Y or Z)	V_O	I_O = -20mA, V_{OH}		Full	2.4	2.7	-	V
		I_O = 20mA, V_{OL}		Full	-	0.2	0.4	V
Change in Magnitude of Driver Differential V_{OUT} for Complementary Output States	ΔV_{OD}	R_L = 100Ω (see Figure 4)		Full	-	0.01	0.2	V
Driver Common-Mode V_{OUT}	V_{OC}	R_L = 100Ω (see Figure 4)		Full	-	2.6	3	V
Change in Magnitude of Driver Common-Mode V_{OUT} for Complementary Output States	ΔV_{OC}	R_L = 100Ω (see Figure 4)		Full	-	0.01	0.2	V
Input High Voltage (Logic Pins, Note 13)	V_{IH1}	3.0V ≤ VCC ≤ 3.6V, DI and ENs		Full	2.2	-	-	V
	V_{IH2}	4.5V ≤ VCC ≤ 5.5V, DI		Full	2.7	-	-	V
	V_{IH2E}	4.5V ≤ VCC ≤ 5.5V, ENs		Full	2.4	-	-	V
Input Low Voltage (Logic Pins, Note 13)	V_{IL1}	3.0V ≤ VCC ≤ 5.5V, DI and ENs		Full	-	-	0.8	V
Logic Input Current	I_{IN1}	DIX = 0V or V_{CC}		Full	-1	-	1	µA
	I_{IN2}	EN, $\overline{EN}$		Full	-15	9	15	µA
Output Leakage Current (Y, Z)	I_{OZ}	EN = 0, V_{CC} = 0V to 5.5V, -0.25 ≤ V_O ≤ 6V		Full	-10	-	10	µA
		EN = 0, V_{CC} = 3V to 5.5V, V_O = 0V to V_{CC}		+25	-8	-	8	nA
				(Note 14)	-30	-	30	nA
Driver Short-Circuit Current, V_O = High or Low	I_{OSD1}	EN = 1, V_Y or V_Z = 0V (Note 8)		Full	-	-	±150	mA
		EN = 1, V_Y or V_Z = V_{CC} (Note 8)		Full	-	-	±200	mA
Thermal Shutdown Threshold	T_{SD}			Full	-	160	-	°C
Supply Current								
No-Load Supply Current	I_{CC}	DI = 0V or V_{CC}, EN = 1		Full	-	0.6	0.8	mA
Shutdown Supply Current	I_{SHDN}	DI = 0V or V_{CC}, EN = 0, /EN = 1		Full		60	90	µA
ESD Performance								
RS-422 Pins (Y, Z)		IEC61000-4-2, from bus pins to GND	Air gap	+25	-	±16.5	-	kV
			Contact	+25	-	±9	-	kV
		Human Body Model, from bus pins to GND		+25	-	±15	-	kV
All Pins		HBM, per MIL-STD-883 Method 3015		+25	-	±12	-	kV
		Machine Model		+25	-	700	-	V
Driver Switching Characteristics								
Maximum Data Rate	f_{MAX}	V_{OD} = ±1.5V, C_D = 100pF (see Figure 7)		Full	50	-	-	Mbps
Driver Single-Ended Output Delay	t_{PLH}, t_{PHL}	R_{DIFF} = 100Ω, C_D = 50pF (see Figure 5)		Full	3	8	15	ns
Driver Single-Ended Output Skew	t_{SSK}	R_{DIFF} = 100Ω, C_D = 50pF (see Figure 5)		Full	-	1	3.5	ns

Test Conditions: V_{CC} = 3.0V to 3.6V and 4.5V to 5.5V; Typicals are at V_{CC} = 3.3V or V_{CC} = 5V, T_A = +25°C unless otherwise specified (Notes 7, 11). **(Continued)**

Parameter	Symbol	Test Conditions	Temp (°C)	Min (Note 10)	Typ	Max (Note 10)	Unit
Channel-to-Channel Output Delay Skew	t_{SKCC}	(Figure 5, Note 12)	Full	-	3	5.5	ns
Part-to-Part Output Delay Skew	t_{SKPP}	(Figure 5, Note 9)	Full	-	-	8	ns
Driver Differential Output Skew	t_{DSK}	R_{DIFF} = 100Ω, C_D = 50pF (see Figure 5)	Full	-	0.5	2	ns
Driver Differential Rise or Fall Time	t_R, t_F	R_{DIFF} = 100Ω, C_D = 50pF (see Figure 5)	Full	-	-	7	ns
Driver Enable to Output High	t_{ZH}	SW = GND (see Figure 6)	Full	-	-	20	ns
Driver Enable to Output Low	t_{ZL}	SW = V_{CC} (see Figure 6)	Full	-	-	20	ns
Driver Disable from Output High	t_{HZ}	SW = GND (see Figure 6)	Full	-	-	20	ns
Driver Disable from Output Low	t_{LZ}	SW = V_{CC} (see Figure 6)	Full	-	-	20	ns

Notes:

7. All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
8. Applies to peak current. See Typical Performance Curves beginning on page 8 for more information.
9. t_{SKPP} is the magnitude of the difference in propagation delays of the specified terminals of two units tested with identical test conditions (V_{CC}, temperature, etc.).
10. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
11. EN = 0 indicates that the output(s) under test are disabled via the appropriate logic pin settings. EN = 1 indicates that the logic pins are set to enable the output(s) under test.
12. Channel-to-channel skew is the magnitude of the worst case delta between any two propagation delays of any two outputs on the same IC at the same test conditions.
13. Logic pins are the DIs, and the enable variants.
14. Temperature range is -20°C to +40°C.

2.5 Test Circuits and Waveforms

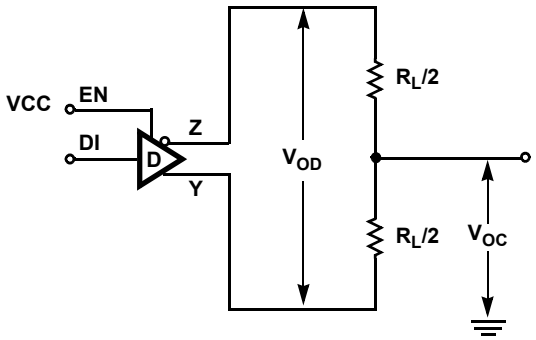


Figure 4. DC Driver Test Circuits

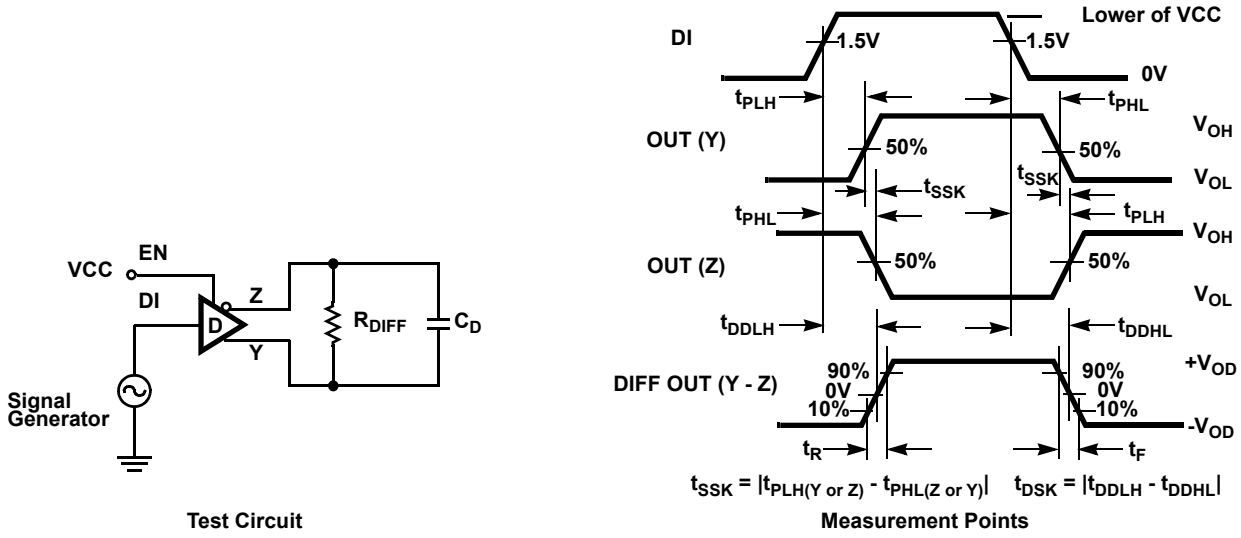
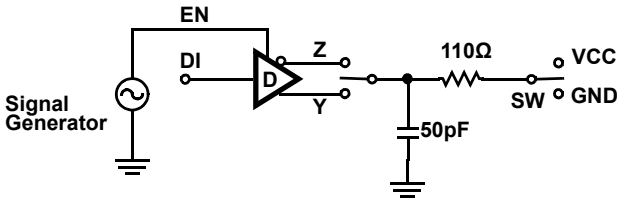


Figure 5. Driver Propagation Delay and Differential Transition Times



Parameter	Output	DI	SW
t_{HZ}	Y/Z	1/0	GND
t_{LZ}	Y/Z	0/1	VCC
t_{ZH}	Y/Z	1/0	GND
t_{ZL}	Y/Z	0/1	V_{CC}

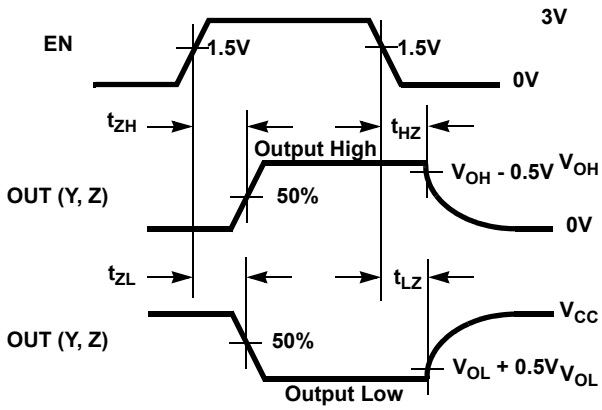


Figure 6. Driver Enable and Disable Times

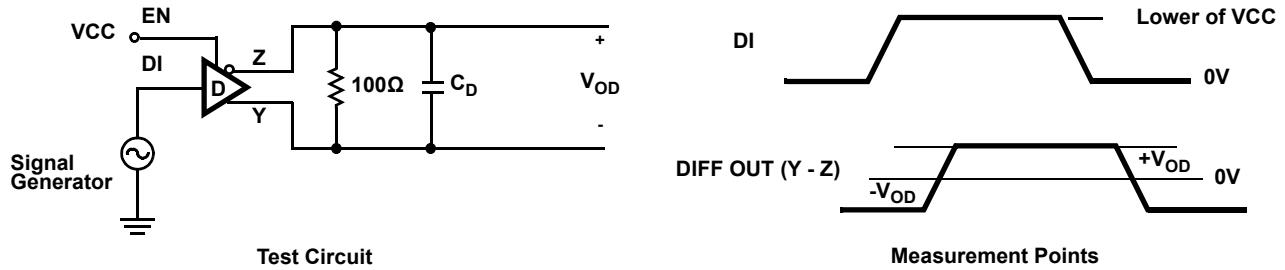


Figure 7. Driver Data Rate

3. Typical Performance Curves

V_{CC} = 3.3V or 5V, T_A = +25°C, unless otherwise specified.

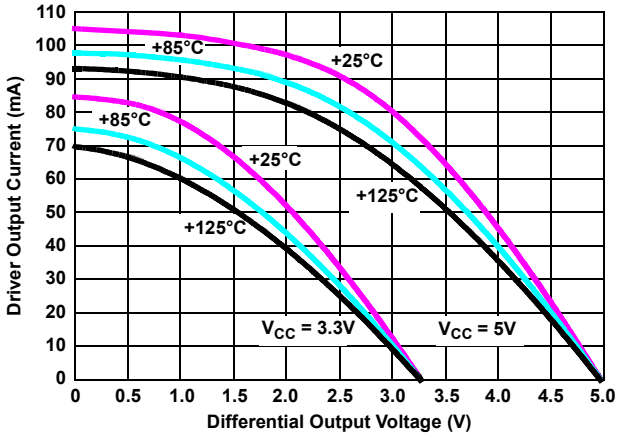


Figure 8. Driver Output Current Vs Differential Output Voltage

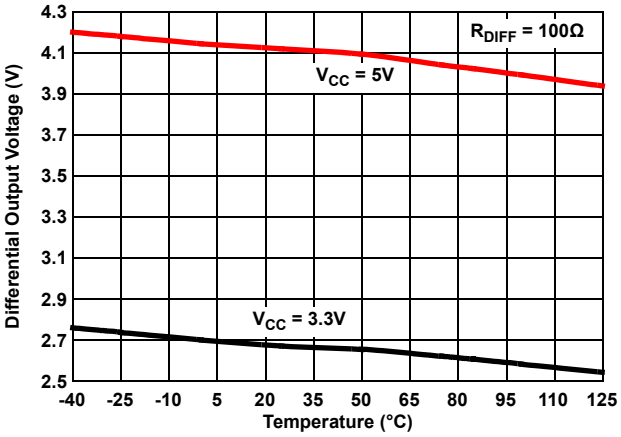


Figure 9. Driver Differential Output Voltage vs Temperature

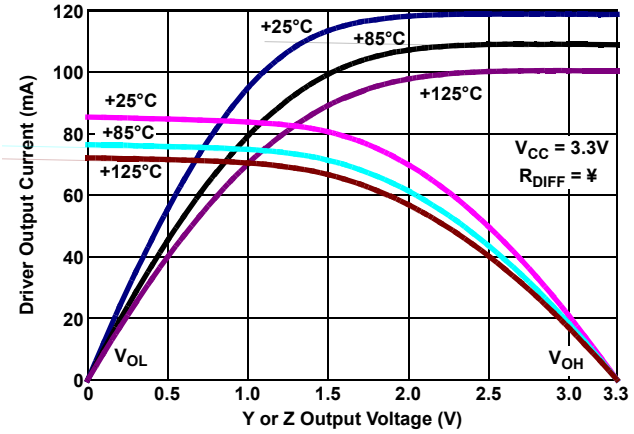


Figure 10. Driver Single-Ended (Y or Z) Output Current vs Output Voltage

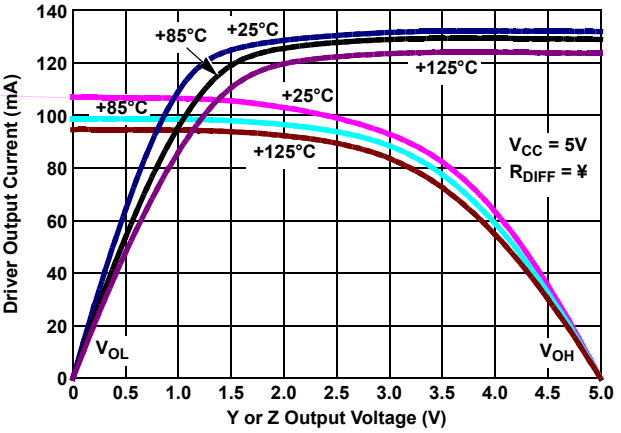


Figure 11. Driver Single-Ended (Y or Z) Output Current vs Output Voltage

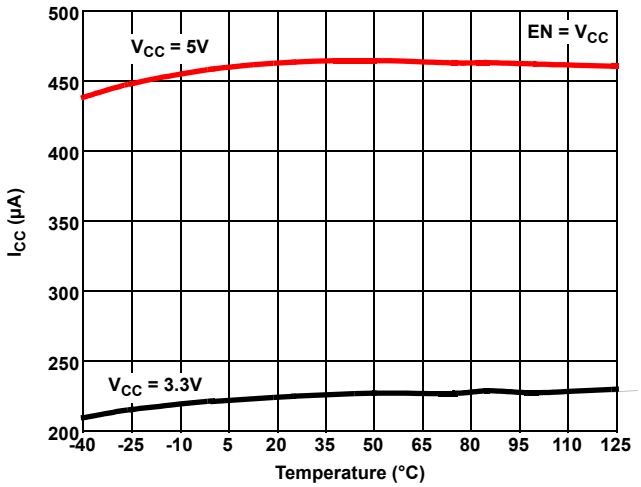


Figure 12. Supply Current vs Temperature

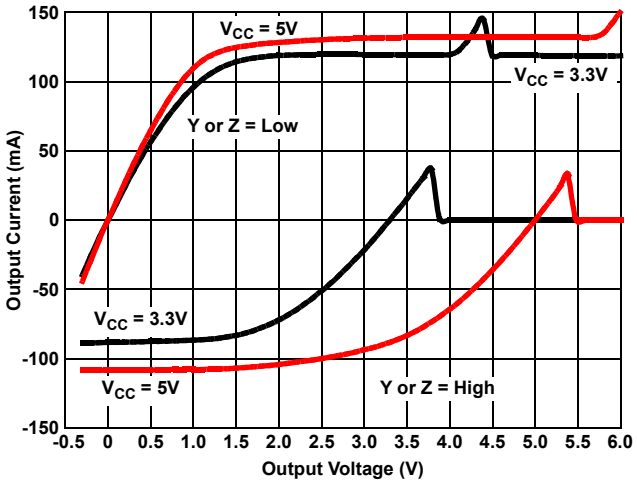


Figure 13. Driver Output Current vs Short-Circuit Voltage

V_{CC} = 3.3V or 5V, T_A = +25°C, unless otherwise specified.

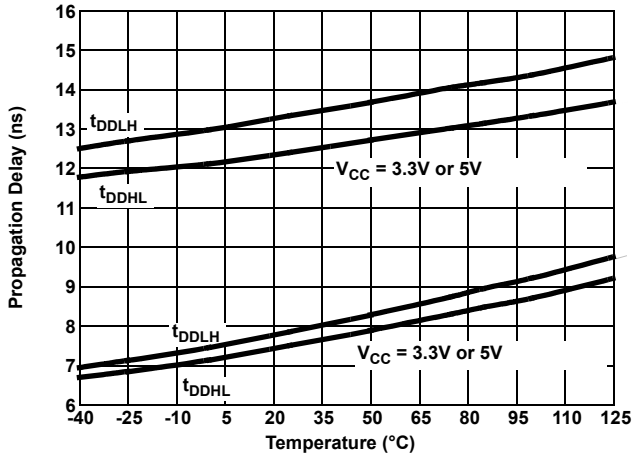


Figure 14. Driver Differential Propagation Delay vs Temperature

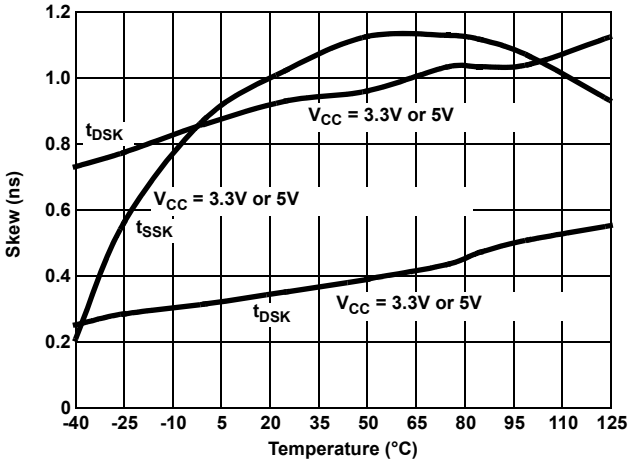


Figure 15. Driver Skew vs Temperature

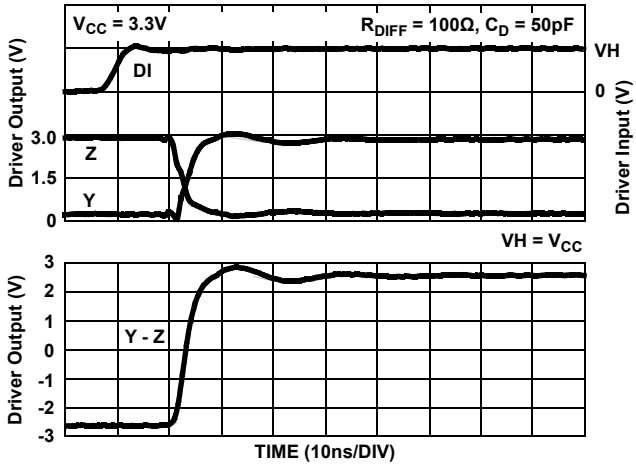


Figure 16. Driver Waveforms, Low to High

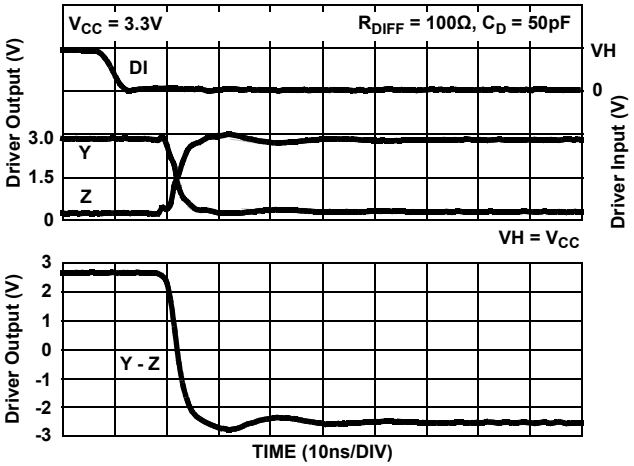


Figure 17. Driver Waveforms, High to Low

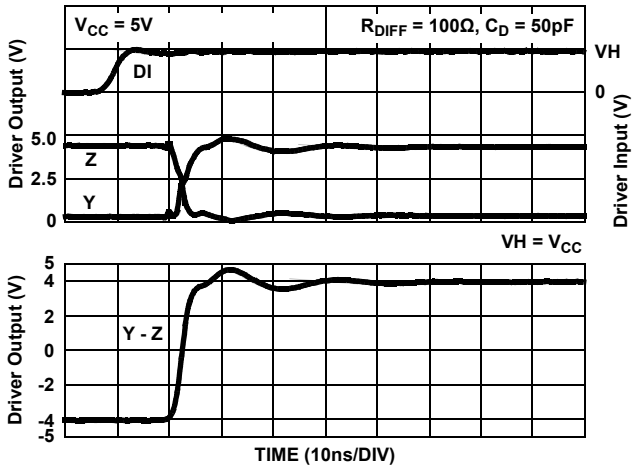


Figure 18. Driver Waveforms, Low to High

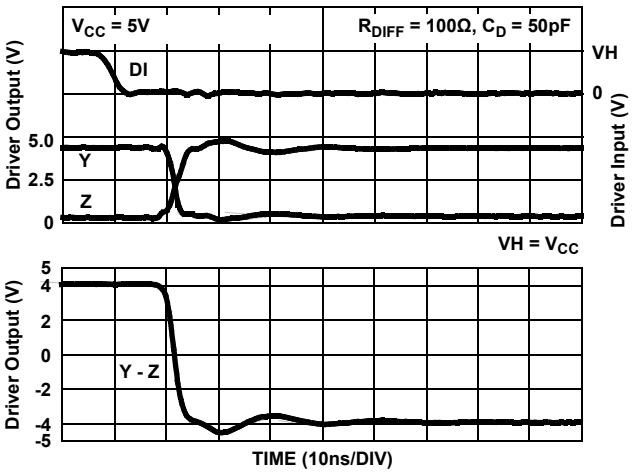


Figure 19. Driver Waveforms, High to Low

V_{CC} = 3.3V or 5V, T_A = +25°C, unless otherwise specified.

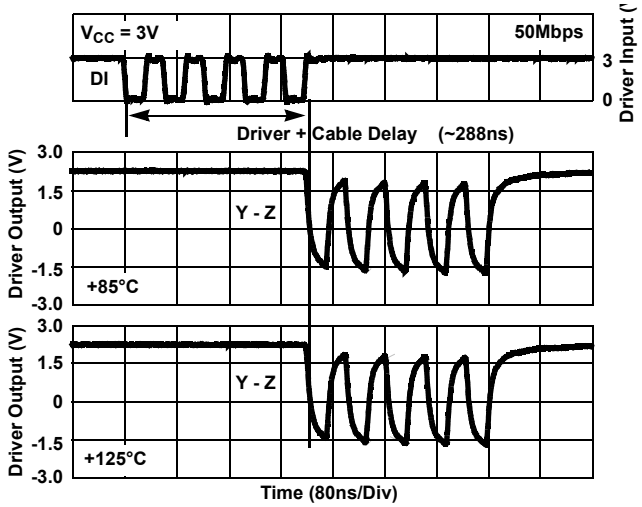


Figure 20. Worst Case (Negative) Five Pulse Driver Waveforms Driving 200 Feet (62m) of Cat5 Cable (Single Terminated with 121Ω)

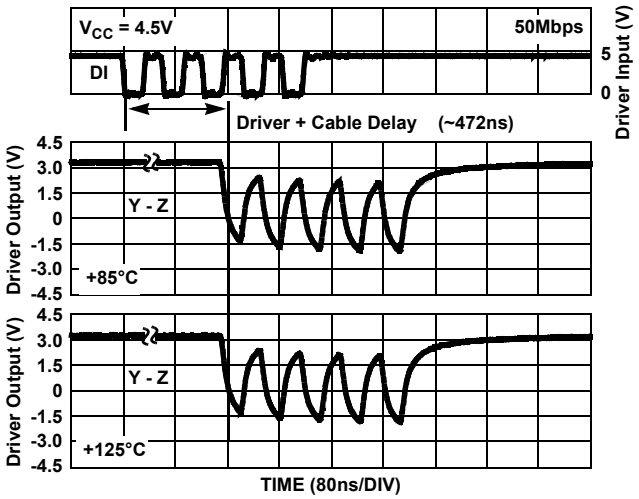


Figure 21. Worst Case (Negative) Five Pulse Driver Waveforms Driving 328 Feet (100m) of Cat5 Cable (Single Terminated with 121Ω)

4. Application Information

RS-422 is a differential (balanced) data transmission standard for use in long haul or noisy environments. RS-422 is a point-to-multipoint (multidrop) standard that allows only one driver and up to 10 receivers on each bus (assuming one unit load devices).

4.1 Driver Features

The RS-422 drivers are differential output devices that deliver at least 2V across a 100Ω load. The drivers feature low propagation delay skew to maximize bit width and minimize EMI.

4.2 Driver Enable Functions

The RAA7884QT feature group (all four Tx) enable functions that are active high (EN) or active low ($\overline{EN}$). Drivers enable when EN = 1 or when $\overline{EN}$ = 0, and they disable only when EN = 0 and $\overline{EN}$ = 1.

4.3 Wide Supply Range

The RAA7884QT is designed to operate with a wide range of supply voltages from 3.0V to 5.5V.

4.3.1 5.5V Tolerant Logic Pins

The logic input pins (driver inputs, enable pins) contain no ESD or parasitic diodes to V_{CC}, so they withstand input voltages exceeding 5.5V regardless of the V_{CC} voltages. Input voltages up to 7V are easily tolerated.

4.4 Hot Plug Function

When a piece of equipment powers up, there is time when the processor or ASIC driving the RS-422 control lines (EN, $\overline{EN}$) is unable to ensure that the RS-422 Tx outputs remain disabled. If the equipment is connected to the bus, a driver activating prematurely during power-up can drive invalid data on the bus. To avoid this scenario, the RAA7884QT incorporates a hot plug function. During power-up, circuitry monitoring V_{CC} ensures that the Tx outputs remain disabled for a while, regardless of the state of the enable pins. The disabled Tx outputs give the processor/ASIC a chance to stabilize and drive the RS-422 control lines to the proper states.

4.5 ESD Protection

The pins on the RAA7884QT include Class 3 (>12kV) Human Body Model (HBM) ESD protection structures, but the RS-422 pins (driver outputs) incorporate advanced structures allowing them to survive ESD events in excess of ±15kV HBM, and ±16.5kV to IEC61000-4-2. The RS-422 pins are particularly vulnerable to ESD damage because they typically connect to an exposed port on the exterior of the finished product. Touching the port pins or connecting a cable can cause an ESD event that could destroy unprotected ICs. The new ESD structures protect the device whether powered up or not and without degrading the RS-422 common-mode range of -0.3V to +6V.

4.6 IEC61000-4-2 Testing

The IEC61000 test method applies to finished equipment rather than to an individual IC, so the pins most likely to suffer an ESD event are those that are exposed to the outside world (the RS-422 pins in this case). Also, the device is tested in its typical application configuration (power applied) rather than testing each pin-to-pin combination. The IEC61000 standard for the lower current limiting resistor coupled with the larger charge storage capacitor yields a test that is more severe than the HBM test. The extra ESD protection, built into the RS-422 pins of the device, allows for the design of equipment to meet a Level 4 criteria without the need for additional board-level protection on the RS-422 port.

4.6.1 Air-Gap Discharge Test Method

For the air-gap discharge test method, a charged probe tip moves toward the IC pin until the voltage arcs to it. The current waveform delivered to the IC pin depends on variables such as approach speed, humidity, and temperature, so it is difficult to obtain repeatable results. The RS-422 pins withstand ±16.5kV air-gap discharges.

4.6.2 Contact Discharge Test Method

During the contact discharge test, the probe contacts the tested pin before the probe tip is energized and eliminates the variables associated with the air-gap discharge. The result is a more repeatable and predictable test, but equipment limits prevent testing devices at voltages higher than ±9kV. The RAA7884QT can survive ±9kV contact discharges on the RS-422 pins.

4.7 Data Rate, Cables, and Terminations

RS-422 is intended for network lengths up to 4000ft, but the maximum system data rate decreases as the transmission length increases. The RAA7884QT operating at 50Mbps handles lengths up to100ft (30m) in 3.3V systems and lengths up to 150ft (45m) in 5V systems.

Use twisted-pair cables for RS-422 networks. Twisted-pair cables tend to pick up noise and other electromagnetically induced voltages as common-mode signals that are effectively rejected by the differential receivers in RS-422 ICs.

Note: Proper termination is imperative to minimize reflections at high data rates.

In point-to-point or multidrop networks, terminate the main cable in its characteristic impedance (typically 100Ω or 120Ω) at the end farthest from the driver. In multidrop applications, keep stubs connecting the receivers to the main cable as short as possible.

4.8 Built-In Driver Overload Protection

The driver output stages incorporate short-circuit current limiting circuitry ensuring that the output current never exceeds the RS-422 specification. A novel design sets the short-circuit current limit depending on the V_{CC} value, so unlike some competing devices, the V_{CC} = 5V short-circuit current is only slightly higher than the corresponding V_{CC} = 3.3V level (see Figure 13).

If a major short-circuit condition occurs, the RAA7884QT thermal shutdown feature disables the drivers whenever the die temperature becomes excessive. Thermal shutdown eliminates the power dissipation and allows the die to cool. The drivers automatically re-enable after the die temperature drops about 20°. If the fault persists, the thermal shutdown/re-enable cycle repeats until the fault is cleared.

4.9 High Temperature Operation

With T_A = +125°C and V_{CC} = 5.5V, four 100Ω differentially terminated drivers put the IC at the edge of its maximum allowed junction temperature. Using larger termination resistors, a lower maximum supply voltage, or one of the packages with a lower thermal resistance (θ_{JA}) provides more safety margin. When designing for +125°C operation, measure the switching current of the application and include it in the thermal calculations.

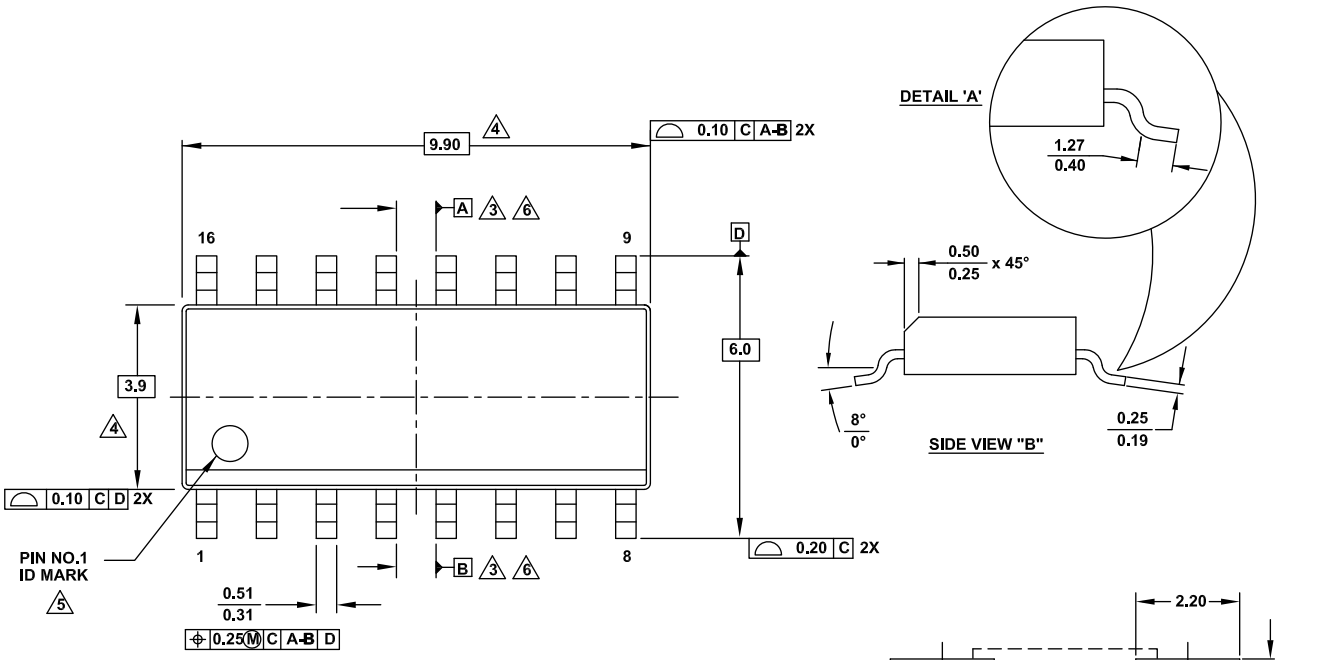
5. Revision History

Rev.	Date	Description
2.00	Oct.14.20	Updated Driver Differential Rise or Fall Time specifications by removing the typical and changing the maximum from 12 to 7.
1.00	Mar.30.20	Initial release

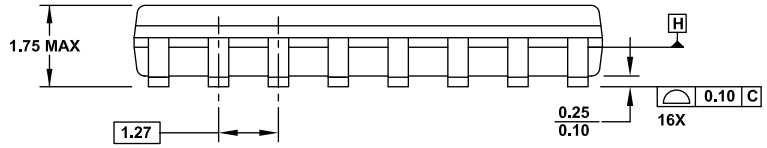
6. Package Outline Drawing

For the most recent package outline drawing, see M16.15.

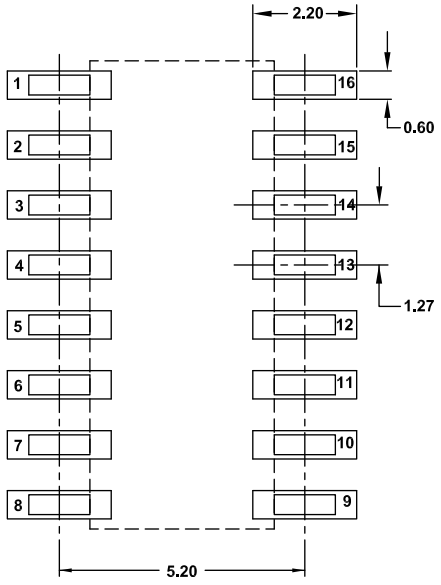
M16.15 (JEDEC MS-012-AC ISSUE C)
16 Lead Narrow Body Small Outline Plastic Package
Rev 2, 11/17



TOP VIEW



SIDE VIEW



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Datums A and B to be determined at Datum H.
4. Dimension does not include interlead flash or protrusions. Interlead flash or protrusions shall not exceed 0.25mm per side.
5. The pin #1 identifier may be either a mold or mark feature.
6. Does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of lead width at maximum condition.
7. Reference to JEDEC MS-012-AC

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