

RAJ306001, RAJ306010

General-Purpose Motor Control IC

1. Overview

RAJ306001 and RAJ306010 are general-purpose motor control ICs for three phase Brushless DC motor applications. RAJ306001 and RAJ306010 combine MCU(RL78/G1F) and a pre-driver in a single package. The pre-driver includes half bridge gate drivers, 5V regulator, a current sense amplifier, hall IC comparators, Back-EMF amplifier, and various protection functions (overtemperature, over/under voltage, overcurrent and the motor lock detection).

Three half bridge gate drivers provide the high efficiency and high flexibility by adjustable gate drive peak current (500mA), self-align dead time generator, selectable gate drive voltage, and control signal configuration function. Self-align dead time generator prevents the short-through current and provides the safe evaluation environment.

MCU supports H/W of the safe standard of IEC60730. The development tools of the RL78 family are available. This IC can realize the suitable motor control and performance corresponding to each application by F/W construction and optimization of register settings.

2. Features

- Operating Power Supply Voltage
 - RAJ306001: 6V to 30V, RAJ306010: 6V to 42V
- Operating Ambient Temperature
 - RAJ3060xxGNP = -40 to +85°C
 - RAJ3060xxZGNP = -40 to +105°C
- Low VM Supply Current
 - [MCU]: 5.2mA (HS mode: $f_{IH} = 32\text{MHz}$, $V_{DD} = 5\text{V}$)
 - [Pre-Driver]: 13.5mA ($V_M = 22.5\text{V}$)
 - VM standby current: 64 μA (Typ.)
- GPIO: 28ch, Port for Input: 2ch

Pre-Driver Function

- Three Half-Bridge Gate Drivers for six N-MOSFET
 - Adjustable Gate Drive Peak current up to 500mA
 - Self-Align Dead Time Generator Function
 - Control Signal Configuration Function for flexibility
- Selectable Single/Double Boost Charge Pump for Gate Drive Voltage (10, 13V)
- Support Hall IC type and Hall Sensor-less type
 - Integrated Hall IC Comparators (adjustable threshold and hysteresis voltage)
- Integrated 1 Shunt Current Sense Amplifier
 - Adjustable Gain (8.25, 25, 50V/V)
- Integrated Protection function:
 - UVLO, Overtemperature, Overcurrent, Overvoltage,
 - Motor Lock for Hall IC type, Alarm Condition Indicator feature

Controller Function

- CPU: 16-bit CISC CPU (RL78/G1F)
- Flash ROM: 64KB, Data Flash: 4KB
- RAM: 5.5KB
- CSI: 2Channel ---- SPI:2ch, IIC:2ch, UART:1ch
- Timer
 - Timer Array Unit: 1unit ----- 16-bit, 4ch
 - Timer RD for motor control ----- 16-bit, 2ch
 - Timer RG with encoding function – 16-bit, 1ch
 - 64 MHz motor control input capture timer
 - (Timer RX)
- 10-bit resolution A/D Converter: 9ch
- Selectable Reference Voltage: Internal/External
- Event Link Controller (ELC): 6ch (External Input)

3. Applications

- Power Tools, Garden Tools, and Vacuum Cleaners
- Printers, Fans, Pumps, and Robotics

Note: With this data sheet, Renesas recommends to read “RAJ306000 Series User’s Manual: Hardware (R18UZ0066EJ)” to understand deeply. And about detail spec on RL78/G1F, please see “RL78/G1F User’s manual: Hardware (R01UH0516EJ)”. This product has some restriction on function. So please check it on “CHAPTER3 RL78/G1F” in “RAJ306000 Series User’s Manual:Hardware (R18UZ0066EJ)”. And on the electrical characteristics of RL78/G1F, please substitute EVDD0/VDD value to $4.75 \leq \text{EVDD0/VDD} \leq 5.25\text{V}$.

4. Ordering Information

| Part Number | Operating Voltage | Temperature Range | Package |
|---------------|-------------------|-------------------|-----------------------|
| RAJ306001GNP | 6V to 30V | -40°C to +85°C | 64pin QFN (8mm x 8mm) |
| RAJ306001ZGNP | | -40°C to +105°C | |
| RAJ306010GNP | 6V to 42V | -40°C to +85°C | |
| RAJ306010ZGNP | | -40°C to +105°C | |

Contents

| | |
|--|-----------|
| 1. Overview | 1 |
| 2. Features | 1 |
| 3. Applications | 1 |
| 4. Ordering Information | 2 |
| 5. Block Diagram | 4 |
| 6. Pin Configuration | 5 |
| 7. Pin Description | 6 |
| 8. Electrical Characteristics | 8 |
| 8.1 Absolute Maximum Rating for RAJ306001 ^{Note1} | 8 |
| 8.2 Recommended Operating Conditions | 13 |
| 8.3 Electrical Characteristics | 14 |
| 9. External Circuit | 16 |
| 10. Block Explanation | 18 |
| 10.1 Power ON Sequence | 18 |
| 10.2 Serial Array Unit | 20 |
| 10.3 CSI timing specification | 21 |
| 10.4 CSI Communication Format | 22 |
| 11. Control Register Map | 23 |
| 12. Package Description | 24 |
| 13. Revision History | 25 |

5. Block Diagram

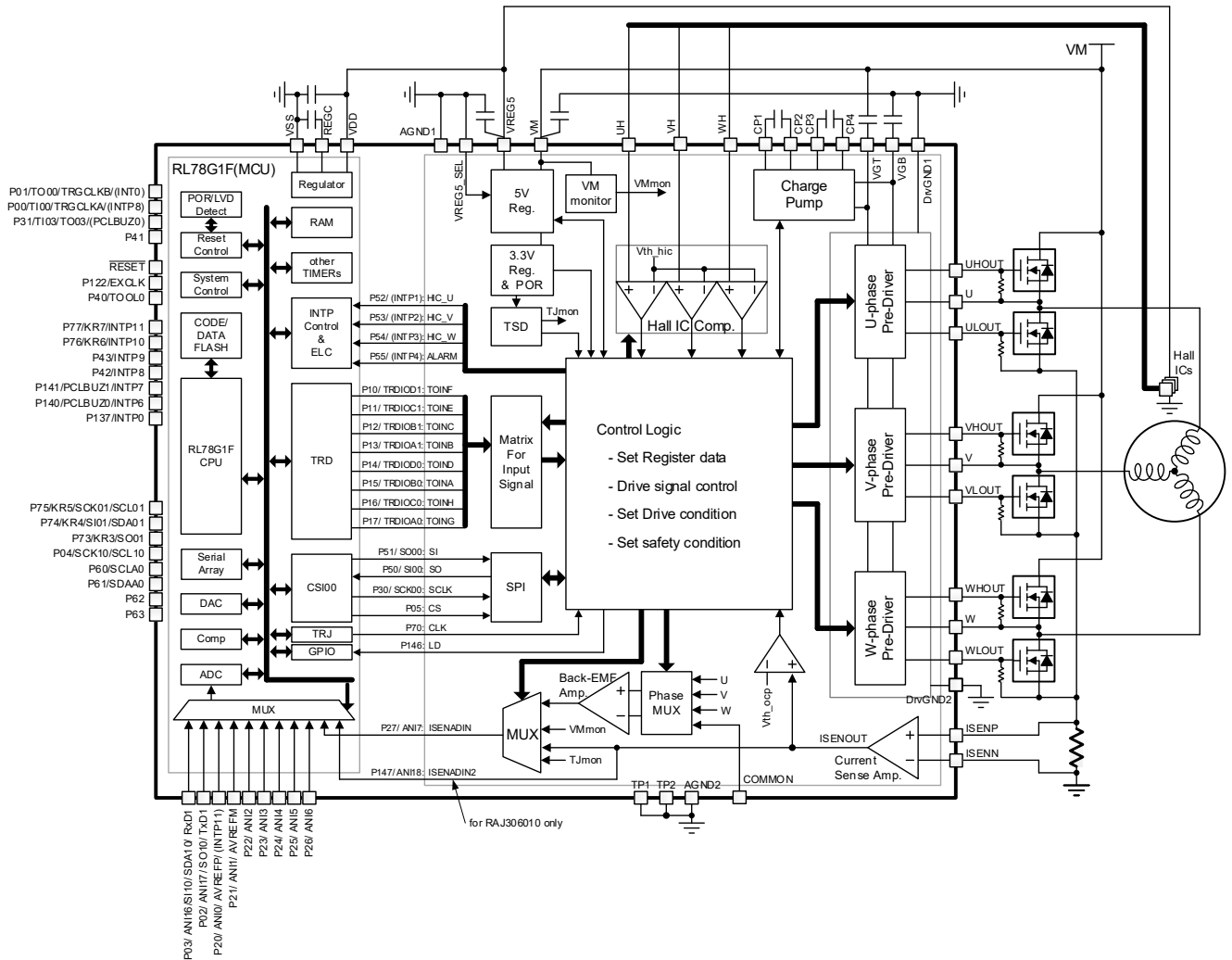


Figure 4-1. Block Diagram (Hall IC type)

- GPIO terminal: 28ch
(Include ADC:9ch & Terminal for External interrupt: 7ch)
- Input terminal: 2ch
 - *1) PIOR00 = 01 [Setting required]
 - *2) SSIE00 = 0 [Setting required] ----Invalidation of SSI00

6. Pin Configuration

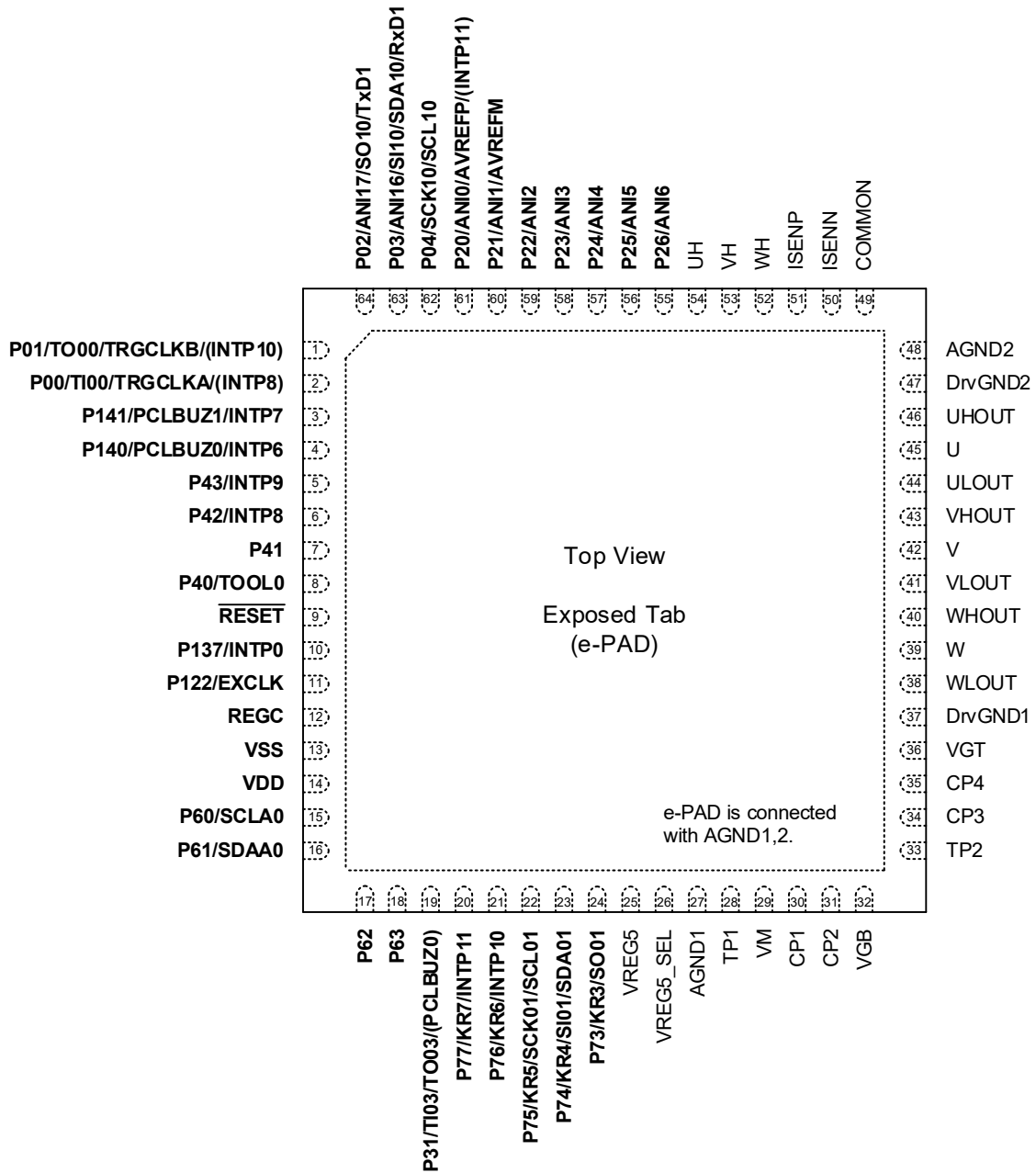


Figure 5-1. Pin configuration diagram

Note: RL78/G1F pins are indicated with the bold font.

7. Pin Description

Table 6-1. Pin description

| PIN | | Alternate Function | I/O level | IN/OUT or Power/GND | Initial Condition | Function | Remarks |
|--------|-----------|----------------------------|-----------|---------------------|-------------------|---|---------|
| Number | Name | | | | | | |
| 1 | P01 | TO00/ TRGCLKB/ (INTP10) | VDD | IN/OUT | INPUT | GPIO / TAU output / TRG external clock input / (External interrupt input) | 1 |
| 2 | P00 | T100/ TRGCLK/ (INTP8) | VDD | IN/OUT | INPUT | GPIO / TAU Input / TRG external clock input / (External interrupt input) | 1 |
| 3 | P141 | PCLBUZ1/ INTP7 | VDD | IN/OUT | INPUT | GPIO / Programmable clock output / External interrupt input | 1 |
| 4 | P140 | PCLBUZ0/ INTP6 | VDD | IN/OUT | INPUT | GPIO / Programmable clock output / External interrupt input | 1 |
| 5 | P43 | INTP9 | VDD | IN/OUT | INPUT | GPIO / INTP9 | 1 |
| 6 | P42 | INTP8 | VDD | IN/OUT | INPUT | GPIO / INTP8 | 1 |
| 7 | P41 | - | VDD | IN/OUT | INPUT | GPIO | 1 |
| 8 | P40 | TOOL0 | VDD | IN/OUT | INPUT | GPIO / TOOL0 for E1 on-chip debugging | 1 |
| 9 | RESET | - | VDD | - | INPUT | External Reset of RL78 | 1 |
| 10 | P137 | INTP0 | VDD | IN/OUT | INPUT | Only input / INTP0 | 1 |
| 11 | P122 | EXCLK | VDD | IN/OUT | INPUT | Only input / Input of Main clock from External | 1 |
| 12 | REGC | - | VDD | - | - | Pin for connecting regulator output stabilization capacitance for internal operation of MCU. | 1 |
| 13 | VSS | - | VDD | GND | | Ground potential for MCU | 1 |
| 14 | VDD | - | VDD | Power | | Positive power supply for MCU | 1 |
| 15 | P60 | SCLA0 | VDD | IN/OUT | INPUT | GPIO / Serial clock I/O pins of serial interface IICA0 | 1 |
| 16 | P61 | SDAA0 | VDD | IN/OUT | INPUT | GPIO / Serial data I/O pins of serial interface IICA0 | 1 |
| 17 | P62 | - | VDD | IN/OUT | INPUT | GPIO / Chip select input pin of serial interface CSI00 [*2] | 1 |
| 18 | P63 | - | VDD | IN/OUT | INPUT | GPIO | 1 |
| 19 | P31 | T103/ T003/ (PCLBUZ0) | VDD | IN/OUT | INPUT | GPIO / TAU input / TAU output / (Output clock, Buzzer output) | 1 |
| 20 | P77 | KR7/ INTP11 | VDD | IN/OUT | INPUT | GPIO / KR7 / INTP11 | 1 |
| 21 | P76 | KR6/ INTP10 | VDD | IN/OUT | INPUT | GPIO / KR6 / INTP10 | 1 |
| 22 | P75 | KR5/ SCK01/ SCL01 | VDD | IN/OUT | INPUT | GPIO / KR5 / Serial clock I/O pins of CSI01 / Serial clock output pins of IIC01 | 1 |
| 23 | P74 | KR4/ SI01/ SDA01 | VDD | IN/OUT | INPUT | GPIO / KR4 / Serial data input pins of CSI01 / Serial data I/O pins of IIC01 | 1 |
| 24 | P73 | KR3/ SO01 | VDD | IN/OUT | INPUT | GPIO / KR3 / Serial data output pins of CSI01 | 1 |
| 25 | VREG5 | - | VREG5(5V) | IN/OUT | IN/OUT | VREG5 pin function depends on VREG5_SEL VREG5_SEL=GND: Built-in 5V regulator is selected. (Output 5V) VREG5_SEL=5V: External 5V regulator is selected. (Input 5V) | |
| 26 | VREG5_SEL | - | VREG5 | INPUT | INPUT | | |
| 27 | AGND1 | - | GND | GND | GND | Ground potential 1 for analog and logic circuits of Pre-Driver | |
| 28 | TP1 | - | VREG5 | INPUT | INPUT | Terminal for Test. (Usually connect to GND) | |
| 29 | VM | - | VM | POWER | POWER | Power Supply input | |
| 30 | CP1 | - | VGB | - | - | Charge pump Pin 1 (CP1) | |
| 31 | CP2 | - | VGB | - | - | Charge pump Pin 2 (CP2) | |
| 32 | VGB | - | VGB | OUTPUT | OUTPUT | Gate drive voltage for Low-side | |

1: RL78/G1F terminal. Please refer to "RL78/G1F User's Manual: Hardware" (R01UH0516EJ) about Terminal function of RL78/G1F. This product has some restriction on function. So please check it on "CHAPTER3 RL78/G1F" in "RAJ306000 Series User's Manual: Hardware (R18UZ0066EJ)".

*2: The nullification of the /SSI00 function is necessary.

Table 6-2. Pin description (continued)

| PIN | | Alternate Function | I/O level | IN/OUT or Power/GND | Initial Condition | Function | Remarks |
|--------|---------|-----------------------------|-----------|---------------------|-------------------|--|---------|
| Number | Name | | | | | | |
| 33 | TP2 | - | VREG5 | INPUT | INPUT | Terminal for Test. (Usually connect to GND) | |
| 34 | CP3 | - | VM | - | - | Charge pump Pin 3 (CP3) | |
| 35 | CP4 | - | VGT | - | - | Charge pump Pin 4 (CP4) | |
| 36 | VGT | - | VGT | OUTPUT | OUTPUT | Gate drive voltage for High-side | |
| 37 | DrvGND1 | - | GND | GND | GND | Ground potential 1 for driving circuits of Pre-Driver | |
| 38 | WLOUT | - | VGB | OUTPUT | OUTPUT | Output of Pre-driver for W phase Low-side (Nch MOSFET) | |
| 39 | W | - | VM | INPUT | INPUT | Detection of BEMF level for W phase | |
| 40 | WHOUT | - | VGT | OUTPUT | OUTPUT | Output of Pre-driver for W phase High-side (Nch MOSFET) | |
| 41 | VLOUT | - | VGB | OUTPUT | OUTPUT | Output of Pre-driver for V phase Low-side (Nch MOSFET) | |
| 42 | V | - | VM | INPUT | INPUT | Detection of BEMF level for V phase | |
| 43 | VHOUT | - | VGT | OUTPUT | OUTPUT | Output of Pre-driver for V phase High-side (Nch MOSFET) | |
| 44 | ULOUT | - | VGB | OUTPUT | OUTPUT | Output of Pre-driver for U phase Low-side (Nch MOSFET) | |
| 45 | U | - | VM | INPUT | INPUT | Detection of BEMF level for U phase | |
| 46 | UHOUT | - | VGT | OUTPUT | OUTPUT | Output of Pre-driver for U phase High-side (Nch MOSFET) | |
| 47 | DrvGND2 | - | GND | GND | GND | Ground potential 2 for driving circuits of Pre-Driver | |
| 48 | AGND2 | - | GND | GND | GND | Ground potential 2 for analog and logic circuits of Pre-Driver | |
| 49 | COMMON | - | VM | INPUT | INPUT | Input for Common signal of Motor | |
| 50 | ISENN | - | VREG5 | INPUT | INPUT | Connect Negative side of Shunt resistor | |
| 51 | ISENP | - | VREG5 | INPUT | INPUT | Connect Positive side of Shunt resistor | |
| 52 | WH | - | VREG5 | IN/OUT | INPUT | Input of Hall IC signal for W phase/ Output BEMF AMP Signal (RAJ306010 Only) | 3 |
| 53 | VH | - | VREG5 | INPUT | INPUT | Input of Hall IC signal for V phase | |
| 54 | UH | - | VREG5 | INPUT | INPUT | Input of Hall IC signal for U phase | |
| 55 | P26 | ANI6 | VDD | IN/OUT | ANALOG | GPIO / ADC analog input | 1 |
| 56 | P25 | ANI5 | VDD | IN/OUT | ANALOG | GPIO / ADC analog input | 1 |
| 57 | P24 | ANI4 | VDD | IN/OUT | ANALOG | GPIO / ADC analog input | 1 |
| 58 | P23 | ANI3 | VDD | IN/OUT | ANALOG | GPIO / ADC analog input / DAC output / PGA reference voltage input | 1 |
| 59 | P22 | ANI2 | VDD | IN/OUT | ANALOG | GPIO / ADC analog input / DAC output / PGA voltage input | 1 |
| 60 | P21 | ANI1/ AVREFM | VDD | IN/OUT | ANALOG | GPIO / ADC analog input / ADC reference(- side) input | 1 |
| 61 | P20 | ANI0/ AVREFP/ (INTP11) | VDD | IN/OUT | ANALOG | GPIO / ADC analog input / ADC reference (+ side) input / (External interrupt input) | 1 |
| 62 | P04 | SCK10/ SCL10 | VDD | IN/OUT | ANALOG | GPIO / Serial clock I/O pins of CSI10 / Serial clock output pins of IIC10 | 1 |
| 63 | P03 | ANI16/ SI10/ SDA10/ RXD1 | VDD | IN/OUT | ANALOG | GPIO / ADC analog input / Serial data input pins of CSI10 / Serial data I/O pins of IIC10 / Serial data output pins of UART | 1 |
| 64 | P02 | ANI17/ SO10/ TXD1 | VDD | IN/OUT | ANALOG | GPIO / ADC analog input / Serial data output pins of CSI10 / Serial data output pins of UART | 1 |

*1: The following pins of RL78/G1F are used for internal connection. P05, P06, P10-17, P27, P30, P50-55, P146, P147

*3: The Hall signal input function is available on both RAJ306001 and RAJ306010. The output function of BEMF AMP Signal is available only for RAJ306010.

8. Electrical Characteristics

8.1 Absolute Maximum Rating for RAJ306001 Note1

| Item | Symbol | Rating | unit | Note |
|---|------------|--|---------|---|
| Power dissipation | Pd | 5840 | mW | This spec is applied for HWQFN64. |
| Thermal derating | K θ | -46.7 | mW/degC | This spec is applied for HWQFN64. Condition: refer to P.10 |
| Power supply for motor drive | VM | -0.3 to +60 | V | Refer to Note2 |
| Power supply | VDD | - 0.3 to +6.5 | V | Pin: VDD (MCU) |
| REGC terminal input voltage | VIREGC | -0.3 to +2.8 | V | Pin: REGC Note3 |
| VREG5 terminal input voltage | VVREG5 | -0.3 to +6.5 | V | Pin: VREG5 |
| VGT output voltage range | VVGT | -0.3 to +48.0 | V | Pin :VGT |
| CP4 terminal voltage range | VCP4 | -0.3 to +48.0 | V | Pin :CP4 |
| CP3 terminal voltage range | VCP3 | -0.3 to +48.0 | V | Pin :CP3 |
| VGB output voltage range | VVGB | -0.3 to +18.0 | V | Pin :VGB |
| CP2 terminal voltage range | VCP2 | -0.3 to +18.0 | V | Pin :CP2 |
| CP1 terminal voltage range | VCP1 | -0.3 to +18.0 | V | Pin :CP1 |
| UHOUT, VHOUT, WHOOUT constant output voltage range 1 | VH_OUT1 | -1.0 to +48.0 | V | Pin :UHOUT, VHOUT, WHOOUT |
| UHOUT, VHOUT, WHOOUT peak output voltage range 2 | VH_OUT2 | -8.0 to +48.0 | V | Pin :UHOUT, VHOUT, WHOOUT Note6 |
| U, V, W, COMMON constant output voltage range 1 | Vphase1 | -1.0 to +48.0 | V | Pin :U, V, W, COMMON |
| U, V, W, COMMON peak output voltage range 2 | Vphase2 | -8.0 to +48.0 | V | Pin :U, V, W, COMMON Note6 |
| ULOUT, VLOUT, WLOUT output voltage range | VL_OUT | -0.5 to +18.0 | V | Pin :ULOUT, VLOUT, WLOUT |
| Sense current terminal | ISEN | -0.3 to VREG5 + 0.3 | V | Pin : ISENP, ISENN |
| Digital terminal Input voltage range | DVIN1 | -0.3 to VDD + 0.3 | V | Pin :P00 to P04, P20~P26, P31, P40 to P43, P73 to P77, P122, P137, P140, P141, EXCLK, /RESET, Note4 |
| | DVIN2 | -0.3 to +6.5 | V | Pin: P60 to P63 (Nch open-drain) |
| Output Voltage | DVOUT | -0.3 to VDD+0.3 | V | Pin: P00 to P04, p20 to P26, P31, P40 to P43, P73 to P77, P140, P141, Note4 |
| Analog input voltage | AVIN1 | -0.3 to VDD + 0.3 and -0.3 to AVREFF + 0.3 | V | Pin: ANI0 to ANI6, ANI16, ANI17 Note4,5 |
| | AVIN2 | -0.3 to VREG5 + 0.3 | V | Pin :VREG5_SEL, TP1, TP2 |
| Hall sensor input terminal voltage | HVIN | -0.3 to VREG5 + 0.3 | V | Pin : UH, VH, WH |

Note1: Not subject to production test, specified at Ta=25degC by design

Note2: Please do not apply the voltage more than 48V to VM terminal more than 1us.

In addition, when the VM voltage is as above 48V at DC level, the surge protective circuit of this IC works, and the applied voltage is clamped.

Note3: Connect the REGC pin to VSS via a capacitor (0.47 to 1uF). This value regulates the absolute maximum rating of REGC pin.

Do not use this pin with voltage applied to it.

Note4: Must be 6.5 V or lower.

Note5: Do not exceed AVREFF +0.3 V in case of A/D conversion target pin.

Note6: This value is for design only and the condition is (PWM period = 20KHz) and (Negative period = 150nsec).

When there is some possibility to exceed the maximum ratings, please investigate to add protection circuit written in "8. External Circuit".

Note7: This value is for design only and the condition is (PWM period = 20KHz) and (Period = 1usec). Do not use beyond the rating.

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Absolute Maximum Rating for RAJ306001 (continued)

Note1

| Item | Symbol | Rating | unit | Note |
|--|--------|-------------|-------------|--|
| Digital output current of High level 1 | DIOH1 | -40 | mA/Terminal | Pin :P00 to P04, P31, P40 to P43, P73 to P77, P140, P141 |
| | | -70 | mA/Total | Pin : P00 to P04, P40 to P43, P140, P141 |
| | | -100 | mA/Total | Pin :P31, P73 to P77 |
| Digital output current of High level 2 | DIOH2 | -0.5 | mA/Terminal | Pin : P20 to P26 (Total current of these terminals: 1.7mA) |
| Digital output current of Low level 1 | DIOL1 | +40 | mA/Terminal | Pin :P00 to P04, P31, P40 to P43, P60 to P63, P73 to P77, P140, P141 |
| | | +70 | mA/Total | Pin :P00 to P04, P40 to P43, P140, P141 |
| | | +100 | mA/Total | Pin :P31, P73 to P77 |
| Digital output current of Low level 2 | DIOL2 | +1 | mA/Terminal | Pin : P20 to P26 (Total current of their terminal: 4.3mA) |
| Maximum junction temperature | Tj | +150 | degC | Pre-Driver chip |
| Operating temperature (Normal Operation) | Tope1 | -40 to +85 | degC | RAJ306001GNP |
| | | -40 to +105 | | RAJ306001ZGNP |
| Operating temperature (at Flash Memory Programming) | Tope2 | -40 to +85 | degC | RAJ306001GNP |
| | | -40 to +105 | | RAJ306001ZGNP |
| Storage temperature | Tstg | -65 to +150 | degC | |

Note1: Not subject to production test, specified at Ta=25degC by design

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark1: Unless specified otherwise, the characteristics of alternate-function pins are same as those of the port pins.

Remark2: AVREFP: positive side reference voltage of the A/D converter.

Remark3: GND pins: Drive block: DrvGND1, DrvGND2, Analog block: AGND1, AGND2
VSS pin: VSS (MCU)

Absolute Maximum Rating for RAJ306010 ^{Note1}

| Item | Symbol | Rating | unit | Note |
|--|------------|--|---------|---|
| Power dissipation | Pd | 5840 | mW | This spec is applied for HWQFN64. |
| Thermal derating | K θ | -46.7 | mW/degC | This spec is applied for HWQFN64. Condition: refer to P.10 |
| Power supply for motor drive | VM | -0.3 to +60 | V | Refer to Note2 |
| Power supply | VDD | -0.3 to +6.5 | V | Pin: VDD (MCU) |
| REGC terminal input voltage | VIREGC | -0.3 to +2.8 | V | Pin: REGC Note3 |
| VREG5 terminal input voltage | VIVREG5 | -0.3 to +6.5 | V | Pin: VREG5 |
| VGT output voltage range | VVGT | -0.3 to +48.0 | V | Pin :VGT |
| CP4 terminal voltage range | VCP4 | -0.3 to +48.0 | V | Pin :CP4 |
| CP3 terminal voltage range | VCP3 | -0.3 to +48.0 | V | Pin :CP3 |
| VGB output voltage range | VVGB | -0.3 to +18.0 | V | Pin :VGB |
| CP2 terminal voltage range | VCP2 | -0.3 to +18.0 | V | Pin :CP2 |
| CP1 terminal voltage range | VCP1 | -0.3 to +18.0 | V | Pin :CP1 |
| UHOUT, VHOUT, WHOUT constant output voltage range 1 | VH_OUT1 | -1.0 to +48.0 | V | Pin :UHOUT, VHOUT, WHOUT |
| UHOUT, VHOUT, WHOUT peak output voltage range 2 | VH_OUT2 | -8.0 to +48.0 | V | Pin :UHOUT, VHOUT, WHOUT Note6 |
| U, V, W, COMMON constant output voltage range 1 | Vphase1 | -1.0 to +48.0 | V | Pin :U, V, W, COMMON |
| U, V, W, COMMON peak output voltage range 2 | Vphase2 | -8.0 to +48.0 | V | Pin :U, V, W, COMMON Note6 |
| ULOUT, VLOUT, WLOUT output voltage range | VL_OUT | -0.5 to +18.0 | V | Pin :ULOUT, VLOUT, WLOUT |
| Sense current terminal | ISEN | -0.3 to VREG5 + 0.3 | V | Pin : ISENP, ISENN |
| Digital terminal Input voltage range | DVIN1 | -0.3 to VDD + 0.3 | V | Pin :P00 to P04, P20~P26, P31, P40 to P43, P73 to P77, P122, P137, P140, P141, EXCLK, /RESET, Note4 |
| | DVIN2 | -0.3 to +6.5 | V | Pin: P60 to P63 (Nch open-drain) |
| Output Voltage | DVOUT | -0.3 to VDD+0.3 | V | Pin: P00 to P04, p20 to P26, P31, P40 to P43, P73 to P77, P140, P141, Note4 |
| Analog input voltage | AVIN1 | -0.3 to VDD + 0.3 and -0.3 to AVREFP + 0.3 | V | Pin: ANI0 to ANI6, ANI16, ANI17 Note4,5 |
| | AVIN2 | -0.3 to VREG5 + 0.3 | V | Pin :VREG5_SEL, TP1, TP2 |
| Hall sensor input terminal voltage | HVIN | -0.3 to VREG5 + 0.3 | V | Pin : UH, VH, WH |

Note1: Not subject to production test, specified at Ta=25degC by design

Note2: Please do not apply the voltage more than 48V to VM terminal more than 1us. In addition, when the VM voltage is as above 48V at DC level, the surge protective circuit of this IC works, and the applied voltage is clamped.

Note3: Connect the REGC pin to VSS via a capacitor (0.47 to 1uF). This value regulates the absolute maximum rating of REGC pin. Do not use this pin with voltage applied to it.

Note4: Must be 6.5 V or lower.

Note5: Do not exceed AVREFP +0.3 V in case of A/D conversion target pin.

Note6: This value is for design only and the condition is (PWM period = 20KHz) and (Negative period = 150nsec).

When there is some possibility to exceed the maximum ratings, please investigate to add protection circuit written in "8. External Circuit".

Note7: This value is for design only and the condition is (PWM period = 20KHz) and (Period = 1usec). Do not use beyond the rating.

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter

That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Absolute Maximum Rating for RAJ306010 (continued) Note1

| Item | Symbol | Rating | unit | Note |
|--|------------|--|---------|---|
| Power dissipation | Pd | 5840 | mW | This spec is applied for HWQFN64. |
| Thermal derating | K θ | -46.7 | mW/degC | This spec is applied for HWQFN64. Condition: refer to P.10 |
| Power supply for motor drive | VM | -0.3 to +60 | V | Refer to Note2 |
| Power supply | VDD | -0.3 to +6.5 | V | Pin: VDD (MCU) |
| REGC terminal input voltage | VIREGC | -0.3 to +2.8 | V | Pin: REGC Note3 |
| VREG5 terminal input voltage | VIVREG5 | -0.3 to +6.5 | V | Pin: VREG5 |
| VGT output voltage range | VVGT | -0.3 to +48.0 | V | Pin :VGT |
| CP4 terminal voltage range | VCP4 | -0.3 to +48.0 | V | Pin :CP4 |
| CP3 terminal voltage range | VCP3 | -0.3 to +48.0 | V | Pin :CP3 |
| VGB output voltage range | VVGB | -0.3 to +18.0 | V | Pin :VGB |
| CP2 terminal voltage range | VCP2 | -0.3 to +18.0 | V | Pin :CP2 |
| CP1 terminal voltage range | VCP1 | -0.3 to +18.0 | V | Pin :CP1 |
| UHOUT, VHOUT, WHOUT constant output voltage range 1 | VH_OUT1 | -1.0 to +48.0 | V | Pin :UHOUT, VHOUT, WHOUT |
| UHOUT, VHOUT, WHOUT peak output voltage range 2 | VH_OUT2 | -8.0 to +48.0 | V | Pin :UHOUT, VHOUT, WHOUT Note6 |
| U, V, W, COMMON constant output voltage range 1 | Vphase1 | -1.0 to +48.0 | V | Pin :U, V, W, COMMON |
| U, V, W, COMMON peak output voltage range 2 | Vphase2 | -8.0 to +48.0 | V | Pin :U, V, W, COMMON Note6 |
| ULOUT, VLOUT, WLOUT output voltage range | VL_OUT | -0.5 to +18.0 | V | Pin :ULOUT, VLOUT, WLOUT |
| Sense current terminal | ISEN | -0.3 to VREG5 + 0.3 | V | Pin : ISENP, ISENN |
| Digital terminal Input voltage range | DVIN1 | -0.3 to VDD + 0.3 | V | Pin :P00 to P04, P20~P26, P31, P40 to P43, P73 to P77, P122, P137, P140, P141, EXCLK, /RESET, Note4 |
| | DVIN2 | -0.3 to +6.5 | V | Pin: P60 to P63 (Nch open-drain) |
| Output Voltage | DVOUT | -0.3 to VDD+0.3 | V | Pin: P00 to P04, p20 to P26, P31, P40 to P43, P73 to P77, P140, P141, Note4 |
| Analog input voltage | AVIN1 | -0.3 to VDD + 0.3 and -0.3 to AVREFP + 0.3 | V | Pin: ANI0 to ANI6, ANI16, ANI17 Note4,5 |
| | AVIN2 | -0.3 to VREG5 + 0.3 | V | Pin :VREG5_SEL, TP1, TP2 |
| Hall sensor input terminal voltage | HVIN | -0.3 to VREG5 + 0.3 | V | Pin : UH, VH, WH |

Note1: Not subject to production test, specified at Ta=25degC by design

Note2: Please do not apply the voltage more than 48V to VM terminal more than 1us.

In addition, when the VM voltage is as above 48V at DC level, the surge protective circuit of this IC works, and the applied voltage is clamped.

Note3: Connect the REGC pin to VSS via a capacitor (0.47 to 1uF). This value regulates the absolute maximum rating of REGC pin. Do not use this pin with voltage applied to it.

Note4: Must be 6.5 V or lower.

Note5: Do not exceed AVREFP +0.3 V in case of A/D conversion target pin.

Note6: This value is for design only and the condition is (PWM period = 20KHz) and (Negative period = 150nsec).

When there is some possibility to exceed the maximum ratings, please investigate to add protection circuit written in "8. External Circuit".

Note7: This value is for design only and the condition is (PWM period = 20KHz) and (Period = 1usec). Do not use beyond the rating.

Caution: Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter

That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Absolute Maximum Rating (continued)

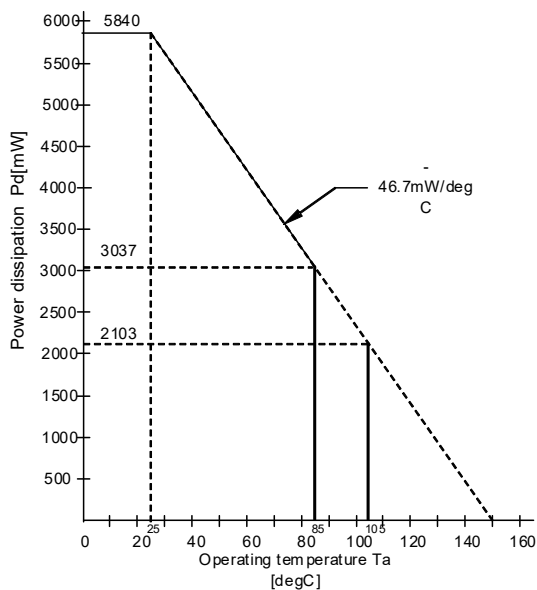


Figure 7-1. Thermal Derating characteristic

Note: Glass epoxy board: 76.2mm x 114.5mm x 1.6mm, copper-occupancy ratio in a 4-layer board: 50% in layers 1 and 4, 95% in layers 2 and 3.

[Note that the allowable power consumption depends on the conditions imposed on the board.]

| Item | Rating Unit | Notes |
|------------------------------------|---------------------|---|
| ψ_{jt} | 1.69 degC/W | junction-to-case (package top surface) thermal resistance |
| θ_{ja} | 21.4 degC/W | junction-to-ambient thermal resistance |
| Exposed power pad / heat slug area | 42.3mm ² | - |

Note1: Glass epoxy board: 76.2mm x 114.5mm x 1.6mm, copper-occupancy ratio in a 4-layer board: 50% in layers 1 and 4, 95% in layers 2 and 3.

[Note that the thermal resistance depends on the conditions imposed on the board.]

8.2 Recommended Operating Conditions

| Item | Symbol | Rating | unit | Note |
|--------------------------------------|--------|-----------------------|------|-------------------------|
| Power supply voltage for motor drive | VM | +6 to +30 | V | RAJ306001 |
| | VM | +6 to +42 | V | RAJ306010 |
| 5V Regulator (VREG5) output current | IVREG5 | 30 [Max] | mA | Total: 60mA [Max] Note1 |
| 5V Regulator (VREG5) output voltage | VREG5 | +4.75~5.25 | V | VREG5_SEL=Hi Note2 |
| MCU operating voltage range | VDD | VREG5-0.25~VREG5+0.25 | V | Note3 |

Note1: Total maximum current including RAA3060xx internal load is 60mA (Max).

For external parts: 30mA (Max), For RAA3060xx: 30mA

Please keep the junction temperature within Tjmax.

Note2: When VREG5 is supplied from external, please keep the sequence as follows.

1. Start up: Supply VM → Supply VREG5 → Release Reset
2. Supply voltage off: Reset → VREG5 Off → VM off

Note3: This operating condition is a restriction of RL78/G1F when using this IC. This value is different from the operating condition in "RL78/G1F User's manual: Hardware" (R01UH0516EJ).

Therefore, this IC cannot operate normally at VDD supply voltage outside the operating voltage range, such as 3.3V.

8.3 Electrical Characteristics

Note: All specifications are for Ta=25degC, VM=22.5V unless otherwise noted.

| Parameter | Symbol | Condition | Rated level | | | Unit | Notes |
|---|--------------------|---|-------------|--------|--------|------|-------------------------------------|
| | | | MIN | TYP | MAX | | |
| Power Supplies (VM, VREG5) | | | | | | | |
| VM operation current | I _{VM} | PS_ALL Reg. (02h): 01h PS Reg. (04h): 09Fh, | | 13.5 | 19 | mA | Pre Driver block (Using Hall IC) |
| VM standby current | I _{STBY} | PS_ALL Reg. (02h): 00h PS Reg. (04h): 00h, System clock: Stop | | 64 | 96 | uA | Pre Driver block (Using Hall IC) |
| VREG5 Output voltage | V _{VREG5} | I _{OUT} = 1 to 30mA | 4.75 | 5 | 5.25 | V | |
| VREG5 load current ability | I _{VREG5} | | | | 30 | mA | |
| Gate Driver Block (VGT, VGB, UHOUT, VHOUT, WHOUT, ULOUT, VLOUT, WLOUT) | | | | | | | |
| Charge pump voltage for High side | V _{vgt} | CPSET2 Reg. (34h)= 02h, I _o =100uA | VM+10 | 13 | VM+15 | V | |
| | | CPSET2 Reg. (34h)= 0Ch, I _o =100uA | VM+10 | | | V | |
| Charge pump voltage for Low side | V _{vgb} | CPSET2 Reg. (34h)= 02h, I _o =100uA | 10 | 13 | 15 | V | |
| | | CPSET2 Reg. (34h)= 0Ch, I _o =100uA | 10 | | | V | |
| Gate drive output voltage for High side | V _{OUTH} | CPSET2 Reg. (34h)= 02h, I _o =100uA | VM+10 | 13 | VM+15 | V | |
| Gate drive output voltage for Low side | V _{OUTL} | CPSET2 Reg. (34h)= 02h, I _o =100uA | 10 | 13 | 15 | V | |
| Impedance of the gate drive output (High side) | R _{OUTH} | IDR_H_P = 111 | - 20% | 9.5 | + 20% | Ω | Note 1) |
| | | IDR_H_P = 100 | | 14.0 | | Ω | |
| | | IDR_H_P = 000 | | 65.0 | | Ω | |
| | | IDR_H_N = 111 | - 25% | 38.5 | + 25% | Ω | |
| | | IDR_H_N = 100 | | 10.0 | | Ω | |
| | | IDR_H_N = 000 | | 5.0 | | Ω | |
| Impedance of the gate drive output (Low side) | R _{OUTL} | IDR_L_P = 111 | - 20% | 5.0 | + 20% | Ω | Note 1) |
| | | IDR_L_P = 100 | | 7.0 | | Ω | |
| | | IDR_L_P = 000 | | 27.0 | | Ω | |
| | | IDR_L_N = 111 | - 25% | 17.5 | + 25% | Ω | |
| | | IDR_L_N = 100 | | 5.0 | | Ω | |
| | | IDR_L_N = 000 | | 2.5 | | Ω | |
| Current Sense Amplifier (ISENP, ISENN) | | | | | | | |
| Input voltage range | V _{ICSA} | | 0.0 | - | 1.0 | V | with respect to ISENN |
| Amplifier Gain | G _{CSA} | CS_SET1 Reg. (20h)= 00h | 50 | | | V/V | |
| | | CS_SET1 Reg. (20h)= 40h | 25 | | | V/V | |
| | | CS_SET1 Reg. (20h)= 50h | 8.25 | | | V/V | |
| Hall signal Block (UH, VH,WH) | | | | | | | |
| Hall IC input signal Threshold voltage level | HIC_TH | HAIC_TH: 000 | + 0.32 | + 0.40 | + 0.48 | V | |
| | | HAIC_TH: 001 | + 0.56 | + 0.70 | + 0.84 | | |
| | | HAIC_TH: 010 | + 0.80 | + 1.00 | + 1.20 | | |
| | | HAIC_TH: 011 | + 1.04 | + 1.30 | + 1.56 | | |
| | | HAIC_TH: 100 | + 1.28 | + 1.60 | + 1.92 | | |
| | | HAIC_TH: 101 | + 1.52 | + 1.90 | + 2.28 | | |
| | | HAIC_TH: 110 | + 1.76 | + 2.20 | + 2.64 | | |
| | | HAIC_TH: 111 | + 2.00 | + 2.50 | + 3.00 | | |
| Hysteresis | HIC_hys | HAIC_HYS: 00 | 0 | | | mV | Note 1) |
| | | HAIC_HYS: 01 | 50 | | | | |
| | | HAIC_HYS: 10 | 100 | | | | |
| BEMF Sense Amplifier (U,V,W) | | | | | | | |
| Input voltage range | V _{IBSA} | | -0.5 | - | VM+0.5 | V | |
| Amplifier Gain | G _{BSA} | | 1 | | | V/V | |

Note1: This specification is the design target of this IC, and Renesas cannot guarantee this specification.

Electrical Characteristics (continued)

Note: All specifications are for Ta=25degC, VM=22.5V unless otherwise noted.

| Parameter | Symbol | Condition | Rated level | | | Unit | Notes |
|---|--------------------|---|-------------|--------|--------|------|-------------------------------------|
| | | | MIN | TYP | MAX | | |
| Power Supplies (VM, VREG5) | | | | | | | |
| VM operation current | I _{VM} | PS_ALL Reg. (02h): 01h PS Reg. (04h): 09Fh, | | 13.5 | 19 | mA | Pre Driver block (Using Hall IC) |
| VM standby current | I _{STBY} | PS_ALL Reg. (02h): 00h PS Reg. (04h): 00h, System clock: Stop | | 64 | 96 | uA | Pre Driver block (Using Hall IC) |
| VREG5 Output voltage | V _{VREG5} | I _{OUT} = 1 to 30mA | 4.75 | 5 | 5.25 | V | |
| VREG5 load current ability | I _{VREG5} | | | | 30 | mA | |
| Gate Driver Block (VGT, VGB, UHOUT, VHOUT, WHOUT, ULOUT, VLOUT, WLOUT) | | | | | | | |
| Charge pump voltage for High side | V _{vgt} | CPSET2 Reg. (34h)= 02h, I _o =100uA | VM+10 | VM+13 | VM+15 | V | |
| | | CPSET2 Reg. (34h)= 0Ch, I _o =100uA | VM+10 | | | V | |
| Charge pump voltage for Low side | V _{vgb} | CPSET2 Reg. (34h)= 02h, I _o =100uA | 10 | 13 | 15 | V | |
| | | CPSET2 Reg. (34h)= 0Ch, I _o =100uA | 10 | | | V | |
| Gate drive output voltage for High side | V _{OUTH} | CPSET2 Reg. (34h)= 02h, I _o =100uA | VM+10 | VM+13 | VM+15 | V | |
| Gate drive output voltage for Low side | V _{OUTL} | CPSET2 Reg. (34h)= 02h, I _o =100uA | 10 | 13 | 15 | V | |
| Impedance of the gate drive output (High side) | R _{OUTH} | IDR_H_P = 111 | - 20% | 9.5 | + 20% | Ω | Note 1) |
| | | IDR_H_P = 100 | | 14.0 | | Ω | |
| | | IDR_H_P = 000 | | 65.0 | | Ω | |
| | | IDR_H_N = 111 | - 25% | 38.5 | + 25% | Ω | |
| | | IDR_H_N = 100 | | 10.0 | | Ω | |
| | | IDR_H_N = 000 | | 5.0 | | Ω | |
| Impedance of the gate drive output (Low side) | R _{OUTL} | IDR_L_P = 111 | - 20% | 5.0 | + 20% | Ω | Note 1) |
| | | IDR_L_P = 100 | | 7.0 | | Ω | |
| | | IDR_L_P = 000 | | 27.0 | | Ω | |
| | | IDR_L_N = 111 | - 25% | 17.5 | + 25% | Ω | |
| | | IDR_L_N = 100 | | 5.0 | | Ω | |
| | | IDR_L_N = 000 | | 2.5 | | Ω | |
| Current Sense Amplifier (ISENP, ISENN) | | | | | | | |
| Input voltage range | V _{ICSA} | | 0.0 | - | 1.0 | V | with respect to ISENN |
| Amplifier Gain | G _{CSA} | CS_SET1 Reg. (20h)= 00h | 50 | | | V/V | |
| | | CS_SET1 Reg. (20h)= 40h | 25 | | | V/V | |
| | | CS_SET1 Reg. (20h)= 50h | 8.25 | | | V/V | |
| Hall signal Block (UH, VH,WH) | | | | | | | |
| Hall IC input signal Threshold voltage level | HIC_TH | HAIC_TH: 000 | + 0.32 | + 0.40 | + 0.48 | V | |
| | | HAIC_TH: 001 | + 0.56 | + 0.70 | + 0.84 | | |
| | | HAIC_TH: 010 | + 0.80 | + 1.00 | + 1.20 | | |
| | | HAIC_TH: 011 | + 1.04 | + 1.30 | + 1.56 | | |
| | | HAIC_TH: 100 | + 1.28 | + 1.60 | + 1.92 | | |
| | | HAIC_TH: 101 | + 1.52 | + 1.90 | + 2.28 | | |
| | | HAIC_TH: 110 | + 1.76 | + 2.20 | + 2.64 | | |
| | | HAIC_TH: 111 | + 2.00 | + 2.50 | + 3.00 | | |
| Hysteresis | HIC_hys | HAIC_HYS: 00 | 0 | | | mV | Note 1) |
| | | HAIC_HYS: 01 | 50 | | | | |
| | | HAIC_HYS: 10 | 100 | | | | |
| BEMF Sense Amplifier (U,V,W) | | | | | | | |
| Input voltage range | V _{IBSA} | | -0.5 | - | VM+0.5 | V | |
| Amplifier Gain | G _{BSA} | | 1 | | | V/V | |

Note1: This specification is the design target of this IC.

The recommended external circuit with the following conditions is shown as Figure 8-2.

- External 5V regulator is used for RL78/G1F and Hall IC.
- Charge Pump circuit does NOT use the double boost function. (R34h: D3, CP_BOOST_N=1)
VGB= 10V, VGT= VM+10V
- Hall sensor-less type

The user can select each condition independently according to the actual application.

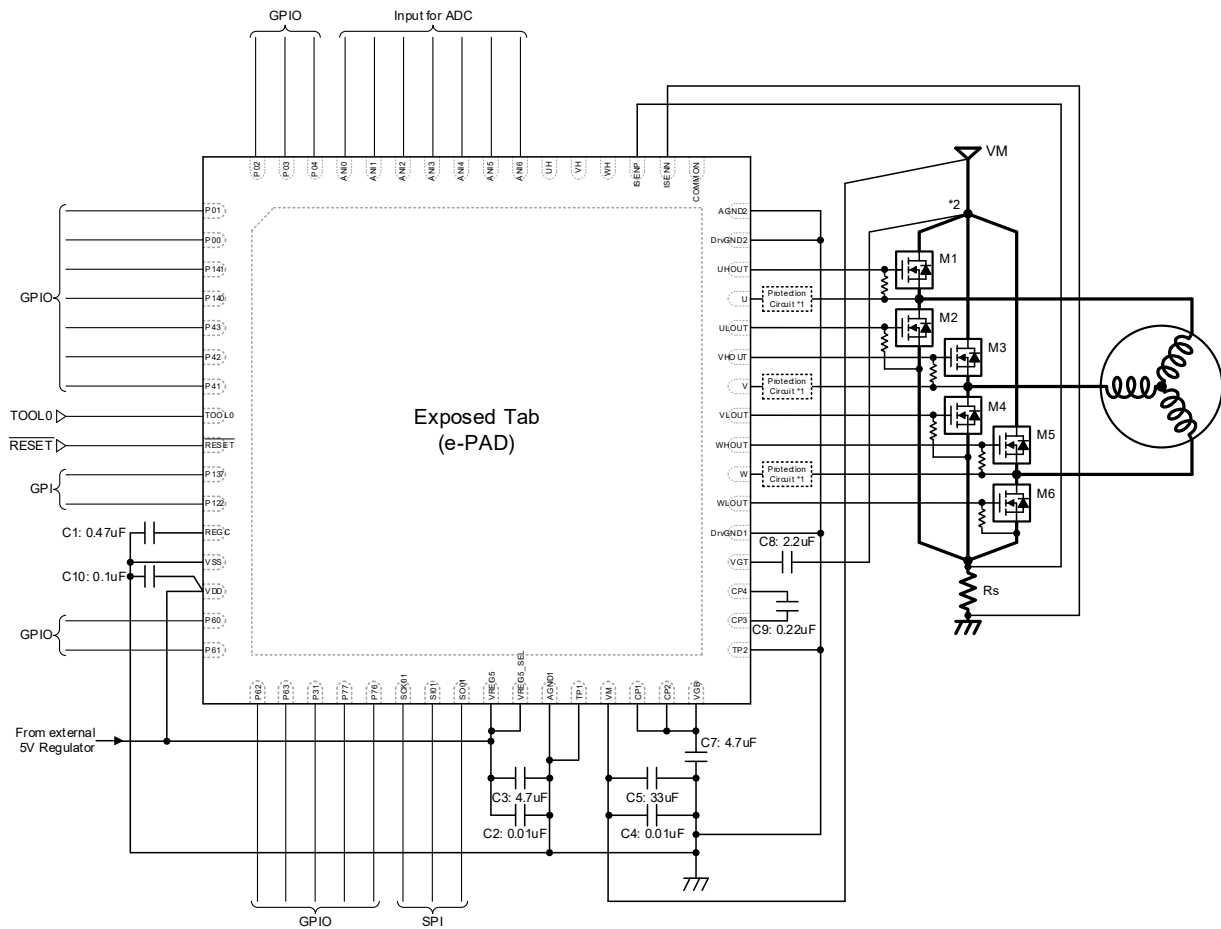


Figure 8-2. Recommended External Circuit example with using external 5V regulator, single boost function, and Hall sensor-less type

1. There are some possibility to add resistor and/or diode according to motor spec and drive condition. Refer to *1 note in Figure8-1.
2. Please pay attention that the connection point of C8 which is attached to terminal VGT is near the drain of M1, M3 and M5 as close as possible.
This request is to synchronize voltage change between Upper External MOS's drain and VGT terminal.
This layout can decrease the potential to be added unexpected VGS voltage on Upper External MOS.

10. Block Explanation

10.1 Power ON Sequence

Fig.9-1 shows the example of Power ON sequence regarding VM, VREG5, and VREG3 (internal Regulator). When the power supply of RL78G1F is VREG5, the operation state of RL78/G1F (MCU) and Pre-Driver depends on VREG5 and VREG3 voltage. When VM is applied, VREG5 and VREG3 starts in synchronization with VM.

RL78/G1F (MCU) and Pre-Driver work as follows sequentially.

1. After $VREG3 > VREC3$ (2.83V),
 - RL78/G1F (MCU): "RESET" is maintained.
 - Pre-Driver: "RESET" is released and goes "Stop".
 - Pre-Driver keeps the motor stop as the control signals from RL78/G1F (MCU) is reset.
2. After $VREG5 > VLVDH$ (4.06V),
 - RL78/G1F (MCU): "RESET" is released and goes "Normal".
 - After RL78/G1F (MCU) sets VREG5_TRIM register (R40h) to the written data in TRIM_DATA0 (Address: EFFECh) of RL78/G1F, VREG5 becomes 5V typical. The default voltage is 4.8V.
 - Pre-Driver can drive the motor by the control of RL78/G1F (MCU).
3. When $VREG5 < VLVDL$ (3.98V),
 - RL78/G1F (MCU) goes "RESET".
 - Pre-Driver stops driving the motor as the control signals from RL78/G1F (MCU) is reset.
4. Same as (2)
5. Same as (3)
6. After $VREG3 < VSD3$ (2.70V),
 - RL78/G1F (MCU): "RESET" is maintained.
 - Pre-Driver keeps the motor stop by "RESET" state.

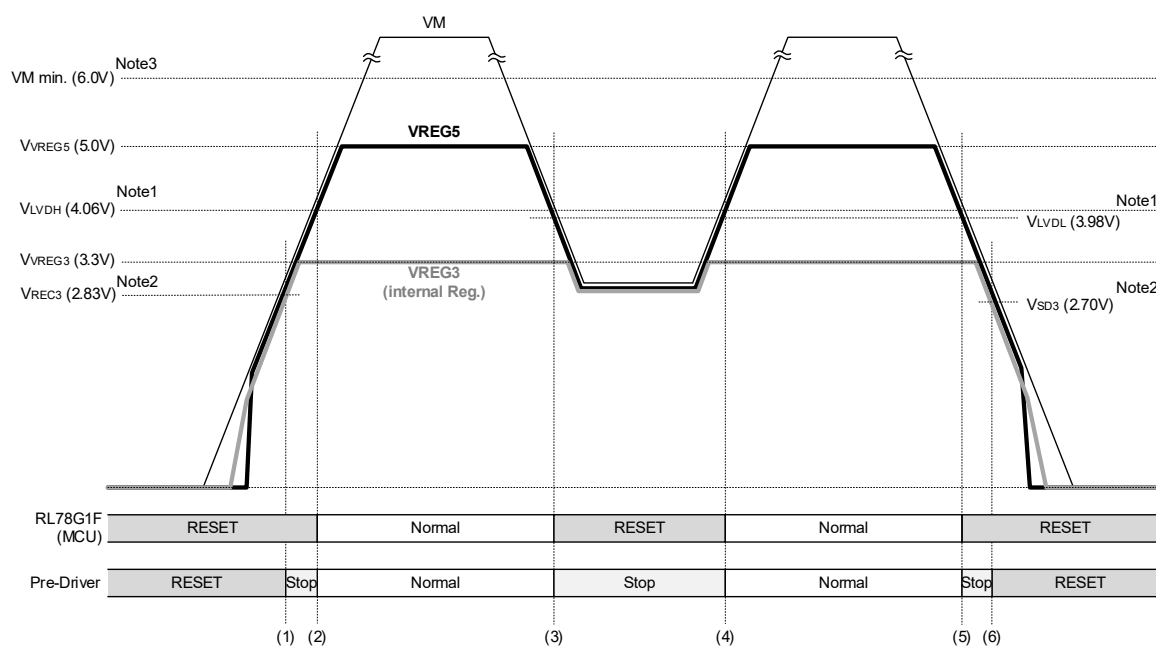


Figure 9-1. Power ON Sequence of VM VREG5, and VREG3

Note1: When a user writes in data of Firmware to Flash, the user needs to set MCU as follows.

Voltage Detector Function: Enable

Setting "Reset mode" of Voltage Detector Function.

Setting '4.06V of Rising edge' and '3.98V of Falling edge' on Detection voltage (VLVD).

Note2: VREC3 and VSD3 are the design target.

Note3: When VM is less than 6V, VGB for the Power MOS gate drive becomes less than 10V.

Refer to section 7.2 "Recommended Operating Condition".

10.2 Serial Array Unit

RL78/G1F(MCU) has two Serial Array Unit. Serial Array Unit 0 is consisted four Serial channel. Serial Array Unit 1 is consisted two Serial channels. The Serial channel has three modes (CSI, UART, and Simplified I2C). Please refer to Chapter 19 Serial Array Unit in “RL78/G1F User’s manual: Hardware” (R01UH0516EJ).

Channel of CSI00: CSI00 is used for the communication of RL78/G1F MCU and the Pre-driver at the inside. The valid function of communication for peripheral circuit are the following.

| Unit | Channel | Used as CSI | Used as UART | Used as simplified I ² C |
|------|---------|---|--------------|-------------------------------------|
| 0 | 0 | CSI00 (Can't use slave select input function) [[internal connection] Note 1] | | |
| | 1 | CSI01 | | |
| | 2 | CSI10 | UART1(TxD1) | IIC10 |
| | 3 | | UART1(RxD1) | |
| 1 | 0 | | | |
| | 1 | | | |

Note 1 Communication between RL78/G1F(MCU) and Pre-Driver

P51, P50, and P30 pins of RL78/G1F(MCU) are connected internally with Pre-Driver. Pre-Driver registers can be access via CSI0 (Channel 0 of Serial Array Unit 0).

Please set to CSI00 settings as follows.

- To disable slave select input function (/SSI00 pin), setting of SSIE00 =0 in ISC register is required. Refer to Chapter 19.3.15 Input switch control register (ISC) in “RL78/G1F User’s manual: Hardware” (R01UH0516EJ).
- To use type1 (DAP00=0, and CPK00=0 in SCR00 register). Refer to Chapter 19.3.4 Serial communication operation setting register mn (SCRmn) in “RL78/G1F User’s manual: Hardware” (R01UH0516EJ).

10.3 CSI timing specification

The following table shows the CSI timing specification during communication at same potential.

HS (Hi-speed main) mode

| parameter | Symbol | Condition | CSI00 | | | Unit |
|----------------------------------|------------|--|----------------|------|-----|------|
| | | | MIN | TYP | MAX | |
| SCK00 cycle time | tKCY1 | tKCY1 >= 4/fCLK 4.75V <= VDD <= 5.25V | - | 1000 | - | ns |
| SCK00 high/low-level width | tKH1, tKL1 | 4.75V <= VDD <= 5.25V | tKCY1/2 -24 | - | - | ns |
| Slp setup time (from SCK00 ↑) | tSIK1 | 4.75V <= VDD <= 5.25V | 66 | - | - | ns |
| Slp hold time (from SCK00 ↓) | tKSI1 | | 38 | - | - | ns |
| Delay from SCK00↓ to SO00 output | tKSO1 | C = 30pF *note1 | - | - | 50 | ns |

MCU SCR00 register, DAP00=0, CKP00=0, /SSIIE=0
 Note1: C is the load capacitance of SCK00 and SO00.

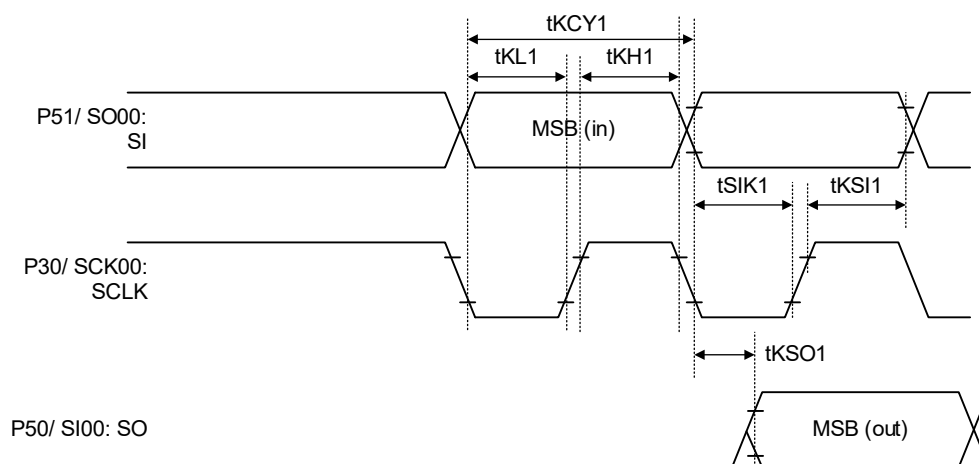
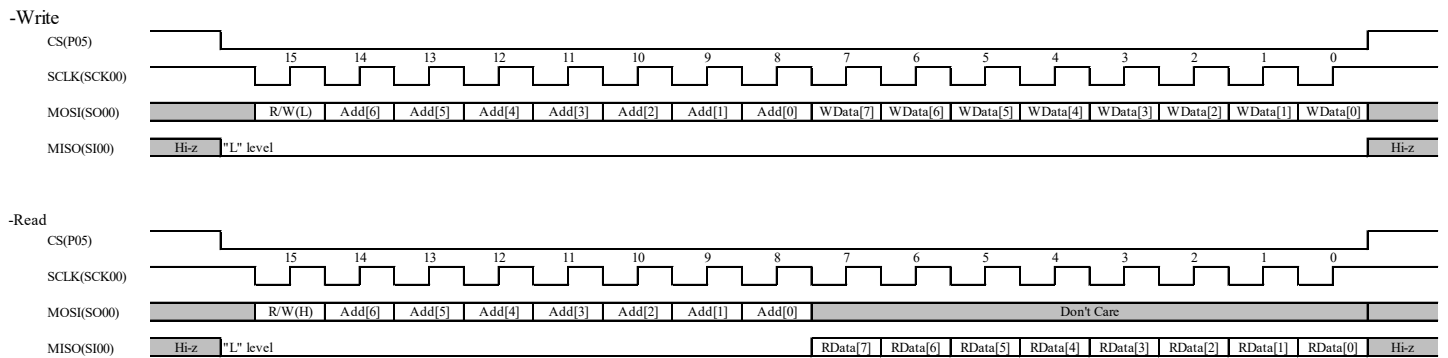


Figure 9-2. CSI Timing Diagram

10.4 CSI Communication Format

Fig.9-3 shows CSI communication format of both write and read mode.

If the communication format is different from this, its communication becomes invalid.



11. Control Register Map

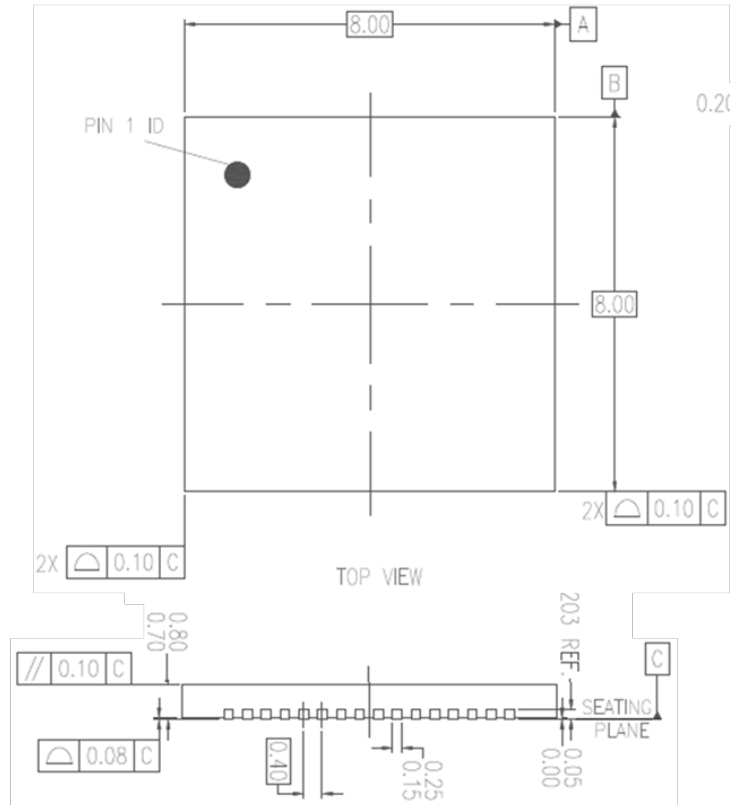
Table 10-1 shows the RAJ3060xx's register map. Check the "2.4 Pre-Driver register " in "RAJ306000 Series User's Manual" for details.

Table 10-1. Register Map

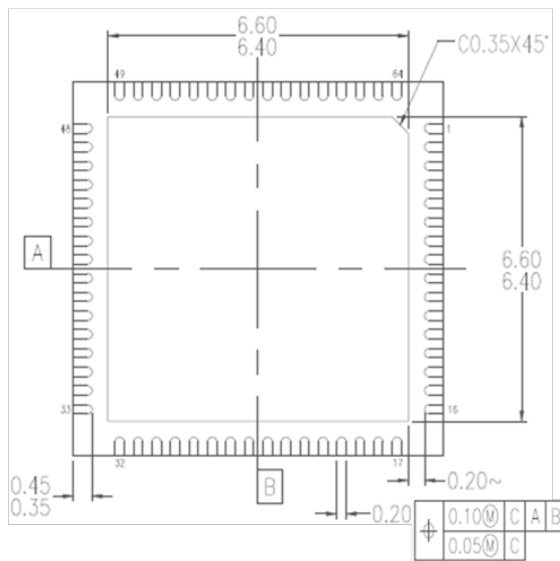
| Addr. | Register Name | Symbol | Initial value | 7 | 6 | 5 | 4 | 3 | |
|------------|--|------------|--------------------------------|-----------------------------|------------------|----------------|----------------|---------------|---|
| 02h | Power Save Control Register | PS_ALL | 00h | 0 | 0 | 0 | 0 | 0 | |
| 04h | By Function Power Save Control Setting Register | PS | 00h | PS_PRE_N | 0 | PS_BMF_N | PS_CSAMP_N | PS_VMC_N | |
| 06h | Software Reset Register | SW_RESET | 00h | 0 | 0 | 0 | 0 | 0 | |
| 08h | ADC Selector Register | ADC_SEL | 00h | 0 | 0 | 0 | 0 | 0 | |
| 0Ah | U Phase Motor Control Signal Select Register | SELSIG_U | 03h | 0 | SELSIG_U_H2 to 0 | | | 0 | |
| 0Ch | V Phase Motor Control Signal Select Register | SELSIG_V | 14h | 0 | SELSIG_V_H2 to 0 | | | 0 | |
| 0Eh | W Phase Motor Control Signal Select Register | SELSIG_W | 25h | 0 | SELSIG_W_H2 to 0 | | | 0 | |
| 10h | Hall Signal Processing Setting Register | HALL_SIG | 00h | BEMF_MODE_SEL | CENTERTAP_SEL | HALL_MODE_SEL | PWM_SEL | HALL_POLA | |
| 12h | ALARM Status Register1 | ALMSTS1 | FFh | VREG5_OVP_N | VGT_OVP1_N | VGT_OVP2_N | VGT_UVP_N | VGB_OVP_N | |
| 14h | ALARM Operation Setting Register1 | ALMOPE1 | 00h | 0 | 0 | 0 | VGT_UVP_OPE_N | 0 | |
| 16h | ALARM Pin Output Setting Register1 | ALMOUT1 | 00h | VREG5_OVP_ALE_N | VGT_OVP1_ALE_N | VGT_OVP2_ALE_N | VGT_UVP_ALE_N | VGB_OVP_ALE_N | |
| 18h | ALARM Status Register2 | ALMSTS2 | FFh | 1 | 1 | 1 | 1 | 1 | |
| 1Ah | Current Sense setting Register2 | CS_SET2 | 00h | CSAMP_IREF1 to 0 | | CSAMP_ATT | 0 | 0 | |
| 1Ch | ALARM Pin Output Setting Register2 | ALMOUT2 | 00h | 0 | 0 | 0 | 0 | 0 | |
| 1Eh | Error Detection Wait Time Setting Register | ERROR_WAIT | 00h | 0 | 0 | 0 | REGV5_OVP_WAIT | UVCP | |
| 20h | Current Sense setting Register1 | CS_SET1 | 00h | 0 | SHUNT_SEL2 to 0 | | | 0 | |
| 22h | Hall IC Threshold Adjustment Register | HAIC_TH | 00h | 0 | 0 | HAIC_HYS1 to 0 | | 0 | |
| 24h | Pre-Driver Drive Status Register | PDDSTS | F0h | 1 | 1 | 1 | LDS_N | FG | |
| 26h | LD Judgment Wait Time Register | LD_WAIT | 00h | LD_ALE_N | 0 | 0 | 0 | 0 | |
| 28h | Motor Drive Control Setting Register | DRIVE_SET | 00h | OCF_HYS_N | ALM_LATCH_CLR | 0 | DECAY_MODE_SEL | DT_REG_N | |
| 2Ah | - | - | - | 0 | 0 | 0 | 0 | 0 | |
| 2Ch | High Side Output Current Capability Setting Register | IDRCNT_H | 00h | 0 | IDR_H_P2 to 0 | | | 0 | |
| 2Eh | Low Side Output Current Capability Setting Register | IDRCNT_L | 00h | 0 | IDR_L_P2 to 0 | | | 0 | |
| 30h | Pch Slew Rate Setting Register | TRCNT_P | 00h | 0 | TR_H_P2 to 0 | | | 0 | |
| 32h | Charge Pump Setting Register1 | CPSET1 | 01h | 0 | 0 | 0 | 0 | 0 | |
| 34h | Charge Pump Setting Register2 | CPSET2 | 02h | 0 | 0 | 0 | 0 | CP_BOOST_N | |
| 36h | Charge Pump Trimming Register | CP_TRIM | 00h | CP_TRIM7 - CP_TRIM0 | | | | | 0 |
| 38h to 3Eh | - | - | - | 0 | 0 | 0 | 0 | 0 | |
| 40h | 5V Regulator Voltage Setting | VREG5_TRIM | 00h | VREG5_TRIM7 - VREG5_TRIM0 | | | | | 0 |
| 42h | Ext. FET Current Detect AMP Setting Register | CSAMP_TRIM | 00h | CSAMP_TRIM7 - CSAMP_TRIM0 | | | | | 0 |
| 44h to 56h | - | - | - | 0 | 0 | 0 | 0 | 0 | |
| 58h | ALARM Raw Status Monitor Register1 | ALMRAW1 | FFh | 1 | VGT_OVP1_RAW_N | VGT_OVP2_RAW_N | VGT_UVP_RAW_N | VGB_OVP_RAW_N | |
| 5Ah | - | - | - | 0 | 0 | 0 | 0 | 0 | |
| 5Ch | TOIN Pin Monitor Register | TOIN_MONI | - | TOINA | TOINB | TOINC | TOIND | TOINE | |
| 5Eh | WHO_AM_I | WHO_AM_I | RAJ306001:6Ah RAJ306010:6Bh | WHO_AM_I_7 - WHO_AM_I_0 | | | | | |
| 60h | Trimming Protect Register | TRIM_PT | 00h | TRIM_PT7 - TRIM_PT0 | | | | | |
| 62h to 72h | - | - | - | 0 | 0 | 0 | 0 | 0 | |
| 74h | Trimming Data Valid Register | TRIM_EN | 00h | 0 | 0 | 0 | 0 | 0 | |
| 76h | - | - | - | 0 | 0 | 0 | 0 | 0 | |
| 78h | High Precise BGR Temp. Correction Register | BGR_TRIM | FFh | BGR_TRIM_7 - BGR_TRIM_0 | | | | | |
| 7Ah | BUFFAMP Absolute Value Correction Register | BFAMP_TRIM | FFh | BFAMP_TRIM_7 - BFAMP_TRIM_0 | | | | | |
| 7Ch to 7Eh | - | - | - | 0 | 0 | 0 | 0 | 0 | |

12. Package Description

TOP VIEW



BOTTOM VIEW



13. Revision History

| Revision | Date | Description |
|----------|--------------|--|
| 1.1 | Mar 24, 2021 | To update the format of the datasheet. |

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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