RC2121xA (AutoClock)

Evaluation Board

The RC2121xA (RC21211A, RC21212A, RC21213A, RC21214A [AutoClock™]) Evaluation Board (EVB) is designed to support users evaluating the clock generation in synthesizer mode for PCIe Gen compliance and commercial automotive applications.

Specifications

- 169fs RMS phase jitter (10kHz–20MHz, 156.25MHz).
- PCIe Gen6 Common Clock (CC) 27fs RMS

Board Contents

Items shipped with EVB kit:

- EVB
- USB cable

Features

- PCIe SRIS and SRNS support
- 1kHz to 650MHz (differential) and 1kHz to 200MHz (single-ended) outputs
- LVCMOS, LVDS or Low-Power HCSL output types with simple AC-coupling to LVPECL and CML. LP-HCSL integrates terminations.
- Seven programmable general-purpose input/outputs (GPIO)
- 1MHz I^2C serial port
- Multiple configurations can be stored in internal One-Time Programmable (OTP) memory.
- 1.8V or 3.3V operation
- Crystal or crystal overdrive (REFIN) via SMA
- Available sense lines on crystal overdrive.
- Test points on Outputs for Hi-Z probes.
- Jumper selectable voltage setting for 3.3V/2.5V/1.8V powered from USB

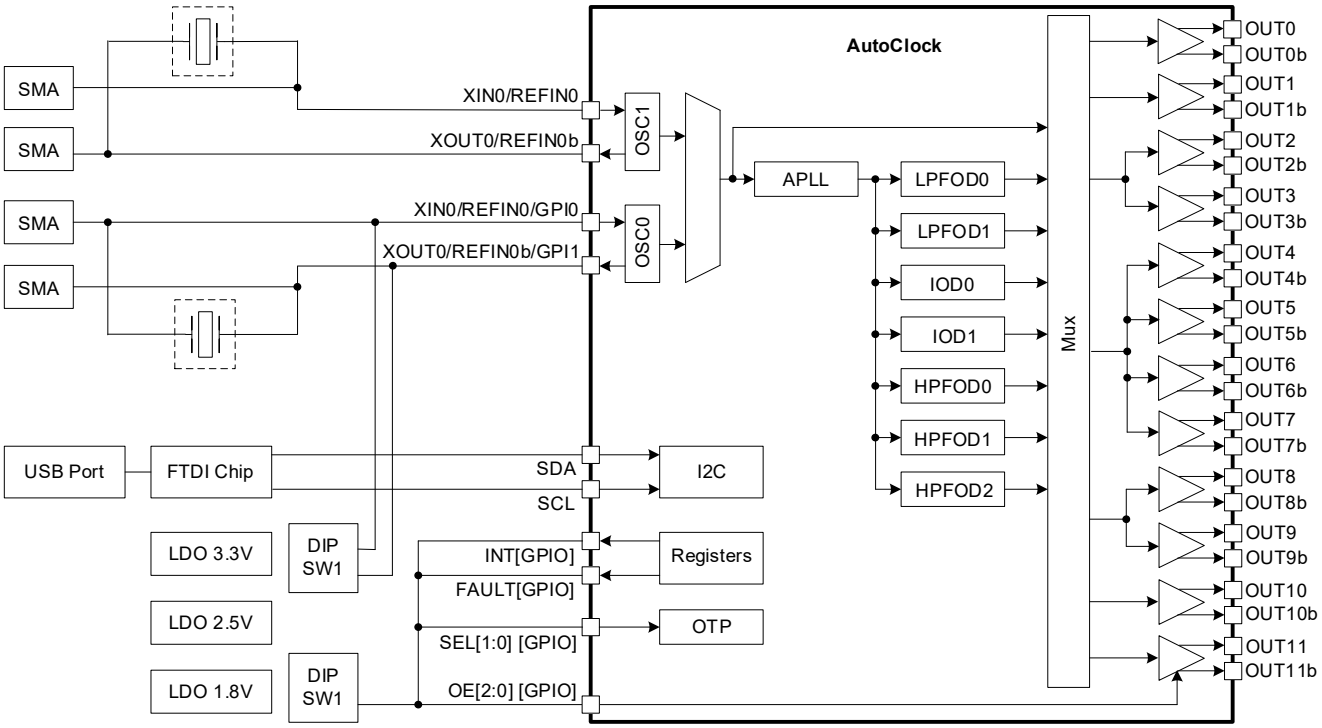

Figure 1. Board Block Diagram

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1. Functional Description

The RC2121xA Evaluation Board (EVB) is designed to support users evaluating the RC21211, RC21212A, RC21213A and RC21214A devices using clock generation in synthesizer mode for PCIe Gen compliance. When the EVB is connected via USB to the user's computer running Renesas Integrated Circuit Toolbox (RICBox™) software, RC2121xA devices can be configured in various frequencies with best-in-class commercial performance. The devices offer various features with eight to twelve pairs of differential outputs. Each pair of output can be programmed to LVCMOS, LVDS, and LP-HCSL style outputs. There are seven general purpose input/output (GPIOs) and two general purpose input (GPIs) to support output enables, configuration selection, and status outputs. Voltage levels for VDDX0, VDDX1, VDDA, VDDD, and VDDO0–6 can be set by jumpers.

1.1 Operational Characteristics

The EVB is capable of functioning in temperature range of -40°C to +105°C and is capable of operating in VDD values of 3.3V, and 1.8V. The VDD_J banana connection can be used to set any desired voltage within the range of 1.71V to 3.63V. RC2121xA devices are ISO9001 compliant, AEC-Q100 qualified, and provides support for PPAP.

1.2 Setup and Configuration

The following sections explain the Crystal/Ref input clock, Serial, GPI/GPIO, and output and power functions used for setting up and configuring the devices using RICBox software.

1.2.1 RC21211/RC21212 vs RC21213/RC21214

The RC21211/RC21212 are twelve differential pair output devices, while the RC21213/RC21214 are eight differential pair output devices. The RC21211/RC21213 devices has single crystal/reference input, whereas the RC21212/RC21214 has two crystal/reference inputs.

The following table summarizes the differences between the devices.

Table 1. Summary of RC21211/RC21212 and RC21213/RC21214

Device	Number of Crystal Inputs	GPIO	GPI	Output Clocks
RC21211A	Single	GPIO0 – GPIO6	GPI0, GPI1	OUT0 – OUT11
RC21212A	Dual	GPIO0 – GPIO6	-	OUT0 – OUT11
RC21213A	Single	GPIO0 – GPIO6	GPI0, GPI1	OUT1, OUT2, OUT3, OUT6, OUT7, OUT8, OUT10, OUT11
RC21214A	Dual	GPIO0 – GPIO6	-	OUT1, OUT2, OUT3, OUT6, OUT7, OUT8, OUT10, OUT11

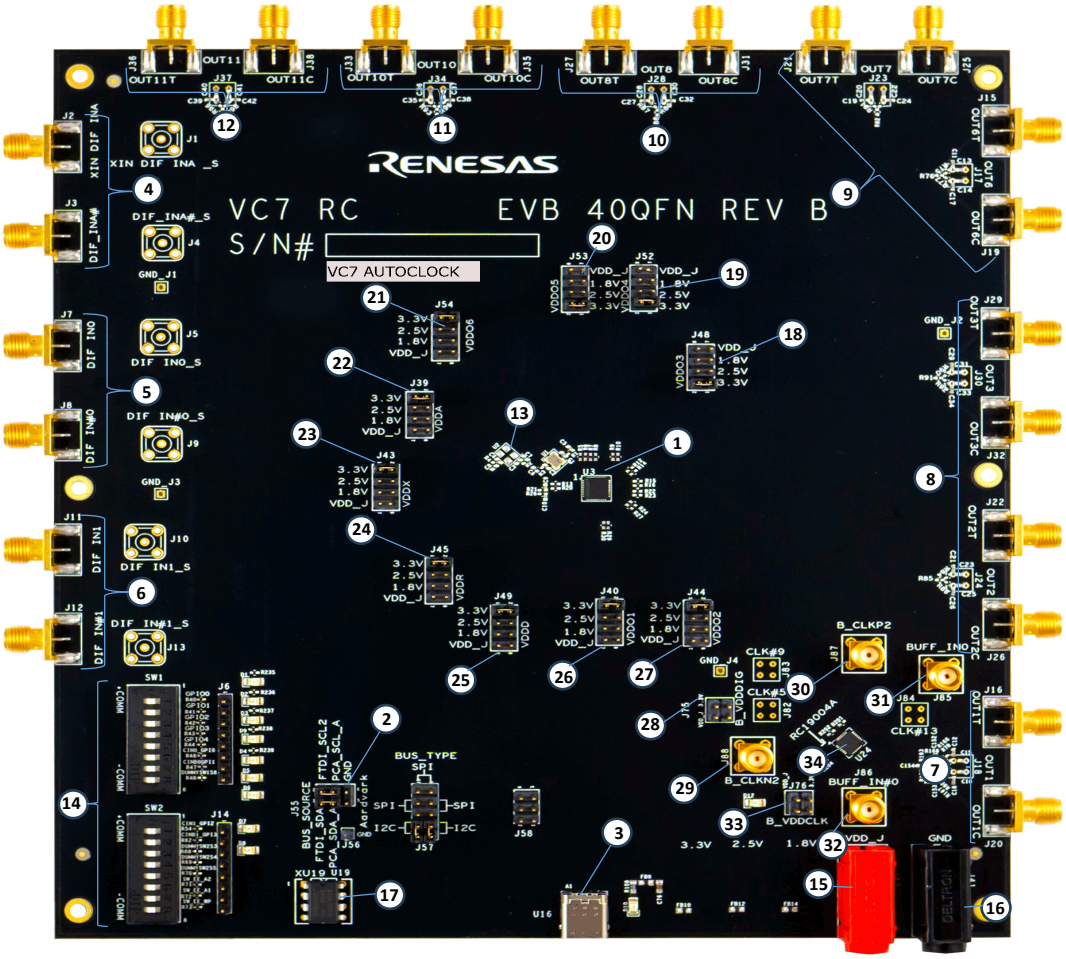


Figure 2. RC21213/RC21214 AutoClock Evaluation Board

Refer to Table 2 for the RC21213A/RC21214A evaluation board pin descriptions and functions.

Table 2. RC21213A/RC21214A EVB Pins and Functions

Item	Name	On-Board Connector Label	Function
1	RC21213/RC21214	U3	Evaluation device, 5 × 5 × 0.75 mm 40-pin VFQFPN.
2	I²C for FTDI or Aardvark Connector	J55	6-pin header of I²C connector for SCL and SDA pins.
3	USB Interface	U16	USB type jack for connection with the computer and interaction with RICBox software.
4	XIN0 / XOUT0 REFIN0/ REFIN0B	J2, J3	Differential REF clock input positive on J2 and negative on J3. If J2 is connected to XIN as REFIN single-ended, J3 must be left unconnected.
5	XIN1 / XOUT1 REFIN0 / REFIN1B GPI0 / GPI1	J7, J8	For RC21214 differential REF clock input positive on J8 and negative on J7. For CMOS single-ended reference clock input J8 is connected to XIN as REFIN single-ended, J7 must be left unconnected. For single crystal variant this pin act as GPI0 and GPI1 SMA Connector.

Item	Name	On-Board Connector Label	Function
6	GPIO5, GPIO6	J11, J12	GPIO5 and GPIO6 SMA Connector
7	Test Points for OUT1	J16, J20	SMA connectors for differential outputs using VDDO1 power rail (populated with a pair of SMA connector): J16, J20 for OUT1
8	Test Points for OUT2, OUT3	J22, J26, J29, J32	SMA connectors for differential outputs using VDDO2 power rail (populated with a pair of SMA connector): J22, J26 for OUT2 J29, J32 for OUT3
9	Test Points for OUT6, OUT7	J15, J19, J21, J25	SMA connectors for differential outputs using VDDO3 power rail (populated with a pair of SMA connector): J15, J19 for OUT6 J21, J25 for OUT7
10	Test Points for OUT8	J27, J31	SMA connectors for differential outputs using VDDO4 power rail (populated with a pair of SMA connector): J27, J31 for OUT8
11	Test Points for OUT10	J33, J35	SMA connectors for differential outputs using VDDO5 power rail (populated with a pair of SMA connector): J33, J35 for OUT10
12	Test Points for OUT11	J36, J38	SMA connectors for differential outputs using VDDO6 power rail (populated with a pair of SMA connector): J36, J38 for OUT11
13	Crystal Pads	U1, U2	To mount different quartz crystals.
14	DIP Switches	SW1, SW2	DIP switch devices are used to setup GPIO/GPI pins based on RC21213/RC21214 device condition. For details, see Figure 8 and Figure 9.
15	Power VDD Jack	J42	External power supply, positive terminal. Apply 3.3Vor 1.8V as default only.
16	Power GND Jack	J41	External power supply, negative terminal, or ground.
17	EEPROM IC	XU19, U19	An external EEPROM IC and an 8-lead PDIP8 socket. Populated with AT24C04C 4-Kbit (512 × 58) EEPROM as default.
18	VDDO3	J48	Power source selector. Select in 3.3V, 1.8V or external power VDD_J for OUT Bank 3.
19	VDDO4	J52	Power source selector. Select in 3.3V, 1.8V or external power VDD_J for OUT Bank 4.
20	VDDO5	J53	Power source selector, select in 3.3V, 1.8V or external power VDD_J for OUT Bank 5.
21	VDDO6	J54	Power source selector. Select in 3.3V, 1.8V or external power VDD_J for OUT Bank 6.
22	VDDA	J39	Power source selector. Select in 3.3V, 1.8V or external power VDD_J for analog circuit power.
23	VDDX	J43	Power source selector. Select in 3.3V, 1.8V or external power VDD_J for crystal circuit power.

Item	Name	On-Board Connector Label	Function
24	VDDR	J45	Power source selector. Select in 3.3V, 1.8V or external power VDD_J for reference input circuit power.
25	VDDD	J49	Power source selector. Select in 3.3V, 1.8V or external power VDD_J for digital circuit power.
26	VDDO1	J40	Power source selector. Select in 3.3V, 1.8V or external power VDD_J for OUT Bank 1.
27	VDDO2	J44	Power source selector. Select in 3.3V, 1.8V or external power VDD_J for OUT Bank 2.
28	B_VDDDIG	J75	Power source selector. Select in 3.3V or external power VDD_J for VDDIG digital power pin of RC19004A.
29	B_CLKN2	J59	Complementary clock output pin of RC19004A.
30	B_CLKP2	J60	True clock output pin of RC19004A.
31	BUFF_IN0	J85	Differential buffer Input 0.
32	BUFF_IN#0	J86	Differential buffer Input #0.
33	B_VDDCLK	J76	Power source selector, select in 3.3V or external power VDD_J for VDDCLK clock power supply pin of RC19004A.
34	RC19004A	U28	Fanout buffer.

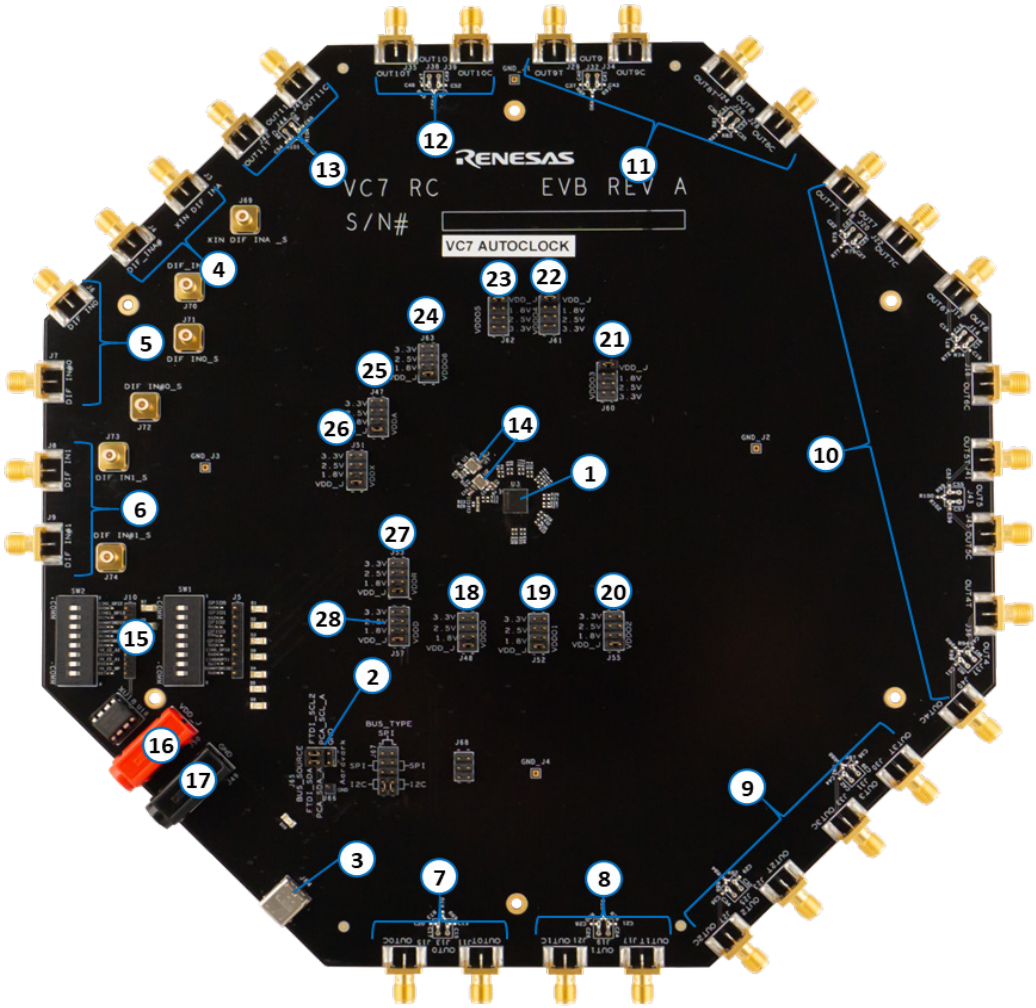


Figure 3. RC21211/RC21212 AutoClock Evaluation Board

Refer to Table 3 for the RC21211A/RC21212A evaluation board pin descriptions and functions.

Table 3. RC21211A/RC21212A – EVB Pins and Functions

Item	Name	On-Board Connector Label	Function
1	RC21212A	U3	Evaluation device, 6 × 6 × 0.9 mm 48-VFQFPN.
2	I^2C for FTDI or Aardvark Connector	J65	6 pins header of I^2C connector for SCL and SDA pins.
3	USB Interface	J64	USB-type jack for connection with the computer and interaction with RICBox software.
4	XIN0 / XOUT0 REFIN0 / REFIN0B	J3,J4	Differential REF clock input positive on J3 and negative on J4 / CMOS single-ended reference clock input. If J3 is connected to XIN0 as REFIN single-ended, J4 must be left unconnected.

Item	Name	On-Board Connector Label	Function
5	XIN1 / XOUT1 REFIN1 / REFIN1B	J6, J7	Differential REF clock input positive on J29 and negative on J31 / CMOS single-ended reference clock input. If J29 is connected to XIN1 as REFIN single-ended, J31 must be left unconnected.
6	GPIO5, GPIO6	J8, J9	GPIO5 and GPIO6 SMA connector.
7	Test Points for OUT0	J11, J15	SMA connectors for differential outputs using VDDO0 power rail (populated with a pair of SMA connectors): J11, J15 for OUT0
8	Test Points for OUT1	J17, J21	SMA connectors for differential outputs using VDDO1 power rail (populated with a pair of SMA connectors): J17, J21 for OUT1
9	Test Points for OUT2, OUT3	J23, J27, J30, J33	SMA connectors for differential outputs using VDDO2 power rail (populated with a pair of SMA connectors): J23, J27 for OUT2 J30, J33 for OUT3
10	Test Points for OUT4, OUT5, OUT6, OUT7	J36, J40, J41, J45, J12, J16, J18, J22	SMA connectors for differential outputs using VDDO3 power rail (populated with a pair of SMA connectors): J36, J40 for OUT4 J41, J45 for OUT5 J12, J16 for OUT6 J18, J22 for OUT7
11	Test points for OUT8, OUT9	J24, J28, J29, J34	SMA connectors for differential outputs using VDDO4 power rail (populated with a pair of SMA connectors): J24, J28 for OUT8 J29, J34 for OUT9
12	Test points for OUT10	J35, J39	SMA connectors for differential outputs using VDDO5 power rail (populated with a pair of SMA connectors): J35, J39 for OUT10
13	Test points for OUT11	J42, J46	SMA connectors for differential outputs using VDDO6 power rail (populated with a pair of SMA connectors): J42, J46 for OUT11
14	Crystal Pads	U1, U2	To mount different quartz crystals.
15	DIP Switches	SW1, SW2	DIP switch devices are used to setup GPIO/GPI pins based on RC21212A device condition (see Figure 8 and Figure 9).
16	Power VDD Jack	J50	External power supply, positive terminal. Apply 3.3V or 1.8V as default only.
17	Power GND Jack	J49	External power supply ground.
18	VDDO0	J48	Power source selector. Select 3.3V, 1.8V or external power VDD_J for OUT Bank 0.
19	VDDO1	J52	Power source selector. Select.3V, 1.8V or external power VDD_J for OUT Bank 1
20	VDDO2	J55	Power source selector. Select 3.3V, 1.8V or external power VDD_J for OUT Bank 2.

Item	Name	On-Board Connector Label	Function
21	VDDO3	J60	Power source selector. Select 3.3V, 2.5V, 1.8V or external power VDD_J for OUT Bank 3.
22	VDDO4	J61	Power source selector. Select 3.3V, 2.5V, 1.8V or external power VDD_J for OUT Bank 4.
23	VDDO5	J62	Power source selector. Select 3.3V, 2.5V, 1.8V or external power VDD_J for OUT Bank 5.
24	VDDO6	J63	Power source selector. Select 3.3V, 2.5V, 1.8V or external power VDD_J for OUT Bank 6.
25	VDDA	J47	Power source selector. Select 3.3V, 1.8V or external power VDD_J for analog circuit power
26	VDDX0 (VDDX)	J51	Power source selector. Select 3.3V, 1.8V or external power VDD_J for crystal circuit power
27	VDDX1 (VDDR)	J53	Power source selector. Select 3.3V, 1.8V or external power VDD_J for reference input circuit power
28	VDDD	J57	Power source selector. Select 3.3V, 1.8V or external power VDD_J for digital circuit power

1.2.2 On Board Crystal PAD and Reference Input

The EVB has two crystal pads U1 and U2 that are left uninstalled. Different crystal frequencies between 8MHz and 80MHz can be used to match the specific application where the RC21211/RC21212 is used. For example, it is recommended to use a 39.0625MHz or 62.5MHz crystal for Ethernet applications with output frequencies of 156.25MHz or 312.5MHz. Refer to the datasheet for more information on crystal recommendations. The RC2121xA devices supports a range of C_L from 6pF to 12pF.

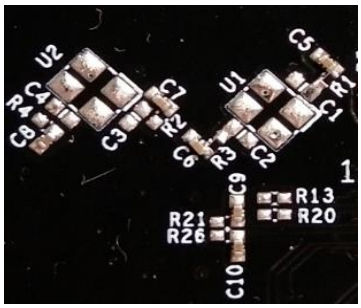


Figure 4. Crystal Footprints

The XIN0/REFIN0 input (J3/J4) can be used to overdrive the XIN pin with an external clock with SMA connectors in single-ended or differential mode. Supported frequency range of the reference input are 1kHz to 650MHz in differential mode, and 8kHz to 250MHz in single-ended mode.

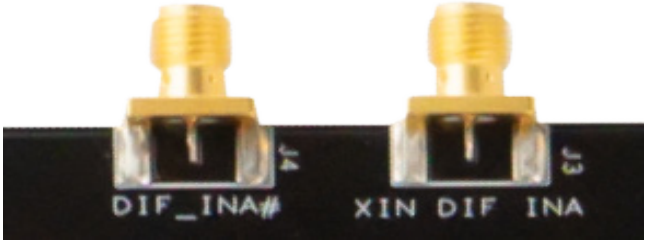


Figure 5. Single-ended Differential Ref Input

1.2.3 Serial Connection

The EVB can be connected to a computer via a USB-C connector. The on-board USB-to-MPSSE Bridge (FTDI FT232HQ) can handle the data communication. The +5V from the USB-C powers the on-board regulators or external +5V via banana connector.

RC2121xA devices only supports I²C. Pins 1 and 2 in J65 are SDA and SCL from the FTDI chip. Pins 3 and 4 pass the SDA and SCL to the I²C level shifter. To use the on-board FTDI chip, install jumpers on pins 1–3 and 2–4. Pin 6 can be used as the ground connection for the I²C connection. By removing this jumpers, pins 3, 4, 5 and 6 are arranged so that an Aardvark connector can be plugged onto these pins (see Figure 6).

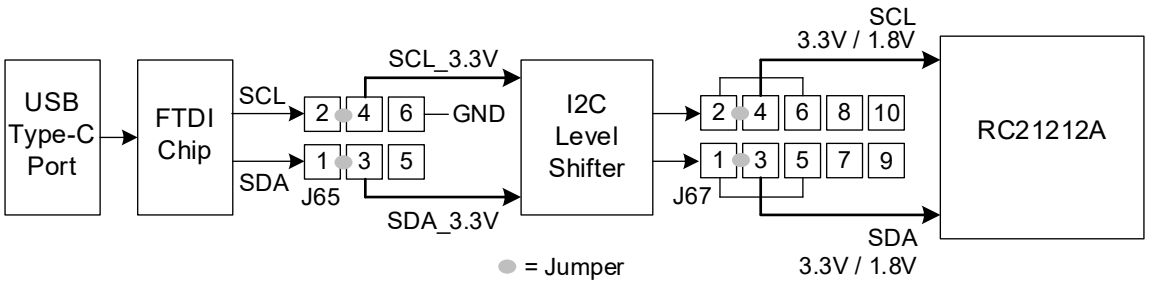


Figure 6. Communication Setup for I²C Mode

In Figure 7, the Aardvark adapter communicates with the RC21211/RC21212.

Figure 7. Aardvark Adapter Connection to J65

1.2.4 GPI/GPIO DIP Switch Selectors

The EVB has two DIP switches (SW1, SW2) to support GPIO and GPI pins on an RC21211/RC21212 device. The middle position leaves the pin open so GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, and GPIO6 could be configured to be 2-level (Hi / Low) as default selection on DIP switches. This is the default setting for each switch on the EVB board. Move to the “+” side to pull the pin high and move to the “-” side to pull the pin low.

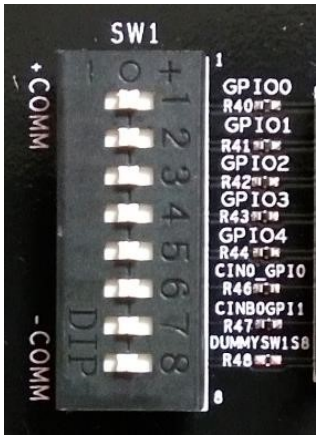


Figure 8. DIP Switch SW1

Table 4. SW1 Description

Switch 1 = GPIO0	Connects to Pin13 as general-purpose input/output 0. Set to middle as default on EVB.
Switch 2 = GPIO1	Connects to Pin14 as general-purpose input/output 1. Set to middle as default on EVB.
Switch 3 = GPIO2	Connects to Pin15 as general-purpose input/output 2. Set to middle as default on EVB.
Switch 4 = GPIO3	Connects to Pin16 as general-purpose input/output 3. Set to middle as default on EVB.
Switch 5 = GPIO4	Connects to Pin17 as general-purpose input/output 4. Set to middle as default on EVB.
Switch 6 = NA	Connects to Pin5 as general-purpose Input 0. Set to middle as default on EVB.
Switch 7 = NA	Connects to Pin6 as general-purpose Input 1. Set to middle as default on EVB.
Switch 8 = NA	No connection.

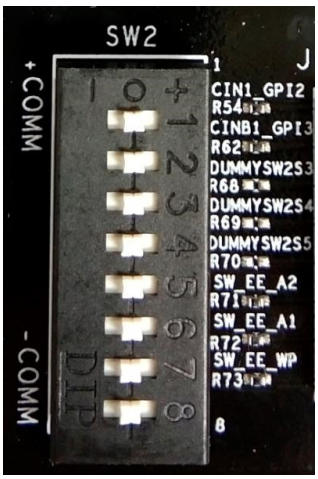


Figure 9. DIP Switch SW2

Table 5. SW2 Description

Switch 1 = GPIO5	Connects to pin 8 as general-purpose input/output 5. Set to middle as default on EVB.
Switch 2 = GPIO6	Connects to pin 9 as general-purpose input/output 6. Set to middle as default on EVB.
Switch 3 = Dummy	No connection.
Switch 4 = Dummy	No connection.
Switch 5 = Dummy	No connection.
Switch 6 = NA	No connection.
Switch 7 = NA	No Connection.
Switch 8 = NA	No Connection.

GPI pins are only available for use in single crystal input variants. In order to use GPI0 and GPI1 in dual crystal/reference input variants, XTAL1 must not be used. GPIO pins 5 and 6 can also be pulled Hi / Lo by applying voltage on SMA J8 and J9.

1.2.5 Outputs

For RC21211/RC21212, twelve differential output pairs can be programmed (out_mode) to LVDS, LP-HCSL or LVCMOS logic type. LVCMOS is a single-ended logic type, and the output pair will essentially be two CMOS outputs of the same frequency.

LP-HCSL is the most versatile output because it can be customized. The LP-HCSL driver is simply a voltage push-pull driver. The RC21211/RC21212 LP-HCSL can be programmed (out_lpamp) to different amplitudes (800mV, and 900mV). The slew rate can be programmed (out_lpsr) to slow, 2–4 V/ns or fast, > 4V/ns. The output impedance can be programmed (out_lpimp) to 100Ω or 85Ω differential. When AC coupled, the LP-HCSL driver can be compatible with LVDS and LVPECL signal swing requirements. The single-ended outputs support LVCMOS swings of 1.8V or 3.3V as determined by their VDDO voltage.

For LVCMOS output type, output phase can be programmed (out_prog0 or out_prog1) to be out-of-phase or in-phase. Each output can also be tri-stated (out_prog2/out_prog3). The slew rate can also be programmed (out_cmdrv) to 4.2 / 2.7 / 3.4 V/ns for 3.3V, or 1.8 / 1.9 V/ns for 1.8V.

RC2121xA devices are defaulted with LP-HCSL output type on all outputs of the EVB. Figure 10 shows the default output termination for LP-HCSL with SMA connectors (J35, J39).

Note: Some features of this EVB are not available for RC2121xA devices. In Figure 11, **DNI** denotes *Do Not Install*.

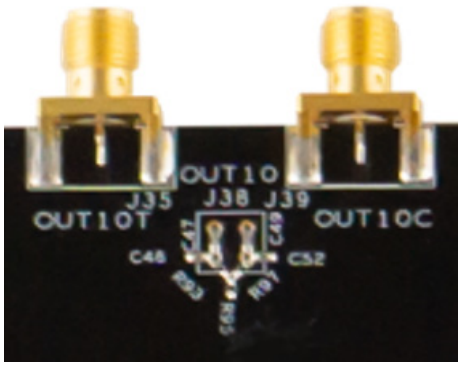


Figure 10. Output Termination with SMA Connector

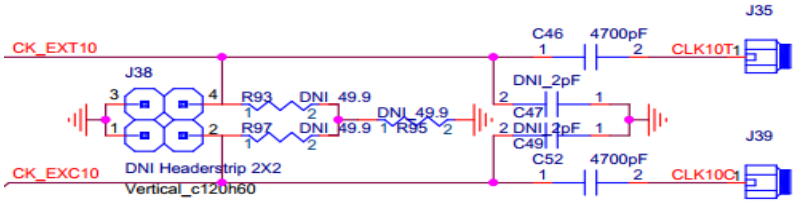


Figure 11. Output Termination with Bias Schematic

1.2.6 Power and USB connection to Computer Host

The EVB is connected to a computer via the USB cable (see section 1.2.3) and is recommended that the cable is connected to a USB 2.0 port. The USB provides +5V as power source to the on-board regulators. The on-board regulators support 3.3V and 1.8V voltages to the entire EVB.

The voltage source can be either from on-board voltage regulators for 3.3V, 1.8V or from VDD_J banana connector. The banana connector can connect to a bench supply and the connection can be used to measure total supply current into pins as reference. When all powers are selected from the VDD_J power jack, the USB connection will still be needed to connect to the computer for programming RC2121xA devices using RICBox.

In Figure 12, the source for pin VDDO1 (J52) is chosen to be VDD_J. To select 3.3V, the jumper can be moved to the top of header J52.

Important: Do not use 2.5V power supply for RC2121xA devices. For more information, refer to the RC2121xA datasheet.

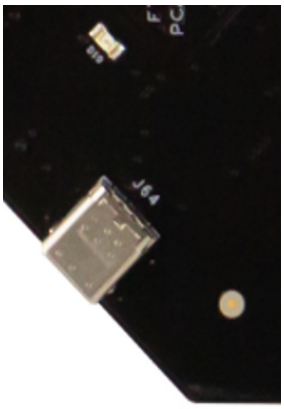


Figure 12. Power Source from USB Connector

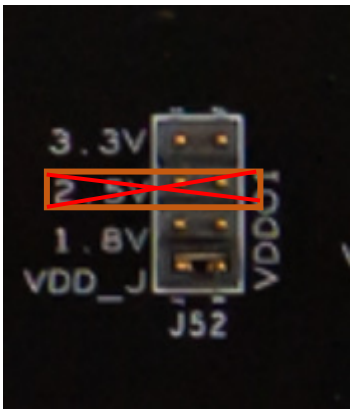


Figure 13. Power Source Selection

1.2.7 Renesas Integrated Circuit Toolbox (RICBox)

The Renesas Integrated Circuit Toolbox (RICBox) software can program RC2121xA devices on the EVB using either the on board FTDI chip or Aardvark tool. RICBox provides a user-friendly interface to support programming configurations into an RC2121xA device on the board. For more information about RICBox, see the Renesas IC Toolbox User Guide.

1.2.8 Programming an RC2121xA Device using RICBox Software

1. Connect J64 on the EVB to the user's computer using a USB cable.
2. Launch RICBox as described in the Renesas IC Toolbox User Guide.
   a. The software and guide are downloadable from the product page.
3. For a new configuration, click on *Create new project*.

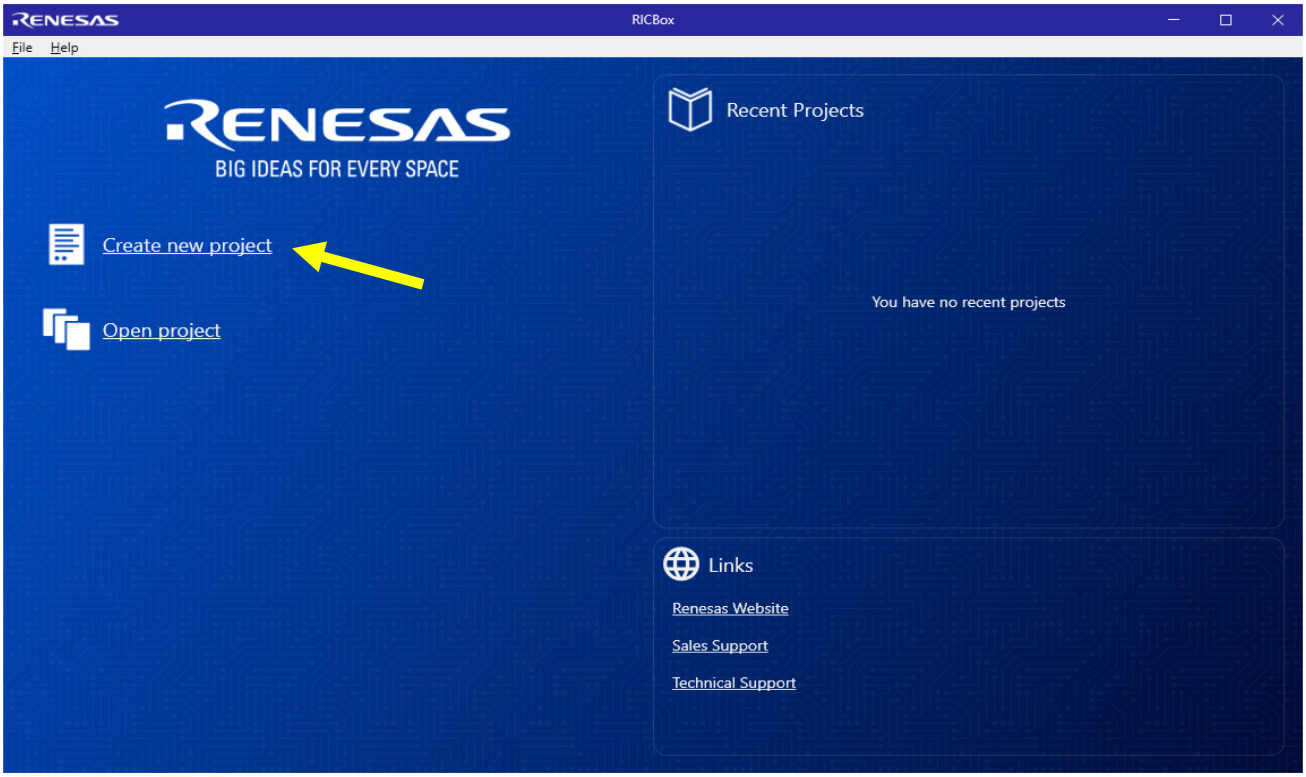


Figure 14. RICBox Start Page

4. Select the AutoClock product family, then select a product variant (part number) and click *OK*.

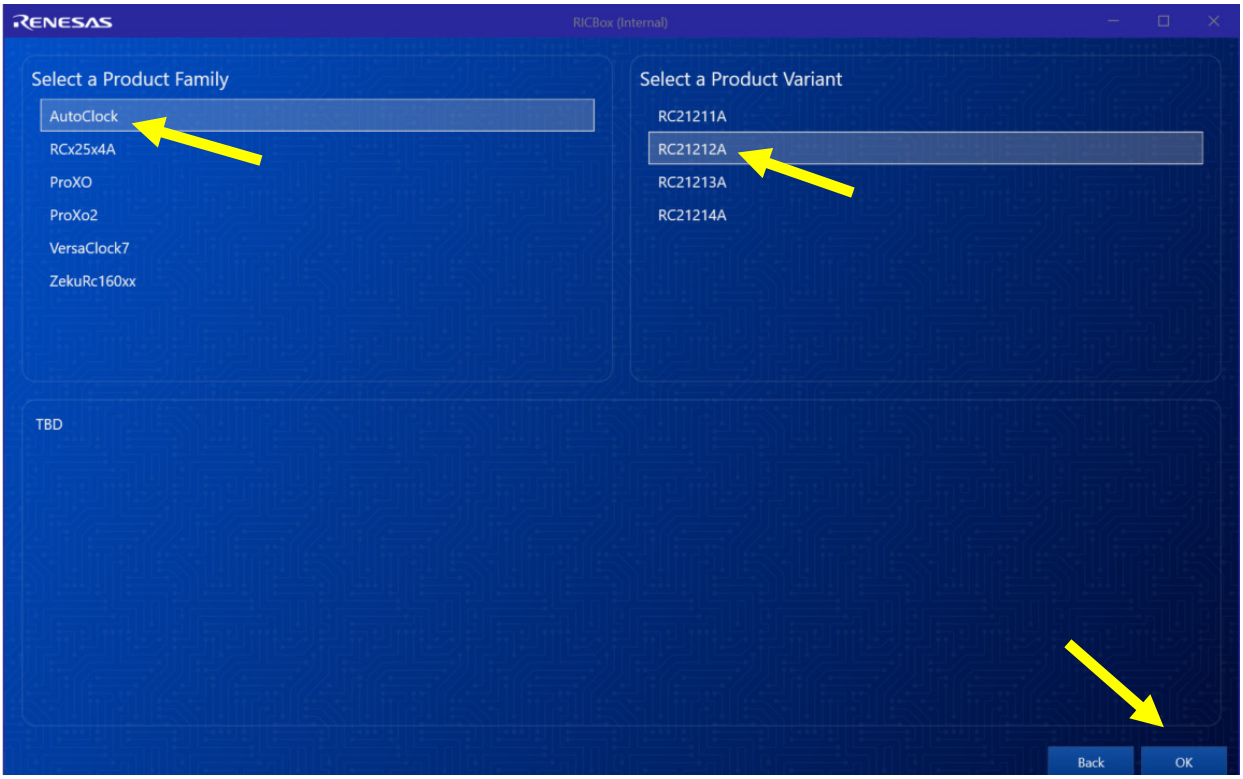


Figure 15. Select Product Family and Variant

5. On the Inputs wizard page, mode for XTAL0/1 REFIN0/1 can be set (Xtal, Differential, Single-ended). Expected input frequency needs to be entered. The C_L can also be set internally between 6pF to 12pF.

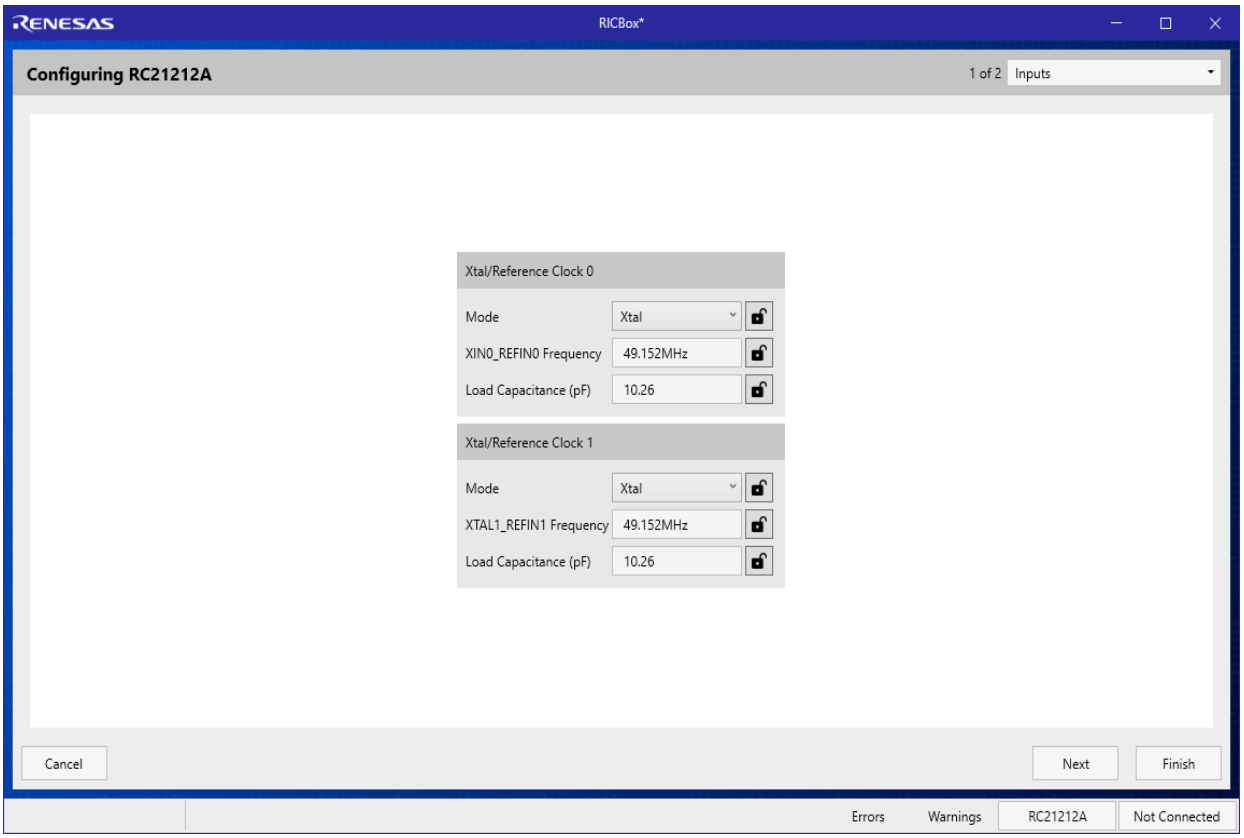


Figure 16. Inputs Wizard Page

6. Configure the output bank settings which includes the divider source (LPFOD0/1, IOD0/1, or HPFOD0/1/2), output frequency and output mode (LPHCSL, LVDS, and LVCMOS). If a bank is to be unused, use the "Power Down" check box to turn off the bank. Click on the settings icon to adjust amplitude, impedance, and slew rate for each output (see Figure 18).

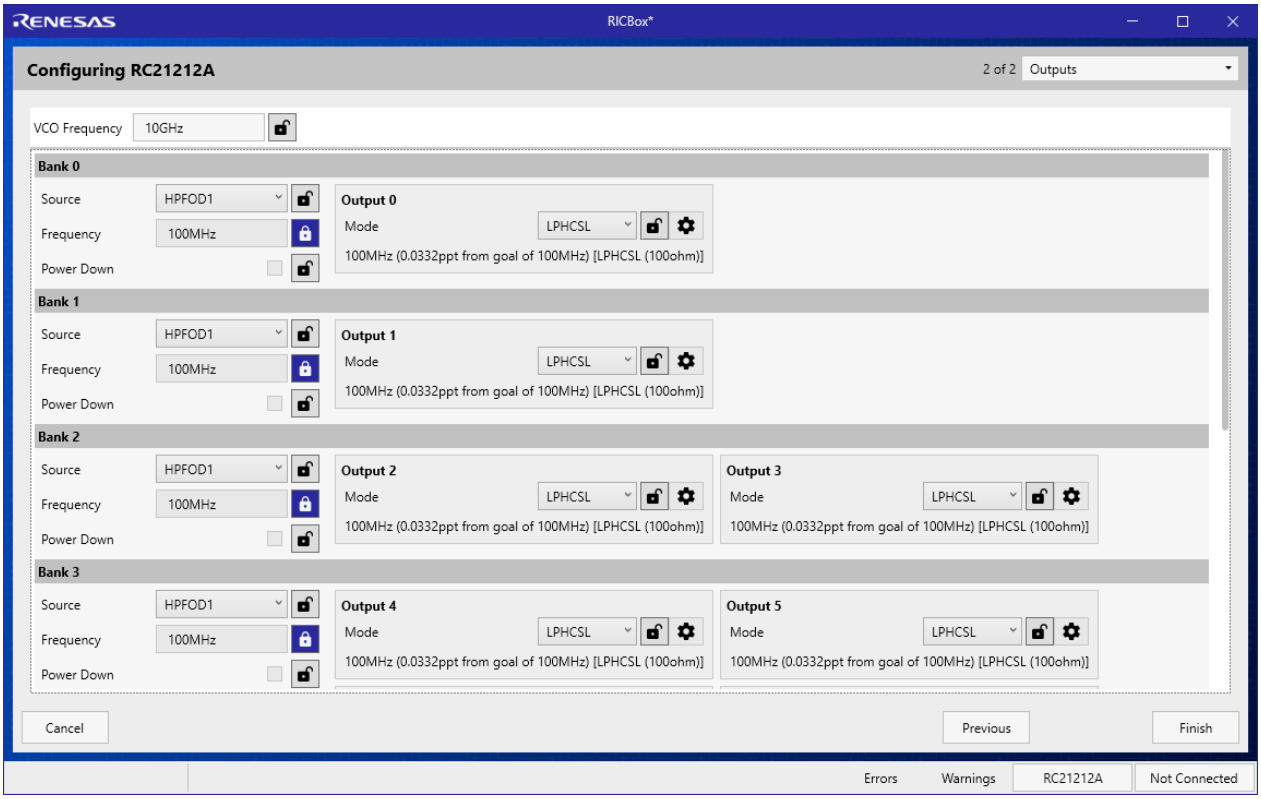


Figure 17. Outputs Wizard Page

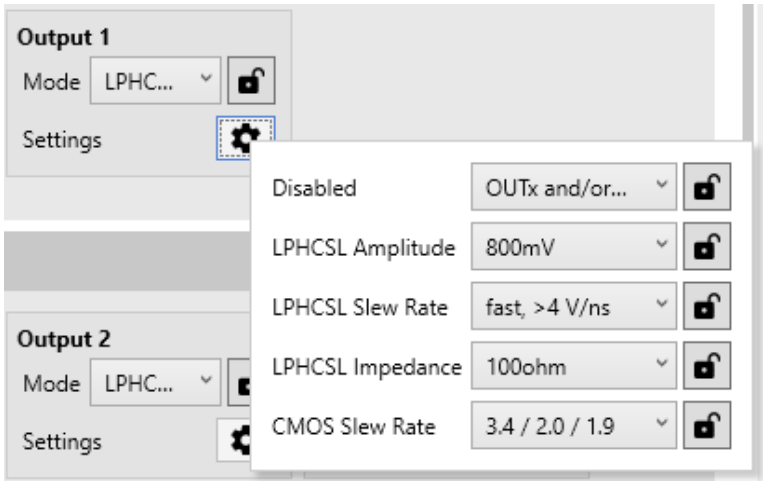


Figure 18. Advanced Output Settings

7. Click the *Finish* button (see Figure 17) to view the summary of the configuration.

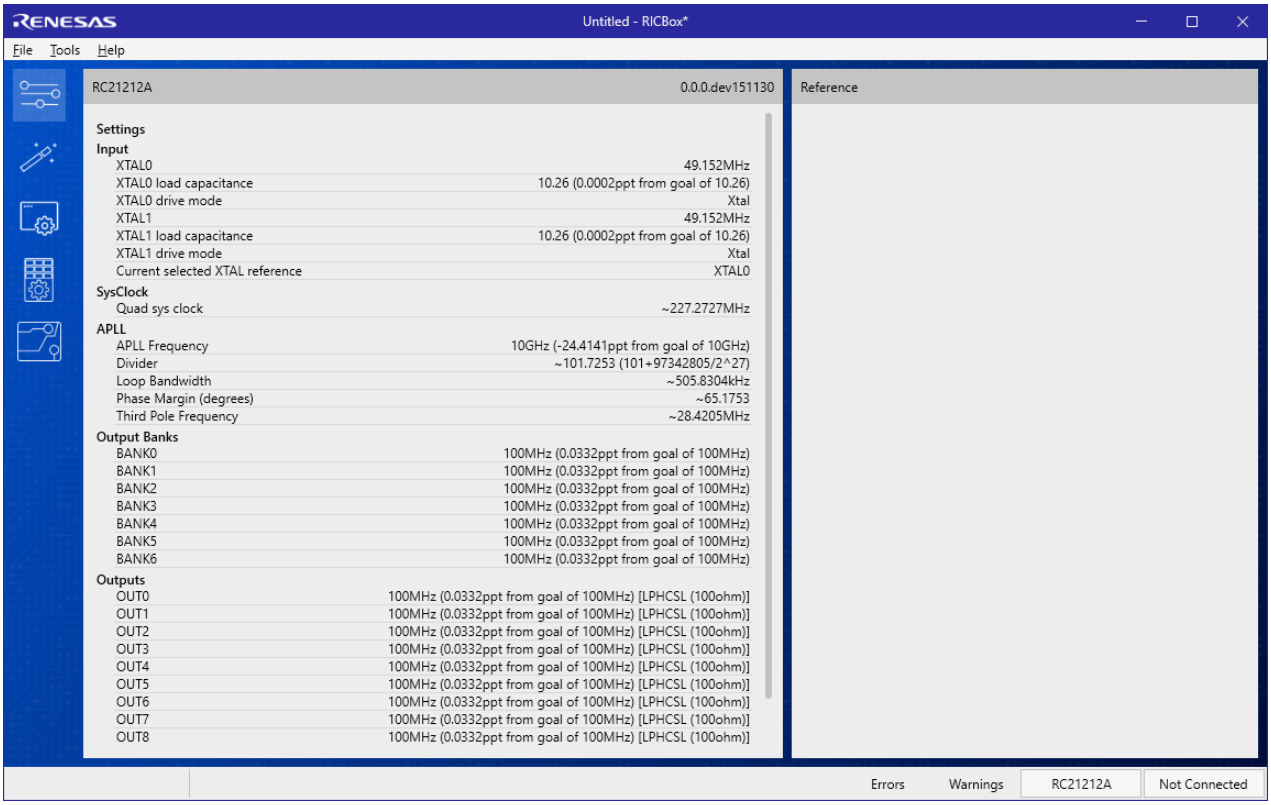


Figure 19. Configuration Summary

8. To go back to any of the previous wizard pages, click the wizard  icon.
9. RICBox is now ready to connect to an RC2121xA device. Clock on the *Not Connected* button in the lower right part of RICBox tool. Then click *Connect*.

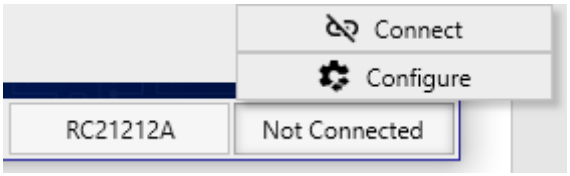


Figure 20. Connect to AutoClock

10. The “Not Connected” button will turn green and changed to “Connected”. Click the *Connected* button again and select “Program” to start programming the part.

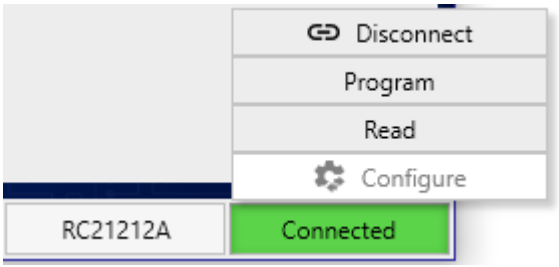


Figure 21. Program AutoClock

11. View the block diagram by pushing the Block Diagram  icon.

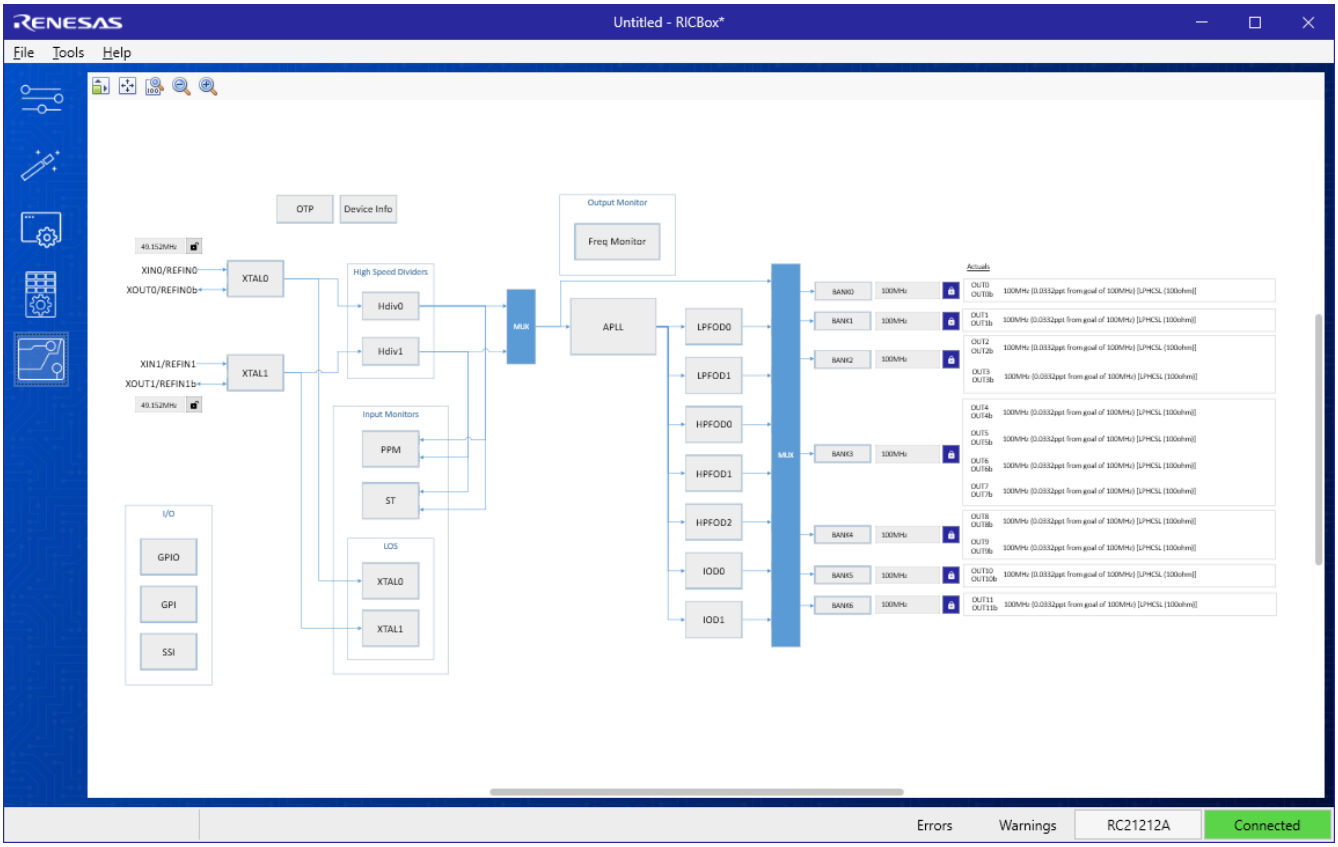


Figure 22. Block Diagram

2. Evaluation Board Components

2.1 Layout Guidelines

Use the following list of items and their guidelines when designing the layout around the RC2121xA devices.

2.1.1 ePAD

For maximizing heat removal, a land pattern must be incorporated on the PCB within the footprint of the package corresponding to the exposed metal pad or exposed heat slug. Design in sufficient clearance on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts. Ensure there are enough vias to allow for proper thermal dissipation. These vias act as “heat pipes”. A via diameter around 12 to 13 mils (0.30 to 0.33 mm) with 1oz copper via barrel plating is recommended. Precaution should be taken to eliminate any solder voids between the exposed heat slug and land pattern. The ePAD may be connected to VEE (negative power supply) to allow for split power planes for different input/outputs styles (see Figure 23).

Note: These recommendations are to be used as a guideline only. For additional information, see the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead Frame Base Package, Amkor Technology.

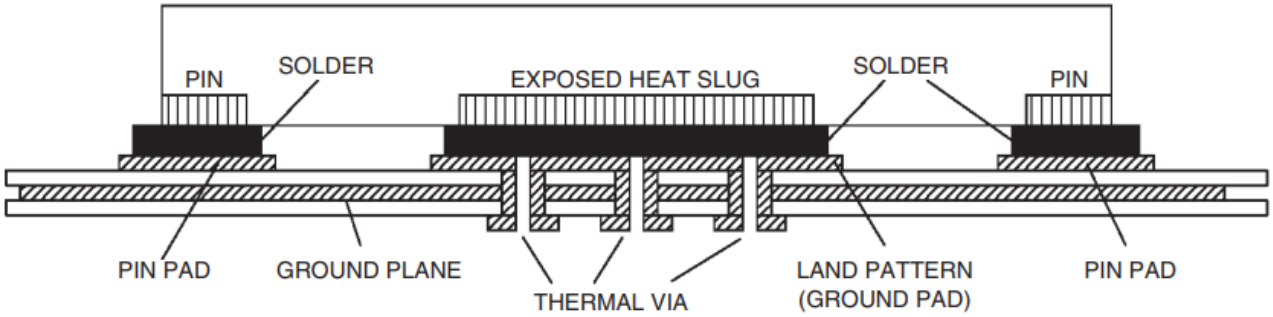


Figure 23. PCB Assembly for Exposed Pad Thermal Release Path – Side View

Table 6.Thermal Characteristics (40-pin)

Symbol	Parameter [1]	Value	Unit
θ_{JC}	Junction to Device Case Thermal Coefficient [2]	26.9	°C/W
θ_{JB}	Junction to Board Thermal Coefficient [2]	1.3	
θ_{JA}	Junction to Ambient Air Thermal Coefficient (still air)	30.5	
	Junction to Ambient Air Thermal Coefficient (1m/s airflow)	26.8	
	Junction to Ambient Air Thermal Coefficient (2m/s airflow)	25.2	
	Junction to Ambient Air Thermal Coefficient (3m/s airflow)	24.3	
-	Moisture Sensitivity Rating (Per J-STD-020)	3	-

1. Multi-Layer PCB with two ground and two voltage planes.
2. Assumes ePAD is connected to a ground plane using a grid of 25 thermal vias

Table 7 Thermal Characteristics (48-pin)

Symbol	Parameter [1]	Value	Unit
θ_{JC}	Junction to Device Case Thermal Coefficient [2]	20.1	°C/W
θ_{JB}	Junction to Board Thermal Coefficient [2]	1.9	
θ_{JA}	Junction to Ambient Air Thermal Coefficient (still air)	25.2	
	Junction to Ambient Air Thermal Coefficient (1m/s airflow)	21.7	
	Junction to Ambient Air Thermal Coefficient (2m/s airflow)	20.2	
	Junction to Ambient Air Thermal Coefficient (3m/s airflow)	19.3	
-	Moisture Sensitivity Rating (Per J-STD-020)	3	-

1. Multi-layer PCB with two ground and two voltage planes.
2. Assumes ePAD is connected to a ground plane using a grid of 25 thermal vias.

2.1.2 Crystal/Reference Input

Place the crystal as close to the AutoClock device as possible. Make XIN/XOUT trace lengths the same. For external tuning caps, connect them from XIN/XOUT to ePAD reference voltage. For single-ended reference input, route only the REFIN trace as single-ended 50Ω. For differential input, route differential 50Ω.

2.1.3 Serial Connection

The serial interface can function from 1.8V to 3.3V for VDDD. If serial communication is needed, the SCL and SDA pull-up resistor needs to connect to VDDD. If needed, use a level translator. Acceptable values for pull-up resistors are 1kΩ to 10kΩ. It is recommended to route the serial signals close to each other.

2.1.4 GPI/GPIO

In order to utilize GPI, XTAL1 input must be disabled as they share the same pins. The logic levels are determined by VDDD relative VEE. The GPI/GPIO can be configured to have internal pull-up/down. Signals should be routed to minimize return loops.

2.1.5 Outputs

For LVCMOS outputs type, route single-ended 50Ω and place an inline 33Ω resistor near the AutoClock device. For differential outputs type, route differential 50Ω. For LPHCSL, an inline 7.5Ω resistor near the AutoClock device is needed if output impedance is set to 85Ω. For LVDS, add 100Ω across P and N if the receiver does not have built-in termination. Inline capacitors may be used to AC couple the outputs as needed.

2.1.6 Power

Please follow the recommended schematic for power filtering. Each 0.1µF needs to be placed as close as possible to the respective RC21212A power pin. For a 1.8V setup, choose feed-through capacitors that minimize voltage drop. For a 3.3V setup, recommended ferrite beads(as described in AN-805) can be used with a DC resistance of less than 0.4 ohms.

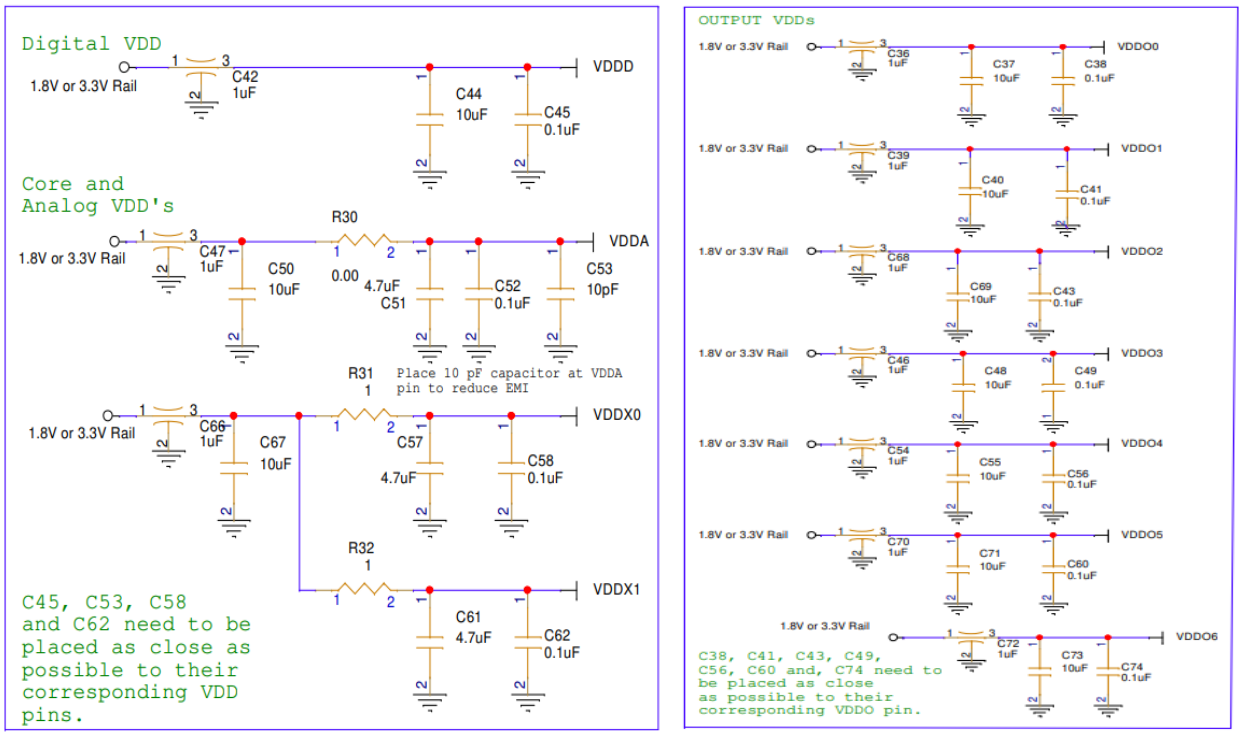


Figure 24. Power Supply Filtering

2.2 Schematic Diagrams

2.2.1 Schematics for 40-Pin VFQFPN

Schematics for the AutoClock 40-pin VFQFPN devise are appended at the end of this document.

2.2.2 Schematics for 48-Pin VFQFPN

Schematics for the AutoClock 48-pin VFQFPN devise are appended at the end of this document.

2.3 Board Layout

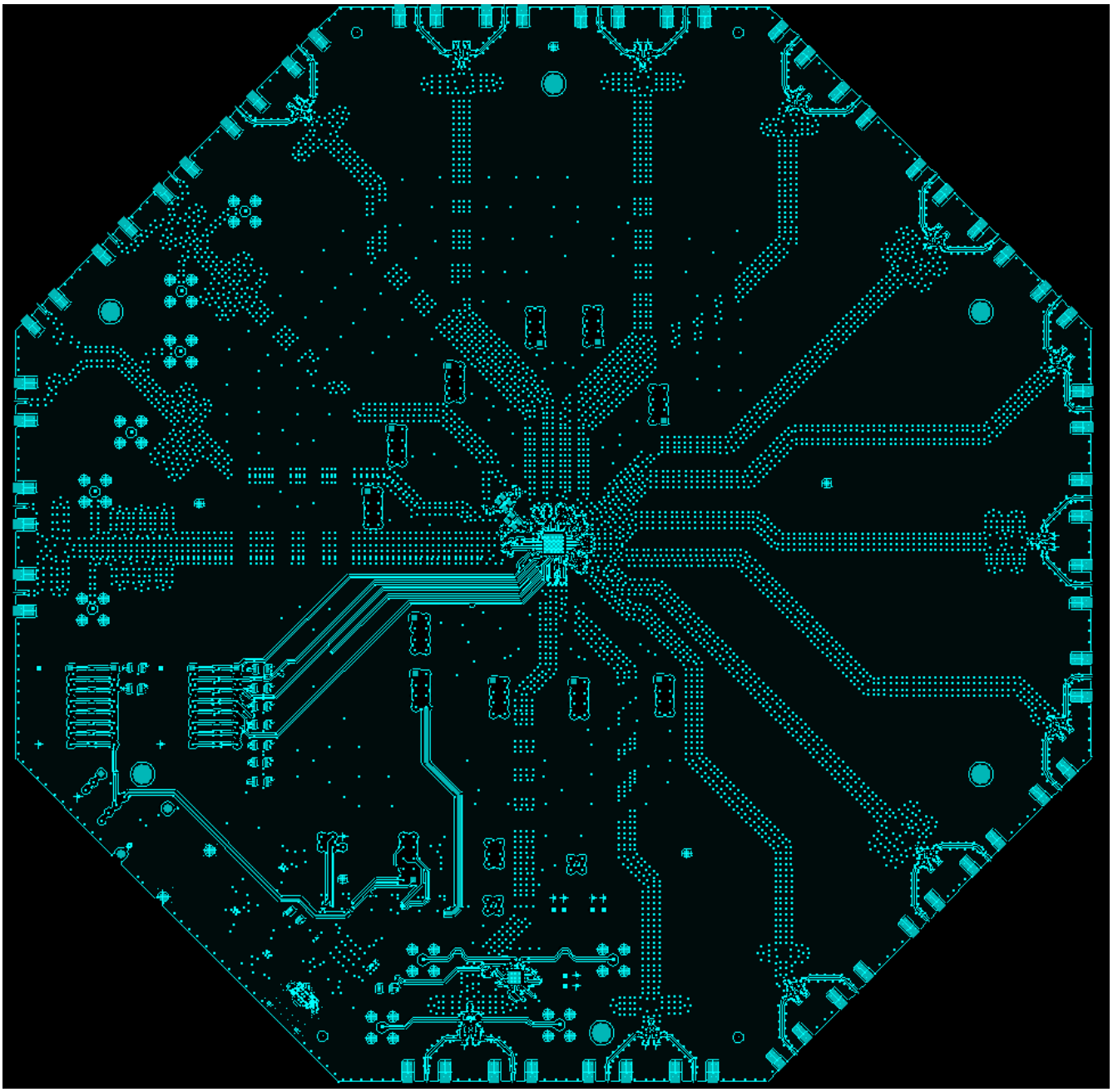


Figure 25. Layer 1 – Top

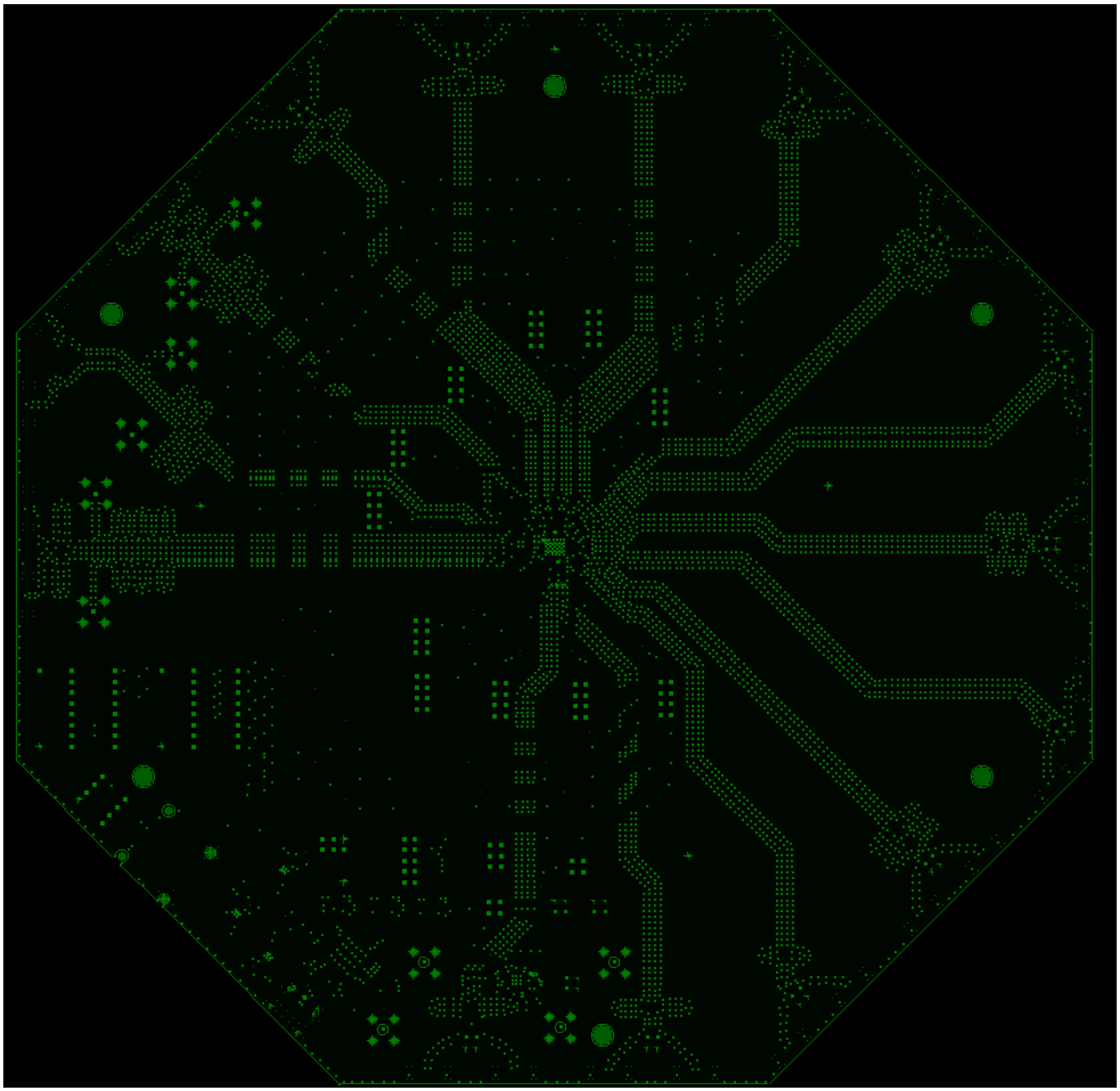


Figure 26. Layer 2 – Signal

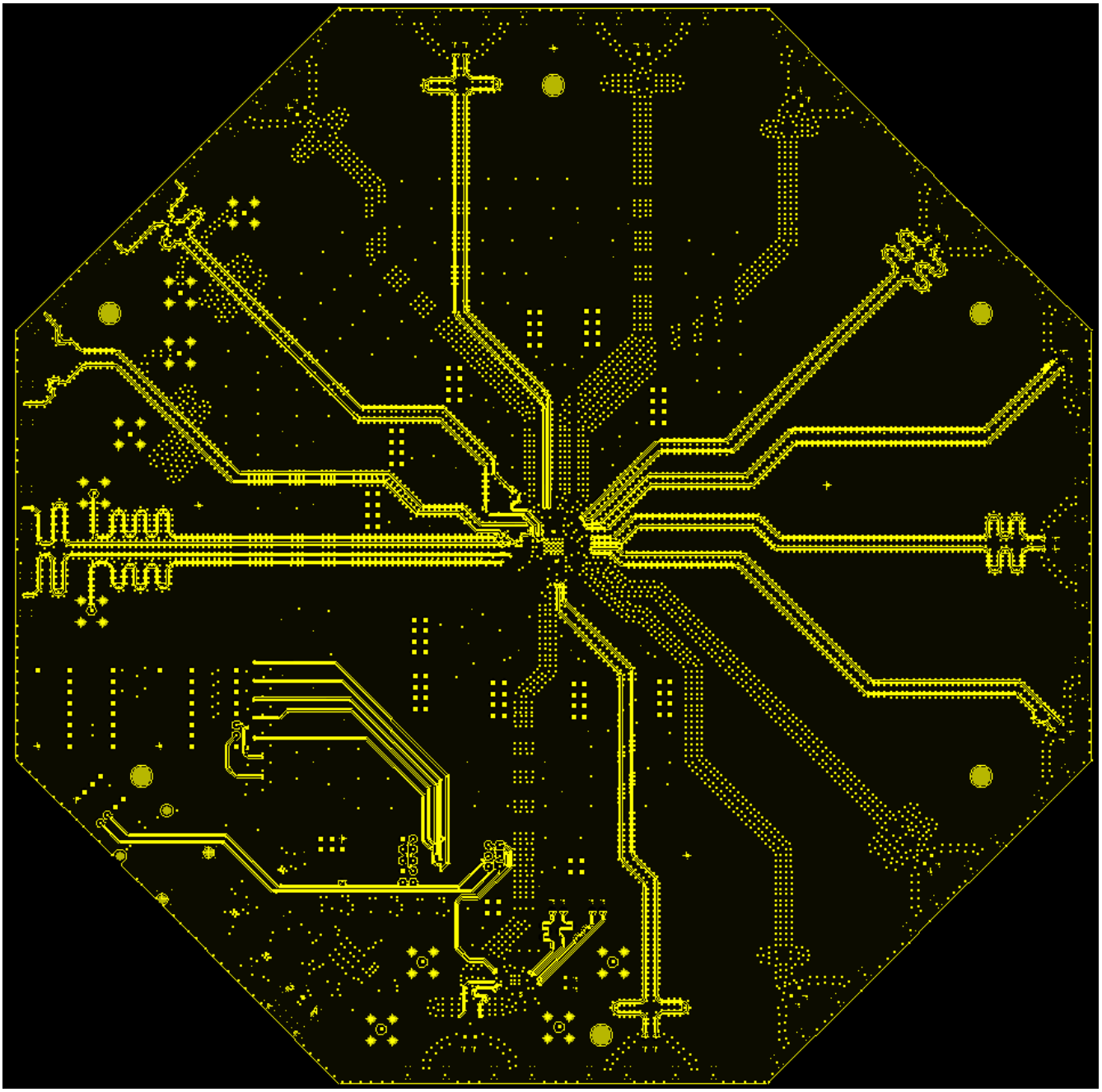


Figure 27. Layer 3 – Clock Signals

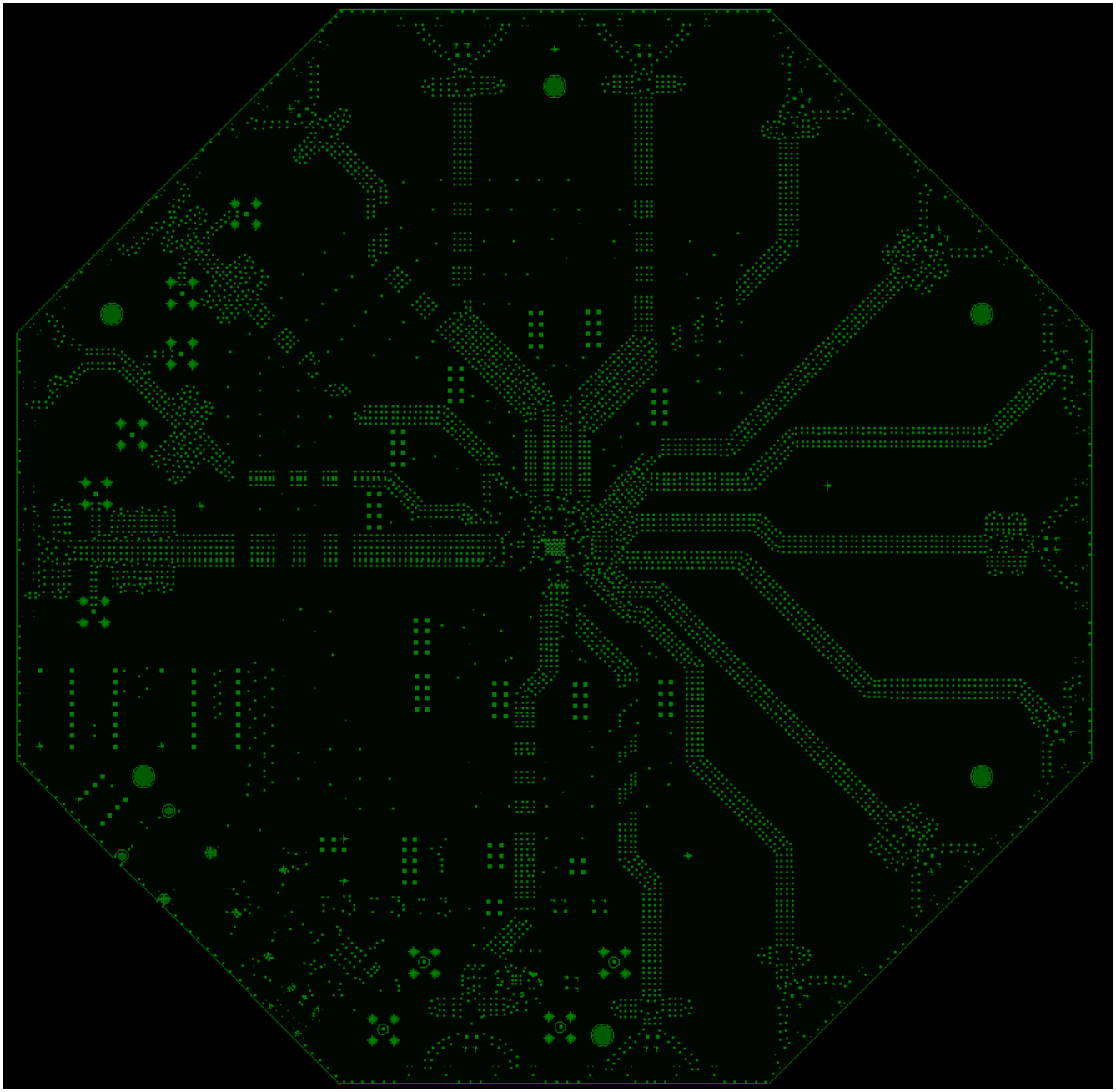


Figure 28. Layer 4 – GND Plane

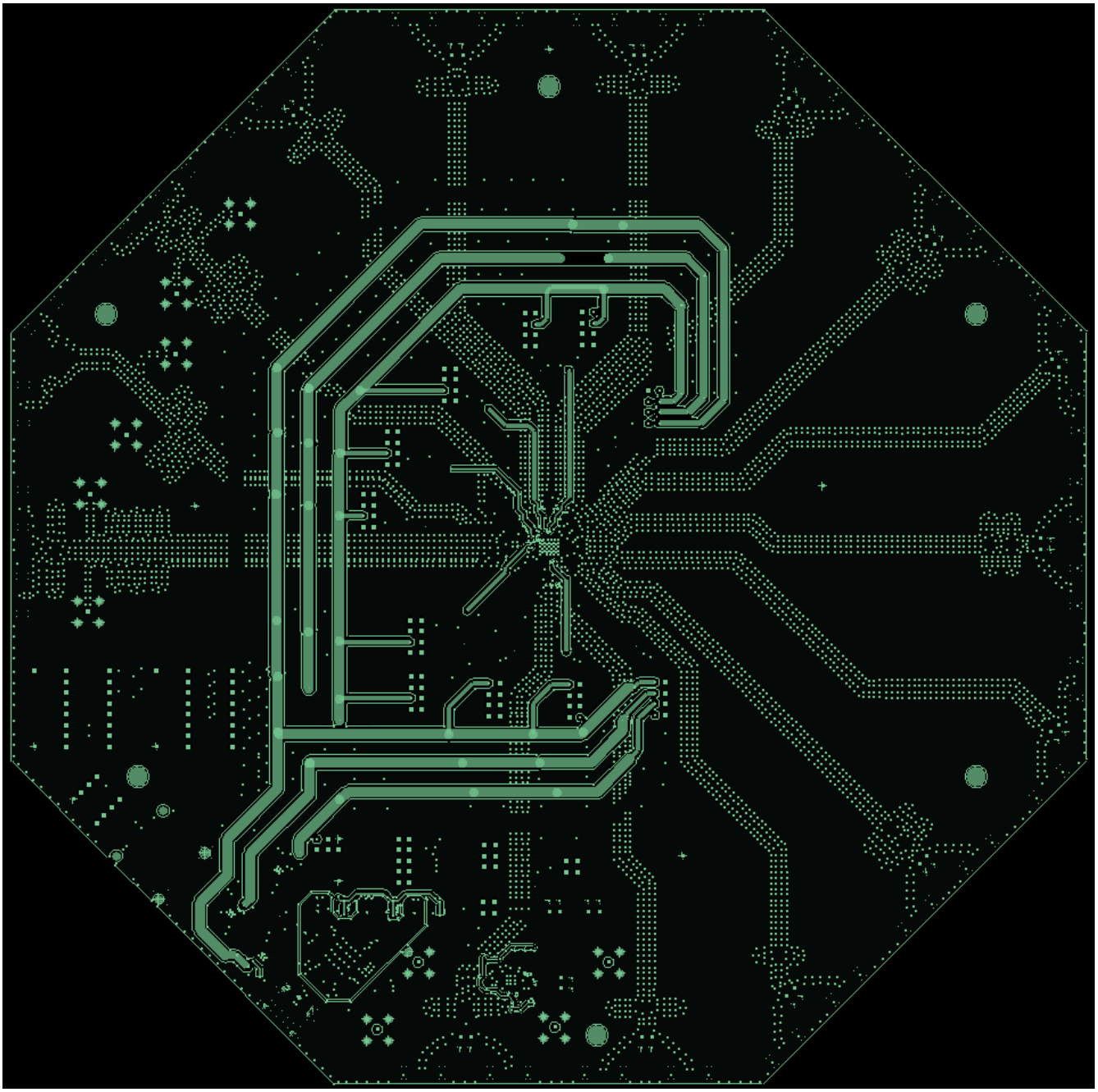


Figure 29. Layer 5 – Power Plane

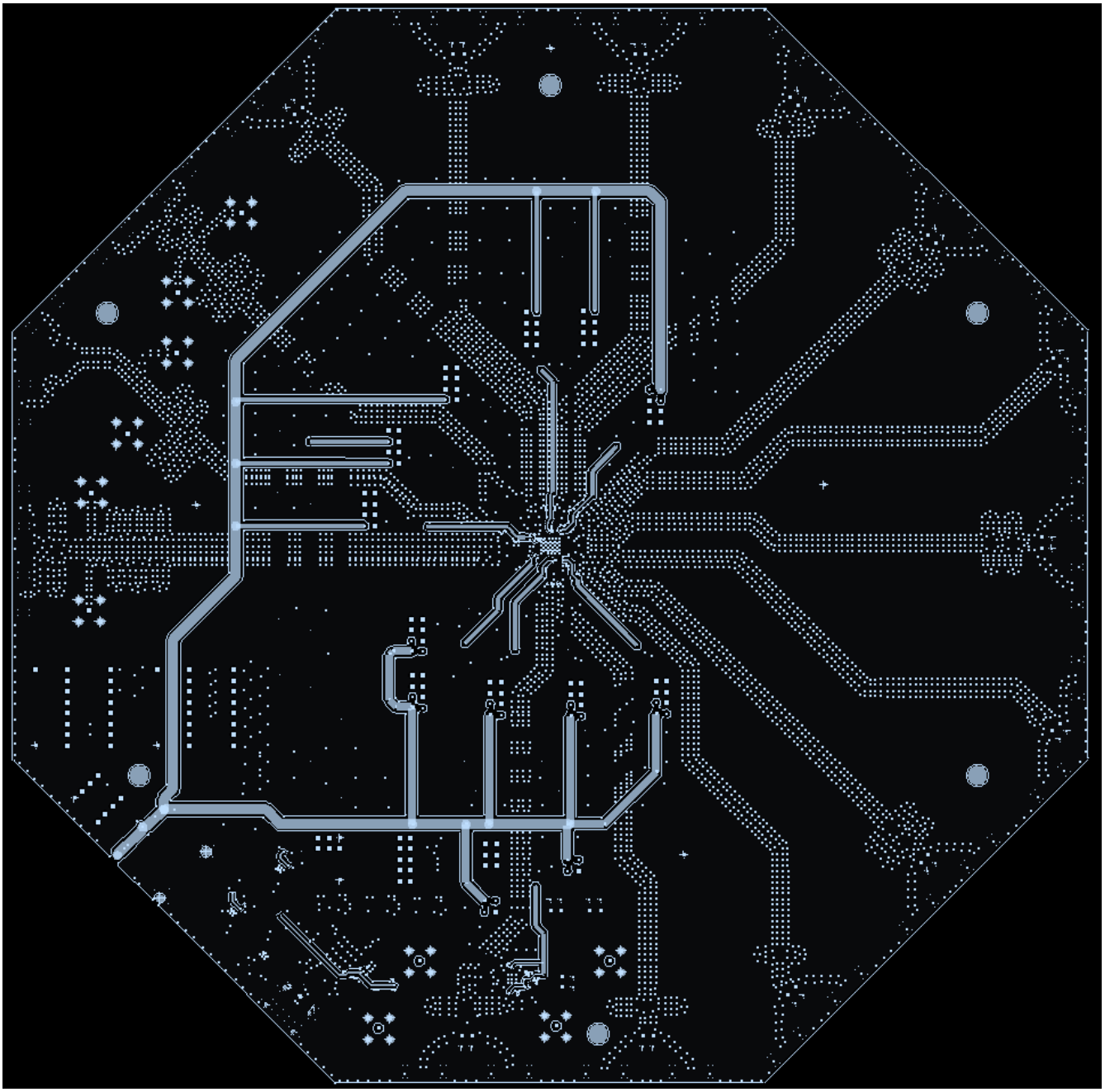


Figure 30. Layer 6 – Power Plane

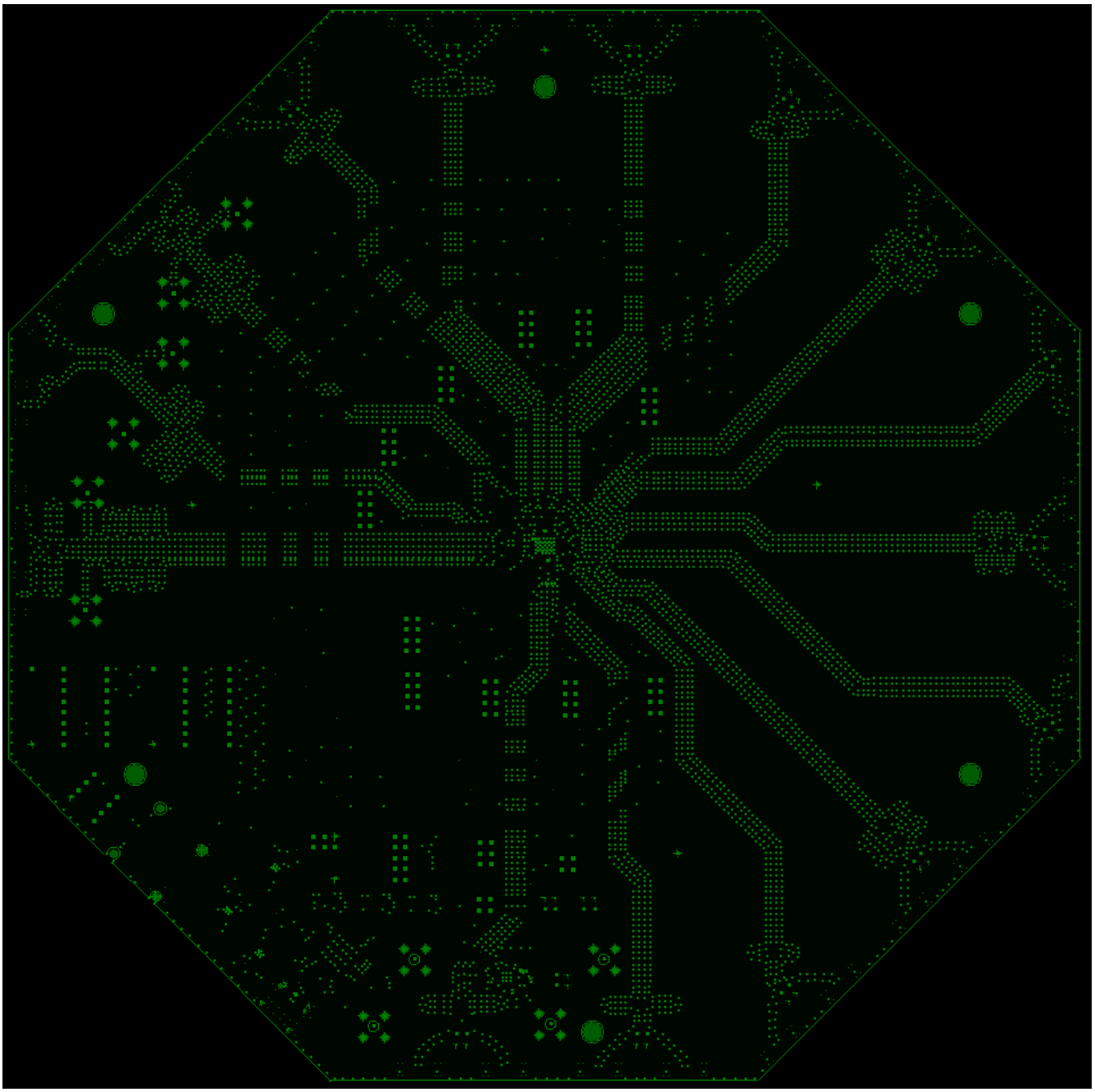


Figure 31. Layer 7 – Ground Plane

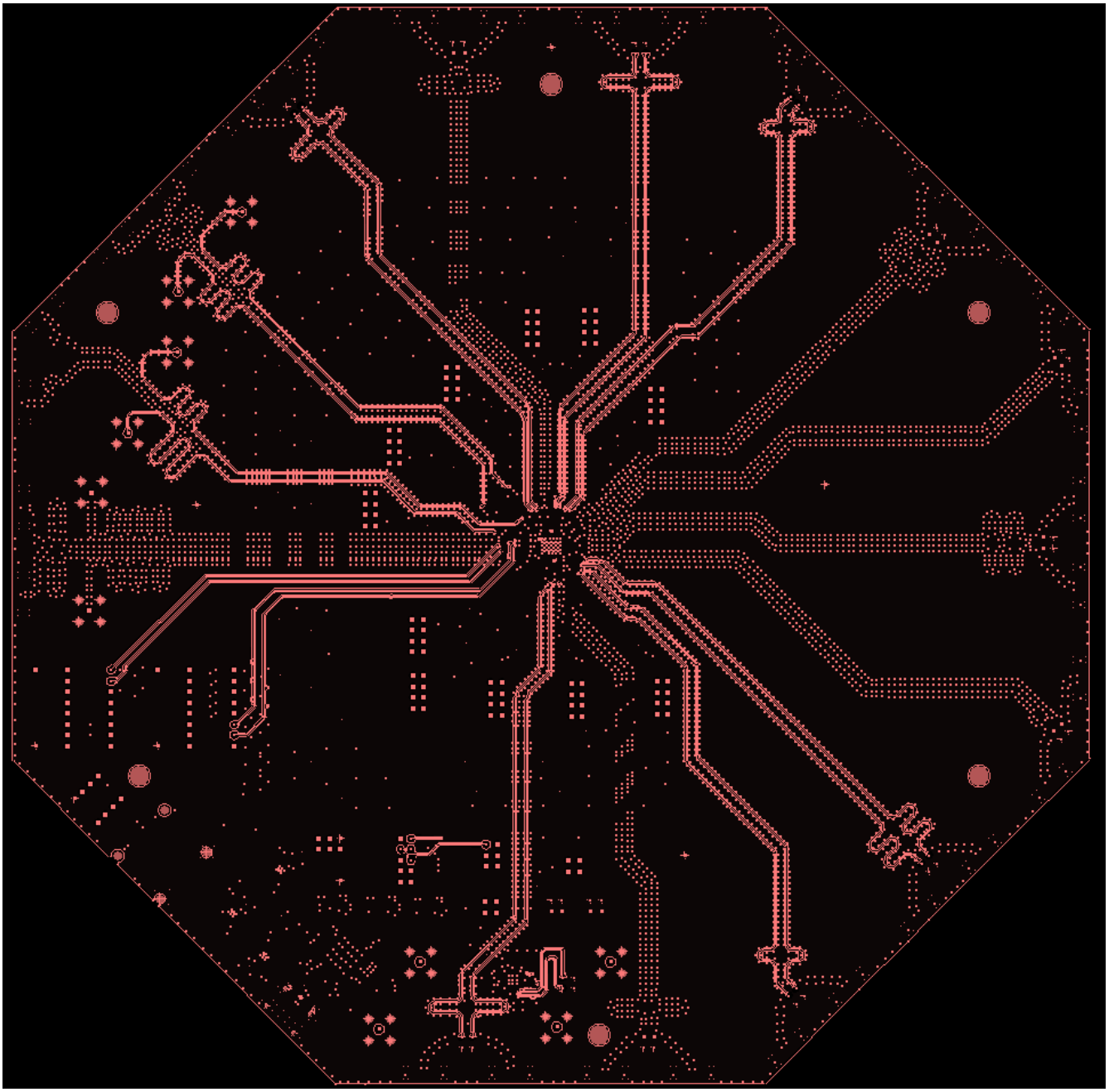


Figure 32. Layer 8 – Signal

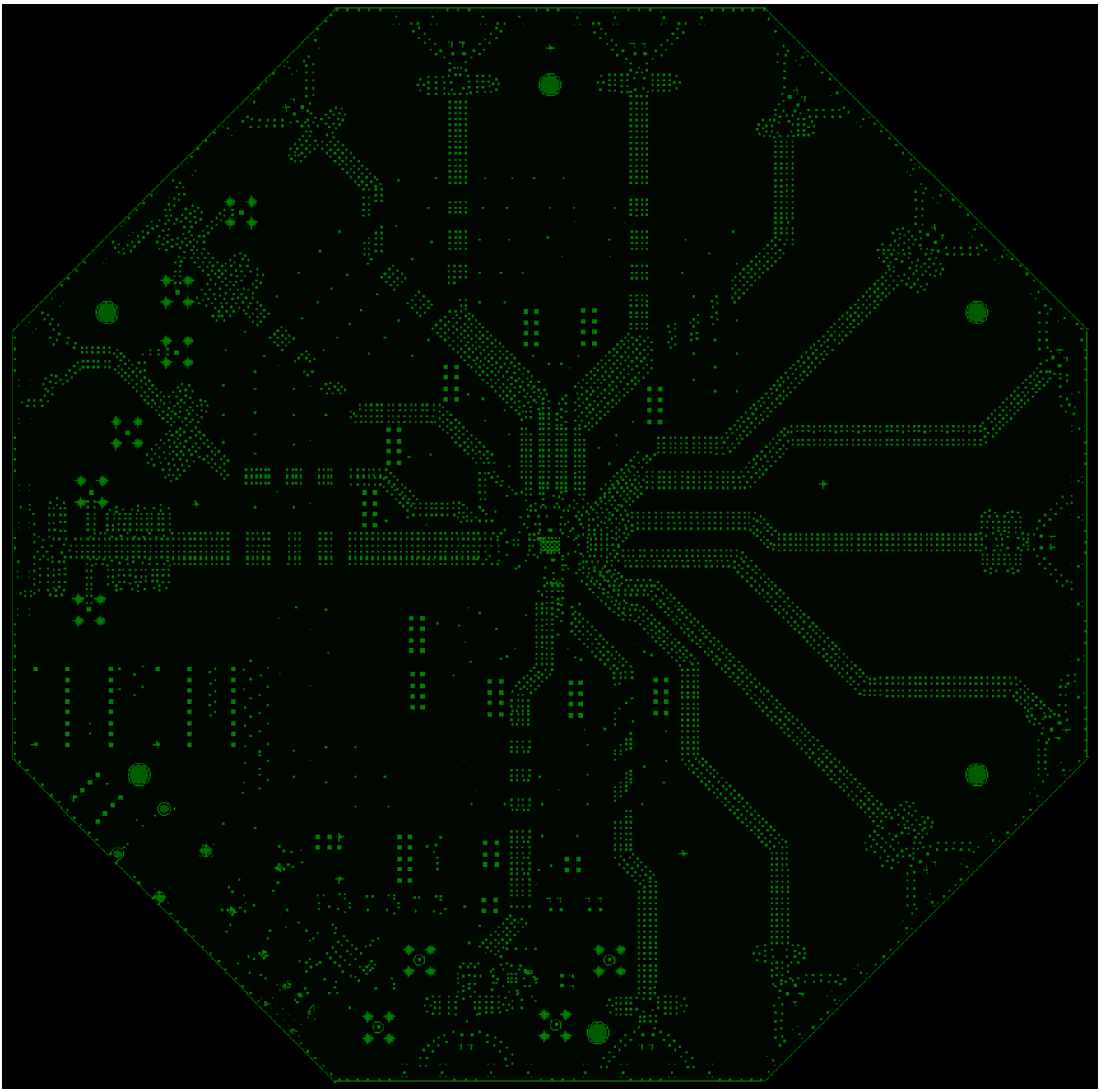


Figure 33. Layer 9 – Ground Plane

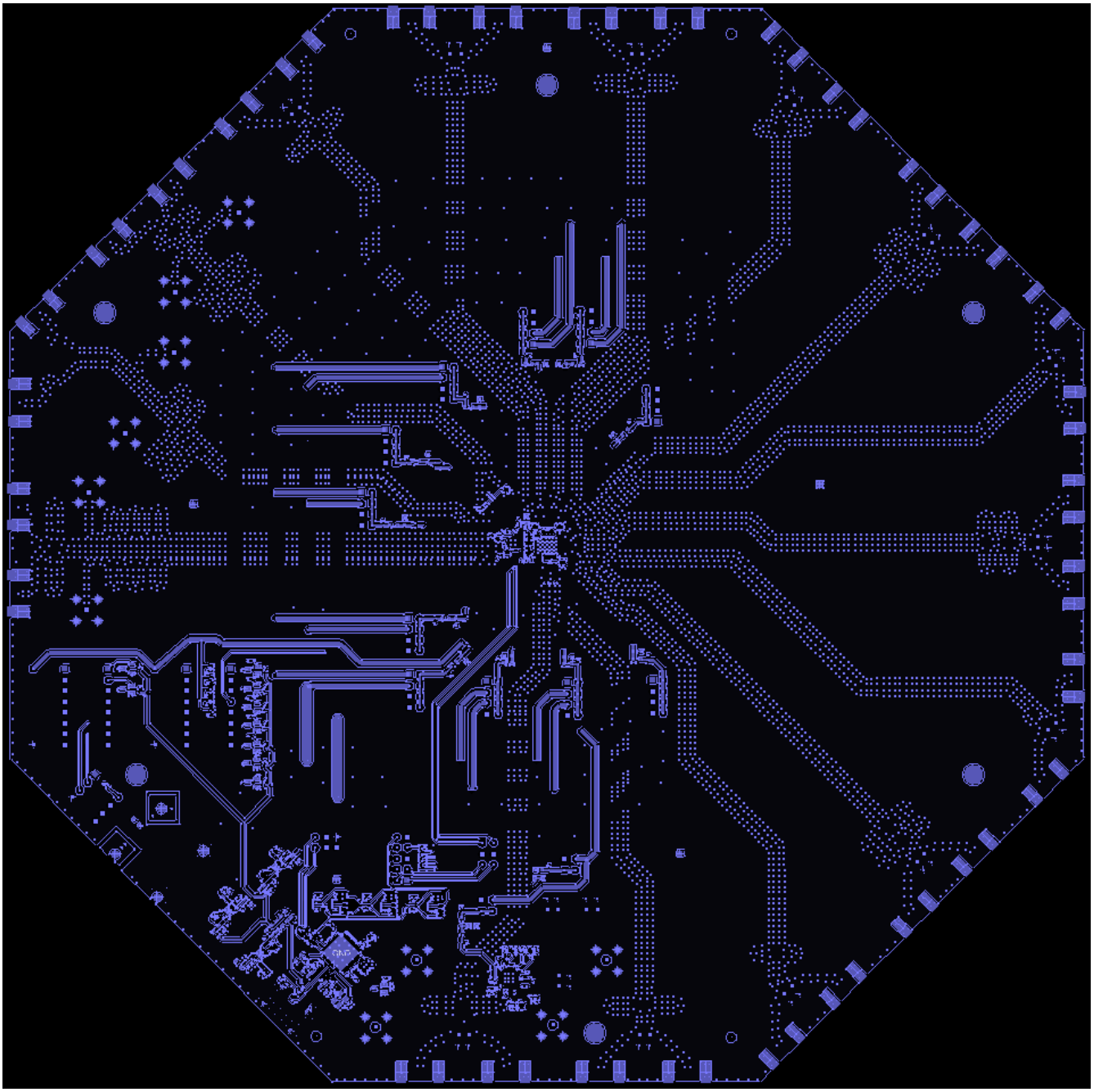


Figure 34. Layer 10 – Bottom

3. Quick Start Guide

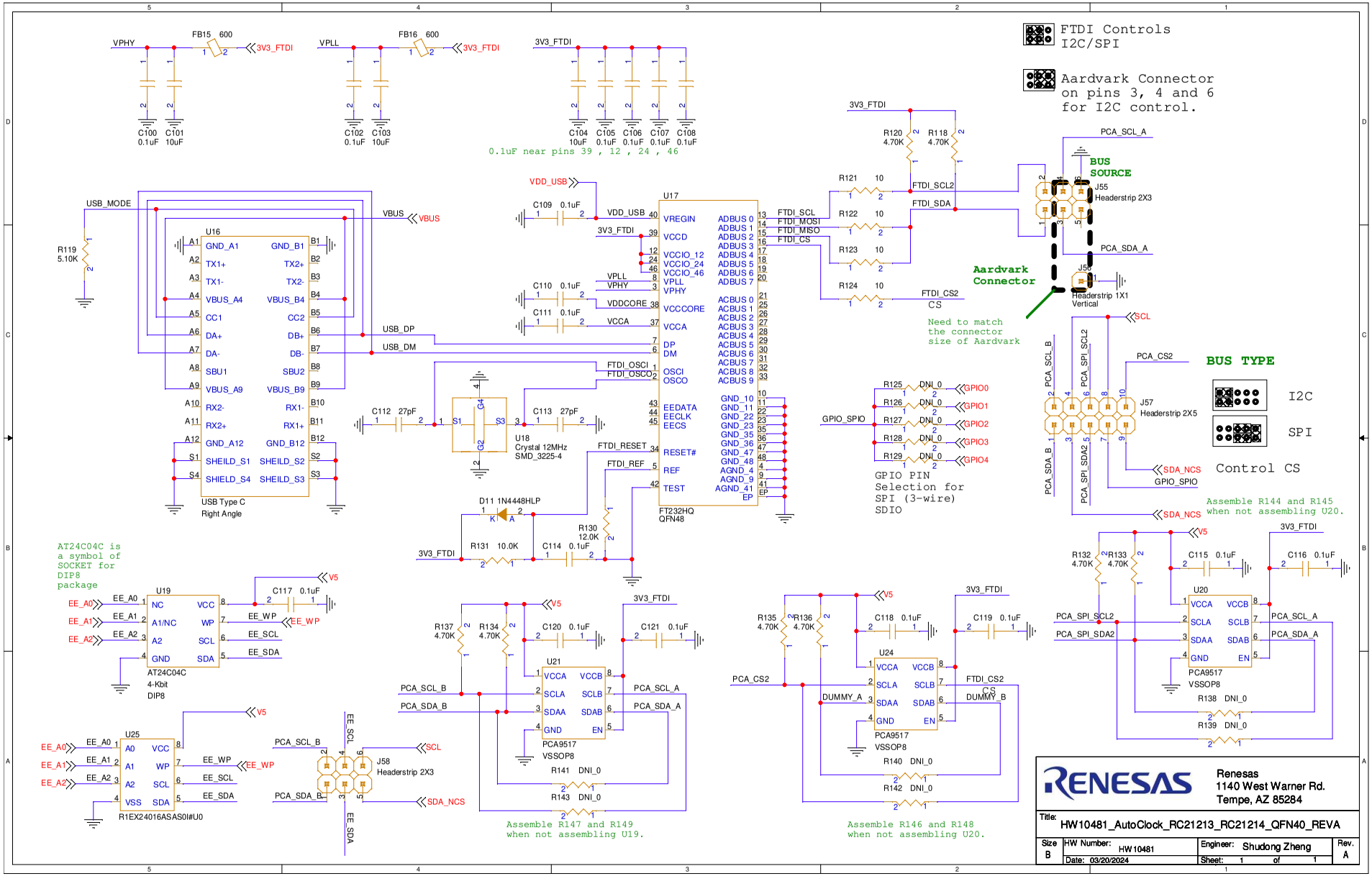
1. Initiate the process by connecting the Evaluation Board (EVB) to your computer using a USB-C cable. This connection will also provide power and set ups the communication to the board.
2. If you prefer using an external power instead of the USB, flip the power source selector on the EVB to 'VDD_J'.
3. Install the RICBox software. You'll find all the instructions in the Renesas IC Toolbox Software Manual.
4. After installing, configure your board as explained in section 1.2.7.
5. Program the board as per the configuration. This configuration can be saved in "**.rbs**" format.
6. Conduct your measurements using the Phase Noise Analyzer (PNA), such as the E5052 or FSWP.

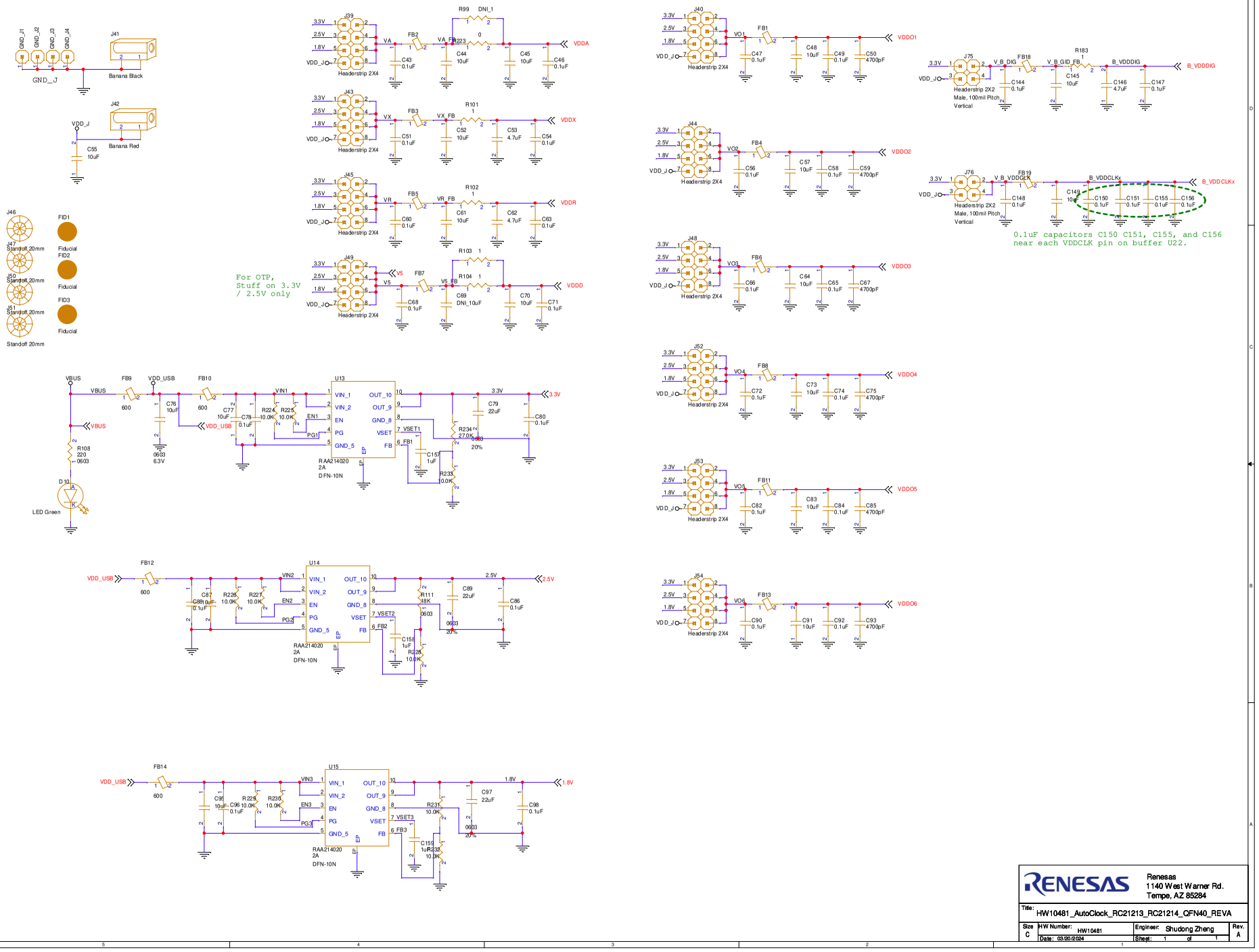
4. Ordering Information

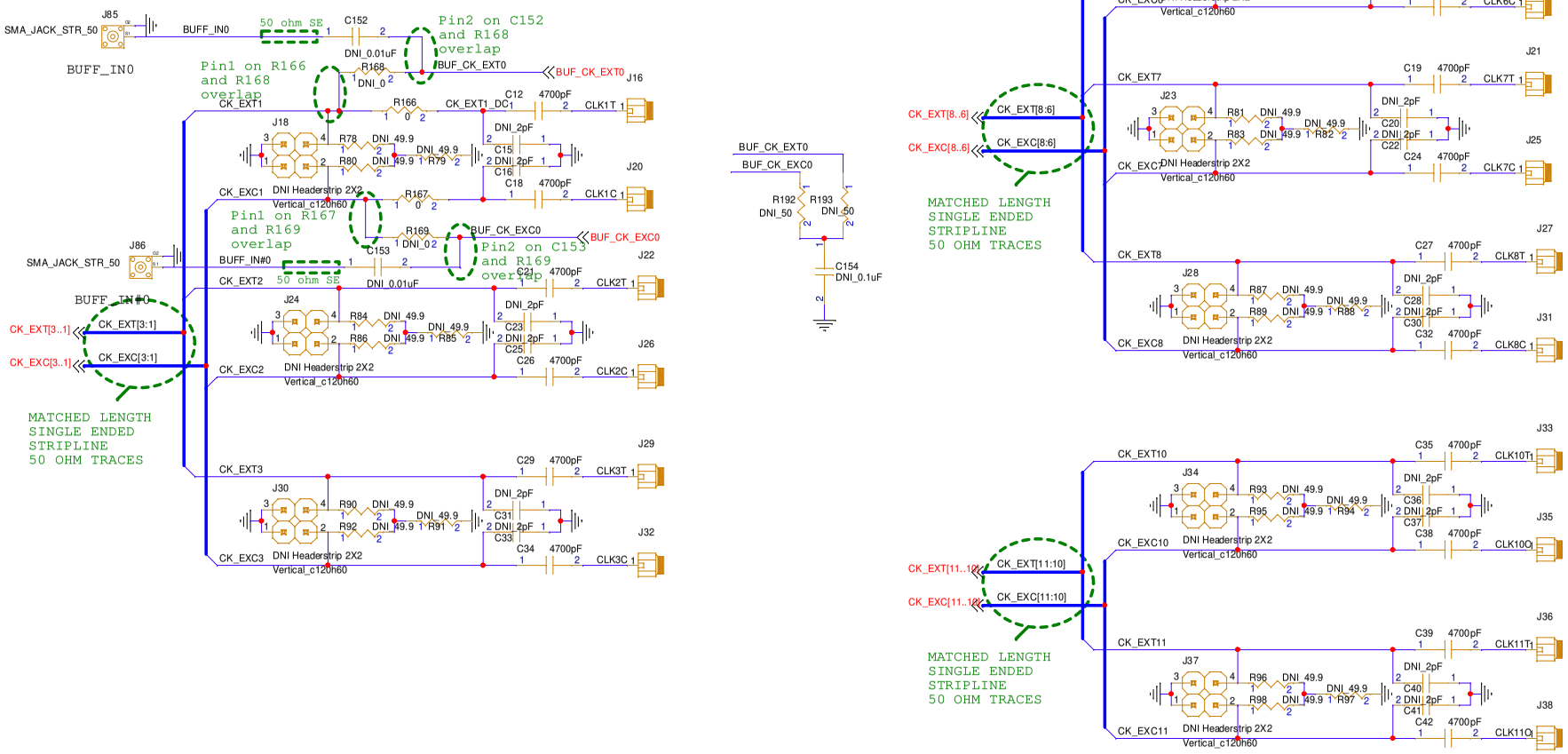
Part Number	Description
RC21212-EVB	AutoClock – 12-output Evaluation Board
RC21214-EVB	AutoClock – 8-output Evaluation Board

5. Revision History

Revision	Date	Description
1.00	Apr 25, 2024	Initial release.


FTDI Controls I2C/SPI
Aardvark Connector on pins 3, 4 and 6 for I2C control.
0.1uF near pins 39 , 12 , 24 , 46
Aardvark Connector
Need to match the connector size of Aardvark
BUS SOURCE
BUS TYPE
I2C
SPI
Control CS
GPIO PIN Selection for SPI (3-wire) SDIO
AT24C04C is a symbol of SOCKET for DIP8 package
Assemble R147 and R149 when not assembling U19.
Assemble R146 and R148 when not assembling U20.
Assemble R144 and R145 when not assembling U20.
RENESAS
Renesas
1140 West Warner Rd.
Tempe, AZ 85284
Title: HW10481_AutoClock_RC21213_RC21214_QFN40_REVA
Size B
HW Number: HW 10481
Engineer: Shudong Zheng
Rev. A
Date: 03/20/2024
Sheet: 1 of 1


GND_J1
GND_J2
GND_J3
GND_J4
GND_J
J41
Banana Black
J42
Banana Red
VDD_J
C55
10uF
J46
J47
J50
J51
Standoff 20mm
FID1
FID2
FID3
Fiducial
For OTP,
Stuff on 3.3V
/ 2.5V only
J39
J43
J45
J49
Headerstrip 2X4
VA
VX
VR
V5
FB2
FB3
FB5
FB7
R99
DNI_1
R101
R102
R103
R104
C43
C44
C45
C46
C51
C52
C53
C54
C60
C61
C62
C63
C68
C69
C70
C71
VDDA
VDDX
VDDR
VDDD
VBUS
FB9
FB10
VDD_USB
C76
C77
C78
R224
R225
EN1
PG1
U13
RAA214020
2A
DFN-10N
R234
27.0K
R233
C157
C79
C80
R108
220
D10
LED Green
FB12
U14
VIN2
EN2
PG2
R226
R227
C87
C88
R111
48K
C89
C86
C158
R228
FB14
U15
VIN3
EN3
PG3
R229
R230
C95
C96
R231
C97
C98
C155
R232
J40
J44
J48
J52
J53
J54
VO1
VO2
VO3
VO4
VO5
VO6
FB1
FB4
FB6
FB8
FB11
FB13
C47
C48
C49
C50
C56
C57
C58
C59
C66
C64
C65
C67
C72
C73
C74
C75
C82
C83
C84
C85
C90
C91
C92
C93
VDDO1
VDDO2
VDDO3
VDDO4
VDDO5
VDDO6
J75
J76
FB18
FB19
R183
V_B_DIG
V_B_GID_FB
B_VDDDIG
B_VDDCLKx
C144
C145
C146
C147
C148
C149
C150
C151
C155
C156
Male, 100mil Pitch
Vertical
0.1uF capacitors C150 C151, C155, and C156
near each VDDCLK pin on buffer U22.
RENESAS
Renesas
1140 West Warner Rd.
Tempe, AZ 85284
Title: HW10481_AutoClock_RC21213_RC21214_QFN40_REVA
Size C
HW Number: HW10481
Engineer: Shudong Zheng
Rev. A
Date: 03/20/2024
Sheet: 1 of 1

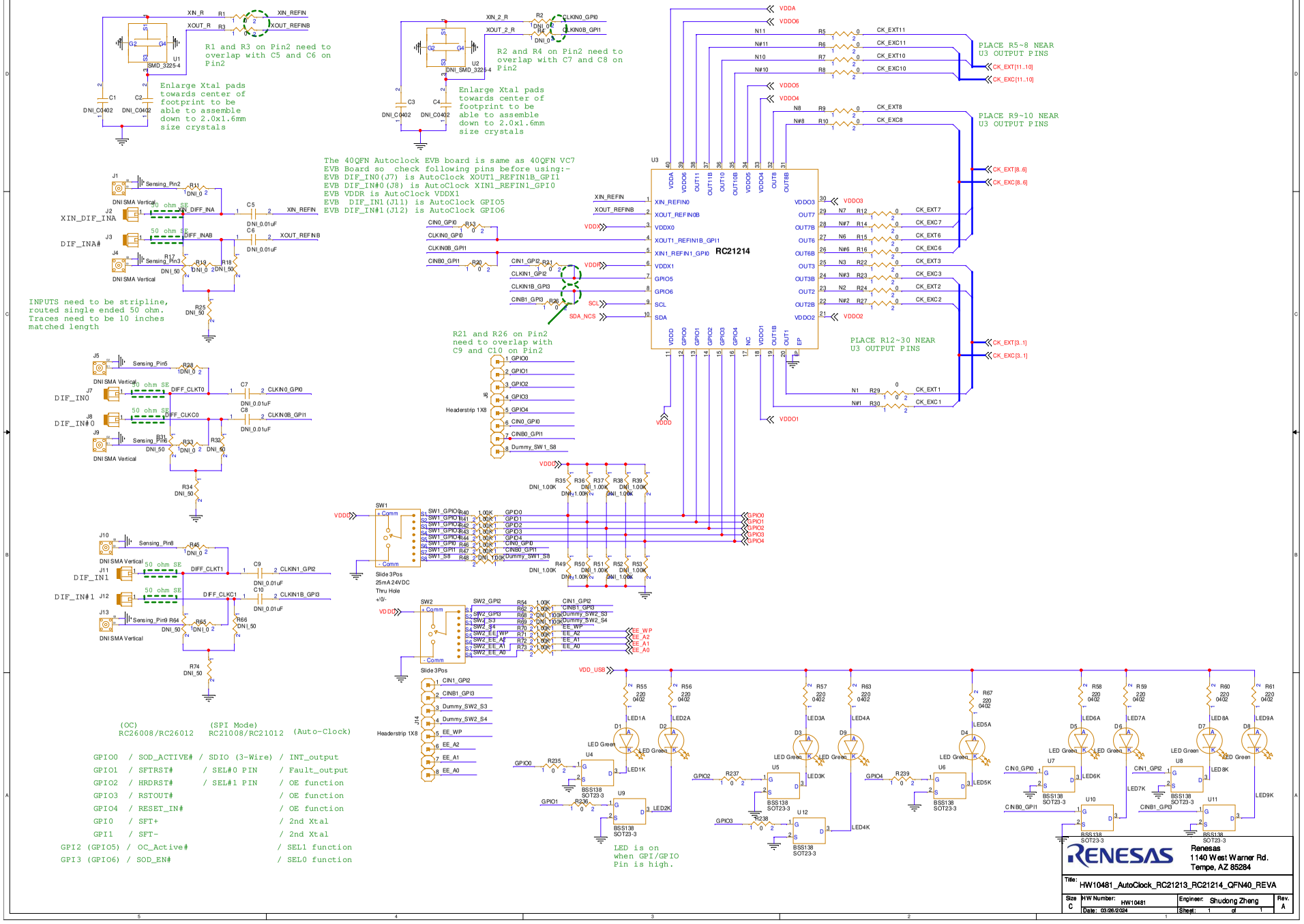


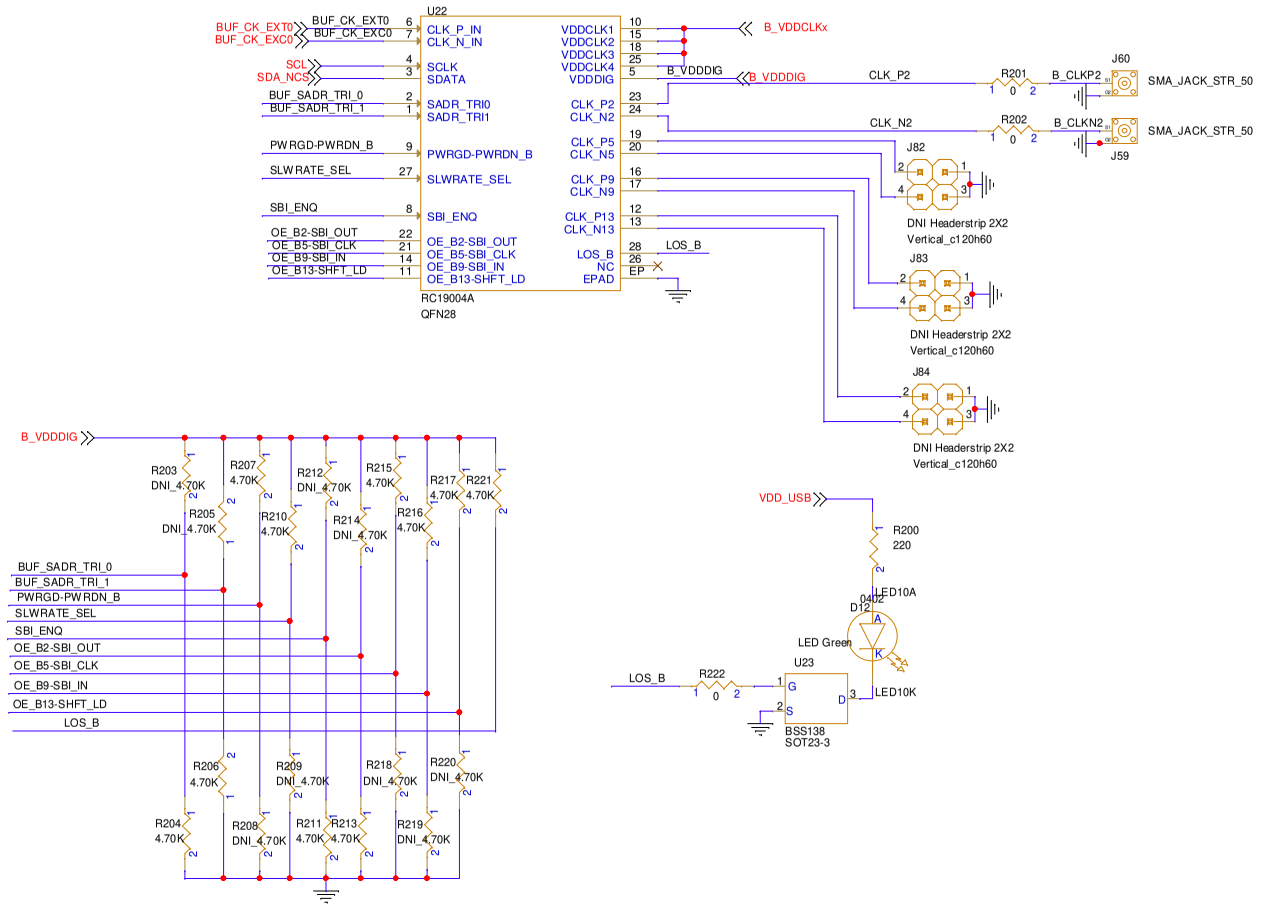
RENESAS

Renesas
1140 West Warner Rd.
Tempe, AZ 85284

Title: HW10481_AutoClock_RC21213_RC21214_QFN40_REVA

Size	HW Number:	Engineer:	Rev.
B	HW 10481	Shudong Zheng	A
	Date: 03/20/2024	Sheet: 1 of 1	


R1 and R3 on Pin2 need to overlap with C5 and C6 on Pin2
Enlarge Xtal pads towards center of footprint to be able to assemble down to 2.0x1.6mm size crystals
R2 and R4 on Pin2 need to overlap with C7 and C8 on Pin2
Enlarge Xtal pads towards center of footprint to be able to assemble down to 2.0x1.6mm size crystals
The 40QFN Autoclock EVB board is same as 40QFN VC7 EVB Board so check following pins before using:-
EVB DIF_IN0(J7) is AutoClock XOUT1_REFIN1B_GPI1
EVB DIF_IN#0(J8) is AutoClock XIN1_REFIN1_GPI0
EVB VDDR is AutoClock VDDX1
EVB DIF_IN1(J11) is AutoClock GPIO5
EVB DIF_IN#1(J12) is AutoClock GPIO6
INPUTS need to be stripline, routed single ended 50 ohm. Traces need to be 10 inches matched length
R21 and R26 on Pin2 need to overlap with C9 and C10 on Pin2
PLACE R5~8 NEAR U3 OUTPUT PINS
PLACE R9~10 NEAR U3 OUTPUT PINS
PLACE R12~30 NEAR U3 OUTPUT PINS
RC21214
(OC) RC26008/RC26012
(SPI Mode) RC21008/RC21012
(Auto-Clock)
GPIO0 / SOD_ACTIVE# / SDIO (3-Wire) / INT_output
GPIO1 / SFTRST# / SEL#0 PIN / Fault_output
GPIO2 / HRDRST# / SEL#1 PIN / OE function
GPIO3 / RSTOUT# / OE function
GPIO4 / RESET_IN# / OE function
GPI0 / SFT+ / 2nd Xtal
GPI1 / SFT- / 2nd Xtal
GPI2 (GPIO5) / OC_Active# / SEL1 function
GPI3 (GPIO6) / SOD_EN# / SEL0 function
LED is on when GPI/GPIO Pin is high.
Renesas
1140 West Warner Rd.
Tempe, AZ 85284
Title: HW10481_AutoClock_RC21213_RC21214_QFN40_REVA
Size C
HW Number: HW10481
Engineer: Shudong Zheng
Date: 03/26/2024
Sheet: 1 of 1
Rev. A

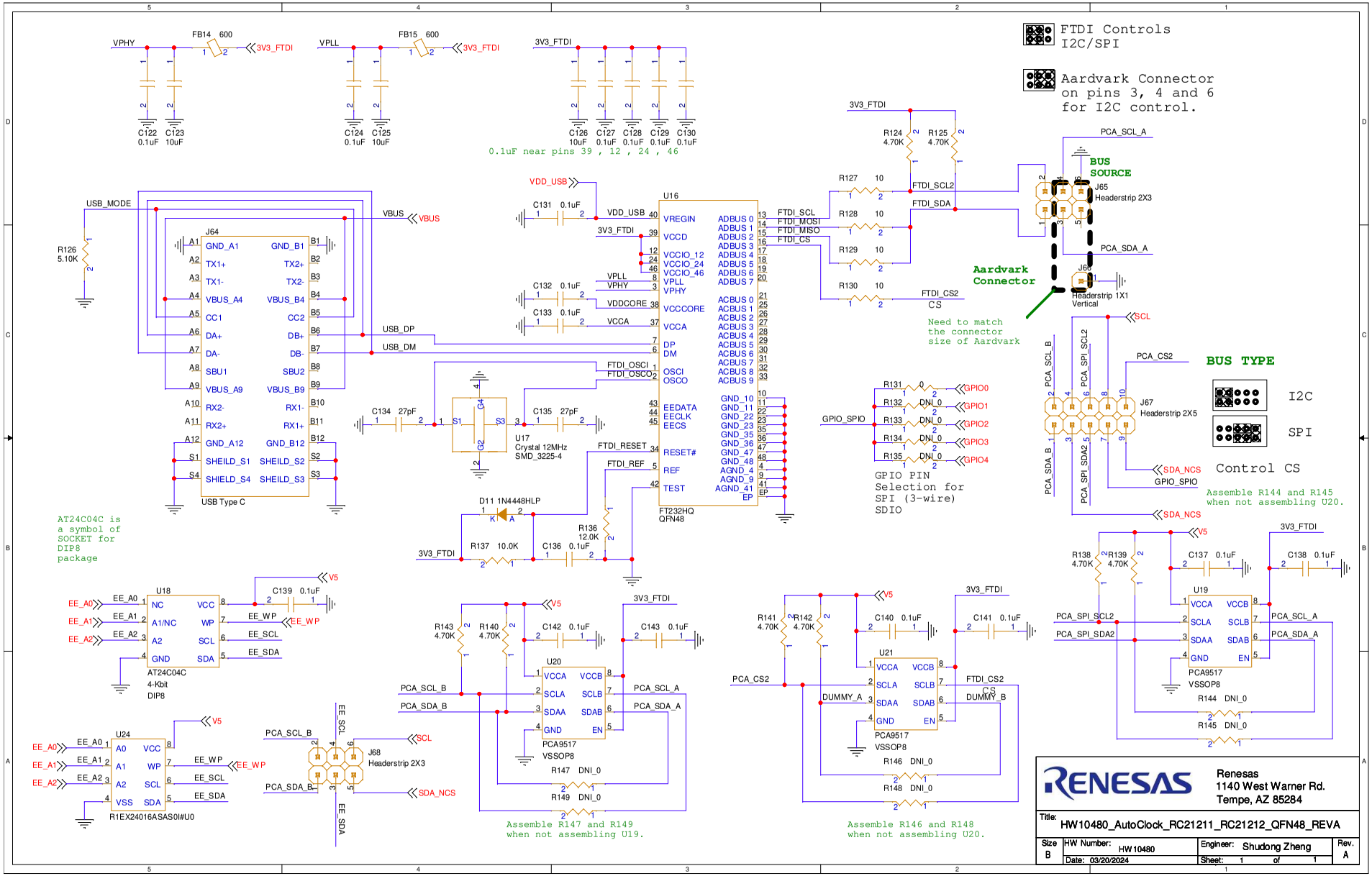


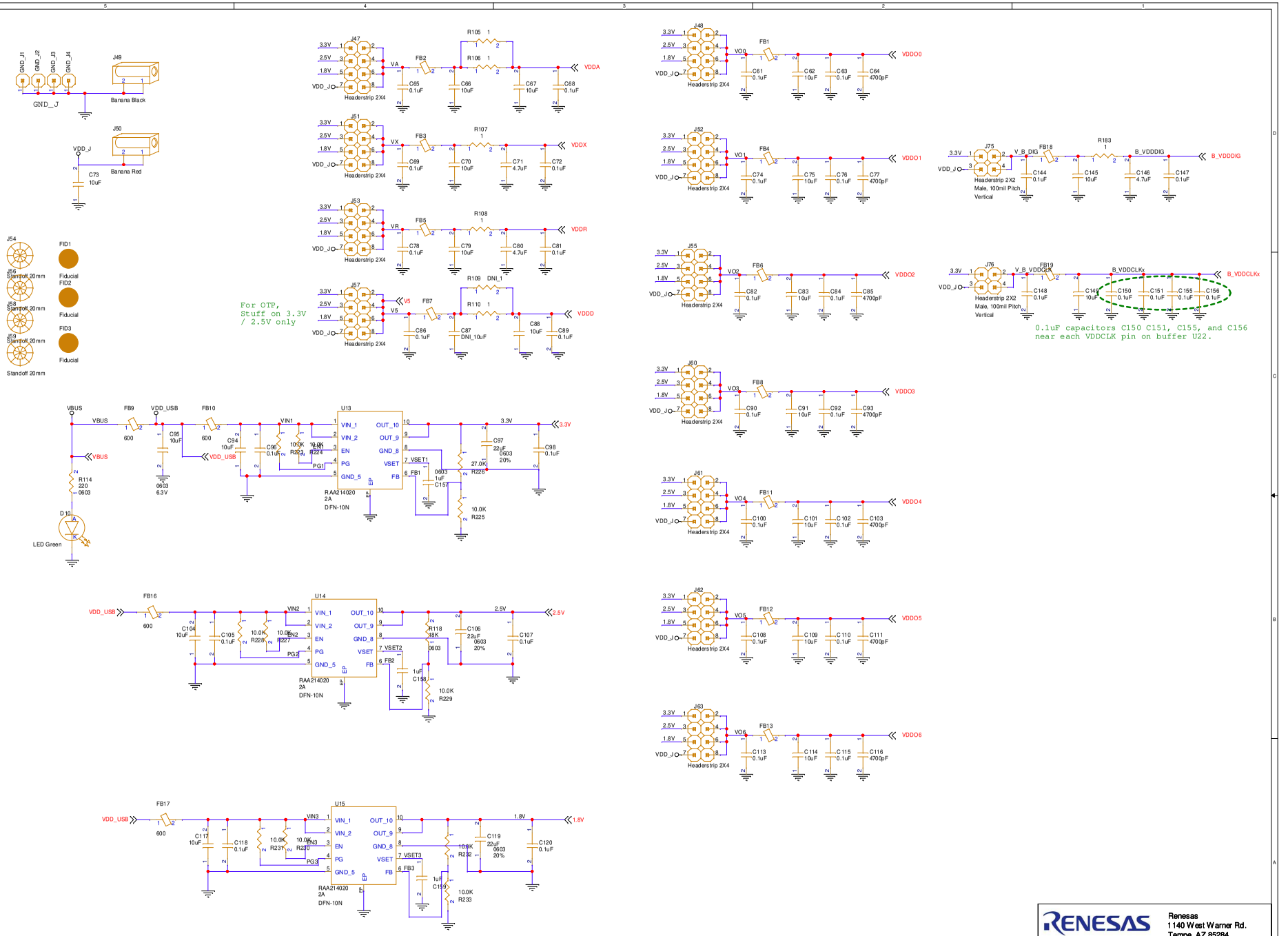
RENESAS

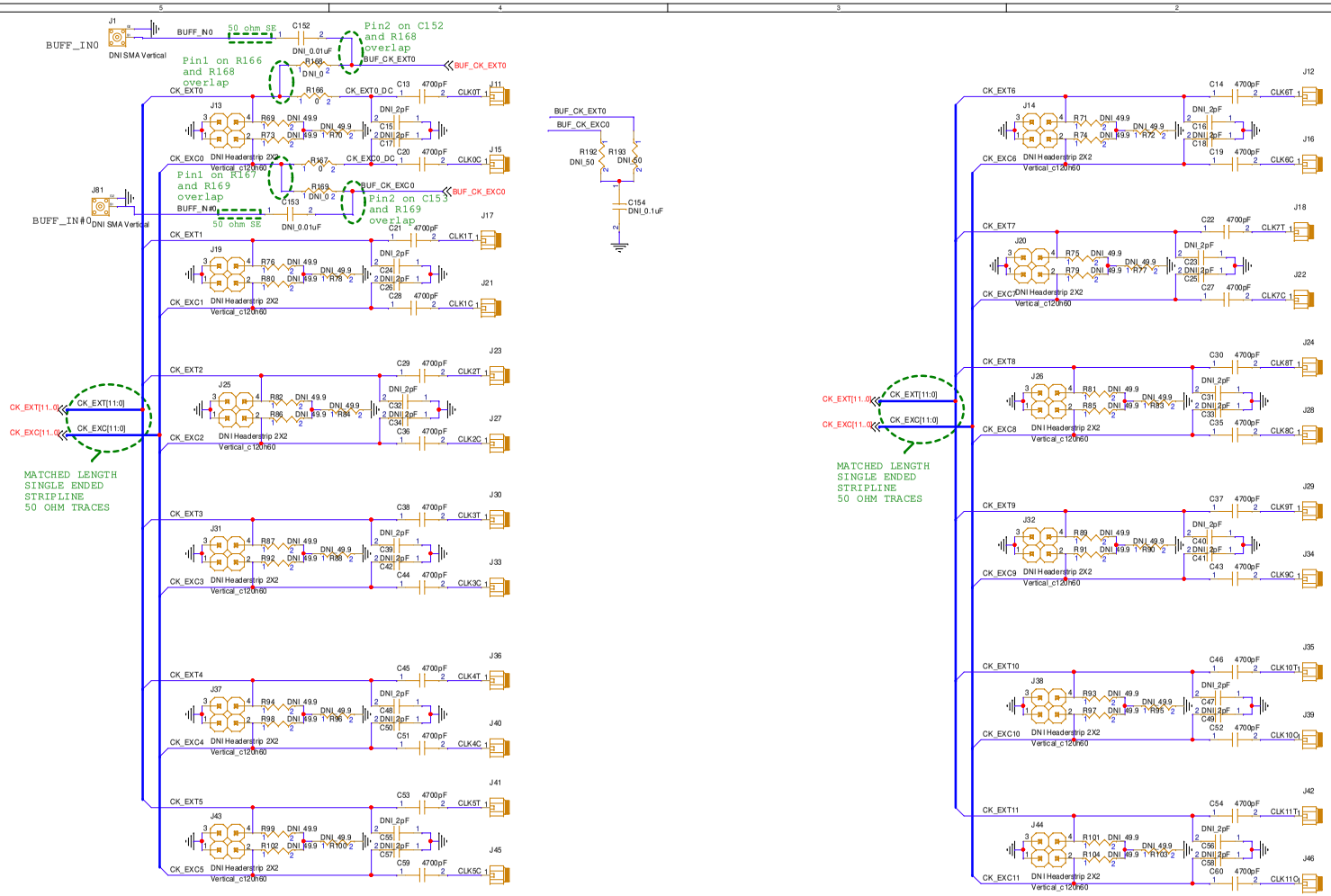
Renesas
1140 West Warner Rd.
Tempe, AZ 85284

Title: HW10481_AutoClock_RC21213_RC21214_QFN40_REVA

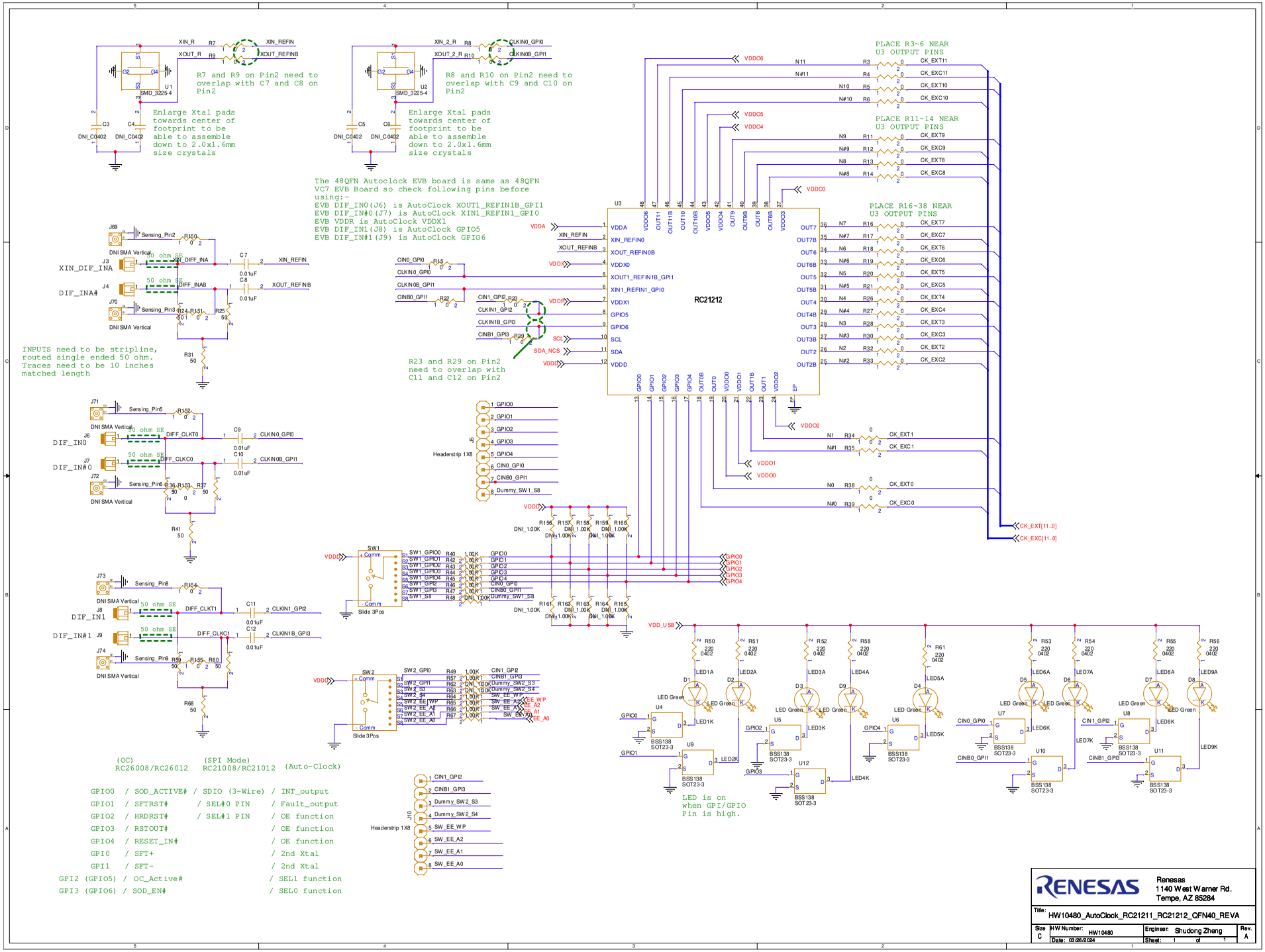
Size	HW Number:	Engineer:	Rev.
B	HW 10481	Shudong Zheng	A
	Date: 03/20/2024	Sheet: 1 of 1	

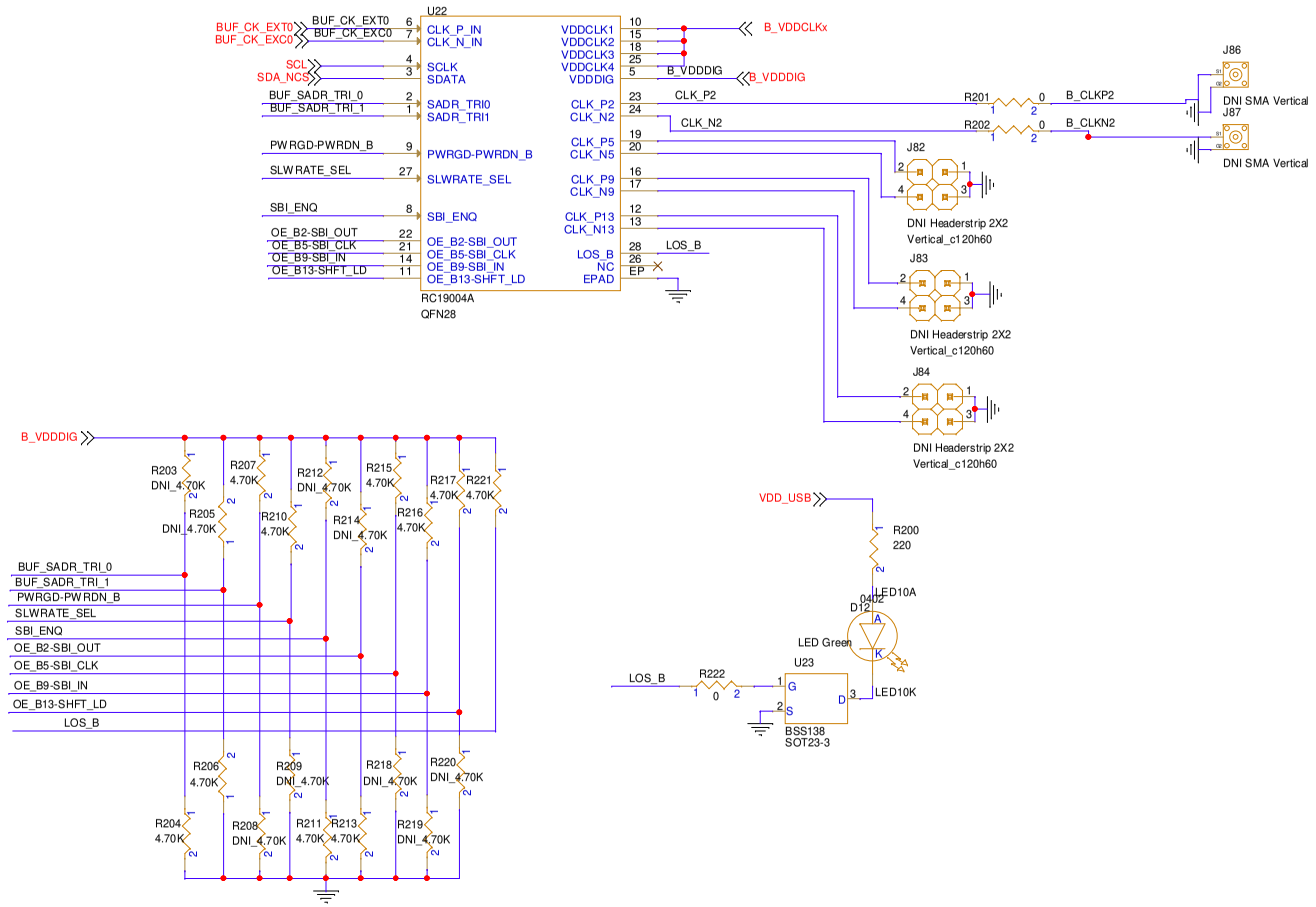

FTDI Controls I2C/SPI
Aardvark Connector on pins 3, 4 and 6 for I2C control.
0.1uF near pins 39 , 12 , 24 , 46
BUS SOURCE
Aardvark Connector
Need to match the connector size of Aardvark
BUS TYPE
I2C
SPI
Control CS
AT24C04C is a symbol of SOCKET for DIP8 package
GPIO PIN Selection for SPI (3-wire) SDIO
Assemble R144 and R145 when not assembling U20.
Assemble R147 and R149 when not assembling U19.
Assemble R146 and R148 when not assembling U20.
USB Type C
Crystal 12MHz SMD_3225-4
FT232HQ QFN48
AT24C04C 4-Kbit DIP8
R1EX24016ASAS0I#U0
PCA9517 VSSOP8
Renesas
1140 West Warner Rd.
Tempe, AZ 85284
Title: HW10480_AutoClock_RC21211_RC21212_QFN48_REVA
Size B
HW Number: HW 10480
Engineer: Shudong Zheng
Rev. A
Date: 03/20/2024
Sheet: 1 of 1


GND_J1
GND_J2
GND_J3
GND_J4
GND_J
J49
Banana Black
VDD_J
J50
Banana Red
C73
10uF
J54
Standoff 20mm
J56
Standoff 20mm
J58
Standoff 20mm
J59
Standoff 20mm
FID1
Fiducial
FID2
Fiducial
FID3
Fiducial
J47
Headerstrip 2X4
VA
FB2
R105
R106
C65
0.1uF
C66
10uF
C67
10uF
C68
0.1uF
VDDA
J51
VX
FB3
R107
C69
0.1uF
C70
10uF
C71
4.7uF
C72
0.1uF
VDDX
J53
VR
FB5
R108
C78
0.1uF
C79
10uF
C80
4.7uF
C81
0.1uF
VDDR
J57
V5
FB7
R109
DNI_1
R110
C86
0.1uF
C87
DNI_10uF
C88
10uF
C89
0.1uF
VDDD
For OTP,
Stuff on 3.3V
/ 2.5V only
J48
VO0
FB1
C61
0.1uF
C62
10uF
C63
0.1uF
C64
4700pF
VDDO0
J52
VO1
FB4
C74
0.1uF
C75
10uF
C76
0.1uF
C77
4700pF
VDDO1
J55
VO2
FB6
C82
0.1uF
C83
10uF
C84
0.1uF
C85
4700pF
VDDO2
J60
VO3
FB8
C90
0.1uF
C91
10uF
C92
0.1uF
C93
4700pF
VDDO3
J61
VO4
FB11
C100
0.1uF
C101
10uF
C102
0.1uF
C103
4700pF
VDDO4
J62
VO5
FB12
C108
0.1uF
C109
10uF
C110
0.1uF
C111
4700pF
VDDO5
J63
VO6
FB13
C113
0.1uF
C114
10uF
C115
0.1uF
C116
4700pF
VDDO6
J75
Headerstrip 2X2
Male, 100mil Pitch
Vertical
V_B_DIG
FB18
R183
C144
0.1uF
C145
10uF
C146
4.7uF
C147
0.1uF
B_VDDDIG
J76
V_B_VDDCLKx
FB19
C148
0.1uF
C149
10uF
C150
0.1uF
C151
0.1uF
C155
0.1uF
C156
0.1uF
B_VDDCLKx
0.1uF capacitors C150 C151, C155, and C156
near each VDDCLK pin on buffer U22.
VBUS
FB9
VDD_USB
FB10
C95
10uF
C94
10uF
VIN1
U13
RAA214020
2A
DFN-10N
VIN_1
VIN_2
EN
PG
GND_5
OUT_10
OUT_9
GND_8
VSET
FB
EP
R114
220
0603
D10
LED Green
C96
0.1uF
R224
100K
R223
10.0K
PG1
R226
27.0K
C97
22uF
0603
20%
C98
0.1uF
C157
1uF
R225
10.0K
3.3V
FB16
C104
10uF
C105
0.1uF
R228
10.0K
R227
10.0K
PG2
U14
VIN2
R118
48K
0603
C106
22uF
0603
20%
C107
0.1uF
C158
1uF
R229
10.0K
2.5V
FB17
C117
10uF
C118
0.1uF
R231
10.0K
R230
10.0K
PG3
U15
VIN3
C119
22uF
0603
20%
C120
0.1uF
R232
10.0K
C159
1uF
R233
10.0K
1.8V
RENESAS
Renesas
1140 West Warner Rd.
Tempe, AZ 85284
Title: HW10480_AutoClock_RC21211_RC21212_QFN48_REVA
Size C
HW Number: HW10480
Engineer: Shudong Zheng
Rev. A
Date: 03/20/2024
Sheet: 1 of 1



Renesas 1140 West Warner Rd. Tempe, AZ 85284			
Title: HW10480_AutoClock_RC21211_RC21212_QFN48_REVA			
Size: C	HW Number: HW10480	Engineer: Shudong Zheng	Rev: A
	Date: 03/20/2024	Sheet: 1 of 1	


R7 and R9 on Pin2 need to overlap with C7 and C8 on Pin2
Enlarge Xtal pads towards center of footprint to be able to assemble down to 2.0x1.6mm size crystals
R8 and R10 on Pin2 need to overlap with C9 and C10 on Pin2
Enlarge Xtal pads towards center of footprint to be able to assemble down to 2.0x1.6mm size crystals
The 48QFN Autoclock EVB board is same as 48QFN VC7 EVB Board so check following pins before using:-
EVB DIF_IN0(J6) is AutoClock XOUT1_REFIN1B_GPI1
EVB DIF_IN#0(J7) is AutoClock XIN1_REFIN1_GPI0
EVB VDDR is AutoClock VDDX1
EVB DIF_IN1(J8) is AutoClock GPIO5
EVB DIF_IN#1(J9) is AutoClock GPIO6
PLACE R3~6 NEAR U3 OUTPUT PINS
PLACE R11~14 NEAR U3 OUTPUT PINS
PLACE R16~38 NEAR U3 OUTPUT PINS
RC21212
INPUTS need to be stripline, routed single ended 50 ohm. Traces need to be 10 inches matched length
R23 and R29 on Pin2 need to overlap with C11 and C12 on Pin2
LED is on when GPI/GPIO Pin is high.
(OC) RC26008/RC26012
(SPI Mode) RC21008/RC21012
(Auto-Clock)
GPIO0 / SOD_ACTIVE# / SDIO (3-Wire) / INT_output
GPIO1 / SFTRST# / SEL#0 PIN / Fault_output
GPIO2 / HRDRST# / SEL#1 PIN / OE function
GPIO3 / RSTOUT# / OE function
GPIO4 / RESET_IN# / OE function
GPI0 / SFT+ / 2nd Xtal
GPI1 / SFT- / 2nd Xtal
GPI2 (GPIO5) / OC_Active# / SEL1 function
GPI3 (GPIO6) / SOD_EN# / SEL0 function
Renesas
1140 West Warner Rd.
Tempe, AZ 85284
Title: HW10480_AutoClock_RC21211_RC21212_QFN40_REVA
Size C
HW Number: HW10480
Engineer: Shudong Zheng
Date: 03/26/2024
Sheet: 1 of 1
Rev. A



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Renesas
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Tempe, AZ 85284

Title: HW10480_AutoClock_RC21211_RC21212_QFN48_REVA

Size	HW Number:	Engineer:	Rev.
B	HW 10480	Shudong Zheng	A
	Date: 03/20/2024	Sheet: 1 of 1	

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