RMLV0808BGSB - 4S2

8Mb Advanced LPSRAM (1024k word × 8bit)

R10DS0232EJ0201
Rev.2.01
2020.02.20

Description

The RMLV0808BGSB is a family of 8-Mbit static RAMs organized 1,048,576-word × 8-bit, fabricated by Renesas's high-performance Advanced LPSRAM technologies. The RMLV0808BGSB has realized higher density, higher performance and low power consumption. The RMLV0808BGSB offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 44pin TSOP (II).

Features

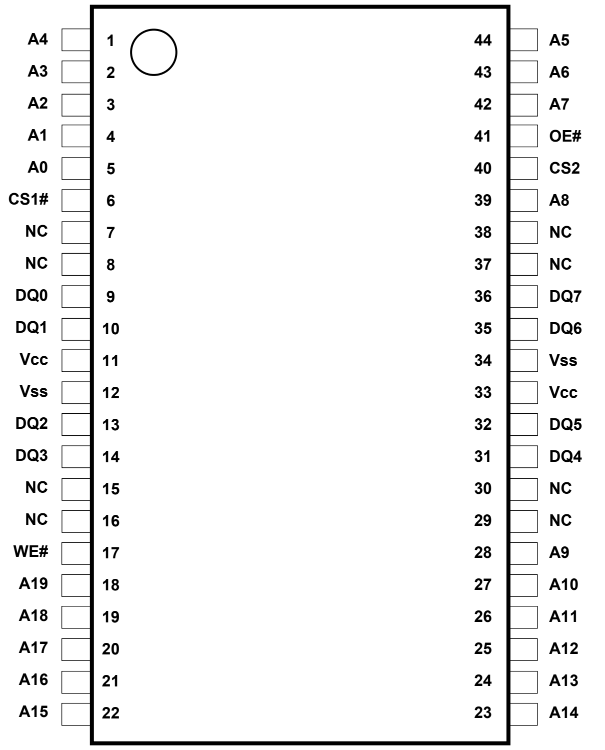
- Single 3V supply: 2.4V to 3.6V
- Access time:
  - Power supply voltage from 2.7V to 3.6V: 45ns (max.)
  - Power supply voltage from 2.4V to 2.7V: 55ns (max.)
- Current consumption:
  - Standby: 0.45µA (typ.)
- Equal access and cycle times
- Common data input and output
  - Three state output
- Directly TTL compatible
  - All inputs and outputs
- Battery backup operation

Part Name Information

Part Name	Power supply	Access time	Temperature Range	Package
RMLV0808BGSB-4S2	2.7V to 3.6V	45 ns	-40 ~ +85°C	11.76mm×18.41mm 44pin plastic TSOP(II)
	2.4V to 2.7V	55 ns		

Pin Arrangement

44pin TSOP(II)

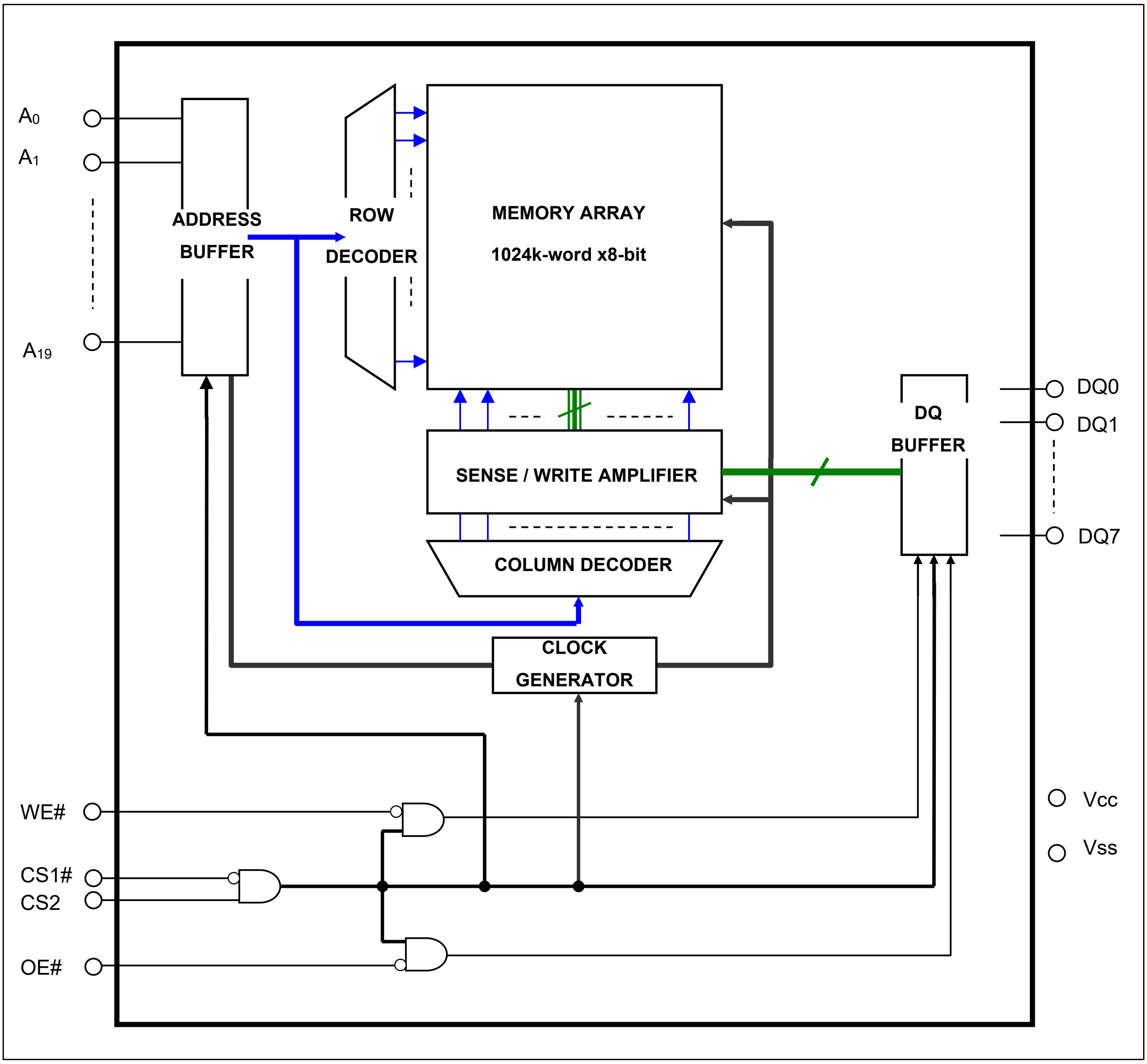


(Top view)

Pin Description

Pin name	Function
V_{CC}	Power supply
V_{SS}	Ground
A0 to A19	Address input
DQ0 to DQ7	Data input/output
CS1#	Chip select 1
CS2	Chip select 2
OE#	Output enable
WE#	Write enable
NC	No connection

Block Diagram



Operation Table

CS1#	CS2	WE#	OE#	DQ0~7	Operation
H	X	X	X	High-Z	Stand-by
X	L	X	X	High-Z	Stand-by
L	H	L	X	Din	Write
L	H	H	L	Dout	Read
L	H	H	H	High-Z	Output disable

Note 1. H: V_{IH} L:V_{IL} X: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5[*2] to V_{CC}+0.3[*3]	V
Power dissipation	P_T	0.7	W
Operation temperature	Topr	-40 to +85	°C
Storage temperature range	Tstg	-65 to +150	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Note 2. -3.0V for pulse ≤ 30ns (full width at half maximum)
3. Maximum voltage is +4.6V.

DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Supply voltage	V_{CC}	2.4	3.0	3.6	V		
	V_{SS}	0	0	0	V		
Input high voltage	V_{IH}	2.0	—	V_{CC}+0.2	V	Vcc=2.4V to 2.7V	
		2.2	—	V_{CC}+0.2	V	Vcc=2.7V to 3.6V	
Input low voltage	V_{IL}	-0.2	—	0.4	V	Vcc=2.4V to 2.7V	4
		-0.2	—	0.6	V	Vcc=2.7V to 3.6V	4
Ambient temperature range	Ta	-40	—	+85	°C		

Note 4. -3.0V for pulse ≤ 30ns (full width at half maximum)

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	
Input leakage current	$\|I_{LI}\|$	—	—	1	µA	Vin = V_{SS} to V_{CC}	
Output leakage current	$\|I_{LO}\|$	—	—	1	µA	CS1# = V_{IH} or CS2 = V_{IL} or OE# = V_{IH} or WE# = V_{IL} , $V_{I/O}$ = V_{SS} to V_{CC}	
Average operating current	I_{CC1}	—	20[*5]	25	mA	Cycle = 55ns, duty =100%, $I_{I/O}$ = 0mA, CS1# = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}	
		—	25[*5]	30	mA	Cycle = 45ns, duty =100%, $I_{I/O}$ = 0mA, CS1# = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}	
	I_{CC2}	—	1.5[*5]	3	mA	Cycle = 1µs, duty =100%, $I_{I/O}$ = 0mA, CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V, V_{IH} ≥ V_{CC}-0.2V, V_{IL} ≤ 0.2V	
Standby current	I_{SB}	—	—	0.3	mA	CS2 = V_{IL}, Others = V_{SS} to V_{CC}	
Standby current	I_{SB1}	—	0.45[*5]	2	µA	~+25°C	Vin = V_{SS} to V_{CC}, (1) CS2 ≤ 0.2V or (2) CS1# ≥ V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V
		—	0.6[*6]	4	µA	~+40°C	
		—	—	7	µA	~+70°C	
		—	—	10	µA	~+85°C	
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = -1mA Vcc≥2.7V	
	V_{OH2}	2.0	—	—	V	I_{OH} = -0.1mA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2mA Vcc≥2.7V	
	V_{OL2}	—	—	0.4	V	I_{OL} = 0.1mA	

Note 5. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=25ºC), and not 100% tested.
Note 6. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=40ºC), and not 100% tested.

Capacitance

(Ta =25°C, f =1MHz)

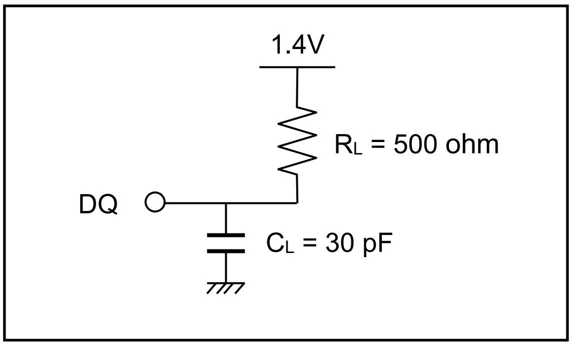
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C in	—	—	8	pF	Vin =0V	7
Input / output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O}$ =0V	7

Note 7. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (Vcc = 2.4V ~ 3.6V, Ta = -40 ~ +85°C)

- Input pulse levels:
  V_{IL} = 0.4V, V_{IH} = 2.4V (Vcc=2.7V to 3.6V)
  V_{IL} = 0.4V, V_{IH} = 2.2V (Vcc=2.4V to 2.7V)
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	Vcc=2.7V to 3.6V		Vcc=2.4V to 2.7V		Unit	Note
		Min.	Max.	Min.	Max.		
Read cycle time	t_{RC}	45	—	55	—	ns	
Address access time	t_{AA}	—	45	—	55	ns	
Chip select access time	t_{ACS1}	—	45	—	55	ns	
	t_{ACS2}	—	45	—	55	ns	
Output enable to output valid	t_{OE}	—	22	—	30	ns	
Output hold from address change	t_{OH}	10	—	10	—	ns	
Chip select to output in low-Z	t_{CLZ1}	10	—	10	—	ns	8,9
	t_{CLZ2}	10	—	10	—	ns	8,9
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	8,9
Chip deselect to output in high-Z	t_{CHZ1}	0	18	0	20	ns	8,9,10
	t_{CHZ2}	0	18	0	20	ns	8,9,10
Output disable to output in high-Z	t_{OHZ}	0	18	0	20	ns	8,9,10

Note 8. This parameter is sampled and not 100% tested.
9. At any given temperature and voltage condition, t_{CHZ1} max is less than t_{CLZ1} min, t_{CHZ2} max is less than t_{CLZ2} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.
10. t_{CHZ1}, t_{CHZ2} and t_{OHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

Write Cycle

Parameter	Symbol	Vcc=2.7V to 3.6V		Vcc=2.4V to 2.7V		Unit	Note
		Min.	Max.	Min.	Max.		
Write cycle time	t_{WC}	45	—	55	—	ns	
Address valid to write end	t_{AW}	35	—	50	—	ns	
Chip select to write end	t_{CW}	35	—	50	—	ns	
Write pulse width	t_{WP}	35	—	40	—	ns	11
Address setup time to write start	t_{AS}	0	—	0	—	ns	
Write recovery time from write end	t_{WR}	0	—	0	—	ns	
Data to write time overlap	t_{DW}	25	—	25	—	ns	
Data hold from write end	t_{DH}	0	—	0	—	ns	
Output enable from write end	t_{OW}	5	—	5	—	ns	12
Output disable to output in high-Z	t_{OHZ}	0	18	0	20	ns	12,13
Write to output in high-Z	t_{WHZ}	0	18	0	20	ns	12,13

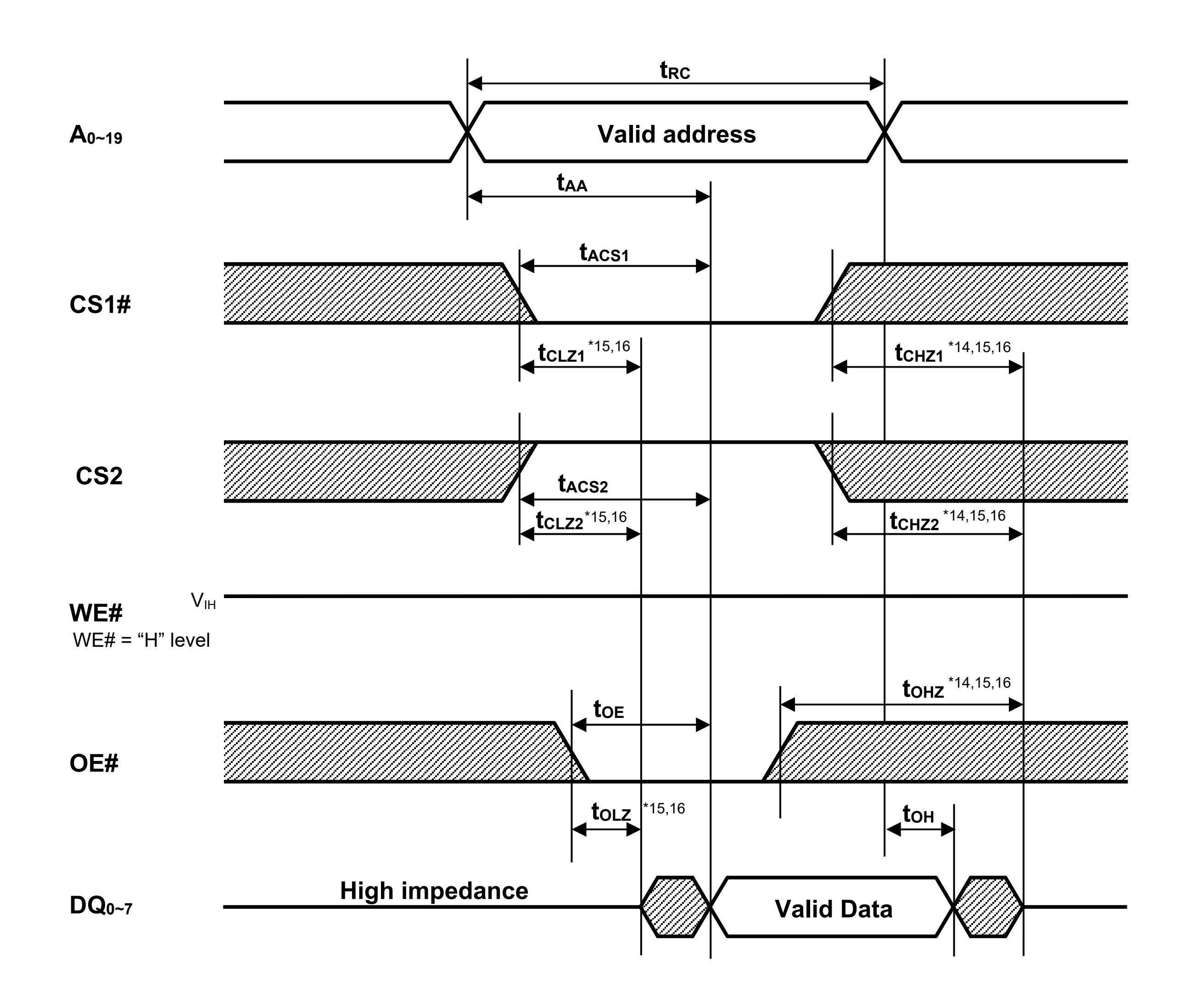
Note 11. t_{WP} is the interval between write start and write end.
A write starts when all of (CS1#), (WE#) and (CS2) become active.
A write is performed during the overlap of a low CS1#, a low WE# and a high CS2.
A write ends when any of (CS1#), (WE#) or (CS2) becomes inactive.

12. This parameter is sampled and not 100% tested.

13. t_{OHZ} and t_{WHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

Timing Waveforms

Read Cycle

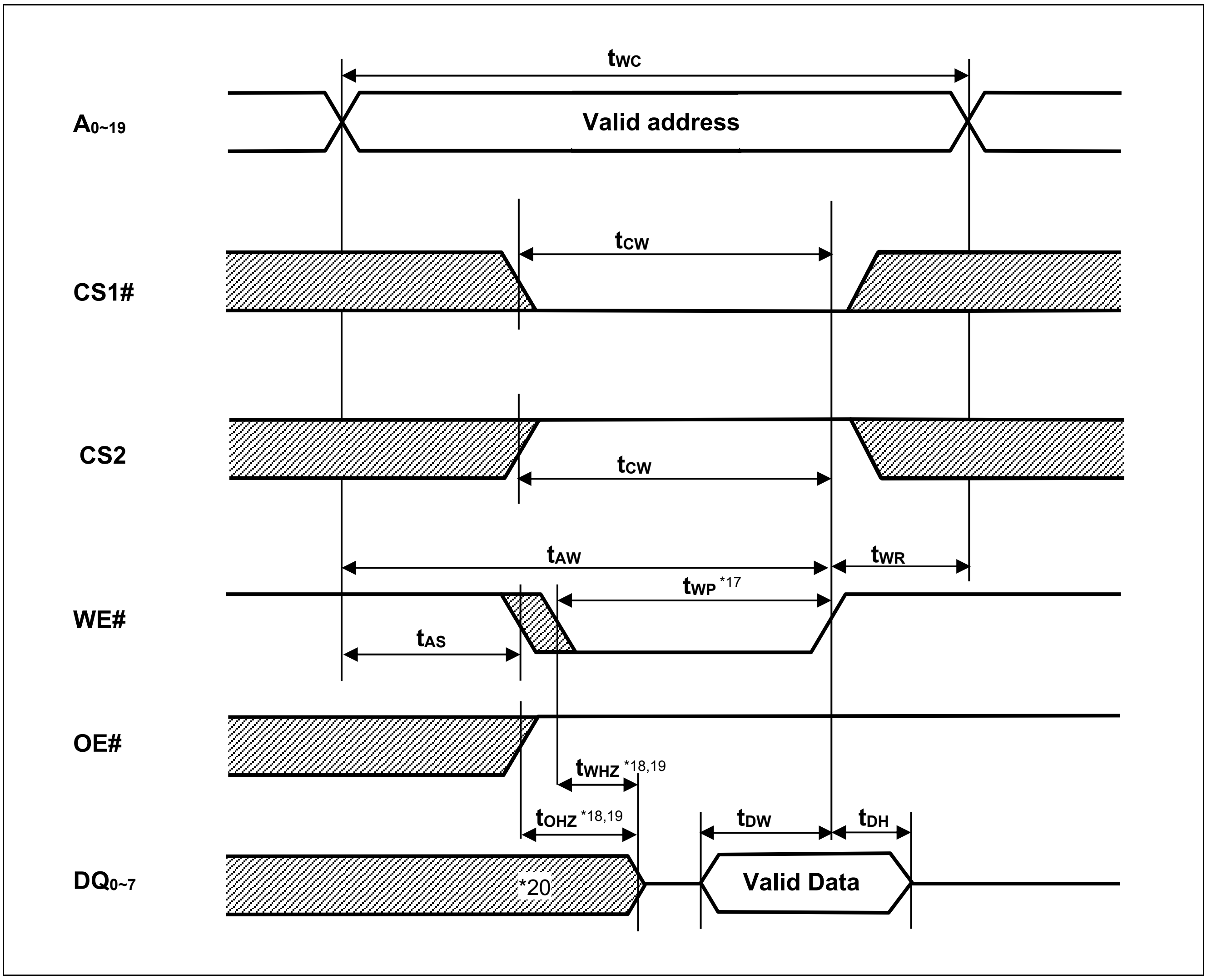


Note 14. t_{CHZ1}, t_{CHZ2} and t_{OHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

15. This parameter is sampled and not 100% tested

16. At any given temperature and voltage condition, t_{CHZ1} max is less than t_{CLZ1} min, t_{CHZ2} max is less than t_{CLZ2} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.

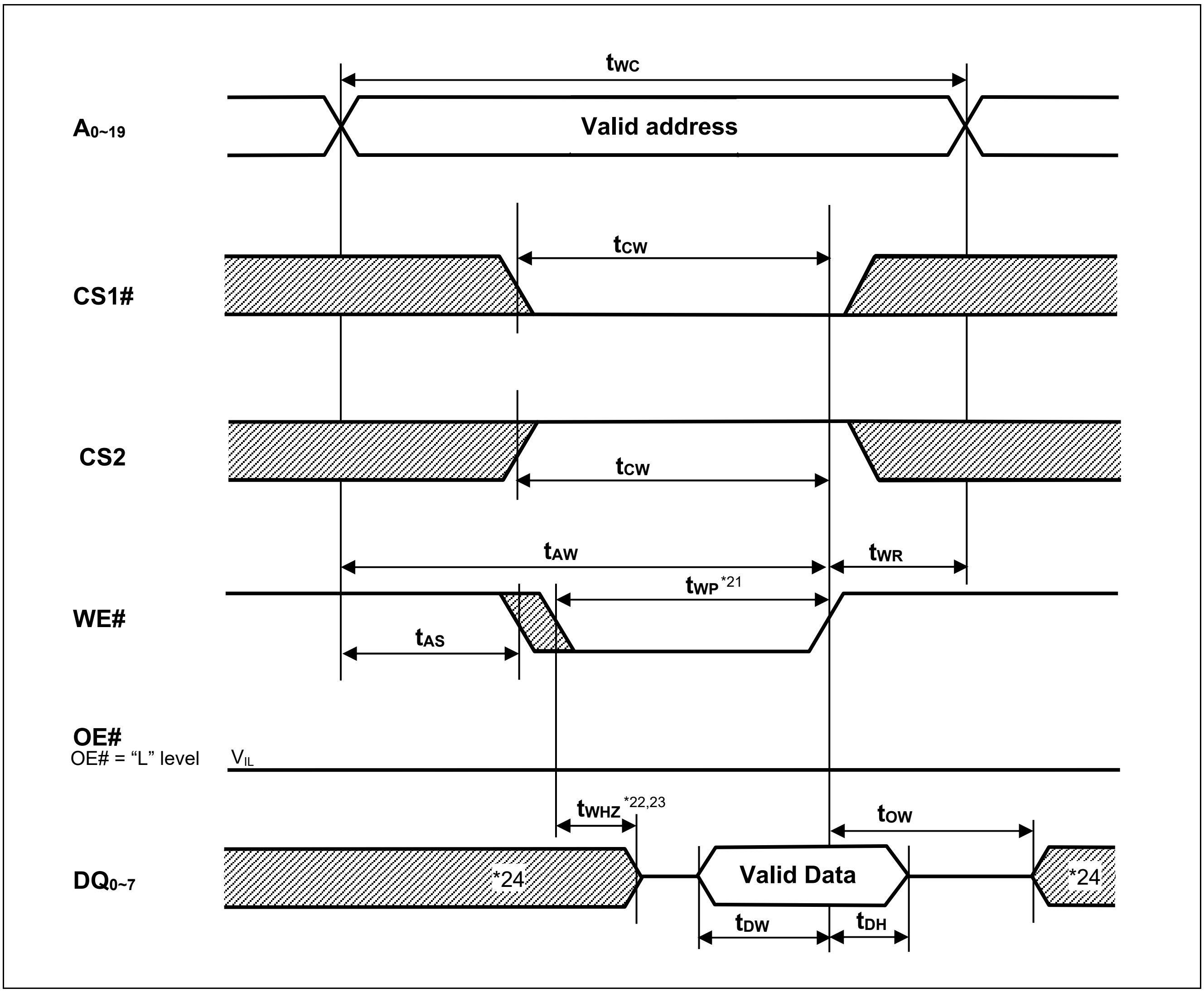
Write Cycle (1) (WE# CLOCK, OE#="H" while writing)



Note 17. t_{WP} is the interval between write start and write end.
A write starts when all of (CS1#), (WE#) and (CS2) become active.
A write is performed during the overlap of a low CS1#, a low WE# and a high CS2.
A write ends when any of (CS1#), (WE#) or (CS2) becomes inactive.

18. t_{OHZ} and t_{WHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.
19. This parameter is sampled and not 100% tested
20. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

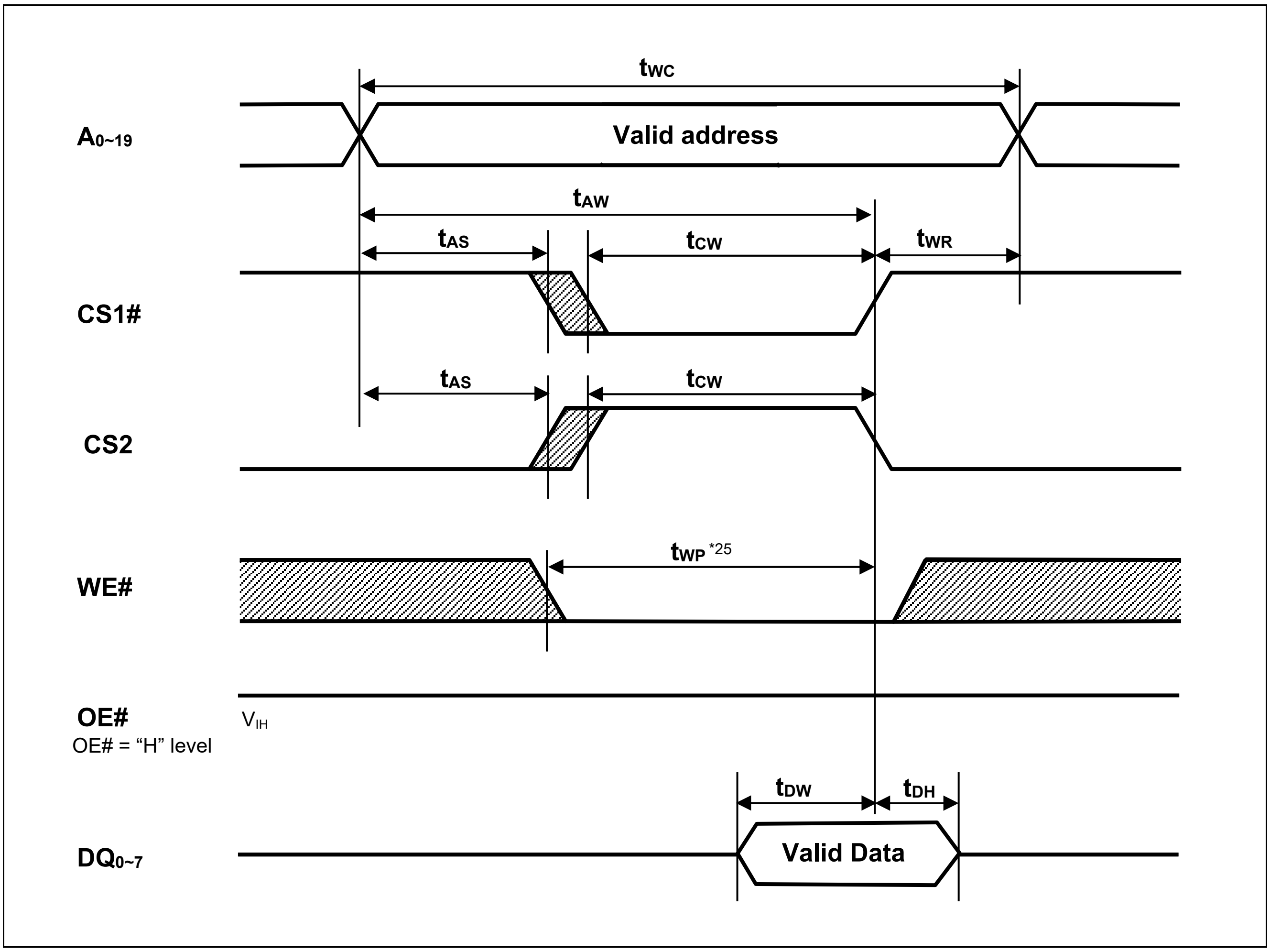
Write Cycle (2) (WE# CLOCK, OE# Low Fixed)



Note 21. t_{WP} is the interval between write start and write end.
A write starts when all of (CS1#), (WE#) and (CS2) become active.
A write is performed during the overlap of a low CS1#, a low WE# and a high CS2.
A write ends when any of (CS1#), (WE#) or (CS2) becomes inactive.

22. t_{WHZ} is defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.
23. This parameter is sampled and not 100% tested.
24. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

Write Cycle (3) (CS1#, CS2 CLOCK)



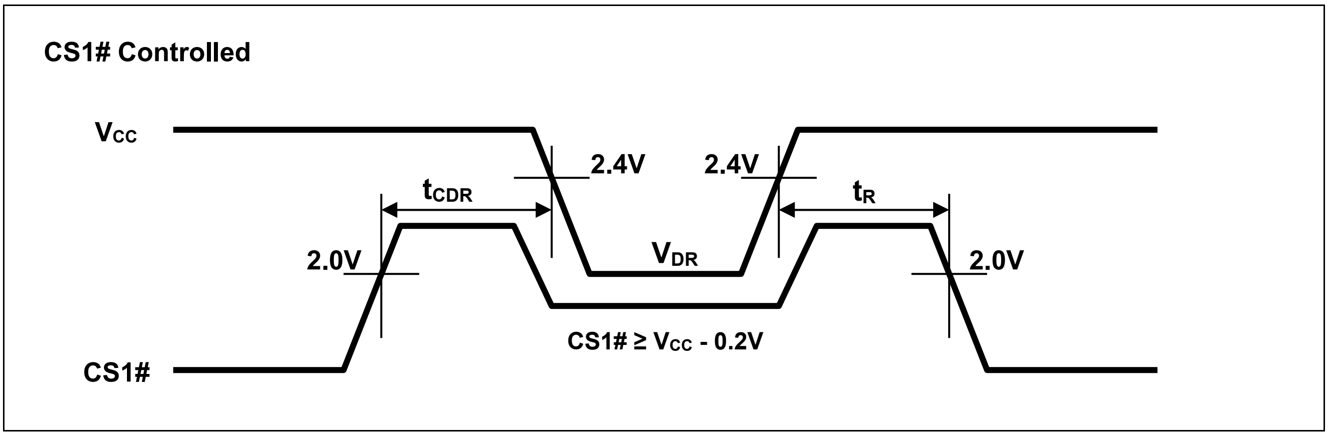
Note 25. t_{WP} is the interval between write start and write end.
A write starts when all of (CS1#), (WE#) and (CS2) become active.
A write is performed during the overlap of a low CS1#, a low WE# and a high CS2.
A write ends when any of (CS1#), (WE#) or (CS2) becomes inactive.

Low V_{CC} Data Retention Characteristics

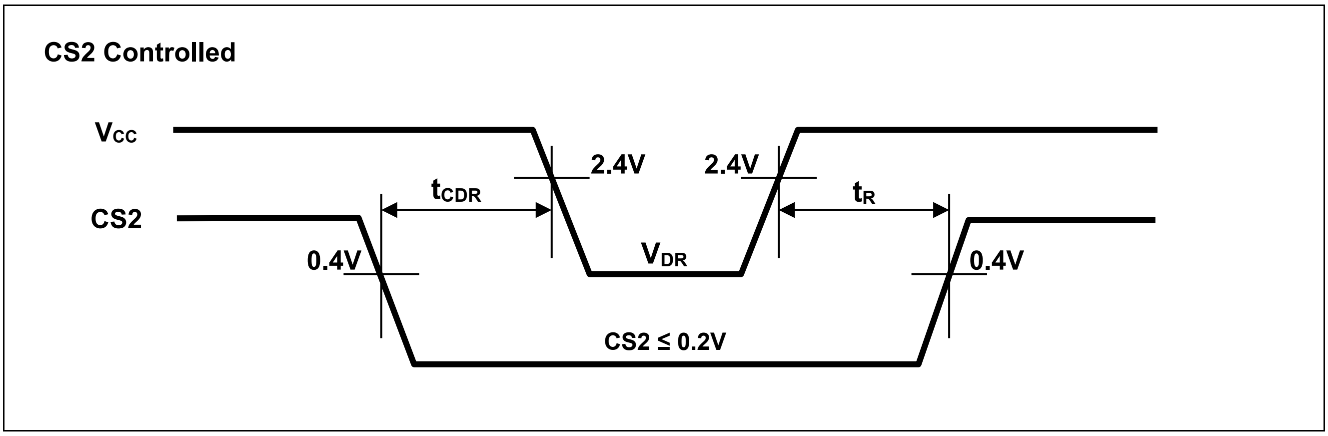
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions[28]	
V_{CC} for data retention	V_{DR}	1.5	—	3.6	V	Vin ≥ 0V, (1) CS2 ≤ 0.2V or (2) CS1# ≥ V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V	
Data retention current	I_{CCDR}	—	0.45[26]	2	μA	~+25°C	V_{CC} = 3.0V, Vin ≥ 0V, (1) CS2 ≤ 0.2V or (2) CS1# ≥ V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V
		—	0.6[27]	4	μA	~+40°C	
		—	—	7	μA	~+70°C	
		—	—	10	μA	~+85°C	
Chip deselect time to data retention	t_{CDR}	0	—	—	ns	See retention waveform.	
Operation recovery time	t_R	5	—	—	ms		

Note 26. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=25ºC), and not 100% tested.
27. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=40ºC), and not 100% tested.
28. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer and DQ buffer. If CS2 controls data retention mode, Vin levels (address, WE#, CS1#, OE#, DQ) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2 ≥ V_{CC}-0.2V or CS2 ≤ 0.2V. The other inputs levels (address, WE#, OE#, DQ) can be in the high-impedance state.

Low Vcc Data Retention Timing Waveforms (CS1# controlled)



Low Vcc Data Retention Timing Waveforms (CS2 controlled)



Revision History	RMLV0808BGSB Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	2014.11.28	—	First Edition issued
2.00	2015.06.26	P.1, 4 P.2 P.4 P.11	Standby current I_{SB1} : 25°C 0.6µA ->0.45µA (typ.), 40°C 2µA ->0.6µA (typ.) Modefy Pin Arrangement : Add 1pin Mark Average operating current I_{CC2} : 25°C 2mA ->1.5mA (typ.) Data retention current I_{CCDR} : 25°C 0.6µA ->0.45µA (typ.), 40°C 2µA ->0.6µA (typ.)
2.01	2020.02.20	Last page	Updated the Notice to the latest version

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