

RMLV0816BGSA - 4S2

8Mb Advanced LPSRAM (512k word × 16bit / 1024k word × 8bit)

R10DS0252EJ0201
Rev.2.01
2020.02.20

Description

The RMLV0816BGSA is a family of 8-Mbit static RAMs organized 524,288-word × 16-bit, fabricated by Renesas's high-performance Advanced LPSRAM technologies. The RMLV0816BGSA has realized higher density, higher performance and low power consumption. The RMLV0816BGSA offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 48pin TSOP (I).

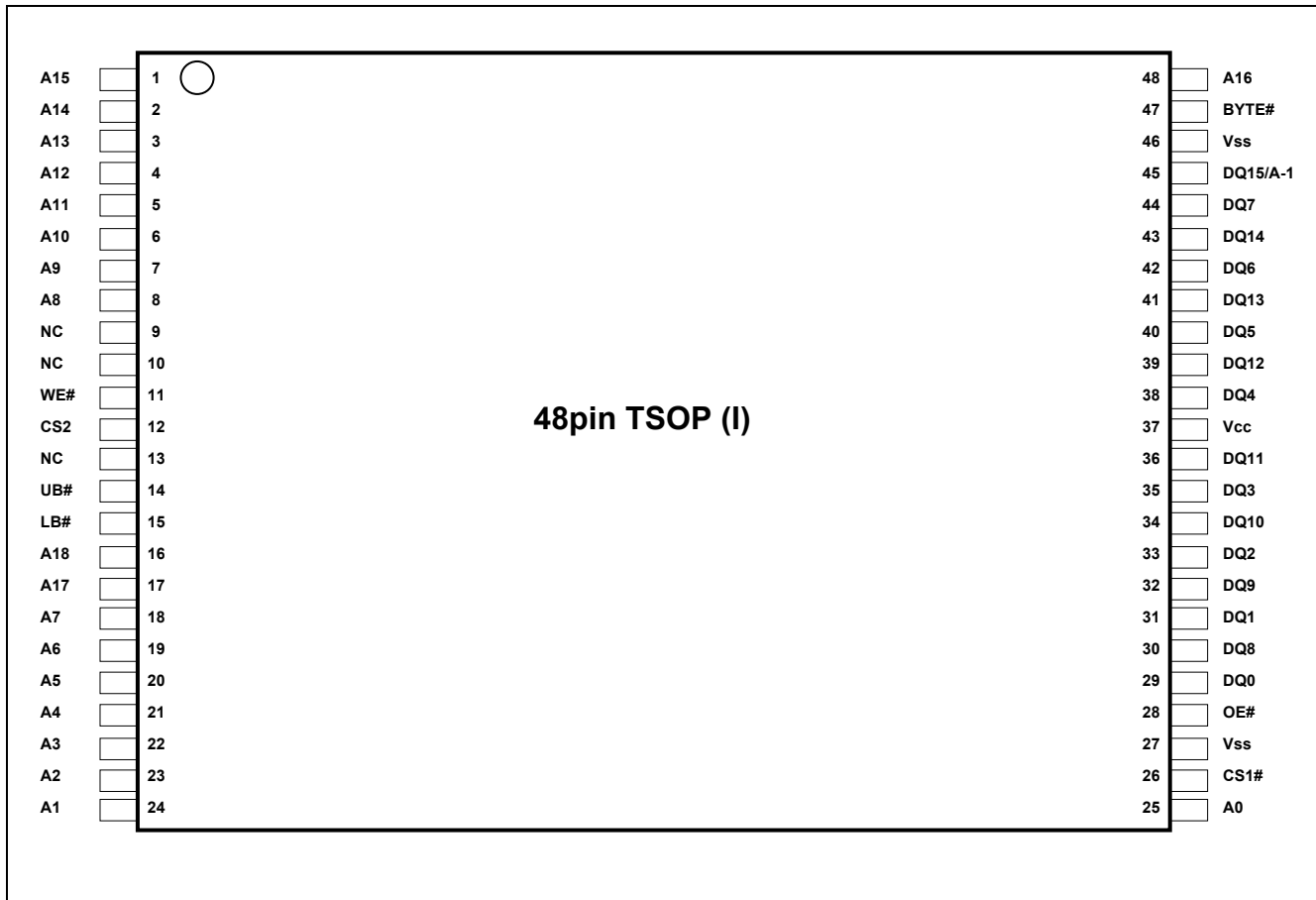
Features

- Single 3V supply: 2.4V to 3.6V
- Access time:
 - Power supply voltage from 2.7V to 3.6V: 45ns (max.)
 - Power supply voltage from 2.4V to 2.7V: 55ns (max.)
- Current consumption:
 - Standby: 0.45μA (typ.)
- Equal access and cycle times
- Common data input and output
 - Three state output
- Directly TTL compatible
 - All inputs and outputs
- Battery backup operation

Part Name Information

Part Name	Power supply	Access time	Temperature Range	Package
RMLV0816BGSA-4S2	2.7V to 3.6V	45 ns	-40 ~ +85°C	12mm x 20mm 48pin plastic TSOP (I)
	2.4V to 2.7V	55 ns		

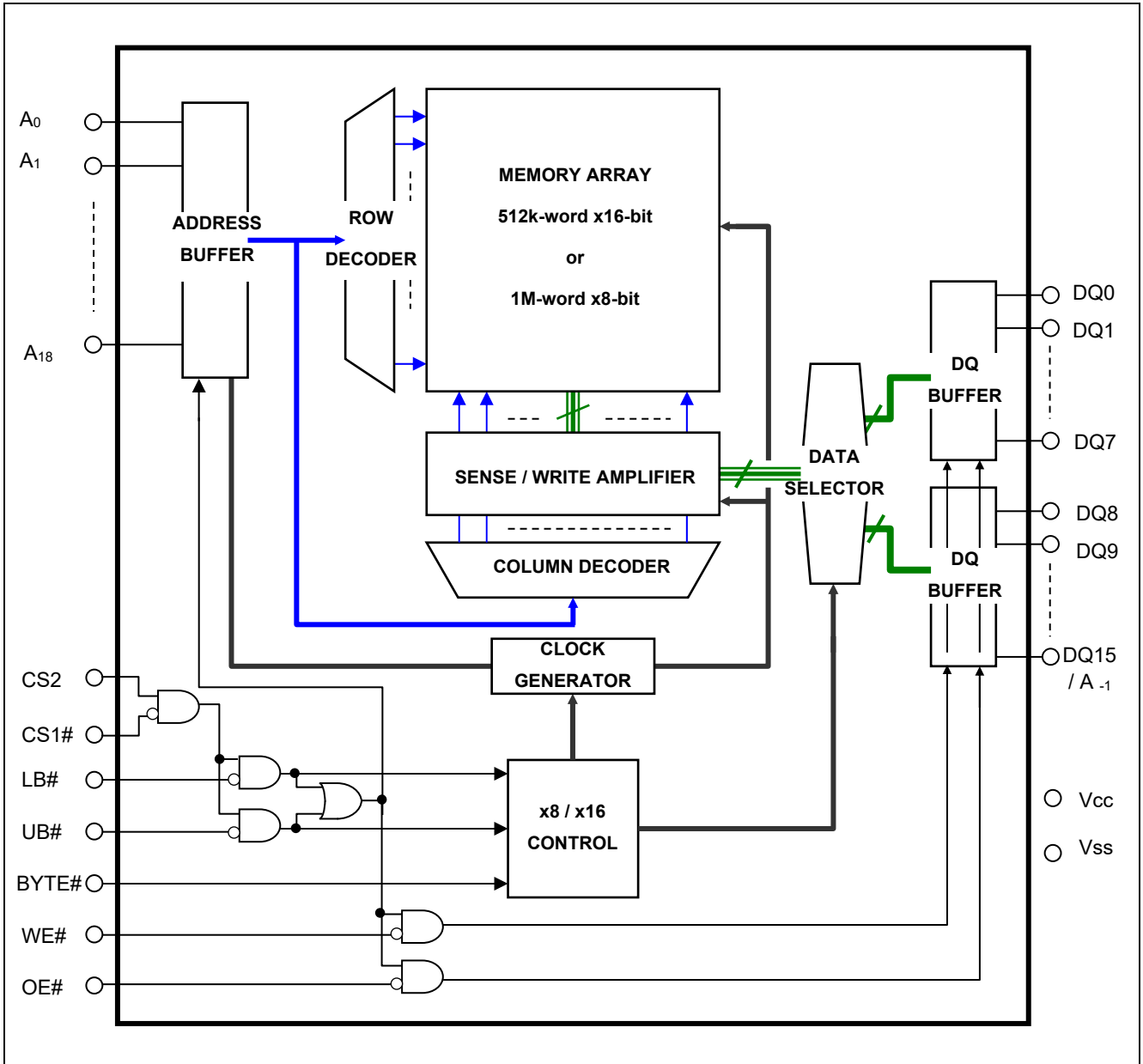
Pin Arrangement



Pin Description

Pin name	Function
V _{CC}	Power supply
V _{SS}	Ground
A0 to A18	Address input (word mode)
A-1 to A18	Address input (byte mode)
DQ0 to DQ15	Data input/output
CS1#	Chip select 1
CS2	Chip select 2
OE#	Output enable
WE#	Write enable
LB#	Lower byte select
UB#	Upper byte select
BYTE#	Byte control mode enable
NC	No connection

Block Diagram



Operation Table

CS1#	CS2	BYTE#	UB#	LB#	WE#	OE#	DQ0~7	DQ8~14	DQ15	Operation
H	X	X	X	X	X	X	High-Z	High-Z	High-Z	Stand-by
X	L	X	X	X	X	X	High-Z	High-Z	High-Z	Stand-by
X	X	H	H	H	X	X	High-Z	High-Z	High-Z	Stand-by
L	H	H	H	L	L	X	Din	High-Z	High-Z	Write in lower byte
L	H	H	H	L	H	L	Dout	High-Z	High-Z	Read in lower byte
L	H	H	H	L	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	L	H	L	X	High-Z	Din	Din	Write in upper byte
L	H	H	L	H	H	L	High-Z	Dout	Dout	Read in upper byte
L	H	H	L	H	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	L	L	L	X	Din	Din	Din	Word write
L	H	H	L	L	H	L	Dout	Dout	Dout	Word read
L	H	H	L	L	H	H	High-Z	High-Z	High-Z	Output disable
L	H	L	X	X	L	X	Din	High-Z	A-1	Byte write
L	H	L	X	X	H	L	Dout	High-Z	A-1	Byte read
L	H	L	X	X	H	H	High-Z	High-Z	A-1	Output disable

Note 1. H: V_{IH} L: V_{IL} X: V_{IH} or V_{IL}

Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5^2 to $V_{CC}+0.3^3$	V
Power dissipation	P_T	0.7	W
Operation temperature	T_{opr}	-40 to +85	°C
Storage temperature range	T_{stg}	-65 to +150	°C
Storage temperature range under bias	T_{bias}	-40 to +85	°C

Note 2. -3.0V for pulse \leq 30ns (full width at half maximum)

3. Maximum voltage is +4.6V.

DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Supply voltage	V_{CC}	2.4	3.0	3.6	V		
	V_{SS}	0	0	0	V		
Input high voltage	V_{IH}	2.0	—	$V_{CC}+0.2$	V	$V_{CC}=2.4V$ to $2.7V$	
		2.2	—	$V_{CC}+0.2$	V	$V_{CC}=2.7V$ to $3.6V$	
Input low voltage	V_{IL}	-0.2	—	0.4	V	$V_{CC}=2.4V$ to $2.7V$	4
		-0.2	—	0.6	V	$V_{CC}=2.7V$ to $3.6V$	4
Ambient temperature range	T_a	-40	—	+85	°C		

Note 4. -3.0V for pulse \leq 30ns (full width at half maximum)

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	
Input leakage current	$ I_{LI} $	—	—	1	μA	$V_{in} = V_{SS}$ to V_{CC}	
Output leakage current	$ I_{LO} $	—	—	1	μA	BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$ CS1# = V_{IH} or CS2 = V_{IL} or OE# = V_{IH} or WE# = V_{IL} or LB# = UB# = V_{IH} , $V_{I/O} = V_{SS}$ to V_{CC}	
Average operating current	I_{CC1}	—	20^{*5}	25	mA	Cycle = 55ns, duty = 100%, $I_{I/O} = 0\text{mA}$, BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$ CS1# = V_{IL} , CS2 = V_{IH} , Others = V_{IH}/V_{IL}	
		—	25^{*5}	30	mA	Cycle = 45ns, duty = 100%, $I_{I/O} = 0\text{mA}$, BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$ CS1# = V_{IL} , CS2 = V_{IH} , Others = V_{IH}/V_{IL}	
	I_{CC2}	—	1.5^{*5}	3	mA	Cycle = 1 μs , duty = 100%, $I_{I/O} = 0\text{mA}$, BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$ CS1# $\leq 0.2\text{V}$, CS2 $\geq V_{CC} - 0.2\text{V}$, $V_{IH} \geq V_{CC} - 0.2\text{V}$, $V_{IL} \leq 0.2\text{V}$	
Standby current	I_{SB}	—	—	0.3	mA	BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$ CS2 = V_{IL} , Others = V_{SS} to V_{CC}	
Standby current	I_{SB1}	—	0.45^{*5}	2	μA	$\sim +25^{\circ}\text{C}$	$V_{in} = V_{SS}$ to V_{CC} , BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$
		—	0.6^{*6}	4	μA	$\sim +40^{\circ}\text{C}$	(1) CS2 $\leq 0.2\text{V}$ or
		—	—	7	μA	$\sim +70^{\circ}\text{C}$	(2) CS1# $\geq V_{CC} - 0.2\text{V}$, CS2 $\geq V_{CC} - 0.2\text{V}$ or
		—	—	10	μA	$\sim +85^{\circ}\text{C}$	(3) LB# = UB# $\geq V_{CC} - 0.2\text{V}$, CS1# $\leq 0.2\text{V}$, CS2 $\geq V_{CC} - 0.2\text{V}$
Output high voltage	V_{OH}	2.4	—	—	V	BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$ $I_{OH} = -1\text{mA}$ $V_{CC} \geq 2.7\text{V}$	
	V_{OH2}	2.0	—	—	V	BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$ $I_{OH} = -0.1\text{mA}$	
Output low voltage	V_{OL}	—	—	0.4	V	BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$ $I_{OL} = 2\text{mA}$ $V_{CC} \geq 2.7\text{V}$	
	V_{OL2}	—	—	0.4	V	BYTE# $\geq V_{CC} - 0.2\text{V}$ or BYTE# $\leq 0.2\text{V}$ $I_{OL} = 0.1\text{mA}$	

Note 5. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a = 25^{\circ}\text{C}$), and not 100% tested.

Note 6. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a = 40^{\circ}\text{C}$), and not 100% tested.

Capacitance

($T_a = 25^{\circ}\text{C}$, $f = 1\text{MHz}$)

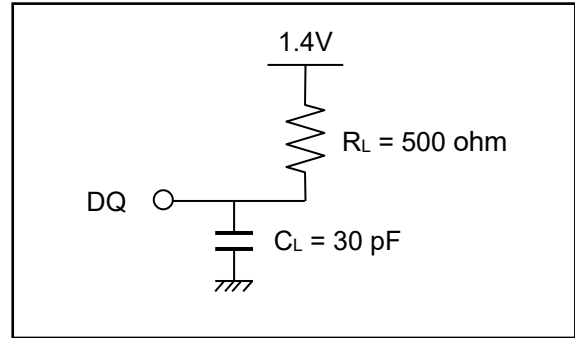
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C_{in}	—	—	8	pF	$V_{in} = 0\text{V}$	7
Input / output capacitance	$C_{I/O}$	—	—	10	pF	$V_{I/O} = 0\text{V}$	7

Note 7. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions ($V_{CC} = 2.4V \sim 3.6V$, $T_a = -40 \sim +85^{\circ}C$)

- Input pulse levels:
 - $V_{IL} = 0.4V$, $V_{IH} = 2.4V$ ($V_{CC}=2.7V$ to $3.6V$)
 - $V_{IL} = 0.4V$, $V_{IH} = 2.2V$ ($V_{CC}=2.4V$ to $2.7V$)
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	$V_{CC}=2.7V$ to $3.6V$		$V_{CC}=2.4V$ to $2.7V$		Unit	Note
		Min.	Max.	Min.	Max.		
Read cycle time	t_{RC}	45	—	55	—	ns	
Address access time	t_{AA}	—	45	—	55	ns	
Chip select access time	t_{ACS1}	—	45	—	55	ns	
	t_{ACS2}	—	45	—	55	ns	
Output enable to output valid	t_{OE}	—	22	—	30	ns	
Output hold from address change	t_{OH}	10	—	10	—	ns	
LB#, UB# access time	t_{BA}	—	45	—	55	ns	
Chip select to output in low-Z	t_{CLZ1}	10	—	10	—	ns	8,9
	t_{CLZ2}	10	—	10	—	ns	8,9
LB#, UB# enable to low-Z	t_{BLZ}	5	—	5	—	ns	8,9
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	8,9
Chip deselect to output in high-Z	t_{CHZ1}	0	18	0	20	ns	8,9,10
	t_{CHZ2}	0	18	0	20	ns	8,9,10
LB#, UB# disable to high-Z	t_{BHZ}	0	18	0	20	ns	8,9,10
Output disable to output in high-Z	t_{OHZ}	0	18	0	20	ns	8,9,10

Note 8. This parameter is sampled and not 100% tested.

9. At any given temperature and voltage condition, t_{CHZ1} max is less than t_{CLZ1} min, t_{CHZ2} max is less than t_{CLZ2} min, t_{BHZ} max is less than t_{BLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.

10. t_{CHZ1} , t_{CHZ2} , t_{BHZ} and t_{OHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

Write Cycle

Parameter	Symbol	Vcc=2.7V to 3.6V		Vcc=2.4V to 2.7V		Unit	Note
		Min.	Max.	Min.	Max.		
Write cycle time	t _{WC}	45	—	55	—	ns	
Address valid to write end	t _{AW}	35	—	50	—	ns	
Chip select to write end	t _{CW}	35	—	50	—	ns	
Write pulse width	t _{WP}	35	—	40	—	ns	11
LB#,UB# valid to write end	t _{BW}	35	—	50	—	ns	
Address setup time to write start	t _{AS}	0	—	0	—	ns	
Write recovery time from write end	t _{WR}	0	—	0	—	ns	
Data to write time overlap	t _{DW}	25	—	25	—	ns	
Data hold from write end	t _{DH}	0	—	0	—	ns	
Output enable from write end	t _{OW}	5	—	5	—	ns	12
Output disable to output in high-Z	t _{OHZ}	0	18	0	20	ns	12,13
Write to output in high-Z	t _{WHZ}	0	18	0	20	ns	12,13

Note 11. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

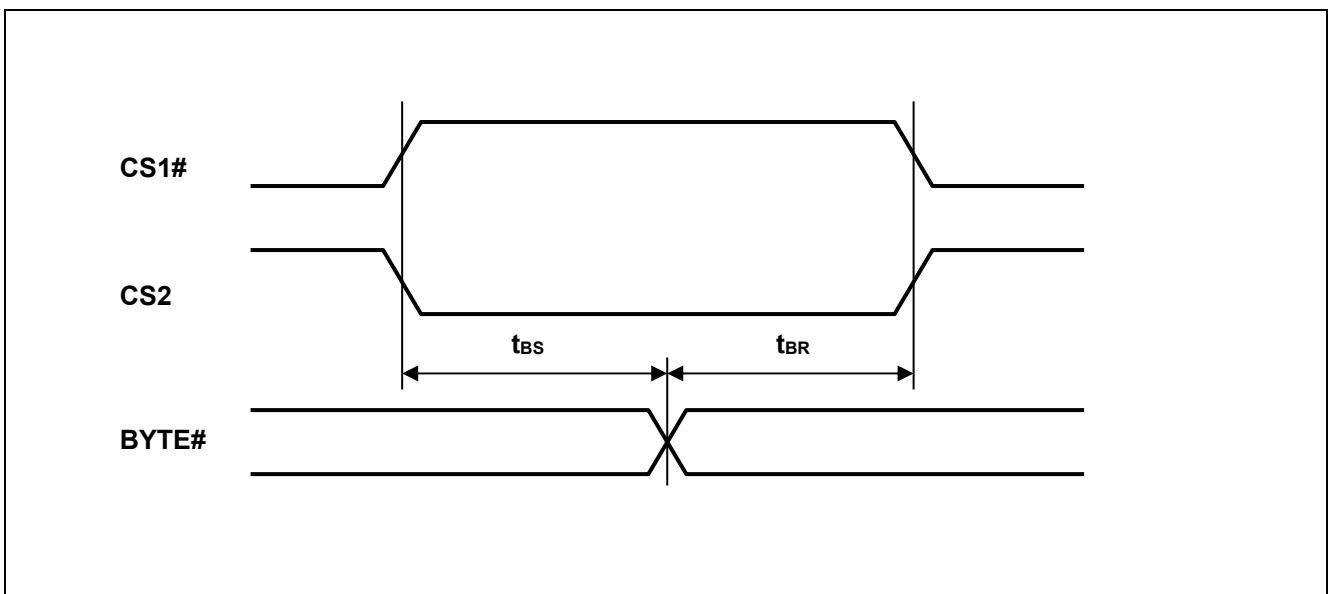
12. This parameter is sampled and not 100% tested.

13. t_{OHZ} and t_{WHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

BYTE# Timing Conditions

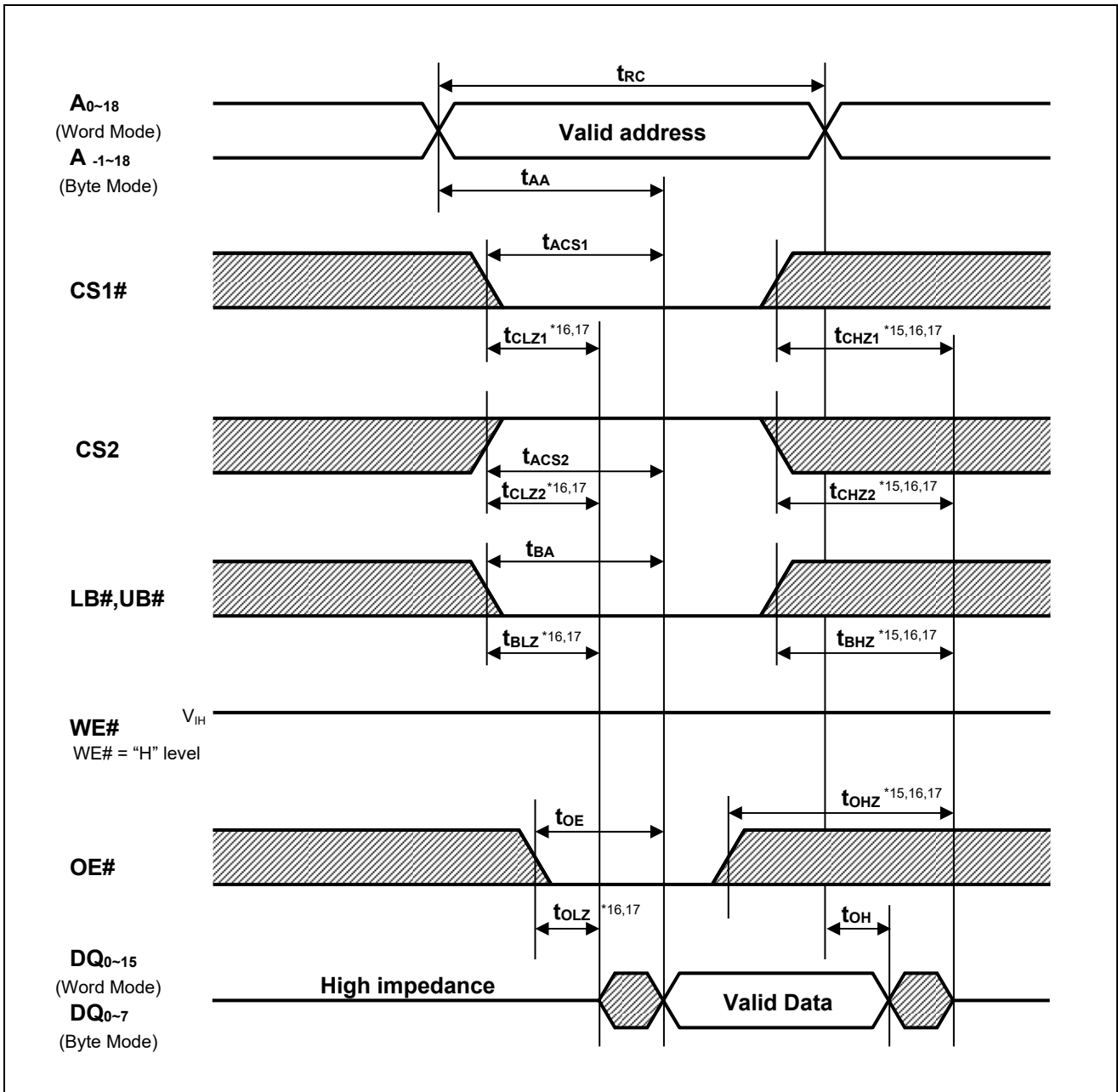
Parameter	Symbol	Vcc=2.7V to 3.6V		Vcc=2.4V to 2.7V		Unit	Note
		Min.	Max.	Min.	Max.		
Byte setup time	t _{BS}	5	—	5	—	ms	
Byte recovery time	t _{BR}	5	—	5	—	ms	

BYTE# Timing Waveforms



Timing Waveforms

Read Cycle^{*14}



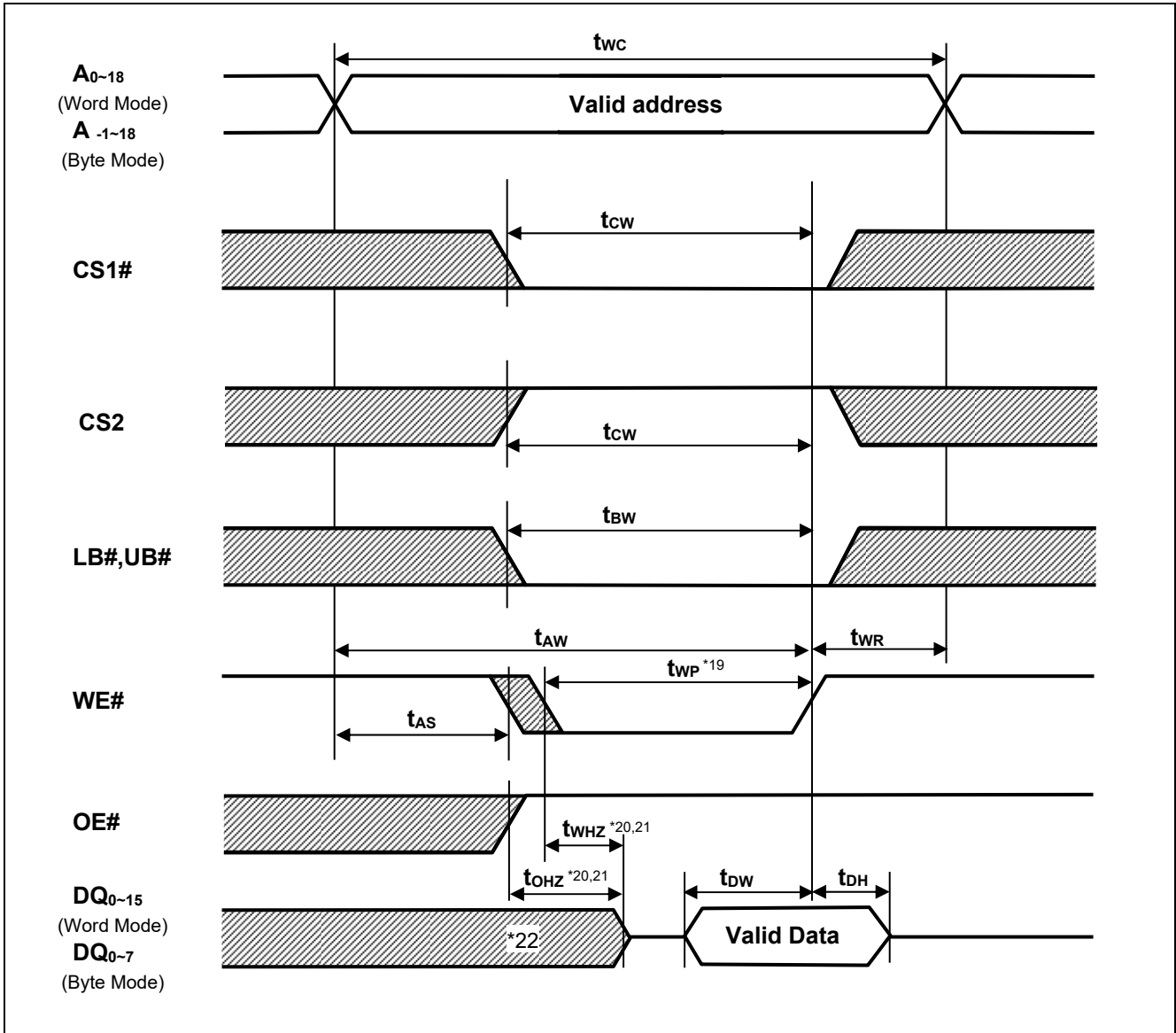
Note 14. BYTE# $\geq V_{CC} - 0.2V$ or BYTE# $\leq 0.2V$

15. t_{CHZ1} , t_{CHZ2} , t_{BHZ} and t_{OHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

16. This parameter is sampled and not 100% tested

17. At any given temperature and voltage condition, t_{CHZ1} max is less than t_{CLZ1} min, t_{CHZ2} max is less than t_{CLZ2} min, t_{BHZ} max is less than t_{BLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.

Write Cycle (1)^{*18} (WE# CLOCK, OE#="H" while writing)



Note 18. $BYTE\# \geq V_{CC} - 0.2V$ or $BYTE\# \leq 0.2V$

19. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

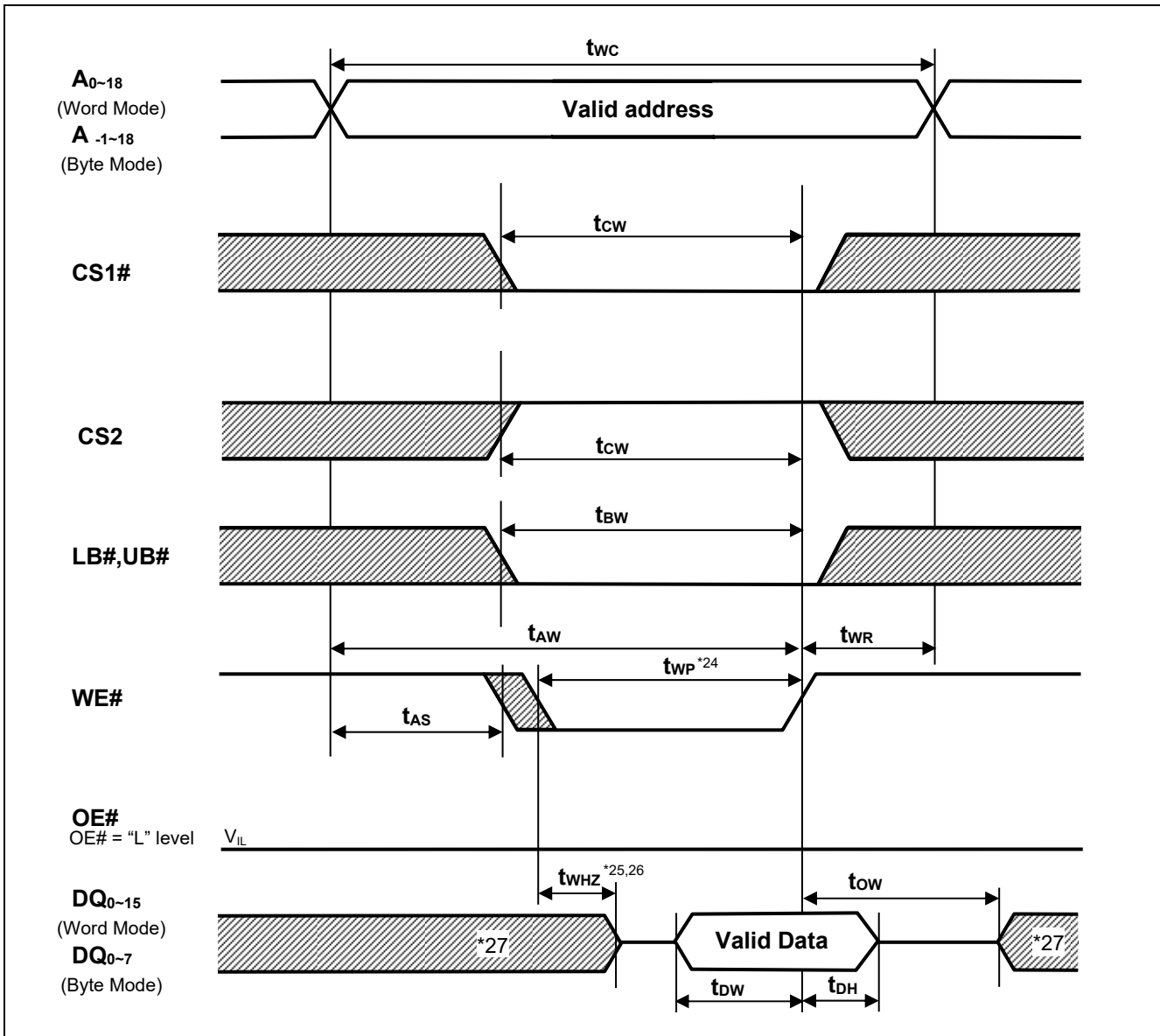
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

20. t_{OHZ} and t_{WHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

21. This parameter is sampled and not 100% tested

22. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

Write Cycle (2)^{*23} (WE# CLOCK, OE# Low Fixed)



Note 23. $BYTE\# \geq V_{CC} - 0.2V$ or $BYTE\# \leq 0.2V$

24. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

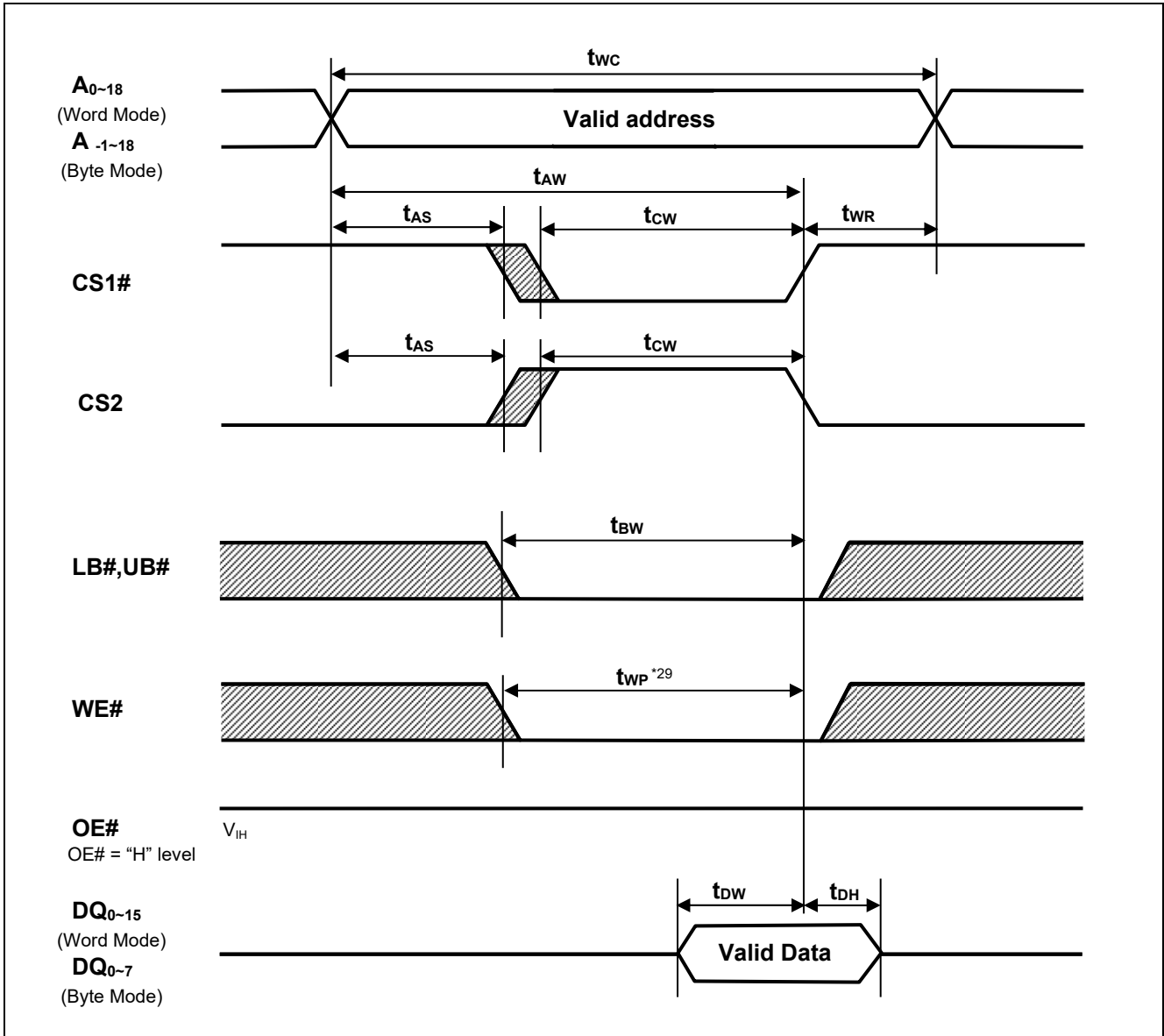
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

25. t_{WHZ} is defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

26. This parameter is sampled and not 100% tested.

27. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

Write Cycle (3)^{*28} (CS1#, CS2 CLOCK)



Note 28. $BYTE\# \geq V_{CC} - 0.2V$ or $BYTE\# \leq 0.2V$

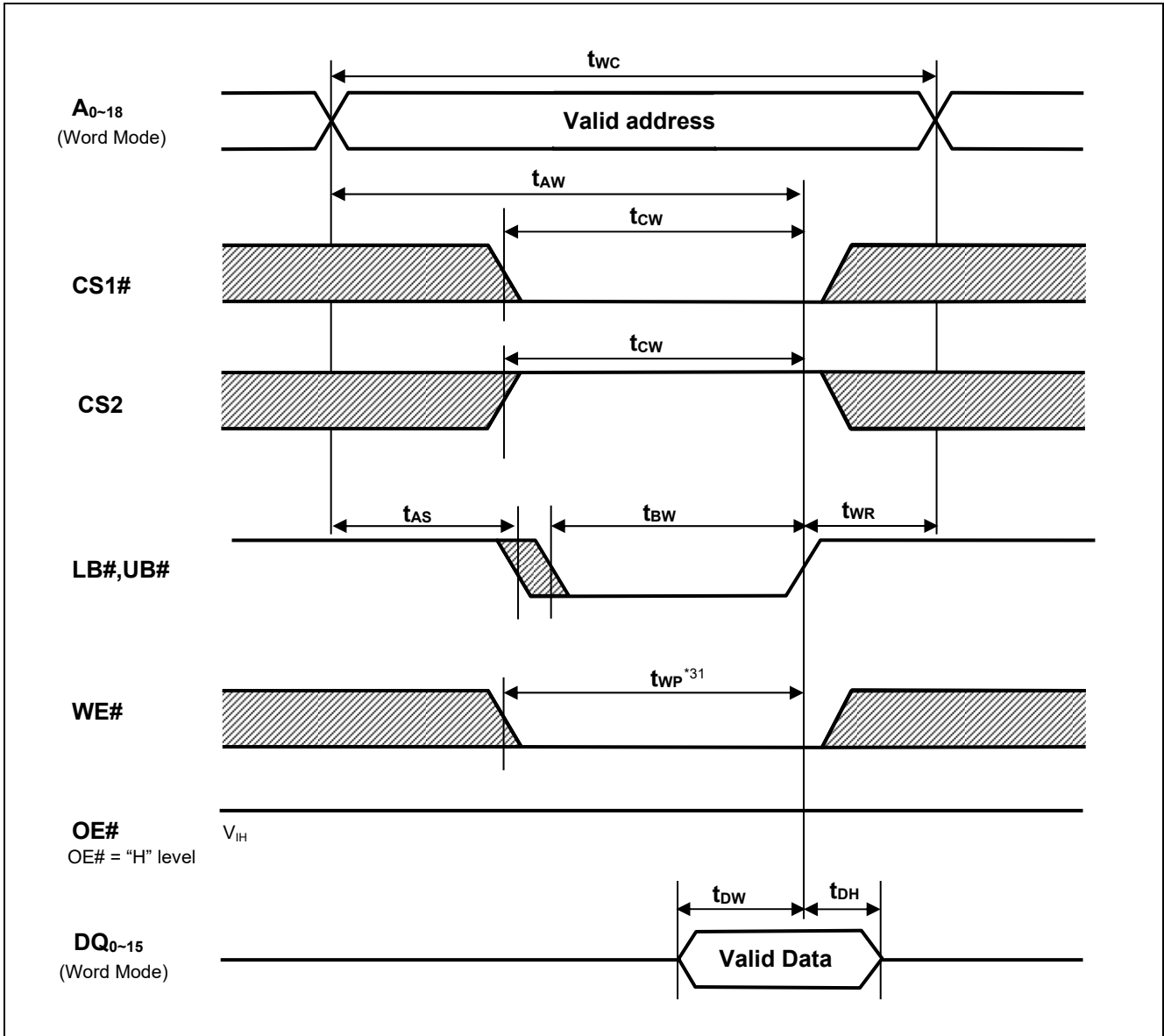
29. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

Write Cycle (4)^{*30} (LB#, UB# CLOCK, Word Mode)



Note 30. BYTE# $\geq V_{CC} - 0.2V$

31. t_{WP} is the interval between write start and write end.

A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.

A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.

A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

Low V_{CC} Data Retention Characteristics

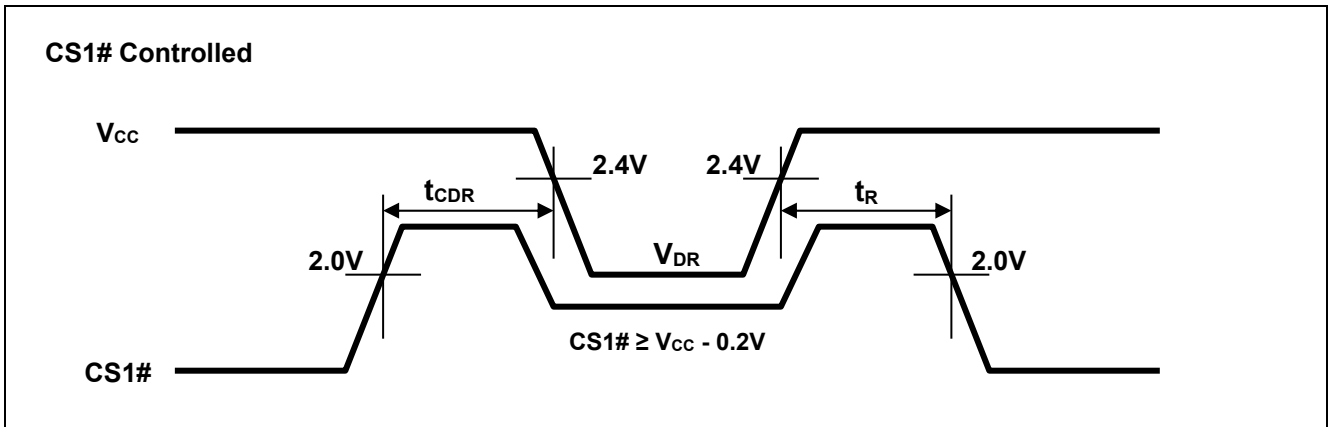
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions ^{*34}	
V_{CC} for data retention	V_{DR}	1.5	—	3.6	V	$V_{in} \geq 0V$, $BYTE\# \geq V_{CC} - 0.2V$ or $BYTE\# \leq 0.2V$ (1) $CS2 \leq 0.2V$ or (2) $CS1\# \geq V_{CC} - 0.2V$, $CS2 \geq V_{CC} - 0.2V$ or (3) $LB\# = UB\# \geq V_{CC} - 0.2V$, $CS1\# \leq 0.2V$, $CS2 \geq V_{CC} - 0.2V$	
Data retention current	I_{CCDR}	—	0.45 ^{*32}	2	μA	$\sim +25^{\circ}C$	$V_{CC} = 3.0V$, $V_{in} \geq 0V$, $BYTE\# \geq V_{CC} - 0.2V$ or $BYTE\# \leq 0.2V$ (1) $CS2 \leq 0.2V$ or (2) $CS1\# \geq V_{CC} - 0.2V$, $CS2 \geq V_{CC} - 0.2V$ or (3) $LB\# = UB\# \geq V_{CC} - 0.2V$, $CS1\# \leq 0.2V$, $CS2 \geq V_{CC} - 0.2V$
		—	0.6 ^{*33}	4	μA	$\sim +40^{\circ}C$	
		—	—	7	μA	$\sim +70^{\circ}C$	
		—	—	10	μA	$\sim +85^{\circ}C$	
Chip deselect time to data retention	t_{CDR}	0	—	—	ns	See retention waveform.	
Operation recovery time	t_R	5	—	—	ms		

Note 32. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a = 25^{\circ}C$), and not 100% tested.

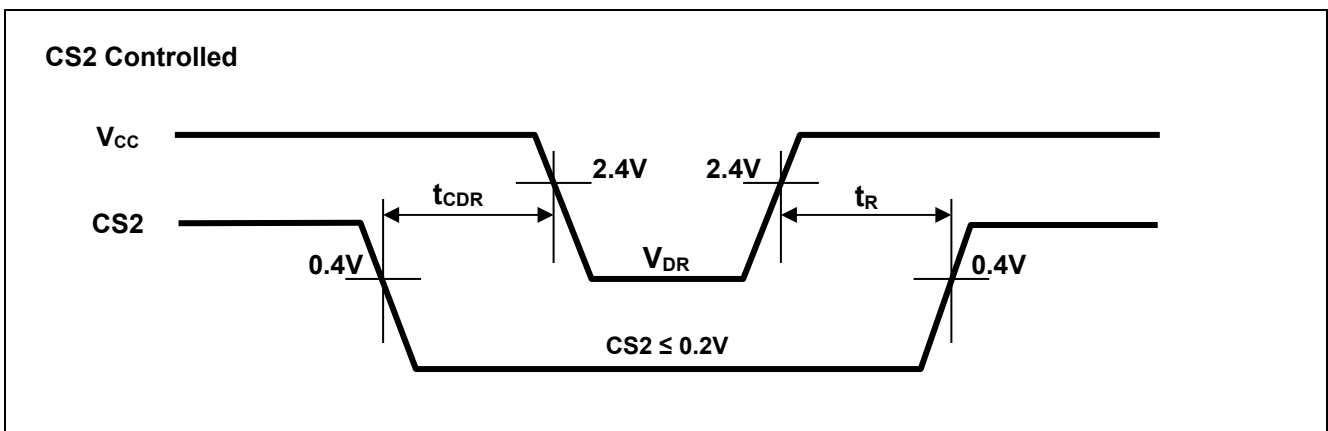
33. Typical parameter indicates the value for the center of distribution at 3.0V ($T_a = 40^{\circ}C$), and not 100% tested.

34. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB# buffer, UB# buffer and DQ buffer. If CS2 controls data retention mode, V_{in} levels (address, WE#, CS1#, OE#, LB#, UB#, DQ) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$. The other inputs levels (address, WE#, OE#, LB#, UB#, DQ) can be in the high-impedance state.

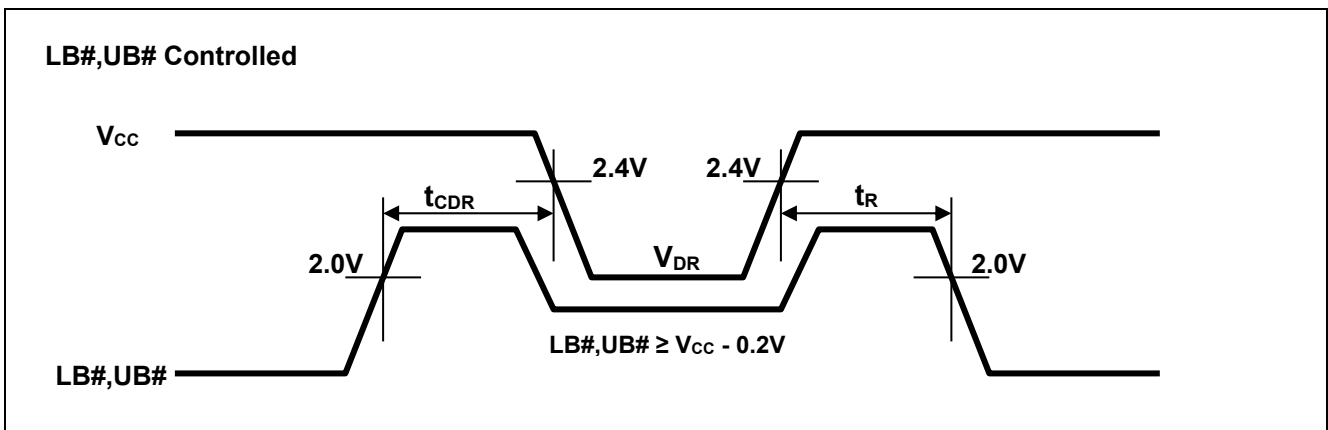
Low Vcc Data Retention Timing Waveforms (CS1# controlled)^{*35}



Low Vcc Data Retention Timing Waveforms (CS2 controlled)^{*35}



Low Vcc Data Retention Timing Waveforms (LB#,UB# controlled, Word Mode)^{*36}



Note 35. $BYTE\# \geq V_{CC} - 0.2V$ or $BYTE\# \leq 0.2V$

36. $BYTE\# \geq V_{CC} - 0.2V$

Revision History	RMLV0816BGSA Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	2014.11.28	—	First Edition issued
2.00	2015.06.26	P.1, 5 P.5 P.13	Standby current I_{SB1} : 25°C 0.6μA ->0.45μA (typ.), 40°C 2μA ->0.6μA (typ.) Average operating current I_{CC2} : 25°C 2mA ->1.5mA (typ.) Data retention current I_{CCDR} : 25°C 0.6μA ->0.45μA (typ.), 40°C 2μA ->0.6μA (typ.)
2.01	2020.02.20	Last page	Updated the Notice to the latest version

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[IS64WV3216BLL-15CTLA3](#) [IS66WVE4M16ECLL-70BLI](#) [PCF8570P](#) [K6F2008V2E-LF70000](#) [K6T4008C1B-GB70](#) [CY7C1353S-100AXC](#)
[AS6C8016-55BIN](#) [AS7C164A-15PCN](#) [515712X](#) [IS62WV51216EBLL-45BLI](#) [IS63WV1288DBLL-10HLI](#) [IS66WVE2M16ECLL-70BLI](#)
[IS66WVE4M16EALL-70BLI](#) [IS61WV102416DBLL-10TLI](#) [CY7C1381KV33-100AXC](#) [CY7C1460KV25-200BZI](#) [CY7C1373KV33-100AXC](#)
[CY7C1381KVE33-133AXI](#) [CY7C4121KV13-600FCXC](#) [GS882Z18CD-150I](#) [IS66WVC2M16ECLL-7010BLI](#) [7140LA35PDG](#)
[CY7C1380KV33-250AXC](#) [AS6C8016-55BINTR](#) [CY7C1370KV33-250AXC](#) [CY7C1370KVE33-167AXI](#) [7140LA100PDG](#) [AS7C34096B-](#)
[10TIN](#) [AS6C8016-55TIN](#) [IS62WV25616EALL-55TLI](#) [GS8128418B-167IV](#) [CY7C1460KV25-200BZXI](#) [CY7C1460KV25-167BZXI](#)
[CY7C1315KV18-333BZXC](#) [CY7C1370KV25-200AXC](#) [71421LA55JI8](#) [CY62158G30-45ZSXI](#) [CY62157G30-45ZSXI](#) [RMLV3216AGSD-](#)
[5S2#AA0](#) [CY62187G30-55BAXI](#) [CY62157G30-45ZXI](#) [IS61VVPS102436B-200B3LI](#) [IS66WVC2M16EALL-7010BLI](#)
[IS66WVE4M16EALL-70BLI-TR](#)