RMLV3216A Series

32Mb Advanced LPSRAM (2M word × 16bit / 4M word x 8bit)

R10DS0277EJ0100
Rev.1.00
2018.12.26

Description

The RMLV3216A Series is a family of 32-Mbit static RAMs organized 2,097,152-word × 16-bit, fabricated by Renesas's high-performance Advanced LPSRAM technologies. The RMLV3216A Series has realized higher density, higher performance and low power consumption. The RMLV3216A Series offers low power standby power dissipation; therefore, it is suitable for battery backup systems. It is offered in 48pin TSOP (I), 52pin µTSOP (II) or 48-ball fine pitch ball grid array.

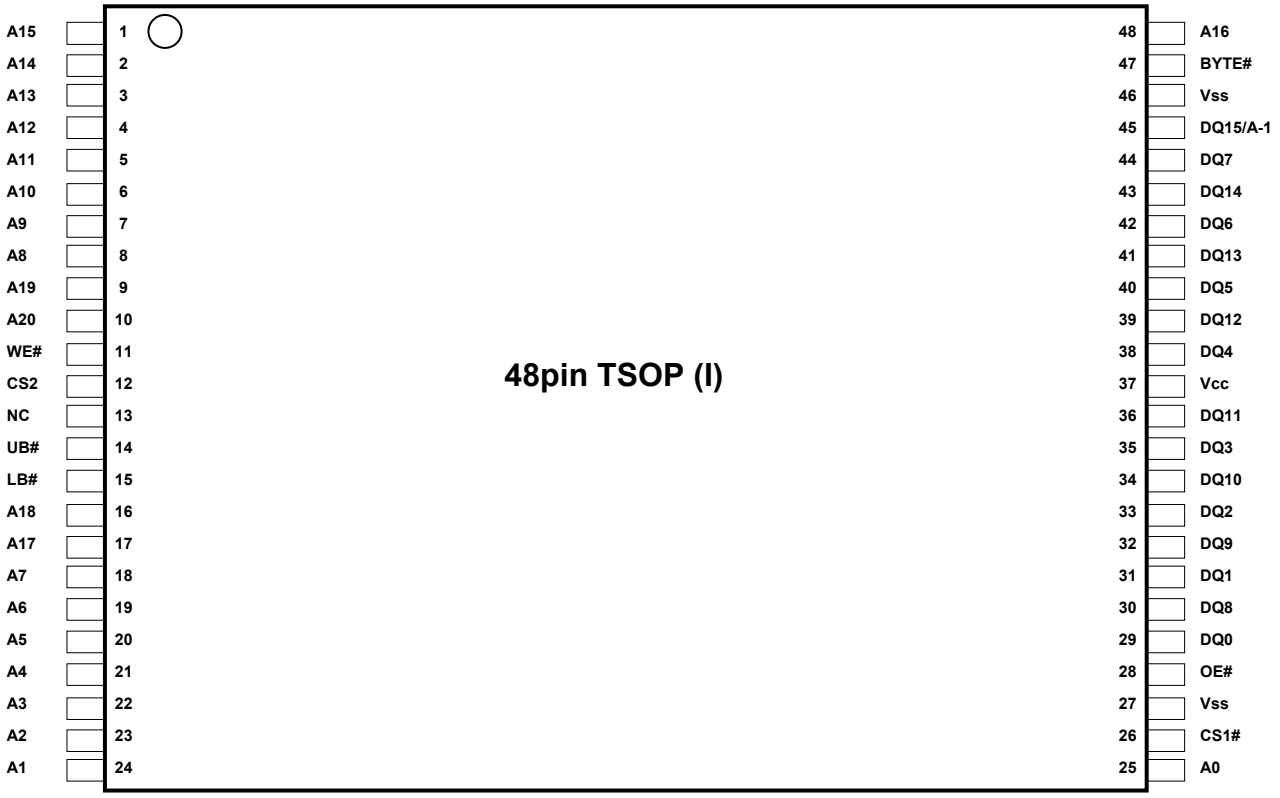
Features

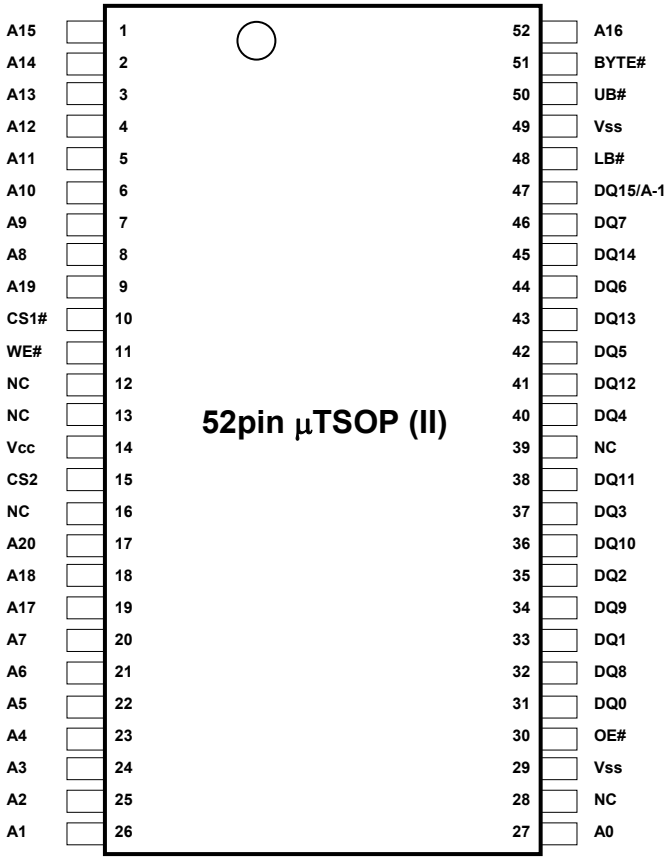
- Single 3V supply: 2.7V to 3.6V
- Access time: 55ns (max.)
- Current consumption:
  — Standby: 0.6µA (typ.)
- Common data input and output
  — Three state output
- Directly TTL compatible
  — All inputs and outputs
- Battery backup operation

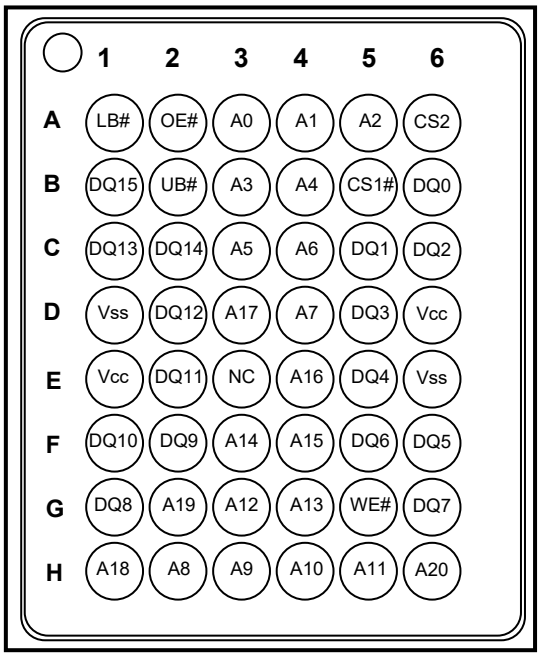
Part Name Information

Part Name	Access time	Temperature Range	Package
RMLV3216AGSA-5S2	55 ns	-40 ~ +85°C	12mm x 20mm 48pin plastic TSOP (I)
RMLV3216AGSD-5S2			10.79mm × 10.49mm 52pin plastic µTSOP (II)
RMLV3216AGBG-5S2			48-ball FBGA with 0.75mm ball pitch

Pin Arrangement



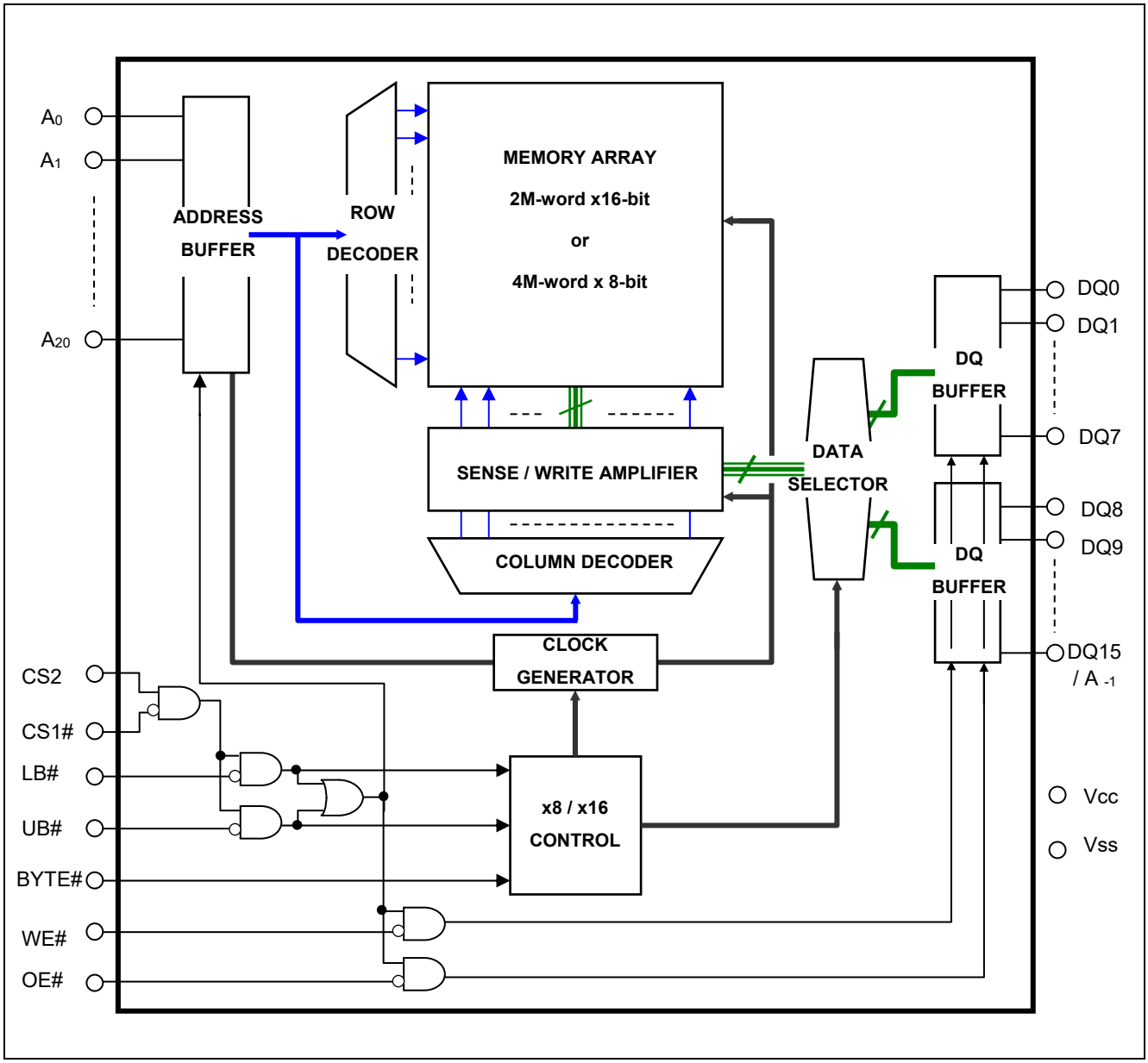




Pin Description

Pin name	Function
V_{CC}	Power supply
V_{SS}	Ground
A0 to A20	Address input (word mode)
A-1 to A20	Address input (byte mode)
DQ0 to DQ15	Data input/output
CS1#	Chip select 1
CS2	Chip select 2
OE#	Output enable
WE#	Write enable
LB#	Lower byte select
UB#	Upper byte select
BYTE#	Byte control mode enable
NC	No connection

Block Diagram



Note 1. BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.

Operation Table

CS1#	CS2	BYTE#	UB#	LB#	WE#	OE#	DQ0~7	DQ8~14	DQ15	Operation
H	X	X	X	X	X	X	High-Z	High-Z	High-Z	Stand-by
X	L	X	X	X	X	X	High-Z	High-Z	High-Z	Stand-by
X	X	H	H	H	X	X	High-Z	High-Z	High-Z	Stand-by
L	H	H	H	L	L	X	Din	High-Z	High-Z	Write in lower byte
L	H	H	H	L	H	L	Dout	High-Z	High-Z	Read in lower byte
L	H	H	H	L	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	L	H	L	X	High-Z	Din	Din	Write in upper byte
L	H	H	L	H	H	L	High-Z	Dout	Dout	Read in upper byte
L	H	H	L	H	H	H	High-Z	High-Z	High-Z	Output disable
L	H	H	L	L	L	X	Din	Din	Din	Word write
L	H	H	L	L	H	L	Dout	Dout	Dout	Word read
L	H	H	L	L	H	H	High-Z	High-Z	High-Z	Output disable
L	H	L	X	X	L	X	Din	High-Z	A-1	Byte write
L	H	L	X	X	H	L	Dout	High-Z	A-1	Byte read
L	H	L	X	X	H	H	High-Z	High-Z	A-1	Output disable

Note 2. H: V_{IH} L:V_{IL} X: V_{IH} or V_{IL}

3. BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.
48-ball FBGA type equals BYTE#=H mode.

Absolute Maximum Ratings

Parameter	Symbol	Value	unit
Power supply voltage relative to V_{SS}	V_{CC}	-0.5 to +4.6	V
Terminal voltage on any pin relative to V_{SS}	V_T	-0.5[*4] to V_{CC}+0.3[*5]	V
Power dissipation	P_T	0.7	W
Operation temperature	Topr	-40 to +85	°C
Storage temperature range	Tstg	-65 to +150	°C
Storage temperature range under bias	Tbias	-40 to +85	°C

Note 4. -2.0V for pulse ≤ 30ns (full width at half maximum)

5. Maximum voltage is +4.6V.

DC Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit	Note
Supply voltage	V_{CC}	2.7	3.0	3.6	V	
	V_{SS}	0	0	0	V	
Input high voltage	V_{IH}	2.2	—	V_{CC}+0.3	V	
Input low voltage	V_{IL}	-0.3	—	0.6	V	6
Ambient temperature range	Ta	-40	—	+85	°C	

Note 6. -2.0V for pulse ≤ 30ns (full width at half maximum)

DC Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions[*7]
Input leakage current	$\lvert I_{LI} \rvert$	—	—	1	µA	Vin = V_{SS} to V_{CC}
Output leakage current	$\lvert I_{LO} \rvert$	—	—	1	µA	CS1# = V_{IH} or CS2 = V_{IL} or OE# = V_{IH} or WE# = V_{IL} or LB# = UB# = V_{IH}, $V_{I/O}$ = V_{SS} to V_{CC}
Average operating current	I_{CC1}	—	27[*8]	35	mA	Cycle = 55ns, duty =100%, $I_{I/O}$ = 0mA, CS1# = V_{IL}, CS2 = V_{IH}, Others = V_{IH}/V_{IL}
	I_{CC2}	—	2[*8]	4	mA	Cycle = 1µs, duty =100%, $I_{I/O}$ = 0mA, CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V, V_{IH} ≥ V_{CC}-0.2V, V_{IL} ≤ 0.2V
Standby current	I_{SB}	—	0.1[*8]	0.3	mA	CS2 = V_{IL}, Others = V_{SS} to V_{CC}
Standby current	I_{SB1}	—	0.6[*8]	4	µA	~+25°C	Vin = V_{SS} to V_{CC}, (1) CS2 ≤ 0.2V or (2) CS1# ≥ V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V or (3) LB# = UB# ≥ V_{CC}-0.2V, CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V
		—	1[*9]	6	µA	~+40°C	
		—	4[*10]	17	µA	~+70°C	
		—	8[*11]	24	µA	~+85°C	
Output high voltage	V_{OH}	2.4	—	—	V	I_{OH} = -1mA	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 2mA	

Note 7. BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.
BYTE# ≥ Vcc - 0.2V or BYTE# ≤ 0.2V

8. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=25ºC), and not 100% tested.
9. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=40ºC), and not 100% tested.
10. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=70ºC), and not 100% tested.
11. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=85ºC), and not 100% tested.

Capacitance

(Ta =25°C, f =1MHz)

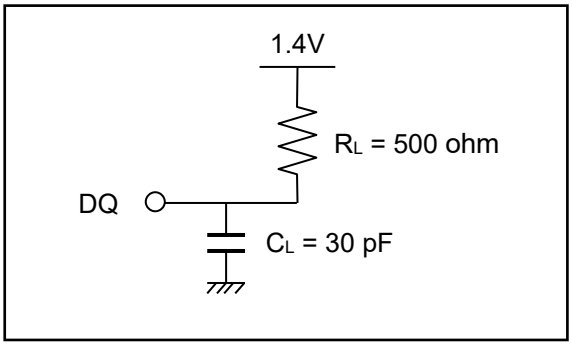
Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions	Note
Input capacitance	C in	—	—	10	pF	Vin =0V	12
Input / output capacitance	C I/O	—	—	10	pF	$V_{I/O}$ =0V	12

Note 12. This parameter is sampled and not 100% tested.

AC Characteristics

Test Conditions (Vcc = 2.7V ~ 3.6V, Ta = -40 ~ +85°C)

- Input pulse levels:
  V_{IL} = 0.4V, V_{IH} = 2.4V
- Input rise and fall time: 5ns
- Input and output timing reference level: 1.4V
- Output load: See figures (Including scope and jig)



Read Cycle

Parameter	Symbol	Min.	Max.	Unit	Note
Read cycle time	t_{RC}	55		ns	
Address access time	t_{AA}	—	55	ns	
Chip select access time	t_{ACS1}	—	45	ns	
	t_{ACS2}	—	45	ns	
Output enable to output valid	t_{OE}	—	22	ns	
Output hold from address change	t_{OH}	10	—	ns	
LB#, UB# access time	t_{BA}	—	45	ns	
Chip select to output in low-Z	t_{CLZ1}	10	—	ns	13,14
	t_{CLZ2}	10	—	ns	13,14
LB#, UB# enable to low-Z	t_{BLZ}	5	—	ns	13,14
Output enable to output in low-Z	t_{OLZ}	5	—	ns	13,14
Chip deselect to output in high-Z	t_{CHZ1}	0	18	ns	13,14,15
	t_{CHZ2}	0	18	ns	13,14,15
LB#, UB# disable to high-Z	t_{BHZ}	0	18	ns	13,14,15
Output disable to output in high-Z	t_{OHZ}	0	18	ns	13,14,15

Note 13. This parameter is sampled and not 100% tested.

14 At any given temperature and voltage condition, t_{CHZ1} max is less than t_{CLZ1} min, t_{CHZ2} max is less than t_{CLZ2} min, t_{BHZ} max is less than t_{BLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.

15. t_{CHZ1}, t_{CHZ2}, t_{BHZ} and t_{OHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

Write Cycle

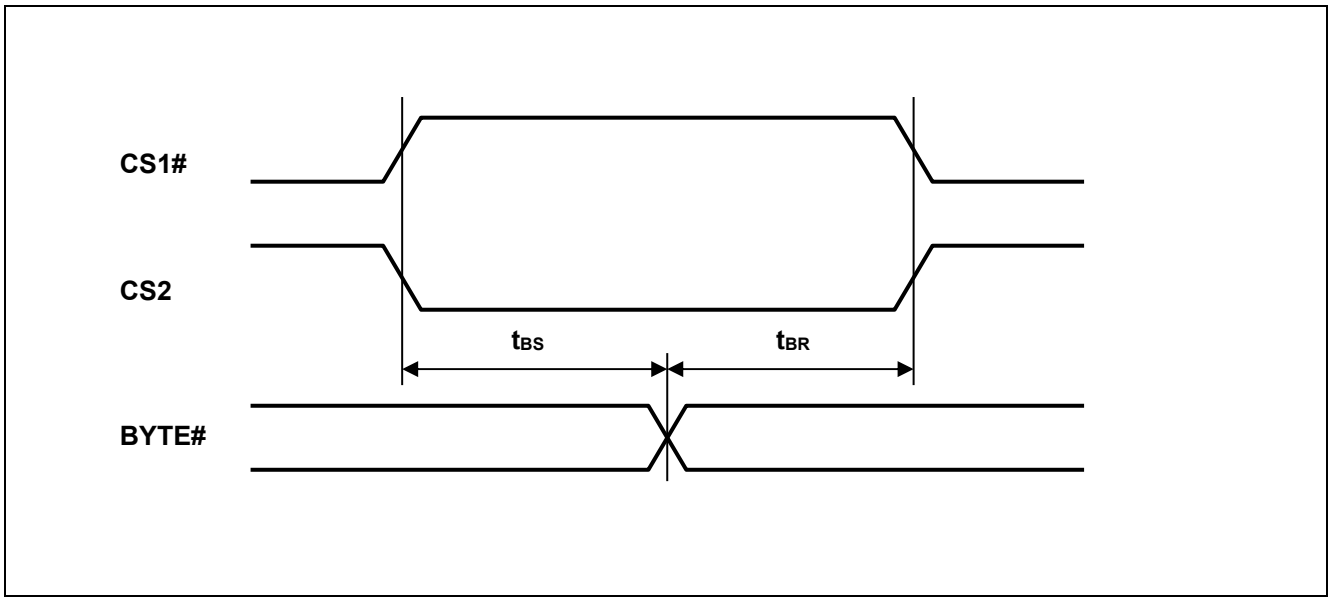
Parameter	Symbol	Min.	Max.	Unit	Note
Write cycle time	t_{WC}	55	—	ns	
Address valid to write end	t_{AW}	35	—	ns	
Chip select to write end	t_{CW}	35	—	ns	
Write pulse width	t_{WP}	35	—	ns	16
LB#,UB# valid to write end	t_{BW}	35	—	ns	
Address setup time to write start	t_{AS}	0	—	ns	
Write recovery time from write end	t_{WR}	0	—	ns	
Data to write time overlap	t_{DW}	25	—	ns	
Data hold from write end	t_{DH}	0	—	ns	
Output enable from write end	t_{OW}	5	—	ns	17
Output disable to output in high-Z	t_{OHZ}	0	18	ns	17,18
Write to output in high-Z	t_{WHZ}	0	18	ns	17,18

Note 16. t_{WP} is the interval between write start and write end.
A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.
A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.
17. This parameter is sampled and not 100% tested.
18. t_{OHZ} and t_{WHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

BYTE# Timing Conditions (BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types)

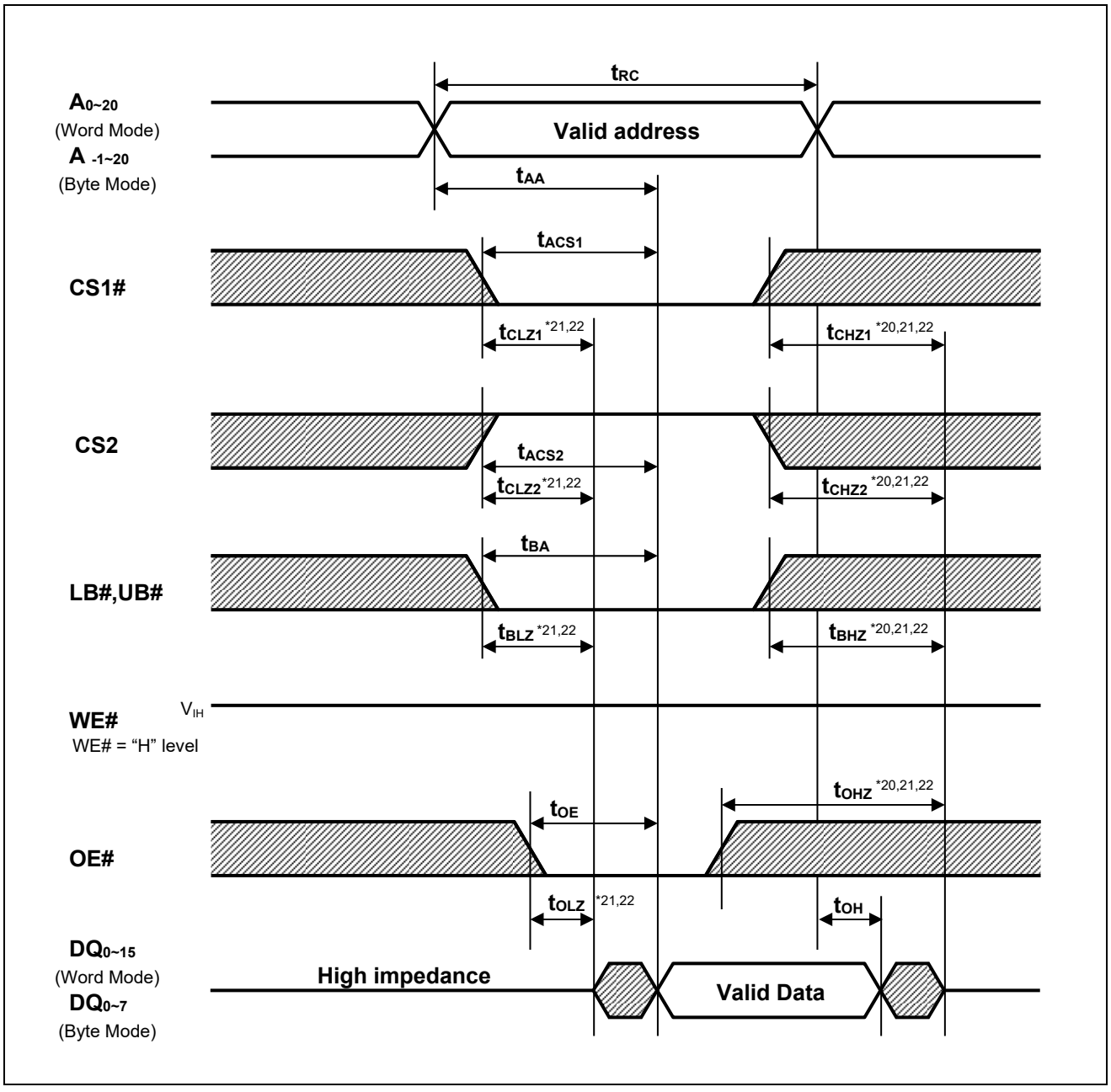
Parameter	Symbol	Min.	Max.	Unit	Note
Byte setup time	t_{BS}	5	-	ms	
Byte recovery time	t_{BR}	5	-	ms	

BYTE# Timing Waveforms



Timing Waveforms

Read Cycle*19



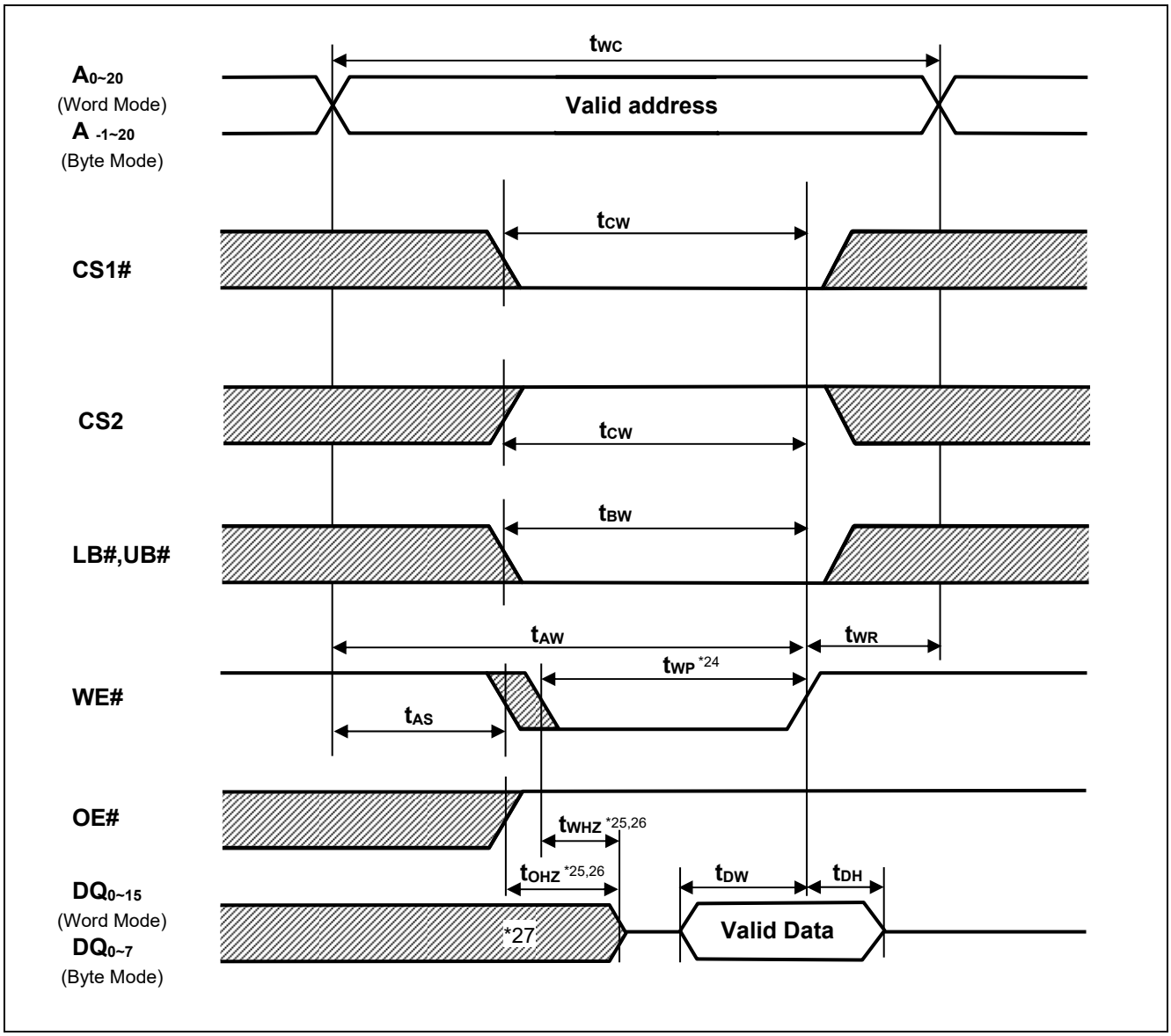
Note 19. BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.
BYTE# ≥ Vcc - 0.2V (Word mode) or BYTE# ≤ 0.2V (Byte mode)

20. t_{CHZ1}, t_{CHZ2}, t_{BHZ} and t_{OHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

21. This parameter is sampled and not 100% tested.

22. At any given temperature and voltage condition, t_{CHZ1} max is less than t_{CLZ1} min, t_{CHZ2} max is less than t_{CLZ2} min, t_{BHZ} max is less than t_{BLZ} min, and t_{OHZ} max is less than t_{OLZ} min, for any device.

Write Cycle (1)[*23] (WE# CLOCK, OE#="H" while writing)



Note 23. BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.
BYTE# ≥ Vcc - 0.2V (Word mode) or BYTE# ≤ 0.2V (Byte mode)

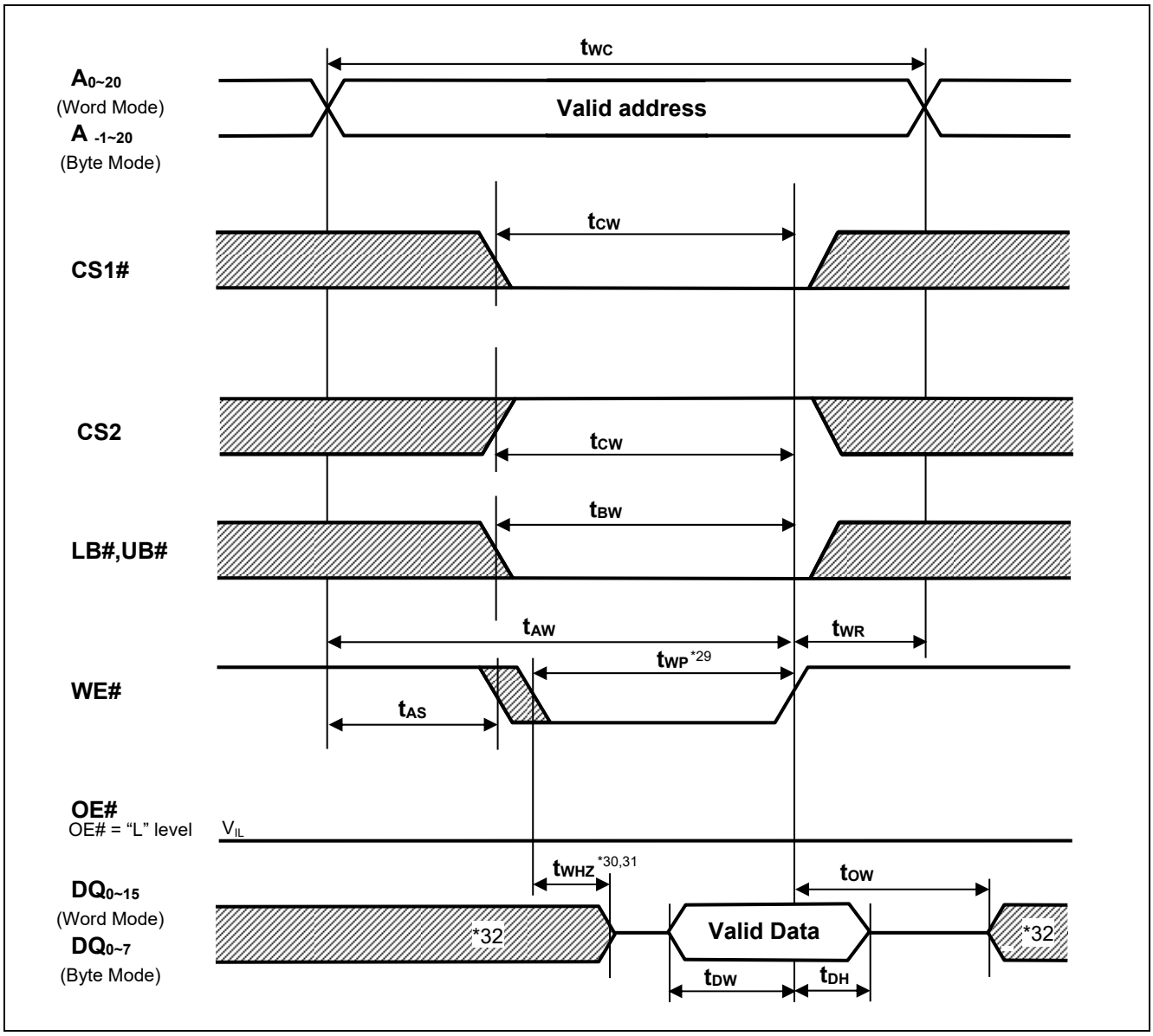
24. t_{WP} is the interval between write start and write end.
A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.
A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

25. t_{OHZ} and t_{WHZ} are defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

26. This parameter is sampled and not 100% tested.

27. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

Write Cycle (2)*28 (WE# CLOCK, OE# Low Fixed)



Note 28. BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.
BYTE# ≥ Vcc - 0.2V (Word mode) or BYTE# ≤ 0.2V (Byte mode)

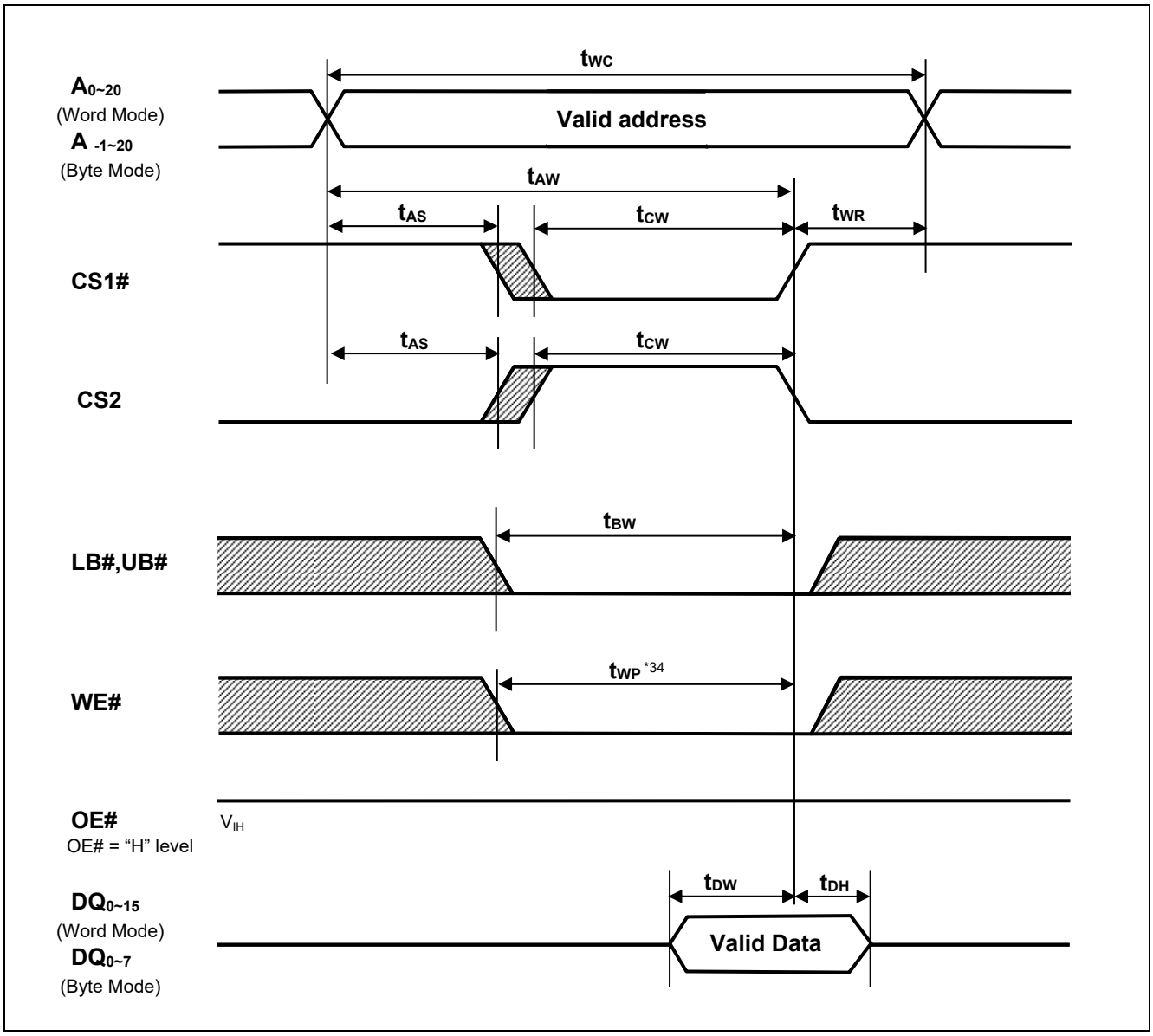
29. t_{WP} is the interval between write start and write end.
A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.
A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

30. t_{WHZ} is defined as the time when the DQ pins enter a high-impedance state and are not referred to the DQ levels.

31. This parameter is sampled and not 100% tested.

32. During this period, DQ pins are in the output state so input signals must not be applied to the DQ pins.

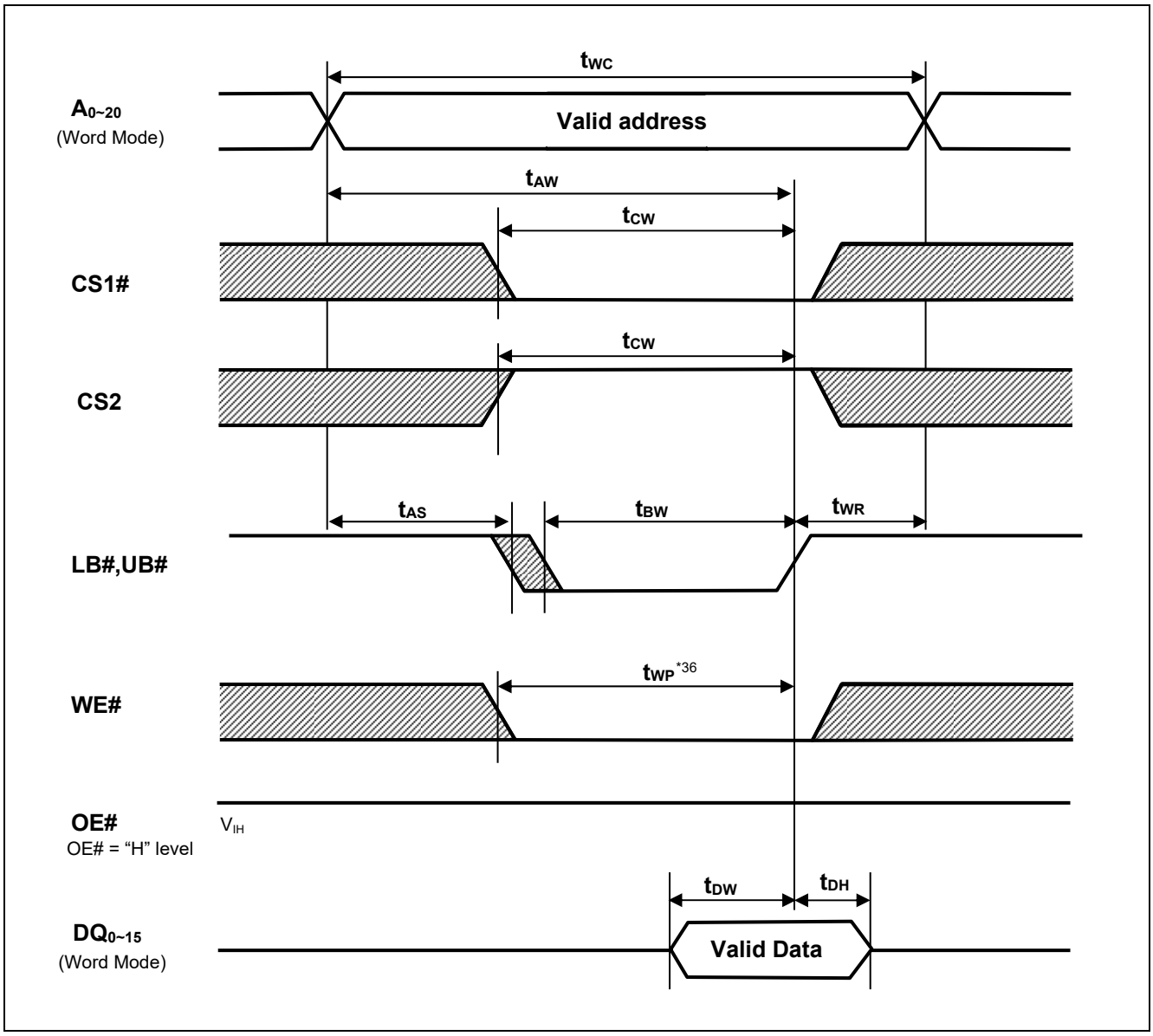
Write Cycle (3)*33 (CS1#, CS2 CLOCK)



Note 33. BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.
BYTE# ≥ Vcc - 0.2V (Word mode) or BYTE# ≤ 0.2V (Byte mode)

34. t_{WP} is the interval between write start and write end.
A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.
A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

Write Cycle (4)[*35] (LB#, UB# CLOCK, Word Mode)



Note 35. BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.
BYTE# ≥ Vcc - 0.2V (Word mode)

36. t_{WP} is the interval between write start and write end.
A write starts when all of (CS1#), (CS2), (WE#) and (one or both of LB# and UB#) become active.
A write is performed during the overlap of a low CS1#, a high CS2, a low WE# and a low LB# or a low UB#.
A write ends when any of (CS1#), (CS2), (WE#) or (one or both of LB# and UB#) becomes inactive.

Low V_{CC} Data Retention Characteristics

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test conditions[*37,38]	
V_{CC} for data retention	V_{DR}	1.5	—	3.6	V	Vin ≥ 0V (1) CS2 ≤ 0.2V or (2) CS1# ≥ V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V or (3) LB# = UB# ≥ V_{CC}-0.2V, CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V	
Data retention current	I_{CCDR}	—	0.6[*39]	4	µA	~+25°C	Vin ≥ 0V (1) CS2 ≤ 0.2V or (2) CS1# ≥ V_{CC}-0.2V, CS2 ≥ V_{CC}-0.2V or (3) LB# = UB# ≥ V_{CC}-0.2V, CS1# ≤ 0.2V, CS2 ≥ V_{CC}-0.2V
		—	1[*40]	6	µA	~+40°C	
		—	4[*41]	17	µA	~+70°C	
		—	8[*42]	24	µA	~+85°C	
Chip deselect time to data retention	t_{CDR}	0	—	—	ns	See retention waveform.	
Operation recovery time	t_R	5	—	—	ms		

Note 37. BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.
BYTE# ≥ Vcc - 0.2V or BYTE# ≤ 0.2V

38. CS2 controls address buffer, WE# buffer, CS1# buffer, OE# buffer, LB# buffer, UB# buffer and DQ buffer.
If CS2 controls data retention mode, Vin levels (address, WE#, CS1#, OE#, LB#, UB#, DQ) can be in the high impedance state. If CS1# controls data retention mode, CS2 must be CS2 ≥ V_{CC}-0.2V or CS2 ≤ 0.2V.
The other inputs levels (address, WE#, OE#, LB#, UB#, DQ) can be in the high-impedance state.

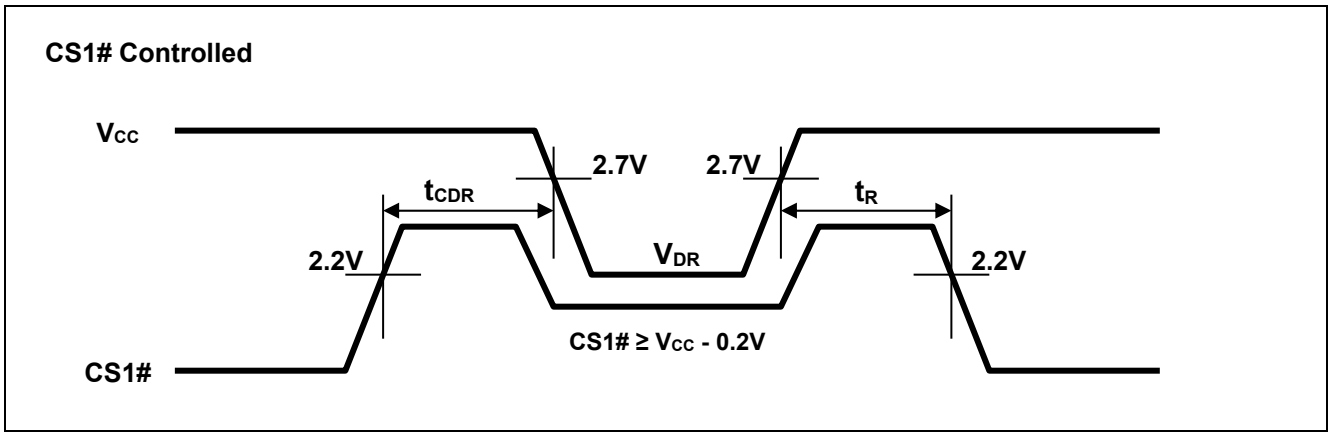
39. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=25ºC), and not 100% tested.

40. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=40ºC), and not 100% tested.

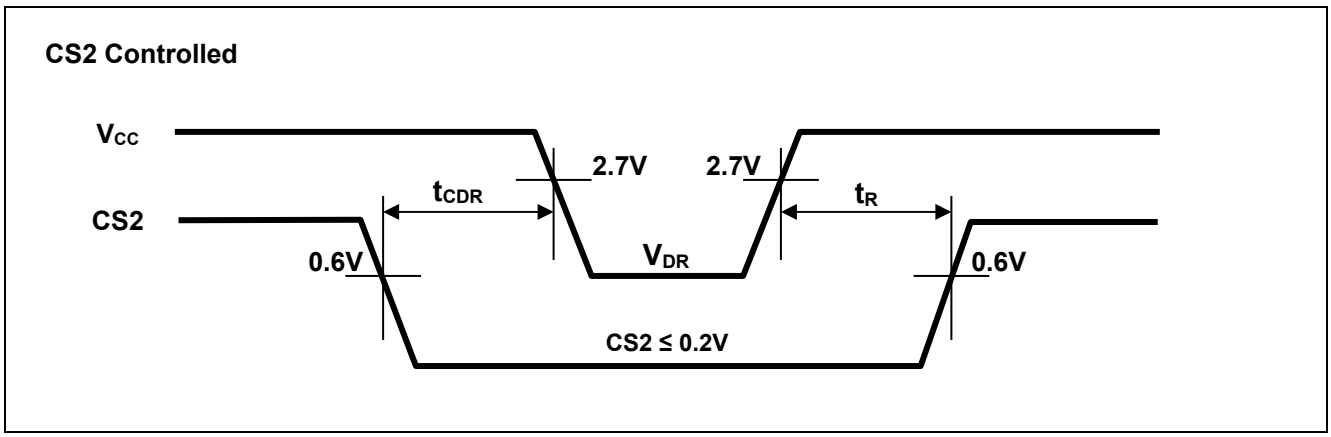
41. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=70ºC), and not 100% tested.

42. Typical parameter indicates the value for the center of distribution at 3.0V (Ta=85ºC), and not 100% tested.

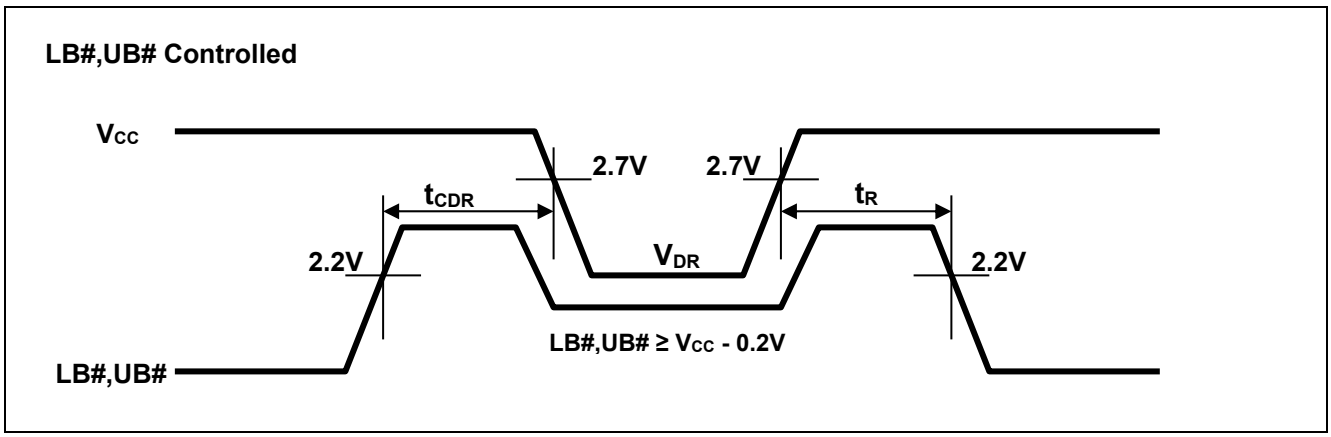
Low Vcc Data Retention Timing Waveforms (CS1# controlled)*43



Low Vcc Data Retention Timing Waveforms (CS2 controlled)*43



Low Vcc Data Retention Timing Waveforms (LB#,UB# controlled, Word Mode)*44



Note 43. BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.
BYTE# ≥ Vcc - 0.2V or BYTE# ≤ 0.2V

44. BYTE# pin supported by only 48pin TSOP (I) and 52pin µTSOP (II) types.
BYTE# ≥ Vcc - 0.2V (Word mode)

Revision History	RMLV3216A Series Data Sheet

Rev.	Date	Description	
		Page	Summary
1.00	2018.12.26	—	First Edition issued

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.
   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note 2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)

RENESAS

SALES OFFICES

Renesas Electronics Corporation

http://www.renesas.com

Refer to "http://www.renesas.com/" for the latest and detailed information.

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

Colophon 7.1

X-ON Electronics

Largest Supplier of Electrical and Electronic Components

Click to view similar products for SRAM ***category:***

Click to view products by Renesas ***manufacturer:***

Other Similar products are found below :

CY6116A-35DMB CY7C1049GN-10VXI GS8161Z36DD-200I GS88237CB-200I RMLV0408EGSB-4S2#AA0 IDT70V5388S166BG IS64WV3216BLL-15CTLA3 IS66WVE4M16ECLL-70BLI PCF8570P K6F2008V2E-LF70000 K6T4008C1B-GB70 CY7C1353S-100AXC AS6C8016-55BIN AS7C164A-15PCN 515712X IDT71V67603S133BG IS62WV51216EBLL-45BLI IS63WV1288DBLL-10HLI IS66WVE2M16ECLL-70BLI IS66WVE4M16EALL-70BLI IS61WV102416DBLL-10TLI CY7C1381KV33-100AXC CY7C1381KVE33-133AXI 8602501XA 5962-3829425MUA 5962-3829430MUA 5962-8866201YA 5962-8866204TA 5962-9062007MXA 5962-9161705MXA GS882Z18CD-150I 8413202RA 5962-8866208YA 5962-8866203YA IS61WV102416DBLL-10BLI IS66WVC2M16ECLL-7010BLI CY7C1380KV33-250AXC AS6C8016-55BINTR GS81284Z18B-250I AS7C34096B-10TIN GS84018CB-200I IS62WV25616EALL-55TLI IS61WV204816BLL-10TLI GS8128418B-167IV CY7C1460KV25-200BZXI CY7C1315KV18-333BZXC CY62157G30-45ZSXI 71V016SA12YG RMLV0416EGBG-4S2#AC0 CY62126EV18LL-70BVXI