

# RNA51951A, B

R03DS0003EJ0400

Rev.4.00

Jul 03, 2012

## Voltage Detecting, System Resetting IC Series

### Description

RNA51951A,B are semiconductor integrated circuits designed for detecting supply voltage and resetting all types of logic circuits such as CPUs.

They include a built-in delay circuit to provide a retardation time (200  $\mu$ s Typ).

They find extensive applications, including battery checking circuit, level detecting circuit and waveform shaping circuit.

### Features

- Few external parts
- Low threshold operating voltage (Supply voltage to keep low-state at low supply voltage): 0.6 V (Typ) at  $R_L = 22 \text{ k}\Omega$
- Wide supply voltage range: 2 V to 17 V
- Wide application range
- Ordering Information

Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)	Surface Treatment
RNA51951AFPH0	SOP-8 pin	PRSP0008DE-C	FP	H (2,500 pcs / Reel)	0 (Ni/Pd/Au)
RNA51951APT0	DIP-8 pin	PRDP0008AF-B	P	T (1,000 pcs / Box)	0 (Ni/Pd/Au)
RNA51951AUPH1	UPAK	PLZZ0004CA-A	UP	H (1,000 pcs / Reel)	1 (Sn-Bi)
RNA51951BFPH0	SOP-8 pin	PRSP0008DE-C	FP	H (2,500 pcs / Reel)	0 (Ni/Pd/Au)
RNA51951BPT0	DIP-8 pin	PRDP0008AF-B	P	T (1,000 pcs / Box)	0 (Ni/Pd/Au)
RNA51951BUPH1	UPAK	PLZZ0004CA-A	UP	H (1,000 pcs / Reel)	1 (Sn-Bi)

### Application

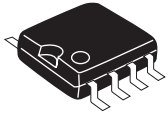
- Reset circuit of Pch, Nch, CMOS, microcomputer, CPU and MCU, Reset of logic circuit, Battery check circuit, switching circuit back-up voltage, level detecting circuit, waveform shaping circuit, delay waveform generating circuit, DC/DC converter, over voltage protection circuit

### Recommended Operating Condition

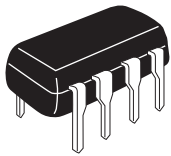
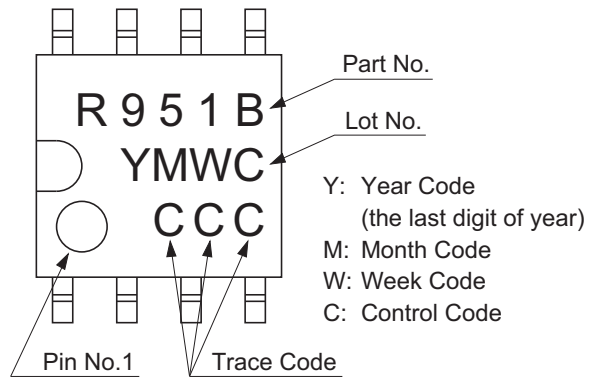
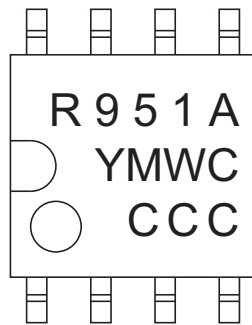
- Supply voltage range: 2 V to 17 V

Outline and Article Indication

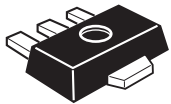
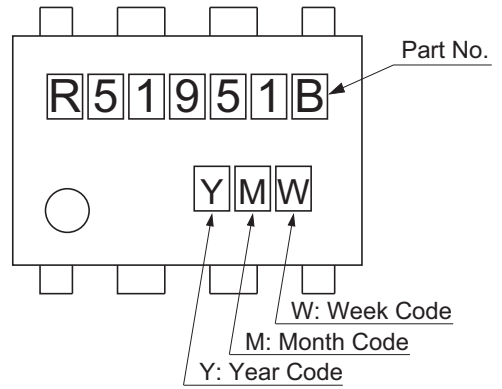
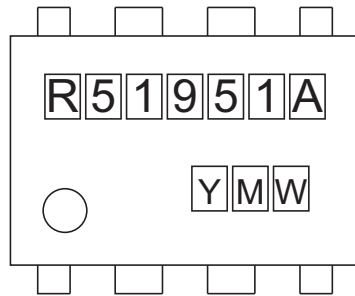
• RNA51951A, B



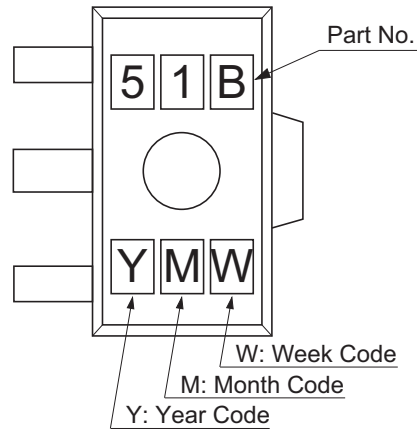
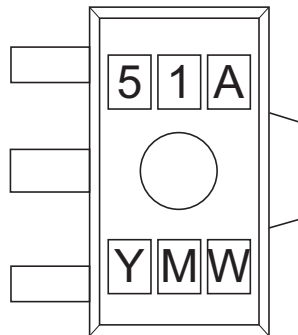
SOP-8



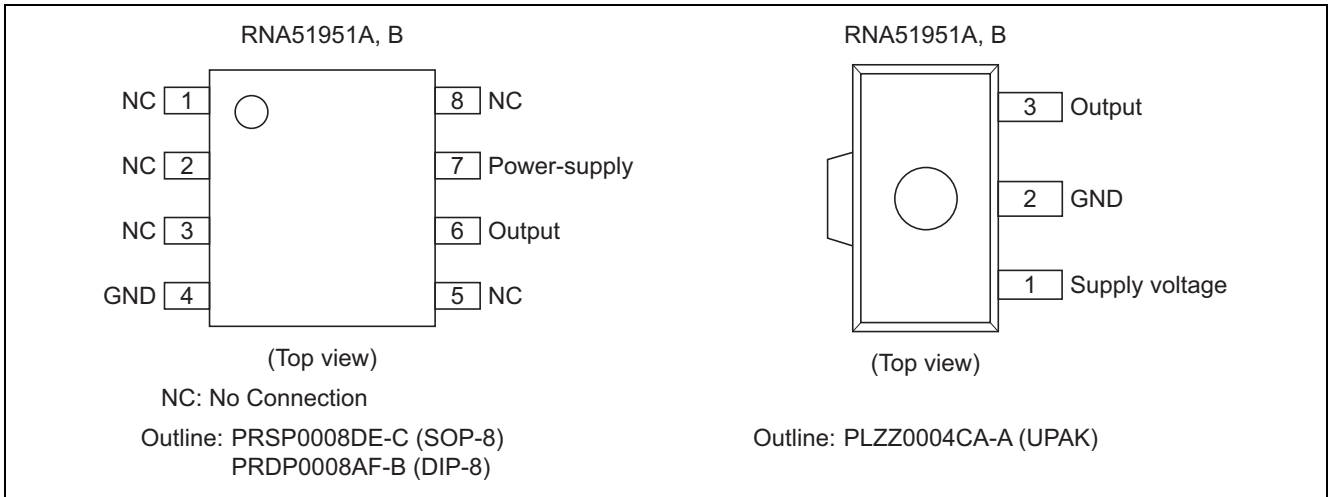
DIP-8



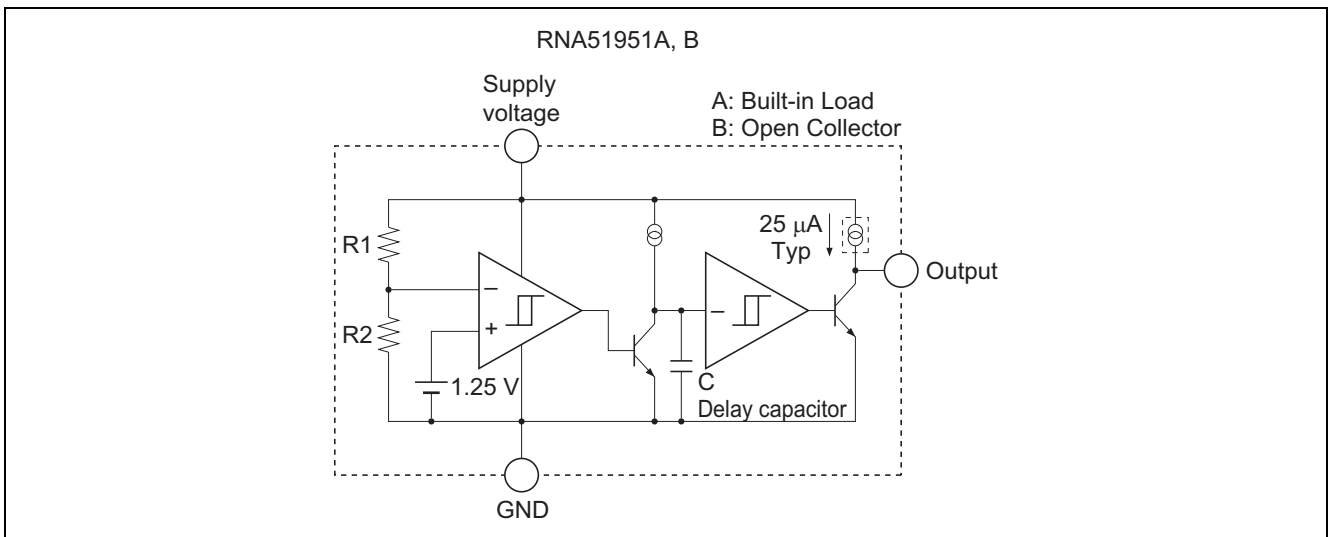
UPAK



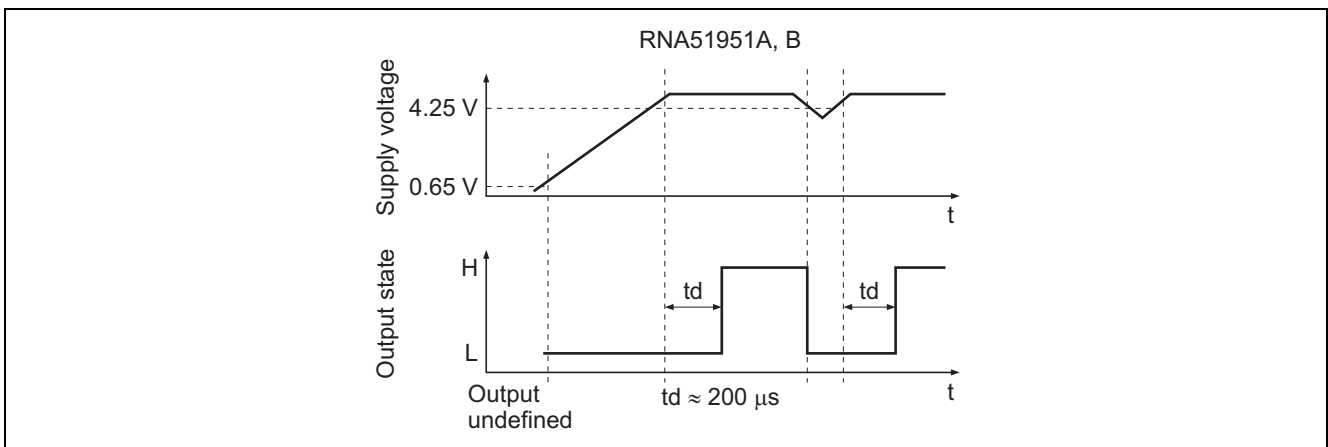
### Pin Arrangement



### Block Diagram



### Operating Waveform



## Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

Item	Symbol	Ratings	Unit	Conditions
Supply voltage	V <sub>CC</sub>	18	V	
Output sink current	I <sub>sink</sub>	6	mA	
Output voltage	V <sub>O</sub>	V <sub>CC</sub>	V	Type A (output with constant current load)
		18		Type B (open collector output)
Power dissipation	P <sub>d</sub>	400	mW	8-pin SOP (PRSP0008DE-C)
		570		8-pin DIP (PRDP0008AF-B)
		640 * <sup>1</sup>		UPAK (PLZZ0004CA-A)
Thermal derating	K <sub>θ</sub>	4.4	mW/°C	8-pin SOP (PRSP0008DE-C)
		8.3		8-pin DIP (PRDP0008AF-B)
		6.4		UPAK (PLZZ0004CA-A)
Operating temperature	T <sub>opr</sub>	-40 to +85	°C	
Storage temperature	T <sub>stg</sub>	-55 to +125	°C	

Note: 1. 15 mm × 25 mm × 0.7 mm alumina ceramic board, Ta ≤ 25°C. If Ta > 25°C, derate by 6.4 mW/°C.

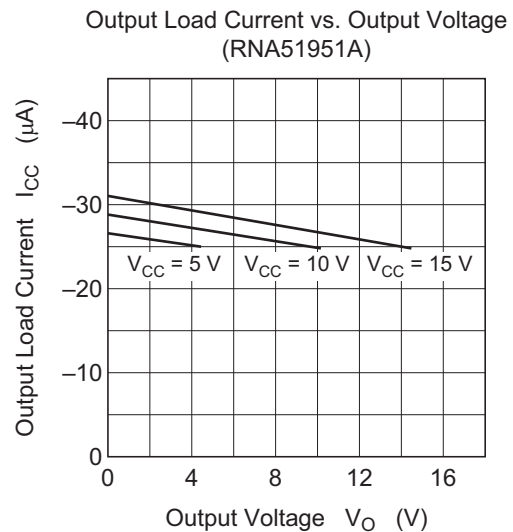
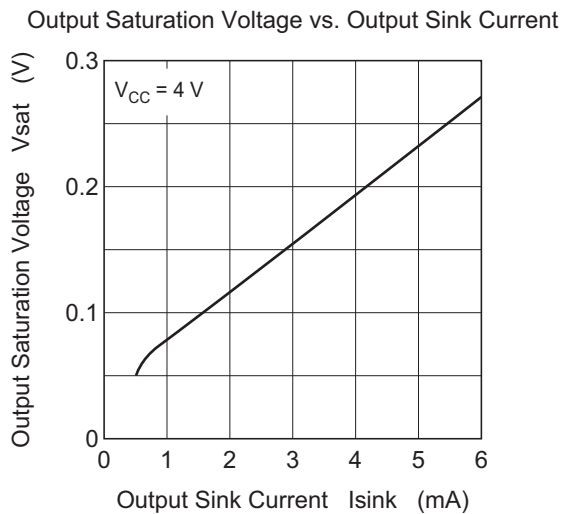
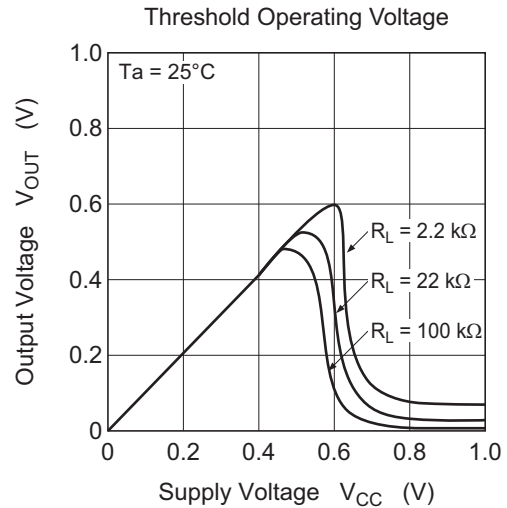
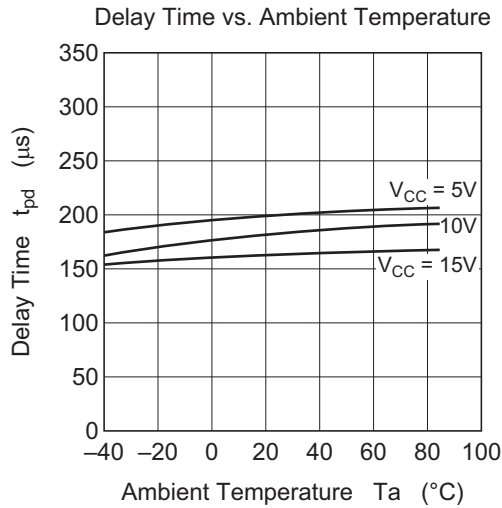
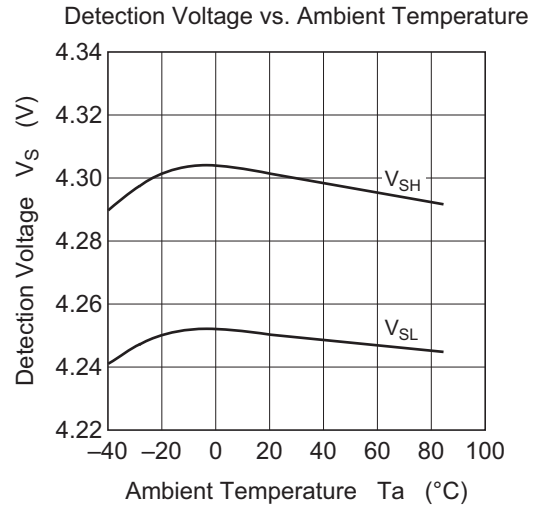
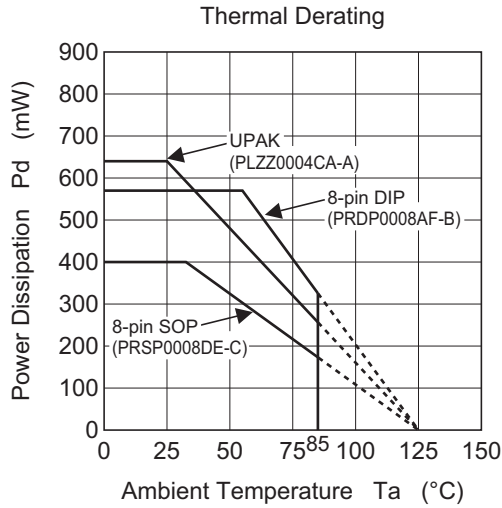
## Electrical Characteristics

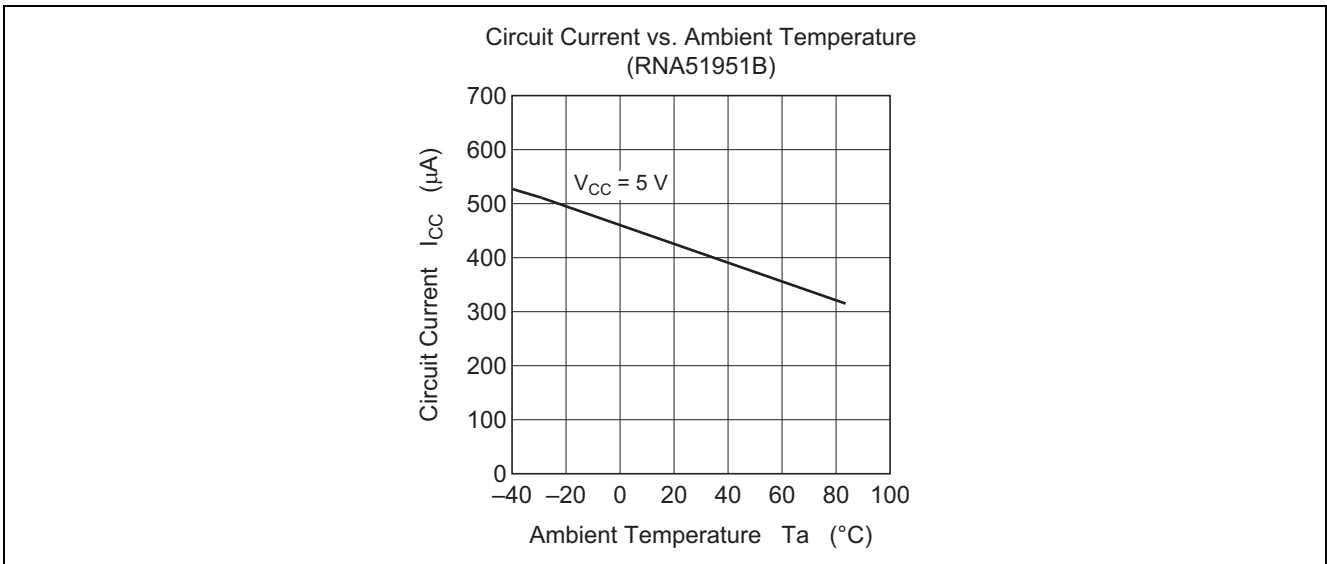
(Ta = 25°C, unless otherwise noted)

- “L” reset type

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Detecting voltage	V <sub>S</sub>	4.05	4.25	4.45	V	
Hysteresis voltage	ΔV <sub>S</sub>	30	50	80	mV	
Detecting voltage temperature coefficient	V <sub>S</sub> /ΔT	—	0.01	—	%/°C	
Circuit current	I <sub>CC</sub>	—	450	680	μA	Type A, V <sub>CC</sub> = 5V
		—	420	630		Type B, V <sub>CC</sub> = 5V
Delay time	t <sub>pd</sub>	80	200	500	μs	
Output saturation voltage	V <sub>sat</sub>	—	0.2	0.4	V	V <sub>CC</sub> = 4V, I <sub>sink</sub> = 4mA
Threshold operating voltage	V <sub>OPL</sub>	—	0.67	0.8	V	R <sub>L</sub> = 2.2kΩ, V <sub>sat</sub> ≤ 0.4V
		—	0.55	0.7		R <sub>L</sub> = 100kΩ, V <sub>sat</sub> ≤ 0.4V
Output leakage current	I <sub>OH</sub>	—	—	30	nA	Type B
Output load current	I <sub>OC</sub>	-40	-25	-17	μA	Type A, V <sub>CC</sub> = 5V, V <sub>O</sub> = 1/2 × V <sub>CC</sub>
Output high voltage	V <sub>OH</sub>	V <sub>CC</sub> -0.2	V <sub>CC</sub> -0.06	—	V	Type A

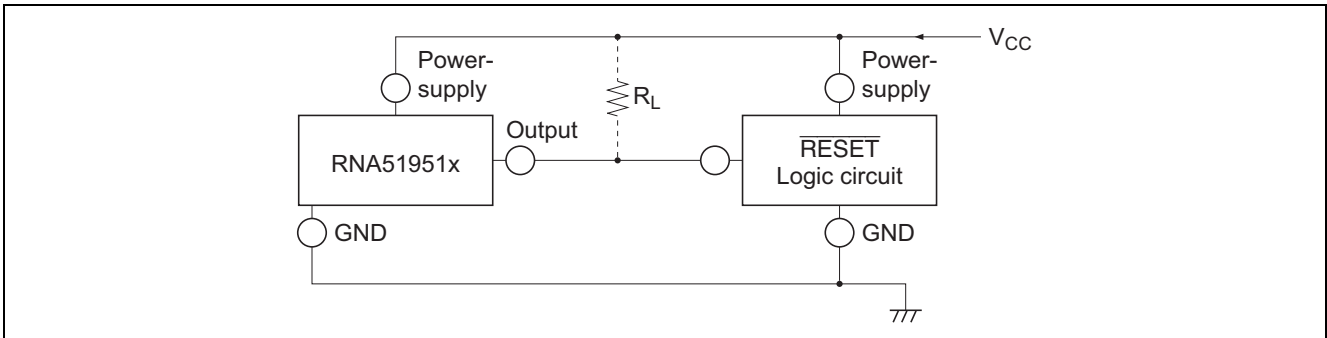
Typical Characteristics





### Example of Application Circuit

#### Reset Circuit of RNA51951



**Figure 1 Reset Circuit of RNA51951**

- Notes:
1. Delay time must be longer than 200 µs, RNA51953, RNA51957, and RNA51958 are used.
  2. If the RNA5195xx and the logic circuit share a common power source, type A (built-in load type) can be used whether a pull-up resistor is included in the logic circuit or not.
  3. The logic circuit preferably should not have a pull-down resistor, but if one is present, add load resistor  $R_L$  to overcome the pull-down resistor.
  4. When a negative supply voltage is used, the supply voltage side of RNA5195xx and the GND side are connected to negative supply voltage respectively.

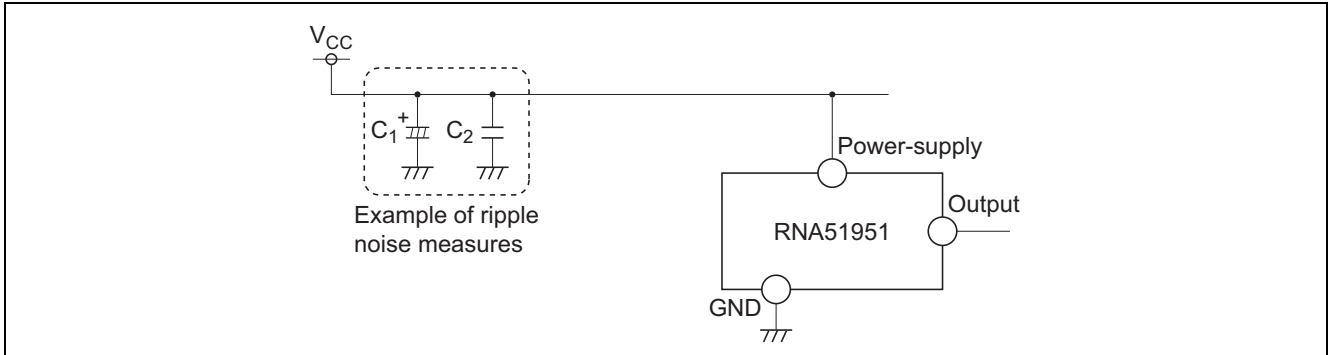
## Notice for use

### About the Power Supply Line

#### 1. About bypass capacitor

Because the ripple and the spike of the high frequency noise and the low frequency are superimposed to the power supply line, it is necessary to remove these.

Therefore, please install  $C_1$  and  $C_2$  for the low frequency and for the high frequency between the power supply line and the GND line as shown in following figure 2.

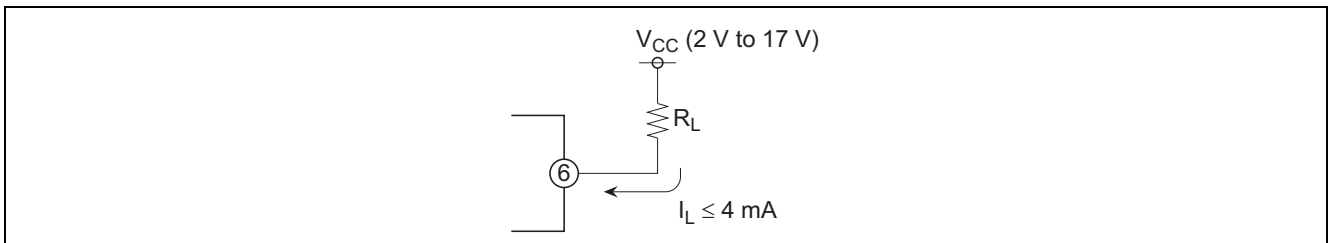


**Figure 2 Example of Ripple Noise Measures**

### Setting of Output Load Resistance (RNA51951B)

High level output voltage can be set without depending on the power-supply voltage because the output terminal is an open collector type. However, please guard the following notes.

1. Please set it in value (2 V to 17 V) within the range of the power-supply voltage recommendation. Moreover, please never impress the voltage of maximum ratings 18 V or more even momentarily either.
2. Please set output load resistance (pull-up resistance)  $R_L$  so that the output current (output inflow current  $I_L$ ) at L level may become 4 mA or less. Moreover, please never exceed absolute maximum rating (6 mA).



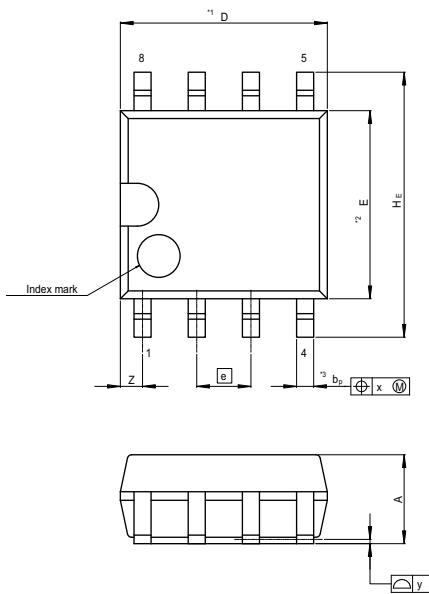
**Figure 3 Output Load Resistance  $R_L$**

### Others

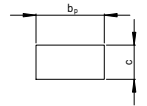
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[http://www.renesas.com/products/common\\_info/reliability/index.jsp](http://www.renesas.com/products/common_info/reliability/index.jsp)
2. Additionally, please inquire of our company when there is an uncertain point on use.

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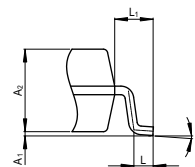
JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-SOP8-4.4x4.85-1.27	PRSP0008DE-C	—	0.1g



NOTE)  
 1. DIMENSIONS\*\*1 (Nom)\*\*AND\*\*2\*  
 DO NOT INCLUDE MOLD FLASH.  
 2. DIMENSION\*\*3\*DOES NOT  
 INCLUDE TRIM OFFSET.



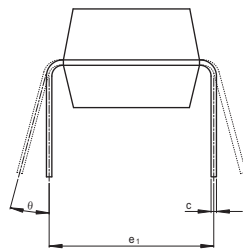
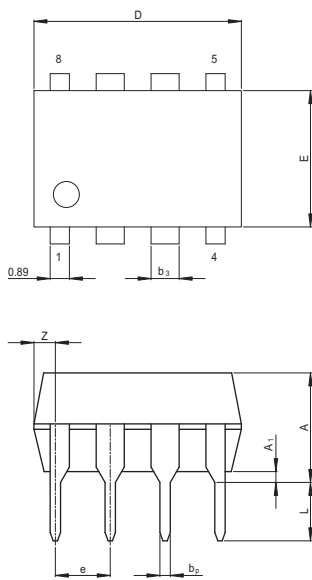
Terminal cross section  
( Ni/Pd/Au plating )



Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	4.65	4.85	5.05
E	4.2	4.4	4.6
A <sub>2</sub>	—	1.85	—
A <sub>1</sub>	0.00	0.1	0.20
A	—	—	2.03
b <sub>p</sub>	0.34	0.4	0.46
b <sub>1</sub>	—	—	—
c	0.15	0.20	0.25
c <sub>1</sub>	—	—	—
θ	0°	—	8°
H <sub>E</sub>	5.7	6.2	6.5
⊕	1.12	1.27	1.42
x	—	—	0.12
y	—	—	0.10
Z	—	—	0.75
L	0.25	0.45	0.65
L <sub>1</sub>	—	0.90	—

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-DIP8-6.3x9.6-2.54	PRDP0008AF-B	DP-8FV	0.54g



( Ni/Pd/Au plating )

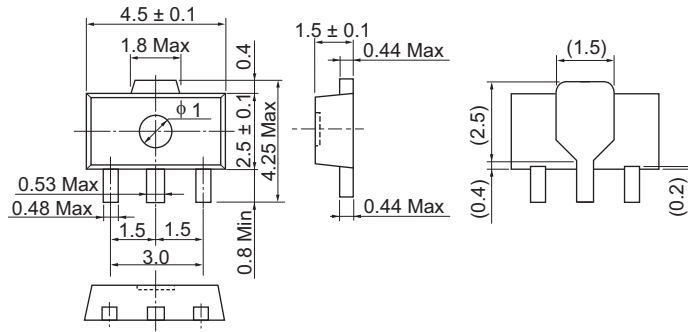
Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
e <sub>1</sub>	—	7.62	—
D	—	9.60	10.6
E	—	6.30	7.4
A	—	—	5.06
A <sub>1</sub>	0.5	—	—
b <sub>p</sub>	0.40	0.48	0.56
b <sub>3</sub>	—	1.30	—
c	0.19	0.25	0.31
θ	0°	—	15°
e	2.29	2.54	2.79
Z	—	—	1.27
L	2.54	—	—



**RNA51951A, B**

Package Name	JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
UPAK	SC-62	PLZZ0004CA-A	UPAK / UPAKV	0.050g

Unit: mm



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