

RTKA214023DE0000BU

The RTKA214023DE0000BU evaluation board provides a simple platform to evaluate the [RAA214023](#). It contains all the important circuitry needed to characterize critical performance parameters.

The RAA214023 is a low noise, high PSRR, low dropout voltage regulator. It accepts a input voltage range of 2.7V to 5.5V, and the output voltage can be programmed from 0.8V to 3.95V by means of voltage setting pins. To extend the output voltage range up to 5.5V- $V_{DROPOUT}$, an external resistor divider feedback network can be used. The device can source a load current of up to 2A and has an output voltage accuracy of $\pm 1.75\%$ over line, load, and temperature.

Features

- Input Voltage Range: 2.7V to 5.5V
- Voltage Set Pins easily programmed with JP1: 0.8V to 3.95V
- Switch between Voltage Set pins or Eternal Resistor Divider using jumper JP_FB
- Convenient shutdown mode function using Jumper JP_EN
- Power good (PG) indication test point

Specifications

This board has been optimized for the following operating conditions:

- V_{IN} range from 2.7V to 5.5V
- V_{OUT} adjustable from 0.8V to 3.95V with Voltage Set Pins
- V_{OUT} adjustable from 0.8V up to 5.5V - $V_{DROPOUT}$ with External Resistor Divider
- Low dropout: 420mV at 2A and $V_{IN} = 3.3V$ (typical)
- High PSRR for $V_{HEADROOM} = 1.7V$:
 - 100kHz: 62dB at 2A and 85dB at 500mA
 - 1MHz: 51dB at 2A and 60dB at 500mA

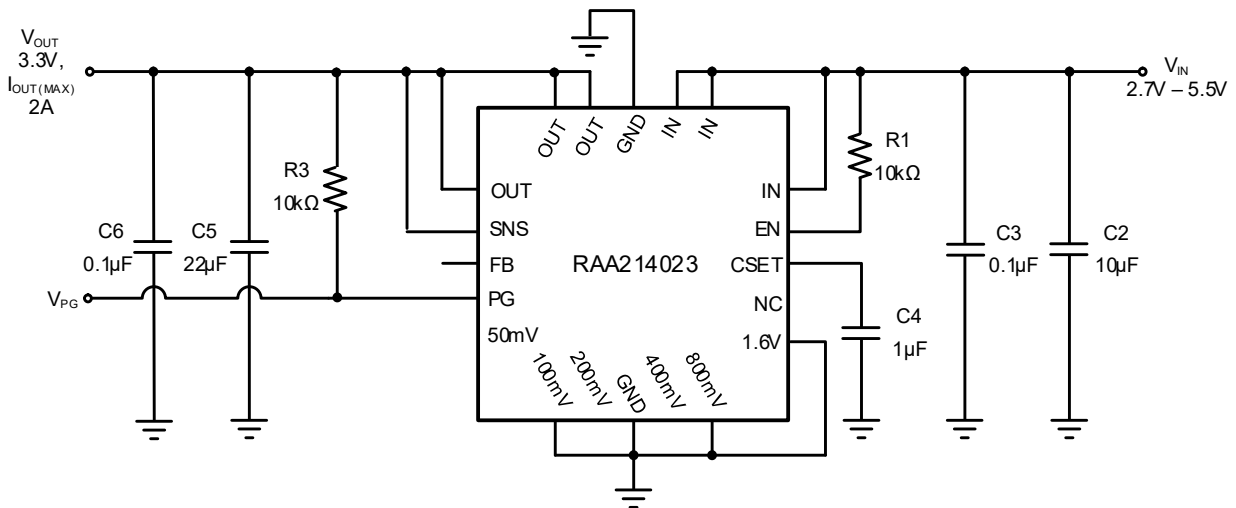


Figure 1. Block Diagram

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1. Functional Description

The RTKA214023DE0000BU evaluation board provides a simple platform to evaluate the features of the RAA214023 low-noise, high PSRR LDO and help characterize important critical performance parameters. The evaluation board is functionally optimized to allow efficient operation up to the maximum output current of 2A.

1.1 Setting the Output Voltage

The output voltage can be programmed by means of the PCB layout or with traditional feedback resistors. To switch between the two configurations, the 3-pin JP_FB jumper is used.

1.1.1 Voltage Set Pins

The evaluation board can be configured to use the Voltage Set pins by shorting the device SNS pin to OUT using the JP_FB jumper as shown in Figure 2.



Figure 2. RTKA214023DE0010BU JP_FB Jumper for Voltage Set Pin Configuration

The voltage set pins are labeled 0.05V, 0.1V, 0.2V, 0.4V, 0.8V, and 1.6V on the PCB Board. Grounding these pins adds the voltages assigned to each grounded pin to the reference voltage (0.8V) as expressed in Equation 1. These pins can easily be grounded on the evaluation board using the J1 jumper. In this configuration, the output voltage can be programmed from 0.8V to 3.95V in steps of 50mV.

(EQ. 1) $V_{OUT} = 0.8V + \Sigma(\text{Grounded Voltage Set Pins})$

For example, to set $V_{OUT(TARGET)}$ to 3.3V ground the 0.1V, 0.8V, and 1.6V pins. The sum of these three pins (2.5V) added to the 0.8V reference gives the expected 3.3V for the output. Table 1 is a full list of all the possible $V_{OUT(TARGET)}$ and the corresponding Voltage Set pins to short to ground.

Table 1. User Configurable Output Voltage Settings

V_{OUT} (V)	50mV	100mV	200mV	400mV	800mV	1.6V	V_{OUT} (V)	50mV	100mV	200mV	400mV	800mV	1.6V
0.80	Open	Open	Open	Open	Open	Open	2.40	Open	Open	Open	Open	Open	GND
0.85	GND	Open	Open	Open	Open	Open	2.45	GND	Open	Open	Open	Open	GND
0.90	Open	GND	Open	Open	Open	Open	2.50	Open	GND	Open	Open	Open	GND
0.95	GND	GND	Open	Open	Open	Open	2.55	GND	GND	Open	Open	Open	GND

Table 1. User Configurable Output Voltage Settings (Cont.)

V _{OUT} (V)	50mV	100mV	200mV	400mV	800mV	1.6V	V _{OUT} (V)	50mV	100mV	200mV	400mV	800mV	1.6V
1.00	Open	Open	GND	Open	Open	Open	2.60	Open	Open	GND	Open	Open	GND
1.05	GND	Open	GND	Open	Open	Open	2.65	GND	Open	GND	Open	Open	GND
1.10	Open	GND	GND	Open	Open	Open	2.70	Open	GND	GND	Open	Open	GND
1.15	GND	GND	GND	Open	Open	Open	2.75	GND	GND	GND	Open	Open	GND
1.20	Open	Open	Open	GND	Open	Open	2.80	Open	Open	Open	GND	Open	GND
1.25	GND	Open	Open	GND	Open	Open	2.85	GND	Open	Open	GND	Open	GND
1.30	Open	GND	Open	GND	Open	Open	2.90	Open	GND	Open	GND	Open	GND
1.35	GND	GND	Open	GND	Open	Open	2.95	GND	GND	Open	GND	Open	GND
1.40	Open	Open	GND	GND	Open	Open	3.00	Open	Open	GND	GND	Open	GND
1.45	GND	Open	GND	GND	Open	Open	3.05	GND	Open	GND	GND	Open	GND
1.50	Open	GND	GND	GND	Open	Open	3.10	Open	GND	GND	GND	Open	GND
1.55	GND	GND	GND	GND	Open	Open	3.15	GND	GND	GND	GND	Open	GND
1.60	Open	Open	Open	Open	GND	Open	3.20	Open	Open	Open	Open	GND	GND
1.65	GND	Open	Open	Open	GND	Open	3.25	GND	Open	Open	Open	GND	GND
1.70	Open	GND	Open	Open	GND	Open	3.30	Open	GND	Open	Open	GND	GND
1.75	GND	GND	Open	Open	GND	Open	3.35	GND	GND	Open	Open	GND	GND
1.80	Open	Open	GND	Open	GND	Open	3.40	Open	Open	GND	Open	GND	GND
1.85	GND	Open	GND	Open	GND	Open	3.45	GND	Open	GND	Open	GND	GND
1.90	Open	GND	GND	Open	GND	Open	3.50	Open	GND	GND	Open	GND	GND
1.95	GND	GND	GND	Open	GND	Open	3.55	GND	GND	GND	Open	GND	GND
2.00	Open	Open	Open	GND	GND	Open	3.60	Open	Open	Open	GND	GND	GND
2.05	GND	Open	Open	GND	GND	Open	3.65	GND	Open	Open	GND	GND	GND
2.10	Open	GND	Open	GND	GND	Open	3.70	Open	GND	Open	GND	GND	GND
2.15	GND	GND	Open	GND	GND	Open	3.75	GND	GND	Open	GND	GND	GND
2.20	Open	Open	GND	GND	GND	Open	3.80	Open	Open	GND	GND	GND	GND
2.25	GND	Open	GND	GND	GND	Open	3.85	GND	Open	GND	GND	GND	GND
2.30	Open	GND	GND	GND	GND	Open	3.90	Open	GND	GND	GND	GND	GND
2.35	GND	GND	GND	GND	GND	Open	3.95	GND	GND	GND	GND	GND	GND

1.1.2 External Feedback Resistors

To evaluate the RAA214023 in applications where V_{OUT} is greater than 3.95V, an external feedback resistor divider, R4 and R5 in [Figure 3](#), can be used.

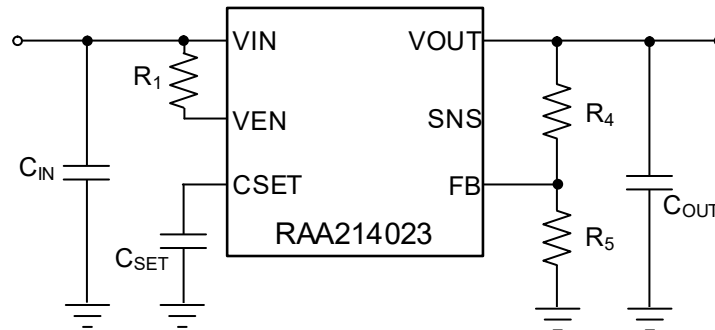


Figure 3. RAA214023 External Feedback Resistors Schematic

To use this configuration, the JP_FB jumper should be connected to short the top of R4 with OUT as shown in [Figure 4](#). R4 and R5 need to be populated with resistors. In this configuration, V_{OUT} can be set from 0.8V up to $5.5V - V_{DROPOUT}$.



Figure 4. RTKA214023DE0000BU JP_FB Jumper for External Feedback Configuration

For a required output voltage, R4 can be easily calculated by setting R5 to 10kΩ and solving for [Equation 2](#) where $V_{OUT(TARGET)}$ is the required output voltage.

$$(EQ. 2) \quad R_4 = R_5 \times \left(\frac{V_{OUT(TARGET)}}{0.8V} - 1 \right)$$

There might not always be a resistor that is exactly the calculated R4 value, but in most cases the closest resistor value commercially available can be used and gives ±1% or better accuracy. Based on the actual resistor values commercially available, the actual output voltage can be calculated with [Equation 3](#). Then, the output voltage percent error can be calculated using [Equation 4](#) to decide if the accuracy meets the application design.

Note: $V_{OUT(ACTUAL)}$ is the V_{OUT} value calculated in [Equation 3](#).

$$(EQ. 3) \quad V_{OUT} = 0.8V \times \left(1 + \frac{R_4}{R_5} \right)$$

$$(EQ. 4) \quad \text{Error}(\%) = \frac{V_{\text{OUT(ACTUAL)}} - V_{\text{OUT(TARGET)}}}{V_{\text{OUT(ACTUAL)}}} \times 100$$

For 0.1% or better accuracy, this method does not give the required accuracy for some $V_{\text{OUT(TARGET)}}$. To remedy this, increase R_5 to the next highest resistor value that is commercially available and calculate for R_4 with Equation 1. Next, verify that the calculated R_4 resistor value is commercially available and meets the required output accuracy. Repeat as needed. Table 2 provides the feedback resistor values to obtain some common voltage rails using this method. These values give a $\pm 0.1\%$ or better nominal voltage accuracy.

Table 2. Recommended R_4 and R_5 Resistor Values for Common Voltage Rails

$V_{\text{OUT(TARGET)}} (V)$	$R_4 (k\Omega)$	$R_5 (k\Omega)$	$V_{\text{OUT}} \text{ Error} (\%)$
1	2.55	10.2	0.0
1.2	5.9	11.8	0.0
1.5	10.5	12	0.0
1.8	15	12	0.0
1.9	15.8	11.5	-0.05
2.5	25.5	12	0.0
3	31.6	11.5	-0.06
3.3	75	24	0.0
4.2	51	12	0.0
4.5	74.1	16	0.1
5	105	20	0.0

1.2 Setting Noise Performance

For low-noise applications, a 1 μ F CSET (C4) capacitor is optimal. Larger capacitor values can be used with little benefit in lowering the internally generated output voltage noise and PSRR for frequencies above 10Hz. C7 is a spot for a feed-forward capacitor and is not populated. Using a feed-forward capacitor does not improve the already low noise and high PSRR of the RAA214023 but is useful to test pin-to-pin compatible competitor LDOs, which do require feed-forward capacitance to achieve the similar noise and PSRR performance on the same EVB.

1.3 Enabling and Disabling the Device

R_1 is a 10k Ω pull-up resistor that ties the device EN pin to VIN. To ENABLE the device, remove the JPP_EN jumper. To DISABLE the device connect JP_EN jumper.

1.4 Quick Start Guide

1.4.1 Voltage Set Pins configuration

1. Verify Jumper JP_EN is not in the circuit. The 10kΩ pull-up R1 resistor provides a logic HIGH that enables the LDO.
2. Use the JP_FB jumper to short the SNS pin to OUT.
3. Use a jumper to short the required voltage set pins to ground to obtain the required V_{OUT} .
4. Connect the input supply to VIN and GND_IN.
5. Connect the load to OUT and GND_OUT.
6. Observe the output voltage.

1.4.2 External Resistor Divider

1. Verify Jumper JP_EN is not in the circuit. The 10kΩ pull-up R1 resistor provides a logic HIGH that enables the LDO.
2. Use the JP_FB jumper to connect the top of R4 with OUT.
3. Populate the R4 and R5 feedback resistor divider for the required V_{OUT} .
4. Connect the input supply to VIN and GND_IN.
5. Connect the load to OUT and GND_OUT.
6. Observe the output voltage.

2. Board Design

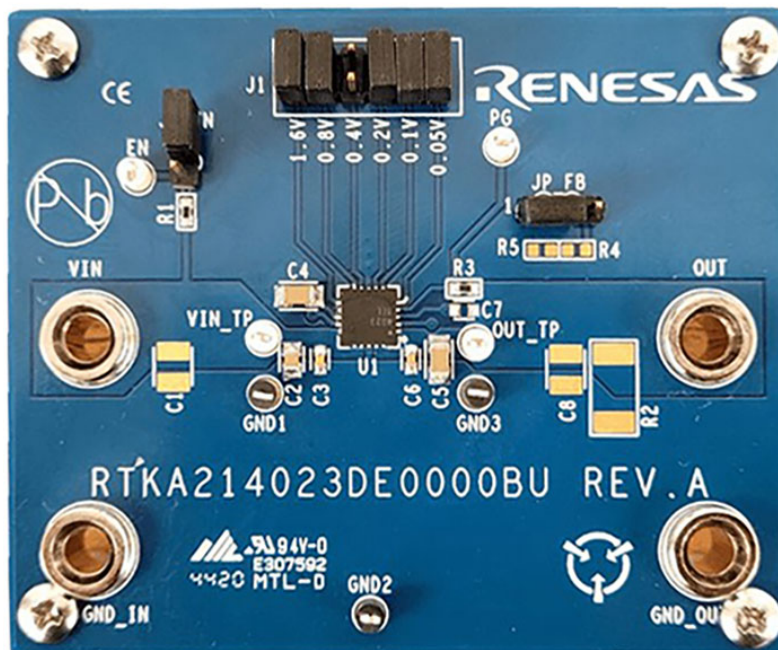


Figure 5. RTKA214023DE0000BU Evaluation Board

2.1 Layout Guidelines

A good PCB layout is important to achieve expected performance. Consideration should be taken when placing the components and routing the trace to minimize the ground impedance, and keep the parasitic inductance low. The input and output capacitors should have a good ground connection and be placed as close to the IC as possible. The trace for FB must be away from noisy planes and traces.

The large 2.05mm x 2.05mm thermal pad under the 5mm x 5mm RAA214023 is connected to a large ground copper plane on the bottom layer for effective thermal dissipation. RTKA214023DE0000BU Evaluation Board

2.2 Schematic Drawing

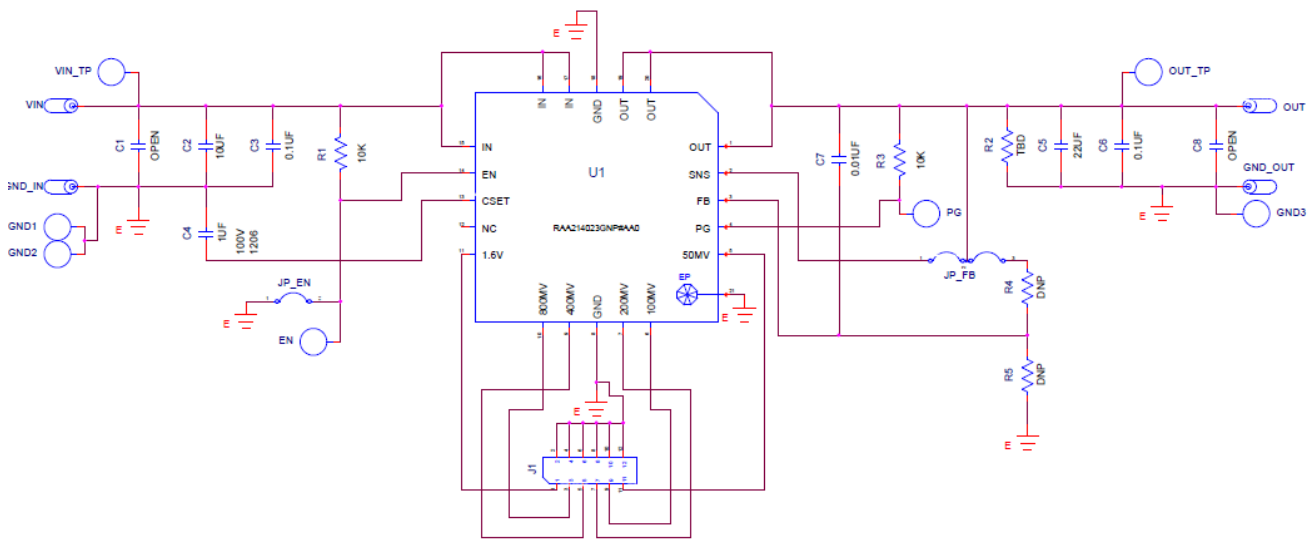


Figure 6. RTKA214023DE0000BU Schematic

2.3 Bill of Materials

Qty	Reference Designator	Description	Mfr	Manufacturer Part Number
2	C2	CAP-AEC-Q200, SMD, 0805, 10µF, 10V, 10%, X7R, ROHS	Murata	GCJ21BR71A106KE01L
2	C5	CAP, SMD, 1206, 22µF, 10V, 10%, X7R, ROHS	Murata	GRM31CR71A226KE15L
1	C7	CAP, SMD, 0603, DNP	Generic	Various
4	C3, C6	CAP, SMD, 0603, 0.1µF, 16V, 10%, X7R, ROHS	Generic	Various
2	C4	CAP, SMD, 1206, 1µF, 100V, 10%, X7R, ROHS	Generic	Various
1	OUT, VIN, GND_IN, GND_OU	CONN-JACK, STD BANANA, SDRLESS, NICKEL/BRASS, 0.350inch, ROHS	Keystone	575-8
1	J1	CONN-HEADER, 2x6, BRKAWY-2x36, 2.54mm, ROHS	BERG/FCI	67996-272HLF
2	JP_FB	CONN-HEADER, 1x3, BREAKAWY 1x36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
1	JP_EN	CONN-HEADER, 1X2, RETENTIVE, 2.54mm, 0.230x 0.120, ROHS	BERG/FCI	69190-202HLF
2	R1, R3	RES, SMD, 0603, 10k, 1/10W, 1%, TF, ROHS	Generic	Various
1	R2	100k, 1%, 1/16W, 0603, Thick Film Chip Resistor	Generic	Various
1	U1	RAA214023, IC-2A LOW NOISE LDO, 20P, QFN, 5x5, ROHS	Renesas	RAA214023

2.4 Board Layout

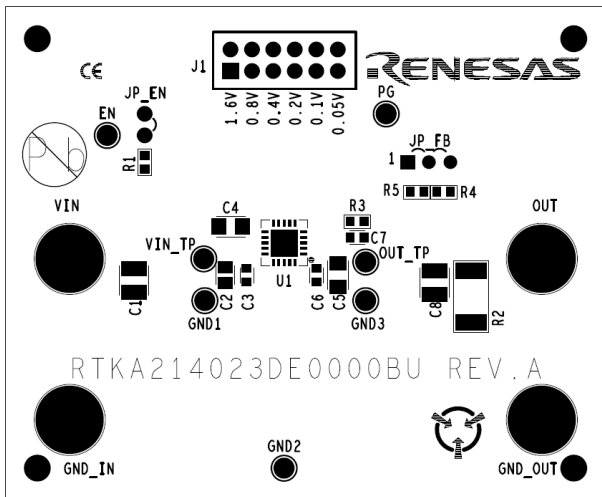


Figure 7. Top Layer Silk Screen

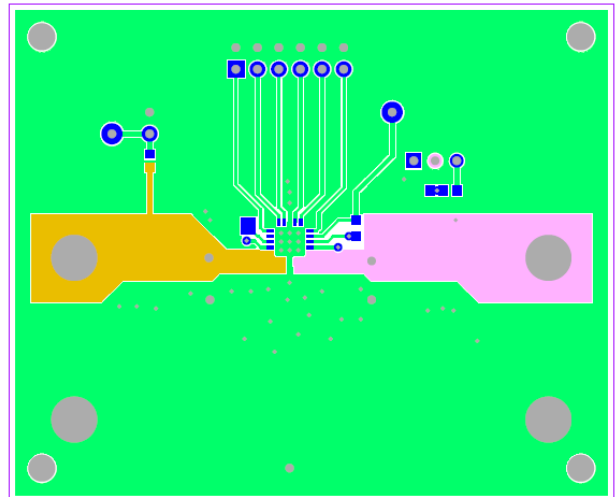


Figure 8. Top Layer

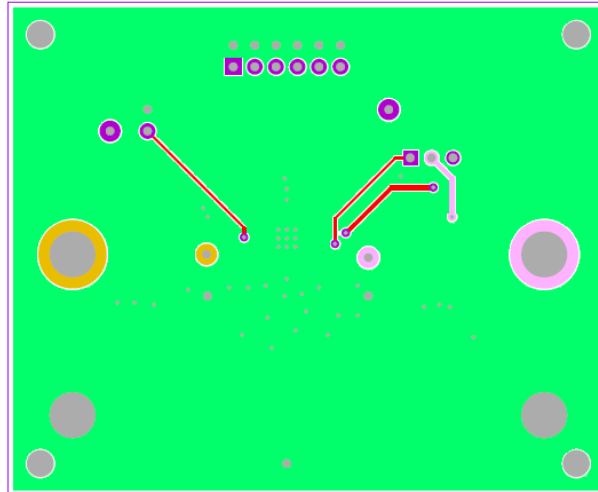


Figure 9. Bottom Layer

3. Typical Performance Curves

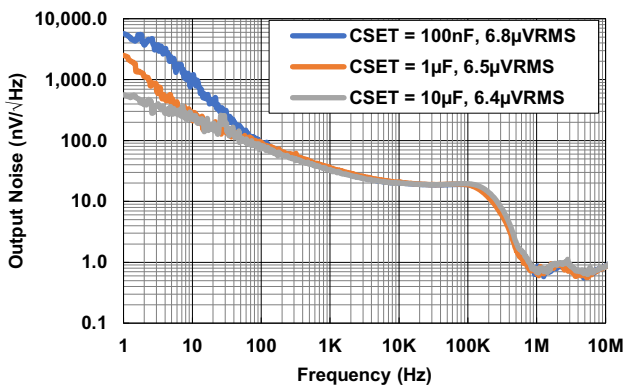


Figure 10. Output Noise vs Frequency for Various C_{SET} ($V_{IN} = V_{OUT} + 500mV$, $I_{OUT} = 2A$, $C_{SET} = 1\mu F$, $C_{OUT} = 22\mu F$)

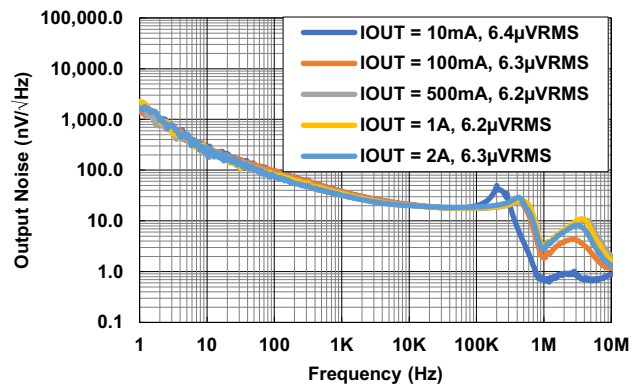


Figure 11. Output Noise vs Frequency for various I_{OUT} ($V_{IN} = V_{OUT} + 1V$, $C_{SET} = 1\mu F$, $C_{OUT} = 22\mu F$)

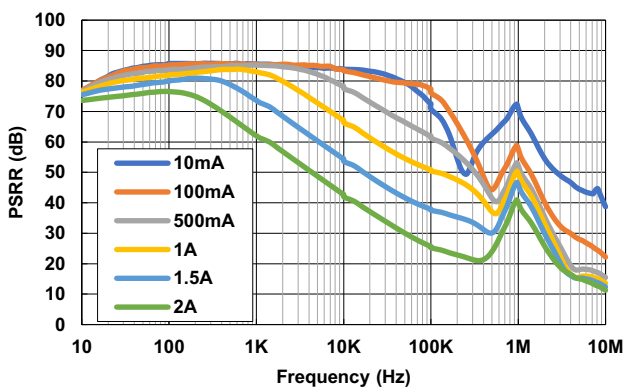


Figure 12. PSRR vs Frequency ($V_{IN} = 4V$, $V_{OUT} = 3.3V$, $C_{SET} = 1\mu F$, $C_{OUT} = 22\mu F$)

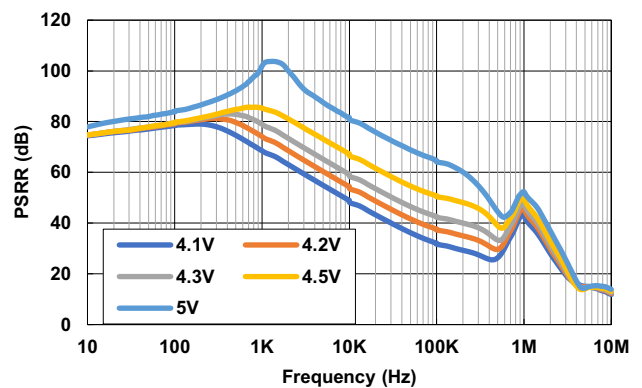


Figure 13. PSRR vs Frequency for various V_{IN} ($V_{OUT} = 3.3V$, $I_{OUT} = 2A$, $C_{SET} = 1\mu F$, $C_{OUT} = 22\mu F$)

4. Ordering Information

Part Number	Description
RTKA214023DE0000BU	RAA214023 evaluation board

5. Revision History

Rev.	Date	Description
1.00	Sep 16, 2021	Initial release

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