To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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DATA SHEET

BIPOLAR ANALOG INTEGRATED CIRCUIT

μPC4570

ULTRA LOW-NOISE, WIDEBAND, DUAL OPERATIONAL AMPLIFIER

DESCRIPTION

The μPC4570 is an ultra low-noise, wideband high slew-rate, dual operational amplifier. Input equivalent noise is three times better than the conventional 4558 type op-amps. The gain bandwidth products and the slew-rate are seven times better than 4558. In spite of fast AC performance, the μPC4570 is extremely stable under voltage-follower circuit conditions. Supply current is also improved compared with conventional wideband op-amps. The μPC4570 is an excellent choice for pre-amplifiers and active filters in audio, instrumentation, and communication circuits.

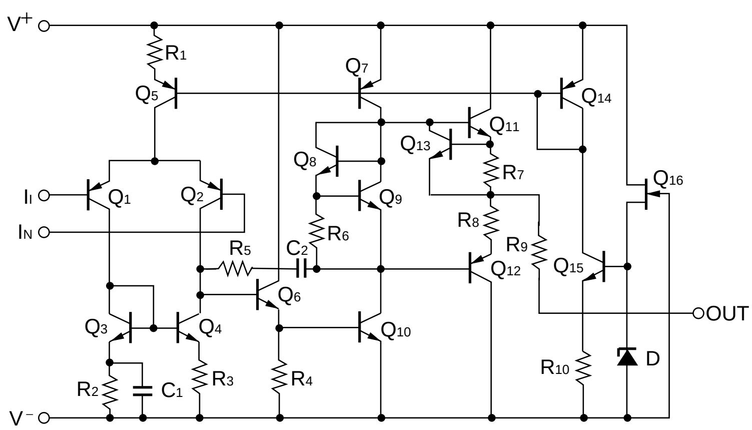
FEATURES

- Ultra low noise: e_n = 4.5 nV/$\sqrt{Hz}$
- High slew rate: 7 V/μs
- High gain bandwidth product: GBW = 15 MHz at 100 kHz
- Internal frequency compensation

<R> **ORDERING INFORMATION**

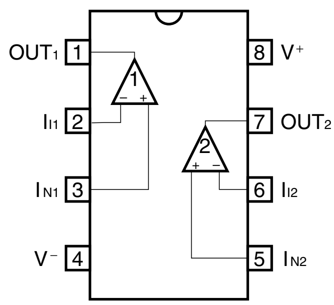
Part Number	Package
μPC4570C	8-pin plastic DIP (7.62 mm (300))
μPC4570G2	8-pin plastic SOP (5.72 mm (225))
μPC4570G2(5)	8-pin plastic SOP (5.72 mm (225))

EQUIVALENT CIRCUIT (1/2 Circuit)



<R> **PIN CONFIGURATION (Top View)**

μPC4570C, 4570G2



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Not all products and/or types are available in every country. Please check with an NEC Electronics sales representative for availability and additional information.

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Date Published December 2007 NS
Printed in Japan

The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

<R> ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Parameter		Symbol	Ratings	Unit
Voltage between V^+ and V^- Note1		$V^+ - V^-$	−0.3 to +36	V
Differential Input Voltage		V_{ID}	±30	V
Input Voltage Note2		V_I	$V^- - 0.3$ to $V^+ + 0.3$	V
Output Voltage Note3		V_O	$V^- - 0.3$ to $V^+ + 0.3$	V
Power Dissipation	C Package Note4	P_T	350	mW
	G2 Package Note5		440	mW
Output Short Circuit Duration Note6		ts	10	sec
Operating Ambient Temperature		T_A	−20 to +80	°C
Storage Temperature		T_{stg}	−55 to +125	°C

Notes 1. Reverse connection of supply voltage can cause destruction.

2. The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.

3. This specification is the voltage which should be allowed to supply to the output terminal from external without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The output voltage of normal operation will be the Output Voltage Swing of electrical characteristics.

4. Thermal derating factor is −5.0 mW/°C when operating ambient temperature is higher than 55°C.

5. Thermal derating factor is −4.4 mW/°C when operating ambient temperature is higher than 25°C.

6. Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings, Note 4 and Note 5.

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage	$V^\pm$	±4		±16	V
Output Current	I_O			±10	mA
Source Resistance	R_S			50	kΩ
Capacitive Load (A_V = +1)	C_L			100	pF

<R> μPC4570C, μPC4570G2

ELECTRICAL CHARACTERISTICS (T_A = 25°C, $V^{\pm}$ = ±15 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Offset Voltage	V_{IO}	$R_S \leq 50\ \Omega$		±0.3	±5	mV
Input Offset Current Note7	I_{IO}			±10	±100	nA
Input Bias Current Note7	I_B			100	400	nA
Large Signal Voltage Gain	A_V	$R_L \geq 2$ kΩ , V_O = ±10 V	30,000	300,000		
Supply Current Note8	I_{CC}	I_O = 0 A		5	8	mA
Common Mode Rejection Ratio	CMR		80	100		dB
Supply Voltage Rejection Ratio	SVR		80	100		dB
Output Voltage Swing	V_{om}	$R_L \geq 10$ kΩ	±12	±13.4		V
		$R_L \geq 2$ kΩ	±10	±12.8		V
Common Mode Input Voltage Range	V_{ICM}		±12	±14		V
Slew Rate	SR	$R_L \geq 2$ kΩ	5	7		V/μs
Gain Bandwidth Product	GBW	f_O = 100 kHz	10	15		MHz
Unity Gain Frequency	f_{unity}	open loop		7		MHz
Phase Margin	ϕ_{unity}	open loop		50		degree
Total Harmonic Distortion	THD	V_O = 3 $V_{r.m.s.}$, f = 20 Hz to 20 kHz (Figure1)		0.002		%
Input Equivalent Noise Voltage	V_n	RIAA (Figure2)		0.9		$\mu V_{r.m.s.}$
		FLAT+JIS A, R_S = 100 Ω (Figure3)		0.53	0.65	$\mu V_{r.m.s.}$
Input Equivalent Noise Voltage Density	e_n	f_O = 10 Hz, R_S = 100 Ω		5.5		nV/$\sqrt{Hz}$
		f_O = 1 kHz, R_S = 100 Ω		4.5		nV/$\sqrt{Hz}$
Input Equivalent Noise Current Density	i_n	f_O = 1 kHz		0.7		pA/$\sqrt{Hz}$
Channel Separation		f = 20 Hz to 20 kHz		120		dB

Notes 7. Input bias currents flow out from IC. Because each currents are base current of PNP-transistor on input stage

8. This current flows irrespective of the existence of use.

μPC4570G2(5)

ELECTRICAL CHARACTERISTICS (T_A = 25°C, $V^{\pm}$ = ±15 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Offset Voltage	V_{IO}	$R_S \leq 50\ \Omega$		±0.3	±1	mV
Input Offset Current Note7	I_{IO}			±10	±50	nA
Input Bias Current Note7	I_B			100	200	nA
Large Signal Voltage Gain	A_V	$R_L \geq 2$ kΩ , V_O = ±10 V	50,000	300,000		
Supply Current Note8	I_{CC}	I_O = 0 A		5	7	mA
Common Mode Rejection Ratio	CMR		85	100		dB
Supply Voltage Rejection Ratio	SVR		85	100		dB
Output Voltage Swing	V_{om}	$R_L \geq 10$ kΩ	±13	±13.4		V
		$R_L \geq 2$ kΩ	±12	±12.8		V
Common Mode Input Voltage Range	V_{ICM}		±13.5	±14		V
Slew Rate	SR	$R_L \geq 2$ kΩ	5	7		V/μs
Gain Bandwidth Product	GBW	f_O = 100 kHz	10	15		MHz
Unity Gain Frequency	f_{unity}	open loop		7		MHz
Phase Margin	ϕ_{unity}	open loop		50		degree
Total Harmonic Distortion	THD	V_O = 3 $V_{r.m.s.}$, f = 20 Hz to 20 kHz (Figure1)		0.002		%
Input Equivalent Noise Voltage	V_n	RIAA (Figure2)		0.9		$\mu V_{r.m.s.}$
		FLAT+JIS A, R_S = 100 Ω (Figure3)		0.53	0.65	$\mu V_{r.m.s.}$
Input Equivalent Noise Voltage Density	e_n	f_O = 10 Hz, R_S = 100 Ω		5.5		nV/$\sqrt{Hz}$
		f_O = 1 kHz, R_S = 100 Ω		4.5		nV/$\sqrt{Hz}$
Input Equivalent Noise Current Density	i_n	f_O = 1 kHz		0.7		pA/$\sqrt{Hz}$
Channel Separation		f = 20 Hz to 20 kHz		120		dB

Notes 7. Input bias currents flow out from IC. Because each currents are base current of PNP-transistor on input stage

8. This current flows irrespective of the existence of use.

MEASUREMENT CIRCUIT

Figure1 Total Harmonic Distortion Measurement Circuit

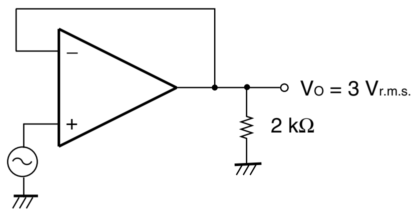


Figure2 Noise Measurement Circuit (RIAA)

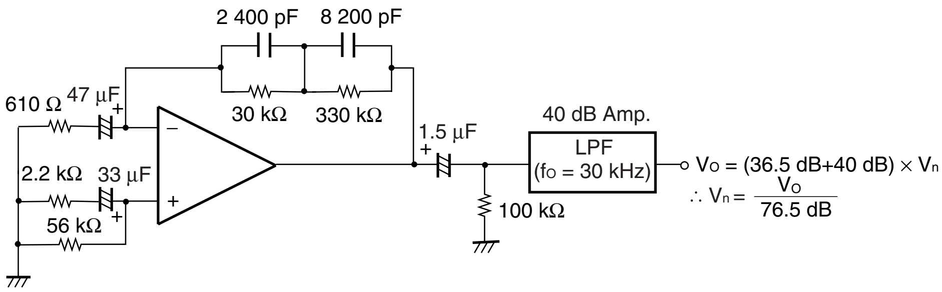
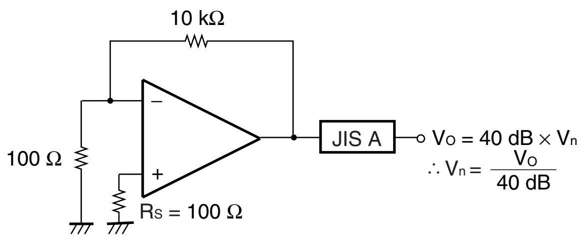
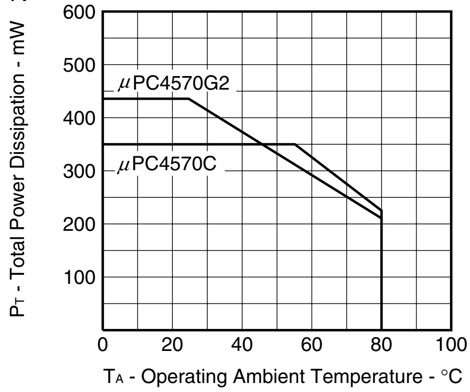


Figure3 Noise Measurement Circuit (FLAT+JIS A)

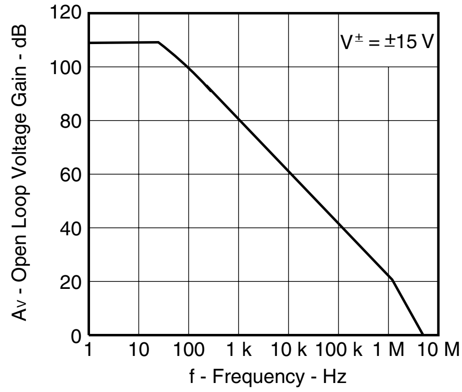


TYPICAL PERFORMANCE CHARACTERISTICS (T_A = 25°C, TYP.)

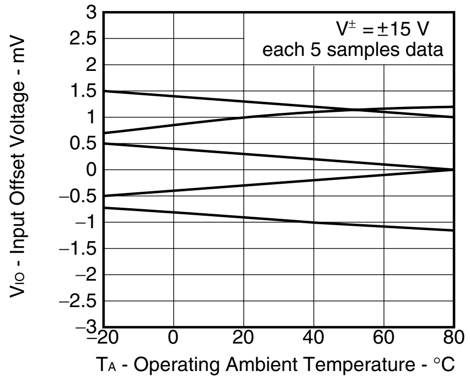
<R> POWER DISSIPATION



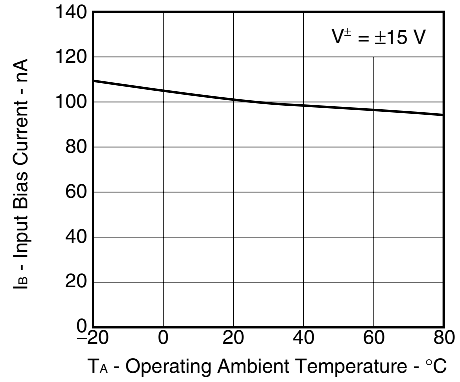
OPEN LOOP FREQUENCY RESPONSE



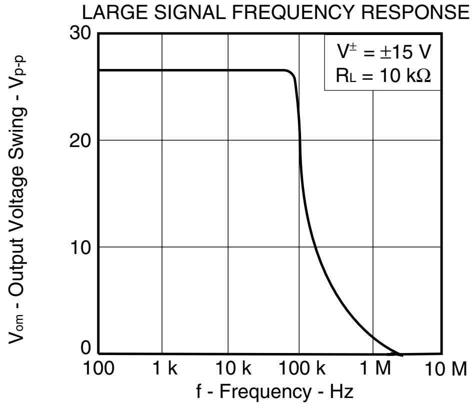
INPUT OFFSET VOLTAGE



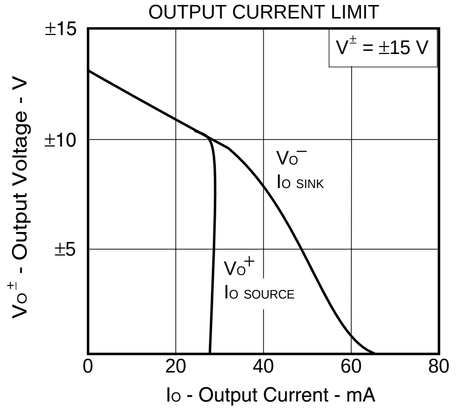
INPUT BIAS CURRENT



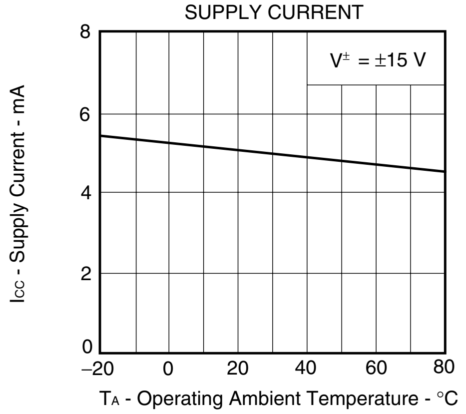
LARGE SIGNAL FREQUENCY RESPONSE



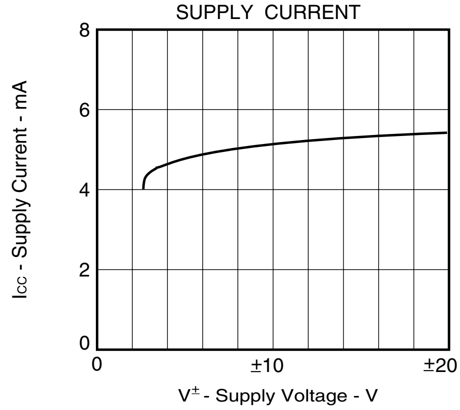
OUTPUT CURRENT LIMIT



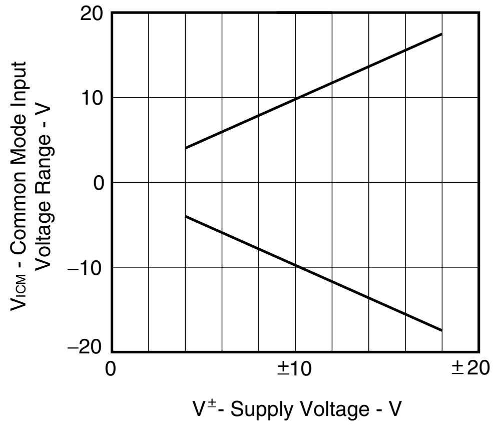
SUPPLY CURRENT



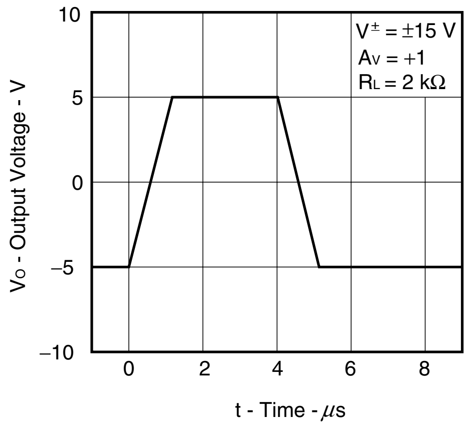
SUPPLY CURRENT



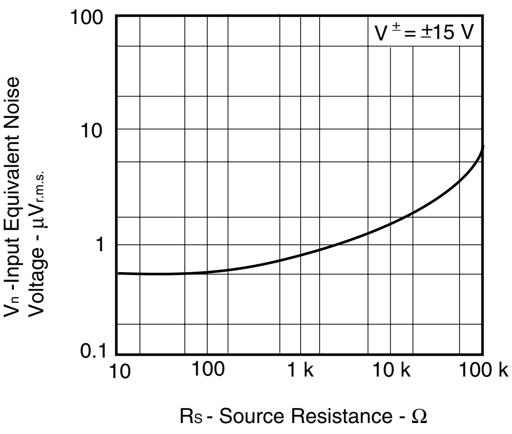
COMMON MODE INPUT VOLTAGE RANGE



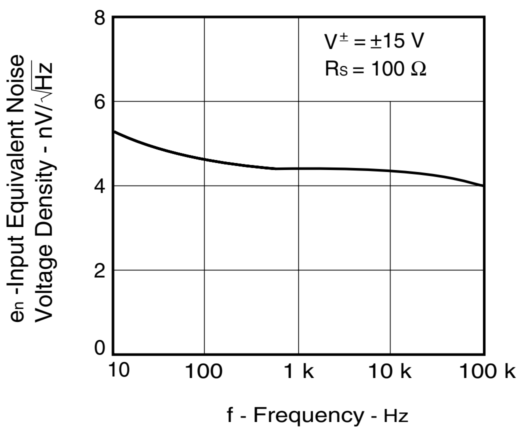
VOLTAGE FOLLOWER PULSE RESPONSE



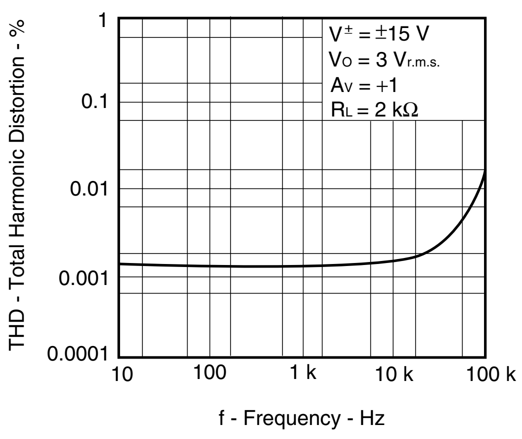
INPUT EQUIVALENT NOISE VOLTAGE (FLAT+JIS A)



INPUT EQUIVALENT NOISE VOLTAGE DENSITY

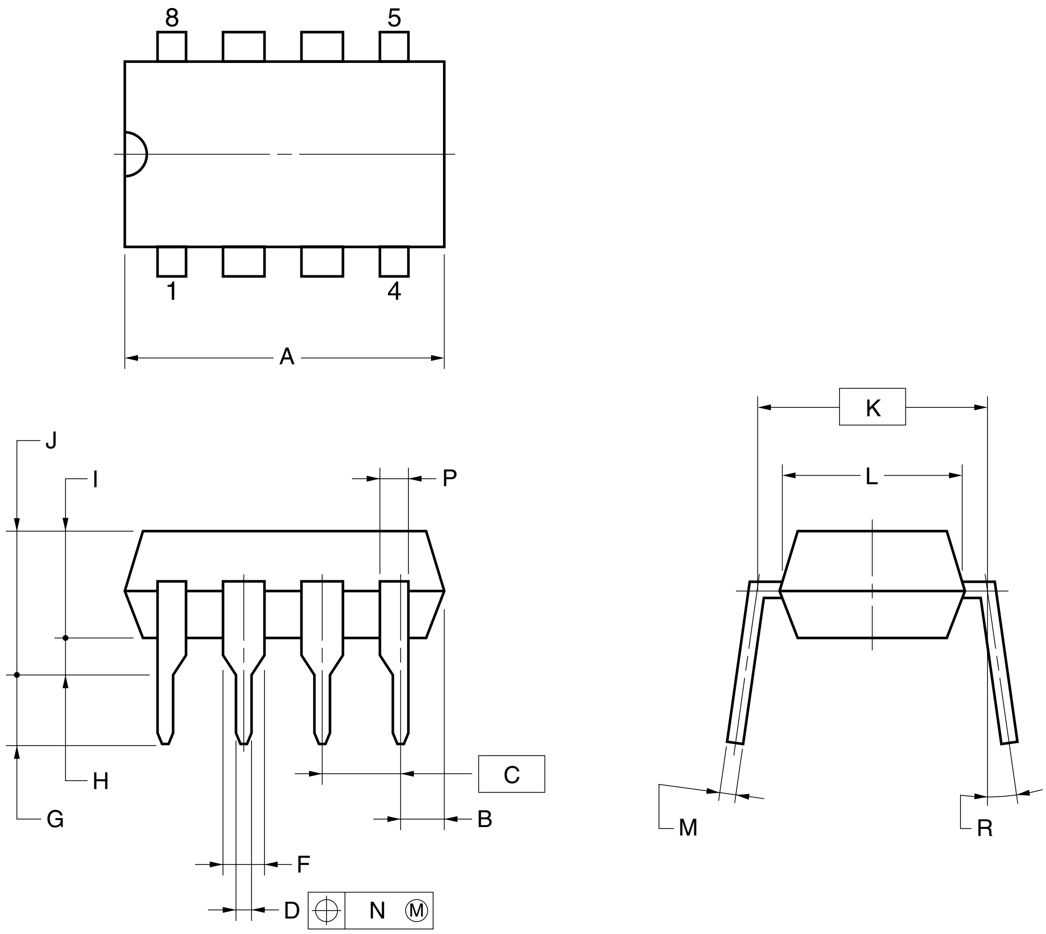


TOTAL HARMONIC DISTORTION



<R> PACKAGE DRAWINGS (Unit: mm)

8-PIN PLASTIC DIP (7.62mm(300))



NOTES

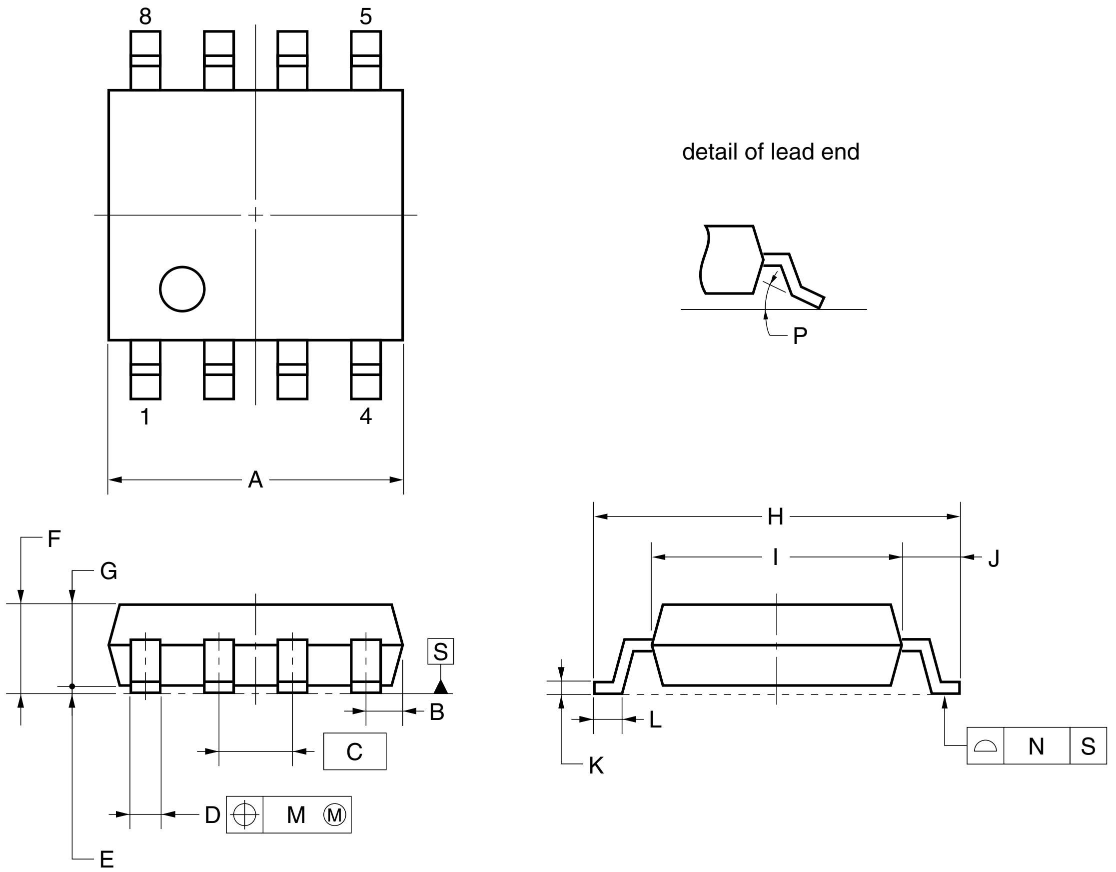
1. Each lead centerline is located within 0.25 mm of its true position (T.P.) at maximum material condition.

2. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS
A	10.16 MAX.
B	1.27 MAX.
C	2.54 (T.P.)
D	0.50±0.10
F	1.4 MIN.
G	3.2±0.3
H	0.51 MIN.
I	4.31 MAX.
J	5.08 MAX.
K	7.62 (T.P.)
L	6.4
M	$0.25^{+0.10}_{-0.05}$
N	0.25
P	0.9 MIN.
R	0~15°

P8C-100-300B,C-2

8-PIN PLASTIC SOP (5.72 mm (225))



NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	$5.2^{+0.17}_{-0.20}$
B	0.78 MAX.
C	1.27 (T.P.)
D	$0.42^{+0.08}_{-0.07}$
E	0.1±0.1
F	1.59±0.21
G	1.49
H	6.5±0.3
I	4.4±0.15
J	1.1±0.2
K	$0.17^{+0.08}_{-0.07}$
L	0.6±0.2
M	0.12
N	0.10
P	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$

S8GM-50-225B-6

<R> RECOMMENDED SOLDERING CONDITIONS

The μPC4570 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.necel.com/pkg/en/mount/index.html)

Type of Surface Mount Device

μPC4570G2, μPC4570G2(5): 8-pin plastic SOP (5.72 mm (225))

Process	Conditions	Symbol
Infrared Ray Reflow	Peak temperature: 230°C or below (Package surface temperature), Reflow time: 30 seconds or less (at 210°C or higher), Maximum number of reflow processes: 1 time.	IR30-00-1
Vapor Phase Soldering	Peak temperature: 215°C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200°C or higher), Maximum number of reflow processes: 1 time.	VP15-00-1
Wave Soldering	Solder temperature: 260°C or below, Flow time: 10 seconds or less, Maximum number of flow processes: 1 time, Pre-heating temperature: 120°C or below (Package surface temperature).	WS60-00-1
Partial Heating Method	Pin temperature: 300°C or below, Heat time: 3 seconds or less (Per each side of the device).	–

Caution Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

Type of Through-hole Device

μPC4570C: 8-pin plastic DIP (7.62 mm (300))

Process	Conditions
Wave Soldering (only to leads)	Solder temperature: 260°C or below, Flow time: 10 seconds or less.
Partial Heating Method	Pin temperature: 300°C or below, Heat time: 3 seconds or less (per each lead).

Caution For through-hole device, the wave soldering process must be applied only to leads, and make sure that the package body does not get jet soldered.

<R> REFERENCE DOCUMENTS

QUALITY GRADES ON NEC SEMICONDUCTOR DEVICES	C11531E
SEMICONDUCTOR DEVICE MOUNT MANUAL	http://www.necel.com/pkg/en/mount/index.html
NEC SEMICONDUCTOR DEVICE RELIABILITY/ QUALITY CONTROL SYSTEM- STANDARD LINEAR IC	IEI-1212

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