

To our customers,

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## Old Company Name in Catalogs and Other Documents

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On April 1<sup>st</sup>, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: <http://www.renesas.com>

April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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# BIPOLAR ANALOG INTEGRATED CIRCUIT

## $\mu$ PC4572

**LOW SUPPLY VOLTAGE, ULTRA LOW-NOISE, HIGH SPEED, WIDE BAND,  
LOW  $I_B$  DUAL OPERATIONAL AMPLIFIER**

### DESCRIPTION

The  $\mu$ PC4572 is a dual wide band, ultra low noise operational amplifier designed for low supply voltage operation of +4 V to +14 V single supply and  $\pm 2$  V to  $\pm 7$  V split supplies. Using high  $h_{FE}$  PNP transistors for the input circuit, Input bias current and input equivalent noise are better than conventional wide band operational amplifier.

The  $\mu$ PC4572 is an excellent choice for preamplifiers and active filters in audio, instrumentation, and communication circuit.

### FEATURES

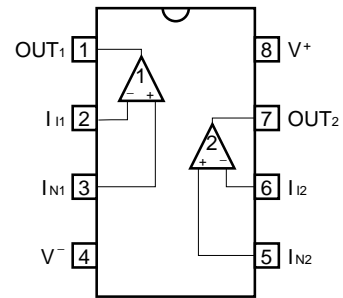
- Ultra low noise:  $e_n = 4.0 \text{ nV} / \sqrt{\text{Hz}}$
- Low input bias current: 100 nA
- High slew rate:  $6 \text{ V} / \mu\text{s}$
- Low supply voltage:  $\pm 2 \text{ V}$  to  $\pm 7 \text{ V}$  (Split)  
+4 V to +14 V (Single)
- Internal frequency compensation

### <R> ORDERING INFORMATION

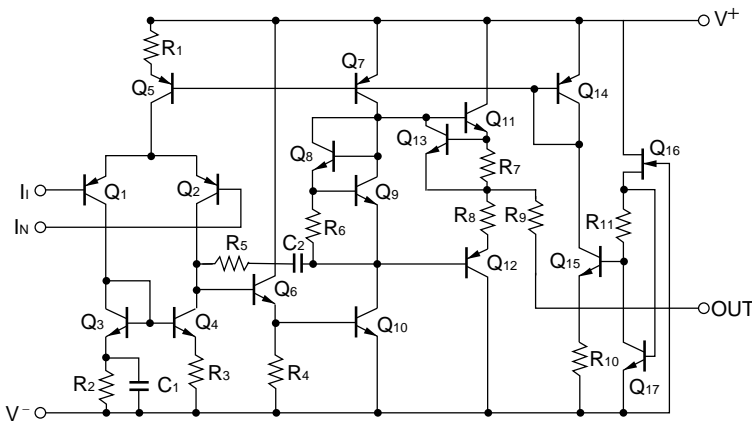
Part Number	Package
$\mu$ PC4572C	8-pin plastic DIP (7.62 mm (300) )
$\mu$ PC4572C(5)	8-pin plastic DIP (7.62 mm (300) )
$\mu$ PC4572G2	8-pin plastic SOP (5.72 mm (225) )
$\mu$ PC4572G2(5)	8-pin plastic SOP (5.72 mm (225) )

### <R> PIN CONFIGURATION (Top View)

$\mu$ PC4572C, 4572C(5), 4572G2, 4572G2(5)



### EQUIVALENT CIRCUIT (1/2 Circuit)



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<R> **ABSOLUTE MAXIMUM RATINGS (T<sub>A</sub> = 25°C)**

Parameter		Symbol	Ratings	Unit
Voltage between V <sup>+</sup> and V <sup>-</sup> <sup>Note1</sup>		V <sup>+</sup> - V <sup>-</sup>	-0.3 to +15	V
Differential Input Voltage		V <sub>ID</sub>	±10	V
Input Voltage <sup>Note2</sup>		V <sub>I</sub>	V <sup>-</sup> - 0.3 to V <sup>+</sup> + 0.3	V
Output Voltage <sup>Note3</sup>		V <sub>O</sub>	V <sup>-</sup> - 0.3 to V <sup>+</sup> + 0.3	V
Power Dissipation	C Package <sup>Note4</sup>	P <sub>T</sub>	350	mW
	G2 Package <sup>Note5</sup>		440	mW
Output Short Circuit Duration <sup>Note6</sup>		t <sub>s</sub>	10	sec
Operating Ambient Temperature		T <sub>A</sub>	-20 to +80	°C
Storage Temperature		T <sub>stg</sub>	-55 to +125	°C

- Notes**
- Reverse connection of supply voltage can cause destruction.
  - The input voltage should be allowed to input without damage or destruction. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The normal operation will establish when the both inputs are within the Common Mode Input Voltage Range of electrical characteristics.
  - This specification is the voltage, which should be allowed to supply to the output terminal from external without damage or destructive. Even during the transition period of supply voltage, power on/off etc., this specification should be kept. The output voltage of normal operation will be the Output Voltage Swing of electrical characteristics.
  - Thermal derating factor is -5.0 mW/°C when ambient temperature is higher than 55°C.
  - Thermal derating factor is -4.4 mW/°C when ambient temperature is higher than 25°C.
  - Pay careful attention to the total power dissipation not to exceed the absolute maximum ratings, Note 4 and Note 5.

**RECOMMENDED OPERATING CONDITIONS**

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Supply Voltage (Split)	V <sup>±</sup>	±2	±5	±7	V
Supply Voltage (V <sup>-</sup> = GND)	V <sup>+</sup>	+4	+5/ +12	+14	V
Output Current	I <sub>o</sub>			±10	mA
Capacitive Load (A <sub>v</sub> = +1)	C <sub>L</sub>			100	pF

<R> μPC4572C, μPC4572G2

**ELECTRICAL CHARACTERISTICS (TA = 25°C, V± = ±5 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Offset Voltage	V <sub>IO</sub>	R <sub>S</sub> ≤ 50 Ω		±0.3	±5	mV
Input Offset Current <sup>Note7</sup>	I <sub>IO</sub>			±10	±100	nA
Input Bias Current <sup>Note7</sup>	I <sub>B</sub>			100	400	nA
Large Signal Voltage Gain	A <sub>V</sub>	R <sub>L</sub> ≥ 2 kΩ, V <sub>O</sub> = ±2 V	10000	100000		
Supply Current <sup>Note8</sup>	I <sub>CC</sub>	I <sub>O</sub> = 0 A		4.5	7	mA
Common Mode Rejection Ratio	CMR		70	90		dB
Supply Voltage Rejection Ratio	SVR		70	85		dB
Output Voltage Swing	V <sub>OM</sub>	R <sub>L</sub> ≥ 10 kΩ	±3.3	±3.7		V
		R <sub>L</sub> ≥ 2 kΩ	±3.0	±3.5		
Common Mode Input Voltage Range	V <sub>ICM</sub>		±3.5	±4		V
Output Short Circuit Current	I <sub>O short</sub>	R <sub>L</sub> = 0	±15	±20		mA
Slew Rate	SR	A <sub>V</sub> = +1, R <sub>L</sub> ≥ 2 kΩ	3.5	6		V/μs
Gain Band Width Product	GBW	f <sub>O</sub> = 100 kHz	10	16		MHz
Unity Gain Frequency	f <sub>unity</sub>	open loop		9		MHz
Phase Margin	φ <sub>unity</sub>	open loop		60		degree
Total Harmonic Distortion	THD	V <sub>O</sub> = 1 V <sub>r.m.s.</sub> , f = 20 Hz to 20 kHz (Fig.1)		0.002		%
Input Equivalent Noise Voltage	V <sub>n</sub>	RIAA (Fig.2)		0.8		μV <sub>r.m.s.</sub>
		FLAT+JIS A, R <sub>S</sub> = 100 Ω (Fig.3)		0.5	0.65	
Input Equivalent Noise Voltage Density	e <sub>n</sub>	f <sub>O</sub> = 10 Hz		4.5		nV/√Hz
		f <sub>O</sub> = 1 kHz		4.0		
Input Equivalent Noise Current Density	i <sub>n</sub>	f <sub>O</sub> = 1 kHz		0.7		pA/√Hz
Channel Separation		f = 20 Hz to 20 kHz		120		dB
Average V <sub>IO</sub> Temperature Drift	ΔV <sub>IO</sub> /ΔT			±2		μV/°C

**ELECTRICAL CHARACTERISTICS (TA = 25°C, V± = ±5 V, V<sup>-</sup> = GND)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Offset Voltage	V <sub>IO</sub>	R <sub>S</sub> ≤ 50 Ω		±0.3	±5	mV
Input Offset Current <sup>Note7</sup>	I <sub>IO</sub>			±10	±100	nA
Input Bias Current <sup>Note7</sup>	I <sub>B</sub>			100	400	nA
Large Signal Voltage Gain	A <sub>V</sub>	R <sub>L</sub> ≥ 2 kΩ	8000	80000		
Supply Current <sup>Note8</sup>	I <sub>CC</sub>	I <sub>O</sub> = 0 A		4	6	mA
Common Mode Rejection Ratio	CMR		60	75		dB
Supply Voltage Rejection Ratio	SVR		60	70		dB
Output Voltage (High)	V <sub>OH</sub>	R <sub>L</sub> ≥ 2 kΩ (R <sub>L</sub> to 1/2 V <sup>+</sup> )	3.2	3.5		V
Output Voltage (Low)	V <sub>OL</sub>	R <sub>L</sub> ≥ 2 kΩ (R <sub>L</sub> to 1/2 V <sup>+</sup> )		1.3	1.6	V
Common Mode Input Voltage Range	V <sub>ICM</sub>		1.5		3.5	V
Slew Rate	SR	A <sub>V</sub> = +1		4		V/μs
Gain Band Width Product	GBW			12		MHz

**Notes 7.** Input bias currents flow out from IC. Because each currents are base current of PNP-transistor on input stage.

**8.** This current flows irrespective of the existence of use.

<R> μPC4572C(5), μPC4572G2(5)

**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sup>±</sup> = ±5 V)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Offset Voltage	V <sub>io</sub>	R <sub>S</sub> ≤ 50 Ω		±0.3	±1.5	mV
Input Offset Current <sup>Note7</sup>	I <sub>io</sub>			±10	±50	nA
Input Bias Current <sup>Note7</sup>	I <sub>b</sub>			100	200	nA
Large Signal Voltage Gain	A <sub>v</sub>	R <sub>L</sub> ≥ 2 kΩ, V <sub>o</sub> = ±2 V	30000	100000		
Supply Current <sup>Note8</sup>	I <sub>cc</sub>	I <sub>o</sub> = 0 A		4.5	5.5	mA
Common Mode Rejection Ratio	CMR		75	90		dB
Supply Voltage Rejection Ratio	SVR		70	85		dB
Output Voltage Swing	V <sub>om</sub>	R <sub>L</sub> ≥ 10 kΩ	±3.45	±3.7		V
		R <sub>L</sub> ≥ 2 kΩ	±3.3	±3.5		
Common Mode Input Voltage Range	V <sub>icm</sub>		+3.8 -3.7	±4		V
Output Short Circuit Current	I <sub>o short</sub>	R <sub>L</sub> = 0	±15	±20		mA
Slew Rate	SR	A <sub>v</sub> = +1, R <sub>L</sub> ≥ 2 kΩ	3.5	6		V/μs
Gain Band Width Product	GBW	f <sub>o</sub> = 100 kHz	10	16		MHz
Unity Gain Frequency	f <sub>unity</sub>	open loop		9		MHz
Phase Margin	φ <sub>unity</sub>	open loop		60		degree
Total Harmonic Distortion	THD	V <sub>o</sub> = 1 V <sub>r.m.s.</sub> , f = 20 Hz to 20 kHz (Figure1)		0.002		%
Input Equivalent Noise Voltage	V <sub>n</sub>	RIAA (Figure2)		0.8		μV <sub>r.m.s.</sub>
		FLAT+JIS A, R <sub>S</sub> = 100 Ω (Figure3)		0.5	0.65	
Input Equivalent Noise Voltage Density	e <sub>n</sub>	f <sub>o</sub> = 10 Hz		4.5		nV/√Hz
		f <sub>o</sub> = 1 kHz		4.0		
Input Equivalent Noise Current Density	i <sub>n</sub>	f <sub>o</sub> = 1 kHz		0.7		pA/√Hz
Channel Separation		f = 20 Hz to 20 kHz		120		dB
Average V <sub>io</sub> Temperature Drift	ΔV <sub>io</sub> /ΔT			±2		μV/°C

**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, V<sup>+</sup> = +5 V, V<sup>-</sup> = GND)**

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Offset Voltage	V <sub>io</sub>	R <sub>S</sub> ≤ 50 Ω		±0.3	±1.5	mV
Input Offset Current <sup>Note7</sup>	I <sub>io</sub>			±10	±50	nA
Input Bias Current <sup>Note7</sup>	I <sub>b</sub>			100	200	nA
Large Signal Voltage Gain	A <sub>v</sub>	R <sub>L</sub> ≥ 2 kΩ ,	40000	80000		
Supply Current <sup>Note8</sup>	I <sub>cc</sub>	I <sub>o</sub> = 0 A		4	5	mA
Common Mode Rejection Ratio	CMR		65	75		dB
Supply Voltage Rejection Ratio	SVR		60	70		dB
Output Voltage (High)	V <sub>OH</sub>	R <sub>L</sub> ≥ 2 kΩ (R <sub>L</sub> to 1/2 V <sup>+</sup> )	3.4	3.5		V
Output Voltage (Low)	V <sub>OL</sub>	R <sub>L</sub> ≥ 2 kΩ (R <sub>L</sub> to 1/2 V <sup>+</sup> )		1.3	1.45	V
Common Mode Input Voltage Range	V <sub>icm</sub>		1.2		3.8	V
Slew Rate	SR	A <sub>v</sub> = +1		4		V/μs
Gain Band Width Product	GBW			12		MHz

**Notes 7.** Input bias currents flow out from IC. Because each currents are base current of PNP-transistor on input stage.

**8.** This current flows irrespective of the existence of use.

MEASUREMENT CIRCUITS

Fig. 1 Total Harmonic Distortion Measurement Circuit

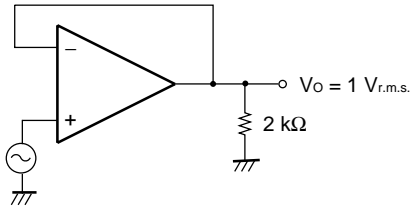


Fig. 2 Noise Measurement Circuit (RIAA)

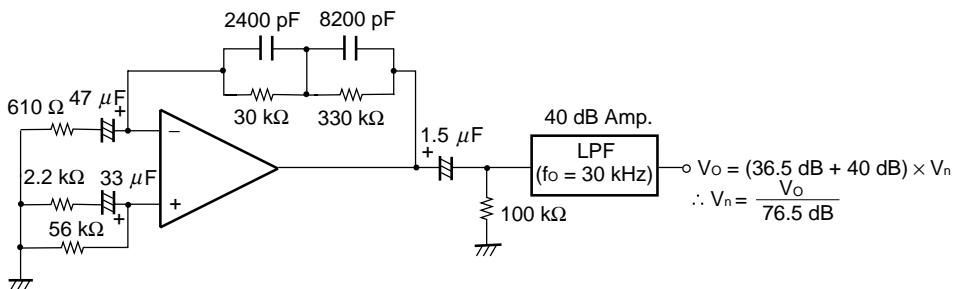
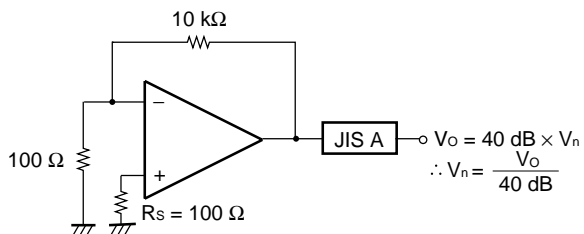
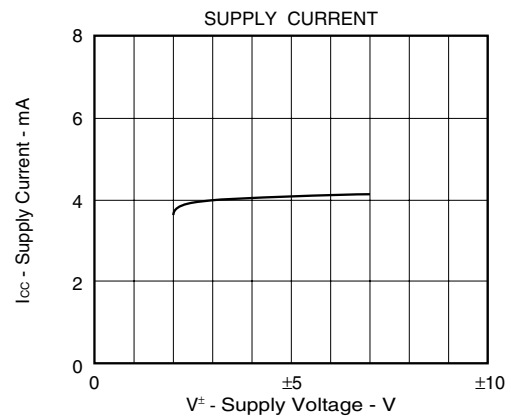
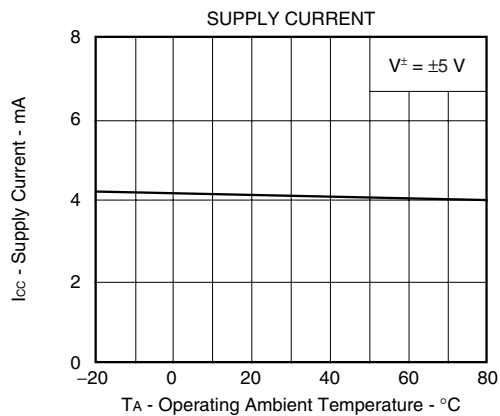
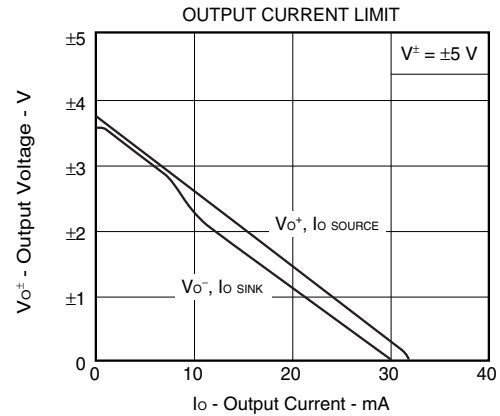
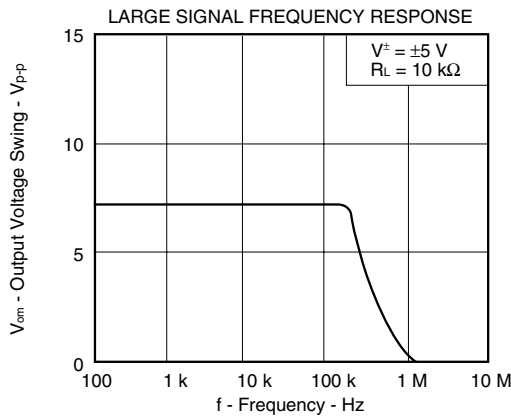
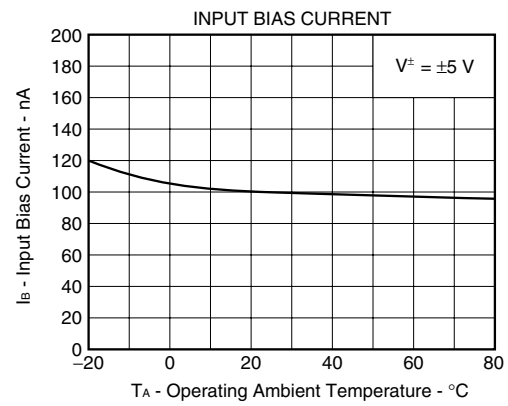
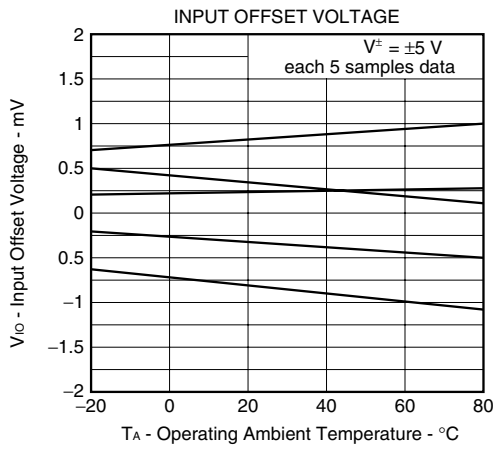
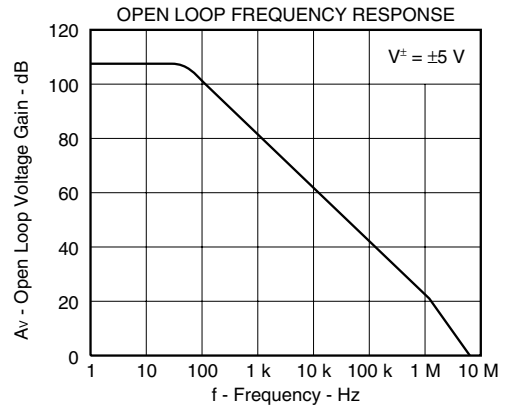
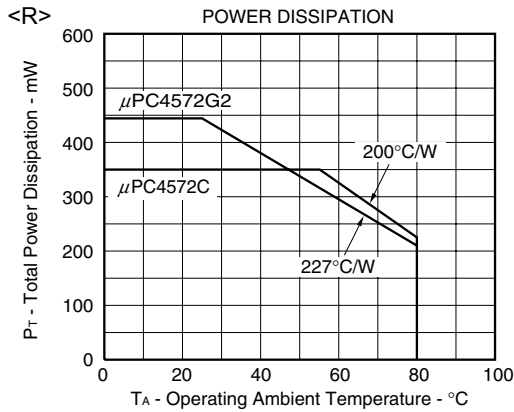


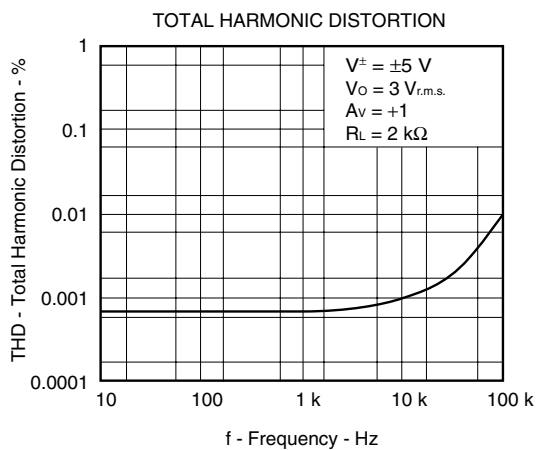
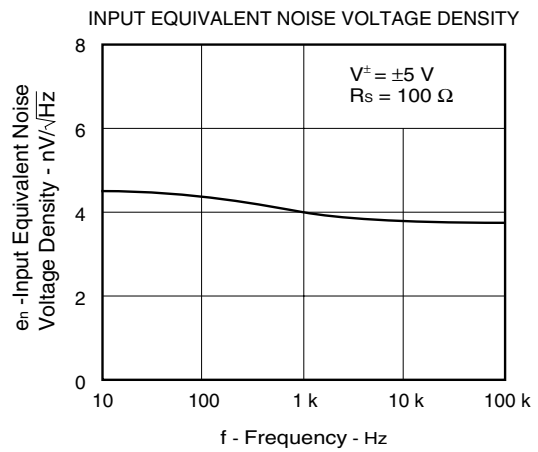
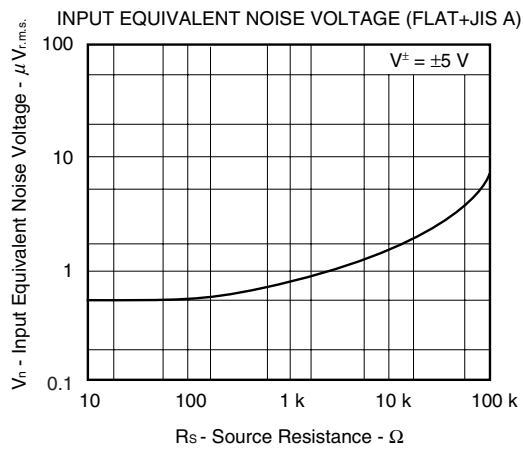
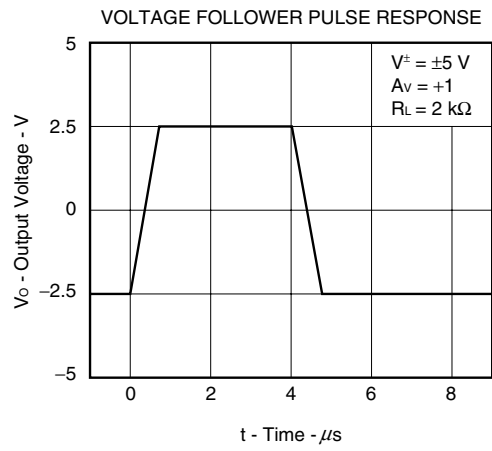
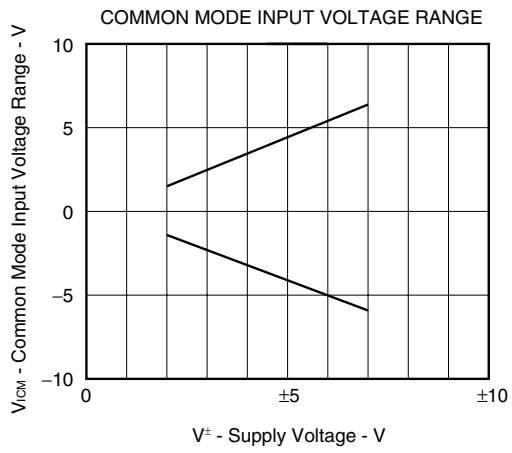
Fig. 3 Flat Noise Measurement Circuit (FLAT + JIS A)



TYPICAL PERFORMANCE CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , TYP.)

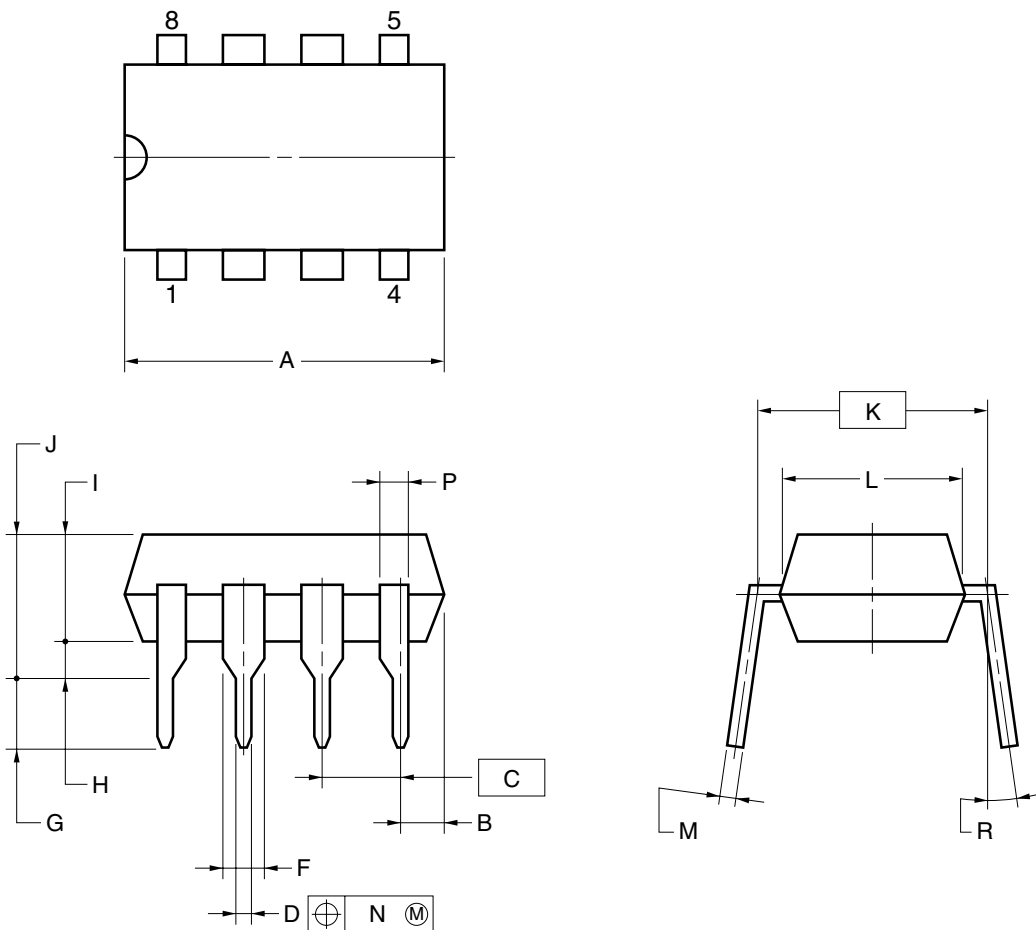






<R> PACKAGE DRAWINGS (Unit: mm)

8-PIN PLASTIC DIP (7.62mm(300))



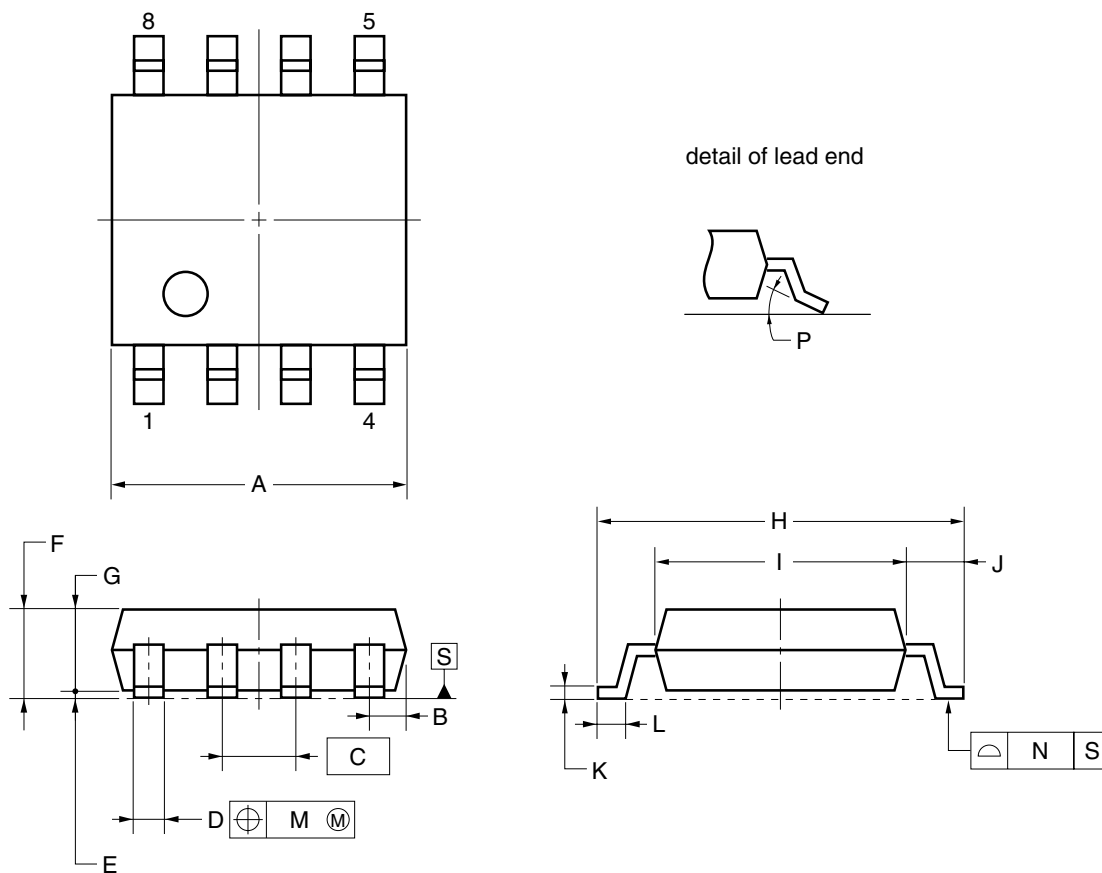
NOTES

1. Each lead centerline is located within 0.25 mm of its true position (T.P.) at maximum material condition.
2. Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS
A	10.16 MAX.
B	1.27 MAX.
C	2.54 (T.P.)
D	0.50±0.10
F	1.4 MIN.
G	3.2±0.3
H	0.51 MIN.
I	4.31 MAX.
J	5.08 MAX.
K	7.62 (T.P.)
L	6.4
M	0.25 <sup>+0.10</sup> <sub>-0.05</sub>
N	0.25
P	0.9 MIN.
R	0~15°

P8C-100-300B,C-2

8-PIN PLASTIC SOP (5.72 mm (225))



**NOTE**

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	5.2 $^{+0.17}_{-0.20}$
B	0.78 MAX.
C	1.27 (T.P.)
D	0.42 $^{+0.08}_{-0.07}$
E	0.1±0.1
F	1.59±0.21
G	1.49
H	6.5±0.3
I	4.4±0.15
J	1.1±0.2
K	0.17 $^{+0.08}_{-0.07}$
L	0.6±0.2
M	0.12
N	0.10
P	3° $^{+7}_{-3}$ °

S8GM-50-225B-6

<R> **RECOMMENDED SOLDERING CONDITIONS**

The μPC4572 should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

For technical information, see the following website.

**Semiconductor Device Mount Manual (<http://www.necel.com/pkg/en/mount/index.html>)**

**Type of Surface Mount Device**

**μPC4572G2, 4572G2(5): 8-pin plastic SOP (5.72 mm (225) )**

Process	Conditions	Symbol
Infrared Ray Reflow	Peak temperature: 230°C or below (Package surface temperature), Reflow time: 30 seconds or less (at 210°C or higher), Maximum number of reflow processes: 1 time.	IR30-00-1
Vapor Phase Soldering	Peak temperature: 215°C or below (Package surface temperature), Reflow time: 40 seconds or less (at 200°C or higher), Maximum number of reflow processes: 1 time.	VP15-00-1
Wave Soldering	Solder temperature: 260°C or below, Flow time: 10 seconds or less, Maximum number of flow processes: 1 time, Pre-heating temperature: 120°C or below (Package surface temperature).	WS60-00-1
Partial Heating Method	Pin temperature: 300°C or below, Heat time: 3 seconds or less (Per each side of the device).	—

**Caution** Apply only one kind of soldering condition to a device, except for "partial heating method", or the device will be damaged by heat stress.

**Type of Through-hole Device**

**μPC4572C, 4572C(5): 8-pin plastic DIP (7.62 mm (300) )**

Process	Conditions
Wave Soldering (only to leads)	Solder temperature: 260°C or below, Flow time: 10 seconds or less.
Partial Heating Method	Pin temperature: 300°C or below, Heat time: 3 seconds or less (per each lead).

**Caution** For through-hole device, the wave soldering process must be applied only to leads, and make sure that the package body does not get jet soldered.

<R> **REFERENCE DOCUMENTS**

QUALITY GRADES ON NEC SEMICONDUCTOR DEVICES	C11531E
SEMICONDUCTOR DEVICE MOUNT MANUAL	<a href="http://www.necel.com/pkg/en/mount/index.html">http://www.necel.com/pkg/en/mount/index.html</a>
NEC SEMICONDUCTOR DEVICE RELIABILITY/	IEI-1212
QUALITY CONTROL SYSTEM- STANDARD LINEAR IC	

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[SC2902DTBR2G](#) [SC2903DR2G](#) [SC2903VDR2G](#) [LM258AYDT](#) [LM358SNG](#) [430227FB](#) [430228DB](#) [460932C](#) [AZV831KTR-G1](#) [409256CB](#)  
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