μPD120Nxx Series

R03DS0030EJ0400
Rev.4.00
Apr 15, 2011

THREE-TERMINAL LOW-DROPOUT POSITIVE-VOLTAGE REGULATOR (OUTPUT CURRENT: 0.3 A)

Description

The μPD120Nxx series provides low-voltage output regulators with the output current capacitance of 0.3 A. The output voltage varies according to the product (1.5 V, 1.8 V, 2.5 V, or 3.3 V). The circuit current is low due to the CMOS structure, so the power consumption in the ICs can be reduced. Moreover, since ICs are mounted in the small package of the μPD120Nxx series, this contributes to the miniaturization of the application set.

Features

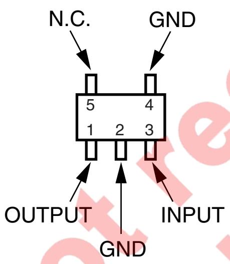
- Output current: 0.3 A
- On-chip overcurrent protection circuit
- On-chip thermal protection circuit
- Small circuit operation current: 60 μA TYP.

Applications

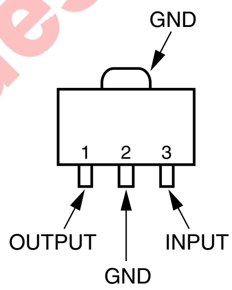
Digital TV, Audio, HDD, DVD, etc.

Pin Configurations (Marking Side)

SC-74A

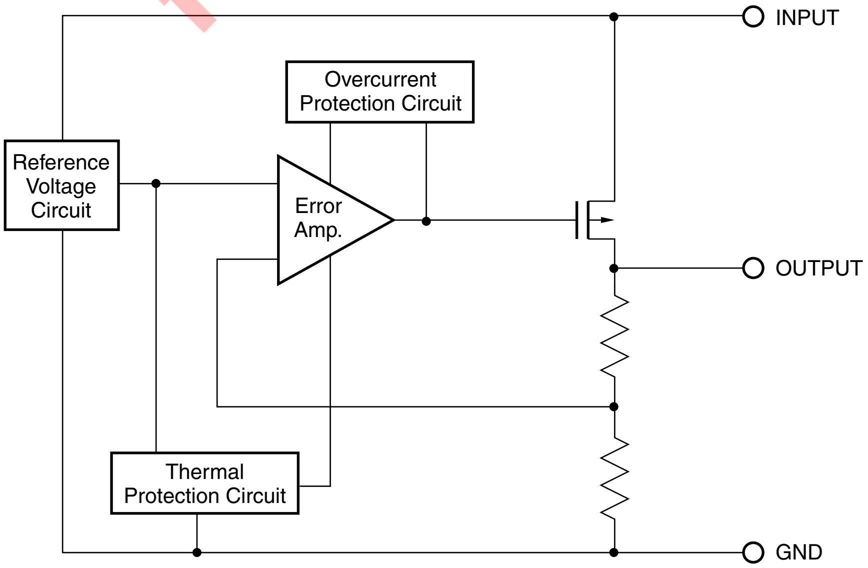


SC-62



Not recommend for new design

Block Diagram



The mark <R> shows major revised points.

The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

Ordering Information

Part Number	Package	Output Voltage	Marking
μPD120N15TA	SC-74A	1.5 V	K71
μPD120N15T1B	SC-62	1.5 V	7D
μPD120N18TA	SC-74A	1.8 V	K72
μPD120N18T1B	SC-62	1.8 V	7E
μPD120N25TA	SC-74A	2.5 V	K73
μPD120N25T1B	SC-62	2.5 V	7F
μPD120N33TA	SC-74A	.3.3 V	K74
μPD120N33T1B	SC-62	3.3 V	7G

Remark -E1 or -E2 is suffixed to the end of the part number of taping products, and -A, -AT, -AY or -AZ to that of Pb-free products. See the table below for details.

<R>

Part Number [Note1]	Package	Package Type
μPD120NxxTA-A [Note2]	SC-74A	• Unit
μPD120NxxTA-AT [Note2]	SC-74A	• Unit
μPD120NxxTA-E1-A [Note2]	SC-74A	• 8 mm wide embossed taping • Pin 1 on take-up side • 3000 pcs/reel (MAX.)
μPD120NxxTA-E1-AT [Note2]	SC-74A	• 8 mm wide embossed taping • Pin 1 on take-up side • 3000 pcs/reel (MAX.)
μPD120NxxTA-E2-A [Note2]	SC-74A	• 8 mm wide embossed taping • Pin 1 on draw-out side • 3000 pcs/reel (MAX.)
μPD120NxxTA-E2-AT [Note2]	SC-74A	• 8 mm wide embossed taping • Pin 1 on draw-out side • 3000 pcs/reel (MAX.)
μPD120NxxT1B-AY [Note3]	SC-62	• Unit
μPD120NxxT1B-AZ [Note3]	SC-62	• Unit
μPD120NxxT1B-E1-AY [Note3]	SC-62	• 12 mm wide embossed taping • Pin 1 on take-up side • 1000 pcs/reel (MAX.)
μPD120NxxT1B-E1-AZ [Note3]	SC-62	• 12 mm wide embossed taping • Pin 1 on take-up side • 1000 pcs/reel (MAX.)
μPD120NxxT1B-E2-AY [Note3]	SC-62	• 12 mm wide embossed taping • Pin 1 on draw-out side • 1000 pcs/reel (MAX.)
μPD120NxxT1B-E2-AZ [Note3]	SC-62	• 12 mm wide embossed taping • Pin 1 on draw-out side • 1000 pcs/reel (MAX.)

Not recommend for new design

Notes 1. xx stands for symbols that indicate the output voltage.

2. Pb-free (This product does not contain Pb in external electrode and other parts.)

3. Pb-free (This product does not contain Pb in external electrode.)

Absolute Maximum Ratings (T_A = 25°C, unless otherwise specified.)

Parameter	Symbol	Rating		Unit
		μPD120NxxTA	μPD120NxxT1B	
Input Voltage	V_{IN}	–0.3 to +6		V
Power Dissipation Note1	P_T	180/510 Note2	400/2000 Note3	mW
Operating Ambient Temperature	T_A	–40 to +85		°C
Operating Junction Temperature	T_J	–40 to +150		°C
Storage Temperature	T_{stg}	–55 to +150		°C
Thermal Resistance (junction to ambient)	$R_{th(J-A)}$	695/245 Note2	315/62.5 Note3	°C/W

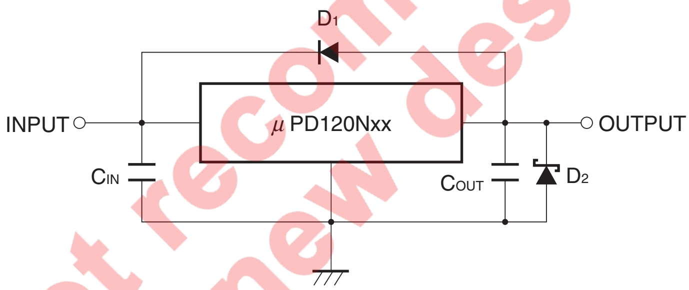
Note 1. Internally limited. When the operating junction temperature rises over 150°C, the internal circuit shuts down the output voltage.

2. Mounted on ceramic substrate of 75 mm^2 x 0.7 mm

3. Mounted on ceramic substrate of 16 cm^2 x 0.7 mm

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Typical Connection



Not recommend for new design

C_{IN}: 0.1 μF or higher. Set this value according to the length of the line between the regulator and INPUT pin. Be sure to connect C_{IN} to prevent parasitic oscillation. If using a laminated ceramic capacitor, it is necessary to ensure that C_{IN} is 0.1 μF or higher for the voltage and temperature range to be used.

C_{OUT}: 10 μF or higher. Be sure to connect C_{OUT} to prevent oscillation and improve excessive load regulation. Place C_{IN} and C_{OUT} as close as possible to the IC pins (within 2 cm). Be sure to use the capacitor of 10 μF or higher of capacity values and 1 to 8 Ω of equivalent series resistance under an operating condition.

D_1: If the OUTPUT pin has a higher voltage than the INPUT pin, connect a diode.

D_2: If the OUTPUT pin has a lower voltage than the GND pin, connect a schottky barrier diode.

Caution Make sure that no voltage is applied to the OUTPUT pin from external.

Recommended Operating Conditions

Parameter	Symbol	Type Number	MIN.	TYP.	MAX.	Unit
Input Voltage	V_{IN}	μPD120N15	3.0		5.5	V
		μPD120N18	3.2		5.5	V
		μPD120N25	4.5		5.5	V
		μPD120N33	4.5		5.5	V
Output Current	I_O	All	0		0.3	A
Operating Ambient Temperature	T_A	All	−40		+85	°C
Operating Junction Temperature	T_J	All	−40		+125	°C

Caution Use of conditions other than the above-listed recommended operating conditions is not a problem as long as the absolute maximum ratings are not exceeded. However, since the use of such conditions diminishes the margin of safety, careful evaluation is required before such conditions are used. Moreover, using the MAX. value for all the recommended operating conditions is not guaranteed to be safe.

Electrical Characteristics

μPD120N15 (T_J = 25°C, V_{IN} = 5.0 V, I_O = 0.15 A, C_{IN} = 0.1 μF, C_{OUT} = 10 μF, unless otherwise specified.)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output Voltage	V_{O1}		1.47	1.5	1.53	V
	V_{O2}	3.0 V ≤ V_{IN} ≤ 5.5 V, 0 A ≤ I_O ≤ 0.3 A	1.455	–	1.545	V
Line Regulation	REG_{IN}	3.0 V ≤ V_{IN} ≤ 5.5 V	–	1	30	mV
Load Regulation	REG_L	0 A ≤ I_O ≤ 0.3 A	–	2	30	mV
Quiescent Current	I_{BIAS}	I_O = 0 A	–	60	120	μA
Quiescent Current Change	ΔI_{BIAS}	3.0 V ≤ V_{IN} ≤ 5.5 V	–	–	25	μA
<R> Output Noise Voltage	V_n	10 Hz ≤ f ≤ 100 kHz	–	100	–	μVr.m.s.
Ripple Rejection	R•R	f = 1 kHz, 3.0 V ≤ V_{IN} ≤ 5.5 V	–	63	–	dB
Dropout Voltage	V_{DIF}	I_O = 0.15 A	–	0.6	0.9	V
		I_O = 0.3 A	–	1.0	–	V
Short Circuit Current	I_{Oshort}	V_{IN} = 5 V	–	0.2	–	A
Peak Output Current	I_{Opeak}	V_{IN} = 5 V	0.3	–	–	A
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	I_O = 0 A, 0°C ≤ T_J ≤ 125°C	–	−0.03	–	mV/°C

μPD120N18 (T_J = 25°C, V_{IN} = 5.0 V, I_O = 0.15 A, C_{IN} = 0.1 μF, C_{OUT} = 10 μF, unless otherwise specified.)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output Voltage	V_{O1}		1.764	1.8	1.836	V
	V_{O2}	3.2 V ≤ V_{IN} ≤ 5.5 V, 0 A ≤ I_O ≤ 0.3 A	1.746	–	1.854	V
Line Regulation	REG_{IN}	3.2 V ≤ V_{IN} ≤ 5.5 V	–	1	30	mV
Load Regulation	REG_L	0 A ≤ I_O ≤ 0.3 A	–	2	30	mV
Quiescent Current	I_{BIAS}	I_O = 0 A	–	60	120	μA
Quiescent Current Change	ΔI_{BIAS}	3.2 V ≤ V_{IN} ≤ 5.5 V	–	–	25	μA
<R> Output Noise Voltage	V_n	10 Hz ≤ f ≤ 100 kHz	–	120	–	μVr.m.s.
Ripple Rejection	R•R	f = 1 kHz, 3.2 V ≤ V_{IN} ≤ 5.5 V	–	63	–	dB
Dropout Voltage	V_{DIF}	I_O = 0.15 A	–	0.4	0.65	V
Short Circuit Current	I_{Oshort}	V_{IN} = 5 V	–	0.2	–	A
Peak Output Current	I_{Opeak}	V_{IN} = 5 V	0.3	–	–	A
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	I_O = 0 A, 0°C ≤ T_J ≤ 125°C	–	−0.06	–	mV/°C

Not recommend for new design

µPD120N25 (T_J = 25°C, V_{IN} = 5.0 V, I_O = 0.15 A, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, unless otherwise specified.)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output Voltage	V_{O1}		2.45	2.5	2.55	V
	V_{O2}	4.5 V ≤ V_{IN} ≤ 5.5 V, 0 A ≤ I_O ≤ 0.3 A	2.425	–	2.575	V
Line Regulation	REG_{IN}	4.5 V ≤ V_{IN} ≤ 5.5 V	–	1	30	mV
Load Regulation	REG_L	0 A ≤ I_O ≤ 0.3 A	–	2	30	mV
Quiescent Current	I_{BIAS}	I_O = 0 A	–	60	120	µA
Quiescent Current Change	ΔI_{BIAS}	4.5 V ≤ V_{IN} ≤ 5.5 V	–	–	25	µA
<R> Output Noise Voltage	V_n	10 Hz ≤ f ≤ 100 kHz	–	170	–	µVr.m.s.
Ripple Rejection	R•R	f = 1 kHz, 4.5 V ≤ V_{IN} ≤ 5.5 V	–	60	–	dB
Dropout Voltage	V_{DIF}	I_O = 0.15 A	–	0.3	0.7	V
Short Circuit Current	I_{Oshort}	V_{IN} = 5 V	–	0.2	–	A
Peak Output Current	I_{Opeak}	V_{IN} = 5 V	0.3	–	–	A
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	I_O = 0 A, 0°C ≤ T_J ≤ 125°C	–	–0.07	–	mV/°C

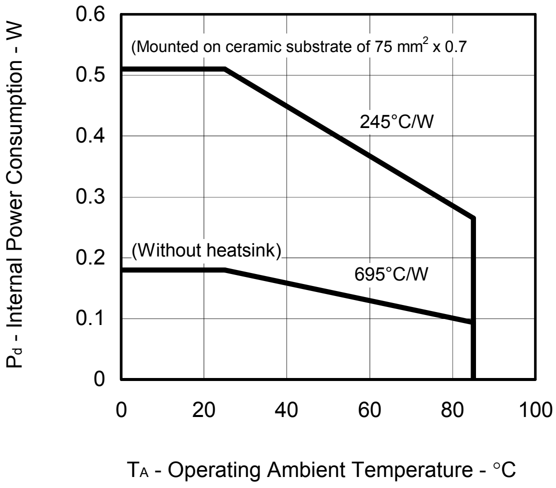
µPD120N33 (T_J = 25°C, V_{IN} = 5.0 V, I_O = 0.15 A, C_{IN} = 0.1 µF, C_{OUT} = 10 µF, unless otherwise specified.)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output Voltage	V_{O1}		3.234	3.3	3.366	V
	V_{O2}	4.5 V ≤ V_{IN} ≤ 5.5 V, 0 A ≤ I_O ≤ 0.3 A	3.201	–	3.399	V
Line Regulation	REG_{IN}	4.5 V ≤ V_{IN} ≤ 5.5 V	–	1	30	mV
Load Regulation	REG_L	0 A ≤ I_O ≤ 0.3 A	–	2	30	mV
Quiescent Current	I_{BIAS}	I_O = 0 A	–	60	120	µA
Quiescent Current Change	ΔI_{BIAS}	4.5 V ≤ V_{IN} ≤ 5.5 V	–	–	25	µA
<R> Output Noise Voltage	V_n	10 Hz ≤ f ≤ 100 kHz	–	220	–	µVr.m.s.
Ripple Rejection	R•R	f = 1 kHz, 4.5 V ≤ V_{IN} ≤ 5.5 V	–	60	–	dB
Dropout Voltage	V_{DIF}	I_O = 0.15 A	–	0.2	0.6	V
Short Circuit Current	I_{Oshort}	V_{IN} = 5 V	–	0.2	–	A
Peak Output Current	I_{Opeak}	V_{IN} = 5 V	0.3	–	–	A
Temperature Coefficient of Output Voltage	$\Delta V_O/\Delta T$	I_O = 0 A, 0°C ≤ T_J ≤ 125°C	–	–0.06	–	mV/°C

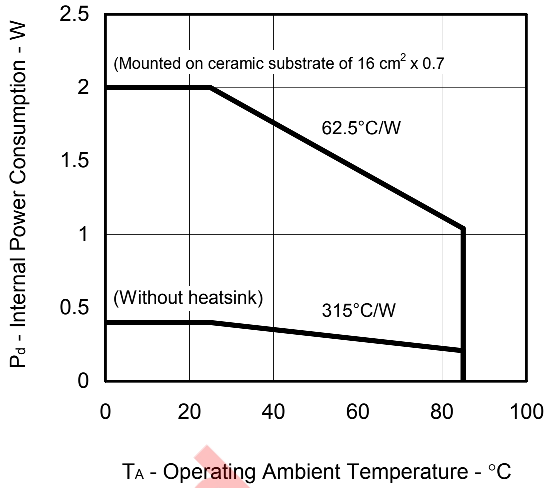
Not recommend for new design

Typical Characteristics

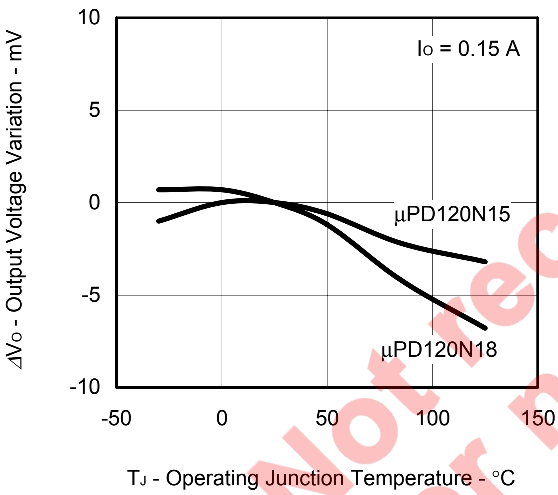
Pd vs. TA (µPD120NxxTA)



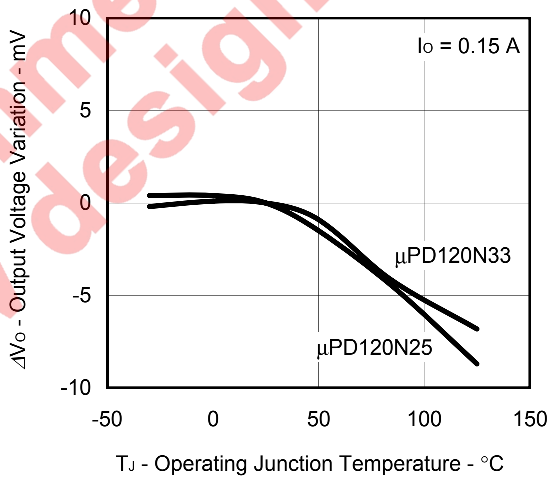
Pd vs. TA (µPD120NxxT1B)



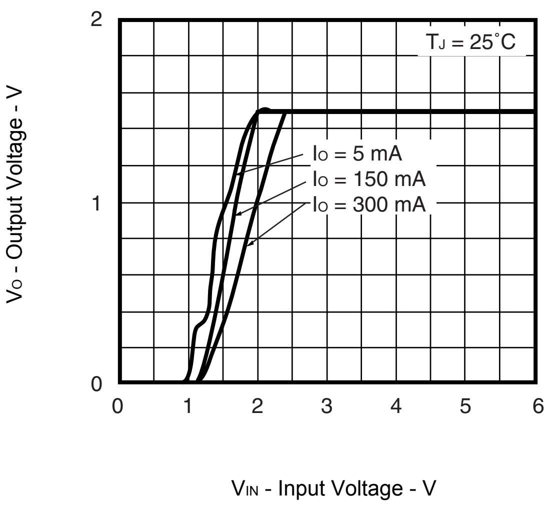
ΔVO vs. TJ



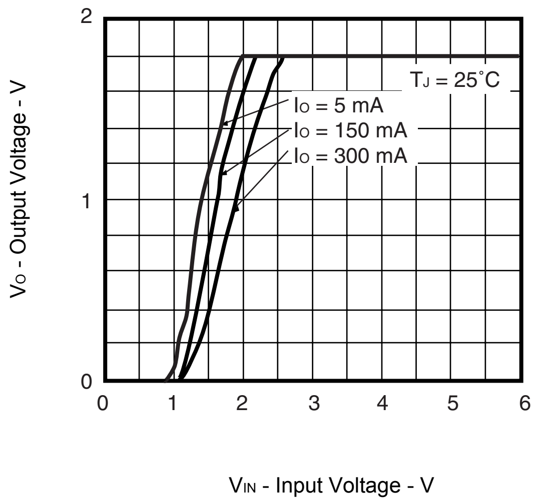
ΔVO vs. TJ



VO vs. VIN (µPD120N15)

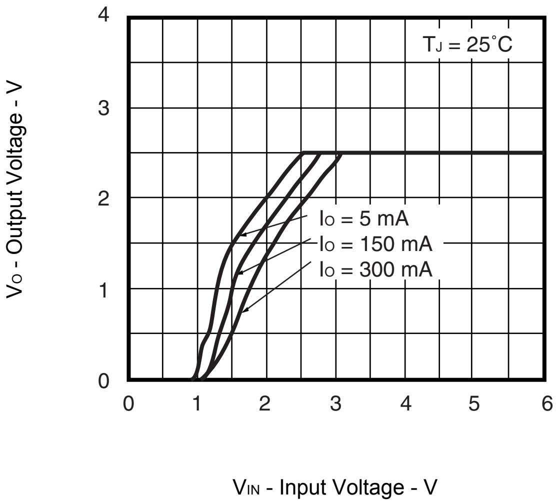


VO vs. VIN (µPD120N18)

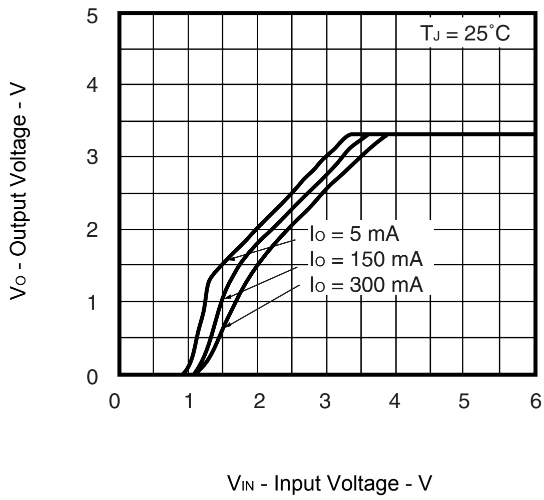


Not recommend for new design

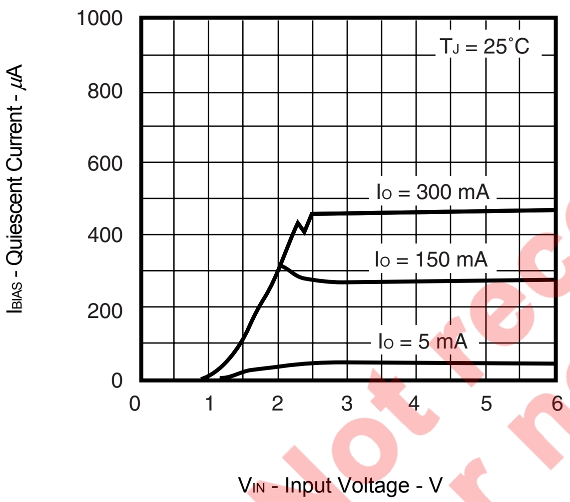
V_O vs. V_{IN} (µPD120N25)



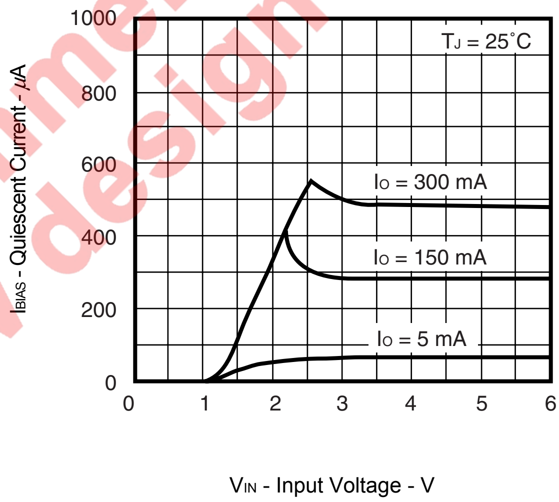
V_O vs. V_{IN} (µPD120N33)



I_{BIAS} ($I_{BIAS(S)}$) vs. V_{IN} (µPD120N15)

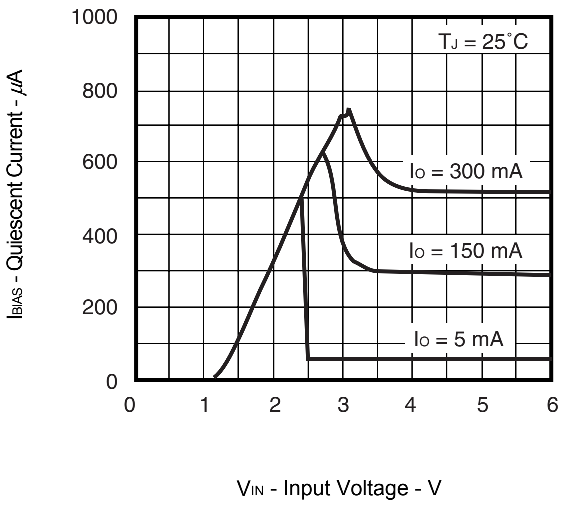


I_{BIAS} ($I_{BIAS(S)}$) vs. V_{IN} (µPD120N18)

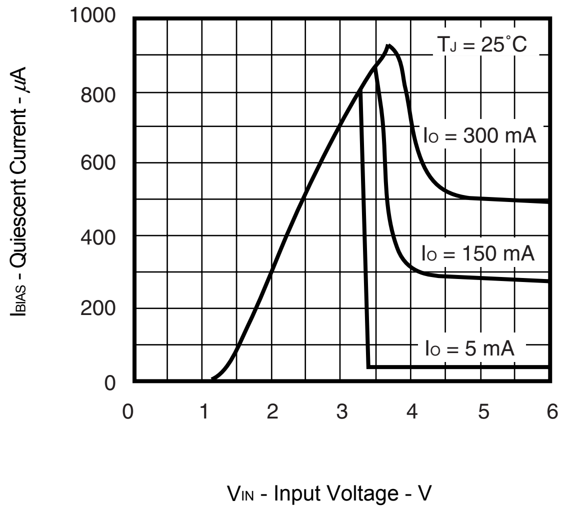


Not recommend for new design

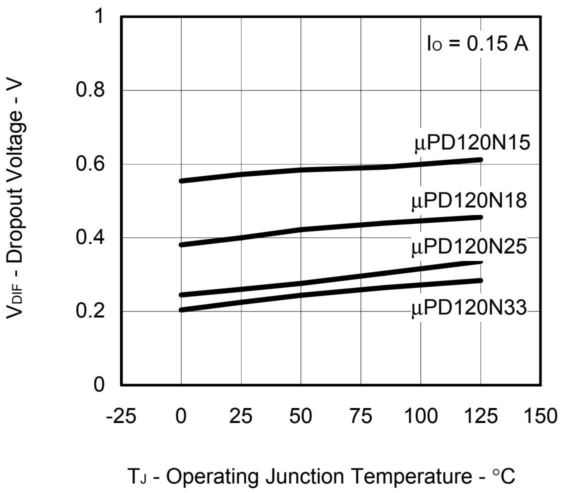
I_{BIAS} ($I_{BIAS(S)}$) vs. V_{IN} (µPD120N25)



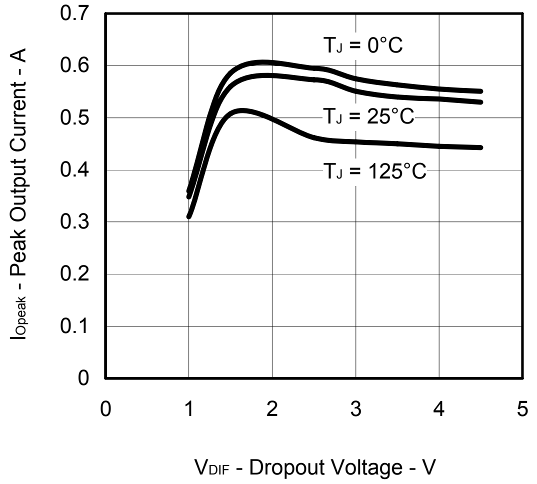
I_{BIAS} ($I_{BIAS(S)}$) vs. V_{IN} (µPD120N33)



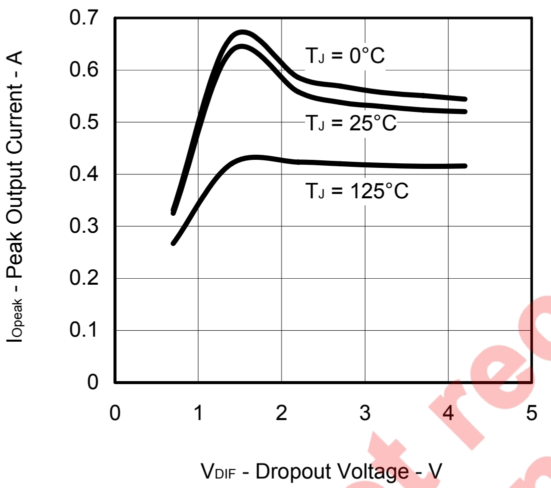
V_{DIF} vs. T_J



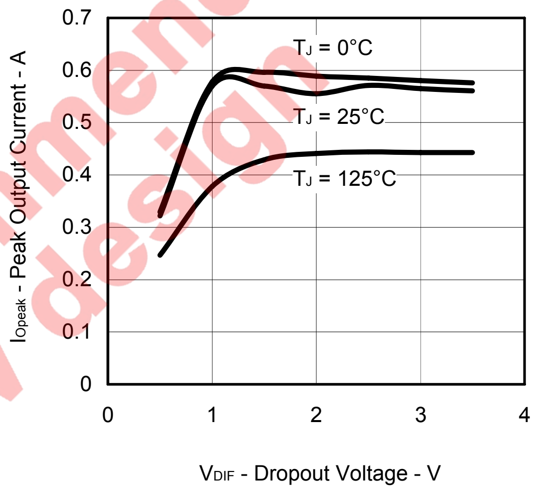
I_{Opeak} vs. V_{DIF} (µPD120N15)



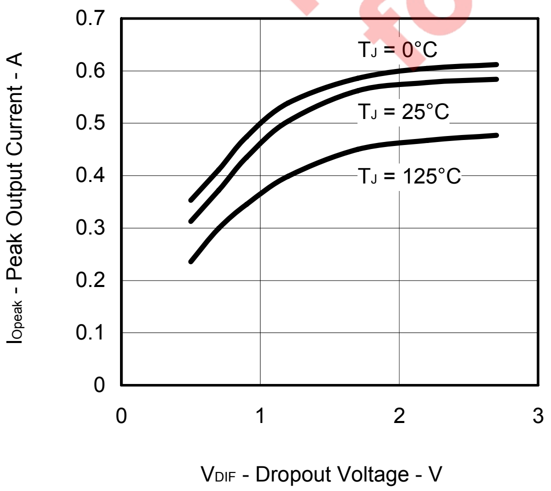
I_{Opeak} vs. V_{DIF} (µPD120N18)



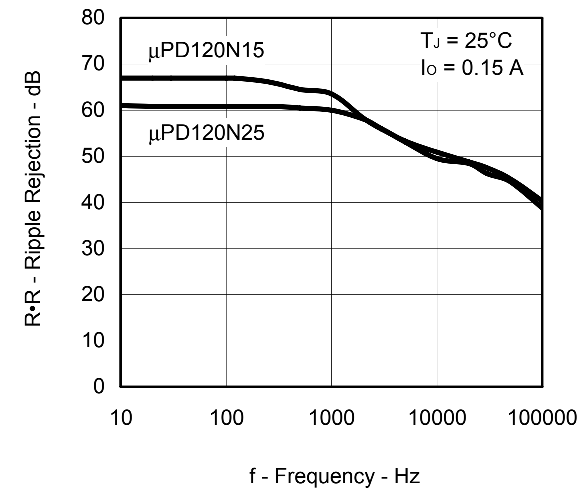
I_{Opeak} vs. V_{DIF} (µPD120N25)



I_{Opeak} vs. V_{DIF} (µPD120N33)

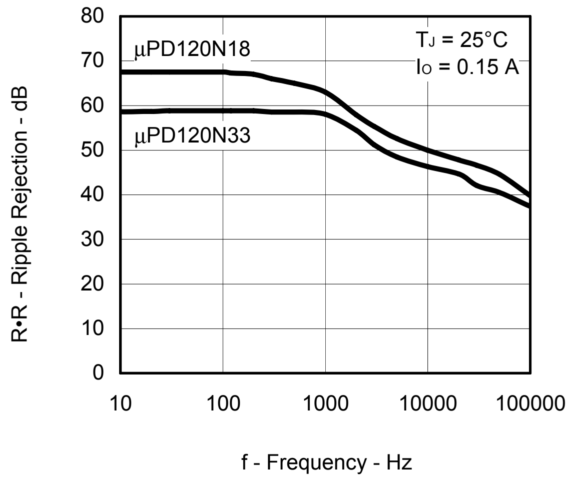


R•R vs. f

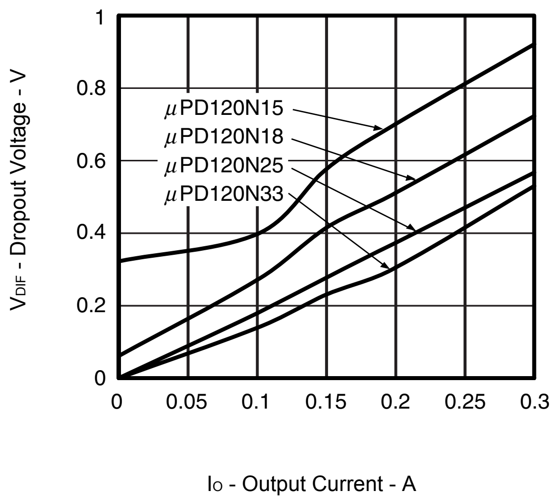


Not recommend for new design

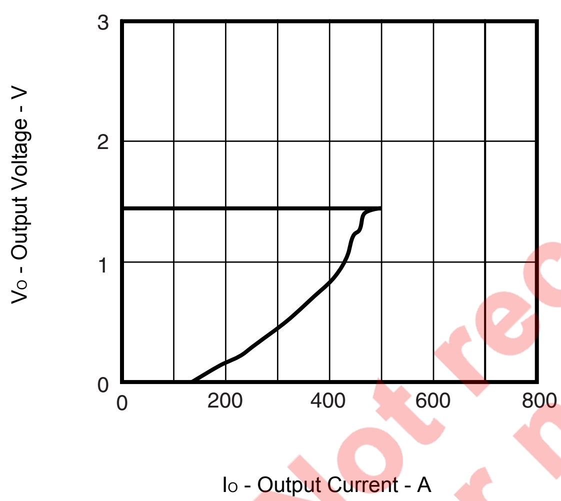
R•R vs. f



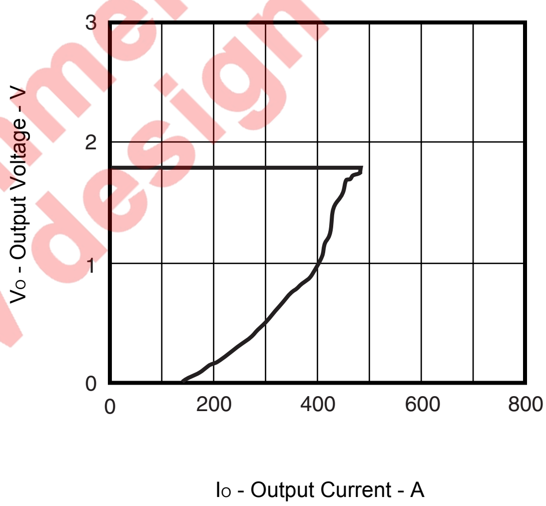
VDIF vs. Io



Vo vs. Io (μPD120N15)

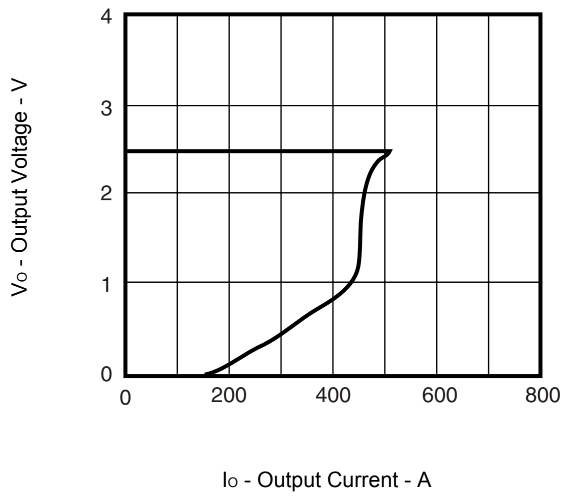


Vo vs. Io (μPD120N18)

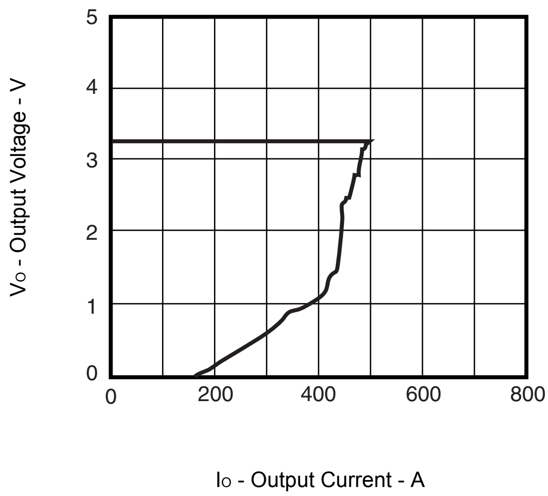


Not recommend for new design

Vo vs. Io (μPD120N25)



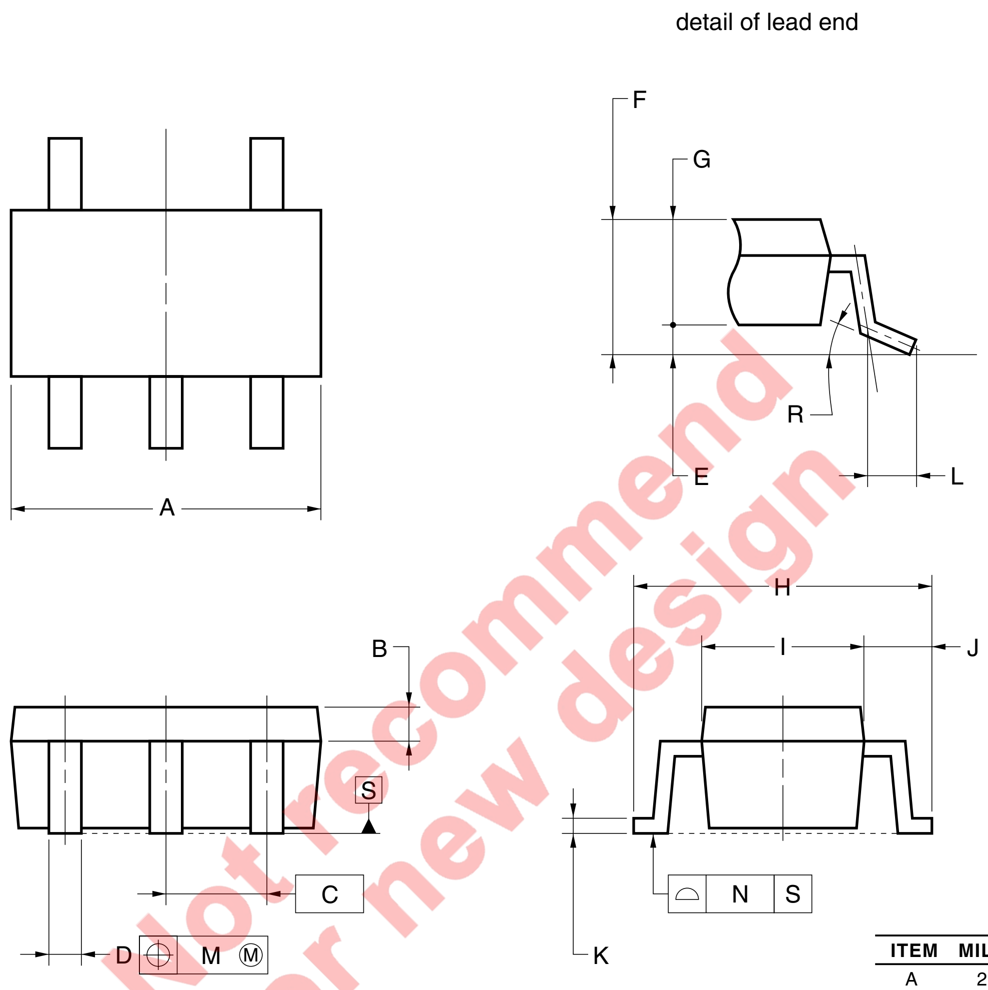
Vo vs. Io (μPD120N33)



Package Drawings (Unit: mm)

SC-74A

5 PIN PLASTIC MINI MOLD

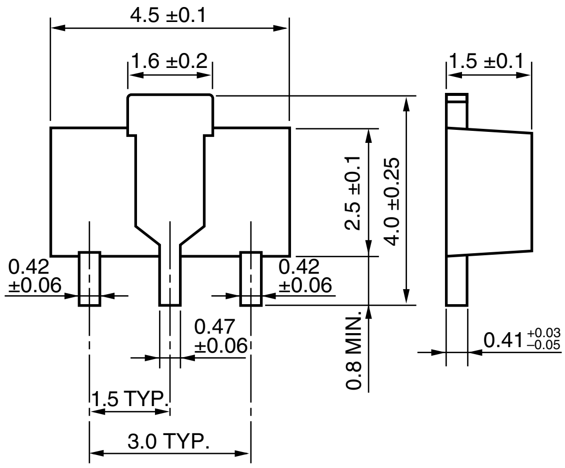


Not recommend for new design

ITEM	MILLIMETERS
A	2.9±0.2
B	0.3
C	0.95 (T.P.)
D	$0.32^{+0.05}_{-0.02}$
E	0.05±0.05
F	1.4 MAX.
G	$1.1^{+0.2}_{-0.1}$
H	2.8±0.2
I	$1.5^{+0.2}_{-0.1}$
J	$0.65^{+0.1}_{-0.15}$
K	$0.16^{+0.1}_{-0.06}$
L	0.4±0.2
M	0.19
N	0.1
R	5°±5°

S5TA-95-15A

SC-62



Not recommend for new design

<R> **Recommended Soldering Conditions**

The µPD120Nxx series should be soldered and mounted under the following recommended conditions.

For soldering methods and conditions other than those recommended below, contact a Renesas Electronics sales representative.

For technical information, see the following website.

Semiconductor Device Mount Manual (http://www.renesas.com/prod/package/manual/)

Surface Mount Device

µPD120N15TA-A, µPD120N18TA-A, µPD120N25TA-A, µPD120N33TA-A: SC-74A [Note1]
µPD120N15TA-AT, µPD120N18TA-AT, µPD120N25TA-AT, µPD120N33TA-AT: SC-74A [Note1]
µPD120N15T1B-AY, µPD120N18T1B-AY, µPD120N25T1B-AY, µPD120N33T1B-AY: SC-62 [Note2]
µPD120N15T1B-AZ, µPD120N18T1B-AZ, µPD120N25T1B-AZ, µPD120N33T1B-AZ: SC-62 [Note2]

Process	Conditions	Symbol
Infrared Ray Reflow	Peak temperature: 260°C or below (Package surface temperature), Reflow time: 60 seconds or less (at 220°C or higher), Maximum number of reflows processes: 3 times or less.	IR60-00-3
Partial Heating Method	Pin temperature: 350°C or below, Heat time: 3 seconds or less (Per each side of the device).	P350

Notes 1. Pb-free (This product does not contain Pb in external electrode and other parts.)

2. Pb-free (This product does not contain Pb in external electrode.)

Caution Do not use different soldering methods together (except for partial heating).

Remark Flux: Rosin-based flux with low chlorine content (chlorine 0.2 Wt% or below) is recommended.

Reference Documents

USER'S MANUAL USAGE OF THREE TERMINAL REGULATORS — Document No.G12702E [Note]
INFORMATION VOLTAGE REGULATOR OF SMD — Document No.G11872E [Note]
SEMICONDUCTOR PACKAGE MOUNT MANUAL — http://www.renesas.com/prod/package/index.html

Note Published by the former NEC Electronics Corporation.

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NOTES FOR CMOS DEVICES

(1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN: Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between VIL (MAX) and VIH (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between VIL (MAX) and VIH (MIN).

(2) HANDLING OF UNUSED INPUT PINS: Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

(3) PRECAUTION AGAINST ESD: A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

(4) STATUS BEFORE INITIALIZATION: Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

(5) POWER ON/OFF SEQUENCE: In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current. The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

(6) INPUT OF SIGNAL DURING POWER OFF STATE : Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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Revision History	μPD120Nxx Series Data Sheet

Rev.	Date	Description	
		Page	Summary
–	Jun 2007	–	Previous No. : S17145EJ3V0DS00
4.00	Apr 15, 2011	Throughout	Addition of Pb-free products (-AT, -AY)
		pp.4, 5	Modification of **Absolute Maximum Ratings** Output Noise Voltage 10 kHz ≤ f ≤ 100 kHz -> 10 Hz ≤ f ≤ 100 kHz

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Renesas Electronics America Inc.
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

Renesas Electronics Hong Kong Limited
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
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Renesas Electronics Malaysia Sdn.Bhd.
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
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