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1 Brief Description

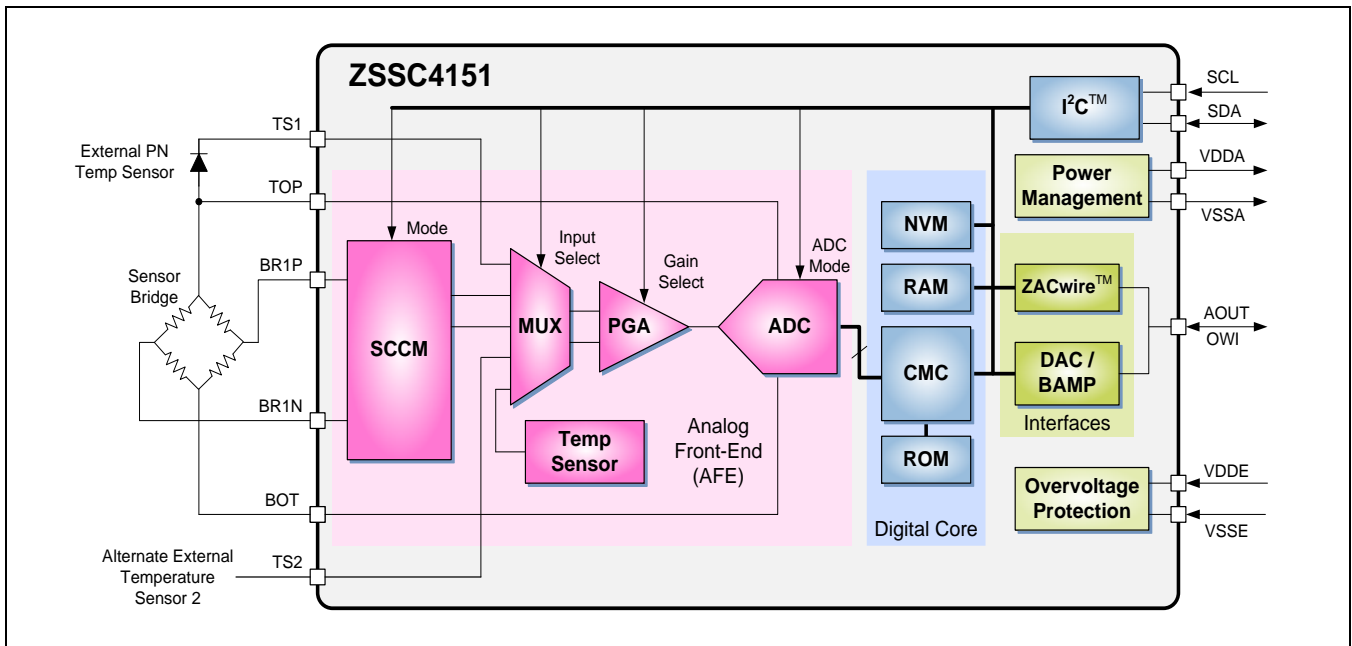
The ZSSC4151 sensor signal conditioner (SSC) is a CMOS integrated circuit for highly accurate amplification and sensor-specific correction of bridge sensor signals. Digital compensation of sensor offset, sensitivity, temperature drift, and non-linearity is accomplished via an internal 16-bit RISC microcontroller running a correction algorithm with calibration coefficients stored in an EEPROM.

The ZSSC4151 is adjustable to nearly all bridge sensor types. Measured values are provided at the analog voltage output and at the digital I²C™* or ZACwire™ interface, also referred to as the One-Wire Interface (OWI). The digital interfaces can be used for a simple PC-controlled calibration procedure in order to program a set of calibration coefficients into an on-chip EEPROM. The specific sensor and the ZSSC4151 can be quickly calibrated together. The ZSSC4151 and the calibration equipment communicate digitally, so the noise sensitivity is greatly reduced. Digital calibration helps keep assembly cost low as no trimming by external devices or lasers is needed.

The ZSSC4151 is optimized for automotive environments by overvoltage and reverse-polarity protection circuitry, excellent electromagnetic compatibility, full automotive temperature range, and multiple diagnostic features.

Figure 1.1 provides a block diagram of the ZSSC4151. Refer to section 5 for definitions of abbreviations.

Figure 1.1 ZSSC4151 Block Diagram



* I²C™ is a trademark of NXP.

2 Electrical Characteristics

Important note: The *absolute maximum ratings* given in section 2.1 are stress ratings only. The ZSSC4151 might not function or be operable above the *recommended operating conditions*. Stresses exceeding the *absolute maximum ratings* might also damage the device. In addition, extended exposure to stresses above the *recommended operating conditions* might affect device reliability. IDT does not recommend designing to the specifications given under “Absolute Maximum Ratings.”

Important note: The *operating conditions* given in section 2.2 set the conditions over which IDT specifies device operation. These are the conditions that the application circuit should provide to the device for it to function as intended. Unless otherwise noted, the limits for parameters that appear in the *operating conditions* section are used as test conditions for the limits given in the *electrical characteristics* (section 2.3), *operating conditions*, and *interface characteristics and nonvolatile memory* sections.

2.1. Absolute Maximum Ratings

Table 2.1 Absolute Maximum Ratings

| No. | Parameter | Symbol | Conditions | Min | Max | Unit |
|-------|---------------------------|-------------------|------------|------|-----------|------|
| 2.1.1 | Supply voltage | VDDE | | -40 | 40 | VDC |
| 2.1.2 | Voltage at AOUT pin | V _{AOUT} | | -40 | 40 | VDC |
| 2.1.3 | Analog supply voltage | VDDA | | -0.3 | 6.5 | VDC |
| 2.1.4 | Digital supply voltage | VDD | | -0.3 | 1.98 | VDC |
| 2.1.5 | Voltage at all other pins | V _{PIN} | | -0.3 | VDDA +0.3 | V |
| 2.1.6 | Storage temperature | T _{STG} | | -55 | 160 | °C |

2.2. Operating Conditions

All voltages in this section are relative to VSSA.

Table 2.2 Operating Conditions

Note: See important notes at the end of the table.

| No. | Parameter | Symbol | Conditions | Min | Typical | Max | Unit |
|-------|-------------------------------------|-----------------------|--|--------------|---------|------|------|
| 2.2.1 | Supply voltage | VDDE | To VSSE | 4.5 | 5 | 5.5 | V |
| | | VDDA | To VSSA VDDE minus drop through protection switch | (VDDE – 0.1) | | VDDE | V |
| 2.2.2 | Junction temperature | T _{TQE} | Extended Temperature Range (TQE) | -40 | | 150 | °C |
| | | T _{AMB_TQA} | Advanced-Performance Temperature Range (TQA) | -40 | | 125 | °C |
| | | T _{AMB_TQI} | Best-Performance Temperature Range (TQI) | -25 | | 85 | °C |
| 2.2.3 | Bridge resistance ^{1), 2)} | R _{BR} | | 2 | | 10 | kΩ |
| | | R _{BR_10-90} | Output range 10-90% | 1 | | 15 | kΩ |

1) No measurement in mass production; parameter is guaranteed by design and/or quality observation.
2) R_{BR} greater than the maximum limit results in higher noise.

2.3. Electrical Parameters

All parameter values in this section are valid under the operating conditions specified in section 2.2. All voltages referenced to VSSA.

Note: All parameters measured/validated for $r_{ADC} = 14$ -bit; segmentation of 1st and 2nd ADC stage = 8/6; $f_{OSC} = 8$ MHz; analog gain = ~ 100 ; T_{AMB_TQE} (see specification 2.2.2).

Table 2.3 Electrical Parameters

Note: See important table notes at the end of the table (page 7).

| No. | Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--|--|----------------|--|------|-----|------|-----------------------|
| 2.3.1. Supply Current and System Operation Conditions | | | | | | | |
| 2.3.1.1 | Supply current ¹⁾ | I_S | Oscillator adjusted (typical $f_{OSC} = 8$ MHz). | | 5.5 | 7 | mA |
| 2.3.1.2 | Sensor bridge supply voltage | V_{SENS} | $V_{SENS} = V_{TOP} - V_{BOT}$ at $R_{BR} \geq 2k\Omega$ | 0.9 | | 1 | VDDA |
| 2.3.1.3 | Oscillator frequency ²⁾ | f_{OSC} | | 7.2 | 8 | 8.8 | MHz |
| 2.3.1.4 | Oscillator frequency temperature coefficient | TC_{OSC} | | -200 | | 200 | ppm/K |
| 2.3.2. Analog Front-End Characteristics | | | | | | | |
| 2.3.2.1 | Input span | V_{IN_SPAN} | Analog gain = 1 to 200 | 1 | | 800 | mV/V |
| 2.3.2.2 | Common mode input range | V_{IN_CM} | Depends on gain adjustment | 0.25 | | 0.75 | V_{SENS} |
| 2.3.2.3 | External capacitance at input | C_{IN_EXT} | Capacitance at pins BR1P and BR1N to VSSA | 0 | | 12 | nF |
| 2.3.2.4 | Input leakage current ³⁾ | I_{IN_leak} | | -15 | | 15 | nA |
| 2.3.3. Temperature Measurement | | | | | | | |
| 2.3.3.1 | PTAT internal temperature sensitivity | ST_{TSI} | Raw values, without conditioning calculation Analog gain setting= 6 | 20 | | | LSB ₁₄ /K |
| 2.3.3.2 | External temperature diode channel gain | A_{TSE_D} | | 10 | | | LSB ₁₄ /mV |
| 2.3.3.3 | External temperature diode bias current | I_{TSE_D} | | 10 | 20 | 40 | μ A |
| 2.3.3.4 | External temperature diode input range ³⁾ | V_{TSE_D} | Relative to V_{TOP} | -1 | | -0.2 | V |

| No. | Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--|--|------------------------|---|------|-----|------|-------------------|
| 2.3.3.5 | External RTD channel gain | ATSE_RTD | | 10 | | | LSB/mV |
| 2.3.3.6 | External RTD input range ³⁾ | V _{TSE_RTD} | Relative to VDDA | -2 | | -0.2 | V |
| 2.3.4. Sensor Diagnostics | | | | | | | |
| 2.3.4.1 | Sensor connection loss threshold | R _{SCC_open} | | 100 | | | kΩ |
| 2.3.4.2 | Sensor short threshold to BOT or TOP pin | R _{SCC_SH_BT} | | | | 50 | Ω |
| 2.3.4.3 | Sensor short threshold between inputs | R _{SCC_SH_IN} | | | | 150 | Ω |
| 2.3.5. A2D Conversion | | | | | | | |
| 2.3.5.1 | ADC resolution ³⁾ | r _{ADC} | Selection: 12, 14, 16 or 18 bit | 12 | | 18 | Bit |
| 2.3.5.2 | DNL ³⁾ | DNL _{ADC} | Best fit; overall AFE; V _{ADC_IN} according to 2.3.6.4. | | | 0.95 | LSB |
| 2.3.5.3 | INL TQA temperature range (specified in 2.2.2) ³⁾ | INL _{ADC_TQA} | Best fit | | | 4 | LSB |
| 2.3.5.4 | INL TQE temperature range (specified in 2.2.2) | INL _{ADC_TQE} | At 14-bit resolution | | | 8 | LSB |
| 2.3.5.5 | ADC input range | V _{ADC_IN} | | 0.1 | | 0.9 | V _{SENS} |
| 2.3.6. DAC and Analog Output (AOUT Pin) | | | | | | | |
| 2.3.6.1 | DAC resolution | r _{DAC} | Analog output | | 12 | | Bit |
| 2.3.6.2 | Output current sink/source | I _{OUT} | V _{AOUT} : 5-95%, R _{LOAD} ≥ 5kΩ | | | 2.5 | mA |
| | | | V _{AOUT} : 10-90%, R _{LOAD} ≥ 1kΩ | | | 5 | mA |
| 2.3.6.3 | Short-circuit current (AOUT to VSSE or VDDE) | I _{OUT_max} | Short to VSSE or VDDE | -25 | | 25 | mA |
| 2.3.6.4 | Addressable output range | V _{R_OUT} | | 0.01 | | 0.99 | VDDE |
| 2.3.6.5 | Load capacitance | C _{LOAD} | Defined for best EMC performance | 4 | 10 | 150 | nF |
| 2.3.6.6 | Output slew rate | SR _{OUT} | C _{LOAD} < 50nF | 0.1 | | | V/μs |
| 2.3.6.7 | Clipping levels | LowLim | Configurable 8-bit value stored in NVM | 0 | | 25 | %VDDE |
| | | UppLim | Configurable 8-bit value stored in NVM | 75 | | 100 | %VDDE |
| 2.3.6.8 | Clipping adjustment step | | | | | 0.1 | %VDDE |
| 2.3.6.9 | Output resistance in Diagnostic Mode | R _{OUT_DIA} | Diagnostic Range: 4% to 96%, R _{LOAD} ≥ 5kΩ 8% to 92%, R _{LOAD} ≥ 1kΩ | | | 80 | Ω |

| No. | Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--|---|------------------------|--|-------|------|------|-------|
| 2.3.6.10 | DNL | DNL _{OUT} | r _{DAC} =12 bit | -1.5 | | 1.5 | LSB |
| 2.3.6.11 | INL TQA temperature range (specified in 2.2.2) ³⁾ | INL _{OUT} | Best fit, r _{DAC} =12-Bit | -5 | | 5 | LSB |
| 2.3.6.12 | INL TQE temperature range (specified in 2.2.2) | INL _{OUT} | Best fit, r _{DAC} =12-Bit | -8 | | 8 | LSB |
| 2.3.6.13 | Output leakage current at 125°C | I _{LEAK_OUT} | In the event of power or ground loss | -12 | | 12 | μA |
| 2.3.6.14 | Output leakage current at 150°C | I _{LEAK_OUT} | In the event of power or ground loss | -20 | | 20 | μA |
| 2.3.7. System Response | | | | | | | |
| 2.3.7.1 | Startup time ^{3), 4)} (time to first valid output after power-on) | t _{STARTUP} | f _{OSC} = 8MHz; ADC: 14-bit and 2 nd order conversion | | | 5 | ms |
| 2.3.7.2 | Response time ^{3) 4) 5)} | t _{RESPONSE} | 100% input step, excluding transmission time | | | 1.1 | ms |
| 2.3.7.3 | Bandwidth ³⁾ | | In comparison to analog signal conditioners; 66% jump | | 1 | | kHz |
| 2.3.7.4 | Analog output noise peak-to-peak ³⁾ | V _{NOISE,PP} | DAC and output buffer only; bandwidth ≤ 10kHz | | | 10 | mV |
| 2.3.7.5 | Analog output noise RMS ³⁾ | V _{NOISE,RMS} | DAC and output buffer only; bandwidth ≤ 10kHz | | | 3 | mV |
| 2.3.7.6 | Ratiometricity error ³⁾ | RE _{OUT_5} | Maximum error of VDDE range = 4.5V to 5.5V | -1000 | | 1000 | ppm |
| 2.3.7.7 | Overall error ⁶⁾ | F _{ALL} | TQA temperature range (specified in 2.2.2) | | 0.35 | | % FSO |
| | | | TQE temperature range (specified in 2.2.2) | | 0.5 | | |
| 1) Excluding bridge supply current and excluding output current at AOUT pin. 2) Oscillator frequency can be trimmed via a setting in nonvolatile memory (NVM). 3) No measurement in mass production; parameter is guaranteed by design and/or quality observation. 4) No bridge settling included in timing. 5) Dependent on the configuration. The specified limit is valid only for ADC resolutions ≤15 bits. 6) FSO: full-scale output. No sensor-caused effects included in overall error. ADC input range from 10% to 90% of V _{SENS} ; DAC from 5% to 95% of output range. | | | | | | | |

2.4. Interface Characteristics and Nonvolatile Memory

Table 2.4 Interface Characteristics and Nonvolatile Memory

Note: See important table notes at the end of the table.

| No. | Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|---|--|---------------------------|--|-------|------|-------|------------------------|
| 2.4.1. I²C™ Interface | | | | | | | |
| 2.4.1.1 | I ² C™ voltage level HIGH ¹⁾ | V _{I2C_HIGH} | | 0.5 | | | VDDA |
| 2.4.1.2 | I ² C™ voltage level LOW ¹⁾ | V _{I2C_LOW} | | | | 0.2 | VDDA |
| 2.4.1.3 | Slave output level LOW ¹⁾ | V _{I2C_LOW_OUT} | Open drain, I _{OL} < 4mA | | | 0.1 | VDDA |
| 2.4.1.4 | SDA load capacitance ¹⁾ | C _{I2C_SDA} | | | | 400 | pF |
| 2.4.1.5 | SCL clock frequency ¹⁾ | f _{I2C} | | | | 400 | kHz |
| 2.4.1.6 | Internal pull-up resistor ¹⁾ | R _{I2C_PULLUP} | | 25 | | 100 | kΩ |
| 2.4.2. ZACwire™ One-Wire Interface (OWI at AOUT pin) | | | | | | | |
| 2.4.2.1 | OWI voltage level HIGH ¹⁾ | V _{OWI_IN_H} | Master to slave | 0.75 | | | VDDE |
| 2.4.2.2 | OWI voltage level LOW ¹⁾ | V _{OWI_IN_L} | Master to slave | | | 0.2 | VDDE |
| 2.4.2.3 | Slave output level LOW ¹⁾ | V _{OWI_OUT_L} | Open drain, I _{OL} ≤ 2mA | | | 0.1 | VDDE |
| 2.4.2.4 | Start window ¹⁾ | t _{OWI_STARTWIN} | | 100 | | 300 | ms |
| 2.4.2.5 | Bus free time | t _{OWI_IDLE} | Between stop and next start | 25 | | | μs |
| 2.4.2.6 | Hold time start condition | t _{OWI_START} | Valid minimum f _{clk} | 25 | | | μs |
| 2.4.2.7 | Bit time | t _{OWI_BIT} | Maximum range | 20 | | 8000 | μs |
| | | | Typical operating range | 40 | | 4000 | μs |
| 2.4.2.8 | Duty ratio bit '0' | t _{OWI_0} | | 0.125 | 0.25 | 0.375 | t _{OWI_BIT} |
| 2.4.2.9 | Duty ratio bit '1' | t _{OWI_1} | | 0.625 | 0.75 | 0.875 | t _{OWI_BIT} |
| 2.4.2.10 | Hold time stop condition | t _{OWI_STOP} | t _{OWI_BIT_L} is the bit time of the last valid bit | 2 | | | t _{OWI_BIT_L} |
| 2.4.2.11 | Bit period deviation | t _{OWI_BIT_DEV} | | 0.55 | 1.0 | 1.5 | t _{OWI_BIT} |

| No. | Parameter | Symbol | Conditions | Min | Typ | Max | Unit |
|--|--|----------------------|---|-----|-----|-----|------|
| 2.4.3. Nonvolatile Memory (NVM) | | | | | | | |
| 2.4.3.1 | Junction temperature for NVM programming ²⁾ | T _{AMB_NVM} | | -40 | | 150 | °C |
| 2.4.3.2 | Re-write cycles ¹⁾ | N _{NVM_TQA} | For T _{TQA} (see range in specification 2.2.2) | 100 | | | |
| 2.4.3.3 | Re-write cycles at 150°C | N _{NVM_TQE} | For T _{TQE} (see range in specification 2.2.2) | 10 | | | |
| 2.4.3.4 | Data retention ¹⁾ | t _{NVM_RET} | Temperature profile: 22h bake at 250°C | 15 | | | Year |
| 2.4.3.5 | Programming time ¹⁾ | t _{NVM_WRI} | Per written word | | 2.2 | 5 | ms |
| ¹⁾ No measurement in mass production; parameter is guaranteed by design and/or quality observation. ²⁾ Valid for dice. Note: Additional package and temperature range cause restrictions. | | | | | | | |

3 ESD Protection and EMC Specification

3.1. ESD Protection

All pins have an ESD protection of $\geq 2000V$ according to the Human Body Model (HBM, based on MIL883, Method 3015.7). The VDDE, VSSE, and AOUT pins have an additional ESD protection of $\geq 4000V$ (HBM).

In addition, Charged Device Model (CDM) tests are processed with protection levels of $\geq 750V$ for corner pins and $\geq 500V$ for all other pins.

The level of ESD protection has been tested with devices in QFN24 4X4mm packages during the product qualification.

3.2. Latch-Up Immunity

All pins pass $\pm 100mA$ latch-up test based on testing that conforms to the standard EIA/JESD 78.

3.3. Electromagnetic Emission

The wired emission of externally connected pins of the device is measured according to the following standard: *IEC 61967_4:2002 + A1:2006*.

Measurements must be performed with the application circuits described in the *ZSSC4151 Application Description*.

For the off-board pins, the spectral power measured with the 150Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 code H10kN*. For the VSSE pin, the spectral power measured with the 1Ω method must not exceed the limits according to *IEC 61967_4k, Annex B.4 code 15KmO*.

3.4. Conducted Susceptibility (DPI)

The conducted susceptibility of externally connected pins of the device is measured according to the IEC 62132-4 standard, which describes the direct power injection (DPI) test method.

Measurements must be performed with the application circuit described in the *ZSSC4151 Application Description*.

Measurements are performed with an internal reference capacitor and internal temperature sensor. The sensing element is replaced by a resistive divider. Calibration is parameterized so that $\sim 50\%$ VDDA is output.

Table 3.1 gives the specifications for the DPI tests. RES refers to the coupling impedance.

Table 3.1 Conducted Susceptibility (DPI) Tests

| Test | Frequency Range | Target (dBm) | Load Pins | Protocol | Error Band | Comment |
|---------------------|-------------------|--------------|------------|------------|------------|--|
| DPI, direct coupled | 1MHz to 300MHz | 26 | VDDE, AOUT | Analog out | $\pm 1\%$ | LOAD RES = $5k\Omega$ LOAD CAP = $10nF$ |
| DPI, direct coupled | 300MHz to 1000MHz | 32 | VDDE, AOUT | Analog out | $\pm 1\%$ | LOAD RES = $5k\Omega$ LOAD CAP = $10nF$ |

4 Reliability and RoHS Conformity

The ZSSC4151 is qualified according to the AEC-Q100 standard, operating temperature grade 0. The qualification is extended to 3000h for the High Temperature Operating Life (HTOL) Test for one lot. Two manufacturing lots of extended HTOL qualification data (minimum of 3000h test time) for the ZSSC4151 or other products using identical technology (metallization), the same package supplier, the same package style, and the same die size within a specific tolerance are used to prove the package and bond reliability in the range of 3000h HTOL.

A FIT rate ≤ 10 FIT (temperature = 55°C, confidence level = 60%) is guaranteed. A typical FIT rate of TSMC's CV018BCD technology, which is used for the ZSSC4151, is 1 FIT.

The ZSSC4151 complies with the RoHS directive and does not contain hazardous substances.

5 Glossary

| Term | Description |
|-------------------|---|
| ADC | Analog-to-Digital Converter |
| AEC | Automotive Electronics Council |
| AFE | Analog Front-End |
| BAMP | Buffer Amplifier |
| BR | Bridge Sensor |
| CDM | Charged Device Model |
| CM | Command Mode |
| CMC | Calibration Microcontroller |
| DAC | Digital-to-Analog Converter |
| DNL | Differential Nonlinearity |
| DPI | Direct Power Injection |
| EMC | Electromagnetic Compatibility |
| ESD | Electrostatic Discharge |
| FIT | Failures in Time |
| FSO | Full Scale Output |
| HBM | Human Body Model |
| HTOL | High Temperature Operating Life |
| I ² C™ | Inter-Integrated Circuit—serial two-wire data bus, trademark of NXP |
| INL | Integral Nonlinearity |
| LSB | Least Significant Bit |
| MUX | Multiplexer |
| NVM | Nonvolatile Memory |

| Term | Description |
|---------------|---|
| OWI | One-Wire Interface |
| PGA | Programmable Gain Amplifier |
| PTAT | Proportional-to-Absolute Temperature |
| PTC | Thermistor – Positive Temperature Coefficient Resistor |
| PWR | Power Management and Protection Unit |
| QFN | Quad-Flat No-Leads – IC package |
| RAM | Random Access Memory |
| RISC | Reduced Instruction Set Computing |
| ROM | Read-Only Memory |
| RMS | Root-Mean-Square |
| RTD | Resistance Temperature Device |
| SCCM | Sensor Check and Common Mode Adjustment Unit |
| SCL | Serial Clock |
| SDA | Serial Data |
| SSC | Sensor Short Check (diagnostic feature) or Sensor Signal Conditioner |
| TQA, TQE, TQI | Temperature range identifier. See specification 2.2.2 for definition. |
| ZACwire™ | IDT-specific One-Wire Interface |

6 Document Revision History

| Revision | Date | Description |
|----------|--------------------|---|
| 1.00 | September 13, 2015 | First release. |
| 1.01 | November 10, 2015 | Extended leakage current description in section 2.3.6 for specifications 2.3.6.13 and 2.3.6.14 Updates for table notes for Table 2.3. Revision of pin names BRP to BR1P and BRN to BR1N. |
| 1.02 | April 12, 2016 | Added minimum value for ratiometricity error in Table 2.3. Updated section 4 regarding completion of AEC-Q100 qualification and extension of the minimum test time to 3000h. Updated specification 2.3.7.7 for improved accuracy of $\pm 0.35\%$ of FSO at -40°C to 125°C and 0.5% FSO at -40°C to 150°C . |
| | April 20, 2016 | Changed to IDT branding. |

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