24V, 3A, 500kHz, ACOT™ Step-Down Converter in 8 Pin TSOT-23

General Description

The RT6217A/B is a simple, easy-to-use, 3A synchronous step-down DC-DC converter with an input supply voltage range of 4.5V to 24V. The device build-in an accurate 0.791V reference voltage and integrates low $R_{DS(ON)}$ power MOSFETs to achieve high efficiency in a TSOT-23-8 (FC) package.

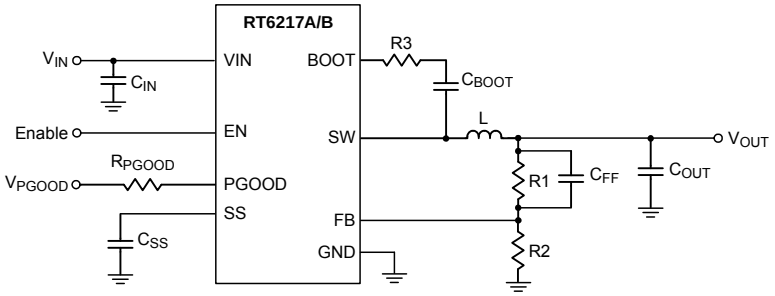
The RT6217A/B adopts Advanced Constant On-Time (ACOT™) control architecture to provide an ultrafast transient response with few external components and to operate in nearly constant switching frequency over the line, load, and output voltage range. The RT6217A operates in automatic PSM that maintains high efficiency during light load operation. The RT6217B operates in Forced PWM that helps meet tight voltage regulation accuracy requirements.

The RT6217A/B senses both FETs current for a robust over-current protection. It features cycle-by-cycle current limit protection and prevent the device from the catastrophic damage in output short circuit, over current or inductor saturation. An externally adjustable soft-start function prevents inrush current during start-up. The device also includes input under-voltage lockout, output under-voltage protection, and over-temperature protection (thermal shutdown) to provide safe and smooth operation in all operating conditions. The RT6217A/B is offered in a TSOT-23-8(FC) package.

Features

- **3A Converter With Built-in 85mΩ/40mΩ Low $R_{DS(ON)}$ Power FETs**
- **Input Supply Voltage Range : 4.5V to 24V**
- **Output Voltage Range : 0.791V to 6V**
- **Advanced Constant On-Time (ACOT™) Control**
- **Ultrafast Transient Response**
- **No Needs For External Compensations**
- **Optimized for Low-ESR Ceramic Output Capacitors**
- **0.791V ±1.5% High-Accuracy Feedback Reference Voltage**
- **Low Quiescent Current (150μA typ.)**
- **Both HS/LS FETs Protection for Robust Over-Current Protection**
- **Optional for Operation Modes :**
  - **Power Saving Mode (PSM) at Light Load (RT6217A)**
  - **Forced PWM Mode (RT6217B)**
- **Light-load V_{OUT} Ripple Reduction Technology in PSM**
- **Steady Switching Frequency (500kHz typ.)**
- **Externally Adjustable Soft-Start**
- **Monotonic Start-up for Pre-biased Output**
- **Input Under-Voltage Lockout (UVLO)**
- **Output Under-Voltage Protection (UVP) with Hiccup Mode**
- **Over-Temperature Protection (OTP) (Thermal Shutdown)**
- **Power Good Indication**
- **Enable Control**
- **RoHS Compliant and Halogen Free**
- **Available In TSOT-23-8 (FC) Package**

Simplified Application Circuit



Ordering Information

RT6217A/B □□□

- Package Type
  J8F : TSOT-23-8 (FC)
- Lead Plating System
  G : Green (Halogen Free and Pb Free)
- UVP Option
  H : Hiccup
- PSM/PWM
  A : PSM/PWM
  B : Forced PWM

Note :

Richtek products are :

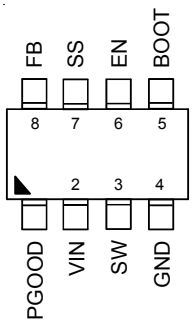
- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Applications

- Set Top Box
- Portable TV
- Access Point Router
- DSL Modem
- LCD TV

Pin Configuration

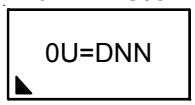
(TOP VIEW)



TSOT-23-8 (FC)

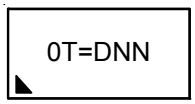
Marking Information

RT6217AHGJ8F



0U= : Product Code
DNN : Date Code

RT6217BHGJ8F

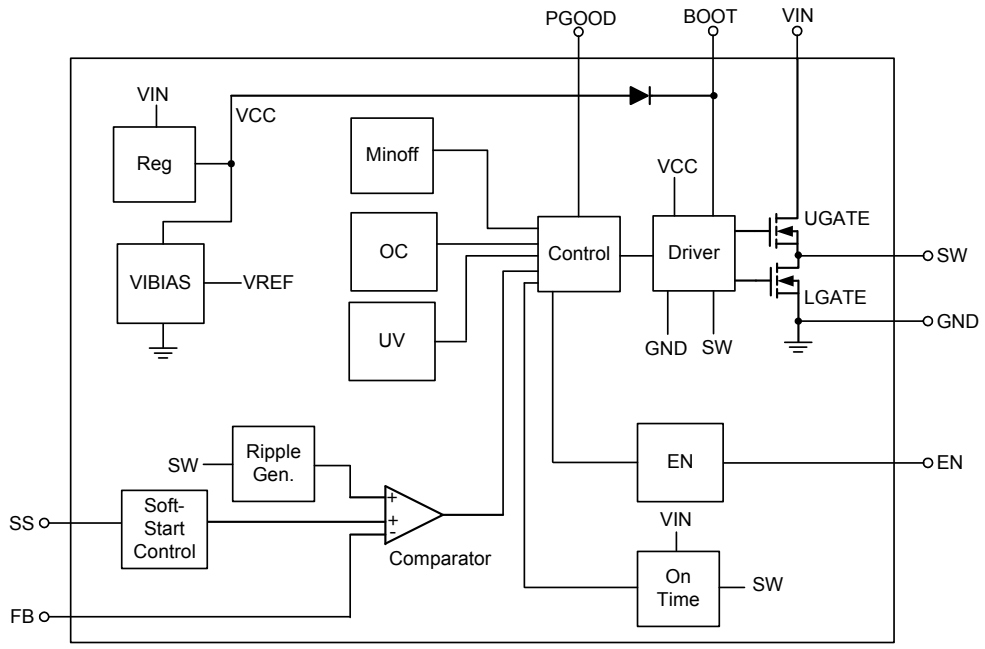


0T= : Product Code
DNN : Date Code

Functional Pin Description

Pin No.	Pin Name	Pin Function
1	PGOOD	Open-drain power-good indication output. Once being started-up, PGOOD will be pulled low to GND if any internal protection is triggered except current limit protection.
2	VIN	Power input. The input voltage range is from 4.5V to 24V. Connect a suitable input capacitor between this pin and GND, usually two 10μF or larger ceramic capacitors with a typical capacitance 22μF.
3	SW	Switch node between the internal switch and the synchronous rectifier. Connect this pin to the inductor and bootstrap capacitor.
4	GND	Power ground.
5	BOOT	Bootstrap capacitor connection node to supply the high-side gate driver. Connect a 0.1μF ceramic capacitor between this pin and SW pin.
6	EN	Enable control input. A logic-high enables the converter; a logic-low forces the device into shutdown mode.
7	SS	Soft-start capacitor connection node. Connect an external capacitor between this pin and ground to set the soft-start time. Do not leave this pin unconnected. A capacitor of 2.8nF to 100nF is suggested.
8	FB	Feedback voltage input. Connect this pin to the midpoint of the external feedback resistive divider to set the output voltage of the converter to the desired regulation level. The device regulates the FB voltage at Feedback Threshold Voltage, typically 0.791V.

Functional Block Diagram



Operation

The RT6217A/B is a high-efficiency, synchronous step-down DC-DC converter that can deliver up to 3A output current from a 4.5V to 24V input supply. The RT6217A/B adopts ACOT™ control mode, which can reduce the output capacitance and provide ultrafast transient responses, and allow minimal components sizes without any additional external compensation network.

Enable Control

The RT6217A/B provides an EN pin, as an external chip enable control, to enable or disable the device. If V_{EN} is held below a logic-low threshold voltage ($V_{ENH} - \Delta V_{EN}$) of the enable input (EN), the converter will enter into shutdown mode, that is, the converter is disabled and switching is inhibited even if the VIN voltage is above VIN under-voltage lockout threshold (V_{UVLO}). During shutdown mode, the supply current can be reduced to I_{SHDN} (10μA or below). If the EN voltage rises above the logic-high threshold voltage (V_{ENH}) while the V_{IN} voltage is higher than UVLO threshold (V_{UVLO}), the device will be turned on, that is, switching being enabled and soft-start sequence being initiated.

Input Under-Voltage Lockout

In addition to the EN pin, the RT6217A/B also provides enable control through the VIN pin. It features an under-voltage lockout (UVLO) function that monitors the internal linear regulator (VCC). If V_{EN} rises above V_{ENH} first, switching will still be inhibited until the VIN voltage rises above V_{UVLO}. It is to ensure that the internal regulator is ready so that operation with not- fully-enhanced internal MOSFET switches can be prevented. After the device is powered up, if the input voltage V_{IN} goes below the UVLO-falling threshold voltage ($V_{UVLO} - \Delta V_{UVLO}$), this switching will be inhibited; if V_{IN} rises above the UVLO-rising threshold (V_{UVLO}), the device will resume switching.

Low-Side Current-Limit Protection

The RT6217A/B features cycle-by-cycle valley-type current-limit protection, measuring the inductor current through the synchronous rectifier (low-side switch). The inductor current level is determined by measuring the low-side switch voltage between the SW pin and GND, which is proportional to the switch current, during the low-side on-time. For greater accuracy, temperature compensation is added to the voltage sensing. Once the current rises above the low-side switch valley current limit (I_{LIM_L}), the

on-time one-shot will be inhibited until the inductor current ramps down to the current limit level (I_{LIM_L}), that is, another on-time can only be triggered when the inductor current goes below the low-side current limit. This function can prevent the average output current from greatly exceeding the guaranteed low-side current limit value.

If the output load current exceeds the available inductor current (clamped by the above-mentioned low-side current limit), the output capacitor needs to supply the extra current such that the output voltage will begin to drop. If it drops below the output under-voltage protection trip threshold, the IC will stop switching to avoid excessive heat.

Output Under-Voltage Protection

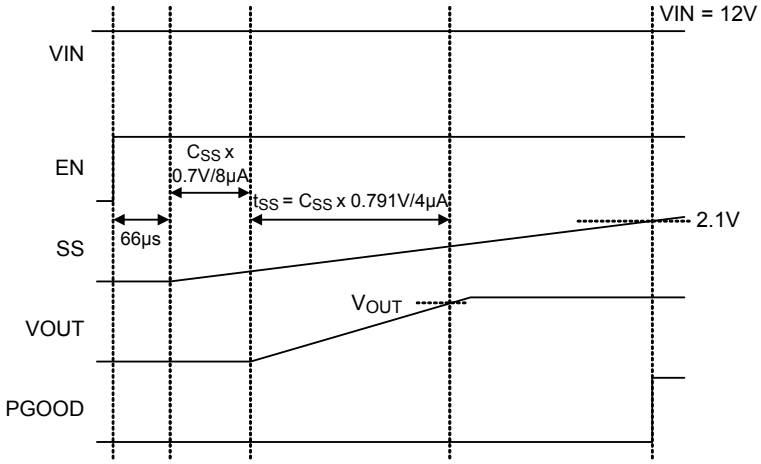
The RT6217A/B includes output under-voltage protection (UVP) against over-load or short-circuited condition by constantly monitoring the feedback voltage V_{FB}. If V_{FB} drops below the under-voltage protection trip threshold (typically 50% of the internal reference voltage), the UV comparator will go high to turn off both the internal high-side and low-side MOSFET switches.

Soft-Start (SS)

The soft-start function is used to prevent large inrush currents while the converter is being powered up. The RT6217A/B provides an SS pin so that the soft-start time can be programmed by selecting the value of the external soft-start capacitor C_{SS} connected from the SS pin to GND. During the start-up sequence, the soft-start capacitor is charged by an internal current source I_{SS} (typically, 4μA) to generate a soft-start ramp voltage as a reference voltage. Only when this ramp voltage is higher than the feedback voltage, the switching will be resumed. The output voltage can then ramp up smoothly to its targeted regulation voltage, and the converter can have a monotonic smooth start-up. For soft-start control, the SS pin should never be left unconnected.

$$t_{SS} = C_{SS} \times 0.791V/4\mu A$$

After the SS pin voltage rises above 2.1V (typically), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high. The typical start-up waveform shown below indicate the sequence and timing between the output voltage and related voltage.



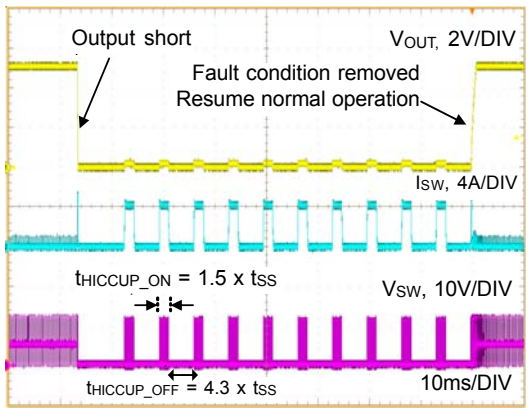
Hiccup Mode

If the output under-voltage condition continues for a period of time, the RT6217A/B will enter output under-voltage protection with hiccup mode. During hiccup mode, the IC will shut down for t_{HICCUP_OFF}, and then attempt to recover automatically for t_{HICCUP_ON}, which can be expressed as

$$t_{HICCUP\_ON} = 1.5 \times t_{SS}$$

$$t_{HICCUP\_OFF} = 4.3 \times t_{SS}$$

Upon completion of the soft-start sequence, if the fault condition is removed, the converter will resume normal operation; otherwise, such cycle for auto-recovery will be repeated until the fault condition is cleared. Hiccup mode allows the circuit to operate safely with low input current and power dissipation, and then resume normal operation as soon as the over-load or short-circuit condition is removed.



Power Good Indication

The RT6217A/B provides a power-good (PGOOD) open-drain output pin. It is to be connected to an external voltage source through a pull-up resistor. The power-good function is activated after soft-start is finished and is controlled by a comparator connected to the feedback signal V_{FB}. If V_{FB} raises above a power-good threshold (V_{TH_PGLH}) (typically 95% of the target value), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high after a certain delay elapsed. When V_{FB} drops by a power-good hysteresis (ΔV_{TH_PGLH}) (typically 5% of the target value) or exceeds V_{TH_PGHL} (typically 115% of the target value), the PGOOD pin will be pulled low. For V_{FB} above V_{TH_PGHL}, V_{PGOOD} will be pulled high again when V_{FB} drops back by a power-good hysteresis (ΔV_{TH_PGHL}) (typically 5% of the target value). Once being started-up, PGOOD will be pulled low to GND if any internal protection is triggered except current limit protection.

Over-Temperature Protection (Thermal Shutdown)

The RT6217A/B includes an over-temperature protection (OTP) circuitry to prevent overheating due to excessive power dissipation. The OTP will shut down switching operation when junction temperature exceeds a thermal shutdown threshold T_{SD}. Once the junction temperature cools down by a thermal shutdown hysteresis (ΔT_{SD}), the IC will resume normal operation with a complete soft-start.

Absolute Maximum Ratings (Note 1)

- Supply Input Voltage, VIN ---------- –0.3V to 28V
- Enable Pin Voltage, EN ---------- –0.3V to 28V
- Switch Voltage, SW ---------- –0.3V to 28V
  SW (t ≤ 10ns) ---------- –5V to 30V
- BOOT to SW, V_{BOOT} – V_{SW} ---------- –0.3V to 6V
- BOOT Voltage ---------- –0.3V to 34V
- Other Pins ---------- –0.3V to 6V
- Power Dissipation, P_D @ T_A = 25°C
  TSOT-23-8 (FC) ---------- 1.428W
- Package Thermal Resistance (Note 2)
  TSOT-23-8 (FC), θ_{JA} ---------- 70°C/W
  TSOT-23-8 (FC), θ_{JC} ---------- 15°C/W
- Junction Temperature ---------- 150°C
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV

Recommended Operating Conditions (Note 4)

- Supply Input Voltage ---------- 4.5V to 24V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = 12V, T_A = 25°C, unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Supply Voltage						
VIN Supply Input Operating Voltage	V_{IN}		4.5	--	24	V
VIN Under-Voltage Lockout Threshold	V_{UVLO}	V_{IN} rising	3.7	3.9	4.1	V
VIN Under-Voltage Lockout Threshold-Hysteresis	ΔV_{UVLO}		--	350	--	mV
Supply Current						
Shutdown Current	I_{SHDN}	V_{EN} = 0V	--	--	10	μA
Quiescent Current	I_Q	V_{EN} = 2V, V_{FB} = 1V, V_{SS} = 0V (not switching)	130	150	240	μA
Soft-Start						
Soft-Start Current	I_{SS}		--	4	--	μA
Enable Voltage						
EN Rising Threshold	V_{ENH}		1.2	1.4	1.6	V
EN Hysteresis	ΔV_{EN}		80	150	220	mV

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Feedback Voltage						
Feedback Threshold Voltage	V_{TH_FB}		779	791	803	mV
Internal MOSFET						
High-Side Switch On-Resistance	$R_{DS(ON)\_H}$	$V_{BOOT}-V_{SW}$ = 4.8V	--	85	--	mΩ
Low-Side Switch On-Resistance	$R_{DS(ON)\_L}$		--	40	--	mΩ
Current Limit						
Low-Side Switch Valley Current Limit	I_{LIM_L}		3.3	4.2	4.9	A
High-Side Switch Peak Current Limit	I_{LIM_H}		4.5	5.5	6.5	A
Switching Frequency						
Switching Frequency	f_{SW}		420	500	620	kHz
On-Time Timer Control						
Maximum Duty Cycle	D_{MAX}		--	90	--	%
Minimum On-Time	t_{ON_MIN}		--	60	--	ns
Thermal Shutdown						
Thermal Shutdown Threshold	T_{SD}		--	160	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	25	--	°C
Output Under Voltage Protections						
UVP Trip Threshold		UVP detect	--	50	--	%
		Hysteresis	--	10	--	%
Power Good						
Power-Good High Threshold	V_{TH_PGLH}	V_{FB} rising. PGOOD goes high.	--	95	--	%
Power-Good High Hysteresis	ΔV_{TH_PGLH}	V_{FB} falling. PGOOD goes low.	--	5	--	%
Power-Good Low Threshold	V_{TH_PGHL}	V_{FB} rising. PGOOD goes low.	--	115	--	%
Power-Good Low Hysteresis	ΔV_{TH_PGHL}	V_{FB} falling. PGOOD goes high.	--	5	--	%

Note 1. Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured under natural convection (still air) at T_A = 25°C with the component mounted on a high effective-thermal-conductivity four-layer test board on a JEDEC 51-7 thermal measurement standard. The first layer of cooper area is filled. θ_{JC} is measured at the lead of the package.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

Note 4. The device is not guaranteed to function outside its operating conditions.

Typical Application Circuit

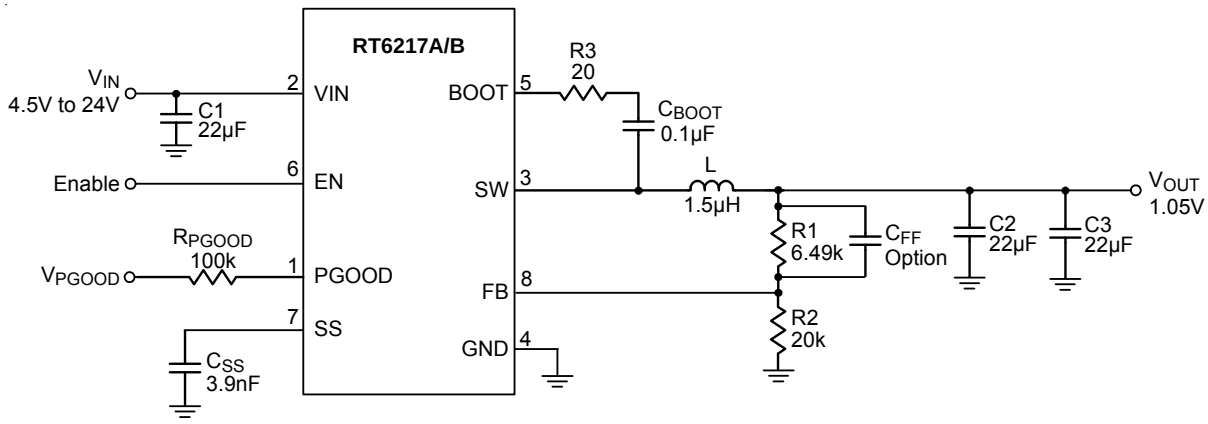


Table 1. Suggested Component Values

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)	L (µH)	C_{OUT} (µF)	C_{FF} (pF)
1.05	6.49	20	1.5	44	--
1.2	10.5	20	2.2	44	--
1.8	25.5	20	2.2	44	--
2.5	43.2	20	3.3	44	22 to 68
3.3	63.4	20	4.7	44	22 to 68
5	107	20	4.7	44	22 to 68

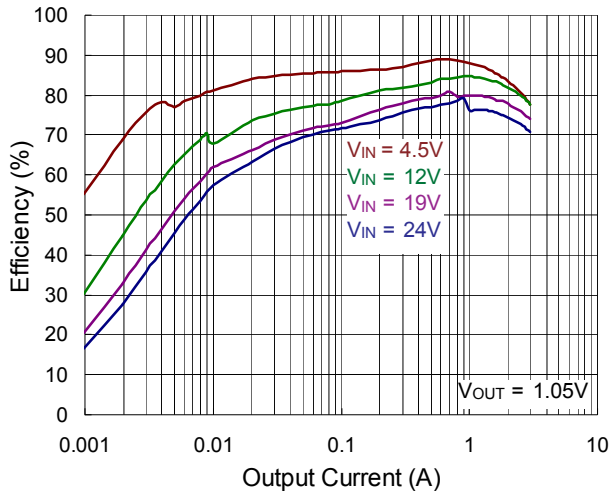
Note :

(1) All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC Bias.

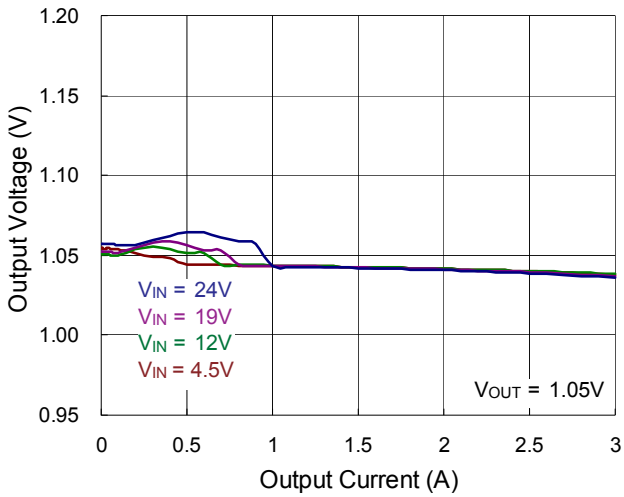
(2) For lower output voltage applications, load transient responses can also be improved by adding a feedforward capacitor (C_{FF}, 22pF to 68pF).

Typical Operating Characteristics

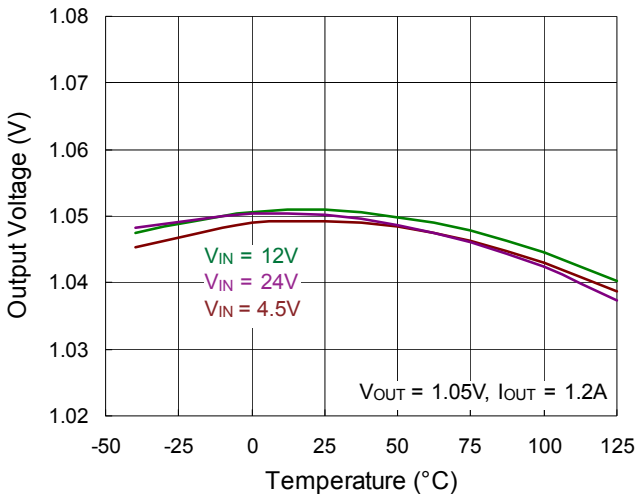
Efficiency vs. Output Current



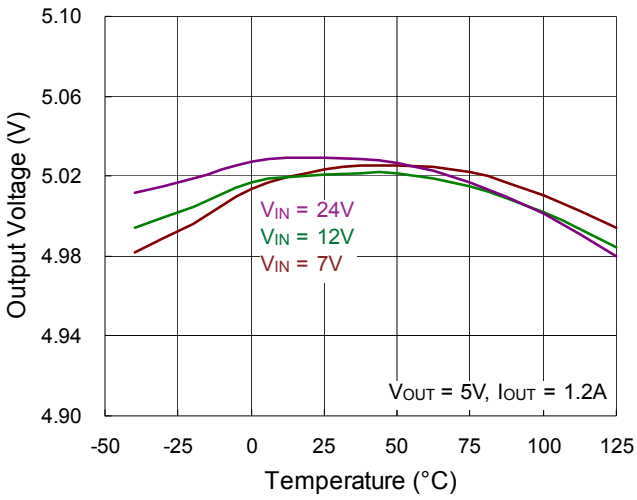
Output Voltage vs. Output Current



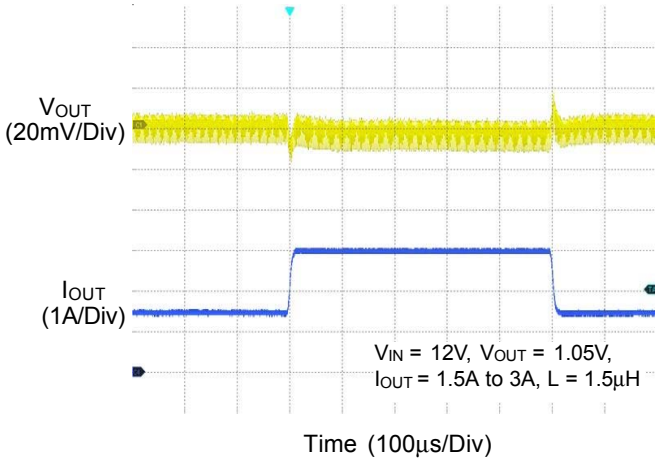
Output Voltage vs. Temperature



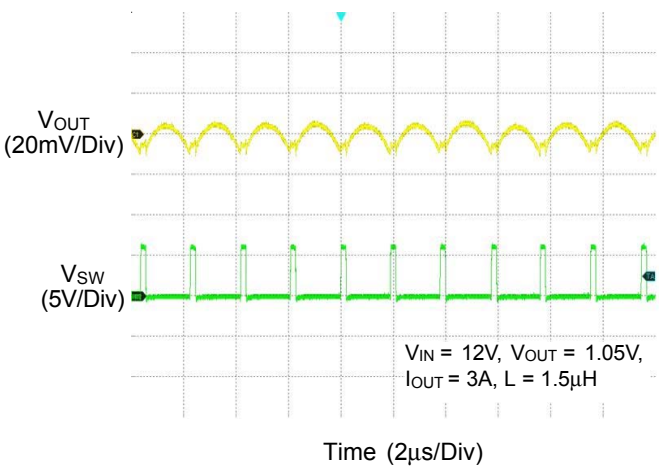
Output Voltage vs. Temperature



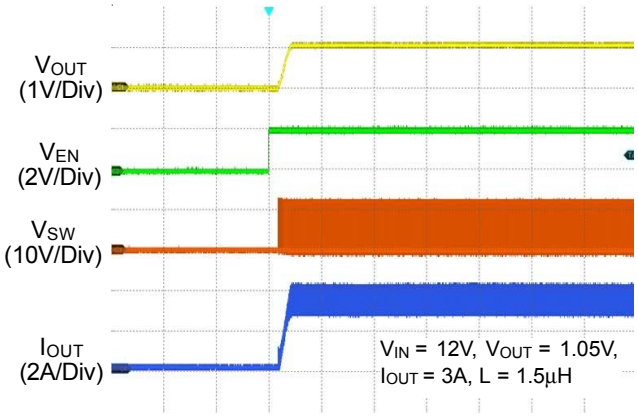
Load Transient Response



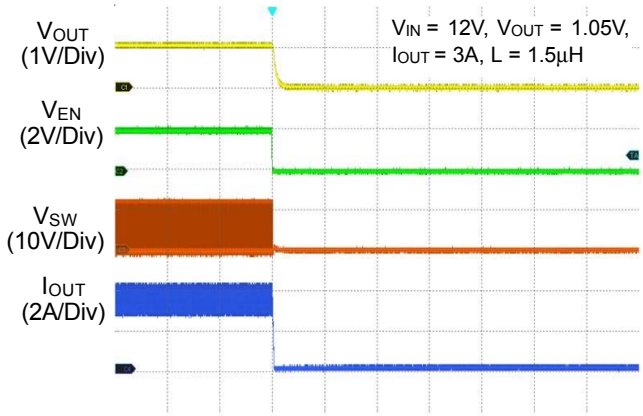
Output Ripple Voltage



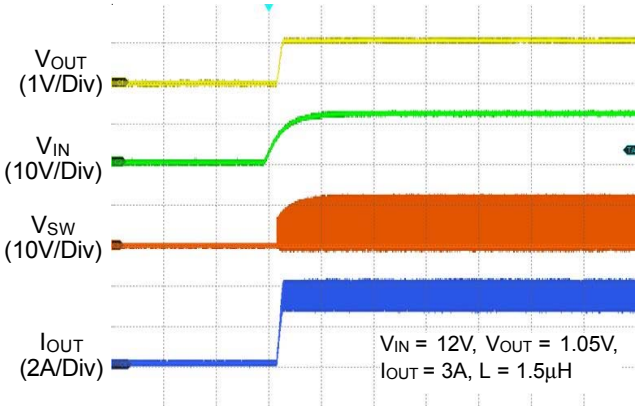
Power On from EN



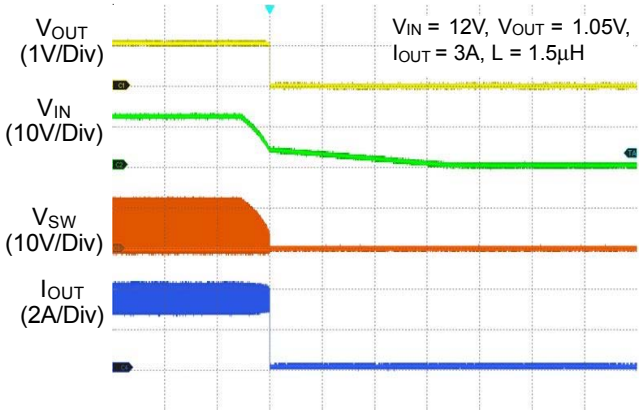
Power Off from EN



Power On from VIN



Power Off from VIN



Application Information

The output stage of a synchronous buck converter is composed of an inductor and capacitor, which stores and delivers energy to the load, and forms a second-order low-pass filter to smooth out the switch node voltage to maintain a regulated output voltage.

Inductor Selection

When designing the output stage of the synchronous buck converter, it is recommended to start with the inductor. However, it may require several iterations because the exact inductor value is generally flexible and is optimized for low cost, small form factor, and high overall performance of the converter. Further, inductors vary with manufacturers in both material and value, and typically have a tolerance of ±20%.

Three key inductor parameters to be specified for operation with the device are inductance (L), inductor saturation current (I_{SAT}), and DC resistance (DCR), which affects performance of the output stage. An inductor with lower DCR is recommended for applications of higher peak current or load current, and it can improve system performance. Lower inductor values are beneficial to the system in physical size, cost, DCR, and transient response, but they will cause higher inductor peak current and output voltage ripple to decrease system efficiency. Conversely, higher inductor values can increase system efficiency at the expense of larger physical size, slower transient response due to the longer response time of the inductor. A good compromise among size, efficiency, and transient response can be achieved by setting an inductor current ripple (ΔI_L) of about 20% to 50% of the desired full output load current. To meet the inductor current ripple (ΔI_L) requirements, a minimum inductance must be chosen and the approximate inductance can be calculated by the selected input voltage, output voltage, switching frequency (f_{SW}), and inductor current ripple (ΔI_L), as below :

$$L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times \Delta I_L}$$

Once the inductance is chosen, the inductor ripple current (ΔI_L) and peak inductor current (I_{L_PEAK}) can be calculated, as below :

$$\Delta I_L = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times f_{SW} \times L}$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2}\Delta I_L$$

$$I_{L\_VALLY} = I_{OUT\_MAX} - \frac{1}{2}\Delta I_L$$

where I_{OUT_MAX} is the maximum rated output current or the required peak current.

The inductor must be selected to have a saturation current and thermal rating which exceed the required peak inductor current I_{L_PEAK}. For a robust design to maintain control of inductor current in overload or short-circuit conditions, some applications may desire inductor saturation current rating up to the high-side switch current limit of the device. However, the built-in output under-voltage protection (UVP) feature makes this unnecessary for most applications.

I_{L_PEAK} should not exceed the minimum value of the device's high-side switch current limit because the device will not be able to supply the desired output current. By reducing the inductor current ripple (ΔI_L) to increase the average inductor current (and the output current), I_{L_PEAK} can be lowered to meet the device current limit requirement.

For best efficiency, a low-loss inductor having the lowest possible DCR that still fits in the allotted dimensions will be chosen. Ferrite cores are often the best choice. However, a shielded inductor, possibly larger or more expensive, will probably give fewer EMI and other noise problems.

The following design example is illustrated to walk through the steps to apply the equations defined above. The RT6217A/B's Typical Application Circuit for output voltage of 1.05V at maximum output current of 3A and an input voltage of 12V with inductor current ripple of 1.5A (i.e. 50%, in the recommended range of 20% to 50%, of the maximum rated output current) is taken as the design example. The approximate minimum inductor value can first be calculated as below :

$$L = \frac{1.05 \times (12 - 1.05)}{12 \times 500kHz \times 1.5A} = 1.28\mu H$$

where f_{SW} is 500kHz. The inductor current ripple will be set at 1.5A, as long as the calculated inductance of 1.28μH is used. However, the inductor of the exact inductance value may not be readily available, and therefore an inductor of a nearby value will be chosen. In this case, 1.5μH inductance is available and actually used in the Typical Application Circuit. The actual inductor current ripple (ΔI_L) and required peak inductor current (I_{L_PEAK}) can be calculated as below :

$$\Delta I_L = \frac{1.05 \times (12 - 1.05)}{12 \times 500kHz \times 1.5\mu H} = 1.28A$$

$$I_{L\_PEAK} = I_{OUT\_MAX} + \frac{1}{2}\Delta I_L = 3 + \frac{1.28}{2} = 3.64A$$

For the 1.5μH inductance value, the inductor saturation current and thermal rating should exceed 3.64A.

Input Capacitor Selection

Input capacitors are needed to smooth out the RMS ripple current (I_{RMS}) imposed by the switching currents and drawn from the input power source, by reducing the ripple voltage amplitude seen at the input of the converters. The voltage rating of the input filter capacitors must be greater than the maximum input voltage. It's also important to consider the ripple current capabilities of capacitors.

The RMS ripple current (I_{RMS}) of the regulator can be determined by the input voltage (V_{IN}), output voltage (V_{OUT}), and rated output current (I_{OUT}) as the following equation :

$$I_{RMS} = I_{OUT} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

From the above, the maximum RMS input ripple current occurs at maximum output load, which will be used as the requirements to consider the current capabilities of the input capacitors. Furthermore, for a single phase buck converter, the duty cycle is approximately the ratio of output voltage to input voltage. The maximum ripple voltage usually occurs at 50% duty cycle, that is, $V_{IN} = 2 \times V_{OUT}$. The maximum I_{RMS}, as I_{RMS_MAX}, can be approximated as 0.5 x I_{OUT_MAX}, where I_{OUT_MAX} is the maximum rated output current. Besides, the variation of the capacitance value with temperature, DC bias voltage, switching frequency, and allowable peal-to-peak ripple voltage that reflects back to the input, also need to be taken into consideration. For example, the capacitance value of a capacitor decreases as the DC bias across the capacitor increases; also, higher switching frequency allows the use of input capacitors of smaller capacitance values.

Ceramic capacitors are most commonly used to be placed right at the input of the converter to reduce ripple voltage amplitude because only ceramic capacitors have extremely low ESR which is required to reduce the ripple voltage. Note that the capacitors need to be placed as close as to the input pins as possible for highest effectiveness. Ceramic capacitors are preferred also due to their low cost, small size, high RMS current ratings, robust inrush surge current capabilities, and low parasitic inductance, which helps reduce the high-frequency ringing on the input supply.

However, care must be taken when ceramic capacitors are used at the input, and the input power is supplied by a wall adapter, connected through a long and thin wire. When a load step occurs at the output, a sudden inrush current will surge through the long inductive wire, which can induce ringing at the device's power input and potentially cause a very large voltage spike at the VIN pin to damage the device. For applications where the input power is located far from the device input, it may be required that the low-ESR ceramic input capacitors be placed in parallel with a bulk capacitor of other types, such as tantalum, electrolytic, or polymer, to dampen the voltage ringing and overshoot at the input, caused by the long input power path and input ceramic capacitor.

It is suggested to choose capacitors with higher temperature ratings than required. Several ceramic capacitors may be parallel to meet application requirements, such as the RMS current, size, and height. The Typical Application Circuit can use one 22μF, or two 10μF and one high-frequency- noise-filtering 0.1μF low-ESR ceramic capacitors at the input.

Output Capacitor Selection

Output capacitance affects the output voltage of the converter, the response time of the output feedback loop, and the requirements for output voltage sag and soar. The sag occurs after a sudden load step current applied, and the soar occurs after a sudden load removal. Increasing the output capacitance reduces the output voltage ripple and output sag and soar, while it increases the response time that the output voltage feedback loop takes to respond to step loads, Therefore, there is a tradeoff between output capacitance and output response. It is recommended to choose a minimum output capacitance to meet the output voltage requirements of the converter, and have a quick transient response to step loads.

The ESR of the output capacitor affects the damping of the output filter and the transient response. In general, low-ESR capacitors are good choices due to their excellent capability in energy storage and transient performance. The RT6217A/B, therefore, is specially optimized for ceramic capacitors. Consider also DC bias and aging effects while selecting the output capacitor.

- **Output Voltage Ripple**

  The output voltage ripple at the switching frequency is a function of the inductor current ripple going through the output capacitor's impedance. To derive the output voltage ripple, the output capacitor with capacitance, C_{OUT}, and its equivalent series resistance, R_{ESR}, must be taken into consideration. The output peak-to-peak ripple voltage ΔV_{P-P}, caused by the inductor current ripple ΔI_L, is characterized by two components, which are ESR ripple ΔV_{P-P_ESR} and capacitive ripple ΔV_{P-P_C}, can be expressed as below :

$$\Delta V_{P-P} = \Delta V_{P-P\_ESR} + \Delta V_{P-P\_C}$$

$$\Delta V_{P-P\_ESR} = \Delta I_L \times R_{ESR}$$

$$\Delta V_{P-P\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}}$$

  If ceramic capacitors are used as the output capacitors, both the components need to be considered due to the extremely low ESR and relatively small capacitance.

  For the RT6217A/B's Typical Application Circuit for output voltage of 1.05V, and actual inductor current ripple (ΔI_L) of 1.28A, using two paralleled 22μF ceramic capacitors with ESR of about 5mΩ as output capacitors, the two output ripple components are as below :

$$\Delta V_{P-P\_ESR} = \Delta I_L \times R_{ESR} = 1.28A \times 5m\Omega = 6.4mV$$

$$\Delta V_{P-P\_C} = \frac{\Delta I_L}{8 \times C_{OUT} \times f_{SW}} = \frac{1.28A}{8 \times 44\mu F \times 500kHz} = 7.27mV$$

$$\Delta V_{P-P} = \Delta V_{P-P\_ESR} + \Delta V_{P-P\_C} = 13.67mV$$

- **Output Transient Undershoot and Overshoot**

  In addition to the output voltage ripple at the switching frequency, the output capacitor and its ESR also affect output voltage sag, which is undershoot on a positive load step, and output voltage soar, which is overshoot on a negative load step. With the built-in ACOT™ architecture, the IC can have very fast transient responses to the load steps and small output transients.

  However, the combination of a small ceramic output capacitor (that is, of little capacitance) and a low output voltage (that is, only little charge stored in the output capacitor), used in low-duty-cycle applications (which require high inductance to get reasonable ripple currents for high input voltages), causes an increase in the size of voltage variations (i.e. sag/soar) in response to very quick load changes. Typically, the load changes slowly, compared with the IC's switching frequency. However, for present-day applications, more and more digital blocks may exhibit nearly instantaneous large transient load changes. Therefore, in the following section, how to calculate the worst-case voltage swings in response to very fast load steps will be explained in details.

  Both of the output transient undershoot and overshoot have two components : a voltage step caused by the output capacitor's ESR, and a voltage sag or soar due to the finite output capacitance and the inductor current slew rate. The following formulas can be used to check if the ESR is low enough (which is usually not a problem with ceramic capacitors) and if the output capacitance is large enough to prevent excessive sag or soar on very fast load steps, with the chosen inductor value.

  The voltage step (ΔV_{OUT_ESR}) caused by the ESR is a function of the load step (ΔI_{OUT}) and the ESR (R_{ESR}) of the output capacitor, described as below :

$$\Delta V_{OUT\_ESR} = \Delta I_{OUT} \times R_{ESR}$$

The voltage amplitude (V_{OUT_SAG}) of the capacitive sag is a function of the load step (ΔI_{OUT}), the output capacitor value (C_{OUT}), the inductor value (L), the input-to-output voltage differential, and the maximum duty cycle (D_{MAX}). And, the maximum duty cycle during a fast transient can be determined by the on-time (t_{ON}) and the minimum off-time (t_{OFF_MIN}) since the ACOT™ control scheme will ramp the current during on-times, which are spaced apart by a minimum off-time, that is, as fast as allowed. The approximate on-time (neglecting parasitics) and maximum duty cycle for a given input and output voltage can be calculated according to the following equations :

$$t_{ON} = \frac{V_{OUT}}{V_{IN} \times f_{SW}}$$

$$D_{MAX} = \frac{t_{ON}}{t_{ON} + t_{OFF\_MIN}}$$

Note the actual on-time will be slightly larger than the calculated one as the IC will automatically adapt to compensate the internal voltage drops, such as the voltage across high-side switch due to on-resistance. However, both of these can be neglected since the on-time increase can compensate for the voltage drops. The output voltage sag (ΔV_{OUT_SAG}) can then be calculated as below :

$$\Delta V_{OUT\_SAG} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times (V_{IN} \times D_{MAX} - V_{OUT})}$$

The voltage amplitude of the capacitive soar is a function of the load step (ΔI_{OUT}), the output capacitor value (C_{OUT}), the inductor value (L), and the output voltage (V_{OUT}). And the output voltage soar (ΔV_{OUT_SOAR}) can be calculated as below :

$$\Delta V_{OUT\_SOAR} = \frac{L \times (\Delta I_{OUT})^2}{2 \times C_{OUT} \times V_{OUT}}$$

Feedforward Capacitor (C_{FF})

The RT6217A/B is optimized for ceramic output capacitors and for low duty-cycle applications. This optimization makes circuit stability easy to achieve with reasonable output capacitors, but it also narrows the optimization of transient responses of the converter. For high output voltage (that is, high duty-cycle) applications, the FB voltage is highly attenuated from the output, the circuit's response becomes under-damped and transient response is slowed. A small feedforward capacitor (C_{FF}) can be introduced into the feedback network to speed up the transient response of high output voltage circuits. The feedforward capacitor is added across the upper FB divider resistor (as seen in Figure 1) to speed up the transient response without affecting the steady-state stability of the circuit.

To optimize transient response, a C_{FF} value is chosen so that the gain and phase boost of the feedback network increases the bandwidth of the converter, while still maintaining an acceptable phase margin. Generally, larger C_{FF} values provide higher bandwidth, but may result in an unacceptable phase margin or instability. Suitable feedforward capacitor values can be chosen from the table of Suggested Component Values.

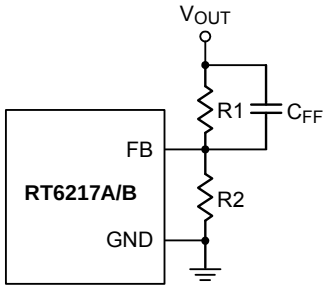


Figure 1. C_{FF} Capacitor Setting

EN Pin for Start-Up and Shutdown Operation

For automatic start-up, the EN pin, with high-voltage rating, can be connected to the input supply V_{IN}, either directly or through a 100kΩ resistor. The large built-in hysteresis band makes the EN pin useful for simple delay and timing circuits. The EN pin can be externally connected to V_{IN} by adding a resistor R_{EN} and a capacitor C_{EN}, as shown in Figure 2, to have an additional delay. The time delay can be calculated with the EN's internal threshold, at which switching operation begins.

An external MOSFET can be added for the EN pin to be logic-controlled, as shown in Figure 3. In this case, a 100kΩ pull-up resistor, R_{EN}, is connected between V_{IN} and the EN pin. The MOSFET Q1 will be under logic control to pull down the EN pin. To prevent the device being enabled when V_{IN} is smaller than the V_{OUT} target level or some other desired voltage level, a resistive divider (R_{EN1}

and R_{EN2}) can be used to externally set the input under-voltage lockout threshold, as shown in Figure 4.

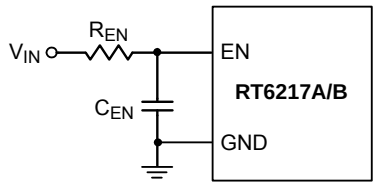


Figure 2. Enable Timing Control

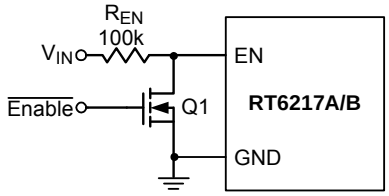


Figure 3. Logic Control for the EN Pin

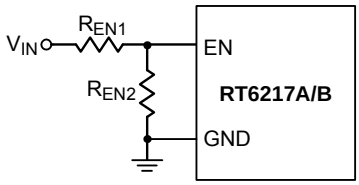


Figure 4. Resistor Divider for Under-Voltage Lockout Threshold Setting

Output Voltage Setting

The output voltage can be programmed by a resistive divider from the output to ground with the midpoint connected to the FB pin. The resistive divider allows the FB pin to sense a fraction of the output voltage as shown in Figure 5. The output voltage is set according to the following equation :

where V_{TH_FB} is around 0.791V (Typ).

$$V_{OUT} = V_{TH\_FB} \times (1 + \frac{R1}{R2})$$

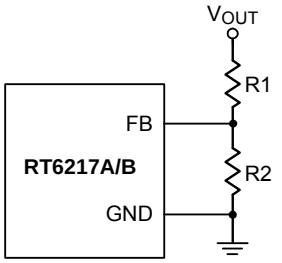


Figure 5. Output Voltage Setting

The placement of the resistive divider should be within 5mm of the FB pin. The resistance of R2 is recommended to 20kΩ to minimize power consumption and noise pick-up at the FB pin. Once R2 is chosen, the resistance of R1 can then be obtained as below :

$$R1 = \frac{R2 \times (V_{OUT} - V_{TH\_FB})}{V_{TH\_FB}}$$

For better output voltage accuracy, the divider resistors (R1 and R2) with ±1% tolerance or better should be used.

External Bootstrap Capacitor

A small capacitor between the BOOT and SW pins provides the gate drive voltage for the high-side MOSFET. The BOOT capacitor is refreshed when the high-side MOSFET is off and low-side MOSFET is conducted. The recommended bootstrap capacitor typical value of 0.1μF, ≥ 6.3V low-ESR ceramic capacitor is required to supply the high-side gate driver.

External Bootstrap Diode

It is recommended to add an external bootstrap diode between an external 5V voltage supply and the BOOT pin to improve enhancement of the internal MOSFET switch and improve efficiency when the input voltage is below 5.5V. The bootstrap diode can be a low-cost one, such as 1N4148 or BAT54. The external 5V can be a fixed 5V voltage supply from the system, or a 5V output voltage generated by the RT6217A/B. Note that the BOOT voltage V_{BOOT} must be lower than 5.5V.

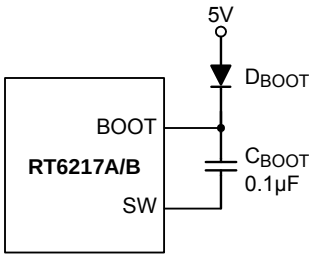


Figure 6. External Bootstrap Diode

Resistor at BOOT Pin

The gate driver of an internal power MOSFET, utilized as a high-side switch, is optimized for turning on the switch not only fast enough for reducing switching power loss, but also slow enough for minimizing EMI. The EMI issue is worse when the switch is turned on rapidly due to high di/dt noises induced. When the high-side switch is being turned off, the SW node will be discharged relatively slowly by the inductor current due to the presence of the dead time when both the high-side and low-side switches are turned off.

In some cases, it is desirable to reduce EMI further, even at the expense of some additional power dissipation. The turn-on rate of the high-side switch can be slowed by placing a small (≤ 20Ω) resistor between the BOOT pin and the external bootstrap capacitor as shown in Figure 7. This will slow down the rates of the high-side switch turn-on and the rise of V_{SW}. In order to improve EMI performance and enhancement of the internal MOSFET switch. The recommended application circuit is shown in Figure 8, which includes an external bootstrap diode for charging the bootstrap capacitor and a bootstrap resistor R_{BOOT} being placed between the BOOT pin and the capacitor/diode connection.

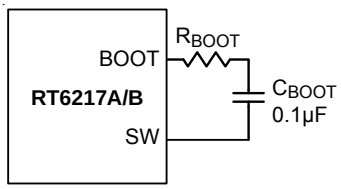


Figure 7. External Bootstrap Resistor at the BOOT Pin

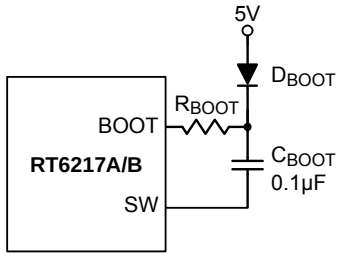


Figure 8. External Bootstrap Diode and Resistor at the BOOT Pin

Soft-Start Function

The RT6217A/B provides an adjustable soft-start function. The soft-start function is used to prevent large inrush current while the converter is being powered-up. The soft-start time is the output voltage rising time from 0V to a settled level and can be programmed by the external soft-start capacitor C_{SS} between the SS and GND pins. An internal current source I_{SS} (typically, 4µA) charges the capacitor to build a soft-start ramp voltage. The FB voltage will track the internal ramp voltage during soft-start. The typical soft-start time can be calculated as follows :

Soft-Start Time

$$t_{SS}\ (ms) = \frac{C_{SS}(nF) \times V_{TH\_FB}}{I_{SS}(\mu A)} = \frac{C_{SS}\ (nF) \times 0.791}{4(\mu A)}$$

Do not leave SS unconnected.

Power-Good Output

The PGOOD pin is an open-drain power-good indication output and is to be connected to an external voltage source through a pull-up resistor. The power-good function is activated after soft-start is finished and is controlled by the feedback signal V_{FB}. During soft-start, PGOOD is actively held low and only allowed to transition high after soft-start is over. If V_{FB} rises above a power-good threshold (V_{TH_PGLH}) (typically 95% of the target value), the PGOOD pin will be in high impedance and V_{PGOOD} will be held high after a certain delay elapsed. When V_{FB} drops by a power-good hysteresis (ΔV_{TH_PGLH}) (typically 5% of the target value) or exceeds V_{TH_PGHL} (typically 115% of the target value), the PGOOD pin will be pulled low. For V_{FB} above V_{TH_PGHL}, V_{PGOOD} will be pulled high again when V_{FB} drops back by a power-good hysteresis (ΔV_{TH_PGHL}) (typically 5% of the target value). Once being started-up, PGOOD will be pulled low to GND if any internal protection is triggered except current limit protection.

Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient

temperatures. The maximum power dissipation can be calculated using the following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

where $T_{J(MAX)}$ is the maximum junction temperature, T_A is the ambient temperature, and θ_{JA} is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, θ_{JA}, is highly package dependent. For a TSOT-23-8 (FC) package, the thermal resistance, θ_{JA}, is 70°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board. The maximum power dissipation at T_A = 25°C can be calculated as below :

$P_{D(MAX)}$ = (125°C – 25°C) / (70°C/W) = 1.428W for a TSOT-23-8 (FC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, θ_{JA}. The derating curves in Figure 9 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

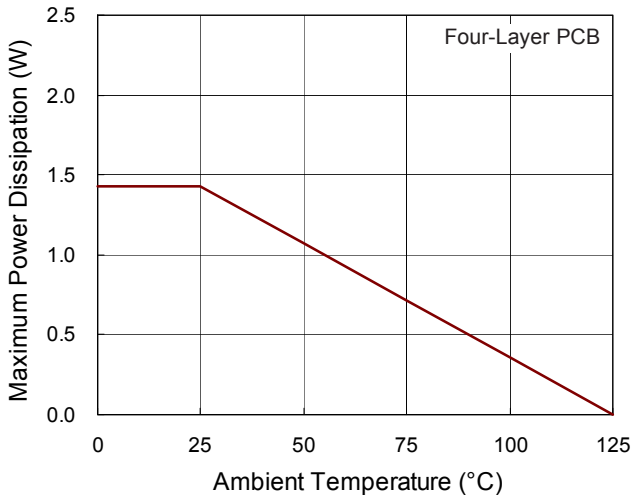


Figure 9. Derating Curve of Maximum Power Dissipation

Layout Considerations

For best performance of the RT6217A/B, the following layout guidelines must be strictly followed.

- Input capacitor must be placed as close to the IC as possible.
- SW should be connected to inductor by wide and short trace. Keep sensitive components away from this trace.
- Keep every trace connected to pin as wide as possible for improving thermal dissipation.
- The feedback components must be connected as close to the device as possible.
- Via can help to reduce power trace and improve thermal dissipation.

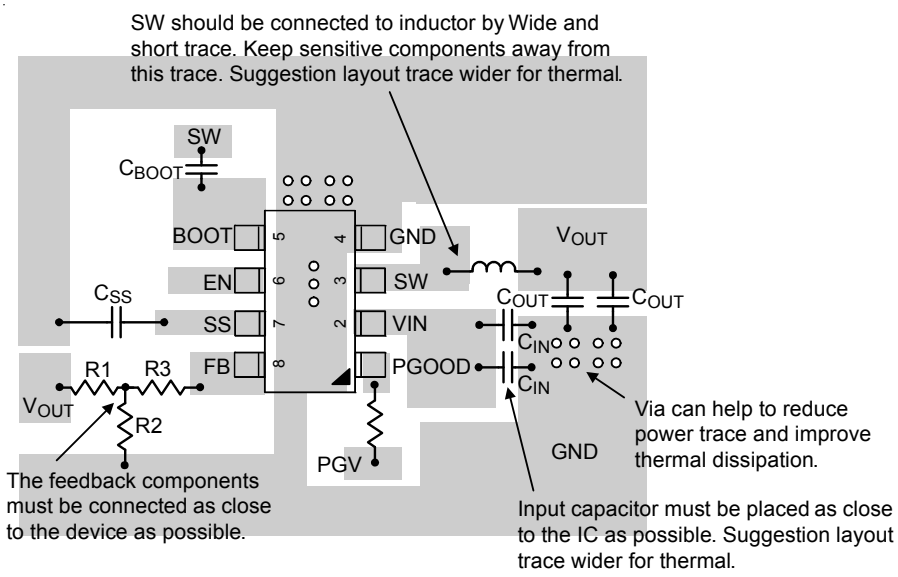
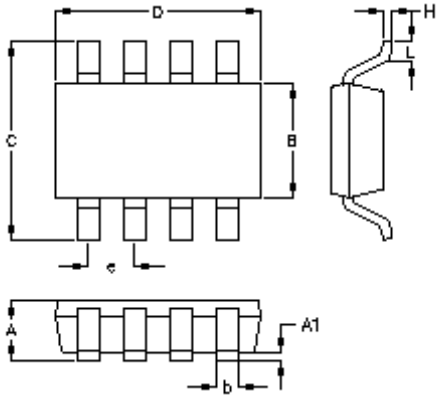


Figure 10. PCB Layout Guide

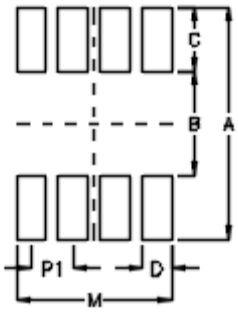
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	1.000	0.028	0.039
A1	0.000	0.100	0.000	0.004
B	1.397	1.803	0.055	0.071
b	0.220	0.380	0.009	0.015
C	2.591	3.000	0.102	0.118
D	2.692	3.099	0.106	0.122
e	0.585	0.715	0.023	0.028
H	0.080	0.254	0.003	0.010
L	0.300	0.610	0.012	0.024

TSOT-23-8 (FC) Surface Mount Package

Footprint Information



Package	Number of Pin	Footprint Dimension (mm)						Tolerance
		P1	A	B	C	D	M	
TSOT-28/TSOT-28(FC)/SOT-28	8	0.65	3.60	1.60	1.00	0.45	2.40	±0.10

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