150mA, Low Input Voltage, Low Dropout, Low Noise Ultra-Fast Without Bypass Capacitor CMOS LDO Regulator

General Description

The RT9030 is a high-performance, 150mA LDO regulator, offering extremely high PSRR and ultra-low dropout. Ideal for portable RF and wireless applications with demanding performance and space requirements.

The RT9030 quiescent current as low as 25μA, further prolonging the battery life. The RT9030 also works with low-ESR ceramic capacitors, reducing the amount of board space necessary for power applications, critical in hand-held wireless devices.

The RT9030 consumes typical 0.7μA in shutdown mode and has fast turn-on time less than 40μs. The other features include ultra-low dropout voltage, high output accuracy, current limiting protection, and high ripple rejection ratio. Available in the SC-70-5 and WDFN-6L 1.6x1.6 package.

Ordering Information

RT9030-□□□□

- Package Type
  - U5 : SC-70-5
  - QW : WDFN-6L 1.6x1.6 (W-Type)
- Lead Plating System
  - G : Green (Halogen Free and Pb Free)
- Fixed Output Voltage
  - 10 : 1.0V
  - 11 : 1.1V
  - :
  - 32 : 3.2V
  - 33 : 3.3V
  - 1B : 1.25V
  - 1H : 1.85V
  - 2H : 2.85V
  - 1K : 1.05V
  - 1C : 1.15V

Note :

Richtek products are :

- RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- Suitable for use in SnPb or Pb-free soldering processes.

Features

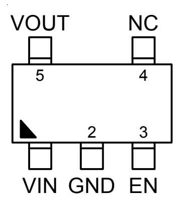
- **Wide Operating Voltage Ranges : 1.65V to 5.5V**
- **Output Voltage Ranges : 1V to 3.3V**
- **Low Dropout : 100mV at 150mA**
- **Ultra-Low-Noise for RF Application**
- **Ultra-Fast Response in Line/Load Transient**
- **Current Limiting Protection**
- **Thermal Shutdown Protection**
- **High Power Supply Rejection Ratio**
- **Only 1μF Output Capacitor Required for Stability**
- **TTL-Logic-Controlled Shutdown Input**
- **RoHS Compliant and Halogen Free**

Applications

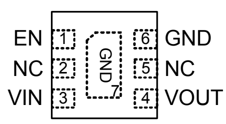
- CDMA/GSM Cellular Handsets
- Portable Information Appliances
- Laptop, Palmtops, Notebook Computers
- Hand-Held Instruments
- Mini PCI & PCI-Express Cards
- PCMCIA & New Cards

Pin Configuration

(TOP VIEW)



SC-70-5

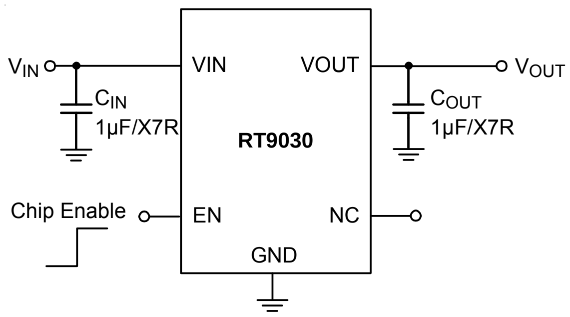


WDFN-6L 1.6x1.6

Marking Information

For marking information, contact our sales representative directly or through a Richtek distributor located in your area.

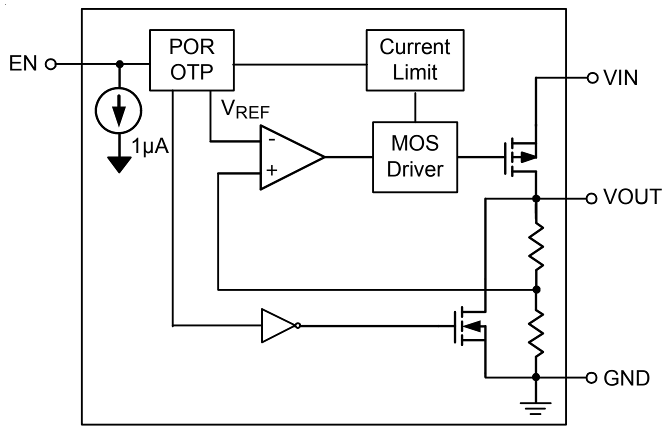
Typical Application Circuit



Functional Pin Description

Pin Number		Pin Name	Pin Function
SC-70-5	WDFN-6L 1.6x1.6		
5	4	VOUT	Regulator output.
4	2, 5	NC	No internal connection.
2	6, 7 (Exposed Pad)	GND	Ground. The exposed pad must be soldered to a large PCB and connected to GND for maximum power dissipation.
3	1	EN	Enable input Logic, active high. When the EN pin is open it will be pulled to low internally.
1	3	VIN	Supply input.

Functional Block Diagram



Absolute Maximum Ratings (Note 1)

- Supply Input Voltage ---------- 6V
- EN Input Voltage ---------- 6V
- Power Dissipation, P_D @ T_A = 25°C
  SC-70-5 ---------- 0.3W
  WDFN-6L 1.6x1.6 ---------- 0.571W
- Package Thermal Resistance (Note 2)
  SC-70-5, θ_{JA} ---------- 333°C/W
  WDFN-6L 1.6x1.6, θ_{JA} ---------- 175°C/W
- Lead Temperature (Soldering, 10 sec.) ---------- 260°C
- Junction Temperature ---------- 150°C
- Storage Temperature Range ---------- –65°C to 150°C
- ESD Susceptibility (Note 3)
  HBM (Human Body Model) ---------- 2kV
  MM (Machine Model) ---------- 200V

Recommended Operating Conditions (Note 4)

- Input Voltage Range ---------- 1.65V to 5.5V
- Junction Temperature Range ---------- –40°C to 125°C
- Ambient Temperature Range ---------- –40°C to 85°C

Electrical Characteristics

(V_{IN} = V_{OUT} + 0.5V, V_{EN} = V_{IN}, C_{IN} = C_{OUT} = 1μF/X5R (Ceramic), T_A = 25°C, unless otherwise specified)

Parameter		Symbol	Test Conditions	Min	Typ	Max	Unit
Output Noise Voltage		V_{ON}	I_{OUT} = 0mA	--	30	--	μV_{RMS}
Output Voltage Accuracy (Fixed Output Voltage)		ΔV_{OUT}	I_{OUT} = 150mA	–2	0	2	%
Quiescent Current (Note 5)		I_Q	I_{OUT} = 0mA	--	25	50	μA
Shutdown Current		I_{SHDN}	V_{EN} = 0V	--	0.7	1.5	μA
Current Limit		I_{LIM}	R_{LOAD} = 0Ω, 1.65V ≤ V_{IN} < 5.5V	170	285	400	mA
Dropout Voltage (Note 6)		V_{DROP}	V_{OUT} = 1.7V to 2.4V, I_{OUT} = 150mA, 1.65V ≤ V_{IN} ≤ 5.5V	50	--	200	mV
			V_{OUT} = 2.5V to 3.3V, I_{OUT} = 150mA, 1.65V ≤ V_{IN} ≤ 5.5V	20	--	150	
Load Regulation (Note 7) (Fixed Output Voltage)		ΔV_{LOAD}	1mA < I_{OUT} < 150mA 1.65V ≤ V_{IN} ≤ 5.5V	--	--	1	%
EN Threshold	Logic-Low Voltage	V_{IL}		0	--	0.3	V
	Logic-High Voltage	V_{IH}		1.6	--	5.5	
Enable Pin Current		I_{EN}		--	1	3	μA
Power Supply Rejection Rate	f = 1kHz	PSRR		--	–67	--	dB
	f = 10kHz			--	–55	--	
	f = 100kHz			--	–40	--	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Line Regulation	ΔV_{LINE}	V_{IN} = (V_{OUT} + 0.5) to 5.5V, I_{OUT} = 1mA to 150mA	--	0.01	0.2	%/V
Thermal Shutdown Temperature	T_{SD}		--	150	--	°C
Thermal Shutdown Hysteresis	ΔT_{SD}		--	20	--	

Note 1. Stresses beyond those listed "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

Note 2. θ_{JA} is measured at T_A = 25°C on a low effective thermal conductivity single-layer test board per JEDEC 51-3.

Note 3. Devices are ESD sensitive. Handling precaution is recommended.

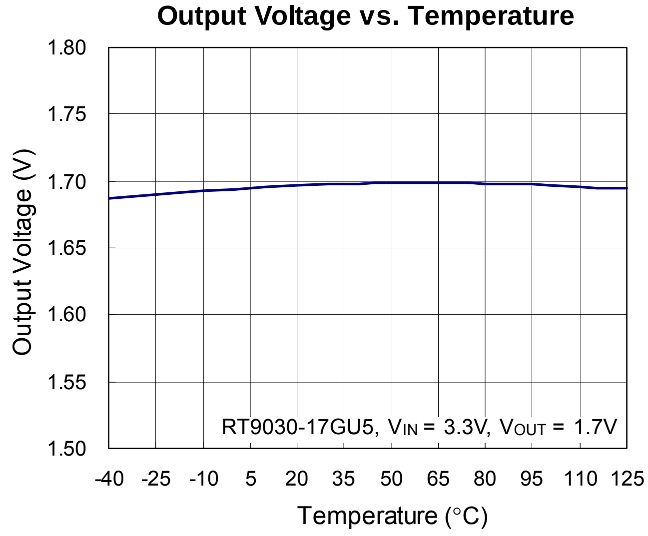
Note 4. The device is not guaranteed to function outside its operating conditions.

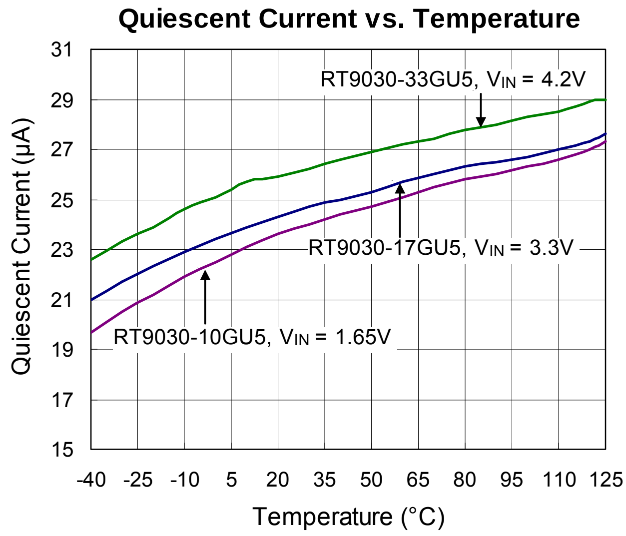
Note 5. Quiescent, or ground current, is the difference between input and output currents. It is defined by $I_Q = I_{IN} - I_{OUT}$ under no load condition (I_{OUT} = 0mA). The total current drawn from the supply is the sum of the load current plus the ground pin current.

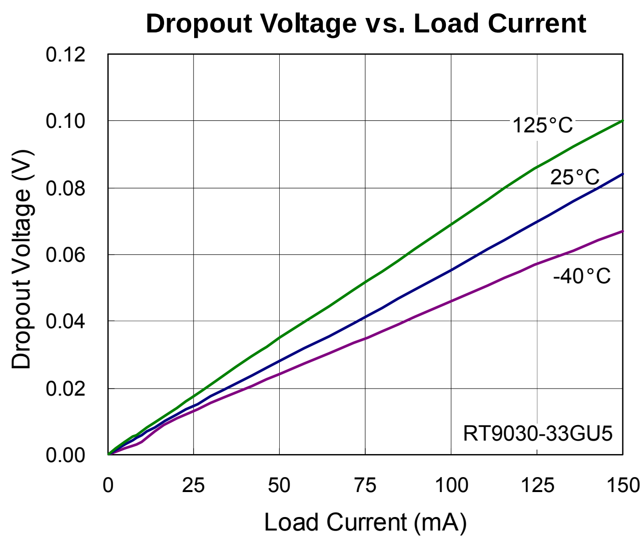
Note 6. The dropout voltage is defined as $V_{IN} - V_{OUT}$, which is measured when V_{OUT} is $V_{OUT(NORMAL)}$ - 100mV.

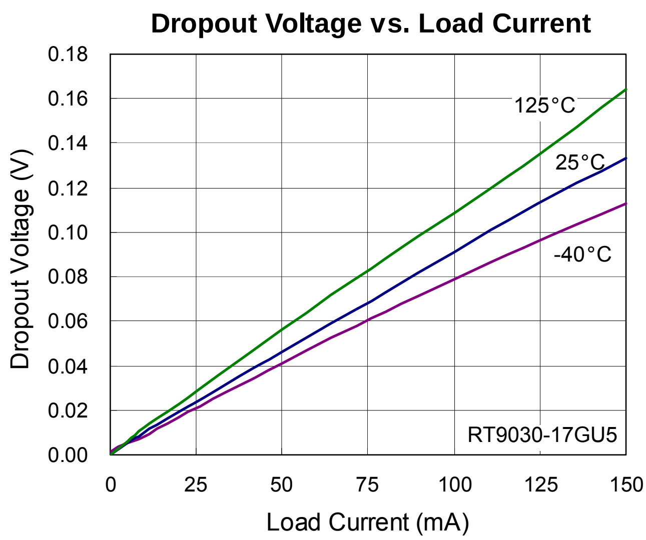
Note 7. Regulation is measured at constant junction temperature by using a 2ms current pulse. Devices are tested for load regulation in the load range from 10mA to 120mA.

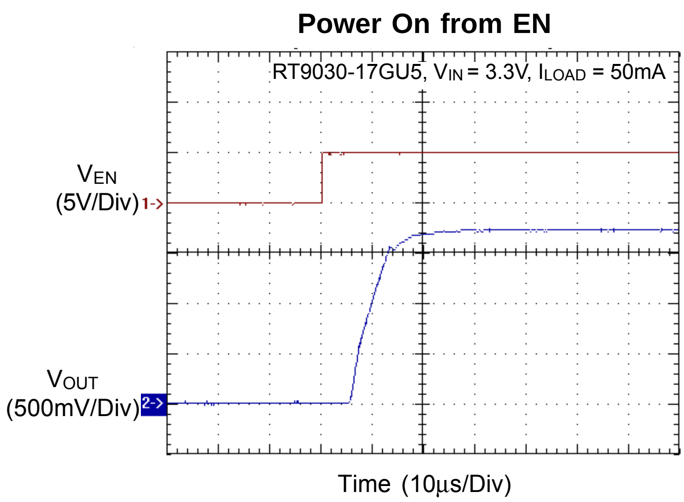
Typical Operating Characteristics

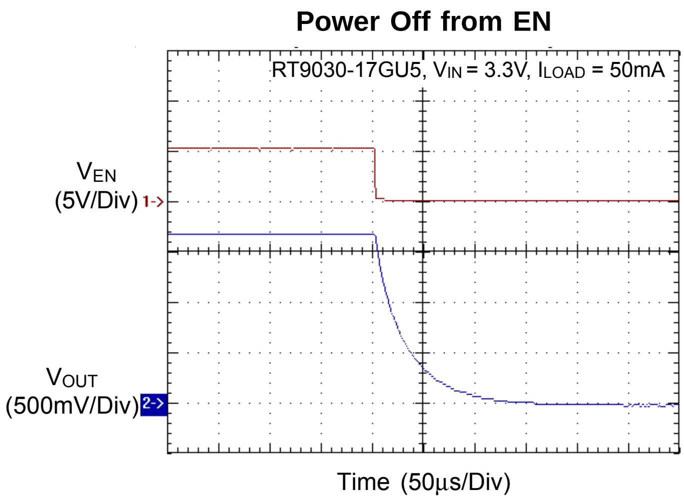




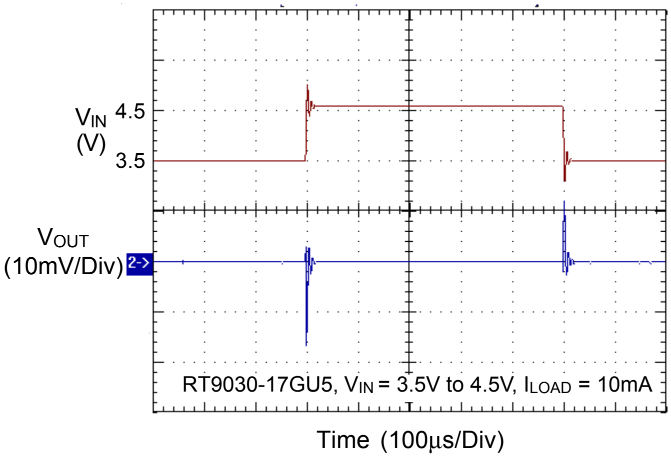




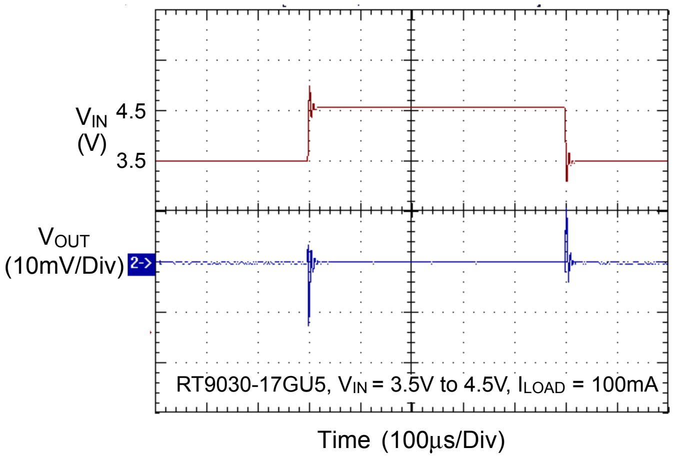




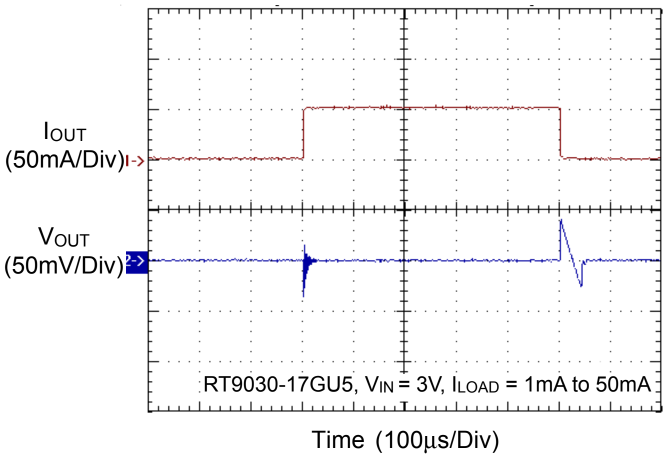
Line Transient Response



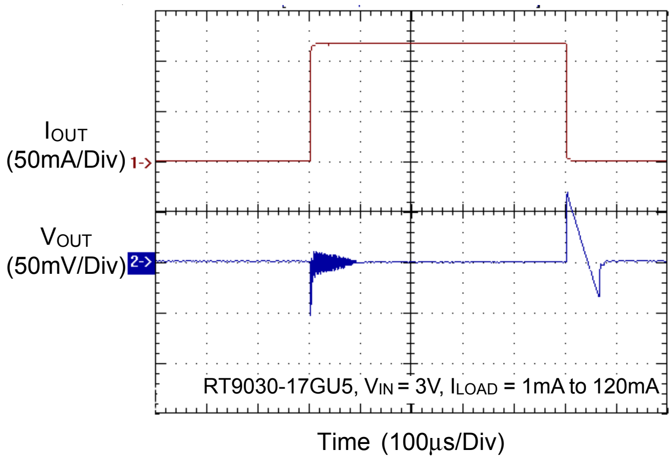
Line Transient Response



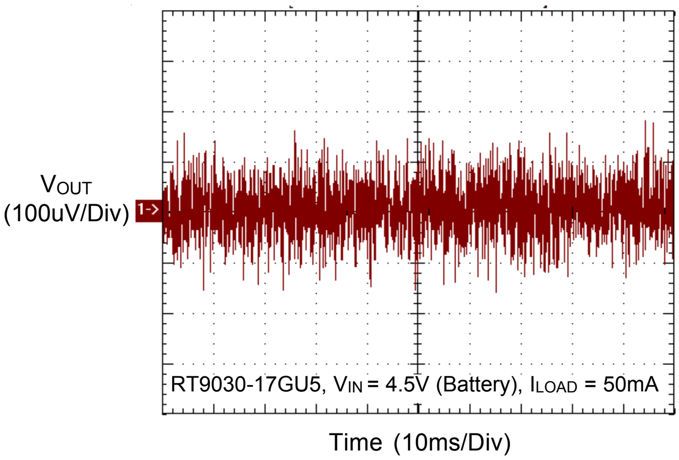
Load Transient Response



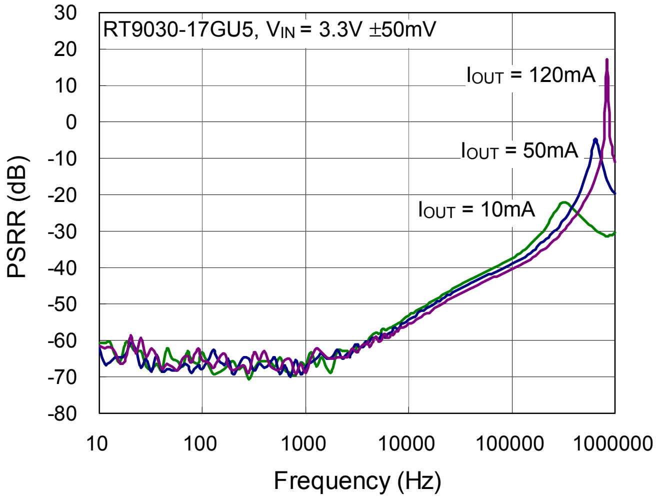
Load Transient Response



Noise



PSRR



Applications Information

Capacitor Selection

In order to confirm the regulator stability and performance, X7R/X5R or other better quality ceramic capacitor should be selected.

Like any low-dropout regulator, the external capacitors used with the RT9030 must be carefully selected for regulator stability and performance. Using a capacitor whose value is larger than 1μF on the RT9030 input and the amount of capacitance can be increased without limit. The input capacitor should be located in a distance of no more than 0.5 inch from the input pin of the IC and returned to a clean analog ground. The capacitor with larger value and lower ESR (equivalent series resistance) provides better PSRR and line-transient response.

The output capacitor must meet both requirements for minimum amount of capacitance in all LDOs application. The RT9030 is designed specifically to work with low ESR ceramic output capacitor in space-saving and performance consideration. Using a ceramic capacitor whose value is at least 1μF on the RT9030 output ensures stability. Output capacitor with larger capacitance can reduce noise and improve load transient response, stability, and PSRR. The output capacitor should be located in a distance of no more than 0.5 inch from the VOUT pin of the RT9030 and returned to a clean analog ground.

Enable

The RT9030 goes into shutdown mode when the EN pin is in a logic low condition. During this condition, the pass transistor, error amplifier, and bandgap are turned off, reducing the supply current to 0.7μA typical. The EN pin can be directly tied to VIN to keep the part on.

Current limit

The RT9030 contains an independent current limiter, which monitors and controls the pass transistor's gate voltage, limiting the output current to 285mA (typ.). The output can be shorted to ground indefinitely without damaging the part.

Thermal Shutdown Protection

As the die temperature is > 150°C , the chip will enter protection mode. The power MOSFET will turn-off during protection mode to prevent abnormal operation.

Thermal Considerations

Thermal protection limits power dissipation in the RT9030. When the operation junction temperature exceeds 170°C , the OTP circuit starts the thermal shutdown function and turns the pass element off. The pass element turn on again after the junction temperature cools by 30°C.

For continuous operation, do not exceed absolute maximum operation junction temperature 125°C. The power dissipation definition in device is :

$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$

The maximum power dissipation depends on the thermal resistance of IC package, PCB layout, the rate of surroundings airflow and temperature difference between junction to ambient. The maximum power dissipation can be calculated by following formula :

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature, T_A is the ambient temperature and the θ_{JA} is the junction to ambient thermal resistance.

For recommended operating conditions specification the maximum junction temperature of the die is 125°C. The junction to ambient thermal resistance θ_{JA} for WDFN-6L 1.6x1.6 package is 165°C/W and SC-70-5 package is 333°C/W on the standard JEDEC 51-3 single-layer thermal test board. The maximum power dissipation at T_A = 25°C can be calculated by following formula :

$P_{D(MAX)}$ = (125°C − 25°C) / (165°C/W) = 0.606W for WDFN-6L 1.6x1.6 packages

$P_{D(MAX)}$ = (125°C − 25°C) / (333°C/W) = 0.300W for SC-70-5 packages

The maximum power dissipation depends on operating ambient temperature for fixed $T_{J(MAX)}$ and thermal resistance θ_{JA}. The Figure 3 of derating curves allows the designer to see the effect of rising ambient temperature on the maximum power allowed.

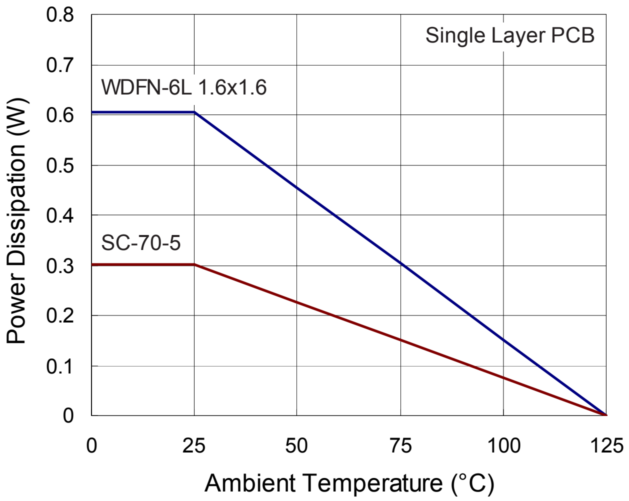


Figure 3. Derating Curve of Maximum Power Dissipation

Layout Considerations

Careful PCB Layout is necessary for better performance. The following guidelines should be followed for good PCB layout.

- Place the input and output capacitors as close as possible to the IC.
- Keep VIN and VOUT trace as possible as short and wide.
- Use a large PCB ground plane for maximum thermal dissipation.

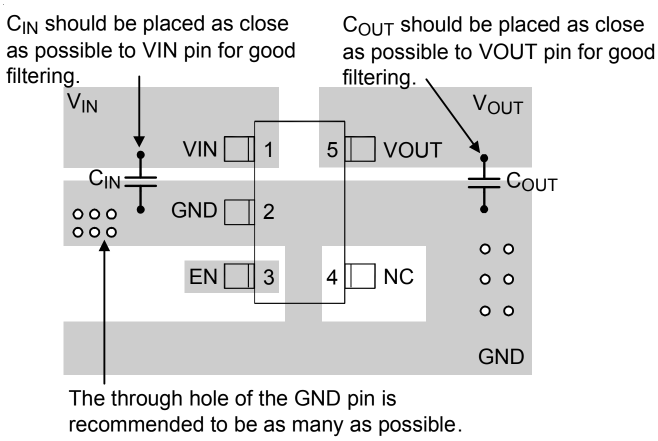
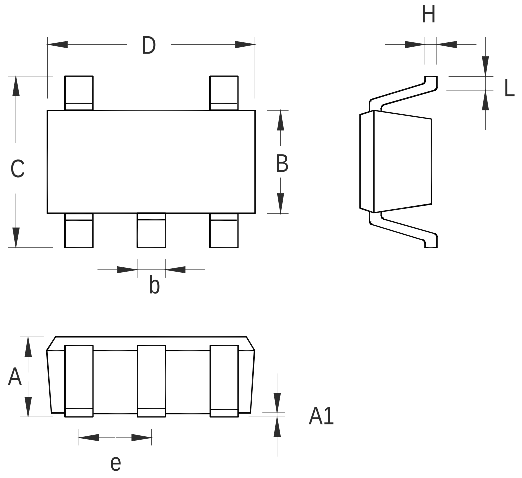


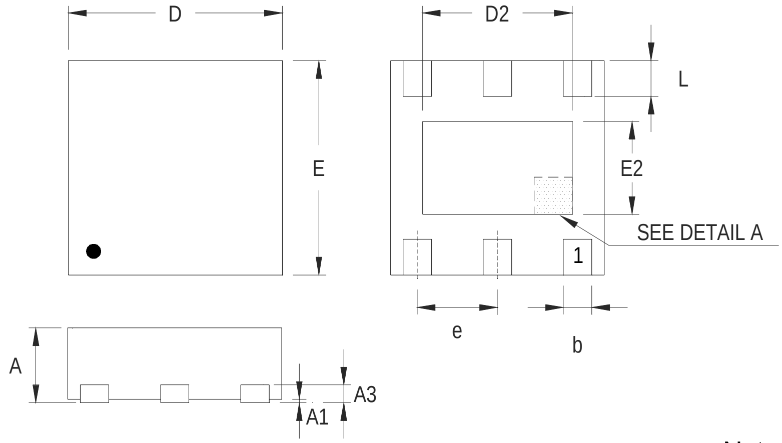
Figure 4

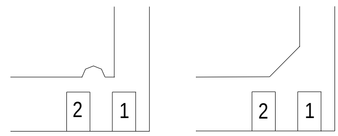
Outline Dimension



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.800	1.100	0.031	0.044
A1	0.000	0.100	0.000	0.004
B	1.150	1.350	0.045	0.054
b	0.150	0.400	0.006	0.016
C	1.800	2.450	0.071	0.096
D	1.800	2.250	0.071	0.089
e	0.650		0.026	
H	0.080	0.260	0.003	0.010
L	0.210	0.460	0.008	0.018

SC-70-5 Surface Mount Package





DETAIL A

Pin #1 ID and Tie Bar Mark Options

Note : The configuration of the Pin #1 identifier is optional, but must be located within the zone indicated.

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A3	0.175	0.250	0.007	0.010
b	0.200	0.300	0.008	0.012
D	1.550	1.650	0.061	0.065
D2	0.950	1.050	0.037	0.041
E	1.550	1.650	0.061	0.065
E2	0.550	0.650	0.022	0.026
e	0.500		0.020	
L	0.190	0.290	0.007	0.011

W-Type 6L DFN 1.6x1.6 Package

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