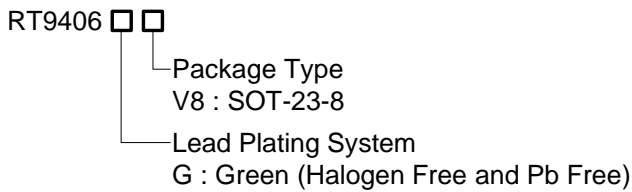


## 2-CH I<sup>2</sup>C-Controlled Reference Generator

### General Description

The RT9406 is a universal DAC generator which supports VID on-the-fly function with five different slew rates : Fast, Fast/2, Fast/4, Fast/8 and Fast/16. An I<sup>2</sup>C interface is built in the RT9406 to communicate with microprocessors. The reference voltage is within 1% accuracy. The RT9406 also provides pins to determine the initial voltage of Vref1 and Vref2. The RT9406 is available in the SOT-23-8 package.

### Ordering Information

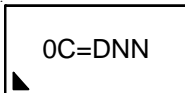


Note :

Richtek products are :

- ▶ RoHS compliant and compatible with the current requirements of IPC/JEDEC J-STD-020.
- ▶ Suitable for use in SnPb or Pb-free soldering processes.

### Marking Information



0C= : Product Code

DNN : Date Code

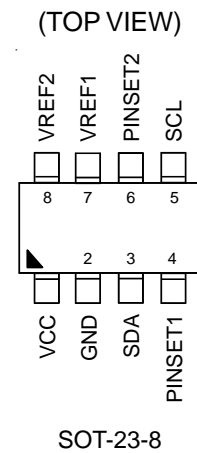
### Features

- I<sup>2</sup>C Interface Compatible
- 1% Reference Voltage Accuracy
- Small SOT-23-8 Package
- RoHS Compliant and Halogen Free

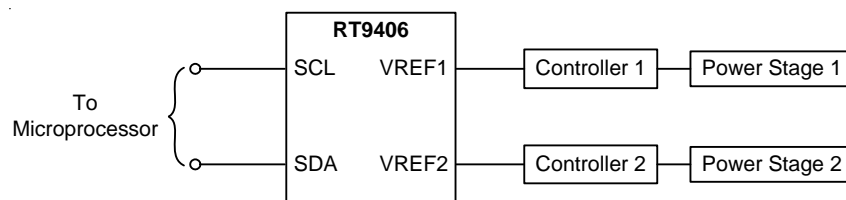
### Applications

- Notebook/Desktop Computer/Servers CPU Core Supply

### Pin Configurations



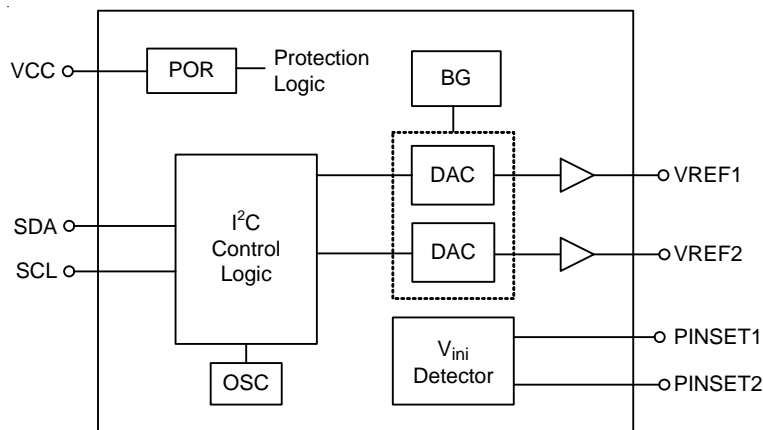
### Simplified Application Circuit



**Functional Pin Description**

Pin No.	Pin Name	Pin Function
1	VCC	Supply Voltage Input for DAC Generator. Connect this pin to 5V and place a decoupling capacitor 2.2μF at least. The decoupling capacitor should be as close to DAC generator as possible.
2	GND	Ground for the IC.
3	SDA	DAC Generator and Microprocessor Data Transmission Interface.
4	PINSET1	Determine VREF1 Initial Voltage. Refer to Application information for details.
5	SCL	Synchronous Clock from the Microprocessor.
6	PINSET2	Determine VREF2 Initial Voltage and I <sup>2</sup> C Address. Refer to Application information for details.
7	VREF1	Reference Voltage Output. The voltage can be programmed through I <sup>2</sup> C bus. The reference voltage of the PWM controller can be controlled by this pin.
8	VREF2	Reference Voltage Output. The voltage can be programmed through I <sup>2</sup> C bus. The reference voltage of the PWM controller can be controlled by this pin.

**Function Block Diagram**



**Operation**

**I<sup>2</sup>C Control Logic**

The interface that receives the I<sup>2</sup>C signal from microprocessor and sends the relative signals to determine VREF voltage.

**DAC**

Receive VID code from I<sup>2</sup>C control logic to generate DAC voltage.

**POR**

Detect the VCC voltage and issue POR and UVLO signal.

**BG**

Generate reference voltage for DAC usage.

**OSC**

Generate clock for I<sup>2</sup>C control logic.

**V<sub>ini</sub> Detector**

Detect the initial voltage of VREF1 and VREF2.

**Table 1. VR12 VID Code Table**

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Vref1/Vref2
0	0	0	0	0	0	0	0	00	0.1
0	0	0	0	0	0	0	1	01	0.5
0	0	0	0	0	0	1	0	02	0.51
0	0	0	0	0	0	1	1	03	0.52
0	0	0	0	0	1	0	0	04	0.53
0	0	0	0	0	1	0	1	05	0.54
0	0	0	0	0	1	1	0	06	0.55
0	0	0	0	0	1	1	1	07	0.56
0	0	0	0	1	0	0	0	08	0.57
0	0	0	0	1	0	0	1	09	0.58
0	0	0	0	1	0	1	0	0A	0.59
0	0	0	0	1	0	1	1	0B	0.6
0	0	0	0	1	1	0	0	0C	0.61
0	0	0	0	1	1	0	1	0D	0.62
0	0	0	0	1	1	1	0	0E	0.63
0	0	0	0	1	1	1	1	0F	0.64
0	0	0	1	0	0	0	0	10	0.65
0	0	0	1	0	0	0	1	11	0.66
0	0	0	1	0	0	1	0	12	0.67
0	0	0	1	0	0	1	1	13	0.68
0	0	0	1	0	1	0	0	14	0.69
0	0	0	1	0	1	0	1	15	0.7
0	0	0	1	0	1	1	0	16	0.71
0	0	0	1	0	1	1	1	17	0.72
0	0	0	1	1	0	0	0	18	0.73
0	0	0	1	1	0	0	1	19	0.74
0	0	0	1	1	0	1	0	1A	0.75
0	0	0	1	1	0	1	1	1B	0.76
0	0	0	1	1	1	0	0	1C	0.77
0	0	0	1	1	1	1	0	1D	0.78
0	0	0	1	1	1	1	1	1E	0.79
0	0	0	1	1	1	1	1	1F	0.8
0	0	1	0	0	0	0	0	20	0.81
0	0	1	0	0	0	0	1	21	0.82
0	0	1	0	0	0	1	0	22	0.83
0	0	1	0	0	0	1	1	23	0.84
0	0	1	0	0	1	0	0	24	0.85
0	0	1	0	0	1	0	1	25	0.86
0	0	1	0	0	1	1	0	26	0.87

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Vref1/Vref2
0	0	1	0	0	1	1	1	27	0.88
0	0	1	0	1	0	0	0	28	0.89
0	0	1	0	1	0	0	1	29	0.9
0	0	1	0	1	0	1	0	2A	0.91
0	0	1	0	1	0	1	1	2B	0.92
0	0	1	0	1	1	0	0	2C	0.93
0	0	1	0	1	1	0	1	2D	0.94
0	0	1	0	1	1	1	0	2E	0.95
0	0	1	0	1	1	1	1	2F	0.96
0	0	1	1	0	0	0	0	30	0.97
0	0	1	1	0	0	0	1	31	0.98
0	0	1	1	0	0	1	0	32	0.99
0	0	1	1	0	0	1	1	33	1
0	0	1	1	0	1	0	0	34	1.01
0	0	1	1	0	1	0	1	35	1.02
0	0	1	1	0	1	1	0	36	1.03
0	0	1	1	0	1	1	1	37	1.04
0	0	1	1	1	0	0	0	38	1.05
0	0	1	1	1	0	0	1	39	1.06
0	0	1	1	1	0	1	0	3A	1.07
0	0	1	1	1	0	1	1	3B	1.08
0	0	1	1	1	1	0	0	3C	1.09
0	0	1	1	1	1	0	1	3D	1.1
0	0	1	1	1	1	1	0	3E	1.11
0	0	1	1	1	1	1	1	3F	1.12
0	1	0	0	0	0	0	0	40	1.13
0	1	0	0	0	0	0	1	41	1.14
0	1	0	0	0	0	1	0	42	1.15
0	1	0	0	0	0	1	1	43	1.16
0	1	0	0	0	1	0	0	44	1.17
0	1	0	0	0	1	0	1	45	1.18
0	1	0	0	0	1	1	0	46	1.19
0	1	0	0	0	1	1	1	47	1.2
0	1	0	0	1	0	0	0	48	1.21
0	1	0	0	1	0	0	1	49	1.22
0	1	0	0	1	0	1	0	4A	1.23
0	1	0	0	1	0	1	1	4B	1.24
0	1	0	0	1	1	0	0	4C	1.25
0	1	0	0	1	1	0	1	4D	1.26
0	1	0	0	1	1	1	0	4E	1.27

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Vref1/Vref2
0	1	0	0	1	1	1	1	4F	1.28
0	1	0	1	0	0	0	0	50	1.29
0	1	0	1	0	0	0	1	51	1.3
0	1	0	1	0	0	1	0	52	1.31
0	1	0	1	0	0	1	1	53	1.32
0	1	0	1	0	1	0	0	54	1.33
0	1	0	1	0	1	0	1	55	1.34
0	1	0	1	0	1	1	0	56	1.35
0	1	0	1	0	1	1	1	57	1.36
0	1	0	1	1	0	0	0	58	1.37
0	1	0	1	1	0	0	1	59	1.38
0	1	0	1	1	0	1	0	5A	1.39
0	1	0	1	1	0	1	1	5B	1.4
0	1	0	1	1	1	0	0	5C	1.41
0	1	0	1	1	1	0	1	5D	1.42
0	1	0	1	1	1	1	0	5E	1.43
0	1	0	1	1	1	1	1	5F	1.44
0	1	1	0	0	0	0	0	60	1.45
0	1	1	0	0	0	0	1	61	1.46
0	1	1	0	0	0	1	0	62	1.47
0	1	1	0	0	0	1	1	63	1.48
0	1	1	0	0	1	0	0	64	1.49
0	1	1	0	0	1	0	1	65	1.5
0	1	1	0	0	1	1	0	66	1.51
0	1	1	0	0	1	1	1	67	1.52
0	1	1	0	1	0	0	0	68	1.53
0	1	1	0	1	0	0	1	69	1.54
0	1	1	0	1	0	1	0	6A	1.55
0	1	1	0	1	0	1	1	6B	1.56
0	1	1	0	1	1	0	0	6C	1.57
0	1	1	0	1	1	0	1	6D	1.58
0	1	1	0	1	1	1	0	6E	1.59
0	1	1	0	1	1	1	1	6F	1.6
0	1	1	1	0	0	0	0	70	1.61
0	1	1	1	0	0	0	1	71	1.62
0	1	1	1	0	0	1	0	72	1.63
0	1	1	1	0	0	1	1	73	1.64
0	1	1	1	0	1	0	0	74	1.65
0	1	1	1	0	1	0	1	75	1.66
0	1	1	1	0	1	1	0	76	1.67

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Vref1/Vref2
0	1	1	1	0	1	1	1	77	1.68
0	1	1	1	1	0	0	0	78	1.69
0	1	1	1	1	0	0	1	79	1.7
0	1	1	1	1	0	1	0	7A	1.71
0	1	1	1	1	0	1	1	7B	1.72
0	1	1	1	1	1	0	0	7C	1.73
0	1	1	1	1	1	0	1	7D	1.74
0	1	1	1	1	1	1	0	7E	1.75
0	1	1	1	1	1	1	1	7F	1.76
1	0	0	0	0	0	0	0	80	1.77
1	0	0	0	0	0	0	1	81	1.78
1	0	0	0	0	0	1	0	82	1.79
1	0	0	0	0	0	1	1	83	1.8
1	0	0	0	0	1	0	0	84	1.81
1	0	0	0	0	1	0	1	85	1.82
1	0	0	0	0	1	1	0	86	1.83
1	0	0	0	0	1	1	1	87	1.84
1	0	0	0	1	0	0	0	88	1.85
1	0	0	0	1	0	0	1	89	1.86
1	0	0	0	1	0	1	0	8A	1.87
1	0	0	0	1	0	1	1	8B	1.88
1	0	0	0	1	1	0	0	8C	1.89
1	0	0	0	1	1	0	1	8D	1.9
1	0	0	0	1	1	1	0	8E	1.91
1	0	0	0	1	1	1	1	8F	1.92
1	0	0	1	0	0	0	0	90	1.93
1	0	0	1	0	0	0	1	91	1.94
1	0	0	1	0	0	1	0	92	1.95
1	0	0	1	0	0	1	1	93	1.96
1	0	0	1	0	1	0	0	94	1.97
1	0	0	1	0	1	0	1	95	1.98
1	0	0	1	0	1	1	0	96	1.99
1	0	0	1	0	1	1	1	97	2
1	0	0	1	1	0	0	0	98	2.01
1	0	0	1	1	0	0	1	99	2.02
1	0	0	1	1	0	1	0	9A	2.03
1	0	0	1	1	0	1	1	9B	2.04
1	0	0	1	1	1	0	0	9C	2.05
1	0	0	1	1	1	0	1	9D	2.06
1	0	0	1	1	1	1	0	9E	2.07

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Vref1/Vref2
1	0	0	1	1	1	1	1	9F	2.08
1	0	1	0	0	0	0	0	A0	2.09
1	0	1	0	0	0	0	1	A1	2.1
1	0	1	0	0	0	1	0	A2	2.11
1	0	1	0	0	0	1	1	A3	2.12
1	0	1	0	0	1	0	0	A4	2.13
1	0	1	0	0	1	0	1	A5	2.14
1	0	1	0	0	1	1	0	A6	2.15
1	0	1	0	0	1	1	1	A7	2.16
1	0	1	0	1	0	0	0	A8	2.17
1	0	1	0	1	0	0	1	A9	2.18
1	0	1	0	1	0	1	0	AA	2.19
1	0	1	0	1	0	1	1	AB	2.2
1	0	1	0	1	1	0	0	AC	2.21
1	0	1	0	1	1	0	1	AD	2.22
1	0	1	0	1	1	1	0	AE	2.23
1	0	1	0	1	1	1	1	AF	2.24
1	0	1	1	0	0	0	0	B0	2.25
1	0	1	1	0	0	0	1	B1	2.26
1	0	1	1	0	0	1	0	B2	2.27
1	0	1	1	0	0	1	1	B3	2.28
1	0	1	1	0	1	0	0	B4	2.29
1	0	1	1	0	1	0	1	B5	2.3
1	0	1	1	0	1	1	0	B6	2.31
1	0	1	1	0	1	1	1	B7	2.32
1	0	1	1	1	0	0	0	B8	2.33
1	0	1	1	1	0	0	1	B9	2.34
1	0	1	1	1	0	1	0	BA	2.35
1	0	1	1	1	0	1	1	BB	2.36
1	0	1	1	1	1	0	0	BC	2.37
1	0	1	1	1	1	0	1	BD	2.38
1	0	1	1	1	1	1	0	BE	2.39
1	0	1	1	1	1	1	1	BF	2.4
1	1	0	0	0	0	0	0	C0	2.41
1	1	0	0	0	0	0	1	C1	2.42
1	1	0	0	0	0	1	0	C2	2.43
1	1	0	0	0	0	1	1	C3	2.44
1	1	0	0	0	1	0	0	C4	2.45
1	1	0	0	0	1	0	1	C5	2.46
1	1	0	0	0	1	1	0	C6	2.47

VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Vref1/Vref2
1	1	0	0	0	1	1	1	C7	2.48
1	1	0	0	1	0	0	0	C8	2.49
1	1	0	0	1	0	0	1	C9	2.5
1	1	0	0	1	0	1	0	CA	2.51
1	1	0	0	1	0	1	1	CB	2.52
1	1	0	0	1	1	0	0	CC	2.53
1	1	0	0	1	1	0	1	CD	2.54
1	1	0	0	1	1	1	0	CE	2.55
1	1	0	0	1	1	1	1	CF	2.56
1	1	0	1	0	0	0	0	D0	2.57
1	1	0	1	0	0	0	1	D1	2.58
1	1	0	1	0	0	1	0	D2	2.59
1	1	0	1	0	0	1	1	D3	2.6
1	1	0	1	0	1	0	0	D4	2.61
1	1	0	1	0	1	0	1	D5	2.62
1	1	0	1	0	1	1	0	D6	2.63
1	1	0	1	0	1	1	1	D7	2.64
1	1	0	1	1	0	0	0	D8	2.65
1	1	0	1	1	0	0	1	D9	2.66
1	1	0	1	1	0	1	0	DA	2.67
1	1	0	1	1	0	1	1	DB	2.68
1	1	0	1	1	1	0	0	DC	2.69
1	1	0	1	1	1	0	1	DD	2.7
1	1	0	1	1	1	1	0	DE	2.71
1	1	0	1	1	1	1	1	DF	2.72
1	1	1	0	0	0	0	0	E0	2.73
1	1	1	0	0	0	0	1	E1	2.74
1	1	1	0	0	0	1	0	E2	2.75
1	1	1	0	0	0	1	1	E3	2.76
1	1	1	0	0	1	0	0	E4	2.77
1	1	1	0	0	1	0	1	E5	2.78
1	1	1	0	0	1	1	0	E6	2.79
1	1	1	0	0	1	1	1	E7	2.8
1	1	1	0	1	0	0	0	E8	2.81
1	1	1	0	1	0	0	1	E9	2.82
1	1	1	0	1	0	1	0	EA	2.83
1	1	1	0	1	0	1	1	EB	2.84
1	1	1	0	1	1	0	0	EC	2.85
1	1	1	0	1	1	0	1	ED	2.86
1	1	1	0	1	1	1	0	EE	2.87



VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0	HEX	Vref1/Vref2
1	1	1	0	1	1	1	1	EF	2.88
1	1	1	1	0	0	0	0	F0	2.89
1	1	1	1	0	0	0	1	F1	2.9
1	1	1	1	0	0	1	0	F2	2.91
1	1	1	1	0	0	1	1	F3	2.92
1	1	1	1	0	1	0	0	F4	2.93
1	1	1	1	0	1	0	1	F5	2.94
1	1	1	1	0	1	1	0	F6	2.95
1	1	1	1	0	1	1	1	F7	2.96
1	1	1	1	1	0	0	0	F8	2.97
1	1	1	1	1	0	0	1	F9	2.98
1	1	1	1	1	0	1	0	FA	2.99
1	1	1	1	1	0	1	1	FB	3
1	1	1	1	1	1	0	0	FC	3.01
1	1	1	1	1	1	0	1	FD	3.02
1	1	1	1	1	1	1	0	FE	3.03
1	1	1	1	1	1	1	1	FF	3.04

## Absolute Maximum Ratings (Note 1)

- VCC to GND ----- -0.3V to 6.8V
- PINSET1, PINSET2, SCL, SDA, VREF1, VREF2 to GND ----- -0.3V to 6.8V
- Power Dissipation,  $P_D$  @  $T_A = 25^\circ\text{C}$ 
  - SOT-23-8 ----- 0.53W
- Package Thermal Resistance (Note 2)
  - SOT-23-8,  $\theta_{JA}$  ----- 186.2°C/W
- Junction Temperature ----- 150°C
- Lead Temperature (Soldering, 10 sec.) ----- 260°C
- Storage Temperature Range ----- -65°C to 150°C
- ESD Susceptibility (Note 3)
  - HBM (Human Body Model) ----- 2kV

## Recommended Operating Conditions (Note 4)

- Supply Voltage, VCC ----- 4.5V to 5.5V
- Junction Temperature Range ----- -40°C to 125°C
- Ambient Temperature Range ----- -40°C to 85°C

## Electrical Characteristics

( $V_{CC} = 5V$ ,  $T_A = 25^\circ\text{C}$ , unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit	
<b>Supply Input</b>							
Supply Voltage	$V_{CC}$		4.5	5	5.5	V	
Supply Current	$I_{CC}$	After Start-up	--	2	--	mA	
Supply Current before POR	$I_{POR}$	$V_{CC} = 2.1V$	--	1.4	--	mA	
<b>Reference and DAC</b>							
Reference Voltage Accuracy	$V_{REF}$	$V_{DAC1} > 1.12V$	-1	0	1	%/VID	
		$V_{DAC} = 0.35V$ to 1.12V	-10	0	10	mV	
Line Regulation	$\Delta V_{LINE}$	REFx = no load, $4.5V < V_{CC} < 5.5V$ , $V_{REF} = 1.12V$	-10	--	12	mV	
Load Regulation	$\Delta V_{LOAD}$	$V_{REFx} = 1.12V$ , $0A < I_{REFx} < 0.5mA$	-10	--	10	mV	
<b>Slew Rate</b>							
Dynamic VID Fast Slew Rate	SR	Set VID fast	10	11.5	13	mV/ $\mu\text{s}$	
<b>Serial VID</b>							
SCL and SDA Input Voltage	Logic-High	$V_{IH}$	Respect to INTEL Spec. with 50mV hysteresis		2.4	--	V
	Logic-Low	$V_{IL}$	--	--	0.8		
Leakage Current of SCL, SDA	$I_{LEAK}$		-1	--	3	$\mu\text{A}$	
Output Low Voltage at SDA		$I_{SDA} = 10mA$	--	--	0.3	V	

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
<b>Protection</b>						
Under Voltage Lockout Threshold	$V_{UVLO}$		3.9	4	4.1	V
Under Voltage Lockout Hysteresis	$\Delta V_{UVLO}$		100	150	200	mV

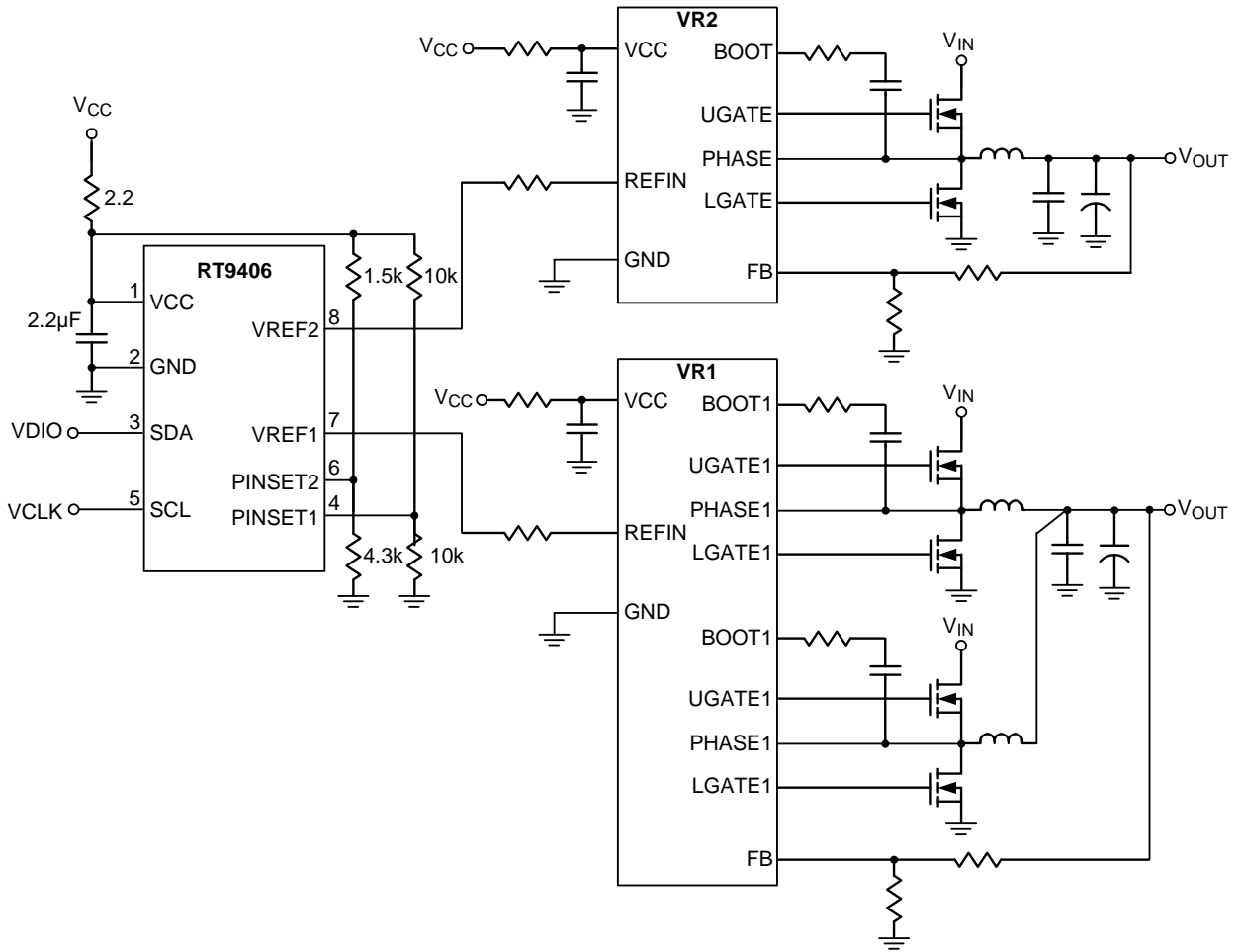
**Note 1.** Stresses beyond those listed “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

**Note 2.**  $\theta_{JA}$  is measured at  $T_A = 25^\circ\text{C}$  on a high effective thermal conductivity four-layer test board per JEDEC 51-7.

**Note 3.** Devices are ESD sensitive. Handling precaution is recommended.

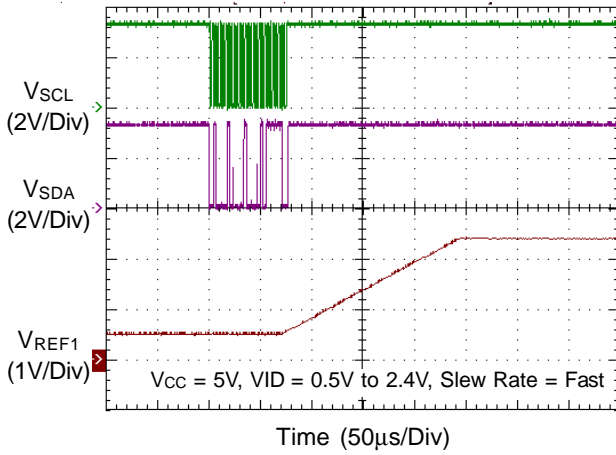
**Note 4.** The device is not guaranteed to function outside its operating conditions.

## Typical Application Circuit

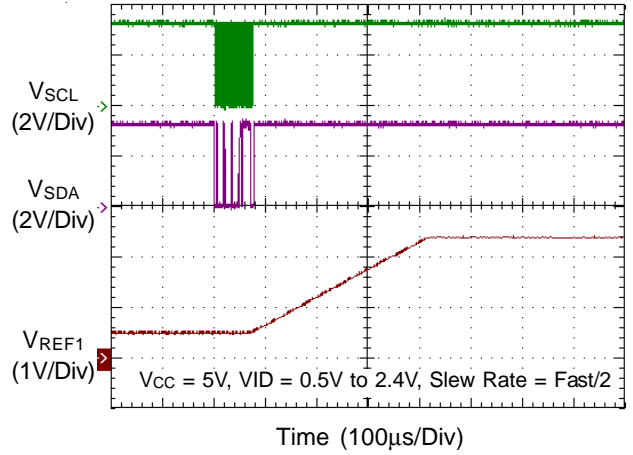


**Typical Operating Characteristics**

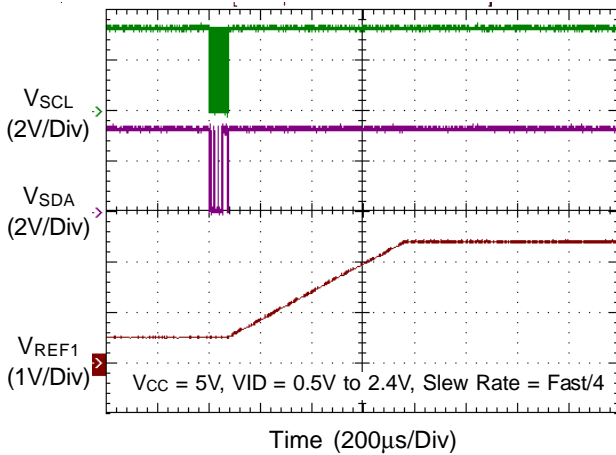
**VREF1 Dynamic VID Up**



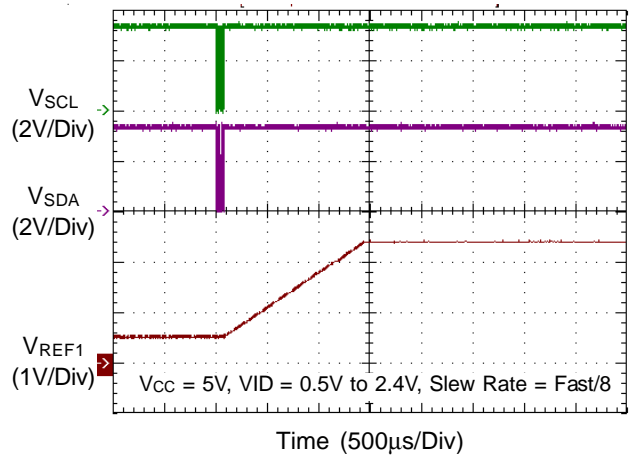
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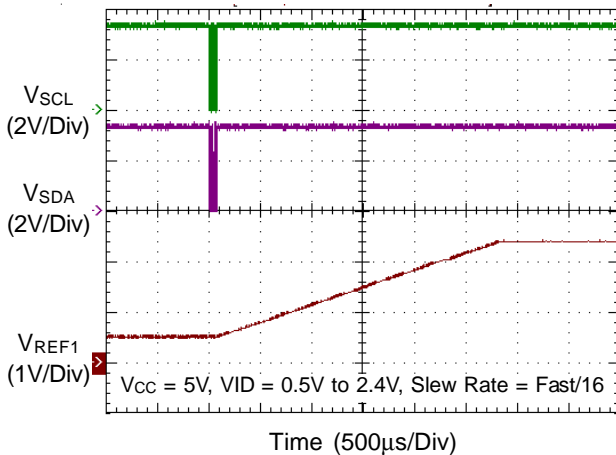
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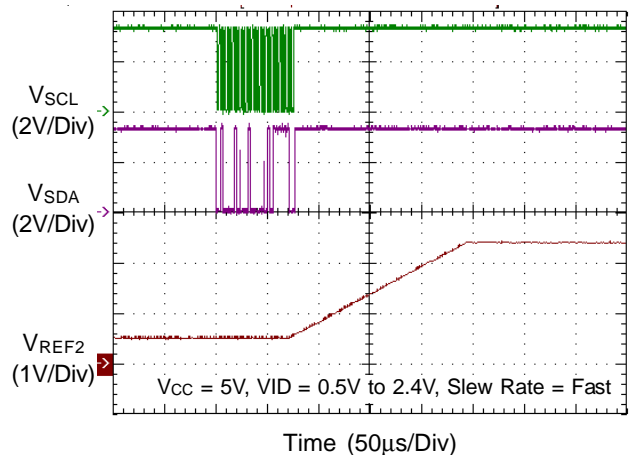
**VREF1 Dynamic VID Up**



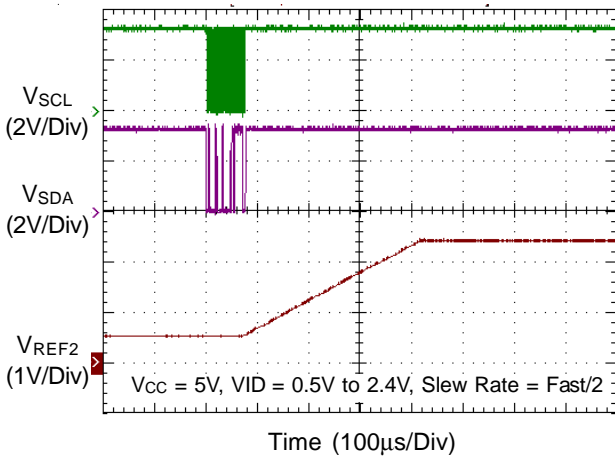
**VREF1 Dynamic VID Up**



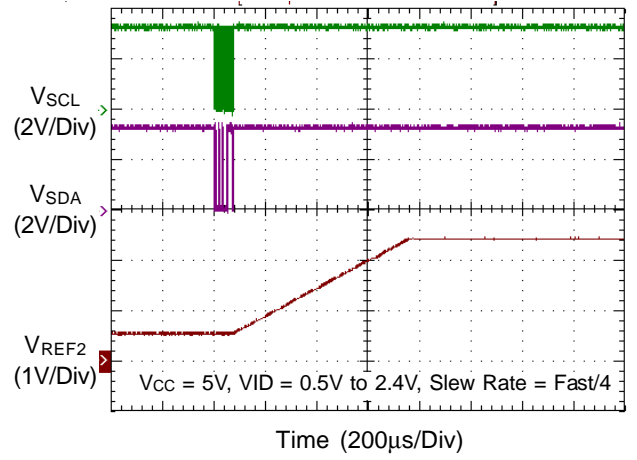
**VREF2 Dynamic VID Up**



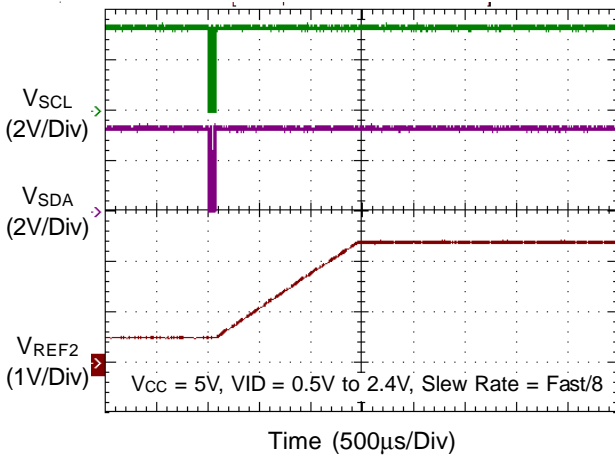
VREF2 Dynamic VID Up



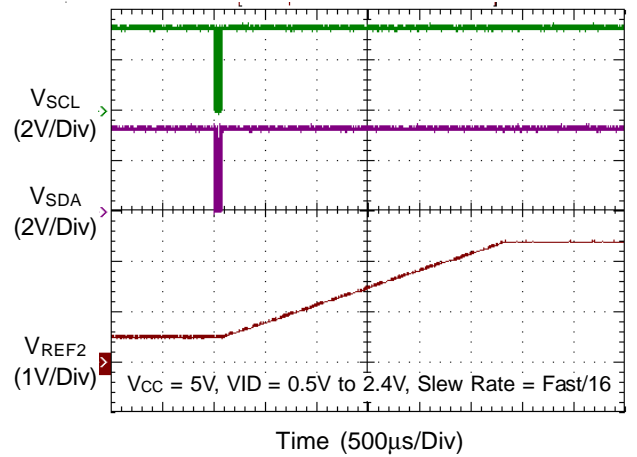
VREF2 Dynamic VID Up



VREF2 Dynamic VID Up



VREF2 Dynamic VID Up



## Application information

The RT9406 is a universal DAC generator that supports VID on-the-fly function with five different slew rates : Fast Fast, Fast/2, Fast/4, Fast/8 and Fast/16. An I<sup>2</sup>C interface is built in the R9406 to communicate with microprocessor.

### I<sup>2</sup>C Interface

The RT9406 adopts I<sup>2</sup>C interface for VREF control. I<sup>2</sup>C is a two wire (SCL, SDA) serial synchronous interface used to transfer power management information. The clock signal is provided from and synchronized with the microprocessor, and the microprocessor drives the SCL signal with a low-voltage open-drain driver. The master may shut down the SCL signal to save power when no data transfer is needed. SDA is a low-voltage, open-drain data signal that master and slaves use to transfer information to each other. The operation frequency can be up to 1MHz.

### Initial Vref Setting

The RT9406 supports the PINSET1 and PINSET2 pins to determine the initial voltage of VREF1 and VREF2 pins. The Vini detector keeps detecting the PINSETx voltage after V<sub>CC</sub> slewing through POR threshold. And the initial VREFx voltage begins to track Vini detector voltage with fast/4 slew rate after V<sub>CC</sub> slewing through UVLO threshold.

### Vref and Slew Rate Control Register

The voltage of VREF1 and VREF2 pins is controlled by I<sup>2</sup>C interface. The Vref1 register address is 0x10 and the Vref2 register address is 0x20. Besides, the slew rate of Vref1 and Vref2 is changed by 0x12 and 0x22, individually. The Table 2 shows the register data definition.

**Table 2. Register Data Definition**

Register Data	Note
0x0	1/2 Fast SR
0x1	1/4 Fast SR
0x2	1/8 Fast SR
0x3	1/16 Fast SR
0x4	Fast SR

### Chip Input and Enable

The RT9406 operates with a well regulated supply input at VCC pin. A minimum 2.2μF ceramic capacitor physically near the VCC pin is required for locally bypassing the supply noise.

### Under-Voltage Lockout (UVLO)

During normal operation, if the voltage at the VCC pin drops below UVLO threshold 3.9V (min), the RT9406 will trigger UVLO and force all function off.

### I<sup>2</sup>C Address Selection

The RT9406 support the I<sup>2</sup>C address selection through adjusting the PINSET2 Voltage. The PINSET2 voltage detection for I<sup>2</sup>C address selection has two conditions. One is PINSET2 voltage is get at V<sub>CC</sub> slewing to UVLO threshold when V<sub>CC</sub> slews from POR threshold to UVLO threshold is larger than 110μs. The other is PINSET2 voltage is obtained at V<sub>CC</sub> going through POR threshold with 110μs delay when V<sub>CC</sub> slews from POR threshold to UVLO threshold is less than 110μs. There are three comparators compare PINSET2 voltage to determine I<sup>2</sup>C address. Table 3 shows the I<sup>2</sup>C address including the write bit in address and Table 4 shows the other way to describe I<sup>2</sup>C address without the write bit.

**Table 3. I<sup>2</sup>C Address Including the Write Bit in Address**

PINSET2 Voltage	I <sup>2</sup> C Address
$V_{PINSET2} < 2$	0x40
$2 \leq V_{PINSET2} < 2.5$	0x42
$2.5 \leq V_{PINSET2} < 3$	0x44
$3 \leq V_{PINSET2}$	0x46

**Table 4. I<sup>2</sup>C Address Without the Write Bit in Address**

PINSET2 Voltage	I <sup>2</sup> C Address
$V_{PINSET2} < 2$	0x20
$2 \leq V_{PINSET2} < 2.5$	0x21
$2.5 \leq V_{PINSET2} < 3$	0x22
$3 \leq V_{PINSET2}$	0x23

## Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where  $T_{J(MAX)}$  is the maximum junction temperature,  $T_A$  is the ambient temperature, and  $\theta_{JA}$  is the junction to ambient thermal resistance.

For recommended operating condition specifications, the maximum junction temperature is 125°C. The junction to ambient thermal resistance,  $\theta_{JA}$ , is layout dependent. For SOT-23-8 package, the thermal resistance,  $\theta_{JA}$ , is 186.2°C/W on a standard JEDEC 51-7 four-layer thermal test board. The maximum power dissipation at  $T_A = 25^\circ\text{C}$  can be calculated by the following formula :

$$P_{D(MAX)} = (125^\circ\text{C} - 25^\circ\text{C}) / (186.2^\circ\text{C/W}) = 0.53\text{W for SOT-23-8 package}$$

The maximum power dissipation depends on the operating ambient temperature for fixed  $T_{J(MAX)}$  and thermal resistance,  $\theta_{JA}$ . The derating curve in Figure 1 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

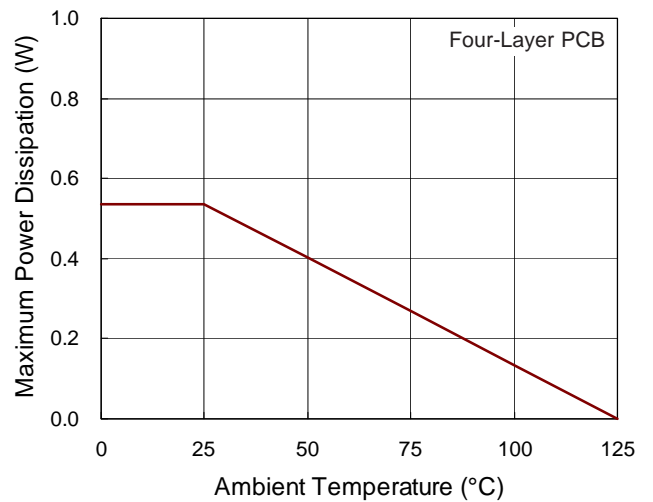
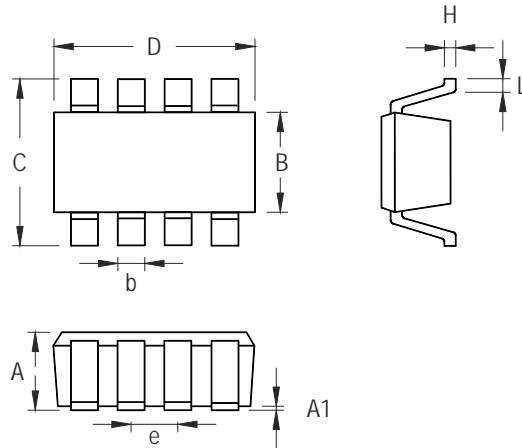


Figure 1. Derating Curve of Maximum Power Dissipation



**Outline Dimension**



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.000	1.450	0.039	0.057
A1	0.000	0.150	0.000	0.006
B	1.500	1.700	0.059	0.067
b	0.220	0.500	0.009	0.020
C	2.600	3.000	0.102	0.118
D	2.800	3.000	0.110	0.118
e	0.585	0.715	0.023	0.028
H	0.100	0.220	0.004	0.009
L	0.300	0.600	0.012	0.024

**SOT-23-8 Surface Mount Package**

**Richtek Technology Corporation**

14F, No. 8, Tai Yuen 1<sup>st</sup> Street, Chupei City  
 Hsinchu, Taiwan, R.O.C.  
 Tel: (8863)5526789

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