



RVT35HHBFWN00

EVE4 IPS 3.5" LCD TFT Datasheet

Rev.0.1

2021-01-18

ITEM	CONTENTS	UNIT
LCD Type	TFT/Transmissive/Normally black/IPS	/
Size	3.5	Inch
Viewing Direction	Free	/
Outside Dimensions (W × H × D)	93.50 × 62.00 × 8.65	mm
Active Area (W × H)	70.08 × 52.56	mm
Pixel Pitch (W × H)	0.219 × 0.219	mm
Resolution	320 (RGB) × 240	/
Brightness	1000	cd/m ²
Color Depth	16.7 M	/
Pixel Arrangement	RGB Vertical Stripe	/
Driver IC of Board	BT817Q	/
Interface	SPI/QSPI	/
Host Connector	RiBUS, ZIF 20 pin, 0.5mm pitch, down-side contact	/
With/Without Touch	Without touch panel	/
Supply Voltage for Module	3.3	V
Supply Voltage for Backlight	5.0 (TYP.)	V
Weight	TBD	g

Note 1: RoHS compliant

Note 2: LCM weight tolerance: ± 5%.

REVISION RECORD

REV NO.	REV DATE	CONTENTS	REMARKS
0.1	2021-01-18	Preliminary	

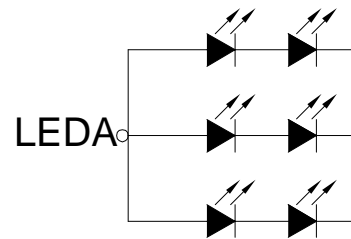
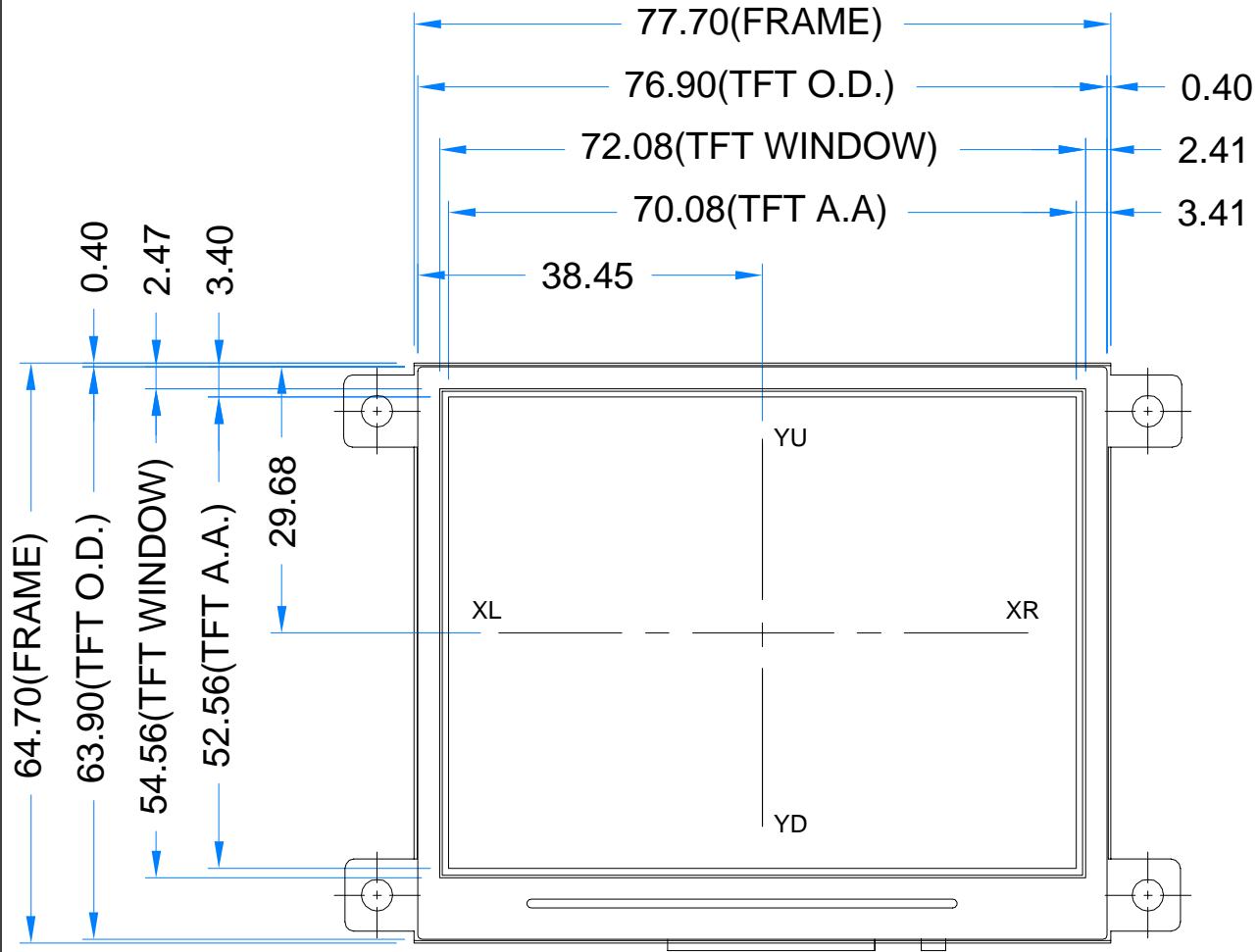
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1 MODULE CLASSIFICATION INFORMATION

RV	T	35	H	H	B	F	W	N	00
1.	2.	3.	4.	5.	6.	7.	8.	9.	10.

1.	BRAND	RV – Riverdi
2.	PRODUCT TYPE	T – TFT Standard
3.	DISPLAY SIZE	35 – 3.5”
4.	MODEL SERIAL NO.	H – High Brightness, IPS
5.	RESOLUTION	H –320 x 240 px
6.	INTERFACE	B – SPI/QSPI
7.	FRAME	F – With Frame
8.	BACKLIGHT TYPE	W – LED White
9.	TOUCH PANEL	N – Without Touch Panel
10.	VERSION	00 – (00-99)



TFT NOTES:

1. LCD TYPE: TRANSMISSIVE, NORMALLY BLACK, IPS
2. RESOLUTION: 320x240
3. VIEWING ANGLE: FREE
4. SURFACE LUMINANCE: 1000 cd/m²
5. DRIVING IC ON THE BOARD: BT817Q
6. INTERFACE: SPI/QSPI
7. SUPPLY VOLTAGE FOR MODULE: 3.3V
8. SUPPLY VOLTAGE FOR BACKLIGHT: 5.0V(TYP.), BUILT-IN LED INVERTER

GENERAL NOTES:

1. OPERATING TEMPERATURE: -20°C ~ 70°C
2. STORAGE TEMPERATURE: -30°C ~ 80°C
3. WITHOUT INDIVIDUAL TOLERANCE: ±0.3mm
4. RoHS3 COMPLIANT

3 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	MIN	MAX	UNIT	NOTE
Supply Voltage for Module	VDD	0	4	V	Note 1
Digital I/O signals (SPI/QSPI/GPIO) Voltage	VIN	-0.5	5.5	V	Note 1, 2
Supply voltage for Backlight	BLVDD	-0.3	6	V	Note 1
Operating Temperature	T _{OP}	-20	70	°C	
Storage Temperature	T _{ST}	-30	80	°C	
Storage Humidity (@ 25 ± 5°C)	H _{ST}	10	-	% RH	
Operating Ambient Humidity (@ 25 ± 5°C)	H _{OP}	10	-	% RH	

Note 1. Exceeding the maximum values may cause improper operation or permanent damage to the unit.

Note 2. Digital I/O signals are to be connected to pins 3 ÷ 9, 11 and 12 pins at RiBUS connector (P1).

4 ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage for Module	VDD	3.0	3.3	3.6	V	
Current drawn from VDD	I _{VDD}	TBD	180	TBD	mA	Note 1
Input Voltage "H" Level	V _{IH}	2.0	TBD	3.3	V	Note 1
Input Voltage "L" Level	V _{IL}	0	TBD	0.8	V	Note 1

Note 1. These values will be announced after the samples have been tested.

5 BACKLIGHT ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE
Supply Voltage for Backlight	BLVDD	2.7	5.0	6.0	V	
Current drawn from BLVDD @5.0V	I _{BLVDD=5.0V}	TBD	150	TBD	mA	100% of backlight, Note 1
Current drawn from BLVDD@5.0V	I _{BLVDD=5.0 V}	TBD	65	TBD	mA	50% of backlight, Note 1
Current drawn from BLVDD @3.3V	I _{BLVDD=3.3V}	TBD	250	TBD	mA	100% of backlight, Note 1
Current drawn from BLVDD@3.3V	I _{BLVDD=3.3 V}	TBD	100	TBD	mA	50% of backlight, Note 1
Life Time	-	-	50,000	-	hours	Note 2

Note 1. Backlight intensity is driven by BT817Q controller by PWM wave from GPIO pin. Please refer to subchapter 8.4.

Note 2. Operating life means the period of time in which the LED brightness goes down to 50% of the initial brightness. Typical operating life time is the estimated parameter.

6 ELECTRO-OPTICAL CHARACTERISTICS

ITEM	SYMBOL	CONDITION	MIN	TYP	MAX	UNIT	REMARK	NOTE
Response Time	Tr+Tf	$\theta=0^\circ$ $\phi=0^\circ$ $T_a=25^\circ\text{C}$	-	30	-	ms	FIG 2.	4
Contrast Ratio	Cr		-	1000	-	---	FIG 3.	1
Luminance Uniformity	δ WHITE		-	75	-	%	FIG 3.	3
Surface Luminance	Lv		-	1000	-	cd/m ²	FIG 3.	2
Viewing Angle Range	θ	$\phi = 90^\circ$	-	80	-	deg	FIG 4.	6
		$\phi = 270^\circ$	-	80	-	deg	FIG 4.	
		$\phi = 0^\circ$	-	80	-	deg	FIG 4.	
		$\phi = 180^\circ$	-	80	-	deg	FIG 4.	
CIE (x, y) Chromaticity	Red	x	0.575	0.615	0.655	FIG 3.	5	
		y	0.296	0.336	0.376			
	Green	x	0.352	0.392	0.432			
		y	0.512	0.552	0.592			
	Blue	x	0.100	0.140	0.180			
		y	0.085	0.125	0.165			
	White	x	0.274	0.316	0.358			
		y	0.295	0.336	0.378			

Note 1. Contrast Ratio(CR) is defined mathematically as below, for more information see Figure 2.

$$\text{Contrast Ratio} = \frac{\text{Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Average Surface Luminance with all black pixels (P1, P2, P3, P4, P5)}}$$

Note 2. Surface luminance is the LCD surface from the surface with all pixels displaying white. For more information see Figure 3.

$$L_v = \text{Average Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}$$

Note 3. The uniformity in surface luminance δ WHITE is determined by measuring luminance at each test position 1 through 5, and then dividing the minimum luminance of 5 points luminance by maximum luminance of 5 points luminance. For more information see Figure 3.

$$\delta \text{ WHITE} = \frac{\text{Minimum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}{\text{Maximum Surface Luminance with all white pixels (P1, P2, P3, P4, P5)}}$$

Note 4. Response time is the time required for the display to transition from white to black (Rise Time, Tr) and from black to white (Decay Time, Tf). For additional information see Figure 1. The test equipment is Autronic-Melchers's ConoScope series.

Note 5. CIE (x, y) chromaticity, the x, y value is determined by measuring luminance at each test position 1 through 5, and then make average value.

Note 6. Viewing angle is the angle at which the contrast ratio is greater than 2. For TFT module the contrast ratio is greater than 10. The angles are determined for the horizontal or x axis and the vertical or y axis with respect to the z axis which is normal to LCD surface. For more information see Figure 4.

Note 7. For viewing angle and response time testing, the testing data is based on Autronic-Melchers's ConoScope series. Instruments for Contrast Ratio, Surface Luminance, Luminance Uniformity, CIE the test data is based on TOPCON's BM-5 photo detector.

Figure 2. The definition of response time

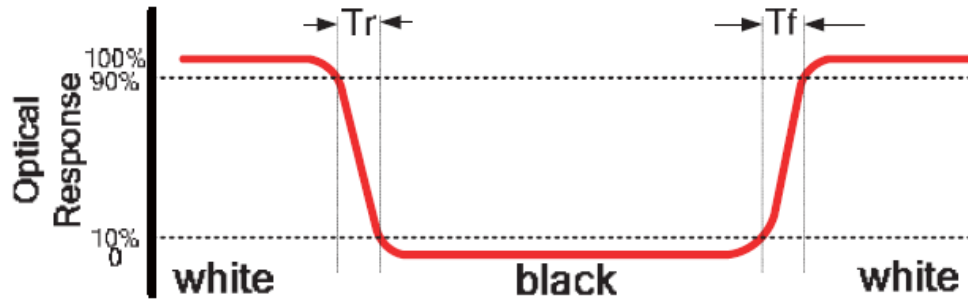


Figure 3. Measuring method for Contrast ratio, surface luminance, Luminance uniformity, CIE (x, y) chromaticity

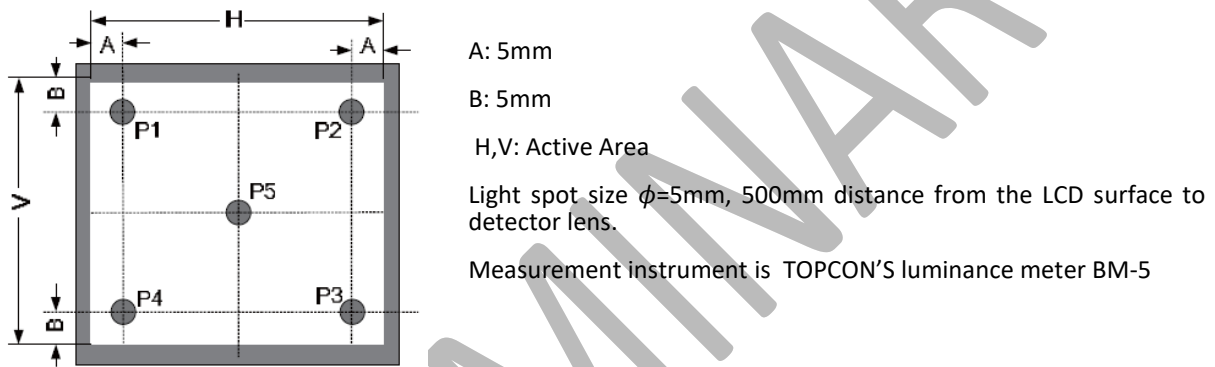
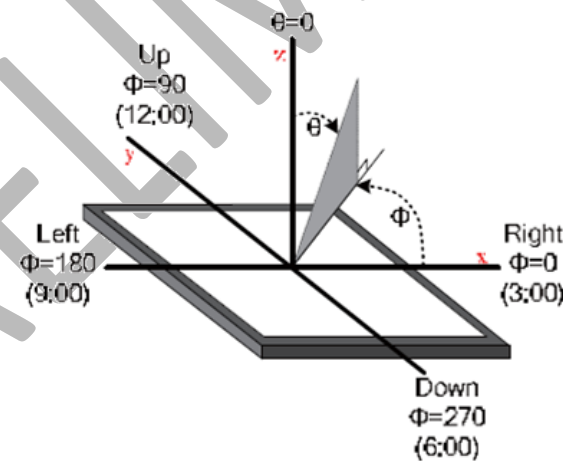


Figure 4. The definition of viewing angle



7 INTERFACE DESCRIPTION

7.1 P1 connector- RIBUS description

PIN NO.	SYMBOL	DESCRIPTION	NOTE
1	VDD	Supply voltage for module: 3.3 V	
2	GND	Ground	
3	SPI_SCLK	SPI SCK signal	
4	MISO/ IO.1	SPI MISO signal / SPI Quad mode: SPI data line 1	
5	MOSI/ IO.0	SPI MOSI signal / SPI Quad mode: SPI data line 0	
6	CS	SPI chip select signal	
7	INT	Interrupt signal from device to the system, Active Low, Internally 47k Pulled UP	
8	RST/PD	Reset / Power down signal, Active Low, Internally 47k Pulled UP	
9	GPIO.0	GPIO.0	
10	DISP_AUDIO	Display audio in/out	Note 1
11	GPIO.1/IO.2	SPI Single/Dual mode: General purpose IO0. QSPI mode: SPI data line 2	
12	GPIO.2/IO.3	SPI Single/Dual mode: General purpose IO1. QSPI mode: SPI data line 3	
13	NC	Not connected	
14	NC	Not connected	
15	NC	Not connected	
16	NC	Not connected	
17	BLVDD	Supply voltage for backlight	
18	BLVDD	Supply voltage for backlight	
19	BLGND	Backlight Ground, Internally connected to GND	
20	BLGND	Backlight Ground, Internally connected to GND	

Note 1. Requirements for audio external signal voltage will be announced after samples have been tested.

7.2 P2 connector description

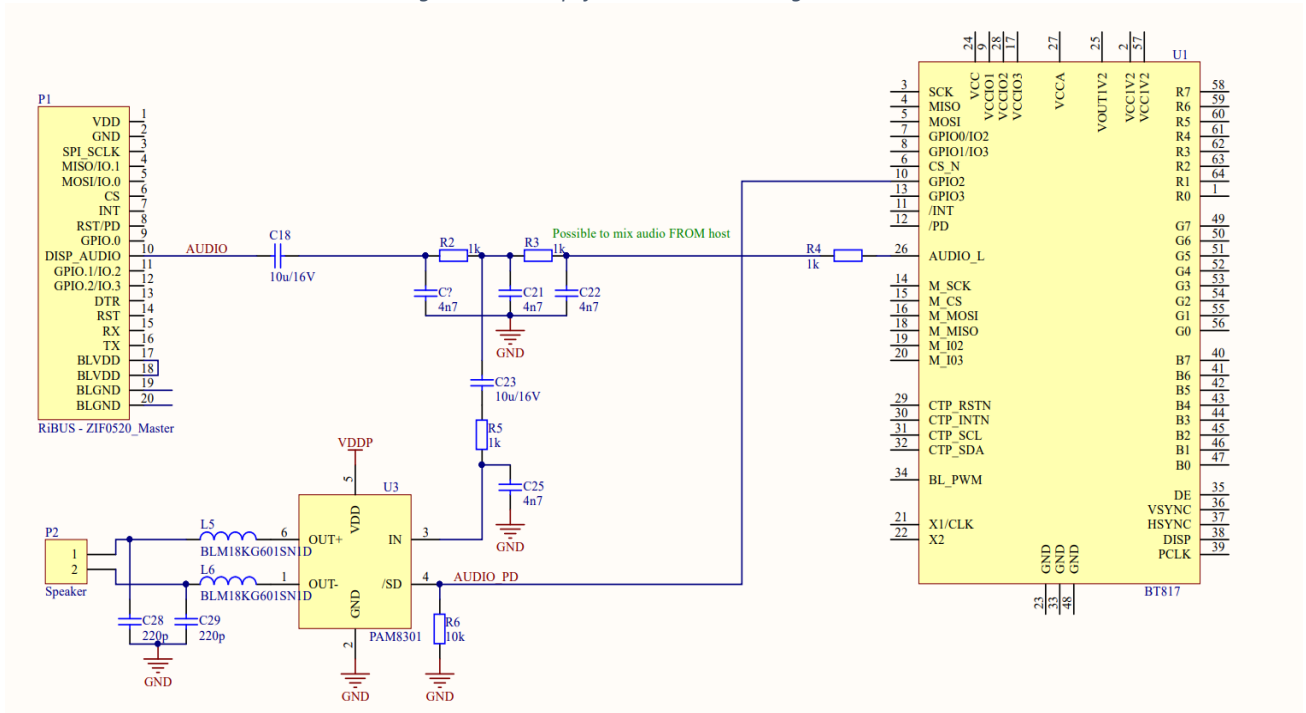
PIN NO.	SYMBOL	DESCRIPTION	NOTE
1	SPEAKER +	Speaker coil "+" terminal	Note 1
2	SPEAKER -	Speaker coil "-" terminal	

The audio circuit allows for the following 3 things:

1. To play sounds from BT817Q on internal amplifier U3.
2. To play sounds from host on internal amplifier U3.
3. To play sounds from BT817Q on external amplifier.

Note 1. The loudspeaker assembly (loudspeaker + cables + plug compatible with P2 connector) will be sold separately. The documentation of the loudspeaker assembly will be released soon.

Figure 5. The simplified audio circuit design



Note 2. By standard, the EVE4 board is equipped with the separate 256Mb Flash memory chip, which allows to show up to 270 full resolution (320 * 240 pixels, JPG) images. If you need to change the memory size, please contact us: contact@riverdi.com

8 BT817Q CONTROLLER SPECIFICATION

BT817Q or EVE4 (Embedded Video Engine 4) simplifies the system architecture for advanced human machine interfaces (HMIs) by providing functionality for display, audio, and touch as well as an object oriented architecture approach that extends from display creation to the rendering of the graphics.

8.1 Serial host interface

Figure 6. SPI single/dual interface connection

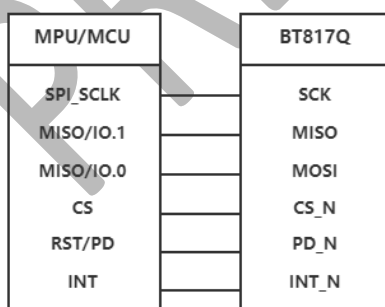
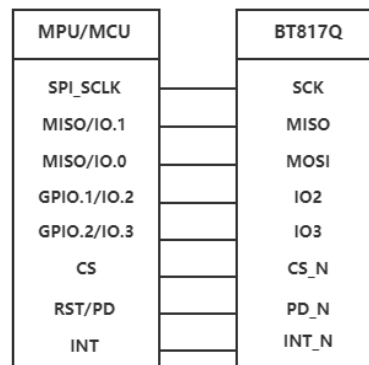


Figure 7. QSPI interface connection



SPI Interface – the SPI slave interface operates up to 30MHz (It depends on EVE4 system clock frequency and needs verification in Riverdi lab).

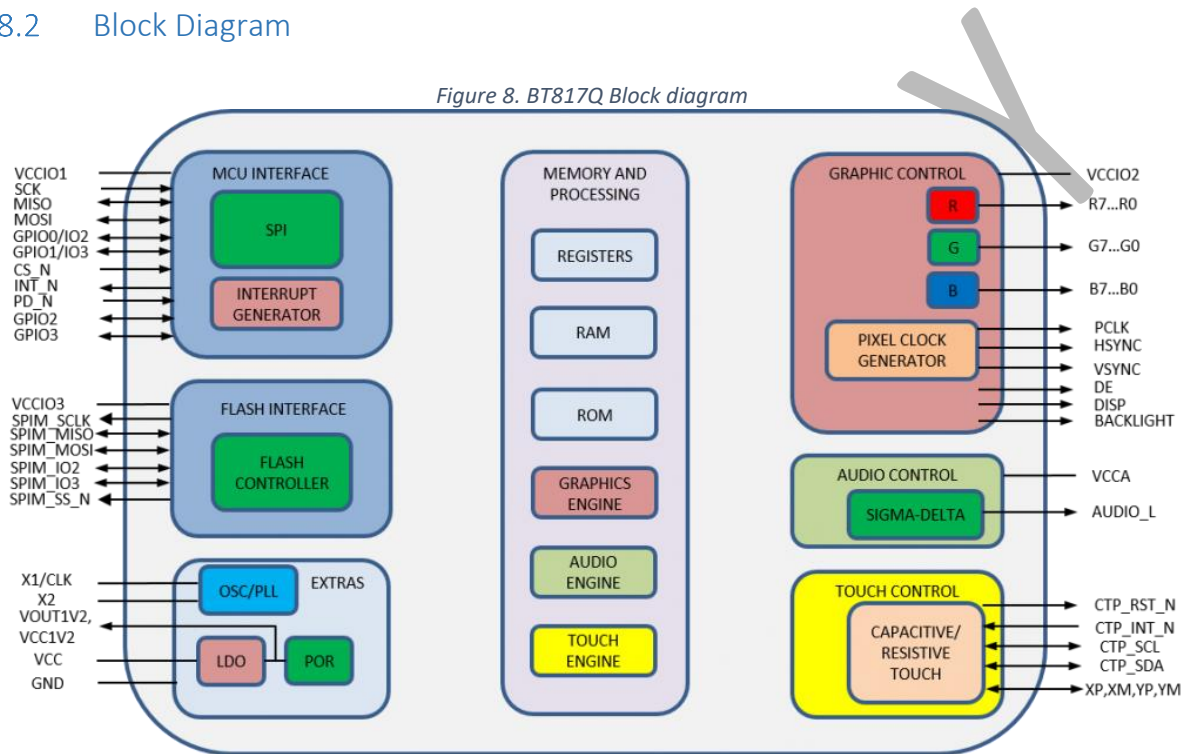
Only SPI mode 0 is supported. The SPI interface is selected by default (MODE pin is internally pulled low by 47k resistor).

QSPI Interface – the QSPI slave interface operates up to 30MHz (It depends on EVE 4 system clock frequency and will be verified in Riverdi lab). Only SPI mode 0 is supported. The QSPI can be configured as a SPI slave in SINGLE, DUAL or QUAD channel modes.

By default the SPI slave operates in the SINGLE channel mode with MOSI as input from the master and MISO as output to the master. DUAL and QUAD channel modes can be configured through the SPI slave itself. To change the channel modes, write to register REG_SPI_WIDTH.

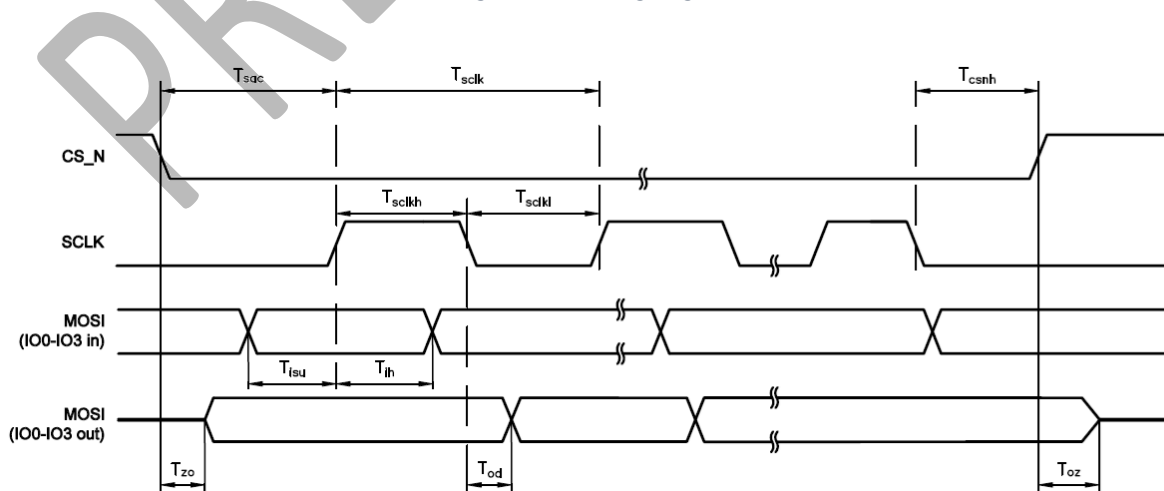
8.2 Block Diagram

Figure 8. BT817Q Block diagram



8.3 Host interface SPI mode 0

Figure 9. SPI timing diagram



The meanings of the timings in the Figure 9 are defined in the table below.

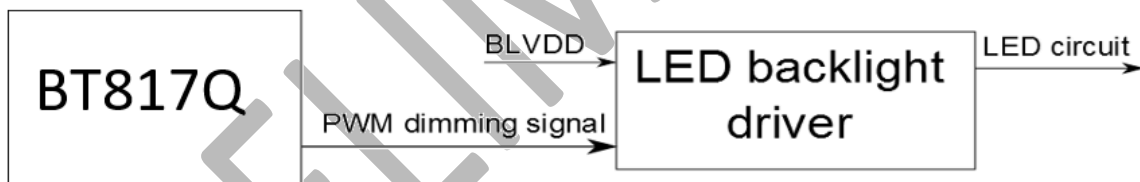
PARAMETER	DESCRIPTION	VCCIO=1.8V		VCCIO=2.5V		VCCIO=3.3V		UNIT
		Min	Max	Min	Max	Min	Max	
T _{sclk}	SPI clock period	33.3		33.3		33.3		ns
T _{sckl}	SPI clock low duration	13		13		13		ns
T _{sckh}	SPI clock high duration	13		13		13		ns
T _{sac}	SPI access time	4		3.5		3		ns
T _{isu}	Input Setup	4		3.5		3		ns
T _{ih}	Input Hold	0		0		0		ns
T _{zo}	Output enable delay		16		13	11		ns
T _{oz}	Output disable delay		13		11	10		ns
T _{od}	Output data delay		15		12	11		ns
T _{csnh}	CSN hold time	0		0		0		ns

For more information about BT817Q controller please go to official BT81x website. <https://brtchip.com/bt81x/>

8.4 Backlight driver block diagram

Backlight enable signal is internally connected to BT817Q backlight control pin. This pin is controlled by two BT817Q's registers. One of them specifies the PWM output frequency, second one specifies the duty cycle. Refer to BT817Q datasheet for more information. After we have done the test on samples, more detailed description will be given in this document.

Figure 10. Backlight driver block diagram



The LED backlight driver used in this module does not burst the LED current. Therefore, it does not generate audible noises on the output capacitor. It is equipped with soft start subsystem, which increases LED life time, as LED current peaks are reduced significantly.

9 TIMING CHARACTERISTICS

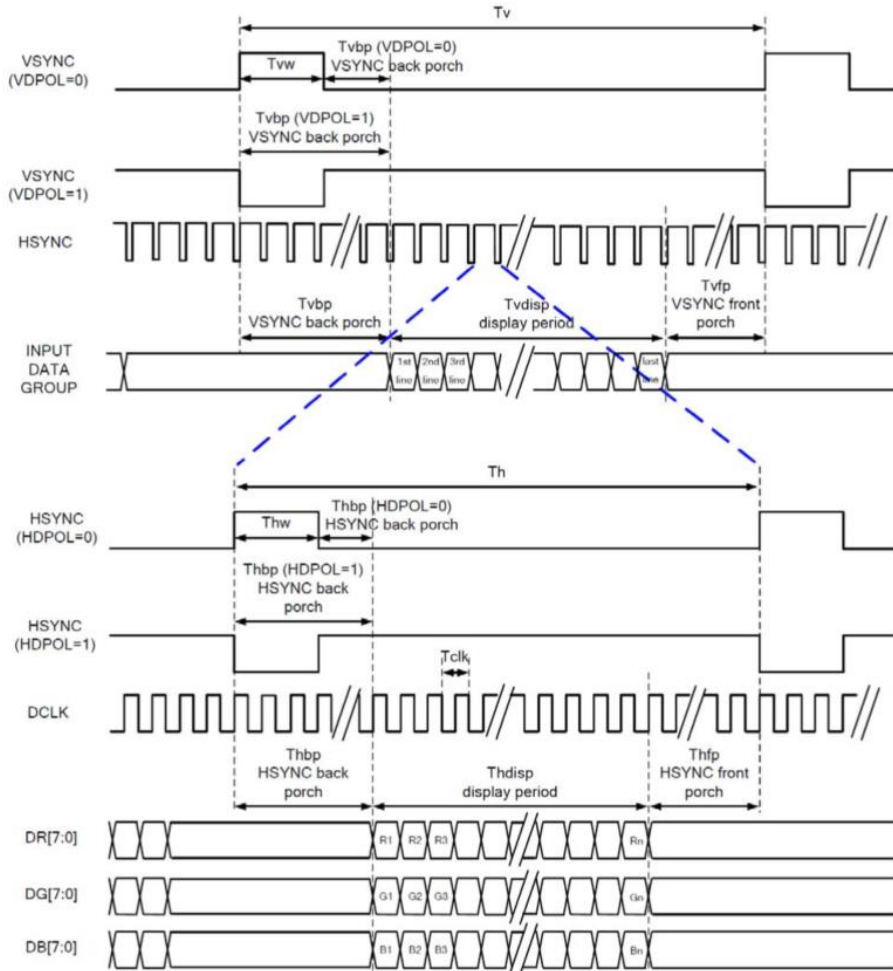
9.1 Input setup timing setting

RGB MODE SELECTION	DCLK	HSYNC	VSYNC	DE
SYNC-DE Mode	Input	Input	Input	Input
SYNC Mode	Input	Input	Input	GND
DE Mode	Input	GND	GND	Input

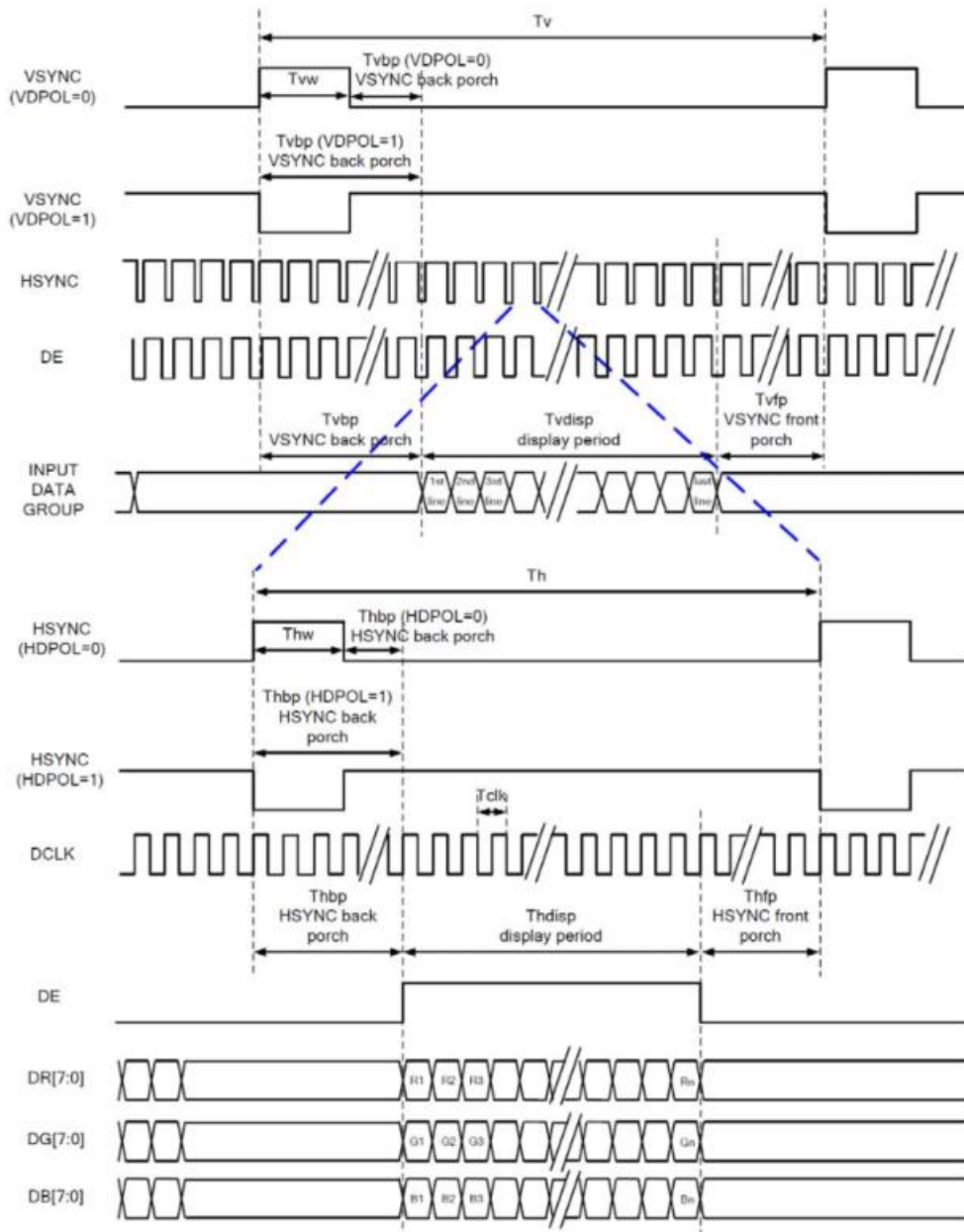
9.1.1 Parallel 24-bit RGB Timing Table

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	NOTE	
DCLK Frequency	F_{clk}	5	6	8	MHz		
DCLK Period	T_{clk}	125	167	200	ns		
HSYNC	Period Time	T_h	325	371	438	DCLK	
	Display Period	T_{hdisp}	320			DCLK	
	Back Porch	T_{hbp}	3	43	43	DCLK	SYNC mode back porch control by H_BLANKING [7:0] setting $T_{hbp} = H_BLANKING [7:0]$
	Front Porch	T_{hfp}	2	8	75	DCLK	
	Pulse Width	T_{hw}	2	4	43	DCLK	
VSYNC	Period Time	T_v	244	260	289	HSYNC	
	Display Period	T_{vdisp}	240			HSYNC	
	Back Porch	T_{vbp}	2	12	12	HSYNC	SYNC mode back porch control by V_BLANKING [7:0] setting $T_{vbp} = V_BLANKING [7:0]$
	Front Porch	T_{vfp}	2	8	37	HSYNC	
	Pulse Width	T_{vw}	2	4	12	HSYNC	

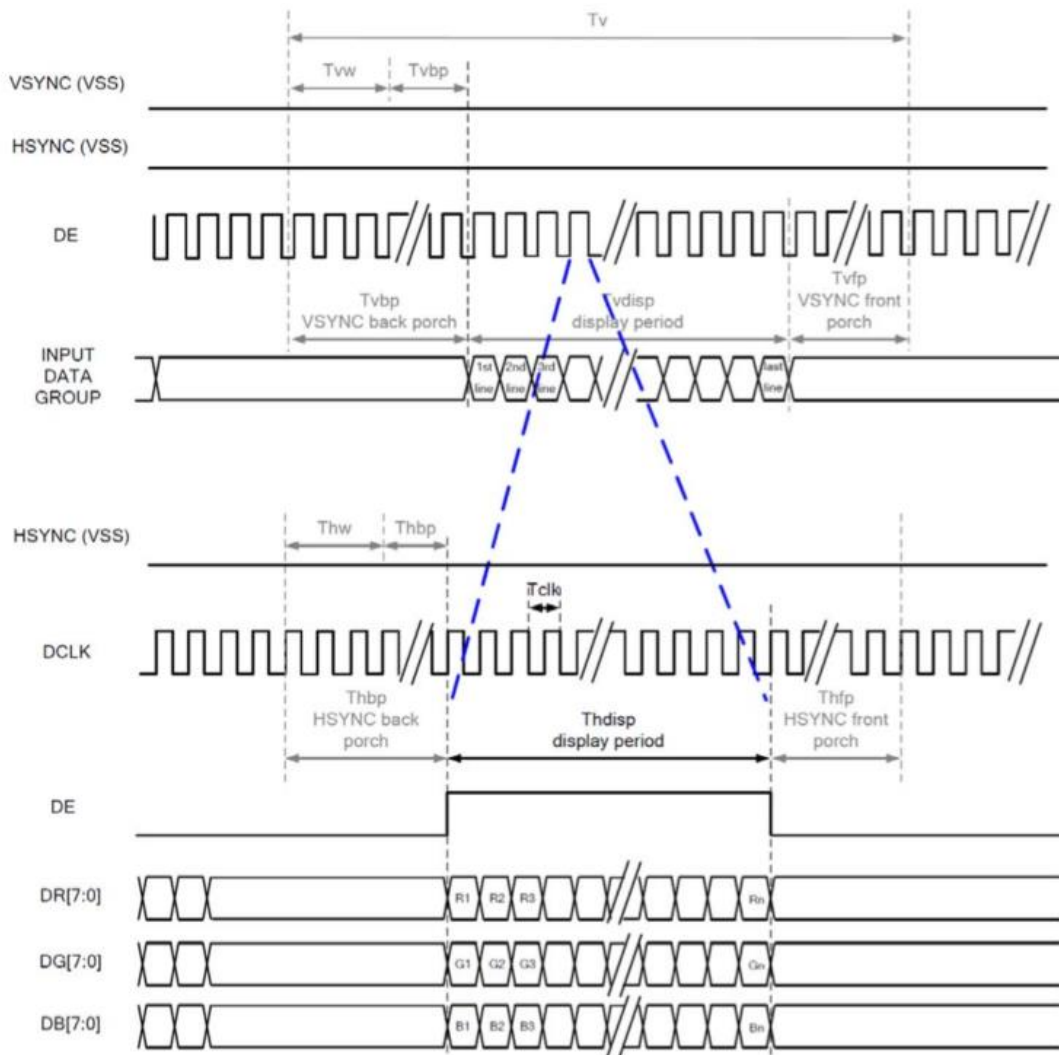
Note. It is necessary to keep $T_{vbp}=12$ and $T_{hbp}=43$ in sync mode. In DE mode it is not necessary.



9.1.2 SYNC-DE mode timing diagram

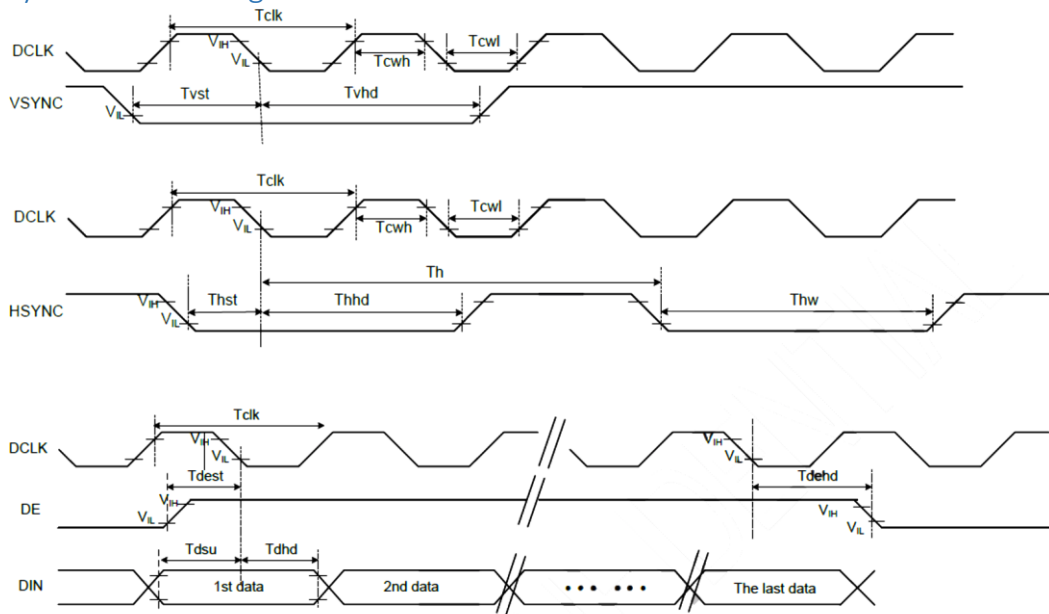


9.1.3 DE mode timing diagram



PREL

9.2 System Bus Timing for RGB Interface



PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
CLK Pulse Duty	T_{clk}	40	50	60	%
HSYNC Width	T_{hw}	2	-	-	DCLK
HSYNC Period	T_h	55	60	65	CLK
VSYNC Setup Time	T_{vst}	12	-	-	ns
VSYNC Hold Time	T_{vhd}	12	-	-	ns
HSYNC Setup Time	T_{hst}	12	-	-	ns
HSYNC Hold Time	T_{hhd}	12	-	-	ns
Data Setup Time	T_{dsu}	12	-	-	ns
Data Hold Time	T_{dhd}	12	-	-	ns
DE Setup Time	T_{dest}	12	-	-	ns
DE Hold Time	T_{dehd}	12	-	-	ns

10 INITIALIZATION CODE

This paragraph will be published in next versions of this datasheet.

PRELIMINARY

11 INSPECTION

Standard acceptance/rejection criteria for TFT module.

11.1 Inspection condition

Ambient conditions:

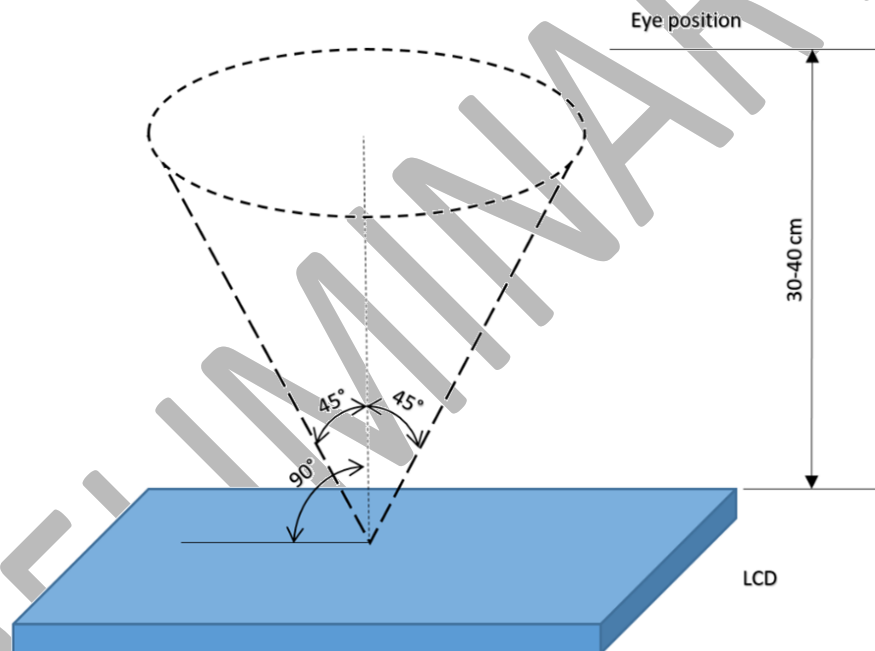
- Temperature: 25 ± 2 °C
- Humidity: (60 ± 10) %RH
- Illumination: Single fluorescent lamp, non-directive (300 to 700 lux)

Viewing distance:

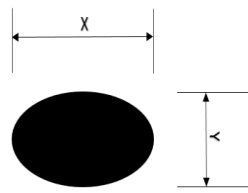
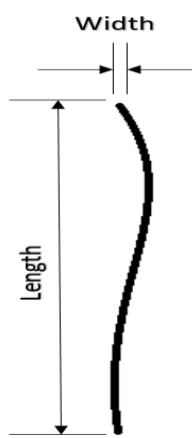
35 ± 5 cm between inspector bare eye and LCD.

Viewing Angle:

U/D: $45^\circ/45^\circ$, L/R: $45^\circ/45^\circ$



11.2 Inspection standard

Item	Criterion																		
Black spots, white spots, light leakage, Foreign Particle (round Type)	 $D = \frac{(x + y)}{2}$ <p>*Spots density: 10 mm</p> <table border="1" data-bbox="758 392 1364 593"> <thead> <tr> <th colspan="2">3.5" ≤ Size ≤ 5"</th> </tr> <tr> <th>Average Diameter</th> <th>Qualified Qty</th> </tr> </thead> <tbody> <tr> <td>D ≤ 0.15 mm</td> <td>Ignored</td> </tr> <tr> <td>0.15 mm < D ≤ 0.30 mm</td> <td>N ≤ 3</td> </tr> <tr> <td>0.3mm < D</td> <td>Not allowed</td> </tr> </tbody> </table>	3.5" ≤ Size ≤ 5"		Average Diameter	Qualified Qty	D ≤ 0.15 mm	Ignored	0.15 mm < D ≤ 0.30 mm	N ≤ 3	0.3mm < D	Not allowed								
3.5" ≤ Size ≤ 5"																			
Average Diameter	Qualified Qty																		
D ≤ 0.15 mm	Ignored																		
0.15 mm < D ≤ 0.30 mm	N ≤ 3																		
0.3mm < D	Not allowed																		
LCD black spots, white spots, light leakage (line Type)	 <p>*Spots density: 10 mm</p> <table border="1" data-bbox="758 884 1380 1131"> <thead> <tr> <th colspan="3">3.5" ≤ Size ≤ 5"</th> </tr> <tr> <th>Length/mm</th> <th>Width/mm</th> <th>Qualified Qty</th> </tr> </thead> <tbody> <tr> <td>-</td> <td>W ≤ 0.03</td> <td>Ignored</td> </tr> <tr> <td>L ≤ 3.0</td> <td>0.03 < W ≤ 0.05</td> <td>2</td> </tr> <tr> <td>L ≤ 3.0</td> <td>0.05 < W ≤ 0.1</td> <td>1</td> </tr> <tr> <td>3.0 < L</td> <td>0.1 < W</td> <td>Not allowed</td> </tr> </tbody> </table>	3.5" ≤ Size ≤ 5"			Length/mm	Width/mm	Qualified Qty	-	W ≤ 0.03	Ignored	L ≤ 3.0	0.03 < W ≤ 0.05	2	L ≤ 3.0	0.05 < W ≤ 0.1	1	3.0 < L	0.1 < W	Not allowed
3.5" ≤ Size ≤ 5"																			
Length/mm	Width/mm	Qualified Qty																	
-	W ≤ 0.03	Ignored																	
L ≤ 3.0	0.03 < W ≤ 0.05	2																	
L ≤ 3.0	0.05 < W ≤ 0.1	1																	
3.0 < L	0.1 < W	Not allowed																	
Bright/Dark Dots	<table border="1" data-bbox="406 1377 1348 1579"> <thead> <tr> <th colspan="2">3.5" ≤ Size ≤ 5"</th> </tr> <tr> <th>item</th> <th>Qualified Qty</th> </tr> </thead> <tbody> <tr> <td>Bright Dots</td> <td>N ≤ 1</td> </tr> <tr> <td>Dark Dots</td> <td>N ≤ 2</td> </tr> <tr> <td>Total Bright and Dark Dots</td> <td>N ≤ 3</td> </tr> </tbody> </table>	3.5" ≤ Size ≤ 5"		item	Qualified Qty	Bright Dots	N ≤ 1	Dark Dots	N ≤ 2	Total Bright and Dark Dots	N ≤ 3								
3.5" ≤ Size ≤ 5"																			
item	Qualified Qty																		
Bright Dots	N ≤ 1																		
Dark Dots	N ≤ 2																		
Total Bright and Dark Dots	N ≤ 3																		

Item	Criterion	
Clear spots	Size < 5"	
	Average Diameter	Qualified Qty
	D < 0.2 mm	Ignored
	0.2 mm < D < 0.3 mm	3
	0.3 mm < D < 0.5 mm	2
	0.5 mm < D	0
	*Spots density: 10 mm	
Polarizer bubbles	3.5" ≤ Size ≤ 5"	
	Average Diameter	Qualified Qty
	D ≤ 0.2 mm	Ignored
	0.2 mm < D ≤ 0.3 mm	2
	0.3 mm < D ≤ 0.5mm	1
	0.5 mm < D	0
	Total Q'ty	3

PRELIMINARY

12 RELIABILITY TEST

NO.	TEST ITEM	TEST CONDITION	REMARK
1	High Temperature Storage	80 °C/120 hours	Note 1
2	Low Temperature Storage	-30 °C/120 hours	Note 1
3	High Temperature Operating	70 °C /120 hours	Note 1
4	Low Temperature Operating	-20 °C/120 hours	Note 1
5	High Temperature && High Humidity	Humidity 40 °C, 90 %RH, 120 hours	Note 1
6	Thermal Cycling Test (No operation)	-20 °C for 30 min, 70 °C for 30 min. 100 cycles. Then test at room temperature after 1 hour	Note 2
7	Damp Proof Test	40 °C, 90 %RH/120 hours	
8	Vibration Test	Frequency: 10 ÷ 55 Hz; Stroke: 1.5 mm; Sweep: 10 Hz ÷ 55 Hz ÷ 10 Hz; 2 hours for each direction of X, Y, Z (6 hours for total)	
9	Package Drop Test	Height: 60 cm 1 corner, 3 edges, 6 surfaces	
10	ESD Test	Air: ±2 kV, human body mode, 100 pF /1500 Ω	

Note 1. Sample quantity for each test item is 5 ÷ 10 pcs.

Note 2. Before cosmetic and function test, the product must have enough recovery time, at least 2 hours at room temperature.

13 LEGAL INFORMATION

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