

CA3059, CA3079

Zero-Voltage Switches for 50-60Hz and 400Hz Thyristor Control Applications

The CA3059 and CA3079 zero-voltage switches are monolithic silicon integrated circuits designed to control a thyristor in a variety of AC power switching applications for AC input voltages of 24V, 120V, 208/230V, and 277V at 50-60Hz and 400Hz.

Rochester Electronics Manufactured Components

Rochester branded components are manufactured using either die/wafers purchased from the original suppliers or Rochester wafers recreated from the original IP. All recreations are done with the approval of the OCM.

Parts are tested using original factory test programs or Rochester developed test solutions to guarantee product meets or exceeds the OCM data sheet.

Quality Overview

- ISO-9001
- AS9120 certification
- Qualified Manufacturers List (QML) MIL-PRF-38535
 - Class Q Military
 - Class V Space Level
- Qualified Suppliers List of Distributors (QSLD)
 - Rochester is a critical supplier to DLA and meets all industry and DLA standards.

Rochester Electronics, LLC is committed to supplying products that satisfy customer expectations for quality and are equal to those originally supplied by industry manufacturers.

The original manufacturer's datasheet accompanying this document reflects the performance and specifications of the Rochester manufactured version of this device. Rochester Electronics guarantees the performance of its semiconductor products to the original OEM specifications. 'Typical' values are for reference purposes only. Certain minimum or maximum ratings may be based on product characterization, design, simulation, or sample testing.

CA3059 CA3079

Zero-Voltage Switches for 50-60Hz and 400Hz Thyristor Control Applications

May 1992

Features

- Relay Control
- Valve Control
- Synchronous Switching of Flashing Lights
- On-Off Motor Switching
- Differential Comparator with Self-Contained Power Supply for Industrial Applications
- Photosensitive Control
- Power One-Shot Control
- Heater Control
- Lamp Control

Type Features

	CA3059	CA3079
• 24V, 120V, 208/230V, 277V at 50/60 or 400Hz Operation	X	X
• Differential Input	X	X
• Low Balance Input Current (Max) - μ A. . .	1	2
• Built-In Protection Circuit for Opened or Shorted Sensor (Term 14)	X	X
• Sensor Range (Rx) - k Ω	2 - 100	2 - 50
• DC Mode (Term 12)	X	
• External Trigger (Term 6).	X	
• External Inhibit (Term 1)	X	
• DC Supply Volts (Max)	14	10
• Operating Temperature Range ($^{\circ}$ C) . . .	-55 to +125	

Description

The CA3059 and CA3079 zero-voltage switches are monolithic silicon integrated circuits designed to control a thyristor in a variety of AC power switching applications for AC input voltages of 24V, 120V, 208/230V, and 277V at 50-60Hz and 400Hz. Each of the zero-voltage switches incorporates 4 functional blocks (see the Functional Block Diagram) as follows:

1. Limiter-Power Supply - Permits operation directly from an AC line.
2. Differential On/Off Sensing Amplifier - Tests the condition of external sensors or command signals. Hysteresis or proportional-control capability may easily be implemented in this section.
3. Zero-Crossing Detector - Synchronizes the output pulses of the circuit at the time when the AC cycle is at zero voltage point; thereby eliminating radio-frequency interference (RFI) when used with resistive loads.
4. Triac Gating Circuit - Provides high-current pulses to the gate of the power controlling thyristor.

In addition, the CA3059 provides the following important auxiliary functions (see the Functional Block Diagram).

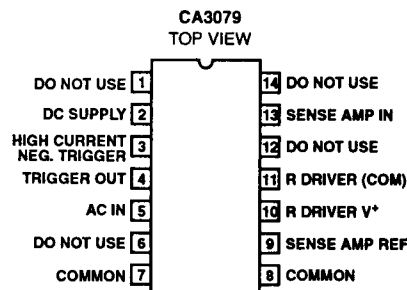
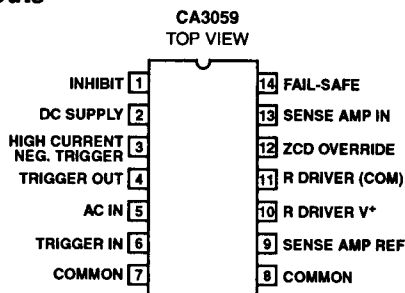
1. A built-in protection circuit that may be actuated to remove drive from the triac if the sensor opens or shorts.
2. Thyristor firing may be inhibited through the action of an internal diode gate connected to Terminal 1.
3. High-power dc comparator operation is provided by overriding the action of the zero-crossing detector. This is accomplished by connecting Terminal 12 to Terminal 7. Gate current to the thyristor is continuous when Terminal 13 is positive with respect to Terminal 9.

The CA3059 and CA3079 are supplied in 14 lead dual-inline plastic packages. They are also available in chip form (H suffix).

Ordering Information

PART NUMBER	TEMPERATURE	PACKAGE
CA3059	-55 $^{\circ}$ C to +125 $^{\circ}$ C	14 Lead Plastic DIP
CA3079	-55 $^{\circ}$ C to +125 $^{\circ}$ C	14 Lead Plastic DIP
CA3059H	+25 $^{\circ}$ C	Dice
CA3079H	+25 $^{\circ}$ C	Dice

Pinouts

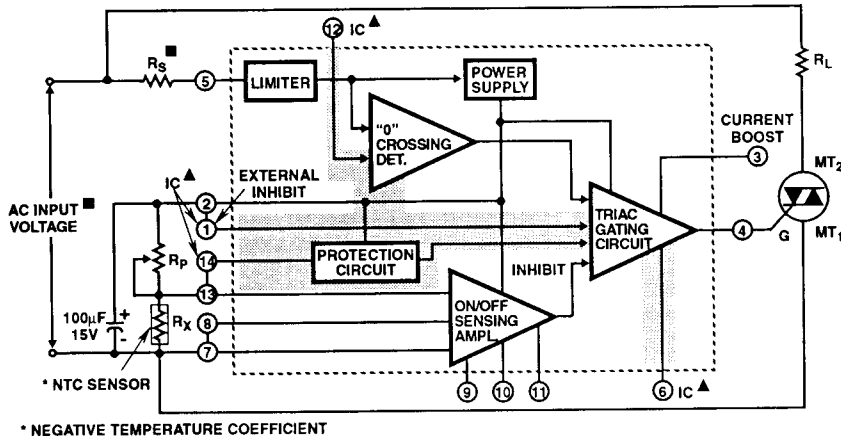


5

AC TO DC
CONVERTERS

CA3059, CA3079

Functional Block Diagram



AC INPUT VOLTAGE (50/60 OR 400Hz) V AC	INPUT SERIES RESISTOR (R _S) kΩ	DISSIPATION RATING FOR R _S W
24	2	0.5
120	10	2
208/230	20	4
277	25	5

NOTE: Circuitry within shaded areas, not included in CA3079

■ See chart

▲ IC = Internal connection - DO NOT USE (Terminal restriction applies only to CA3079)

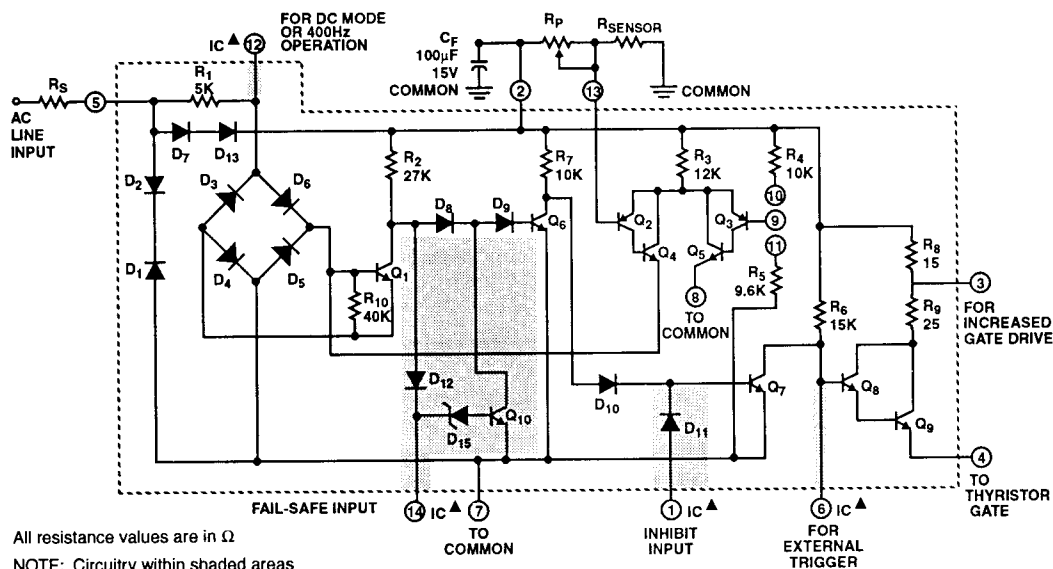


FIGURE 1. SCHEMATIC DIAGRAM OF CA3059 AND CA3079

Specifications CA3059, CA3079

Absolute Maximum Ratings $T_A = +25^\circ\text{C}$

DC Supply Voltage (Between Terminals 2 & 7) CA3059 14V CA3079 10V DC Supply Voltage (Between Terminals 2 & 8) CA3059 14V CA3079 10V Peak Supply Current (Terminals 5 & 7) $\pm 50\text{mA}$ Output Pulse Current (Terminal 4) 150mA	Power Dissipations Up to $T_A = +55^\circ\text{C}$ CA3059, CA3079 700mW Above $T_A = +55^\circ\text{C}$ CA3059, CA3079 Derate Linearly 6.67mW/ $^\circ\text{C}$ Ambient Temperature Operating -55°C to $+125^\circ\text{C}$ Storage -65°C to $+150^\circ\text{C}$ Lead Temperature (During Soldering) At distance $1/16" \pm 1/32"$ (1.59 ± 0.79) from case for 10 seconds max $+265^\circ\text{C}$
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CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Electrical Specifications $T_A = +25^\circ\text{C}$, For all Types, Unless Otherwise Specified. All voltages are measured with respect to Terminal 7. For Operating at 120V_{RMS}, 50-60Hz (AC Line Voltage) (Note 1)

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS	
			MIN	TYP	MAX		
DC SUPPLY VOLTAGE (Figure 2a, 2b, 2c)							
Inhibit Mode		V_S	$R_S = 8\text{k}\Omega, I_L = 0$	6.1	6.5	7	V
			$R_S = 10\text{k}\Omega, I_L = 0$	-	6.8	-	V
			$R_S = 5\text{k}\Omega, I_L = 0$	-	6.4	-	V
Pulse Mode		V_S	$R_S = 8\text{k}\Omega, I_L = 0$	6	6.4	7	V
			$R_S = 10\text{k}\Omega, I_L = 0$	-	6.7	-	V
			$R_S = 5\text{k}\Omega, I_L = 0$	-	6.3	-	V
GATE TRIGGER CURRENT (Figures 3, 4(a))		$I_{GT}(4)$	Terminals 3 and 2 connected, $V_{GT} = 1\text{V}$	-	105	-	mA
PEAK OUTPUT CURRENT (PULSED) (Figures 4, 5)							
With Internal Power Supply Figure 4a, 4b		$I_{OM}(4)$	Terminal 3 open, Gate Trigger Voltage (V_{GT}) = 0	50	84	-	mA
			Terminals 3 and 2 connected, Gate Trigger Voltage (V_{GT}) = 0	90	124	-	mA
With External Power Supply Figure 5a, 5b, 5c		$I_{OM}(4)$	Terminal 3 open, $V_+ = 12\text{V}, V_{GT} = 0$	-	170	-	mA
			Terminals 3 and 2 connected, $V_+ = 12\text{V}, V_{GT} = 0$	-	240	-	mA
INHIBIT INPUT RATIO (Figure 6)		V_9/V_2	Voltage Ratio of Terminals 9 to 2	0.465	0.485	0.520	-
TOTAL GATE PULSE DURATION (Note 2) (Figure 7a, 7b, 7c, 7d)							
For Positive dv/dt	50-60Hz	t_P	$C_{EXT} = 0$	70	100	140	μs
	400Hz		$C_{EXT} = 0, R_{EXT} = \infty$	-	12	-	μs
For Negative dv/dt	50-60Hz	t_N	$C_{EXT} = 0$	70	100	140	μs
	400Hz		$C_{EXT} = 0, R_{EXT} = \infty$	-	10	-	μs
PULSE DURATION AFTER ZERO CROSSING (50-60Hz) (Figure 7a)							
For Positive dv/dt		t_{P1}	$C_{EXT} = 0, R_{EXT} = \infty$	-	50	-	μs
For Negative dv/dt		t_{N1}		-	60	-	μs
OUTPUT LEAKAGE CURRENT (Figure 8)							
Inhibit Mode		I_4		-	0.001	10	μA
INPUT BIAS CURRENT (Figure 9)							
CA3059		I_I		-	220	1000	nA
CA3079				-	220	2000	nA
COMMON-MODE INPUT VOLTAGE RANGE		V_{CMR}	Terminals 9 and 13 connected	-	1.5 to 5	-	V

5
 AC TO DC
 CONVERTERS

Specifications CA3059, CA3079

Electrical Specifications $T_A = +25^\circ\text{C}$, For all Types, Unless Otherwise Specified. All voltages are measured with respect to Terminal 7. For Operating at 120V_{RMS}, 50-60Hz (AC Line Voltage) (Note 1) **(Continued)**

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS			UNITS
			MIN	TYP	MAX	
SENSITIVITY (Note 3) (Figures 4(a), 11)						
Pulse Mode	ΔV_{13}	Terminal 12 open	-	6	-	mV

NOTES:

1. The values given in the Electrical Characteristics Chart at 120V also apply for operation at input voltages of 208/230V, and 277V, except for Pulse Duration. However, the series resistor (R_S) must have the indicated value, shown in the chart in the Functional Block Diagram, for the specified input voltage.
2. Pulse Duration in 50Hz applications is approximately 15% longer than shown in Figure 7(b).
3. Required voltage change at Terminal 13 to either turn OFF the triac when ON or turn ON the triac when OFF.

Maximum Voltage Ratings $T_A = +25^\circ\text{C}$

MAXIMUM VOLTAGE RATINGS $T_A = +25^\circ\text{C}$															MAXIMUM CURRENT RATINGS	
TERM. NO.	NOTE 3 1	2	3	4	NOTE 1 5	NOTE 3 6	7	8	9	10	11	NOTE 3 12	13	NOTES 2,3 14	I_{IN} mA	I_{OUT} mA
1		*	*	*	*	15	10	*	*	*	*	*	*	*	10	0.1
Note 3						0	-2									
2			0	0	2	0	0**	0**	0	0	0	*	0	0	150	10
			-15	-15	-14	-14	-14	-14	-14	-14	-14	*	-14	-14		
3				0	*	*	*	*	*	*	*	*	*	*	*	*
				-15												
4					*	2	*	*	*	*	*	*	*	*	0.1	150
						-10										
5						*	7	*	*	*	*	*	*	*	50	10
Note 1							-7									
6							14	*	*	*	*	*	*	*	*	*
Note 3							0									
7								*	14	*	20	2.5	14	6	*	*
									0		0	-2.5	0	-6		
8									10	*	*	*	*	*	0.1	2
									0							
9										*	*	*	*	*	*	*
10										*	*	*	*	*	*	*
11										*	*	*	*	*	*	*
12												*	*	*	50	50
Note 3																
13													*	*	*	*
14															2	2
Note 3																

This chart gives the range of voltages which can be applied to the terminals listed horizontally with respect to the terminals listed vertically. For example, the voltage range of horizontal Terminal 6 to vertical Terminal 4 is 2 to -10 volts.

NOTES:

1. Resistance should be inserted between Terminal 5 and external supply or line voltage for limiting current into Terminal 5 to less than 50mA.
 2. Resistance should be inserted between Terminal 14 and external supply for limiting current into Terminal 14 to less than 2mA.
 3. For the CA3079 indicated terminal is internally connected and, therefore, should not be used.
- * Voltages are not normally applied between these terminals; however, voltages appearing between these terminals are safe, if the specified voltage limits between all other terminals are not exceeded.
- ** For CA3079 (0V to -10V).

CA3059, CA3079

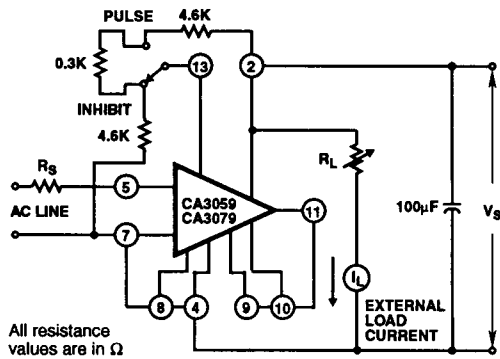


FIGURE 2(a). DC SUPPLY VOLTAGE TEST CIRCUIT FOR CA3059 AND CA3079

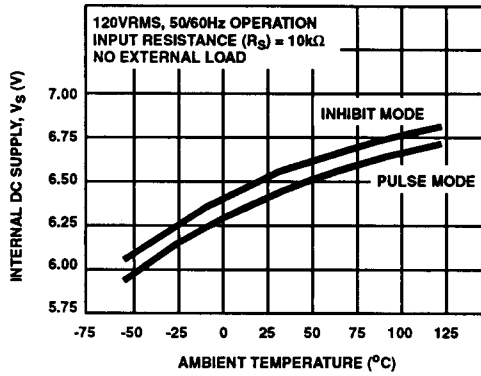


FIGURE 2(b). DC SUPPLY VOLTAGE vs. AMBIENT TEMPERATURE FOR CA3059 AND CA3079

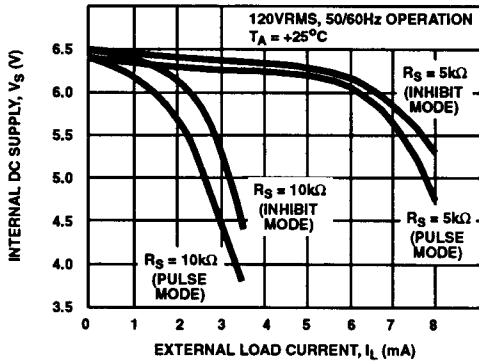


FIGURE 2(c). DC SUPPLY VOLTAGE vs. EXTERNAL LOAD CURRENT FOR CA3059 AND CA3079

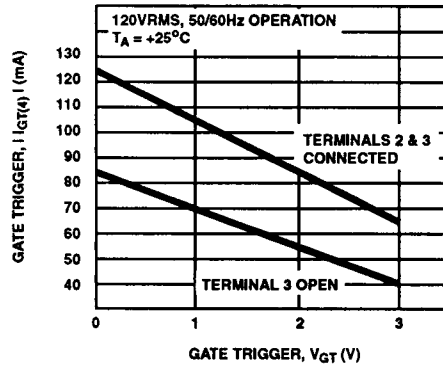


FIGURE 3. GATE TRIGGER CURRENT vs. GATE TRIGGER VOLTAGE FOR CA3059 AND CA3079

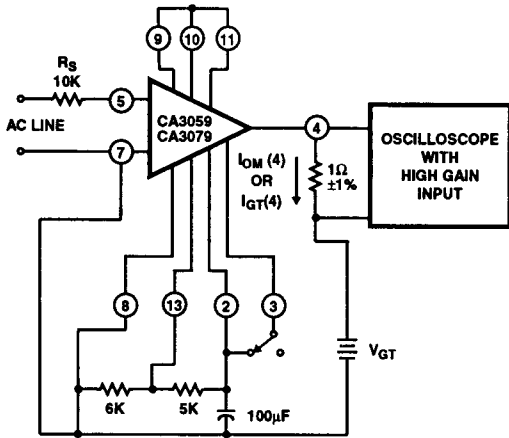


FIGURE 4(a). PEAK OUTPUT (PULSED) AND GATE TRIGGER CURRENT WITH INTERNAL POWER SUPPLY TEST CIRCUIT FOR CA3059 AND CA3079

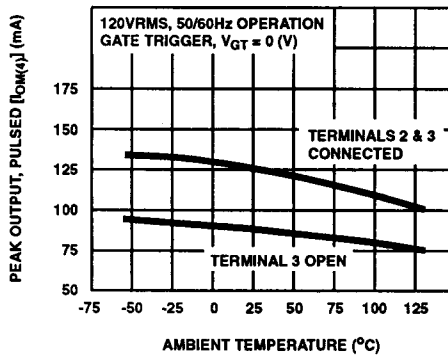


FIGURE 4(b). PEAK OUTPUT CURRENT (PULSED) vs. AMBIENT TEMPERATURE FOR CA3059 AND CA3079

CA3059, CA3079

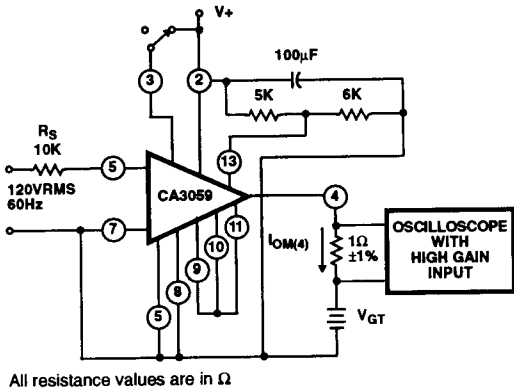


FIGURE 5(a). PEAK OUTPUT CURRENT (PULSED) WITH EXTERNAL POWER SUPPLY TEST CIRCUIT FOR CA3059

FIGURE

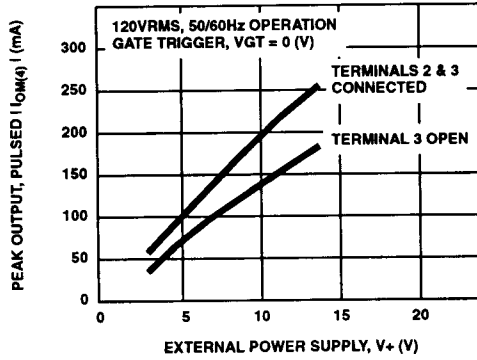


FIGURE 5(b). PEAK OUTPUT CURRENT (PULSED) vs. EXTERNAL POWER SUPPLY VOLTAGE FOR CA3059

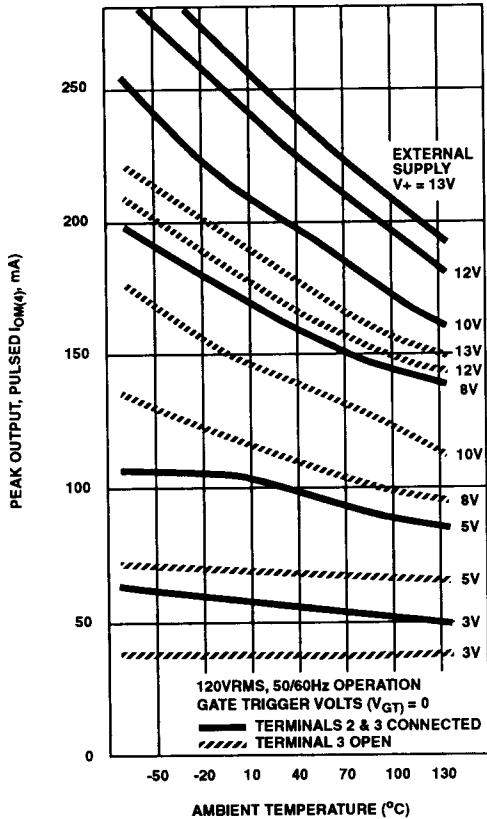


FIGURE 5(c). PEAK OUTPUT CURRENT (PULSED) vs. AMBIENT TEMPERATURE FOR CA3059

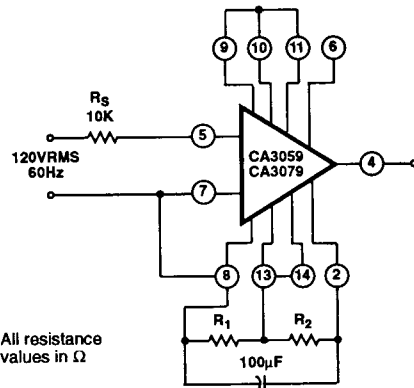


FIGURE 6(a). INPUT INHIBIT VOLTAGE RATIO TEST CIRCUIT FOR CA3059 AND CA3079

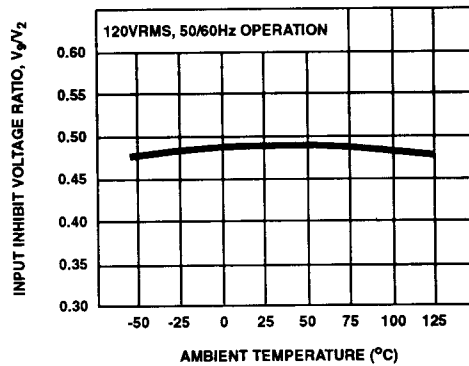
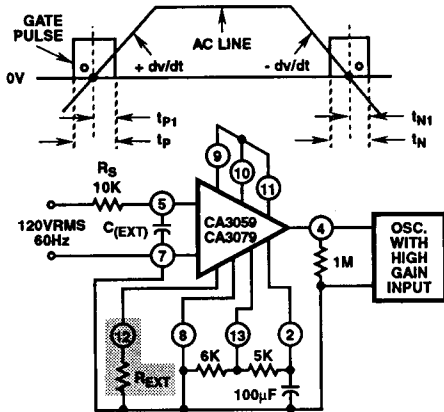


FIGURE 6(b). INPUT INHIBIT VOLTAGE RATIO vs. AMBIENT TEMPERATURE FOR CA3059 AND CA3079

CA3059, CA3079



NOTE: Circuitry within shaded area not included in CA3079. All resistance values are in Ω .

FIGURE 7(a). GATE PULSE DURATION TEST CIRCUIT WITH ASSOCIATED WAVEFORM FOR CA3059 AND CA3079

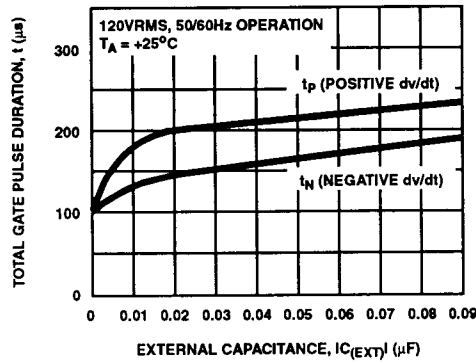


FIGURE 7(b). TOTAL GATE PULSE DURATION vs. EXTERNAL CAPACITANCE FOR CA3059 AND CA3079

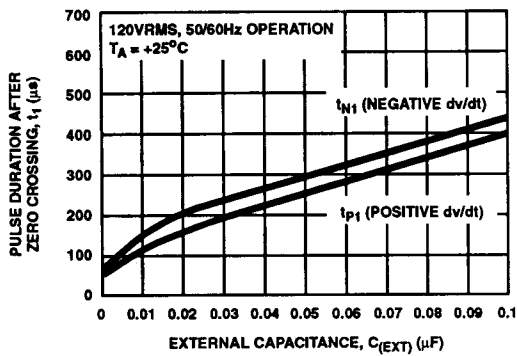


FIGURE 7(c). PULSE DURATION AFTER ZERO CROSSING vs. EXTERNAL CAPACITANCE FOR CA3059 AND CA3079

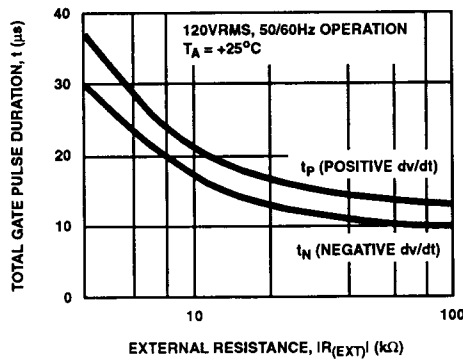


FIGURE 7(d). TOTAL GATE PULSE DURATION vs. EXTERNAL RESISTANCE FOR CA3059

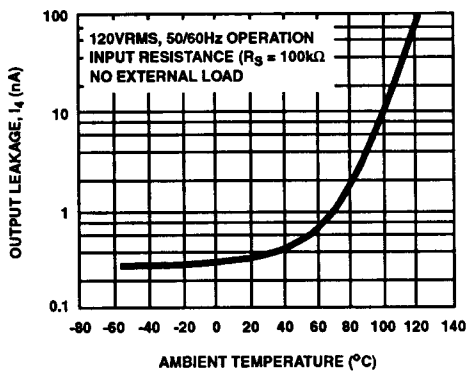


FIGURE 8. OUTPUT LEAKAGE CURRENT (INHIBIT MODE) vs. AMBIENT TEMPERATURE FOR CA3059 AND CA3079

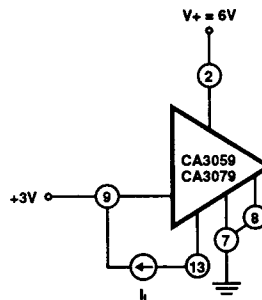


FIGURE 9. INPUT BIAS CURRENT TEST CIRCUIT FOR CA3059 AND CA3079

CA3059, CA3079

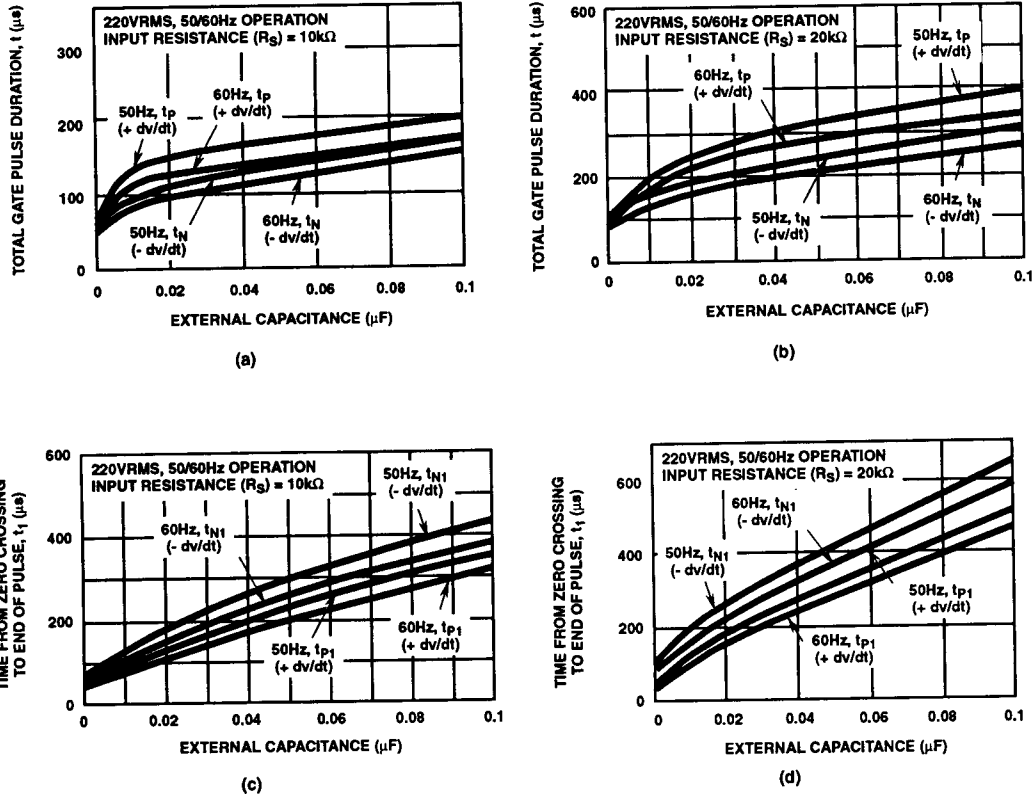


FIGURE 10. RELATIVE PULSE WIDTH AND LOCATION OF ZERO CROSSING FOR 220 VOLT OPERATION FOR CA3059 AND CA3079

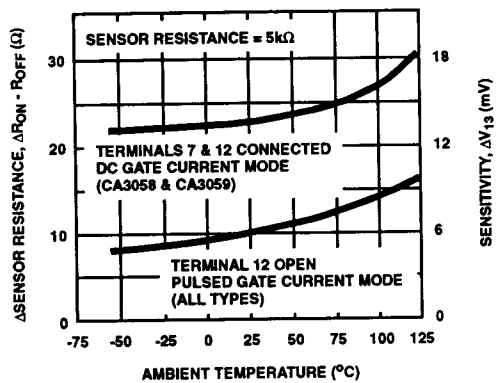


FIGURE 11. SENSITIVITY vs. AMBIENT TEMPERATURE FOR CA3059 AND CA3079

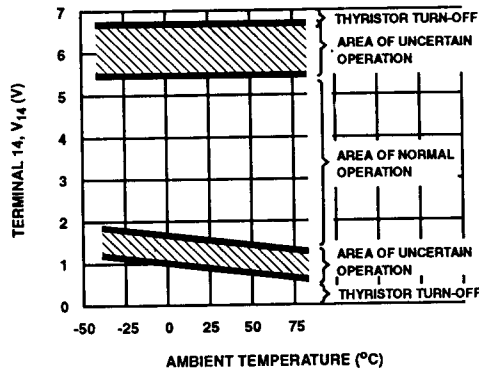
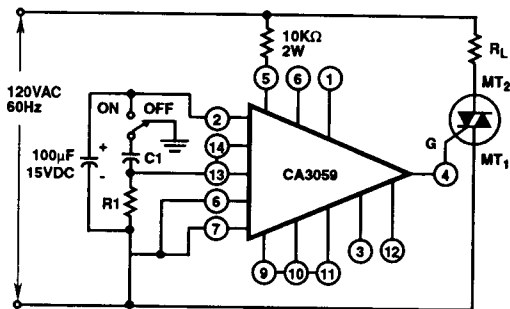


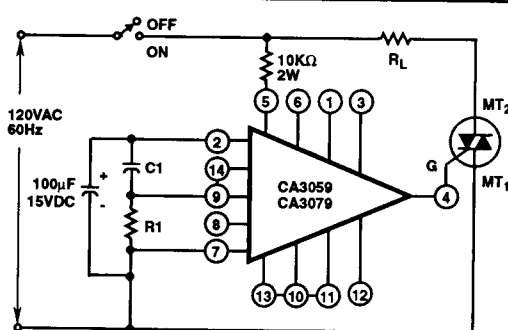
FIGURE 12. OPERATING REGIONS FOR BUILT-IN PROTECTION CIRCUIT FOR CA3059

CA3059, CA3079



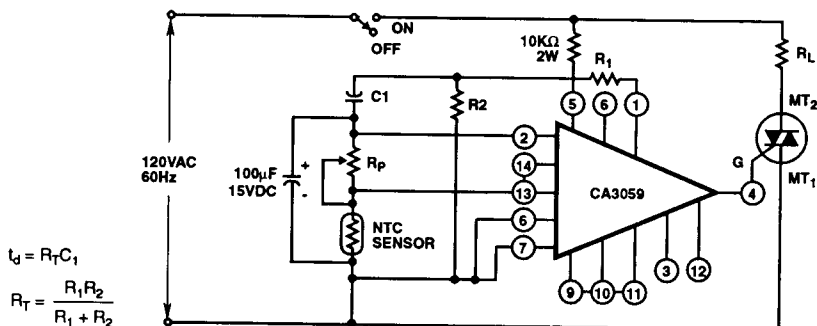
$t_{ON} = 0.67 R_1 C_1$
 R_1 (max. value allowable) = 1mΩ

FIGURE 13. LINE-OPERATED ONE-SHOT TIMER



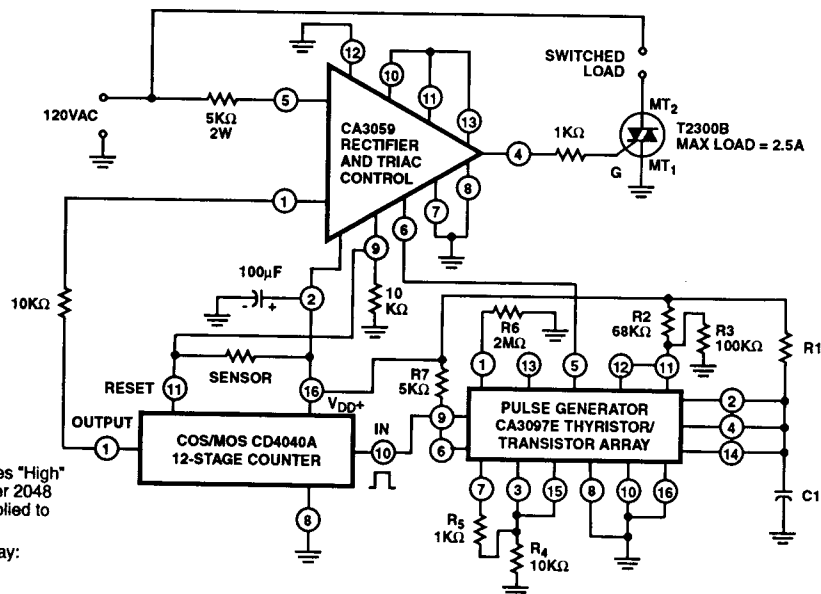
$t_d = 0.67 R_1 C_1$

FIGURE 14. LINE-OPERATED THYRISTOR CONTROL TIME DELAY TURN-ON CIRCUIT



$t_d = R_T C_1$
 $R_T = \frac{R_1 R_2}{R_1 + R_2}$

FIGURE 15. ON/OFF TEMPERATURE CONTROL CIRCUIT WITH DELAYED TURN-ON



NOTE:
 Terminal 1 goes "High" (Logic "1") after 2048 pulses are applied to Terminal 10.
 For 8 hour delay:
 $R_1 = 12M\Omega$
 $C_1 = 2\mu F$

FIGURE 16(a). LINE-OPERATED IC TIMER FOR LONG TIME PERIODS

CA3059, CA3079

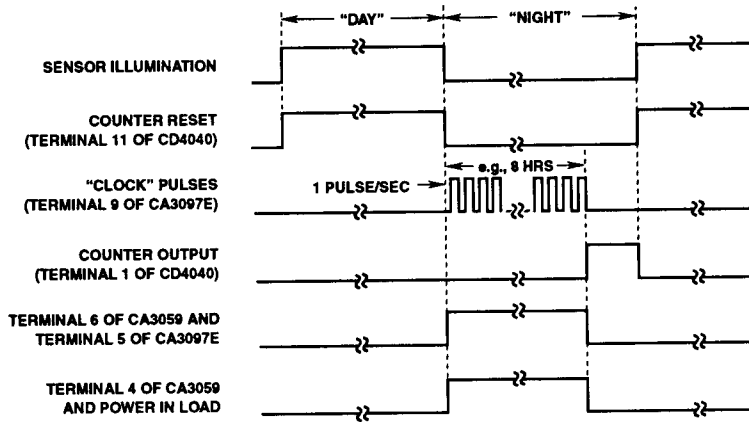


FIGURE 16(b). TIMING DIAGRAM FOR FIGURE 16(a)

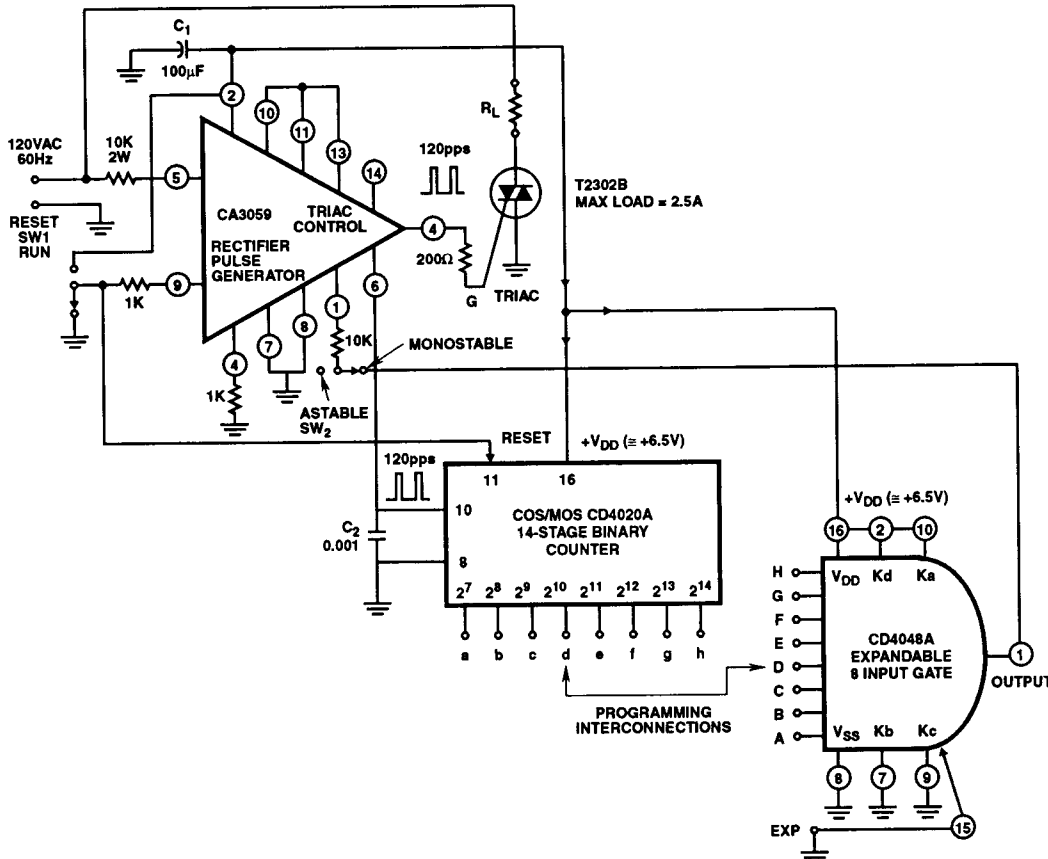


FIGURE 17(a). PROGRAMMABLE ULTRA-ACCURATE LINE-OPERATED TIMER.

CA3059, CA3079

TIME PERIODS (t = 0.5333 s)								
1t	2t	4t	8t	16t	32t	64t	128t	t ₀
CD4020A TERMINALS								
a	b	c	d	e	f	g	h	
CD4048A TERMINALS								
A	B	C	D	E	F	G	H	
C	NC	NC	NC	NC	NC	NC	NC	1t
NC	C	NC	NC	NC	NC	NC	NC	2t
C	C	NC	NC	NC	NC	NC	NC	3t
NC	NC	C	NC	NC	NC	NC	NC	4t
C	NC	C	NC	NC	NC	NC	NC	5t
NC	C	C	NC	NC	NC	NC	NC	6t
C	C	C	NC	NC	NC	NC	NC	7t
NC	NC	NC	C	NC	NC	NC	NC	8t
C	NC	NC	C	NC	NC	NC	NC	9t
NC	C	NC	C	NC	NC	NC	NC	10t
C	C	NC	C	NC	NC	NC	NC	11t
NC	NC	C	C	NC	NC	NC	NC	12t
C	NC	C	C	NC	NC	NC	NC	13t
NC	C	C	C	NC	NC	NC	NC	14t
C	C	C	C	NC	NC	NC	NC	15t
C	C	C	C	NC	C	C	NC	111t
NC	NC	NC	NC	C	C	C	NC	112t
C	NC	NC	NC	C	C	C	NC	113t
C	C	C	C	C	C	C	C	255t

NOTES:

1. t₀ = Total time delay = n₁ t + n₂ t + ... n_n t.
2. C = Connect. For example, interconnect terminal a of the CD4020A and terminal A of the CD4048A.
3. NC = No Connection. For example, terminal b of the CD4020A open and terminal B of the CD4048A connected to +V_{DD} bus.

5
AC TO DC
CONVERTERS

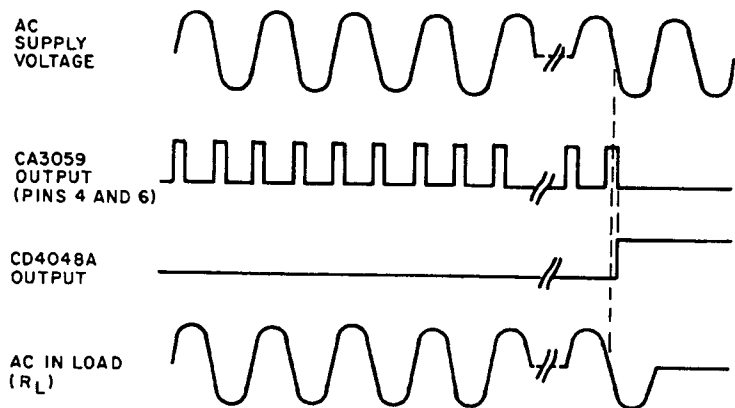


FIGURE 17(b). "PROGRAMMING" TABLE FOR FIGURE 17(a).

CA3059, CA3079

Operating Considerations

Power Supply Considerations for CA3059 and CA3079

The CA3059 and CA3079 are intended for operation as self-powered circuits with the power supplied from an AC line through a dropping resistor. The internal supply is designed to allow for some current to be drawn by the auxiliary power circuits. Typical power supply characteristics are given in Figures 2(b) and 2(c).

Power Supply Considerations for CA3059

The output current available from the internal supply may not be adequate for higher power applications. In such applications an external power supply with a higher voltage should be used with a resulting increase in the output level. (See Figure 4 for the peak output current characteristics.) When an external power supply is used, Terminal 5 should be connected to Terminal 7 and the synchronizing voltage applied to Terminal 12 as illustrated in Figure 5(a).

Operation of Built-In Protection for the CA3059

A special feature of the CA3059 is the inclusion of a protection circuit which, when connected, removes power from the load if the sensor either shorts or opens. The protection circuit is activated by connecting Terminal 14 to Terminal 13 as shown in the Functional Block Diagram. To assure proper operation of the protection circuit the following conditions should be observed:

1. Use the internal supply and limit the external load current to 2mA with a 5k Ω dropping resistor.

2. Set the value of R_p and sensor resistance (R_x) between 2k Ω and 100k Ω .
3. The ratio of R_x to R_p typically, should be greater than 0.33 and less than 3. If either of these ratios is not met with an unmodified sensor over the entire anticipated temperature range, then either a series or shunt resistor must be added to avoid undesired activation of the circuit.

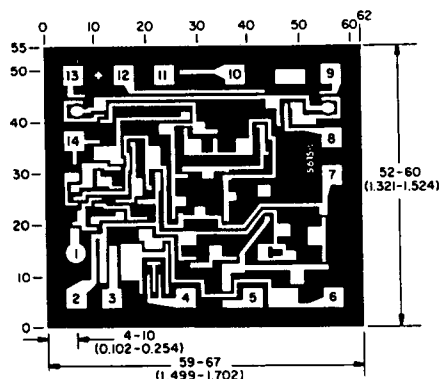
If operation of the protection circuit is desired under conditions other than those specified above, then apply the data given in Figure 12.

External Inhibit Function for the CA3059

A priority inhibit command may be applied to Terminal 1. The presence of at least +1.2V at 10 μ A will remove drive from the thyristor. This required level is compatible with DTL or T²L logic. A logical 1 activates the inhibit function.

DC Gate Current Mode for the CA3059

Connecting Terminals 7 and 12 disables the zero-crossing detector and permits the flow of gate current on demand from the differential sensing amplifier. This mode of operation is useful when comparator operation is desired or when inductive loads are switched. Care must be exercised to avoid overloading the internal power supply when operating in this mode. A sensitive gate thyristor should be used with a resistor placed between Terminal 4 and the gate in order to limit the gate current.



Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid gradations are in mils (10^{-3} inch).

The photographs and dimensions represent a chip when it is part of the wafer. When the wafer is cut into chips, the cleavage angles are 57° instead of 90° with respect to the face of the chip. Therefore, the isolated chip is actually 7 mils (0.17mm) larger in both dimensions.

DIMENSIONS AND PAD LAYOUT FOR CA3059H AND CA3079H

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