Rockchip RK3562 Datasheet

Revision History

Date	Revision	Description
2024-04-28	1.2	Update the electrical parameters
2023-03-23	1.1	Update the thermal parameter
2023-03-02	1.0	Initial release

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Warranty Disclaimer

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Chapter 1 Introduction

1.1 Overview

RK3562 is a high-performance and low-power quad-core application processor designed for consumer electronics equipments.

RK3562 features several embedded hardware engines to optimize performance for high-end applications. It supports almost full-format H.264 decoding at 1080p@60fps, H.265 decoding at 4K@30fps, and H.264 encoding at 1080p@60fps. Additionally, it includes a high-quality JPEG encoder and decoder.

RK3562 includes an embedded 3D GPU that ensures complete compatibility with OpenGL ES 1.1/2.0/3.2, OpenCL 2.0, and Vulkan 1.1. Additionally, a special 2D hardware engine is included to maximize display performance and ensure smooth operation.

The built-in NPU supports hybrid operations with INT4/INT8/INT16/FP16 data types. Additionally, it boasts strong compatibility with a series of frameworks, such as TensorFlow, MXNet, PyTorch, and Caffe, enabling easy conversion of network models."

RK3562 has a high-performance external memory interface(DDR3/DDR3L/DDR4 /LPDDR3/LPDDR4/LPDDR4X) capable of sustaining demanding memory bandwidths.

1.2 Features

1.2.1 Microprocessor
- Quad-core ARM Cortex-A53 MPCore processor, high-performance, low-power and cached application processor
- Full implementation of the ARM architecture v8-A instruction set, ARM Neon Advanced SIMD (single instruction, multiple data) support for accelerated media and signal processing computation
- ARMv8 Cryptography Extensions
- In-order pipeline with symmetric dual-issue of most instructions.
- Integrated 32KB L1 instruction cache, 32KB L1 data cache with 4-way set associative
- Level 2 (L2) memory system providing cluster memory coherency, including an L2 cache.
- Include VFP v3 hardware to support single and double-precision add, subtract, divide, multiply and accumulate, and square root operations
- TrustZone technology support
- Separate power domains for CPU core system to support internal power switch and externally turn on/off based on different application scenario
  - PD_A53_0: 1st Cortex-A53 + Neon + FPU + L1 I/D Cache
  - PD_A53_1: 2nd Cortex-A53 + Neon + FPU + L1 I/D Cache
  - PD_A53_2: 3rd Cortex-A53 + Neon + FPU + L1 I/D Cache
  - PD_A53_3: 4th Cortex-A53 + Neon + FPU + L1 I/D Cache
- One isolated voltage domain

1.2.2 Neural Process Unit
- Neural network acceleration engine with processing performance up to 1 TOPS
- Support integer 8, integer 16, float point 16, bfloat point 16 and tf32 neural network operation
- Support deep-learning frameworks: TensorFlow, TF-lite, Pytorch, Caffe, ONNX, MXNet, Keras, Darknet
- One isolated voltage domain

1.2.3 Memory Organization
- Internal on-chip memory
  - BootROM
    - Support system boot from the following device:

- ➢ SPI Flash interface
- ➢ eMMC interface
- ➢ SDMMC interface
- ◆ Support system code download by the following interface:
  - ➢ USB OTG interface (Device mode)
- ■ Internal SRAM
- ● External off-chip memory
  - ■ Dynamic Memory Interface
    - ◆ Compatible with JEDEC standards①DDR3-2133/DDR3L-2133/LPDDR3-2133/DDR4-2666/LPDDR4-2666/LPDDR4X-2666
    - ◆ Support 32bits data width, 2 ranks (chip selects), total addressing space is 8GB(max) for DDR3/DDR3L/DDR4
    - ◆ Support 32bits data width, 4 ranks (chip selects), total addressing space is 8GB(max) for LPDDR3/LPDDR4/LPDDR4X
    - ◆ Low power modes, such as power-down and self-refresh for SDRAM
    - ◆ Compensation for board delays and variable latencies through programmable pipelines
    - ◆ Programmable output and ODT impedance with dynamic PVT compensation
  - ■ eMMC Interface
    - ◆ Compatible with standard iNAND interface
    - ◆ Compatible with eMMC specification 4.41, 4.51, 5.0 and 5.1
    - ◆ Support three data bus width: 1bit, 4bits or 8bits
    - ◆ Support up to HS200 and HS400;
    - ◆ Support CMD Queue
  - ■ SD/MMC Interface
    - ◆ Compatible with SD3.0, MMC ver4.51
    - ◆ Data bus width is 4bits
  - ■ Flexible Serial Flash Interface(FSPI)
    - ◆ Support transfer data from/to serial flash device
    - ◆ Support 1bit/2bit/4bit data bus width
    - ◆ Support 2 chip select

1.2.4 System Component

- ● CRU (clock & reset unit)
  - ■ Support total 6 PLLs to generate all clocks
  - ■ One oscillator with 24MHz clock input
  - ■ Support clock gating control for individual components
  - ■ Support global soft-reset control for whole chip, also individual soft-reset for each component
- ● MCU
  - ■ Two MCUs inside RK3562
    - ◆ One in VD_LOGIC integrate 16KB Cache
    - ◆ One in VD_PMU
  - ■ Integrated Programmable Interrupt Controller (IPIC), all IRQ lines connected to GIC for CPU also connect to MCU in VD_LOGIC
  - ■ Integrated Debug Controller with JTAG interface
- ● PMU(power management unit)
  - ■ Multiple configurable work modes to save power by different frequency or automatic clock gating control or power domain on/off control
  - ■ Lots of wakeup sources in different modes
  - ■ Support 5 separate voltage domains
  - ■ Support 13 separate power domains, which can be power up/down by software based on different application scenes
- ● Timer
  - ■ Six 64bits timers with interrupt-based operation for non-secure application
  - ■ Two 64bits timers with interrupt-based operation for secure application
  - ■ Support two operation modes: free-running and user-defined count
  - ■ Support timer work state checkable

- Watchdog
    - 32bits watchdog counter
    - Counter counts down from a preset value to 0 to indicate the occurrence of a timeout
    - WDT can perform two types of operations when timeout occurs:
        - Generate a system reset
        - First generate an interrupt and if this is not cleared by the service routine by the time a second timeout occurs then generate a system reset
    - Totally 3 Watchdog for CPU and MCU
- Interrupt Controller
    - Support 3 PPI interrupt sources and 256 SPI interrupt sources input from different components
    - Support 16 software-triggered interrupts
    - Two interrupt outputs (nFIQ and nIRQ) separately for each Cortex-A53, both are low-level sensitive
    - Support different interrupt priority for each interrupt source, and they are always software-programmable
- Mailbox
    - Two Mailbox in SoC to service Cortex-A53 and MCU communication
    - Support four mailbox elements per mailbox, each element includes one data word, one command word register and one flag bit that can represent one interrupt
    - Provide 32 lock registers for software to use to indicate whether mailbox is occupied
- DMAC
    - Micro-code programming based DMA
    - Linked list DMA function is supported to complete scatter-gather transfer
    - Support data transfer types with memory-to-memory, memory-to-peripheral, peripheral-to-memory
    - One embedded DMA controller for system
    - DMAC features:
        - 8 channels totally
        - 32 hardware request from peripherals
        - 2 interrupt outputs
- Secure System
    - Embedded two Cipher engine
        - Support Link List Item (LLI) DMA transfer
        - Support SHA-1, SHA-256/224, MD5 with hardware padding
        - Support HMAC of SHA-1, SHA-256, MD5 with hardware padding
        - Support AES-128, AES-192, AES-256 cipher
        - Support DES & TDES cipher
        - Support AES ECB/CBC/OFB/CFB/CTR/CTS/XTS/CCM/GCM/CBC-MAC/CMAC mode
        - Support DES/TDES ECB/CBC/OFB/CFB mode
        - Support up to 4096 bits PKA mathematical operations for RSA
        - Support generating random numbers
    - Support keyladder to guarantee key secure
    - Support data scrambling for all DDR types
    - Support secure OTP
    - Support secure debug
    - Support secure OS
    - Except CPU, the other masters in the SoC can also support security and non-security mode by software-programmable
    - Some slave components in SoC can only be addressed by security master and the other slave components can be addressed by security master or non-security master by software-programmable
    - System SRAM, part of space is addressed only in security mode
    - External DDR space can be divided into 16 parts, each part can be software-

programmable to be enabled by each master

1.2.5 Video CODEC

- Video Decoder
  - H.265 HEVC/MVC Main Profile yuv420@L5.0 up to 4096x2304@30fps
  - H.264 AVC/MVC Main Profile yuv400/yuv420/yuv422/@L5.0 up to 1920x1080@60fps
  - VP9 Profile0 yuv420@L5.0 up to 4096x2304@30fps
- Video Encoder
  - H.264 High Profile level4.2, up to 1920x1080@60fps
  - Support YUV/RGB video source with rotation and mirror

1.2.6 JPEG CODEC

- JPEG decoder
  - 48x48 to 65536x65536(4295Mpixels), Step size 8 pixels
  - Baseline interleaved, and support DRI decode
- JPEG encoder
  - Baseline Non-progressive
  - up to 8192x8192
  - up to 90 million pixels per second

1.2.7 Graphics Engine

- 3D Graphics Engine:
  - Mali-G52 1-Core-2EE
  - Support OpenGL ES 1.1, 2.0, and 3.2
  - Support Vulkan 1.0 and 1.1
  - Support OpenCL 2.0 Full Profile
  - Support 1600Mpix/s fill rate when 800MHz clock frequency
  - Support 38.4 FP32 GFLOPs when 800MHz clock frequency
- 2D Graphics Engine:
  - Data format
    - Support input of ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422/YUYV；
    - Support input of YUV422SP10bit/YUV420SP10bit(YUV-8bits out)
    - Support output of ARGB/RGB888/RGB565/RGB4444/RGB5551/YUV420/YUV422/YUYV；
    - Pixel Format conversion, BT.601/BT.709
    - Dither operation, Y dither update;
    - Max resolution: 8192x8192 source, 4096x4096 destination
  - Scaling
    - Down-scaling: Average filter
    - Up-scaling: Bi-cubic filter(source>2048 would use Bi-linear)
    - Arbitrary non-integer scaling ratio，from 1/16 to 16
  - Rotation
    - 0, 90, 180, 270 degree rotation
    - x-mirror, y-mirror& rotation operation
  - BitBLT
    - Block transfer
    - Color palette/Color fill, support with alpha
    - Transparency mode (color keying/stencil test, specified value/value range)
    - Two source BitBLT:
    - A+B=B only BitBLT, A support rotate&scale when B fixed
    - A+B=C second source (B) has same attribute with (C) plus rotation function
  - Alpha Blending
    - New comprehensive per-pixel alpha(color/alpha channel separately)
    - Fading
    - SRC1(R2Y)&&SRC0(YUV)─alpha->DST(YUV)
  - OSD Automatic Inversion
    - Supports OSD sources in ARGB8888/ARGB1555/ARGB444/ARGB2BPP format
    - Support SRC0 and OSD overlay

1.2.8 Video input interface

- Interface and video input processor
  - Support MIPI CSI RX interface
  - Support VICAP block(Video Input Processor)
    - ◆ Support video data from MIPI CSI
  - Support ISP block(Image Signal Processor)
- MIPI CSI RX Interface
  - Compatible with the MIPI Alliance Interface specification v1.2
  - Support 2 MIPI CSI RX interfaces, with each up to 4 data lanes, 2.5Gbps maximum data rate per lane
  - Support MIPI-HS, MIPI-LP mode
  - Support two mode
    - ◆ One interface with 1 clock lane and 4 data lanes
    - ◆ Two interface, each with 1 clock lane and 2 data lanes
- VICAP
  - Support receiving four interfaces of MIPI CSI/DSI, up to four IDs for each interface
  - Support VC/DT configurable for each ID
  - Support five CSI data formats: RAW8/10/12/14, YUV422
  - Support YUYV input sequence configurable and YUYV sequence reorder
  - Support three modes of MIPI CSI HDR: virtual channel mode, identification code mode, line counter mode
  - Support one DSI data formats: RGB888, support video mode/command mode
  - Support reducing frame rate
  - Support window cropping
  - Support sending RAW data directly to ISP
  - Support 8/16/32 times down-sampling for RAW data
  - Support virtual stride when write to DDR
  - Support NV16/NV12/YUV400/YUYV output format for YUV data
  - Support compact/non-compact output format for RAW data
- ISP
  - VICAP input: RX raw8/raw10/raw12
  - 3A: Include Auto Enhance (AE)/Histogram, Auto Focus (AF), and Auto White Balance (AWB) statistics output
  - BLC: Black Level Correction
  - DPCC: Static/Dynamic Defect Pixel Cluster Correction
  - PDAF: Phase Detection Auto Focus
  - LSC: Lens Shading Correction
  - Bayer-3DNR: Temporal Bayer-raw Noise Reduction
  - HDR-MGE: 2-Frame Merge into High-Dynamic Range
  - HDR-DRC: HDR Dynamic Range Compression, Tone mapping
  - DeBayer: Advanced Adaptive Demosaic
  - CCM/CSM: Color Correction Matrix, RGB2YUV, etc.
  - Gamma: Gamma out correction
  - Dehaze/Enhance: Automatic Dehaze and effect enhancement
  - 3DLUT: 3D-LUT Color Palette for Customer
  - LDCH: Lens Distortion Correction only in the Horizontal direction
  - YUV-2DNR: Spatial YUV Noise Reduction
  - Sharp: Image sharpening and boundary filtering
  - Gain: Image local gain
  - Multi-sensor reuse ISP, 4 sensors for maximum
  - Maximum resolution is 4224x3136, throughput 13M @30fps

1.2.9 Display interface

- Display interface
  - Support RGB Parallel Display interface
  - Support BT656/BT1120 interface
  - Support MIPI_DSI interface
  - Support LVDS interface

- RGB video output interface
  - Support up to 2048x1080@60Hz
  - Support RGB(up to 8bit) format
  - Up to 150MHz data rate
- BT.656/BT.1120 video output interface
  - BT1120 up to 1080 P/I output
  - BT656 up to 576 P/I output
- MIPI DSI TX interface
  - Compatible with MIPI Alliance Interface specification v1.2
  - Support 1 channel DSI
  - Support 4 data lanes per channel
  - Support 1.2Gbps maximum data rate per lane
  - Up to 2048x1080@60Hz display output
  - Support RGB(up to 8bit) format
- LVDS interface
  - Compliant with the TIA/EIA-644-A LVDS specification
  - Support RGB888 and RGB666 input for LVDS interface
  - Support VESA/JEIDA LVDS data format transfer
  - Up to 800x1280@60Hz display output

1.2.10 Video Output Processor

- Video input
  - Support 4 Esmart layer
    - Support up to 3840x2160 input resolution
    - Support RGB/YUV/YUYV format
    - Support scale up/down ratio 8~1/8
    - Support 4 regions
- Overlay
  - Support MAX 4 layers overlay
  - Support RGB/YUV domain overlay
- Post process
  - 3D-LUT/P2I/CSC/BCSH/DITHER/GAMMA/COLORBAR
- Write back
  - Format: XRGB8888/RGB888/RGB565/YUV420
  - Max resolution: 1920x1080
- Video output
  - Video output, up to 2048x1080@60Hz resolution

1.2.11 Audio Interface

- SAI(Serial Audio Interface)
  - Support audio protocol: I2S, PCM, TDM
  - Support 3 SAI controllers
    - Up to 4 lanes TX and 4 lanes RX path for SAI0/SAI1
    - Up to 1 lanes TX and 1 lanes RX path for SAI2
  - Audio resolution from 8bits to 32bits
  - Sample rate up to 192KHz
  - Provides master and slave work mode, software configurable
  - Support 3 I2S formats (normal, left-justified, right-justified)
  - Support 4 PCM formats (early, late1, late2, late3)
  - Support TDM normal, 1/2 cycle left shift, 1 cycle left shift, 2 cycle left shift, right shift mode serial audio data transfer
  - I2S, PCM and TDM mode cannot be used at the same time
- SPDIF
  - Support two 16-bit audio data store together in one 32-bit wide location
  - Support biphase format stereo audio data output
  - Support 16 to 31 bit audio data left or right justified in 32-bit wide sample data buffer
  - Support 16, 20, 24 bits audio data transfer in linear PCM mode
  - Support non-linear PCM transfer

- PDM
    - Up to 8 channels
    - Audio resolution from 16bits to 24bits
    - Sample rate up to 192KHz
    - Support PDM master receive mode
- Digital Audio Codec
    - Support 2-channel digital DAC
    - Support I2S/PCM interface
    - Support I2S/PCM master and slave mode
    - Support 2-channel audio receiving in I2S mode
    - Support 2-channel audio receiving in PCM mode
    - Support I2S normal, left and right justified mode serial audio data transfer
    - Support PCM early, late1, late2, late3 mode serial audio data transfer
    - Support MSB or LSB first serial audio data transfer
    - Support configurable SCLK and LRCK polarity
    - Support 16 bit sample resolution
    - Support programmable left and right channel exchangeable in I2S mode and PCM mode
    - Support three modes of mixing for every digital DAC channel
    - Support volume control
    - Support programmable negative and positive volume gain

1.2.12 Connectivity

- SDIO interface
    - Compatible with SDIO3.0 protocol
    - 4bits data bus widths
- MAC 10/100 Ethernet Controller
    - Support 10/100 Mbps data transfer rates with the RMII interfaces
    - Support both full-duplex and half-duplex operation
- GMAC 10/100/1000 Ethernet Controller
    - Support 10/100/1000 Mbps data transfer rates with the RGMII interfaces
    - Support 10/100 Mbps data transfer rates with the RMII interfaces
    - Support both full-duplex and half-duplex operation
- USB 2.0 Host
    - Support one USB2.0 Host
    - Compatible with USB 2.0 specification
    - Supports high-speed(480Mbps), full-speed(12Mbps) and low-speed(1.5Mbps) mode
    - Support Enhanced Host Controller Interface Specification (EHCI), Revision 1.0
    - Support Open Host Controller Interface Specification (OHCI), Revision 1.0a
- Multi-PHY Interface
    - Support multi-PHY with one PCIe2.1 and one USB3.0 controller
    - support one of the following interfaces
        - USB3.0 Host
        - PCIe2.1
    - USB 3.0 Dual-Role Device (DRD) Controller
        - Static USB3.0 Device
        - Static USB3.0 xHCI host
        - USB3.0/USB2.0 OTG A device and B device basing on ID
    - PCIe2.1 interface
        - Compatible with PCI Express Base Specification Revision 2.1
        - Support one lane
        - Support Root Complex(RC) mode only
        - Support 2.5Gbps and 5.0Gbps serial data transmission rate per lane per direction
- SPI interface
    - Support 3 SPI Controller
    - Support two chip-select output
    - Support serial-master and serial-slave mode, software-configurable

- I2C interface
    - Support 6 I2C Master
    - Support 7bits and 10bits address mode
    - Software programmable clock frequency
    - Data on the I2C-bus can be transferred at rates of up to 100Kbit/s in the Standard-mode, up to 400Kbit/s in the Fast-mode.
- UART Controller
    - Support 10 UART interfaces
    - Embedded two 64-byte FIFO for TX and RX operation respectively
    - Support 5bits,6bits,7bits,8bits serial data transmit or receive
    - Standard asynchronous communication bits such as start, stop and parity
    - Support different input clock for UART operation to get up to 4Mbps baud rate
    - Support auto flow control mode except for UART0
- PWM
    - Support 16 on-chip PWMs(PWM0~PWM15) with interrupt-based operation
    - Programmable pre-scaled operation to bus clock and then further scaled
    - Embedded 32bits timer/counter facility
    - Support capture mode
    - Support continuous mode or one-shot mode
    - Provides reference mode and output various duty-cycle waveform
    - Optimized for IR application for PWM3,PWM7,PWM11 and PWM15

1.2.13 Others

- Multiple group of GPIO
    - All of GPIOs can be used to generate interrupt to CPU
    - Support level trigger and edge trigger interrupt
    - Support configurable polarity of level trigger interrupt
    - Support configurable rising edge, falling edge and both edge trigger interrupt
    - Support configurable pull direction(a weak pull-up and a weak pull-down)
    - Support configurable drive strength
- Temperature Sensor(TSADC)
    - Up to 50KS/s sampling rate
    - Support two temperature sensor
    - -20~120°C temperature range and 5°C temperature resolution
- Successive Approximation ADC (SARADC)
    - 10bits resolution
    - Up to 1MS/s sampling rate
    - 16 single-ended input channels
- OTP
    - Support 8K bits Size, 7K bits for secure application
    - Support Program/Read/Idle mode
- Package Type
    - FCCSP478L (body: 13.9mm x 13.9mm; ball size: 0.3mm; ball pitch: 0.5mm&0.65mm)

Notes: *① DDR3/DDR3L/DDR4/LPDDR3/LPDDR4/LPDDR4X are not used simultaneously*

1.3 Block Diagram

The following diagram shows the basic block diagram.

RK3562

System
Clock & Reset
WDT
PLL x6
Timer x6
Secure Timer x2
PMU
Crypto
Interrupt Controller
DMAC
SARADC(8ch) x2
TSADC
MCU
Mailbox

Cortex-A53 Quad-Core

Core0	Core1
32KB L1 I-Cache	32KB L1 I-Cache
32KB L1 D-Cache	32KB L1 D-Cache
NOEN/FPU/Crypto	NOEN/FPU/Crypto

Core2	Core3
32KB L1 I-Cache	32KB L1 I-Cache
32KB L1 D-Cache	32KB L1 D-Cache
NOEN/FPU/Crypto	NOEN/FPU/Crypto

512KB L2-Cache

NPU

Multi-Media Processor

4K@30fps Video Decoder	GPU Mali-G52-2EE
H.264 1080p@60fps Video Encoder	2D Graphics Engine
13M ISP	JPEG Codec

Connectivity
PCIe2.1/USB3.0 OTG
USB2.0 HOST
SAI x3
PDM(8ch)
SPDIF(8ch)
UART x10
SPI x3
SDIO 3.0
Ethernet MAC (10/100M)
Ethernet GMAC (10/100/1000M)
I2C x6
PWM x16
GPIO x108

Multi-Media Interface
VOP
LVDS/MIPI-DSI_TX
Parallel RGB Interface
MIPI-CSI_RX 4 Lanex2

External Memory Interface

eMMC 5.1	Nor Flash /Async SRAM
SD3.0/MMC4.51	
32Bit DDR Controller (DDR3/DDR3L/DDR4/LPDDR4/LPDDR4X)	

Embedded Memory
SRAM (64KB)
ROM (32KB)
OTP(8K bit)

Fig.1-1 Block Diagram

Chapter 2 Package Information

2.1 Order Information

Orderable Device	RoHS status	Package	Package Q'ty	Device Feature
RK3562	RoHS	FCCSP478L	1190pcs	Quad-core application processor

2.2 Top Marking
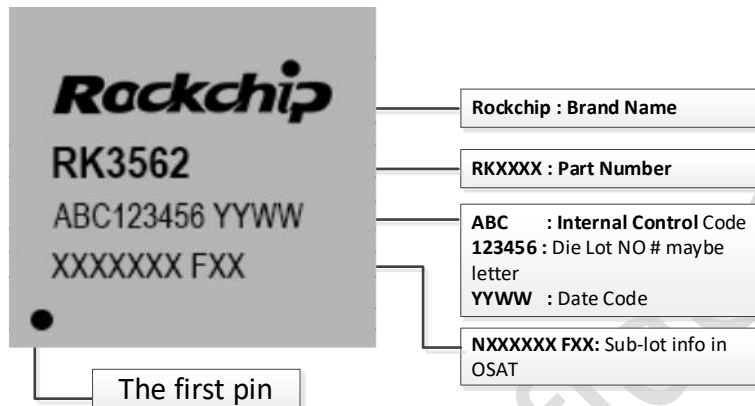
Fig.2-1 Package definition

2.3 Package Dimension
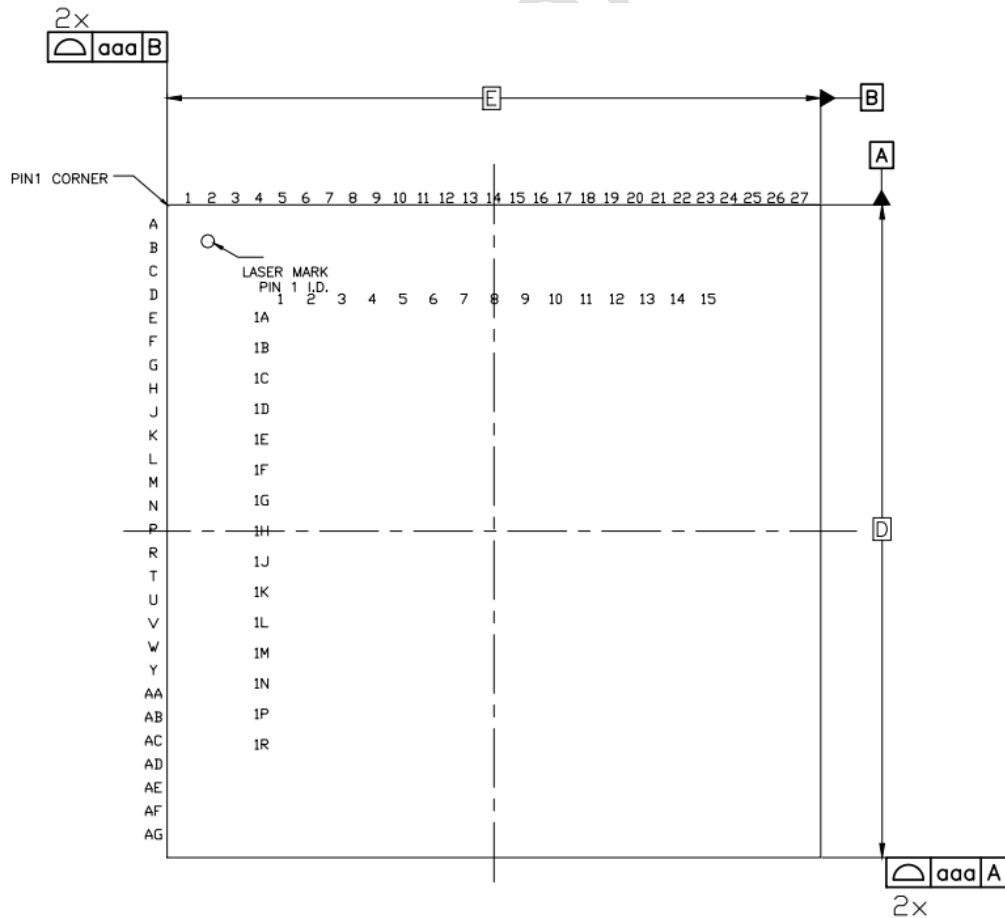
Fig.2-2 Package Top View
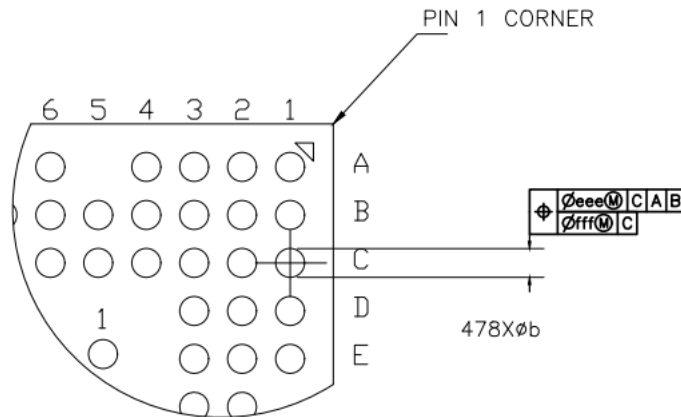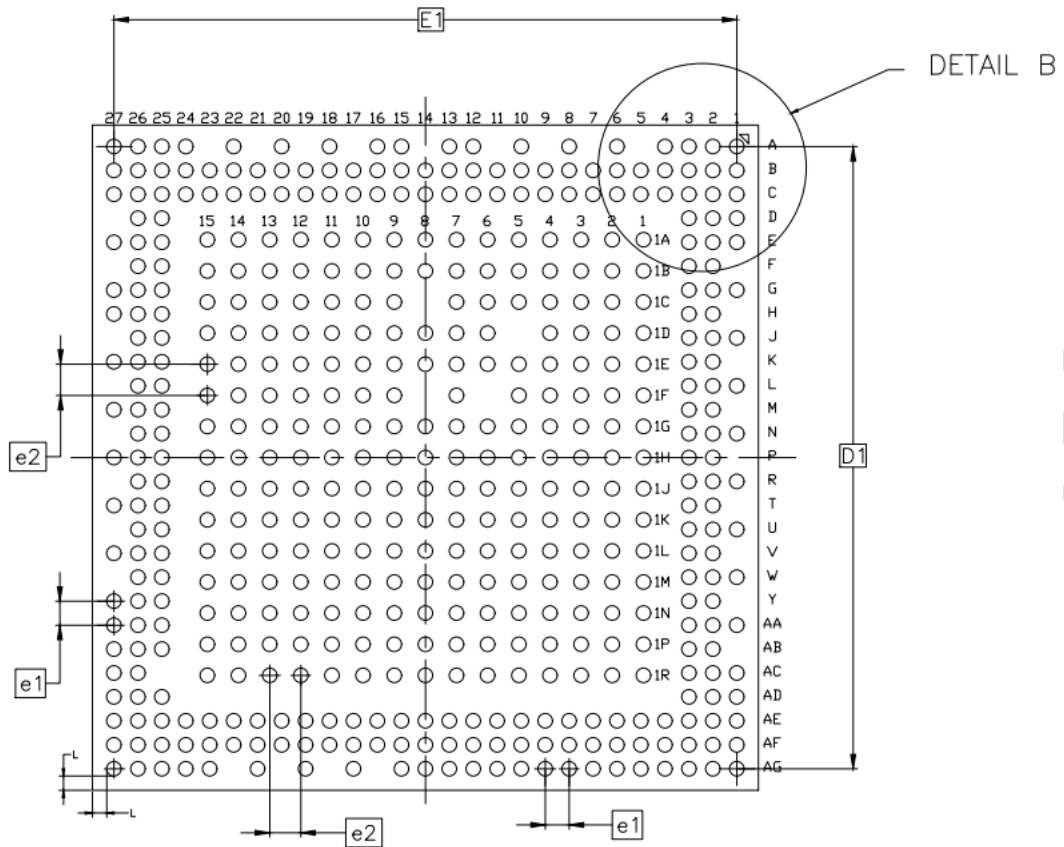
DETAIL B(2:1)
Fig.2-3 Package bottom view

DETAIL A(2:1)
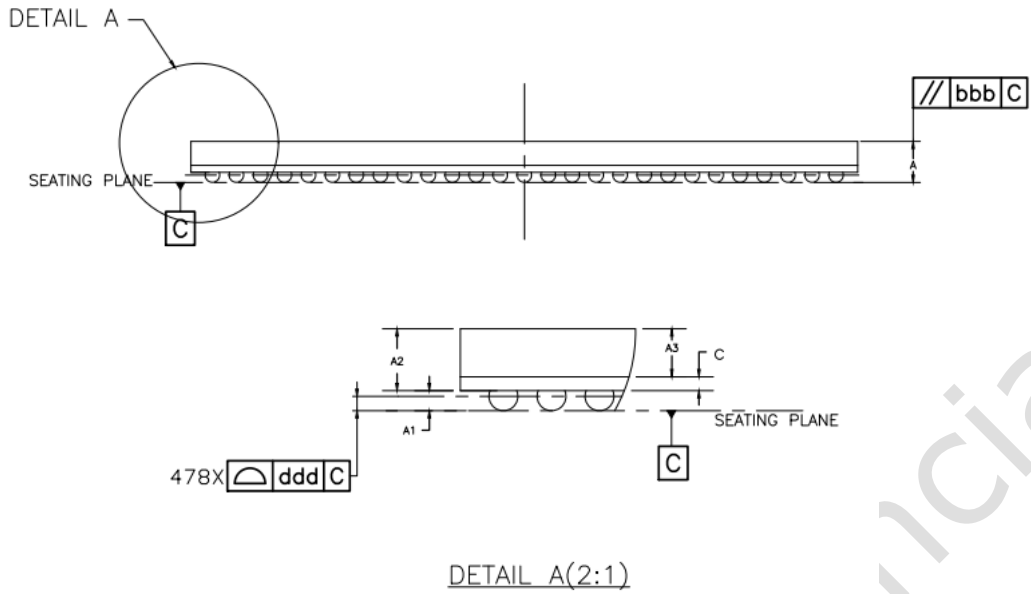
Fig.2-4 Package side view

SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.795	0.87	0.947
A1	0.16	0.21	0.26
A2	0.605	0.66	0.7
A3	0.50 BASIC		
c	0.125	0.145	0.165
D	13.80	13.90	14.00
D1	13.00 BASIC		
E	13.80	13.90	14.00
E1	13.00 BASIC		
e1	0.50 BASIC		
e2	0.65 BASIC		
b	0.25	0.30	0.35
L	0.300 REF		
aaa	0.15		
bbb	0.10		
ddd	0.08		
eee	0.15		
fff	0.05		

Fig.2-5 Package dimension

2.4 MSL Information

Moisture sensitivity Level ：MSL3

2.5 Lead Finish/Ball material Information

Lead Finish/Ball material ：SnAgCu

2.6 Pin Number List

Table 2-1 Pin Number List Information

Pin Name	No.	Pin Name	No.
DDR_DQS1P_A/DDR4_DQSU_P_A/LPDDR4_DQS1P_A/DDR3_DQS1P/LPDDR3_DQS1P	1A1	VO_LCDC_D22/RGMII_TXD0_M0/UART6_CTSN_M1/SPI1_MOSI_M0/GPIO4_A2_d	AA1
AC4/DDR4_A4/LPDDR4_A3_B/DDR3_BA1	1A10	VO_LCDC_D23/RGMII_TXD1_M0/UART6_RTSN_M1/SPI1_MISO_M0/GPIO4_A3_d	AA2
VSS_1A11	1A11	UART1_RTSN_M0/RGMII_TXEN_M1/I2S0_SDI2_M1/PWM6_M1/RMII_TXEN/GPIO1_D3_d	AA25
VSS_1A12	1A12	AVSS2_AA26	AA26
DDR_DQS0P_B/DDR4_DQSU_P_B/LPDDR4_DQS0P_B/DDR3_DQS2P/LPDDR3_DQS2P	1A13	VSS_AA27	AA27
VSS_1A14	1A14	VO_LCDC_D0/RGMII_TXEN_M0/PWM13_M0/GPIO4_A4_d	AA3
DDR_DQS1P_B/DDR4_DQSL_P_B/LPDDR4_DQS1P_B/DDR3_DQS3P/LPDDR3_DQS0P	1A15	VO_LCDC_D14/RGMII_TXD3_M0/UART8_RX_M1/I2S2_SDO_M1/GPIO3_D5_d	AB2
VSS_1A2	1A2	AVSS2_AB25	AB25
DDR_DQS0P_A/DDR4_DQSL_P_A/LPDDR4_DQS0P_A/DDR3_DQS0P/LPDDR3_DQS3P	1A3	USB30_OTG0_SSRXP/PCIE20_RXDP	AB26
VSS_1A4	1A4	USB30_OTG0_SSRXN/PCIE20_RXDN	AB27
VSS_1A5	1A5	VO_LCDC_D13/RGMII_TXD2_M0/UART8_TX_M1/I2S2_SDI_M1/GPIO3_D4_d	AB3
AC12/DDR4_A12/LPDDR4_A3_A/DDR3_BA0	1A6	VO_LCDC_D2/RGMII_MDC_M0/UART9_TX_M0/GPIO4_B2_d	AC1
AC16/DDR4_A16_RASN/LPDDR4_A5_A/DDR3_RASN	1A7	VO_LCDC_D18/RGMII_MDIO_M0/UART9_RX_M0/GPIO4_B3_d	AC2
AC5/DDR4_A5/LPDDR4_A5_B/DDR3_A11	1A8	PCIE20_REFCLKP	AC26
AC19/DDR4_BA1/LPDDR4_A4_B/DDR3_A12	1A9	PCIE20_REFCLKN	AC27
DDR_DQS1N_A/DDR4_DQSU_N_A/LPDDR4_DQS1N_A/DDR3_DQS1N/LPDDR3_DQS1N	1B1	AVSS1_AC3	AC3
AC20/DDR4_BG0/LPDDR4_ODT1_CA_B/DDR3_WEN	1B10	MIPI_CSI_RX1_D3P	AD1
AC29/DDR4_RESETN/LPDDR4_RESETN/DDR3_RESETN	1B11	MIPI_CSI_RX1_D3N	AD2
VSS_1B12	1B12	AVSS2_AD25	AD25
DDR_DQS0N_B/DDR4_DQSU_N_B/LPDDR4_DQS0N_B/DDR3_DQS2N/LPDDR3_DQS2N	1B13	USB30_OTG0_SSTXP/PCIE20_TXDP	AD26
VSS_1B14	1B14	USB30_OTG0_SSTXN/PCIE20_TXDN	AD27
DDR_DQS1N_B/DDR4_DQSL_N_B/LPDDR4_DQS1N_B/DDR3_DQS3N/LPDDR3_DQS0N	1B15	AVSS1_AD3	AD3
VSS_1B2	1B2	MIPI_CSI_RX1_D2P	AE1
DDR_DQS0N_A/DDR4_DQSL_N_A/LPDDR4_DQS0N_A/DDR3_DQS0N/LPDDR3_DQS3N	1B3	AVSS1_AE10	AE10
VSS_1B4	1B4	AVSS1_AE11	AE11
VSS_1B5	1B5	AVSS1_AE12	AE12
AC1/DDR4_A1/DDR3_A2	1B6	AVSS1_AE13	AE13
AC21/DDR4_BG1/LPDDR4_ODT1_CA_A/DDR3_BA2	1B7	AVSS1_AE14	AE14
AC14/DDR4_A14_WEN/LPDDR4_A4_A/DDR3_A15	1B8	I2C2_SDA_M0/PCIE20_WAKEN_M0/GPIO0_B6_d	AE15
VSS_1B9	1B9	UART2_RTSN_M0/PWM0_M0/SPI0_CLK_M0/GPIO0_C3_d	AE16
VSS_1C1	1C1	I2C1_SCL_M0/GPIO0_B3_d	AE17
VSS_1C10	1C10	UART6_RTSN_M0/PWM2_M0/SPI0_MISO_M0/GPIO0_C5_d	AE18
VSS_1C11	1C11	UART6_RX_M0/GPIO0_C7_d	AE19
VSS_1C12	1C12	AVSS1_AE2	AE2
VSS_1C13	1C13	UART0_TX_M0/JTAG_CPU_MCU_TCK_M0/GPIO0_D1_u	AE20
VSS_1C14	1C14	VSS_AE21	AE21
VSS_1C15	1C15	SDMMC0_PWREN/I2C4_SCL_M1/PMU_DEBUG/GPIO0_A5_d	AE22
VSS_1C2	1C2	I2C0_SDA/GPIO0_B2_d	AE23
VSS_1C3	1C3	REF_CLK_OUT/GPIO0_A0_d	AE24
VSS_1C4	1C4	VSS_AE25	AE25
VSS_1C5	1C5	USB20_HOST1_DM	AE26
VSS_1C6	1C6	USB20_HOST1_DP	AE27
VSS_1C7	1C7	AVSS1_AE3	AE3
DDR_VREFOUT	1C9	AVSS1_AE4	AE4
VSS_1D1	1D1	AVSS1_AE5	AE5
VSS_1D10	1D10	AVSS1_AE6	AE6
DDRPHY_VDDQ_6	1D11	AVSS1_AE7	AE7
VSS_1D12	1D12	AVSS1_AE8	AE8
VSS_1D13	1D13	AVSS1_AE9	AE9
VSS_1D14	1D14	MIPI_CSI_RX1_D2N	AF1
VSS_1D15	1D15	MIPI_DSI_TX_D3N/LVDS_TX_D3N	AF10
VSS_1D2	1D2	MIPI_DSI_TX_D2P/LVDS_TX_D2P	AF11
VSS_1D3	1D3	MIPI_DSI_TX_CLKN/LVDS_TX_CLKN	AF12

Pin Name	No.	Pin Name	No.
DDR_RZQ	1D4	MIPI_DSI_TX_D1P/LVDS_TX_D1P	AF13
DDRPHY_VDDQ_3	1D6	MIPI_DSI_TX_D0N/LVDS_TX_D0N	AF14
VSS_1D7	1D7	SPI0_CSN1_M0/PWM4_M0/CPU_AVS/SPDIF_TX_M1/GPIO0_B7_d	AF15
VSS_1D8	1D8	I2C2_SCL_M0/PCIE20_PERSTN_M0/GPIO0_B5_d	AF16
VSS_1D9	1D9	UART2_TX_M0/PWM7_M0/GPU_AVS/GPIO0_C0_d	AF17
SARADC1_IN7	1E1	I2C1_SDA_M0/GPIO0_B4_d	AF18
DDRPHY_VDDQL_4	1E10	UART6_TX_M0/GPIO0_C6_d	AF19
VSS_1E11	1E11	MIPI_CSI_RX1_CLK0P	AF2
VDD_GPU_1	1E12	UART0_RX_M0/JTAG_CPU_MCU_TMS_M0/GPIO0_D0_u	AF20
VSS_1E13	1E13	CLK_32K_IN/CLK0_32K_OUT/PCIE20_BUTTONRSTN/GPIO0_B0_d	AF21
SARADC0_AVDD_1V8	1E14	PWR_CTRL1/GPIO0_A3_u	AF22
OTP_VCC_1V8	1E15	PWR_CTRL0/TSADC_SHUT_M1/GPIO0_A2_d	AF23
VSS_1E2	1E2	VSS_AF24	AF24
DDRPHY_VDDQ_1	1E3	OSC_SOC_XOUT	AF25
DDRPHY_VDDQL_1	1E4	USB30_OTG0_DM	AF26
DDRPHY_VDDQ_2	1E5	USB30_OTG0_DP	AF27
DDRPHY_VDDQL_2	1E6	MIPI_CSI_RX1_D1P	AF3
DDRPHY_VDDQ_4	1E7	MIPI_CSI_RX1_D0P	AF4
DDRPHY_VDDQL_3	1E8	MIPI_CSI_RX0_D3P	AF5
DDRPHY_VDDQ_5	1E9	MIPI_CSI_RX0_D2P	AF6
SARADC1_IN0	1F1	MIPI_CSI_RX0_CLK0P	AF7
VSS_1F10	1F10	MIPI_CSI_RX0_D1P	AF8
VDD_GPU_2	1F11	MIPI_CSI_RX0_D0P	AF9
VDD_GPU_3	1F12	AVSS1_AG1	AG1
VDD_GPU_4	1F13	MIPI_DSI_TX_D3P/LVDS_TX_D3P	AG10
VCCIO2	1F14	MIPI_DSI_TX_D2N/LVDS_TX_D2N	AG11
VSS_1F15	1F15	MIPI_DSI_TX_CLKP/LVDS_TX_CLKP	AG12
SARADC1_IN2	1F2	MIPI_DSI_TX_D1N/LVDS_TX_D1N	AG13
VSS_1F3	1F3	MIPI_DSI_TX_D0P/LVDS_TX_D0P	AG14
VSS_1F4	1F4	VSS_AG15	AG15
VSS_1F5	1F5	UART2_CTSN_M0/PWM5_M0/SPI0_CSN0_M0/GPIO0_C2_d	AG17
VSS_1F7	1F7	UART6_CTSN_M0/PWM1_M0/SPI0_MOSI_M0/GPIO0_C4_d	AG19
VSS_1F9	1F9	MIPI_CSI_RX1_CLK0N	AG2
SYSPLL_AVDD_1V8	1G1	PWM3_M0/GPIO0_A7_d	AG21
VDD_LOGIC_1	1G10	I2C0_SCL/GPIO0_B1_d	AG23
VDD_GPU_5	1G11	PCIE20_CLKREQN_M0/GPIO0_A6_d	AG24
VDD_GPU_6	1G12	OSC_SOC_XIN	AG25
VSS_1G13	1G13	VSS_AG26	AG26
VSS_1G14	1G14	AVSS2_AG27	AG27
VCCIO3	1G15	MIPI_CSI_RX1_D1N	AG3
VSS_1G2	1G2	MIPI_CSI_RX1_D0N	AG4
VDD_NPU_1	1G3	MIPI_CSI_RX0_D3N	AG5
VDD_NPU_2	1G4	MIPI_CSI_RX0_D2N	AG6
VDD_NPU_3	1G5	MIPI_CSI_RX0_CLK0N	AG7
VSS_1G6	1G6	MIPI_CSI_RX0_D1N	AG8
VSS_1G7	1G7	MIPI_CSI_RX0_D0N	AG9
VDD_CPU_1	1G8	DDR_DQ10_A/DDR4_DQU3_A/LPDDR4_DQ10_A/DDR3_DQ12/LPDDR3_DQ15	B1
VSS_1G9	1G9	AC11/DDR4_A11/LPDDR4_A0_A/DDR3_A6/LPDDR3_A8	B10
SARADC1_IN4	1H1	AC3/DDR4_A3/LPDDR4_CS0N_A/DDR3_ODT1/LPDDR3_ODT0	B11
VDD_LOGIC_2	1H10	AC25/DDR4_CS0N/LPDDR4_CKE1_A/DDR3_A3	B12
VDD_LOGIC_MEM	1H11	AC24/DDR4_CLK0N/LPDDR4_CLKP_A/DDR3_CLKN/LPDDR3_CLKN	B13
VSS_1H12	1H12	VSS_B14	B14
VSS_1H13	1H13	AC9/DDR4_A9/LPDDR4_CLKP_B/DDR3_A13	B15
VCCIO4	1H14	AC17/DDR4_ACTN/LPDDR4_CKE1_B/DDR3_CASN/LPDDR3_CS1N	B16
I2S2_SDO_M0/RGMII_RXD1_M1/UART4_RTSN_M1/SPI2_MOSI_M1/PWM14_M1/RMII_RXD1/GPIO1_D7_d	1H15	AC28/DDR4_ODT1/LPDDR4_CS0N_B/DDR3_CS0N/LPDDR3_A2	B17
VSS_1H2	1H2	AC7/DDR4_A7/LPDDR4_A0_B/DDR3_A5/LPDDR3_A0	B18
VDD_NPU_4	1H3	AC13/DDR4_A13/LPDDR4_ODT0_CA_B/DDR3_A8/LPDDR3_ODT1	B19
VDD_NPU_5	1H4	DDR_DQ11_A/DDR4_DQU7_A/LPDDR4_DQ11_A/DDR3_DQ8/LPDDR3_DQ14	B2

Pin Name	No.	Pin Name	No.
VSS_1H5	1H5	DDR_DQ1_B/DDR4_DQU3_B/LPDDR4_DQ1_B/DDR3_DQ20/LPDDR3_DQ21	B20
VDD_CPU_2	1H6	DDR_DM0_B/DDR4_DMU_B/LPDDR4_DM0_B/DDR3_DM2/LPDDR3_DM2	B21
VDD_CPU_3	1H7	DDR_DQ0_B/DDR4_DQU7_B/LPDDR4_DQ0_B/DDR3_DQ16/LPDDR3_DQ17	B22
VDD_CPU_4	1H8	DDR_DQ5_B/DDR4_DQU4_B/LPDDR4_DQ5_B/DDR3_DQ23/LPDDR3_DQ19	B23
VSS_1H9	1H9	DDR_DQ13_B/DDR4_DQL7_B/LPDDR4_DQ13_B/DDR3_DQ31/LPDDR3_DQ5	B24
SARADC1_IN1	1J1	DDR_DQ15_B/DDR4_DQL3_B/LPDDR4_DQ15_B/DDR3_DQ29/LPDDR3_DQ7	B25
VDD_LOGIC_3	1J10	DDR_DQ11_B/DDR4_DQL6_B/LPDDR4_DQ11_B/DDR3_DQ24/LPDDR3_DQ6	B26
VDD_LOGIC_4	1J11	DDR_DQ10_B/DDR4_DQL2_B/LPDDR4_DQ10_B/DDR3_DQ28/LPDDR3_DQ2	B27
VDD_LOGIC_5	1J12	DDR_DQ15_A/DDR4_DQU6_A/LPDDR4_DQ15_A/DDR3_DQ9/LPDDR3_DQ10	B3
VSS_1J13	1J13	DDR_DQ13_A/DDR4_DQU4_A/LPDDR4_DQ13_A/DDR3_DQ15/LPDDR3_DQ8	B4
SDMMC1_PWREN/RGMII_MDC_M1/PWM2_M1/I2C5_SCL_M1/RMII_MDC/GPIO1_C7_d	1J14	DDR_DQ5_A/DDR4_DQL1_A/LPDDR4_DQ5_A/DDR3_DQ3/LPDDR3_DQ28	B5
I2S2_SDI_M0/RGMII_RXER_M1/UART4_CTSN_M1/SPI2_MISO_M1/PWM15_M1/RMII_RXER/GPIO2_A0_d	1J15	DDR_DQ0_A/DDR4_DQL6_A/LPDDR4_DQ0_A/DDR3_DQ0/LPDDR3_DQ30	B6
SARADC1_IN3	1J2	DDR_DM0_A/DDR4_DML_A/LPDDR4_DM0_A/DDR3_DM0/LPDDR3_DM3	B7
VSS_1J3	1J3	DDR_DQ1_A/DDR4_DQL2_A/LPDDR4_DQ1_A/DDR3_DQ4/LPDDR3_DQ26	B8
VSS_1J4	1J4	AC8/DDR4_A8/LPDDR4_ODT0_CA_A/DDR3_A7/LPDDR3_A9	B9
VSS_1J5	1J5	DDR_DQ9_A/DDR4_DQU5_A/LPDDR4_DQ9_A/DDR3_DQ10/LPDDR3_DQ13	C1
VDD_CPU_5	1J6	AC15/DDR4_A15_CASN/LPDDR4_A2_A/DDR3_A0/LPDDR3_A7	C10
VDD_CPU_6	1J7	AC26/DDR4_CS1N/LPDDR4_CS1N_A/DDR3_CS1N/LPDDR3_A5	C11
VSS_1J8	1J8	AC22/DDR4_CKE0/LPDDR4_CKE0_A/DDR3_CKE/LPDDR3_CKE	C12
VSS_1J9	1J9	VSS_C13	C13
SARADC1_IN6	1K1	VSS_C14	C14
VDD_LOGIC_6	1K10	VSS_C15	C15
VSS_1K11	1K11	AC10/DDR4_A10/LPDDR4_CKE0_B/DDR3_A10/LPDDR3_CS0N	C16
VSS_1K12	1K12	AC27/DDR4_ODT0/LPDDR4_CS1N_B/DDR3_ODT0/LPDDR3_A4	C17
VSS_1K13	1K13	AC18/DDR4_BA0/LPDDR4_A2_B/DDR3_A1/LPDDR3_A3	C18
MULTI_PHY_AVDD_0V9	1K14	VSS_C19	C19
MULTI_PHY_AVDD_1V8	1K15	DDR_DQ8_A/DDR4_DQU1_A/LPDDR4_DQ8_A/DDR3_DQ14/LPDDR3_DQ9	C2
SARADC1_AVDD_1V8	1K2	DDR_DQ3_B/DDR4_DQU5_B/LPDDR4_DQ3_B/DDR3_DQ18/LPDDR3_DQ20	C20
VCCIO5	1K3	VSS_C21	C21
VSS_1K4	1K4	DDR_DQ6_B/DDR4_DQU2_B/LPDDR4_DQ6_B/DDR3_DQ19/LPDDR3_DQ18	C22
VSS_1K5	1K5	DDR_DQ4_B/DDR4_DQU0_B/LPDDR4_DQ4_B/DDR3_DQ21/LPDDR3_DQ23	C23
VSS_1K6	1K6	VSS_C24	C24
VSS_1K7	1K7	VSS_C25	C25
VSS_1K8	1K8	DDR_DQ8_B/DDR4_DQL0_B/LPDDR4_DQ8_B/DDR3_DQ26/LPDDR3_DQ0	C26
VSS_1K9	1K9	DDR_DQ9_B/DDR4_DQL4_B/LPDDR4_DQ9_B/DDR3_DQ30/LPDDR3_DQ1	C27
I2C3_SDA_M0/UART2_RX_M1/SPDIF_TX_M0/UART5_RTSN_M1/GPIO3_A1_d	1L1	VSS_C3	C3
VSS_1L10	1L10	VSS_C4	C4
PMUIO1	1L11	DDR_DQ4_A/DDR4_DQL5_A/LPDDR4_DQ4_A/DDR3_DQ1/LPDDR3_DQ24	C5
PMUIO0	1L12	DDR_DQ7_A/DDR4_DQL3_A/LPDDR4_DQ7_A/DDR3_DQ5/LPDDR3_DQ29	C6
PMUPLL_AVDD_1V8	1L13	VSS_C7	C7
USB_AVDD_0V9	1L14	DDR_DQ3_A/DDR4_DQL4_A/LPDDR4_DQ3_A/DDR3_DQ6/LPDDR3_DQ27	C8
AVSS2_1L15	1L15	VSS_C9	C9
SARADC1_IN5	1L2	I2S1_SDO0_M1/CAM_CLK3_OUT/UART8_RTSN_M0/SPI0_CLK_M1/PWM13_M1/GPIO3_B5_d	D1
VCCIO1	1L3	VSS_D2	D2
VSS_1L4	1L4	SARADC0_IN4	D25
VCCIO6_2	1L5	SARADC0_BOOT	D26
MIPI_CSI_RX1_AVDD_0V9	1L6	I2C5_SDA_M0/ISP_FLASH_TRIGOUT/UART9_RX_M1/GPIO3_C3_d	D3
AVSS1_1L7	1L7	I2C5_SCL_M0/ISP_PRELIGHT_TRIGOUT/UART9_TX_M1/GPIO3_C2_d	E1

Pin Name	No.	Pin Name	No.
MIPI_CSI_RX0_AVDD_0V9	1L8	I2S1_SDI0_M1/ISP_FLASH_TRIGIN/UART3_RTSN_M1/GPIO3_C1_d	E2
AVSS1_1L9	1L9	SARADC0_IN2	E25
I2C3_SCL_M0/UART2_TX_M1/PDM_SDI3_M0/UART5_CTSN_M1/GPIO3_A0_d	1M1	SARADC0_IN5	E26
SYSPLL_AVDD_0V9	1M10	SARADC0_IN6	E27
PMU_VDD_LOGIC_0V9	1M11	VSS_E3	E3
PMUPLL_AVSS	1M12	I2S1_LRCK_M1/CAM_CLK2_OUT/UART8_CTSN_M0/SPI0_MOSI_M1/PWM12_M1/GPIO3_B4_d	F2
PMUPLL_AVDD_0V9	1M13	SARADC0_IN7	F25
USB_AVDD_3V3	1M14	SARADC0_IN1	F26
USB_AVDD_1V8	1M15	VSS_F3	F3
I2S0_SDO3_M0/I2S0_SDI1_M0/PDM_SDI1_M0/PCIE20_PERSTN_M1/GPIO3_B0_d	1M2	I2S1_SCLK_M1/CAM_CLK1_OUT_M0/UART8_RX_M0/GPIO3_B3_d	G1
VSS_1M3	1M3	I2S1_SDO2_M1/I2S1_SDI2_M1/UART3_TX_M1/SPI0_CSN0_M1/I2C4_SDA_M0/GPIO3_B7_d	G2
VCCIO6_1	1M4	VSS_G25	G25
VSS_1M5	1M5	SARADC0_IN3	G26
AVSS1_1M6	1M6	VSS_G27	G27
MIPI_CSI_RX1_AVDD_1V8	1M7	I2S1_SDO1_M1/I2S1_SDI3_M1/UART3_CTSN_M1/SPI0_CSN1_M1/I2C4_SCL_M0/GPIO3_B6_d	G3
MIPI_CSI_RX0_AVDD_1V8	1M8	I2S1_SDO3_M1/I2S1_SDI1_M1/UART3_RX_M1/SPI0_MISO_M1/GPIO3_C0_d	H2
MIPI_DSI_TX/LVDS_TX_AVDD_0V9	1M9	EMMC_D2/FSPI_D2/GPIO1_A2_u	H25
VSS_1N1	1N1	EMMC_D6/GPIO1_A6_u	H26
AVSS1_1N10	1N10	EMMC_D7/GPIO1_A7_u	H27
VSS_1N11	1N11	I2S1_MCLK_M1/CAM_CLK0_OUT_M0/UART8_TX_M0/GPIO3_B2_d	H3
VSS_1N12	1N12	I2S0_SDO1_M0/I2S0_SDI3_M0/PDM_CLK0_M0/PCIE20_CLKREQN_M1/UART5_TX_M1/GPIO3_A6_d	J1
TVSS	1N13	I2S0_SDI0_M0/PDM_SDI0_M0/GPIO3_B1_d	J2
AVSS2_1N14	1N14	EMMC_D0/FSPI_D0/GPIO1_A0_u	J25
AVSS2_1N15	1N15	EMMC_D1/FSPI_D1/GPIO1_A1_u	J26
VSS_1N2	1N2	VSS_J3	J3
VSS_1N3	1N3	I2S0_MCLK_M0/UART2_CTSN_M1/PDM_CLK1_M0/GPIO3_A2_d	K2
VSS_1N4	1N4	EMMC_D5/GPIO1_A5_u	K25
AVSS1_1N5	1N5	EMMC_D4/GPIO1_A4_u	K26
AVSS1_1N6	1N6	EMMC_D3/FSPI_D3/GPIO1_A3_u	K27
AVSS1_1N7	1N7	I2S0_SDO0_M0/PWM9_M0/GPIO3_A5_d	K3
AVSS1_1N8	1N8	I2S0_LRCK_M0/PWM8_M0/GPIO3_A4_d	L1
MIPI_DSI_TX/LVDS_TX_AVDD_1V8	1N9	I2S0_SDO2_M0/I2S0_SDI2_M0/PDM_SDI2_M0/PCIE20_WAKEN_M1/UART5_RX_M1/GPIO3_A7_d	L2
AVSS1_1P1	1P1	VSS_L25	L25
AVSS1_1P10	1P10	EMMC_STRB/FSPI_CSN1/GPIO1_B2_d	L26
VSS_1P11	1P11	I2S0_SCLK_M0/UART2_RTSN_M1/GPIO3_A3_d	L3
nPOR	1P12	VO_LCDC_HSYNC/I2S1_SDO1_M0/UART9_CTSN_M0/SPI2_CSN1_M0/I2C1_SCL_M1/UART3_TX_M0/GPIO4_B4_d	M2
VSS_1P13	1P13	EMMC_CLK/FSPI_CLK/GPIO1_B1_d	M25
USB30_OTG0_VBUSDET	1P14	EMMC_CMD/FSPI_CSN0/GPIO1_B0_u	M26
USB30_OTG0_ID	1P15	VSS_M27	M27
AVSS1_1P2	1P2	VO_LCDC_VSYNC/I2S1_SDO2_M0/UART9_RTSN_M0/SPI2_CSN0_M0/I2C1_SDA_M1/UART3_RX_M0/GPIO4_B5_d	M3
MIPI_CSI_RX1_CLK1P	1P3	VO_LCDC_D3/I2S1_MCLK_M0/UART7_TX_M0/GPIO3_C4_d	N1
AVSS1_1P4	1P4	VO_LCDC_D4/I2S1_SCLK_M0/UART4_CTSN_M0/PWM14_M0/GPIO3_C5_d	N2
AVSS1_1P5	1P5	SDMMC0_D2/JTAG_CPU_MCU_TCK_M1/UART5_CTSN_M0/SPI1_CSN1_M1/PWM10_M0/DSM_AUD_RP/GPIO1_B5_u	N25
AVSS1_1P6	1P6	SDMMC0_D3/JTAG_CPU_MCU_TMS_M1/UART5_RTSN_M0/SPI1_CSN0_M1/PWM11_M0/DSM_AUD_RN/GPIO1_B6_u	N26
MIPI_CSI_RX0_CLK1P	1P7	VO_LCDC_DEN/I2S1_SDO3_M0/UART3_CTSN_M0/SPI2_CLK_M0/GPIO4_B6_d	N3
AVSS1_1P8	1P8	VO_LCDC_D6/I2S1_SDO0_M0/UART7_RX_M0/GPIO3_C7_d	P2
AVSS1_1P9	1P9	SDMMC0_CMD/SPDIF_TX_M2/UART5_RX_M0/GPIO1_B7_u	P25
AVSS1_1R1	1R1	VSS_P26	P26
AVSS1_1R10	1R10	SDMMC0_CLK/TEST_CLK_OUT/UART5_TX_M0/SPI1_CLK_M1/GPIO1_C0_d	P27
UART2_RX_M0/PWM6_M0/NPU_AVS/GPIO0_C1_d	1R11	VO_LCDC_D5/I2S1_LRCK_M0/UART4_RTSN_M0/PWM15_M0/GPIO3_C6_d	P3
VSS_1R12	1R12	VO_LCDC_D10/I2S1_SDI1_M0/UART4_RX_M0/UART3_RTSN_M0/GPIO3_D1_d	R1
TSADC_SHUT_M0/TSADC_SHUT_ORG/GPIO0_A1_z	1R13	VO_LCDC_D11/I2S1_SDI2_M0/UART7_CTSN_M0/SPI2_MISO_M0/I2C2_SCL_M1/GPIO3_D2_d	R2
VSS_1R14	1R14	SDMMC0_D0/UART0_RX_M1/UART7_RX_M1/SPI1_MOSI_M1/DSM_AUD_LP/GPIO1_B3_u	R25

Pin Name	No.	Pin Name	No.
SDMMC0_DETN/I2C4_SDA_M1/GPIO0_A4_u	1R15	SDMMC0_D1/UART0_TX_M1/UART7_TX_M1/SPI1_MISO_M1/DSM_AUD_LN/GPIO1_B4_u	R26
AVSS1_1R2	1R2	VO_LCDC_D7/I2S1_SDI0_M0/UART4_TX_M0/GPIO3_D0_d	R3
MIPI_CSI_RX1_CLK1N	1R3	VO_LCDC_D17/ETH_CLK_25M_OUT_M0/CAM_CLK0_OUT_M1/I2S2_SCLK_M1/PDM_CLK1_M1/GPIO4_B1_d	T2
AVSS1_1R4	1R4	SDMMC1_D2/RGMII_TXCLK_M1/I2S0_SDO0_M1/PWM10_M1/GPIO1_C3_d	T25
AVSS1_1R5	1R5	SDMMC1_D3/RGMII_RXD2_M1/I2S0_LRCK_M1/PWM11_M1/GPIO1_C4_d	T26
AVSS1_1R6	1R6	SDMMC1_CMD/RGMII_RXD3_M1/I2S0_SCLK_M1/PWM0_M1/GPIO1_C5_d	T27
MIPI_CSI_RX0_CLK1N	1R7	VO_LCDC_D12/I2S1_SDI3_M0/UART7_RTSN_M0/SPI2_MOSI_M0/I2C2_SDA_M1/GPIO3_D3_d	T3
AVSS1_1R8	1R8	VO_LCDC_CLK/RGMII_CLK_M0/CAM_CLK1_OUT_M1/PDM_CLK0_M1/GPIO4_B7_d	U1
AVSS1_1R9	1R9	VO_LCDC_D21/RGMII_RXCLK_M0/I2S2_LRCK_M1/PWM12_M0/GPIO4_A1_d	U2
VSS_A1	A1	SDMMC1_CLK/RGMII_RXCLK_M1/I2S0_MCLK_M1/PWM1_M1/GPIO1_C6_d	U25
AC2/DDR4_A2/LPDDR4_A1_A/DDR3_A4/LPDDR3_A6	A10	SDMMC1_D0/RGMII_TXD2_M1/I2S0_SDI0_M1/PWM8_M1/GPIO1_C1_d	U26
VSS_A12	A12	VSS_U3	U3
AC23/DDR4_CLK0P/LPDDR4_CLKN_A/DDR3_CLKP/LPDDR3_CLKP	A13	VO_LCDC_D9/RGMII_RXDV_M0/UART1_RTSN_M1/PDM_SDI0_M1/UART6_TX_M1/GPIO4_A7_d	V2
AC0/DDR4_A0/LPDDR4_CLKN_B/DDR3_A9	A15	SDMMC1_D1/RGMII_TXD3_M1/I2S0_SDI1_M1/PWM9_M1/GPIO1_C2_d	V25
VSS_A16	A16	SDMMC1_DETN/RGMII_MDIO_M1/PWM3_M1/I2C5_SDA_M1/RMII_MDIO/GPIO1_D0_d	V26
AC6/DDR4_A6/LPDDR4_A1_B/DDR3_A14/LPDDR3_A1	A18	I2S2_LRCK_M0/RGMII_RXDV_M1/UART4_TX_M1/SPI2_CSN0_M1/RMII_RXDV_CRS/GPIO1_D6_d	V27
DDR_DM1_A/DDR4_DMU_A/LPDDR4_DM1_A/DDR3_DM1/LPDDR3_DM1	A2	VO_LCDC_D16/RGMII_RXER_M0/UART1_CTSN_M1/PDM_SDI1_M1/UART6_RX_M1/GPIO4_B0_d	V3
DDR_DQ2_B/DDR4_DQU1_B/LPDDR4_DQ2_B/DDR3_DQ22/LPDDR3_DQ16	A20	VO_LCDC_D8/RGMII_RXD1_M0/UART1_RX_M1/PDM_SDI3_M1/I2C3_SDA_M1/GPIO4_A6_d	W1
DDR_DQ7_B/DDR4_DQU6_B/LPDDR4_DQ7_B/DDR3_DQ17/LPDDR3_DQ22	A22	VO_LCDC_D19/RGMII_RXD2_M0/UART8_CTSN_M1/SPI1_CSN0_M0/GPIO3_D7_d	W2
DDR_DQ12_B/DDR4_DQL5_B/LPDDR4_DQ12_B/DDR3_DQ25/LPDDR3_DQ3	A24	I2S2_MCLK_M0/ETH_CLK_25M_OUT_M1/CLK1_32K_OUT/SPI2_CLK_M1/I2S0_SDO3_M1/GPIO2_A1_d	W25
DDR_DQ14_B/DDR4_DQL1_B/LPDDR4_DQ14_B/DDR3_DQ27/LPDDR3_DQ4	A25	I2S2_SCLK_M0/RGMII_CLK_M1/UART4_RX_M1/SPI2_CSN1_M1/RMII_CLK/GPIO1_D5_d	W26
DDR_DM1_B/DDR4_DML_B/LPDDR4_DM1_B/DDR3_DM3/LPDDR3_DM0	A26	VO_LCDC_D1/RGMII_RXD0_M0/UART1_TX_M1/PDM_SDI2_M1/I2C3_SCL_M1/GPIO4_A5_d	W3
VSS_A27	A27	VO_LCDC_D15/RGMII_TXCLK_M0/I2S2_MCLK_M1/SPI1_CLK_M0/GPIO3_D6_d	Y2
DDR_DQ14_A/DDR4_DQU2_A/LPDDR4_DQ14_A/DDR3_DQ11/LPDDR3_DQ11	A3	UART1_RX_M0/RGMII_TXD0_M1/I2S0_SDO1_M1/PWM4_M1/RMII_TXD0/GPIO1_D1_d	Y25
DDR_DQ12_A/DDR4_DQU0_A/LPDDR4_DQ12_A/DDR3_DQ13/LPDDR3_DQ12	A4	UART1_TX_M0/RGMII_TXD1_M1/I2S0_SDO2_M1/PWM5_M1/RMII_TXD1/GPIO1_D2_d	Y26
DDR_DQ6_A/DDR4_DQL7_A/LPDDR4_DQ6_A/DDR3_DQ7/LPDDR3_DQ25	A6	UART1_CTSN_M0/RGMII_RXD0_M1/I2S0_SDI3_M1/PWM7_M1/RMII_RXD0/GPIO1_D4_d	Y27
DDR_DQ2_A/DDR4_DQL0_A/LPDDR4_DQ2_A/DDR3_DQ2/LPDDR3_DQ31	A8	VO_LCDC_D20/RGMII_RXD3_M0/UART8_RTSN_M1/SPI1_CSN1_M0/GPIO4_A0_d	Y3

Chapter 3 Electrical Specification

3.1 Absolute Ratings

The below table provides the absolute ratings.
Absolute maximum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute maximum ratings conditions may affect device reliability.
Absolute minimum ratings specify the values beyond which the device may be damaged permanently. Long-term exposure to absolute minimum ratings conditions may affect device reliability.

Table 3-1 Absolute ratings

Parameters	Related Power Group	Min	Max	Unit
Supply voltage for CPU	VDD_CPU	-0.3	1.2	V
Supply voltage for GPU	VDD_GPU	-0.3	1.2	V
Supply voltage for NPU	VDD_NPU	-0.3	1.2	V
Supply voltage for core logic	VDD_LOGIC VDD_LOGIC_MEM	-0.3	0.99	V
0.9V supply voltage	PMU_VDD_LOGIC_0V9 PMUPLL_AVDD_0V9 SYSPLL_AVDD_0V9 USB_AVDD_0V9 MULTI_PHY_AVDD_0V9 MIPI_CSI_RX0_AVDD_0V9 MIPI_CSI_RX1_AVDD_0V9 MIPI_DSI_TX/LVDS_TX_AVDD_0V9	-0.3	0.99	V
1.8V supply voltage	PMUPLL_AVDD_1V8 SYSPLL_AVDD_1V8 USB_AVDD_1V8 MULTI_PHY_AVDD_1V8 MIPI_CSI_RX0_AVDD_1V8 MIPI_CSI_RX1_AVDD_1V8 MIPI_DSI_TX/LVDS_TX_AVDD_1V8 SARADC0_AVDD_1V8 SARADC1_AVDD_1V8 OTP_VCC_1V8	-0.3	1.98	V
3.3V supply voltage	USB_AVDD_3V3	-0.3	3.63	V
Supply voltage for DDR IO	DDRPHY_VDDQ	-0.3	1.65	V
Storage Temperature	Tstg	-40	125	℃
Max Conjunction Temperature	Tj	NA	125	℃

3.2 Recommended Operating Condition

The following table describes the recommended operating conditions.

Table 3-2 Recommended operating condition

Parameters	Symbol	Min	Typ	Max	Unit
Voltage for CPU	VDD_CPU	0.81	0.9	1.15	V
Voltage for GPU	VDD_GPU	0.81	0.9	0.99	V
Voltage for NPU	VDD_NPU	0.81	0.9	0.99	V
Voltage for core logic	VDD_LOGIC VDD_LOGIC_MEM	0.81	0.9	0.99	V
Voltage for PMU	PMU_VDD_LOGIC_0V9	0.81	0.9	0.99	V
PMUIO0 GPIO Power	PMUIO0	2.97	3.3	3.63	V
Digital GPIO Power (3.3V/1.8V)	VCCIO1,VCCIO2, VCCIO3,	2.97	3.3	3.63	V
	VCCIO4,VCCIO5, VCCIO6, PMUIO1	1.62	1.8	1.98	
DDR3 IO VDDQ power	DDRPHY _VDDQ	1.425	1.5	1.575	V
DDR3L IO VDDQ Power	DDRPHY _VDDQ	1.283	1.35	1.417	V
LPDDR3 IO VDDQ Power	DDRPHY _VDDQ	0.994	1.2	1.3	V
DDR4 IO VDDQ Power	DDRPHY _VDDQ	0.994	1.2	1.3	V
LPDDR4 IO VDDQ Power	DDRPHY _VDDQ	1.0	1.1	1.21	V
LPDDR4X IO VDDQ Power	DDRPHY _VDDQ	0.54	0.6	0.66	V
PMU PLL Analog Power(0.9V)	PMUPLL_AVDD_0V9	0.81	0.9	0.99	V
PMU PLL Analog Power(1.8V)	PMUPLL_AVDD_1V8	1.62	1.8	1.98	V
System PLL Analog Power(0.9V)	SYSPLL_AVDD_0V9	0.81	0.9	0.99	V
System PLL Analog Power(1.8V)	SYSPLL_AVDD_1V8	1.62	1.8	1.98	V
USB Analog Power (0.9V)	USB_AVDD_0V9	0.81	0.9	0.99	V
USB Analog Power (1.8V)	USB_AVDD_1V8	1.62	1.8	1.98	V
USB Analog Power (3.3V)	USB_AVDD_3V3	2.97	3.3	3.63	V
Multi-phy Analog Power(0.9V)	MULTI_PHY_AVDD_0V9	0.81	0.9	0.99	V
Multi-phy Analog Power(1.8V)	MULTI_PHY_AVDD_1V8	1.62	1.8	1.98	V
MIPI CSI Analog Power(0.9V)	MIPI_CSI_RX0_AVDD_0V9 MIPI_CSI_RX1_AVDD_0V9	0.81	0.9	0.99	V
MIPI CSI Analog Power(1.8V)	MIPI_CSI_RX0_AVDD_1V8 MIPI_CSI_RX1_AVDD_1V8	1.62	1.8	1.98	V
MIPI DSI Analog Power(0.9V)	MIPI_DSI_TX/LVDS_TX_AVDD_0V9	0.81	0.9	0.99	V
MIPI DSI Analog Power(1.8V)	MIPI_CSI_TX/LVDS_TX_AVDD_1V8	1.62	1.8	1.98	V
SARADC Analog Power(1.8V)	SARADC_AVDD_1V8	1.62	1.8	1.98	V
OTP Analog Power(1.8V)	OTP_VCC_1V8	1.62	1.8	1.98	V
OSC input clock frequency		NA	24	NA	MHz
Max frequency for CPU	Frequency	NA	NA	2	GHz
Max frequency for GPU	Frequency	NA	NA	900	MHz
Max frequency for NPU	Frequency	NA	NA	1	GHz
Ambient Operating Temperature	T$_A$	0	NA	80	℃

Notes:
  ① *Symbol name is same as the pin name in the IO descriptions*

3.3 DC Characteristics

Table 3-3 DC Characteristics

Parameters		Symbol	Min	Typ	Max	Unit
Digital GPIO	Input Low Voltage	Vil	-0.3	NA	0.8	V
@3.3V	Input High Voltage	Vih	2.0	NA	VDDO+0.3	V

	Parameters	Symbol	Min	Typ	Max	Unit
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	2.4	NA	VDDO+0.3	V
	Pullup Resistor	Rpu	16	NA	43	Kohm
	Pulldown Resistor	Rpd	16	NA	43	Kohm
Digital GPIO @1.8V	Input Low Voltage	Vil	-0.3	NA	0.35*VDDO	V
	Input High Voltage	Vih	0.65*VDDO	NA	VDDO+0.3	V
	Output Low Voltage	Vol	-0.3	NA	0.4	V
	Output High Voltage	Voh	1.4	NA	VDDO+0.3	V
	Pullup Resistor	Rpu	16	NA	43	Kohm
	Pulldown Resistor	Rpd	16	NA	43	Kohm

	Parameters	Symbol	Min	Typ	Max	Unit
DDR IO @DDR3 mode	Input High Voltage	Vih_ddr	Vref+0.1		DDRPHY_VDDQ	V
	Input Low Voltage	Vil_ddr	VSSQ		Vref-0.1	V
	output impedence	Rtt	20		60	Ohm
DDR IO @DDR3L mode	Input High Voltage	Vih_ddr	Vref+0.1		DDRPHY_VDDQ	V
	Input Low Voltage	Vil_ddr	VSSQ		Vref-0.1	V
	output impedence	Rtt	20		60	Ohm
DDR IO @DDR4 mode	Input High Voltage	Vih_ddr	Vref+0.1		DDRPHY_VDDQ	V
	Input Low Voltage	Vil_ddr	VSSQ		Vref-0.1	V
	output impedence	Rtt	20		60	Ohm
DDR IO @ LPDDR3 mode	Input High Voltage	Vih_ddr	Vref+0.1		DDRPHY_VDDQ	V
	Input Low Voltage	Vil_ddr	VSSQ		Vref-0.1	V
	output impedence	Rtt	20		60	Ohm
DDR IO @LPDDR4 mode	Input High Voltage	Vih_ddr	Vref+0.1		DDRPHY_VDDQ	V
	Input Low Voltage	Vil_ddr	VSSQ		Vref-0.1	V
	output impedence	Rtt	20		60	Ohm
DDR IO @LPDDR4X mode	Input High Voltage	Vih_ddr	Vref+0.1		DDRPHY_VDDQL	V
	Input Low Voltage	Vil_ddr	VSSQ		Vref-0.1	V
	output impedence	Rtt	20		60	Ohm

3.4 Electrical Characteristics for General IO

Table 3-4 Electrical Characteristics for Digital General IO

	Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Digital GPIO @3.3V	Input leakage current	Ii	Vin = 3.3V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 3.3V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 3.3V, pulldown disabled	NA	NA	10	uA

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
			Vin = 3.3V, pulldown enabled	NA	NA	10	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	10	uA
Digital GPIO @1.8V	Input leakage current	Ii	Vin = 1.8V or 0V	NA	NA	10	uA
	Tri-state output leakage current	Ioz	Vout = 1.8V or 0V	NA	NA	10	uA
	High level input current	Iih	Vin = 1.8V, pulldown disabled	NA	NA	10	uA
			Vin = 1.8V, pulldown enabled	NA	NA	10	uA
	Low level input current	Iil	Vin = 0V, pullup disabled	NA	NA	10	uA
			Vin = 0V, pullup enabled	NA	NA	10	uA

3.5 Electrical Characteristics for PLL

Table 3-5 Electrical Characteristics for Frac PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Frac PLL	Input clock frequency(Frac)	F_{in}	Fin = FREF @1.8V/0.99V	1	NA	1200	MHz
	VCO operating range	F_{vco}	Fvco = Fref * FBDIV @3.3V/0.99V	950	NA	3800	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV @3.3V/0.99V	19	NA	3800	MHz
	Lock time	T_{lt}	@ 3.3V/0.99V, FREF=24M,REFDIV=1	NA	250	500	Input clock cycles

Table 3-6 Electrical Characteristics for Int-PLL

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
Int PLL	Input clock frequency(Frac)	F_{in}	Fin = FREF @1.8V/0.99V	10	NA	800	MHz
	VCO operating range	F_{vco}	Fvco = Fref * FBDIV @3.3V/0.99V	475	NA	1900	MHz
	Output clock frequency	F_{out}	Fout = Fvco/POSTDIV @3.3V/0.99V	9	NA	1900	MHz
	Lock time	T_{lt}	@ 3.3V/0.99V, FREF=24M,REFDIV=1	NA	1000	1500	Input clock cycles

Notes:

  ① *REFDIV is the input divider value;*

  ② *FBDIV is the feedback divider value;*

  ③ *POSTDIV is the output divider value*

3.6 Electrical Characteristics for USB 2.0 Interface

Table 3-7 Electrical Characteristics for USB 2.0 Interface

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Transmitter						
Output resistance	ROUT	Classic mode (Vout = 0 or 3.3V)	40.5	45	49.5	ohms
		HS mode (Vout = 0 to 800mV)	40.5	45	49.5	ohms
Output Capacitance	COUT	seen from D+ or D-			3	pF
Output Common Mode Voltage	VM	Classic (LS/FS) mode	1.45	1.65	1.85	V
		HS mode	0.175	0.2	0.225	V
Differential output signal high	VOH	Classic (LS/FS); Io=0mA	2.97	3.3	3.63	V
		Classic (LS/FS); Io=6mA	2.2	NA	NA	V
		HS mode; Io=0mA	360	400	440	mV
Differential output signal low	VOL	Classic (LS/FS); Io=0mA	-0.33	0	0.33	V
		Classic (LS/FS); Io=6mA	NA	0.3	0.8	V
		HS mode; Io=0mA	-40	0	40	mV
Receiver						
Receiver sensitivity	RSENS	Classic mode	NA	+-250	NA	mV
		HS mode	NA	+-25	NA	mV
Receiver common mode	RCM	Classic mode	0.8	1.65	2.5	V
		HS mode (differential and squelch comparator)	0.1	0.2	0.3	V
		HS mode (disconnect comparator)	0.5	0.6	0.7	V
Input capacitance (seen at D+ or D-)			NA	NA	3	pF
Squelch threshold			100	112	150	mV
Disconnect threshold			570	590	625	mV
High input level	VIH		0.6	NA	NA	V
Low input level	VIL		NA	NA	0.2	V

3.7 Electrical Characteristics for DDR IO

Table 3-8 Electrical Characteristics for DDR IO

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
DDR IO @DDR3 mode	Input leakage current		@ 1.5V , 125℃	-80		6	uA
DDR IO @DDR3L mode	Input leakage current		@ 1.35V , 125℃	-65		5	uA
DDR IO @DDR4 mode	Input leakage current		@ 1.2V , 125℃	-50		4	uA
DDR IO @LPDDR3 mode	Input leakage current		@ 1.2V , 125℃	-50		4	uA

Parameters		Symbol	Test condition	Min	Typ	Max	Unit
DDR IO @LPDDR4 mode	Input leakage current		@ 1.1V , 125℃	-45		3.5	uA
DDR IO @LPDDR4X mode	Input leakage current		@ 0.6V , 125℃	-20		1.5	uA

3.8 Electrical Characteristics for TSADC

Table 3-9 Electrical Characteristics for TSADC

Parameters	Symbol	Test condition	Min	Typ	Max	Unit
Temperature Resolution			NA	+-5	NA	℃
Temperature Range			-40	NA	125	℃

3.9 Electrical Characteristics for MIPI DSI

Table 3-10 Electrical Characteristics for MIPI DSI

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Common-mode variations above 450 MHz	ΔVcmtx(HF)		NA	NA	15	mVrms
Common-mode variations between 50MHz – 450MHz	ΔVcmtx(LF)		NA	NA	25	mVpeak
20%-80% rise time and fall time	Tr and Tf		NA	NA	0.3	UI
			10	NA	NA	ps

3.10 Electrical Characteristics for MIPI CSI

Table 3-11 Electrical Characteristics for MIPI CSI

Parameters	Symbol	Test condition	Min	Typ	Max	Units
Common-mode interference beyond 450 MHz	ΔVcmrx(HF)		NA	NA	100	mV
Common-mode interference 50MHz-450MHz	ΔVcmrx(LF)		NA	NA	50	mV
Common-mode termination	Ccm		NA	NA	60	pF
Input pulse rejection	Espike		NA	NA	300	V.ps
Minimum pulse width response	Tmin-rx		20	NA	NA	ns
Peak interference amplitude	Vint		NA	NA	200	mV
Interference frequency	Fint		450	NA	NA	MHz

3.11 Electrical Characteristics for Multi-PHY

Table 3-12 Electrical Characteristics for PCIe PHY

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Transmitter						
Differential p-pTx voltage swing	$V_{TX-DIFF-PP}$		0.8	NA	1.2	V
Low power differential p-p Tx voltage swing	$V_{TX-DIFF-PP-LOW}$		0.4	NA	1.2	V
Tx de-emphasis level ratio	$R_{TX-DIFF-DC}$		80	NA	120	ohm

Parameters	Symbol	Condition	Min	Typ	Max	Unit
Single Ended Output Resistance Matching	$R_{TX-DC-OFFSET}$		NA	NA	5	%
The amount of voltage change allowed during Receiver Detection	$V_{TX-RCV-DETECT}$		NA	NA	600	mV
Output rising time for 20% to 80%	Tr		25	NA	NA	ps
Output falling time for 20% to 80%	Tf		25	NA	NA	ps
AC Coupling Capacitor(USB3.0/PCIE)	C_{TX}		75	NA	200	nF
AC Coupling Capacitor(SATA)	C_{TX}		6	NA	12	nF
Unit Interval	UI		399.88	NA	400.12	ps
Input Voltage Swing	$V_{rxdpp-c}$		250	NA	1200	mV
Input differential impedance	R_{rxd-c}		80	NA	120	ohm
Single Ended input Resistance Matching	$T_{rxd-c-ms}$		NA	NA	5	%

Chapter 4 Thermal Management

4.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature has to be below 125℃.

4.2 Package Thermal Characteristics

Table 4-1 provides the thermal resistance characteristics for the package used on the SoC. The resulting simulation data for reference only, please prevail in kind test.

Table 4-1 Thermal Resistance Characteristics

Parameter	Symbol	Typical	Unit
Junction-to-ambient thermal resistance	θ_{JA}	22.646	(℃/W)
Junction-to-board thermal resistance	θ_{JB}	15.937	(℃/W)
Junction-to-case thermal resistance	θ_{JC}	3.347	(℃/W)

Note: The testing PCB is 4 layers, 114.3mmx101.6mm, *1.6mm thickness, Ambient temperature is 25℃.*

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