Rockchip RK806 Datasheet

Revision 1.2
Jul.2022

Revision History

Date	Revision	Description
2022-07-11	1.2	1. Modify the description of the dimension 2. Modify NLDO and PLDO voltage range description of the DC Characteristics 3. Modify the Read and write waveforms of the SPI 4. Add the restrictions of the PWRCTRLn_FUN
2022-03-22	1.1	5. Modify description of the Register Description 6. Modify description of the SPI communication
2021-11-02	1.01	1. Modify block diagram and typical application diagram; 2. Modify BUCKx inductor current threshold information. 3. Modify Package Thermal Characteristics description 4. Modify description of the BUCK1
2021-10-20	0.1	Initial release

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Chapter 1 Introduction

1.1 Overview

The RK806 is a complex power-management integrated circuit (PMIC). The RK806 can provide a complete power management solution with very few external components.

The RK806 provides 10 fast load transient synchronous step-down converters. The device also contains 6 LDO regulators, 5 NMOS LDO regulators for high efficiency. Power-up/power-down controller is configurable and can support any customized power-up/power-down sequences (OTP based).

The RK806 integrates 10 channels step-down DC-DC converters. All of them adopt ripple base control to achieve very fast load transient response. Meanwhile, all of them can dynamically adjust the output voltage, as required by the processor based on the processor's operation status so as to maximize the system efficiency. The output voltages of most channels can be configured through the I2C or SPI interface. The inputs of all channels have soft start function, which greatly reduces the inrush current at the startup. 2MHz switching frequency and good control method decrease the external inductance and capacitance.

The RK806 integrates 6 channels LDO regulators. The inputs of all LDO regulators could be decrease to 2V for high convert efficiency. Meanwhile 5 channels NMOS LDO regulators are integrated. The output voltages of all LDO regulators can be configured through the I2C or SPI interface.

Two RK806 could work together that one of them is master, another is slave. The power-up/power-down sequences could be synchronization.

The RK806 is available in a QFN68 7.0 mm x 7.0 mm package, with a 0.35-mm pin pitch.

1.2 Feature

- Input range: 2.7V - 5.5V
- Low standby current of 10uA
- Power channels:
  - BUCK1: 0.5V~3.4V, 6.5A max, very fast transient response
  - BUCK2/3/4: 0.5V~3.4V, 5A max, very fast transient response
  - BUCK5/6/7/8/9/10: 0.5V~3.4V, 3A max, very fast transient response
  - NLDO1/2/5: 0.5V~3.4V, 300mA max
  - NLDO3/4: 0.5V~3.4V, 500mA max
  - PLDO1/4: 0.5V~3.4V, 500mA max
  - PLDO2/3/5: 0.5V~3.4V, 300mA max
  - VCCIO：0.5V~3.4V, 300mA max
- OTP Programmable power up/down sequences and voltage
- Support dual PMIC cooperation
- Support I2C and SPI two communication modes
- Package:7mmx7mm QFN68

1.3 Block Diagram

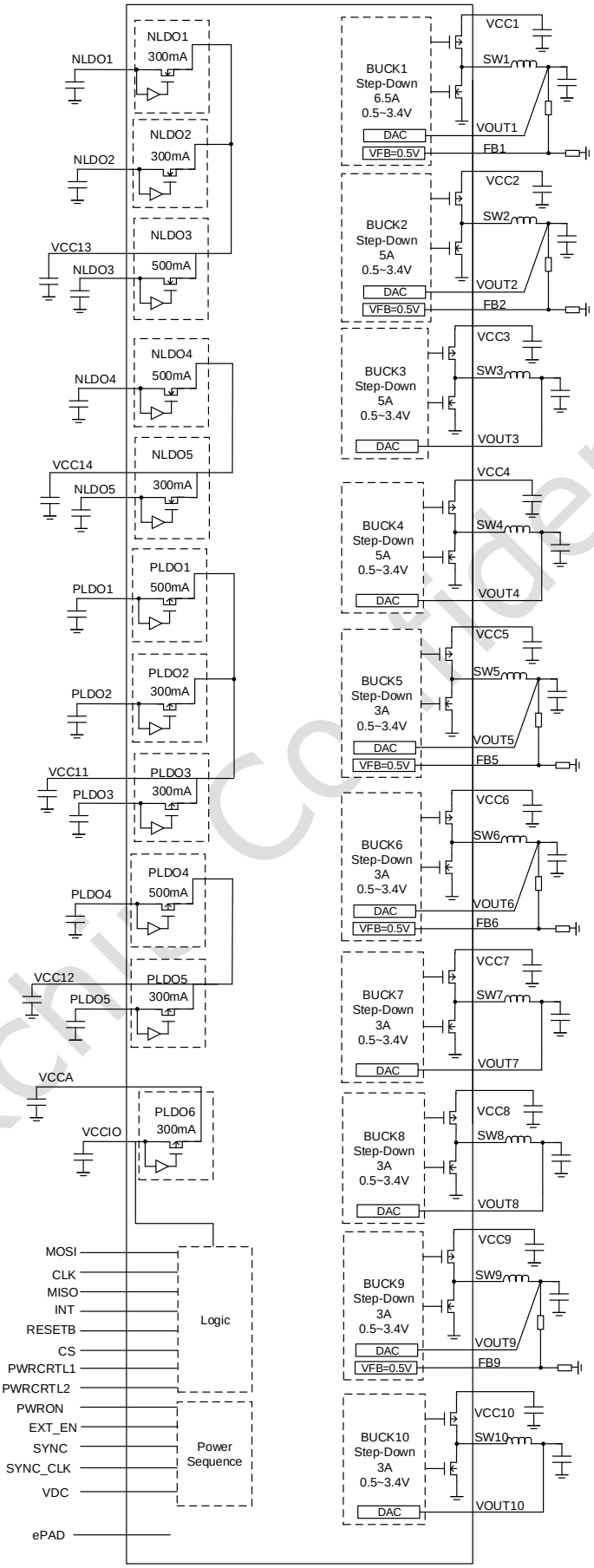


Fig. 1-1 RK806 Functional Block Diagram

1.4 Typical Application Diagrams

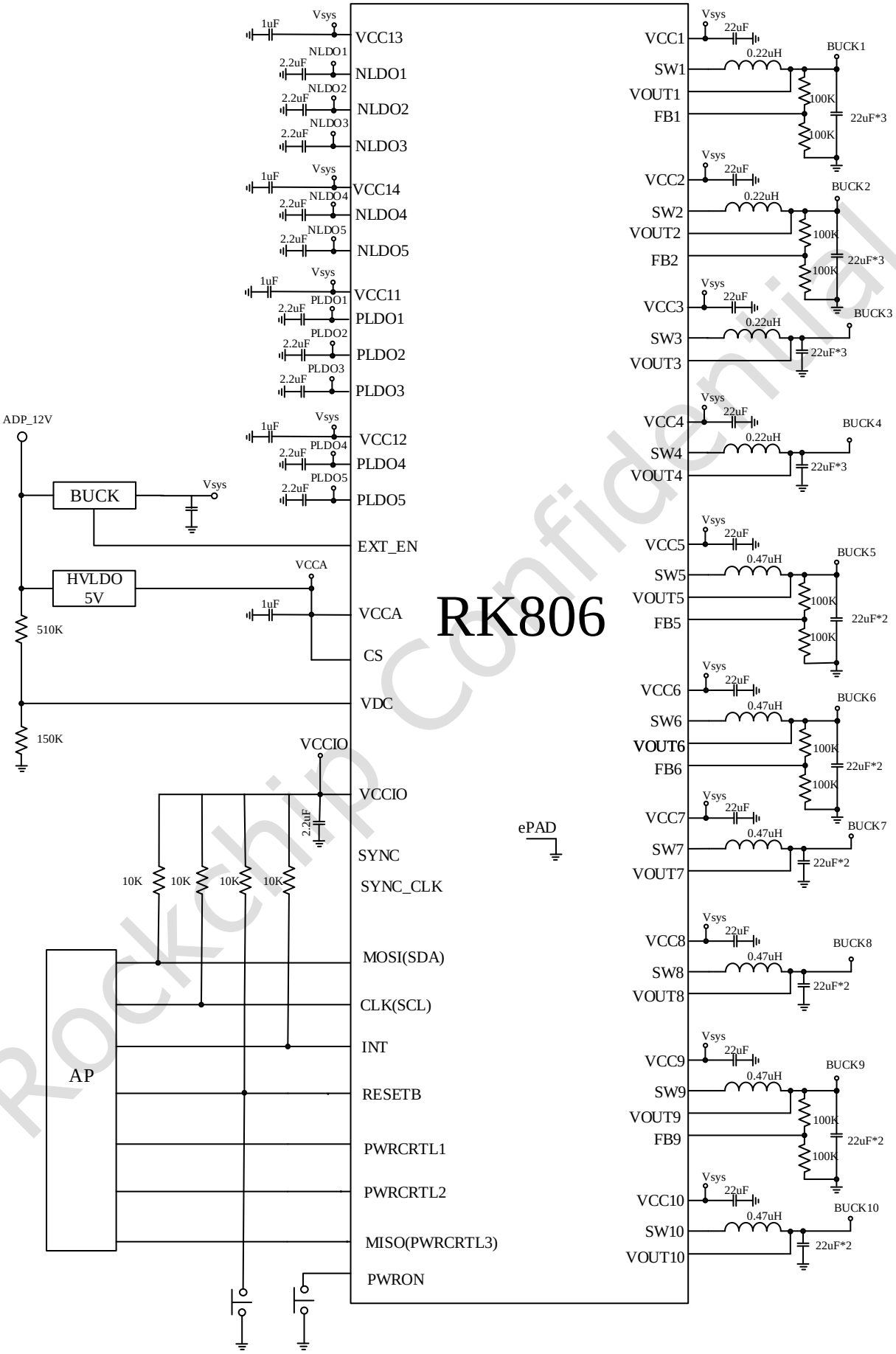


Fig. 1-2 RK806 Typical Application Diagram

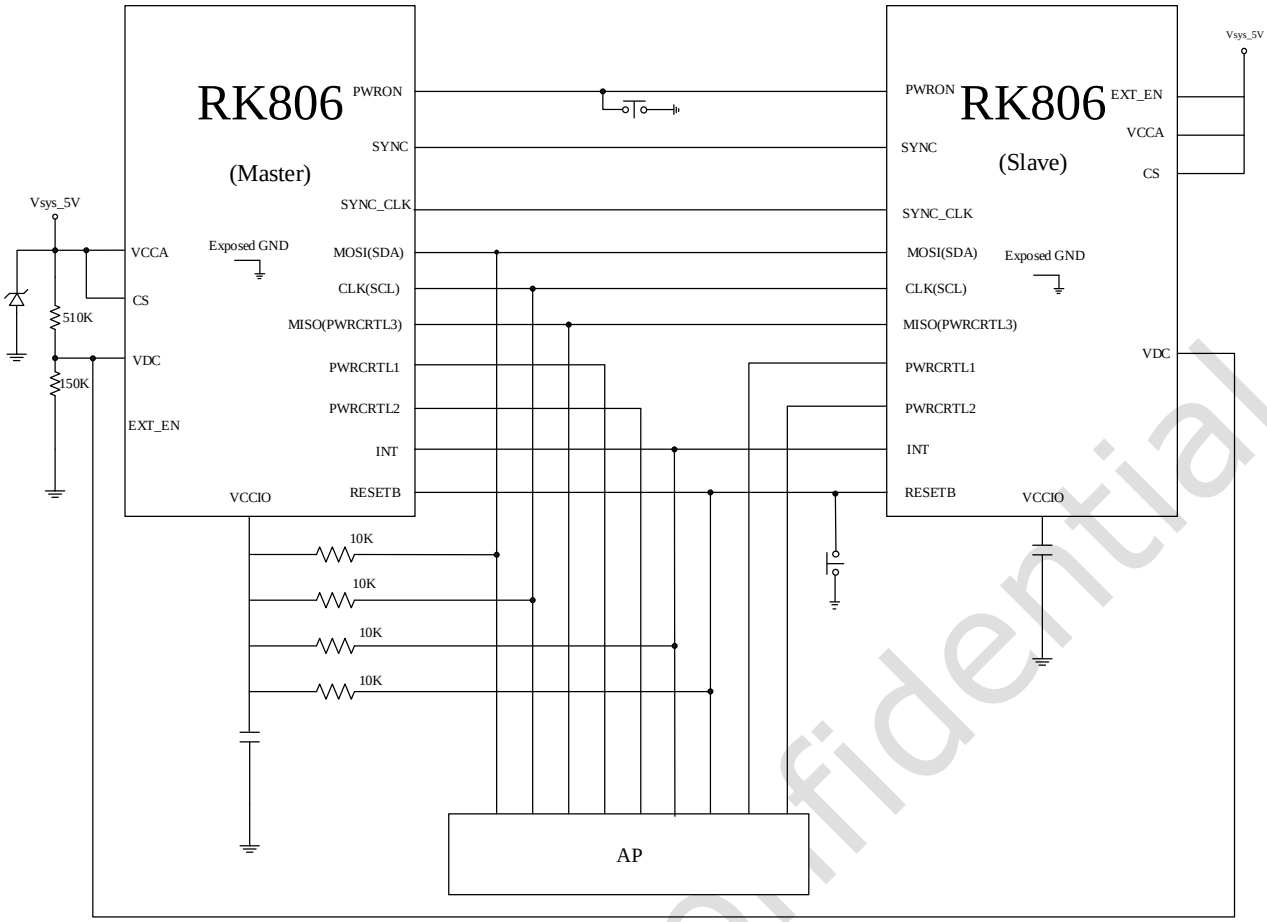


Fig. 1-3 Two RK806 Typical Application Diagram (I2C communication mode)

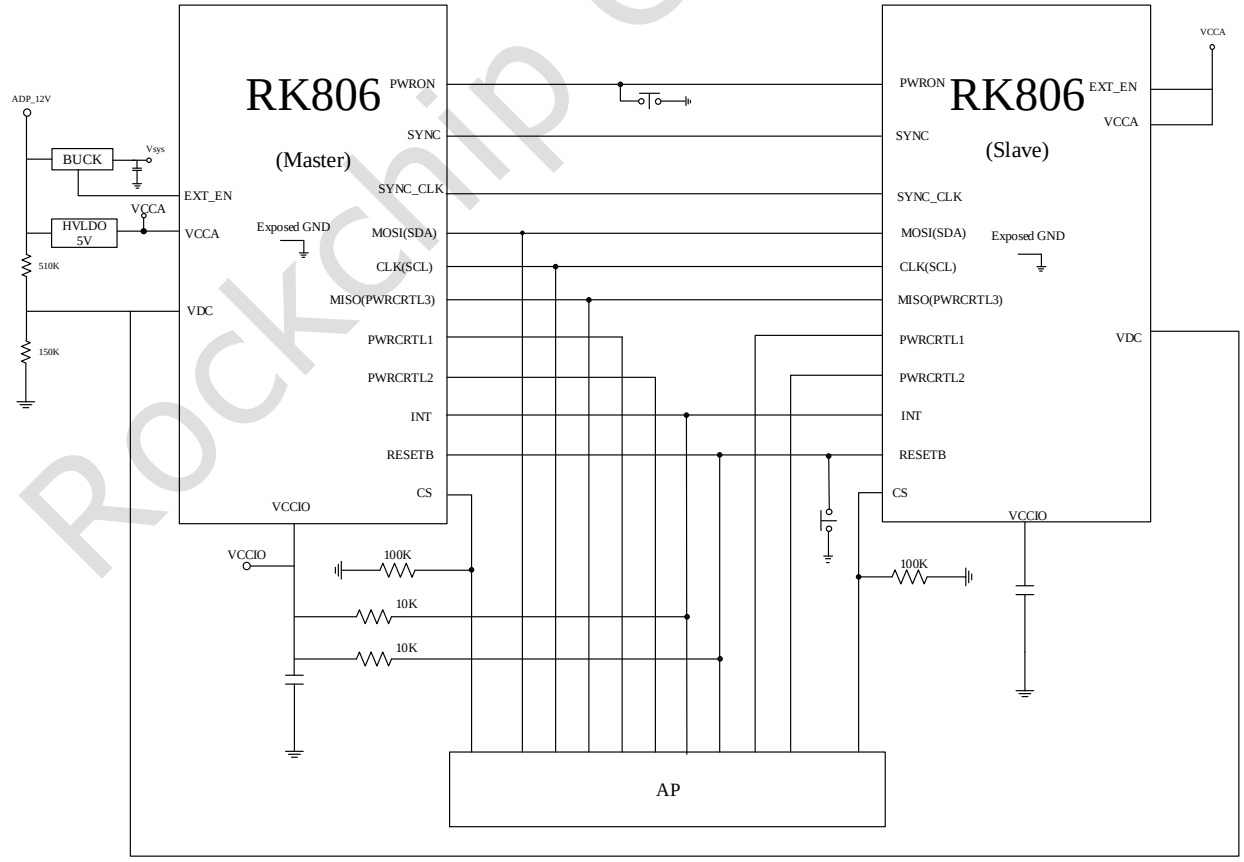


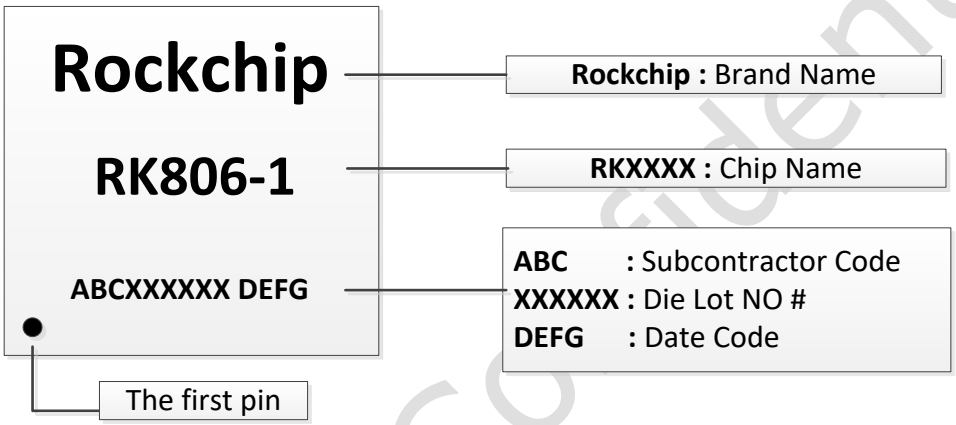
Fig. 1-4 Two RK806 Typical Application Diagram (SPI communication mode)

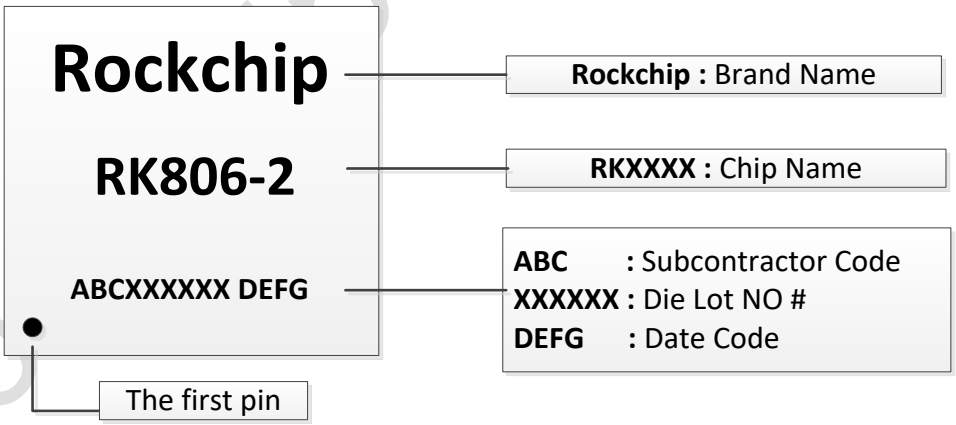
Chapter 2 Package information

2.1 Ordering Information

Orderable Device	RoHS status	Package	Package Detail
RK806-1	RoHS	QFN68 (7X7)	2000 pcs/ tape, 5 tapes/box, by reel
RK806-2	RoHS	QFN68 (7X7)	2000 pcs/ tape, 5 tapes/box, by reel

2.2 Top Marking





2.3 Dimension

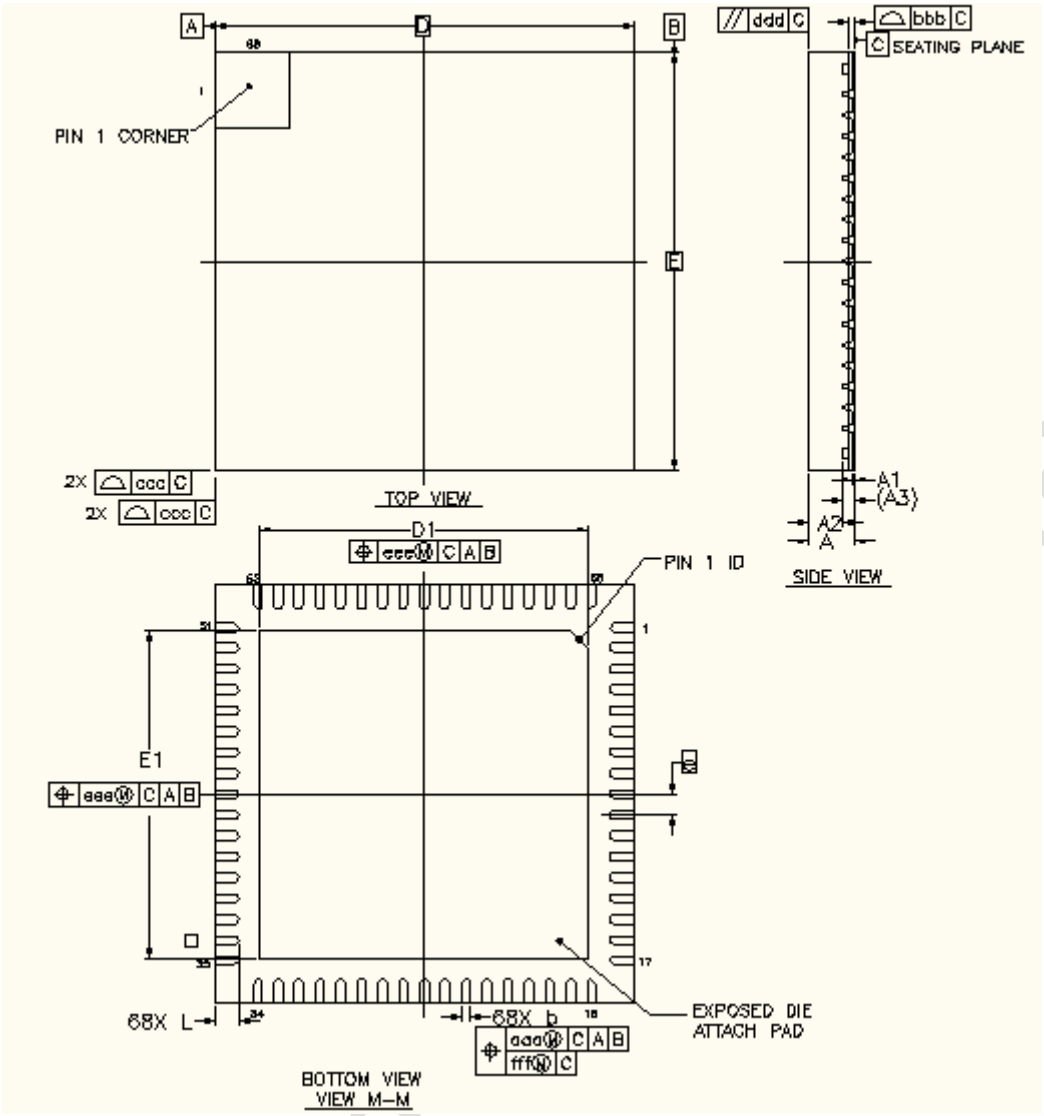


Fig. 2-1 QFN687mm X 7mm

DESCRIPTION	SYMBOL	MILLIMETER		
		MIN	NOM	MAX
TOTAL THICKNESS	A	0.80	0.85	0.90
STAND OFF	A1	0	0.035	0.05
MOLD THICKNESS	A2	-	0.55	0.57
MATERIAL THICKNESS	A3	-	0.203_{REF}	-
PACKAGE SIZE	D	-	7_{BSC}	-
	E	-	7_{BSC}	-
EP SIZE	D1	5.39	5.49	5.59
	E1	5.39	5.49	5.59
LEAD LENGTH	L	0.30	0.4	0.50
LEAD PITCH	e		0.35_{BSC}	
LEAD WIDTH	b	0.1	0.15	0.2
LEAD OSITION OFFSET	aaa		0.07	
LEAD COPLANARITY	bbb		0.08	
PACKAGE EDGE PROFILE	ccc		0.10	
MOLD FLATNESS	ddd		0.10	
EP POSITION OFFSET	eee		0.10	
	fff		0.05	

Note:

1. *Coplanarity applies to leads, corner leads and die attach pad.*

2. *Dimension b applies to metalized terminal and is measured between 0.15mm and 0.30mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension b should not be measure in that radius area.*

2.4 Pin Assignment

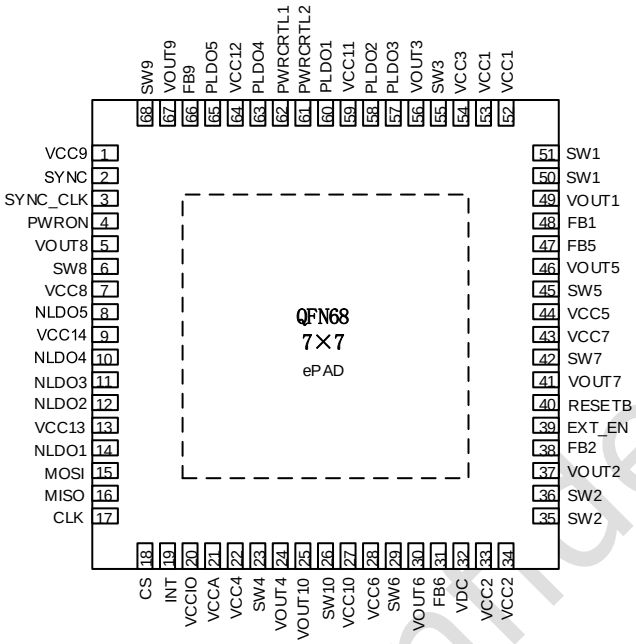


Fig. 2-2 Pin Assignment QFN7x7-68(Pitch=0.35mm)

2.5 Pinout Number Order

PIN NO	PIN NAME	PIN DESCRIPTION	I/O
1	VCC9	Power supply of buck9.	I
2	SYNC	Master and slave synchronization signal.	I/O
3	SYNC_CLK	32k synchronization clk.	I/O
4	PWRON	Power on key. The internal pull-up resistance is about 45K to VCCA.	I
5	VOUT8	Output feedback voltage of buck8.	I
6	SW8	Switching node of buck8.	O
7	VCC8	Power supply of buck8.	I
8	NLDO5	NMOS LDO5 output.	O
9	VCC14	Power supply of NLDO4/5.	I
10	NLDO4	NMOS LDO4 output.	O
11	NLDO3	NMOS LDO3 output.	O
12	NLDO2	NMOS LDO2 output.	O
13	VCC13	Power supply of NLDO1/2/3.	I
14	NLDO1	NMOS LDO1 output.	O
15	MOSI/SDA	SPI MOSI. I2C SDA.	I/O
16	MISO/ PWRCRTL3	SPI MISO. PWRCRTL3 control.	I/O
17	CLK/SCL	SPI CLK. I2C SCL.	I
18	CS	Select SPI/I2C mode when powering on. (I2C mode when connecting to VCCA, SPI mode when not connecting to VCCA). In SPI mode, use for CS pin of SPI	I

PIN NO	PIN NAME	PIN DESCRIPTION	I/O
19	INT	Interrupt.	O
20	VCCIO	Output for I2C/SPI.	O
21	VCCA	Analog power supply. Power supply of PLDO6/RESETB/INT and system logic.	I
22	VCC4	Power supply of buck4.	I
23	SW4	Switching node of buck4.	O
24	VOUT4	Output feedback voltage of buck4.	I
25	VOUT10	Output feedback voltage of buck10.	I
26	SW10	Switching node of buck10.	O
27	VCC10	Power supply of buck10.	I
28	VCC6	Power supply of buck6.	I
29	SW6	Switching node of buck6.	O
30	VOUT6	Output feedback voltage of buck6.	I
31	FB6	Extended divided resistor mode feedback voltage of buck6.	I
32	VDC	VDC power on signal.	I
33	VCC2	Power supply of buck2.	I
34	VCC2	Power supply of buck2.	I
35	SW2	Switching node of buck2.	O
36	SW2	Switching node of buck2.	O
37	VOUT2	Output feedback voltage of buck2.	I
38	FB2	External divided resistor mode feedback voltage of buck2.	I
39	EXT_EN	Control extended DCDC enable. Master/Slave select.	I/O
40	RESETB	Reset the AP. The equivalent capacitance of this foot to GND cannot be greater than 0.3uF	I/O
41	VOUT7	Output feedback voltage of buck7.	I
42	SW7	Switching node of buck7.	O
43	VCC7	Power supply of buck7.	I
44	VCC5	Power supply of buck5.	I
45	SW5	Switching node of buck5.	O
46	VOUT5	Output feedback voltage of buck5.	I
47	FB5	External divided resistor mode feedback voltage of buck5.	I
48	FB1	External divided resistor mode feedback voltage of buck1.	I
49	VOUT1	Output feedback voltage of buck1.	I
50	SW1	Switching node of buck1.	O
51	SW1	Switching node of buck1.	O
52	VCC1	Power supply of buck1.	I
53	VCC1	Power supply of buck1.	I
54	VCC3	Power supply of buck3.	I
55	SW3	Switching node of buck3.	O
56	VOUT3	Output feedback voltage of buck3.	I
57	PLDO3	PMOS LDO3 output.	O
58	PLDO2	PMOS LDO2 output.	O
59	VCC11	Power supply of PLDO1/2/3.	I
60	PLDO1	PMOS LDO1 output.	O
61	PWRCRTL2	PWRCRTL2 control.	I/O
62	PWRCRTL1	PWRCRTL1 control.	I/O
63	PLDO4	PMOS LDO4 output.	O
64	VCC12	Power supply of PLDO4/5.	I
65	PLDO5	PMOS LDO5 output.	O

PIN NO	PIN NAME	PIN DESCRIPTION	I/O
66	FB9	External divided resistor mode feedback voltage of buck9.	I
67	VOUT9	Output feedback voltage of buck9.	I
68	SW9	Switching node of buck9.	O
Exposed	ePAD	Ground	

Chapter 3 Electrical Characteristics

3.1 Absolute Maximum Ratings

Parameter	Min	Max	Units
Voltage range all pins	-0.3	6.5	V
Storage temperature range, T_S	-40	150	℃
Operating temperature range, T_J	-40	125	℃
Maximum Soldering Temperature, T_{SOLDER}		300	℃

Note：

Exposure to the conditions exceeded absolute maximum ratings may cause the permanent damages and affect the reliability and safety of both device and systems using the device. The functional operations cannot be guaranteed beyond specified values in the recommended conditions.

3.2 Recommended Operating Conditions

Test conditions: VCCA=5.0V, TA=25°C for typical values, unless otherwise noted.

Parameter	Min	TYP	Max	Units
Voltage range on pins VCCx/VCCA/SYNC/ SYNC_CLK/VDC/PWRON/EST_EN/CS/RESETB/INT	2.7	5	5.5	V
Power Dissipation			2	W
Voltage range on pin VCCIO/MOSI/MISO/ PWRCRTL1/ PWRCRTL2	0.5		3.4	V

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
I2C interface (7bits I2C address ： Master I2C address is 0x23, Slave I2C address is 0x25)						
SCL clock frequency	f_{SCL}				1000	KHz
LOGIC INPUT						
Input LOW-Level Voltage:PWRON,SYNC,SYNS_ CLK	V_{IL}				0.3+VCCA	V
Input LOW-Level Voltage: VDC	V_{IL1}				0.65	V
Input HIGH-Level Voltage: MOSI,MISO,CS,PWRCRTL1/2, RESETB,INT	V_{IH1}		VCCIO*0.7		0.3+VCCIO	V
Input HIGH-Level Voltage: PWRON , VCCx,VCCA,SYNC, SYNC_CLK	V_{IH2}		VCCA*0.7		0.3+VCCA	V
Input HIGH-Level Voltage: VDC	V_{IH3}		0.88			V

3.3 DC Characteristics

Test conditions: VCCA=5.0V,TA=25°C for typical values, unless otherwise noted.

PARAMETERS	SYMBOL	Note		MIN	TYP	MAX	UNIT
Power dissipation							
Shut down Current	Isd				10	12	uA
Power on current 1: All bucks, LDOs power on, Null load	Iq1				1.803		mA
Power on and sleep current: All bucks, LDOs power on, low power mode, sleep mode, Null load	Isleep				0.769		mA
System Characteristics							
VB_UV threshold, when the VCCx voltage is lower than it, The PMIC would be shutdown.	Vuv	2.7V~3.4V by I2C programmed. Typical is 2.7V.	VB_UV_SEL=0b000	2.646	2.7	2.754	V
			VB_UV_SEL=0b011	2.94	3.0	3.06	V
			VB_UV_SEL=0b111	3.332	3.4	3.468	V
VB_LO threshold, when the VCCx voltage is lower than it, The PMIC would be shut down or interrupt happen.	Vlo	2.8V~3.5V by I2C programmed. Typical is 3.2V.	VB_LO_SEL=0b000	2.744	2.8	2.856	V
			VB_LO_SEL=0b100	3.136	3.2	3.264	V
			VB_LO_SEL=0b111	3.43	3.5	3.57	V
VB_OV threshold, when the VCCx voltage is higher than it, The PMIC would be shutdown.	Vov			5.8	6.0	6.2	V
TSD threshold, when the temperature is higher than it, The PMIC would be shutdown.	Tsd	140/160℃ by I2C/SPI programmed. Typical is 160℃.	TSD_TEMP=0b0	135	140	145	℃
			TSD_TEMP=0b1	155	160	165	℃
T warning threshold, when the temperature is higher than it, interrupt happen.	Twa	85~115℃ by I2C/SPI programmed. Typical is 115℃.	HOTDIE_TEMP[1:0]=0b00	80	85	90	℃
			HOTDIE_TEMP=0b01	90	95	100	℃
			HOTDIE_TEMP=0b10	100	105	110	℃
			HOTDIE_TEMP=0b11	110	115	120	℃
Long press PWRON key time	Tlp	6s~12s by I2C/SPI programmed. Typical is 6s.	PWRON_LP_OFF_TIME=0b00	5.76	6	6.24	s
			PWRON_LP_OFF_TIME=0b01	7.68	8	8.32	s
			PWRON_LP_OFF_TIME=0b10	9.6	10	10.4	s
			PWRON_LP_OFF_TIME=0b11	11.52	12	12.48	s
Short press PWRON key time	Tst	20ms/500ms by I2C/SPI programmed and OTP programed. Typical is 500ms.	PWRON_ON_TIME=0b0	480	500	520	ms
			PWRON_ON_TIME=0b1	19.2	20	20.8	ms

Test conditions: VCCA=5.0V,TA=25°C for typical values, unless otherwise noted.

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
BUCK1: Fast load transient response step-down converter						
Input supply voltage range	Vcc1		2.7		5.5	V
Feedback Voltage, Default	Vfb1	Selection of external resistor divider, R1=R2=100K	0.99	1.0	1.01	V
Internal Feedback Reference	Vref_exfb	Default disable. Enable in Register 0xFD<0>=1.	0.495	0.5	0.505	V
Output Voltage Accuracy @ all load @ all input voltage range	Vfb1	If internal divide mode selected: 0.5V~3.4V by I2C/SPI programmed. Typical is 0.8V.Adjust in Register 0x1A, Step=6.25mV.	0.792	0.8	0.808	V
Load Transient Response L=0.22uH, Cout=66uF.	Vdrop1	0.65A to 6.5A, 1A/uS, Vout=0.8V		38		mV
Rated output current	Imax1		6.5			A
Switching Frequency when CCM mode	Fsw1	Vin-Vout>1.5V		2		MHz
Conversion Efficiency (Vin=4.2V,Vout=0.8V)		Iout=6.5A Iout=1.5A Iout=0.65A		68 85 81		%
BUCK2: Fast load transient response step-down converter						
Input supply voltage range	Vcc2		2.7		5.5	V
Feedback Voltage, Default	Vfb2	Selection of external resistor divider, R1=R2=100K	0.99	1.0	1.01	V
Internal Feedback Reference	Vref_exfb	Default disable. Enable in Register 0xFD<1>=1.	0.495	0.5	0.505	V
Output Voltage Accuracy @ all load @ all input voltage range	Vfb2	If internal divide mode selected: 0.5V~3.4V by I2C /SPI programmed. Typical is 0.8V. Adjust in Register 0x1B, Step=6.25mV.	0.792	0.8	0.808	V
Load Transient Response L=0.22uH, Cout=66uF.	Vdrop2	0.5A to 5A, 1A/uS, Vout=0.8V		30		mV
Rated output current	Imax2		5			A
Switching Frequency when CCM mode	Fsw2	Vin-Vout>1.5V		2		MHz
Conversion Efficiency (Vin=4.2V,Vout=0.8V)		Iout=5A Iout=1A Iout=0.5A		67 84 81		%
BUCK3: Fast load transient response step-down converter						
Input supply voltage range	Vcc3		2.7		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vbuck3	0.5V~3.4V by I2C /SPI programmed. Typical is 0.8V. Adjust in Register 0x1C, Step=6.25mV	0.792	0.8	0.808	V

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
Load Transient Response L=0.22uH, Cout=66uF.	Vdrop3	0.5A to 5.0A, 1A/uS, Vout=0.8V		30		mV
Rated output current	Imax3		5			A
Switching Frequency when CCM mode	Fsw3	Vin-Vout>1.5V		2		MHz
Conversion Efficiency (Vin=4.2V,Vout=0.8V)		Iout=5A Iout=1A Iout=0.5A		66 84 82		%
BUCK4: Fast load transient response step-down converter						
Input supply voltage range	Vcc4		2.7		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vfb4	0.5V~3.4V by I2C /SPI programmed. Typical is 0.8V. Adjust in Register 0x1D, Step=6.25mV	0.792	0.8	0.808	V
Load Transient Response L=0.22uH, Cout=66uF.	Vdrop4	0.5A to 5A, 1A/uS, Vout=0.8V		22		mV
Rated output current	Imax4		5			A
Switching Frequency when CCM mode	Fsw4	Vin-Vout>1.5V	2.242	2.3	2.357	MHz
Conversion Efficiency (Vin=4.2V,Vout=0.8V)		Iout=5A Iout=1A Iout=0.5A		66 84 82		%
BUCK5: Fast load transient response step-down converter						
Input supply voltage range	Vcc5		2.7		5.5	V
Feedback Voltage, Default	Vfb5	Selection of external resistor divider, R1=R2=100K.	0.99	1.0	1.01	V
Internal Feedback Reference	Vref_exfb	Default disable. Enable in Register 0xFD<4>=1.	0.495	0.5	0.505	V
Output Voltage Accuracy @ all load @ all input voltage range	Vfb5	If internal divide mode selected: 0.5V~3.4V by I2C /SPI programmed. Typical is 0.8V. Adjust in Register 0x1E, Step=6.25mV.	0.792	0.8	0.808	V
Load Transient Response L=470nH, Cout=44uF.	Vdrop5	0.3A to 3A, 1A/uS, Vout=0.8V		20		mV
Rated output current	Imax5		3			A
Switching Frequency when CCM mode	Fsw5	Vin-Vout>1.5V		2		MHz
Conversion Efficiency (Vin=4.2V,Vout=0.8V)		Iout=3A Iout=1A Iout=0.25A		65 82 81		%
BUCK6: Fast load transient response step-down converter						
Input supply voltage range	Vcc6		2.7		5.5	V
Feedback Voltage, Default	Vfb6	Selection of external resistor divider, R1=R2=100K.	0.99	1.0	1.01	V
Internal Feedback Reference	Vref_exfb	Default disable. Enable in Register 0xFD<5>=1.	0.495	0.5	0.505	V
Output Voltage Accuracy @ all load @ all input voltage range	Vfb6	If internal divide mode selected:	0.792	0.8	0.808	V

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
		0.5V~3.4V by I2C/SPI programmed. Typical is 0.8V. Adjust in Register 0x1F, Step=6.25mV.				
Load Transient Response L=470nH, Cout=44uF.	Vdrop6	0.3A to 3A, 1A/uS, Vout=0.8V		20		mV
Rated output current	Imax6		3			A
Switching Frequency when CCM mode	Fsw6	Vin-Vout>1.5V		2		MHz
Conversion Efficiency (Vin=4.2V,Vout=0.8V)		Iout=2.5A Iout=1A Iout=0.25A		65 82 81		%
BUCK7: Fast load transient response step-down converter						
Input supply voltage range	Vcc7		2.7		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vfb7	0.5V~3.4V by I2C /SPI programmed. Typical is 0.8V. Adjust in Register 0x20, Step=6.25mV.	0.792	0.8	0.808	V
Load Transient Response L=470nH, Cout=44uF.	Vdrop7	0.3A to 3A, 1A/uS, Vout=0.8V		22		mV
Rated output current	Imax7		3			A
Switching Frequency when CCM mode	Fsw7	Vin-Vout>1.5V		2		MHz
Conversion Efficiency (Vin=4.2V,Vout=0.8V)		Iout=3A Iout=1A Iout=0.25A		65 82 81		%
BUCK8: Fast load transient response step-down converter						
Input supply voltage range	Vcc8		2.7		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vfb8	0.5V~3.4V by I2C / SPI programmed. Typical is 0.8V. Adjust in Register 0x21, Step=6.25mV	0.792	0.8	0.808	V
Load Transient Response L=470nH, Cout=44uF.	Vdrop8	0.3A to 3A, 1A/uS, Vout=0.8V		22		mV
Rated output current	Imax8		3			A
Switching Frequency when CCM mode	Fsw8	Vin-Vout>1.5V		2		MHz
Conversion Efficiency (Vin=4.2V,Vout=0.8V)		Iout=3A Iout=1A Iout=0.25A		65 82 81		%
BUCK9: Fast load transient response step-down converter						
Input supply voltage range	Vcc9		2.7		5.5	V
Feedback Voltage, Default	Vfb9	Selection of external resistor divider, R1=R2=100K.	0.99	1.0	1.01	V
Internal Feedback Reference	Vref_exfb	Default disable. Enable in Register 0xFE<0>=1.	0.495	0.5	0.505	V
Output Voltage Accuracy @ all load @ all input voltage range	Vfb9	If internal divide mode selected: 0.5V~3.4V by I2C / SPI programmed. Typical is 0.8V.	0.784	0.8	0.816	V

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
		Adjust in Register 0x22, Step=6.25mV				
Load Transient Response L=470nH, Cout=44uF.	Vdrop9	0.3A to 3A, 1A/uS, Vout=0.8V		20		mV
Rated output current	Imax9		3			A
Switching Frequency when CCM mode	Fsw9	Vin-Vout>1.5V		2		MHz
Conversion Efficiency (Vin=4.2V,Vout=0.8V)		Iout=3A Iout=1A Iout=0.25A		65 82 81		%
BUCK10: Fast load transient response step-down converter						
Input supply voltage range	Vcc10		2.7		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vfb10	0.5V~3.4V by I2C / SPI programmed. Typical is 0.8V. Adjust in Register 0x23, Step=6.25mV	0.792	0.8	0.808	V
Load Transient Response L=470nH, Cout=44uF.	Vdrop10	0.3A to 3A, 0.5A/uS, Vout=0.8V		22		mV
Rated output current	Imax10		3			A
Switching Frequency when CCM mode	Fsw10	Vin-Vout>1.5V		2		MHz
Conversion Efficiency (Vin=4.2V,Vout=0.8V)		Iout=3A Iout=1A Iout=0.25A		65 82 81		%
NLDO1						
Input supply voltage range	Vcc13		0.6		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vnldo1	0.5V~3.4V by I2C / SPI programmed. Typical is 1V. Adjust in Register 0x43, Step=12.5mV	0.99	1	1.01	V
Rated output current	Imaxl1	Vcc13-Vnldo1>0.2V	300			mA
PSRR@ 1KHz		Vin rms=200mV		65		dB
PSRR@ 10KHz		Vin rms=200mV		60		dB
NLDO2						
Input supply voltage range	Vcc13		0.6		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vnldo2	0.5V~3.4V by I2C SPI programmed. Typical is 1.8V. Adjust in Register 0x44, Step=12.5mV	0.99	1	1.01	V
Rated output current	Imaxl2	Vcc13-Vnldo2>0.2V	300			mA
PSRR@ 1KHz		Vin rms=200mV		65		dB
PSRR@ 10KHz		Vin rms=200mV		60		dB
NLDO3						
Input supply voltage range	Vcc13		0.6		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vnldo3	0.5V~3.4V by I2C /SPI programmed. Typical is 1V. Adjust in Register 0x45, Step=12.5mV	0.99	1	1.01	V
Rated output current	Imaxl3	Vcc13-Vnldo3>0.2V	500			mA
PSRR@ 1KHz		Vin rms=200mV		65		dB
PSRR@ 10KHz		Vin rms=200mV		60		dB
NLDO4						
Input supply voltage range	Vcc14		0.6		5.5	V

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
Output Voltage Accuracy @ all load @ all input voltage range	Vnldo4	0.5V~3.4V by I2C /SPI programmed. Typical is 1V. Adjust in Register 0x46, Step=12.5mV	0.99	1	1.01	V
Rated output current	Imaxl4	Vcc14-Vnldo4>0.2V	500			mA
PSRR@ 1KHz		Vin rms=200mV		65		dB
PSRR@ 10KHz		Vin rms=200mV		60		dB
NLDO5						
Input supply voltage range	Vcc14		0.6		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vnldo5	0.5V~3.4V by I2C /SPI programmed. Typical is 3V. Adjust in Register 0x47, Step=12.5mV	0.99	1	1.01	V
Rated output current	Imaxl5	Vcc14-Vnldo5>0.2V	300			mA
PSRR@ 1KHz		Vin rms=200mV		65		dB
PSRR@ 10KHz		Vin rms=200mV		60		dB
PLDO1						
Input supply voltage range	Vcc11		2		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vpldo1	0.5V~3.4V by I2C /SPI programmed. Typical is 3V. Adjust in Register 0x4E, Step=12.5mV	0.99	1	1.01	V
Rated output current	Imaxl1	Vcc11-Vpldo1>0.2V	500			mA
PSRR@ 1KHz		Vin rms=200mV		65		dB
PSRR@ 10KHz		Vin rms=200mV		60		dB
PLDO2						
Input supply voltage range	Vcc11		2		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vpldo2	0.5V~3.4V by I2C /SPI programmed. Typical is 2.8V. Adjust in Register 0x4F, Step=12.5mV	0.99	1	1.01	V
Rated output current	Imaxl2	Vcc11-Vpldo2>0.2V	300			mA
PSRR@ 1KHz		Vin rms=200mV		65		dB
PSRR@ 10KHz		Vin rms=200mV		60		dB
PLDO3						
Input supply voltage range	Vcc11		2		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vpldo3	0.5V~3.4V by I2C /SPI programmed. Typical is 1.8V. Adjust in Register 0x50, Step=12.5mV	0.99	1	1.01	V
Rated output current	Imaxl3	Vcc11-Vpldo3>0.2V	300			mA
PSRR@ 1KHz		Vin rms=200mV		65		dB
PSRR@ 10KHz		Vin rms=200mV		60		dB
PLDO4						
Input supply voltage range	Vcc12		2		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vpldo4	0.5V~3.4V by I2C /SPI programmed. Typical is 1.5V. Adjust in Register 0x51, Step=12.5mV	0.99	1	1.01	V
Rated output current	Imaxl4	Vcc12-Vpldo3>0.2V	500			mA
PSRR@ 1KHz		Vin rms=200mV		65		dB
PSRR@ 10KHz		Vin rms=200mV		60		dB
PLDO5						
Input supply voltage range	Vcc12		2		5.5	V

PARAMETERS	SYMBOL	Note	MIN	TYP	MAX	UNIT
Output Voltage Accuracy @ all load @ all input voltage range	Vpldo5	0.5V~3.4V by I2C /SPI programmed. Typical is 1.8V. Adjust in Register 0x52, Step=12.5mV	0.99	1	1.01	V
Rated output current	Imaxl5	Vcc12-Vpldo3>0.2V	300			mA
PSRR@ 1KHz		Vin rms=200mV		65		dB
PSRR@ 10KHz		Vin rms=200mV		60		dB
VCCIO						
Input supply voltage range[1]	VccA		2		5.5	V
Output Voltage Accuracy @ all load @ all input voltage range	Vccio	0.5V~3.4V by I2C /SPI programmed. Typical is 1.8V. Adjust in Register 0x53, Step=12.5mV	1.782	1.8	1.818	V
Rated output current	Imaxl6	VccA-Vccio>0.2V	300			mA
PSRR@ 1KHz		Vin rms=200mV		65		dB
PSRR@ 10KHz		Vin rms=200mV		60		dB

Note:

[1] VCCA is the analog power supply which needs to be greater than or equal to VCC1~VCC14.

Chapter 4 Function Description

4.1 Top State Machine

4.1.1 State Machine Description

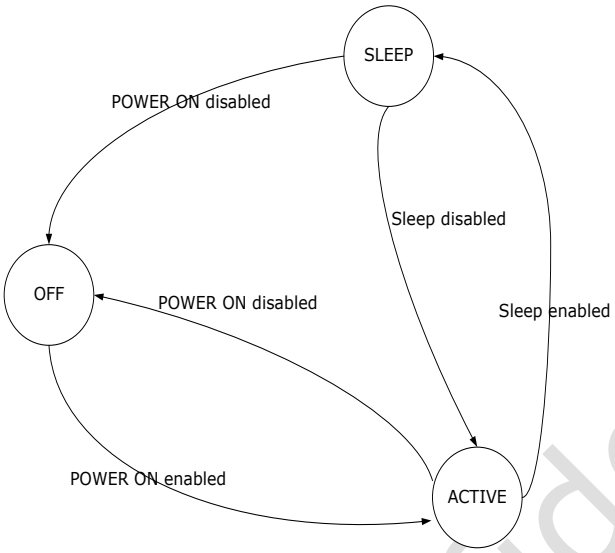


Fig. 4-1 State Machine

The RK806 state machine shown as above. The state shift by "power on", "power down", "reset", "active to sleep" and "sleep to active".

4.1.2 Power on Description

There are three kinds of method to power on the PMIC.

1. Press "PWRON" key

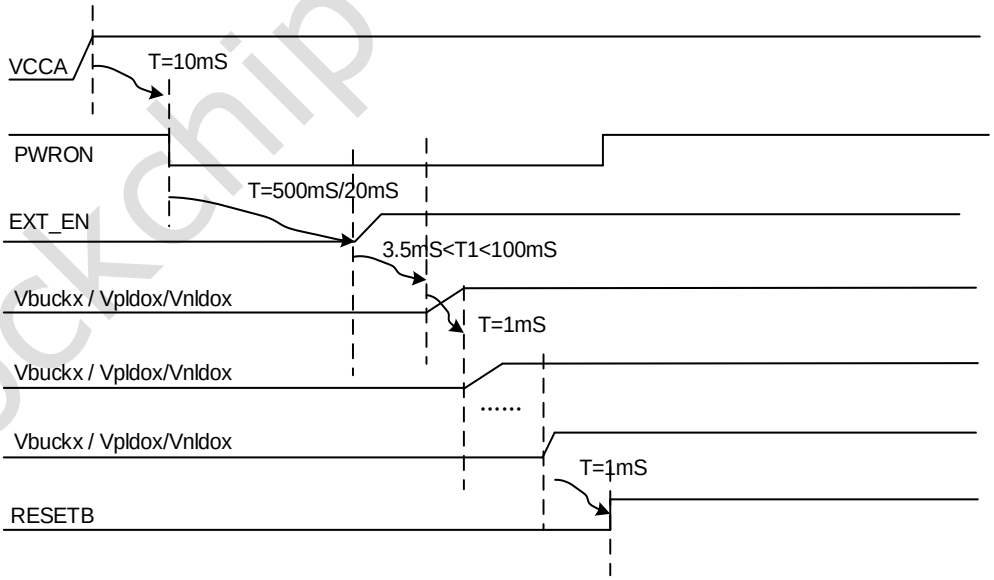


Fig. 4-2 Press "PWRON" key to turn on the PMIC

When the PMIC VCCA,VCC1,VCC2 voltage is higher than "VB_OK" threshold, keeping low level at "PWRON" pin for 500/20mS would turn on the PMIC. The "PWRON" pin de-bounce time (500mS/20mS) can be adjusted by I2C or SPI.

All the power channels start up at the default output voltages with a preset power up sequence, which has 1mS intervals between the channels. When the power up process is

done, the RESETB turns to high logic level to inform the processor that all the power rails are up and stable.

Note:T1 is used to Check whether the external power supply meets requirements. If the requirements are met within 100mS, the system can start normally.

2. VDC HIGH LEVEL

When the PMIC VCCA,VCC1,VCC2 voltage is higher than "VB_OK" threshold, And the high level continues to exceed 2mS for VDC , the PMIC would be turn on.

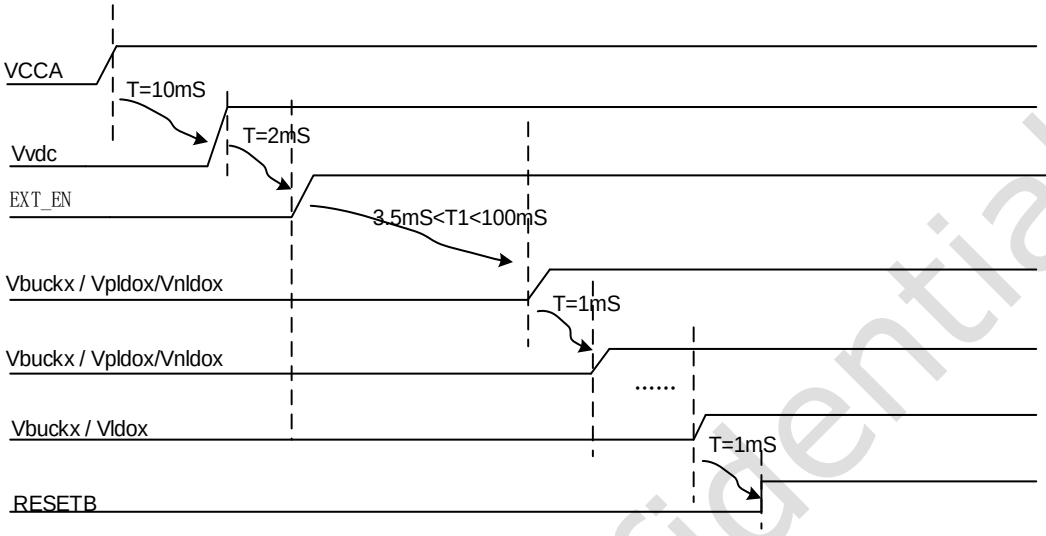


Fig. 4-3 VDC high level to turn on the PMIC

Note:T1 is used to Check whether the external power supply meets requirements. If the requirements are met within 100mS, the system can start normally.

3. ABNORMAL ON

When the PMIC turns on and register bit 0x5F<7>="0", and if the PMIC triggers OVP or UVLO, the system would restart automatically. After the system voltage is detected to be normal during the restart, the system can be turn on normally.

4.1.3 Power down Description

There are 7 kinds of method to power down the PMIC.

1. Long press "PWRON" key

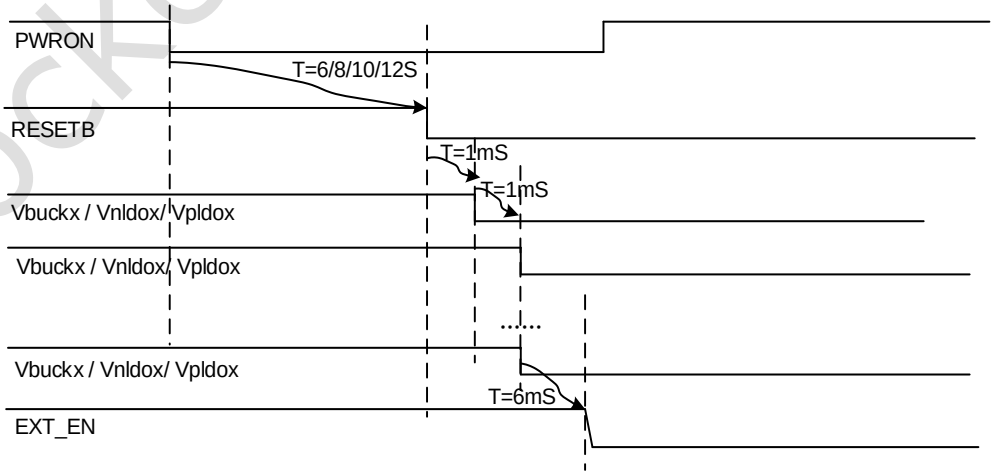


Fig. 4-4 Long press "PWRON" key to turn off the PMIC

When the PMIC work in the "ON" state or "SLEEP" state, writing register bit 0x76<6>="0", and then keeping low level at "PWRON" pin for 6/8/10/12S would turn off the PMIC. The "PWRON" pin de-bounce time (6/8/10/12S) can be adjusted by I2C.

When the PMIC power down, The RESETB pin would be pulled low to reset the processor. After 1ms de-bounce time, the power channels start to be turned off as the set of power off sequence.

2. Write shutdown Register

When the PMIC work in the "ON" state or "SLEEP" state, writing register bit 0x72<0>="1" would turn off the PMIC. The power off sequence is the same with the first one.

3. SYNC PULL DOWN

When the PMIC work in the "ON" state or "SLEEP" state and register bit 0x5F<7>="1", if VCCA or VCC1 or VCC2 lower than VB_UV threshold (typical 2.7V) or higher than VB_OV threshold (typical 6.0V), SYNC will pull down, and the PMIC would be turn off immediately.

4. SYS low-voltage

When the PMIC work in the "ON" state or "SLEEP" state and register bit 0x5E<3>="0", if VCCA or VCC1 or VCC2 lower than VB_LO threshold (typical 3.2V) for 1mS, the PMIC would be turn off. The power off sequence is the same with the first one.

5. PWRCTRL pin active

When the PMIC work in the "ON" state or "SLEEP" state, if PWRCTRLn_FUN set "010", and PWRCTRLn pin active (the polarity can be programmed by Register), the PMIC would be turn off. The power off sequence is the same with the first one.

6. TSD protection

When the PMIC work in the "ON" state or "SLEEP" state, if the temperature is higher than TSD threshold (typical 140 degree), the PMIC would be turn off. The power off sequence is the same with the first one.

7. ABNORMAL

When the PMIC work in the "ON" state or "SLEEP" state and register bit 0x5F<7>="0", if VCCA or VCC1 or VCC2 lower than VB_UV threshold (typical 2.7V) or higher than VB_OV threshold (typical 6.0V), the PMIC would be turn off immediately. The power off sequence is the same with the first one.

4.1.4 Reset Description

There are 4 kinds of method to reset the PMIC. If register bits 0x72<7:6>="00", reset function means restart PMIC. If register bits 0x72<7:6>="01", reset function means reset registers, all channels of power would be reset to default state.

1. Long press "PWRON" key

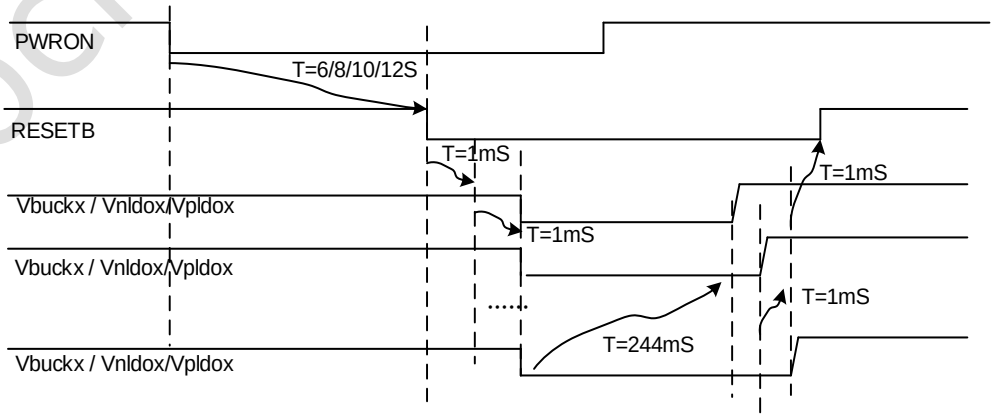


Fig. 4-5 Long press "PWRON" key to restart the PMIC

When the PMIC work in the "ON" state or "SLEEP" state, Writing register bit

0x76<6>="1", and then keeping low level at "PWRON" pin for 6/8/10/12S would restart the PMIC. The "PWRON" pin de-bounce time (6/8/10/12S) can be adjusted by I2C or SPI.

2. PWRCTRLn pin active

When the PMIC work in the "ON" state or "SLEEP" state, if PWRCTRLn_FUN set "011", and "PWRCTRLn" pin active (the polarity can be programmed by Register of PWRCTRLn_POL), the PMIC would restart. The restart sequence is the same with the first one.

3. RESETB pin pull low

When the PMIC work in the "ON" state or "SLEEP" state, if "RESETB" pin is pull down, the PMIC would restart immediately. The restart sequence is the same with the first one.

4. WDT active

When the PMIC work in the "ON" state or "SLEEP" state, if register bit 0x73<4:3>="11", the PMIC would restart. The restart sequence is the same with the first one.

5. **Write Reset Register**

When the PMIC work in the "ON" state or "SLEEP" state, writing register bit 0x72<7:5>="001" would restart the PMIC. The restart sequence is the same with the first one.

4.1.5 Power Sequence Description

			RK806-1 (master)	
	Range of output voltage	Maximum output current	Default voltage[1]	Start up sequence
BUCK1	0.5V-3.4V	6.5A	0.75V	5
BUCK2	0.5V-3.4V	5A	0.75V	3
BUCK3	0.5V-3.4V	5A	0.75V	2
BUCK4	0.5V-3.4V	5A	0.75V	5
BUCK5	0.5V-3.4V	3A	0.85V	2
BUCK6	X(external divided resistor) Or 0.5V-3.4v(internal divided resistor)	3A	0.5V	4
BUCK7	0.5V-3.4V	3A	2.0V	1
BUCK8	0.5V-3.4V	3A	3.3V	6
BUCK9	X(external divided resistor) Or 0.5V-3.4v(internal divided resistor)	3A	0.5V	6
BUCK10	0.5V-3.4V	3A	1.8V	3
NLDO1	0.5V-3.4V	300mA	0.75V	2
NLDO2	0.5V-3.4V	300mA	0.85V	2
NLDO3	0.5V-3.4V	500mA	0.75V	2
NLDO4	0.5V-3.4V	500mA	0.85V	2
NLDO5	0.5V-3.4V	300mA	0.75V	2

PLDO1	0.5V-3.4V	500mA	1.8V	3
PLDO2	0.5V-3.4V	300mA	1.8V	3
PLDO3	0.5V-3.4V	300mA	1.2V	4
PLDO4	0.5V-3.4V	500mA	3.3V	6
PLDO5	0.5V-3.4V	300mA	3.3V	6
PLDO6	0.5V-3.4V	300mA	1.8V	3
VB_OK	2.8V-3.6V	x	2.8V	x
RESETB	x	x	x	11

Table 4-1 RK806-1 Power up/down sequence (Short press PWRON key time is 20ms.)

			RK806-2 (master)	
	Range of output voltage	Maximum output current	Default voltage[2]	Start up sequence
BUCK1	0.5V-3.4V	6.5A	0.75V	7
BUCK2	0.5V-3.4V	5A	0.75V	7
BUCK3	0.5V-3.4V	5A	0.75V	2
BUCK4	0.5V-3.4V	5A	0.75V	7
BUCK5	0.5V-3.4V	3A	0.75V	7
BUCK6	0.5V-3.4V	3A	0.75V	7
BUCK7	0.5V-3.4V	3A	2.0V	1
BUCK8	0.5V-3.4V	3A	0.75V	7
BUCK9	X(external divided resistor) Or 0.5V-3.4v(internal divided resistor)	3A	0.5V	4
BUCK10	0.5V-3.4V	3A	1.10V	1
NLDO1	0.5V-3.4V	300mA	0.75V	2
NLDO2	0.5V-3.4V	300mA	0.90V	5
NLDO3	0.5V-3.4V	500mA	0.75V	2
NLDO4	0.5V-3.4V	500mA	0.75V	2
NLDO5	0.5V-3.4V	300mA	0.85V	2
PLDO1	0.5V-3.4V	500mA	1.80V	3
PLDO2	0.5V-3.4V	300mA	1.80V	3
PLDO3	0.5V-3.4V	300mA	1.80V	3
PLDO4	0.5V-3.4V	500mA	3.30V	6
PLDO5	0.5V-3.4V	300mA	3.30V	6
PLDO6	0.5V-3.4V	300mA	1.80V	3
VB_OK	2.8V-3.6V	x	2.8V	x
RESETB	x	x	x	18

			RK806-2 (slave)	
	Range of output voltage	Maximum output current	Default voltage[3]	Start up sequence
BUCK1	0.5V-3.4V	6.5A	0.75V	9
BUCK2	0.5V-3.4V	5A	0.75V	9
BUCK3	0.5V-3.4V	5A	0.75V	8
BUCK4	0.5V-3.4V	5A	3.30V	6
BUCK5	0.5V-3.4V	3A	0.75V	9
BUCK6	0.5V-3.4V	3A	0.75V	9
BUCK7	0.5V-3.4V	3A	1.80V	3
BUCK8	0.5V-3.4V	3A	0.75V	8
BUCK9	X(external divided resistor) Or 0.5V-3.4v(internal divided resistor)	3A	0.5V	6
BUCK10	0.5V-3.4V	3A	0.85V	2
NLDO1	0.5V-3.4V	300mA	0.75V	2
NLDO2	0.5V-3.4V	300mA	0.85V	2
NLDO3	0.5V-3.4V	500mA	0.85V	2
NLDO4	0.5V-3.4V	500mA	0.50V	OFF
NLDO5	0.5V-3.4V	300mA	1.20V	4
PLDO1	0.5V-3.4V	500mA	0.50V	OFF
PLDO2	0.5V-3.4V	300mA	1.80V	3
PLDO3	0.5V-3.4V	300mA	1.80V	3
PLDO4	0.5V-3.4V	500mA	3.30V	6
PLDO5	0.5V-3.4V	300mA	2.80V	OFF
PLDO6	0.5V-3.4V	300mA	1.80V	3
VB_OK	2.8V-3.6V	x	2.8V	x
RESETB	x	x	x	18

Table 4-2 RK806-2 Power up/down sequence (Short press PWRON key time is 20ms.)

Note:

[1][2][3] Default output voltage supports any voltage at the range of the 0.5V~3.4V, also start up sequence can be changed by OTP. Channel BUCK1, BUCK2, BUCK5, BUCK6, BUCK9 can also be configured for customized values by using external feedback resistors.

After PMIC turns on, we can set power down sequence through register (B2~C3).

4.1.6 Sleep Description

The RK806 could be set to SLEEP mode, The register of PWRCTRLn_FUN set "001", and then "PWRCTRLn" pin active (the polarity can be programmed by Register of

PWRCTRLn_POL)

When sleep mode, the power dissipation of RK806 would be decreased. Writing register bits 0x0D=”FF”, 0x0C=” FF”, 0x61<1>=”1” would be decrease quiescent current further.

4.1.7 Master and Slave work together

Two RK806 could work together that one of them is master, another is slave. Master/Slave chip configurations are distinguished by the level state of pin EXT_EN when first powered on, EXT_EN connect with VCCA is slave chip, floating or pulled down by a resistor is the master chip.

When two RK806 work together the SYNC_CLK and SYNC pin of master and slave must be connected. The master chip provides clock to slave chip through SYNC_CLK, and SYNC is used to provide synchronization signal and generate synchronization pulse to realize the synchronization of startup, shutdown, reset and power-on and power-off.

The two signal pins PWRON and RESETB of the master and slave shall be connected separately used to power on of PMIC and reset signal input generated by the external reset button.

The signal pin VDC of the master and slave can be connected, and also connect the VDC of slave with the EXT_EN of master.

If the number of IO of the master is not enough, the master and slave INT pins can also be connected. The software can distinguish the master and slave registers by reading them.

4.1.8 I2C and SPI communication

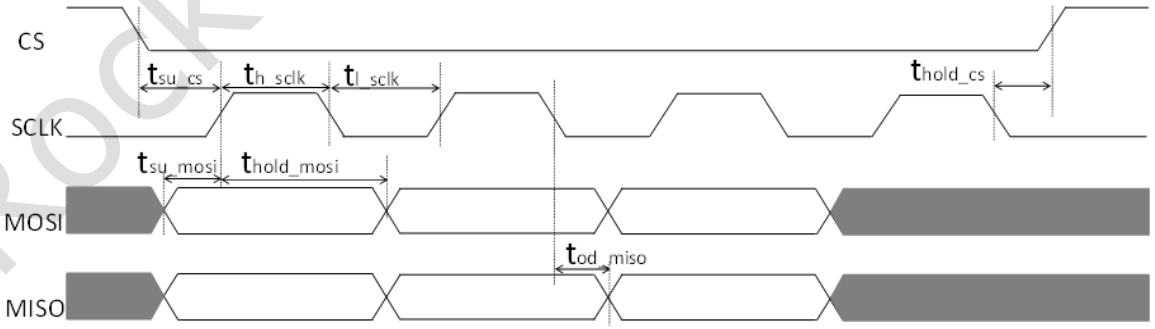
RK806 can be used as an extended PMIC, master - slave control. The register address of the master is 0X23, the register address of the slave is 0X25. RK806 also have SPI/I2C communication mode, when first turned on, if CS pin is connected to the VCCA, RK806 automatically selects the communication mode of I2C,else RK806 automatically selects the communication mode of SPI. The voltage of VCCIO must greater than 1.62V, do not close this channel in standby mode.

If we select SPI mode, SPI defaults to 3-line mode. To enable 4-line mode, when the host initializes, set register E8<2>=”1”, in 4-wire mode, the pin of SO for slave must be configured E9<5>=”1”.CLK falling edge to prepare data, CLK high level latch data. The maximum rate of communication is 20MHz.

In SPI mode, the pin of MISO can be reuse SLEEP3 function, when this pin used to SLEEP3 function, SPI only select 3-line mode, and the pins of MOSI and MISO for master chip should connect together, the data of input and output transfer from the pin of MOSI of PMIC.

In SPI mode, after sending data, you need to send two more bytes of dummy empty packets.

SPI communication must also meet the following conditions:



Test Item	Reference	Spec limited			Unit
		Min	Tpical	Max	

CLK	F_{sclk}	Clock Frequency	-	-	20	MHz
	t_{h_sclk}	Clock High Time	5	25	-	ns
	t_{l_sclk}	Clock Low Time	5	25	-	ns
CS	t_{su_cs}	CS In Setup Time	10	-	-	ns
	t_{hold_cs}	CS In Hold Time	20	-	-	ns
MOSI	t_{su_mosi}	Data In Setup Time	2	-	-	ns
	t_{hold_mosi}	Data In Hold Time	2	-	-	ns
MISO	t_{od_miso}	Clock Low To Output Valid	-	20	23	ns

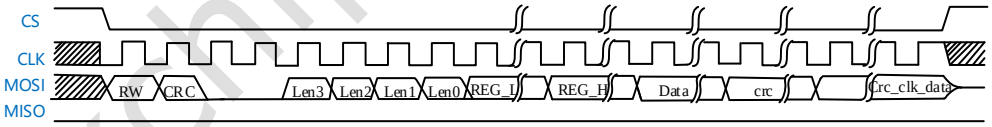
4.1.9 Format of SPI commands

1, Every time when the host computer starts transmission, the following 3 data packages will be transmitted: CMD, REG_L and REG_H.

2, When the data is written or read with CRC, the Len position of CMD has to be specified with the length of data 'n'. (Len=n-1, the maximum of the length of data is 16Byte.)

3, The polynomial of CRC is X8+X4+X+1, and the initial value of CRC is 0. Under the circumstance of the computation of CRC, REG_L=REG_H=0 and data will be engaged in the computation.

4, When the data is written with CRC, another empty package 'CRC_CLK_DATA' will be transmitted after finishing writing CRC code. The CLK is used to transport data from the inner computer. (Reading data with CRC does not need this operation.)



The Format of Commands of CMD package is described as following:

- R/W[7]: R=0, W=1
- CRC_EN[6]: Enable=1, Disable=0
- Len[3:0]: case 1: CRC_EN=1
  The length of data written or read is noted in Len[3:0].
  The host or slave computer transmits CRC data at the position of len+1.
  case 2: CRC_EN=0
  The data transmission takes no advantage of the length.
  The addresses of registers of slave computer self-increase within the interval of 0~255.
- REG_L[7:0]: The address of the target register is low-8 bit.
- REG_H[15:8]: The address of the target register is high-8 bit. (RK806 does not comprehend this address and recognizes it as 0 forever. The host computer will set MO as input in this Byte in 3-thread-read mode. The aim of adding REG_H is preventing SI of the

slave computer switching to SO in 3-thread mode from engendering conflict with the MO signal.)

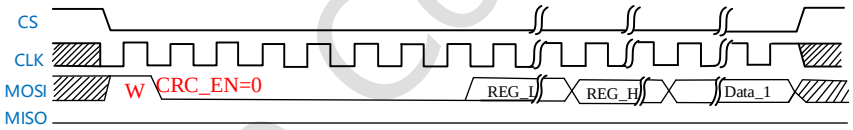
- Writing data when CRC_EN=1: Len equals the length of data minus 1. An extra 1 Byte empty package has to be written after the CRC code when data writing. This package is used as a CLK for computation and data transmission of RK806 chips. If there is still CLK not comprehended by slave computer after 8 bit, CRC will be set as error, RK806 will terminate working and simultaneously registers will show 'CRC_ERR'.
- Reading data when CRC_EN=1: The slave computer will return CRC code after the length that Len indicates. If there is CLK after CRC code, the slave computer will show no response or return invalid data.

The Format of CRC is described as following:
The polynomial of CRC is X8+X4+X+1.
The initial value of CRC is 0x00.
The CRC computation embraces REG_L, REG_H and data.

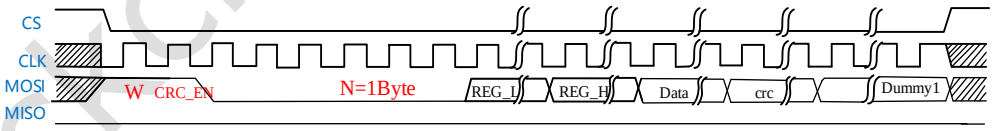
Note: When reading data in 3-thread mode, the host computer will switch to input when REG_H is reading. Because both host and slave computer are input mode so the slave one have to force the data to be set as 0.

Read and write waveforms are as follows:

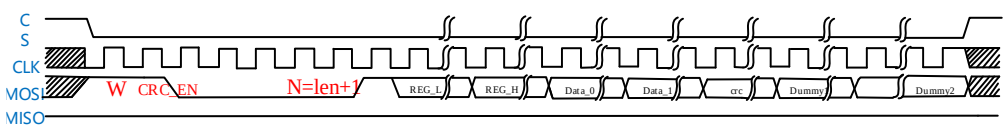
Single byte without CRC write waveform : (Regardless of the length of Len, the address automatically increments by 1 after 8 CLK)



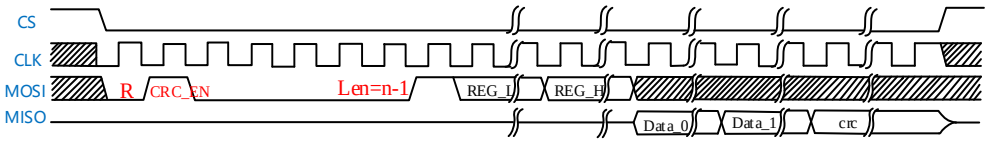
Single byte with CRC write waveform:



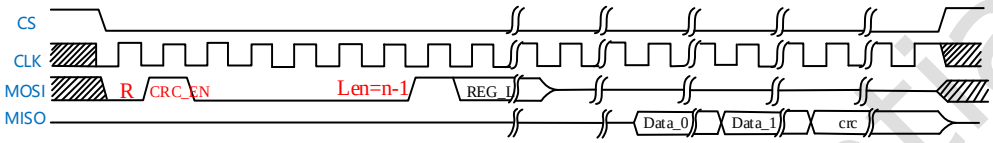
Multi-byte with CRC write waveform: (If data is smaller than or equal to 8 byte, send at least one packet. If data is larger than 8 byte, send two packets)



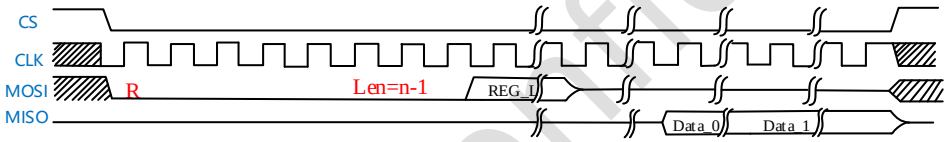
Multi-byte 4-line with CRC read :



Multi-byte 3-line with CRC read :(The position where the master reads empty packets and the slave forcibly receives data for 0)



Read without CRC :(The slave register address is automatically incremented by 1 after 8 CLK)



4.2 Power Channels

4.2.1 Buck Description

The RK806 provides ten high current synchronous buck converters, which deliver up to 6.5A, 5A and 3A, respectively. An enhanced COT architecture is used, which improves the transient response significantly. 2MHz switching frequency and good control method de5crease the external inductance and capacitance. All output voltages can be adjusted dynamically during operation through DVS (Dynamic Voltage Scaling), which guarantees a linear and gradual voltage ramping up and down. A complete set of protection functions, such as short circuit protection, is implemented in the buck converters too.

For example, the BUCK1: Vout=0.8V, Vin=5V, L=0.22uH, Cout=66uF. Load Current transient from 0.065A to 6.5A, the current slew rate is 3A/uS (using MOSFET transition). The output voltage drops when load current rising edge is about **38mV**, that is very good characteristics. The other bucks have the same architecture with BUCK1, so they have the same load transient response characteristics.

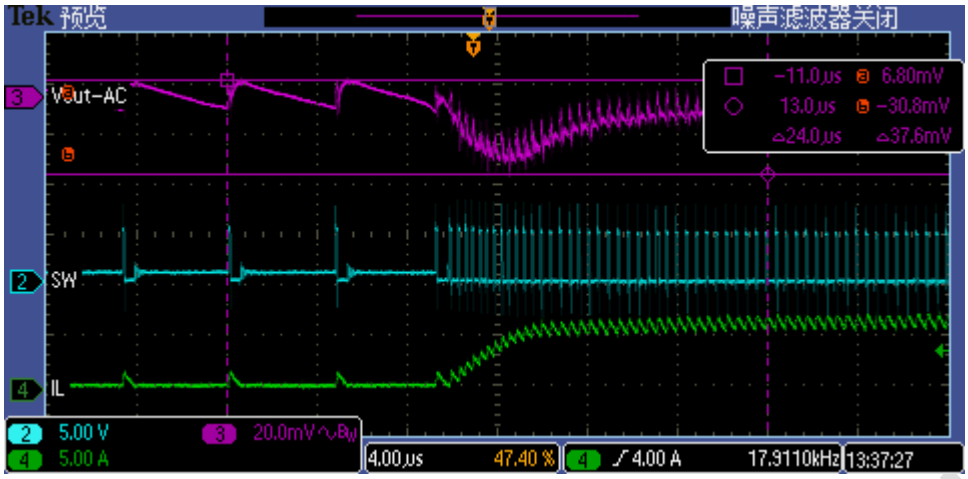


Fig. 4-6 BUCK1 load transient rising edge

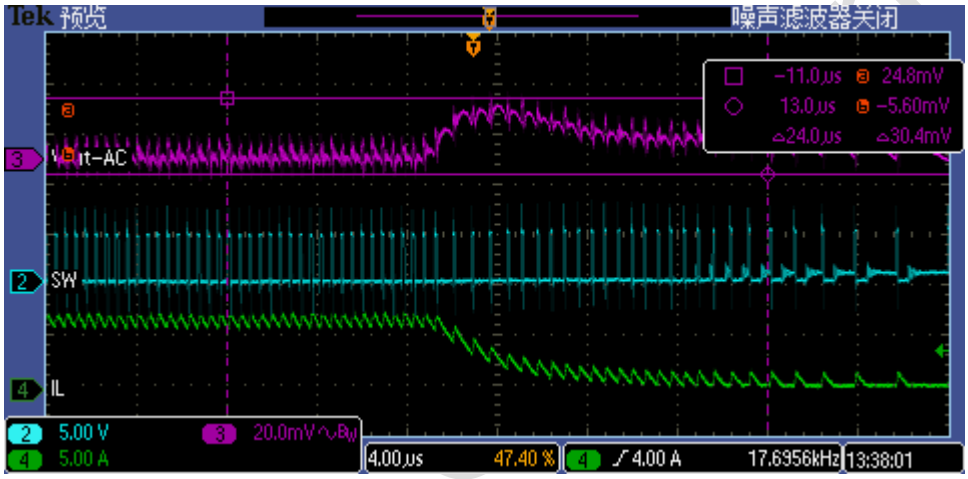


Fig. 4-7 BUCK1 load transient falling edge

Meanwhile, bucks converters have good efficiency characteristics. The test data is shown as below. All channels of buck output voltage set to default.

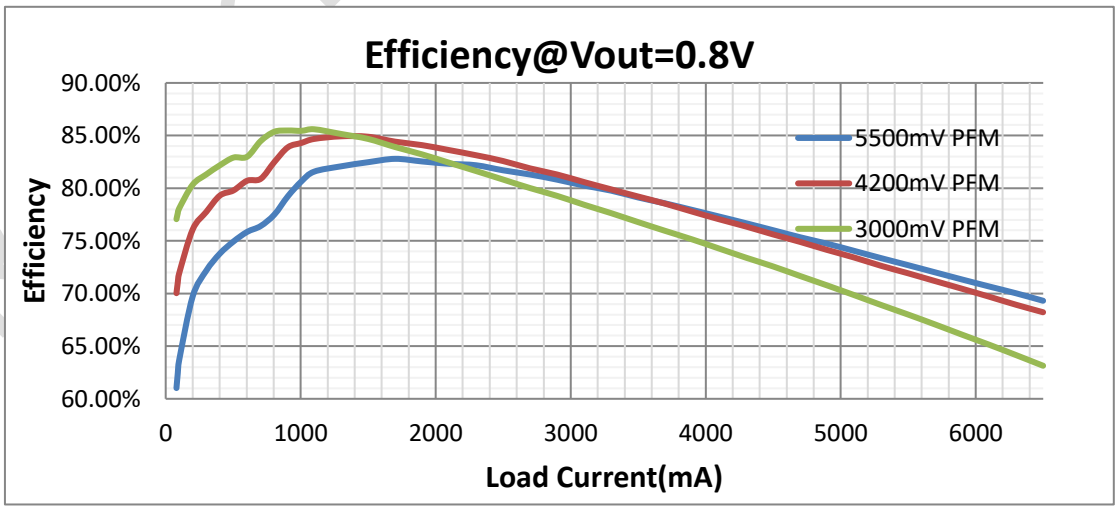


Fig. 4-8 BUCK1 efficiency curve when different input voltage

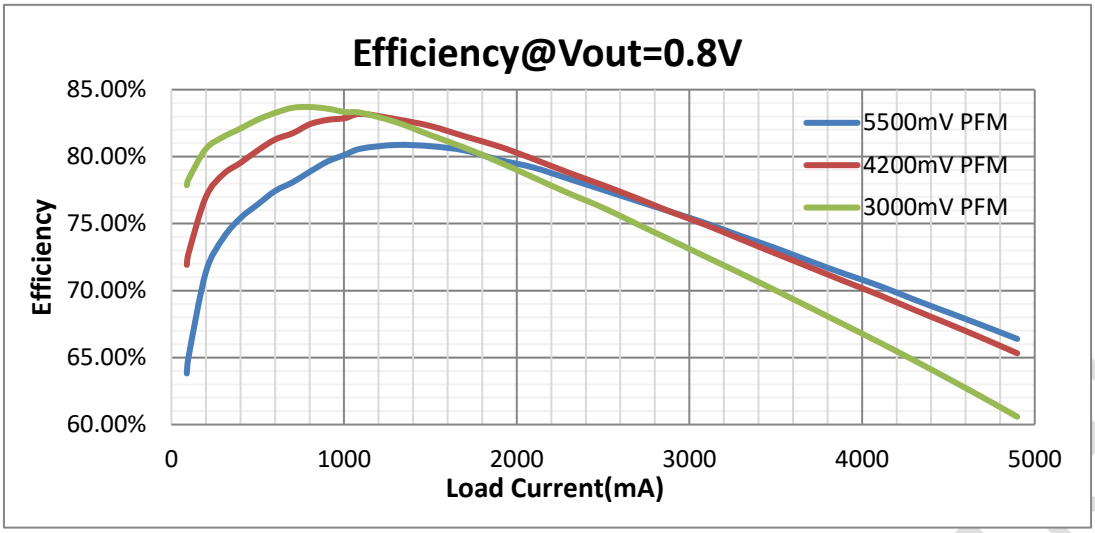


Fig. 4-9 BUCK2 efficiency curve when different input voltage

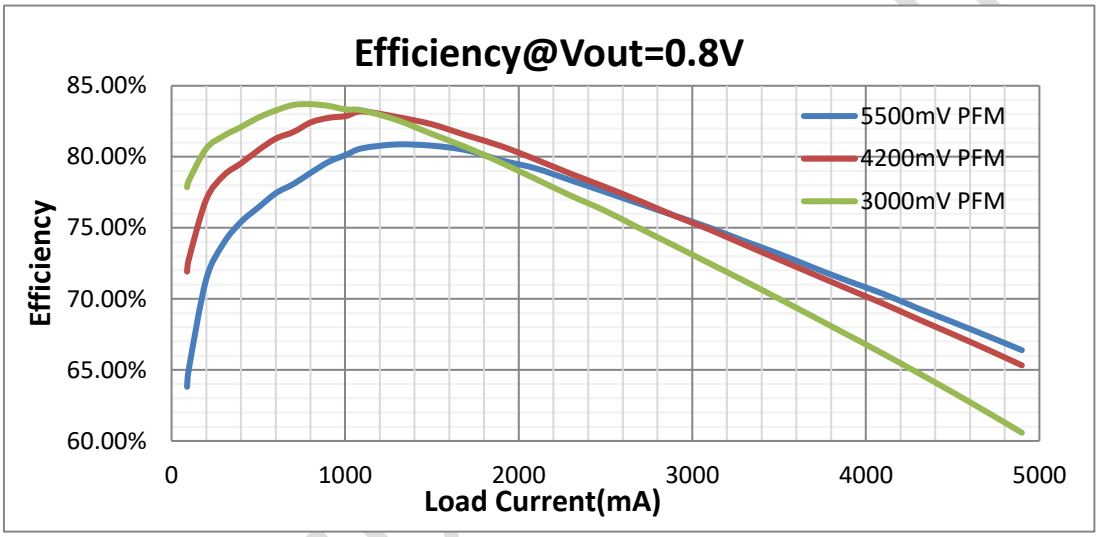


Fig. 4-10 BUCK3 efficiency curve when different input voltage

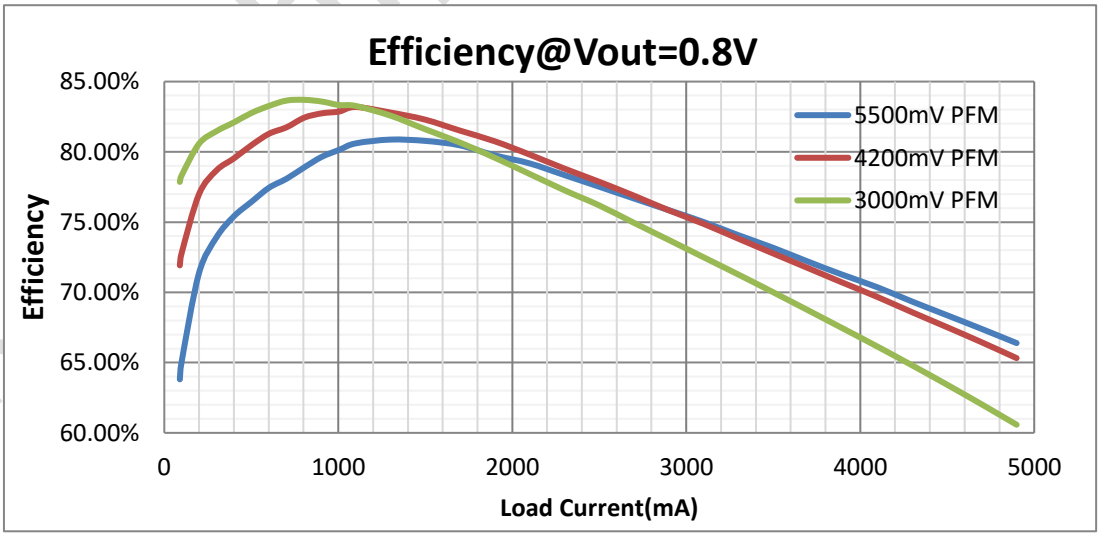


Fig. 4-11 BUCK4 efficiency curve when different input voltage

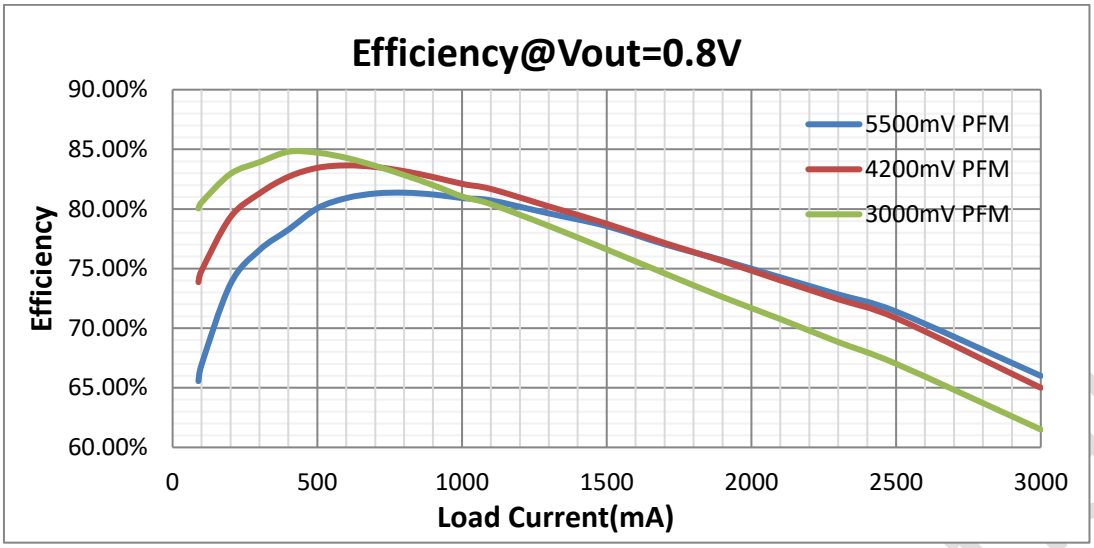


Fig. 4-12 BUCK5 efficiency curve when different input voltage

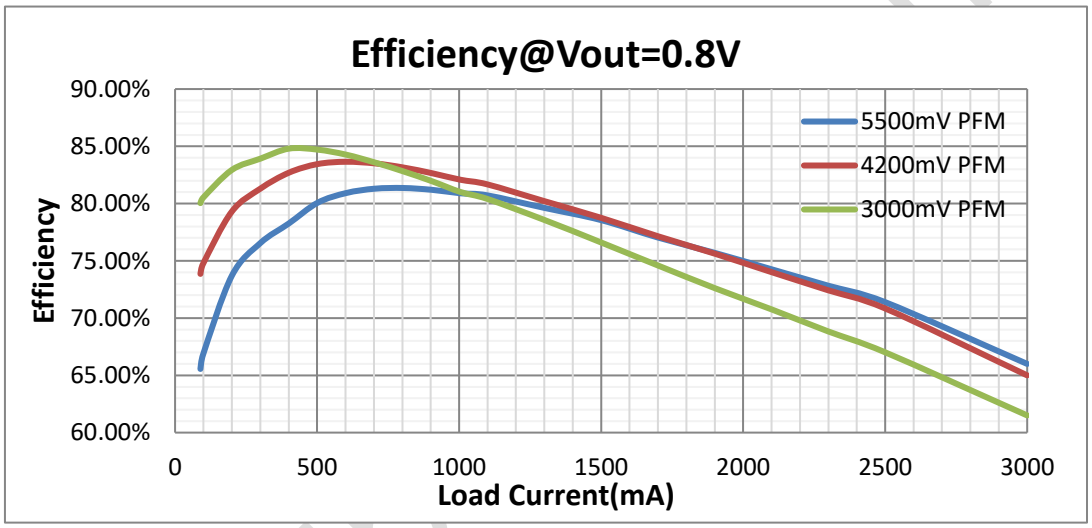


Fig. 4-13 BUCK6 efficiency curve when different input voltage

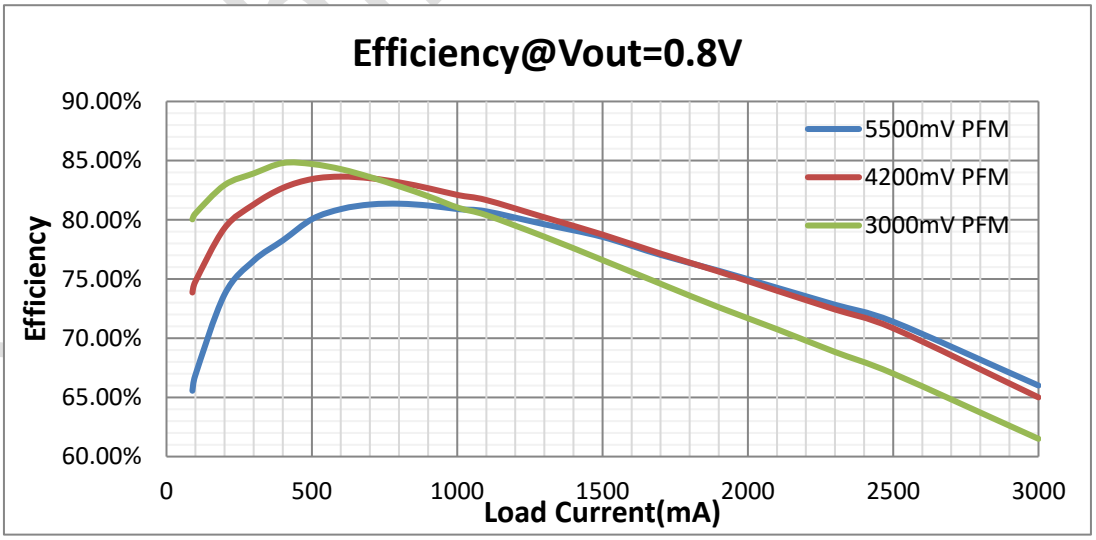


Fig. 4-14 BUCK7 efficiency curve when different input voltage

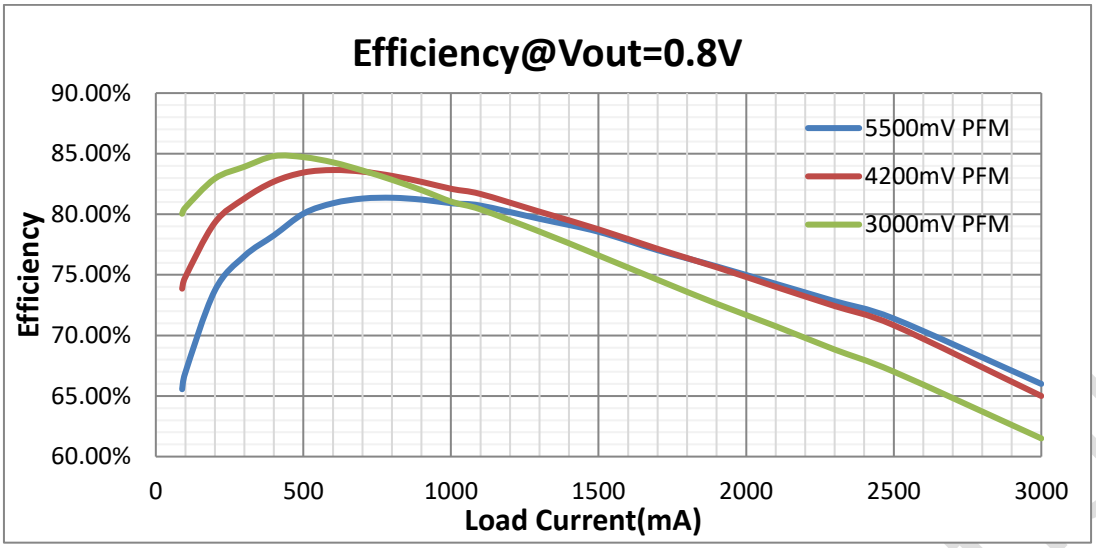


Fig. 4-15 BUCK8 efficiency curve when different input voltage

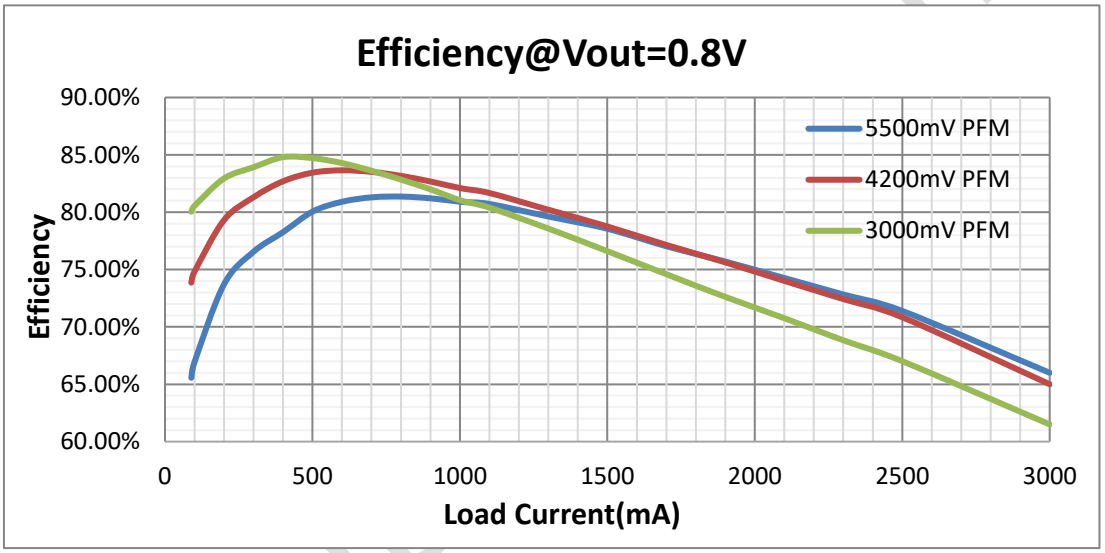


Fig. 4-16 BUCK9 efficiency curve when different input voltage

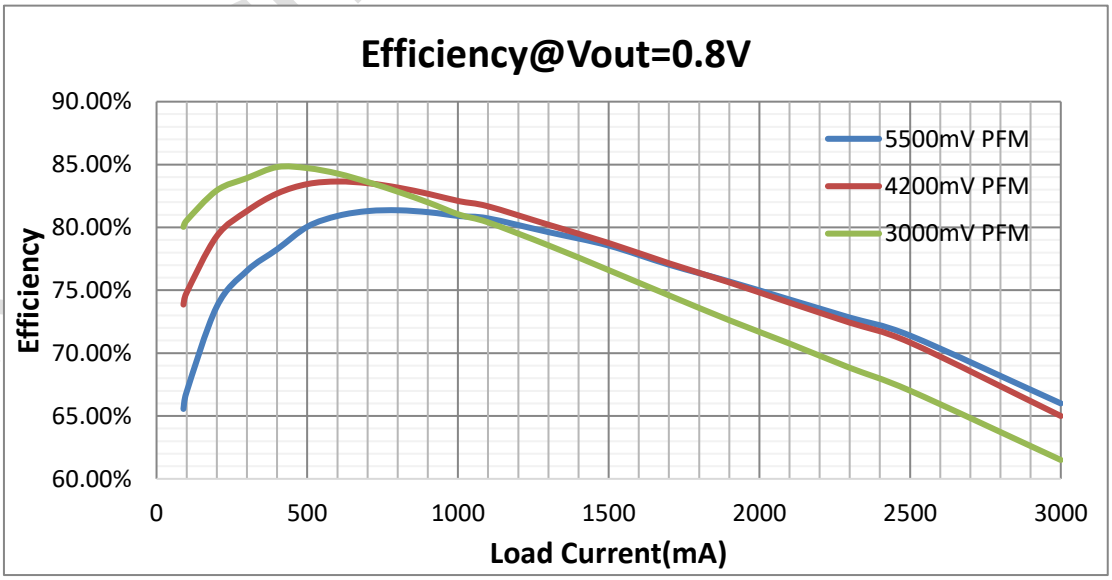


Fig. 4-17 BUCK10 efficiency curve when different input voltage

4.2.2 LDO Description

The RK806 also integrates five NLDOs, with 2 NLDOs (NLDO3, NLDO4) capable of providing up to 500mA and 3 (NLDO1, NLDO2, NLDO5) providing maximum 300mA. And also integrates six PLDOs, with 2 PLDOs (PLDO1, PLDO4) capable of providing up to 500mA and 3 (PLDO2, PLDO3, VCCIO) providing maximum 300mA. All channels of LDO output capacitance could be 1.0uF that decreases the system cost. The parameters such as output voltage in the different operating modes can be adjusted through the I^2C or SPI interface.

Chapter 5 Register Description

5.1 Register Summary

Name	Offset	Size	Reset Value	Description
POWER_EN0	0x0000	B	OTP	
POWER_EN1	0x0001	B	OTP	
POWER_EN2	0x0002	B	OTP	
POWER_EN3	0x0003	B	OTP	
POWER_EN4	0x0004	B	OTP	
POWER_EN5	0x0005	B	OTP	
POWER_SLP_EN0	0x0006	B	OTP	
POWER_SLP_EN1	0x0007	B	OTP	
POWER_SLP_EN2	0x0008	B	OTP	
POWER_DISCHRG_EN0	0x0009	B	0xff	
POWER_DISCHRG_EN1	0x000a	B	0xdf	
POWER_DISCHRG_EN2	0x000b	B	0x3f	
BUCK_FB_CONFIG	0x000c	B	0x01	
SLP_LP_CONFIG	0x000d	B	0x00	
POWER_FPWM_EN0	0x000e	B	0x00	
POWER_FPWM_EN1	0x000f	B	0x00	
BUCK1_CONFIG	0x0010	B	0x64	
BUCK2_CONFIG	0x0011	B	0x64	
BUCK3_CONFIG	0x0012	B	0x64	
BUCK4_CONFIG	0x0013	B	0x64	
BUCK5_CONFIG	0x0014	B	0x64	
BUCK6_CONFIG	0x0015	B	0x64	
BUCK7_CONFIG	0x0016	B	0x64	
BUCK8_CONFIG	0x0017	B	0x64	
BUCK9_CONFIG	0x0018	B	0x64	
BUCK10_CONFIG	0x0019	B	0x64	
BUCK1_ON_VSEL	0x001a	B	OTP	
BUCK2_ON_VSEL	0x001b	B	OTP	
BUCK3_ON_VSEL	0x001c	B	OTP	
BUCK4_ON_VSEL	0x001d	B	OTP	
BUCK5_ON_VSEL	0x001e	B	OTP	
BUCK6_ON_VSEL	0x001f	B	OTP	
BUCK7_ON_VSEL	0x0020	B	OTP	
BUCK8_ON_VSEL	0x0021	B	OTP	
BUCK9_ON_VSEL	0x0022	B	OTP	
BUCK10_ON_VSEL	0x0023	B	OTP	
BUCK1_SLP_VSEL	0x0024	B	OTP	
BUCK2_SLP_VSEL	0x0025	B	OTP	
BUCK3_SLP_VSEL	0x0026	B	OTP	
BUCK4_SLP_VSEL	0x0027	B	OTP	
BUCK5_SLP_VSEL	0x0028	B	OTP	
BUCK6_SLP_VSEL	0x0029	B	OTP	
BUCK7_SLP_VSEL	0x002a	B	OTP	
BUCK8_SLP_VSEL	0x002b	B	OTP	
BUCK9_SLP_VSEL	0x002c	B	OTP	
BUCK10_SLP_VSEL	0x002d	B	OTP	
BUCK_DEBUG13	0x003c	B	0x44	

Name	Offset	Size	Reset Value	Description
BUCK_DEBUG14	0x003d	B	0x44	
BUCK_DEBUG15	0x003e	B	0x44	
BUCK_DEBUG16	0x003f	B	0x44	
BUCK_DEBUG17	0x0040	B	0x44	
NLDO_IMAX	0x0042	B	0x00	
NLDO1_ON_VSEL	0x0043	B	OTP	
NLDO2_ON_VSEL	0x0044	B	OTP	
NLDO3_ON_VSEL	0x0045	B	OTP	
NLDO4_ON_VSEL	0x0046	B	OTP	
NLDO5_ON_VSEL	0x0047	B	OTP	
NLDO1_SLP_VSEL	0x0048	B	OTP	
NLDO2_SLP_VSEL	0x0049	B	OTP	
NLDO3_SLP_VSEL	0x004a	B	OTP	
NLDO4_SLP_VSEL	0x004b	B	OTP	
NLDO5_SLP_VSEL	0x004c	B	OTP	
PLDO_IMAX	0x004d	B	0x00	
PLDO1_ON_VSEL	0x004e	B	OTP	
PLDO2_ON_VSEL	0x004f	B	OTP	
PLDO3_ON_VSEL	0x0050	B	OTP	
PLDO4_ON_VSEL	0x0051	B	OTP	
PLDO5_ON_VSEL	0x0052	B	OTP	
PLDO6_ON_VSEL	0x0053	B	OTP	
PLDO1_SLP_VSEL	0x0054	B	OTP	
PLDO2_SLP_VSEL	0x0055	B	OTP	
PLDO3_SLP_VSEL	0x0056	B	OTP	
PLDO4_SLP_VSEL	0x0057	B	OTP	
PLDO5_SLP_VSEL	0x0058	B	OTP	
PLDO6_SLP_VSEL	0x0059	B	OTP	
CHIP_NAME	0x005a	B	0x80	
CHIP_VER	0x005b	B	0x62	
OTP_VER	0x005c	B	OTP	
SYS_STS	0x005d	B	0x00	
SYS_CFG0	0x005e	B	0x0c	
SYS_CFG1	0x005f	B	0x00	
SYS_OPTION	0x0061	B	0x00	
PWRCTRL_CONFIG0	0x0062	B	0x88	
PWRCTRL_CONFIG1	0x0063	B	0x08	
VSEL_CTR_SEL0	0x0064	B	0x00	
VSEL_CTR_SEL1	0x0065	B	0x00	
VSEL_CTR_SEL2	0x0066	B	0x00	
VSEL_CTR_SEL3	0x0067	B	0x00	
VSEL_CTR_SEL4	0x0068	B	0x00	
VSEL_CTR_SEL5	0x0069	B	0x00	
DVS_CTRL_SEL0	0x006a	B	0x00	
DVS_CTRL_SEL1	0x006b	B	0x00	
DVS_CTRL_SEL2	0x006c	B	0x00	
DVS_CTRL_SEL3	0x006d	B	0x00	
DVS_CTRL_SEL3	0x006e	B	0x00	
DVS_START_CTRL	0x0070	B	0x00	
PWRCTRL_GPIO	0x0071	B	0x00	
SYS_CFG3	0x0072	B	0x00	
WDT_REG	0x0073	B	0x00	

Name	Offset	Size	Reset Value	Description
ON_SOURCE	0x0074	B	0x00	
OFF_SOURCE	0x0075	B	0x00	
PWRON_KEY	0x0076	B	0x06 bit7：OTP	
INT_STS0	0x0077	B	0x00	
INT_MSK0	0x0078	B	0x00	
INT_STS1	0x0079	B	0x00	
INT_MSK1	0x007a	B	0x00	
GPIO_INT_CONFIG	0x007b	B	0x02	
DATA_REG0	0x007c	B	0x00	
DATA_REG1	0x007d	B	0x00	
DATA_REG2	0x007e	B	0x00	
DATA_REG3	0x007f	B	0x00	
DATA_REG4	0x0080	B	0x00	
DATA_REG5	0x0081	B	0x00	
DATA_REG6	0x0082	B	0x00	
DATA_REG7	0x0083	B	0x00	
DATA_REG8	0x0084	B	0x00	
DATA_REG9	0x0085	B	0x00	
DATA_REG10	0x0086	B	0x00	
DATA_REG11	0x0087	B	0x00	
DATA_REG12	0x0088	B	0x00	
DATA_REG13	0x0089	B	0x00	
DATA_REG14	0x008a	B	0x00	
DATA_REG15	0x008b	B	0x00	
BUCK_SEQ_REG0	0x00B2	B	0x00	
BUCK_SEQ_REG1	0x00B3	B	0x00	
BUCK_SEQ_REG2	0x00B4	B	0x00	
BUCK_SEQ_REG3	0x00B5	B	0x00	
BUCK_SEQ_REG4	0x00B6	B	0x00	
BUCK_SEQ_REG5	0x00B7	B	0x00	
BUCK_SEQ_REG6	0x00B8	B	0x00	
BUCK_SEQ_REG7	0x00B9	B	0x00	
BUCK_SEQ_REG8	0x00BA	B	0x00	
BUCK_SEQ_REG9	0x00BB	B	0x00	
BUCK_SEQ_REG10	0x00BC	B	0x00	
BUCK_SEQ_REG11	0x00BD	B	0x00	
BUCK_SEQ_REG12	0x00BE	B	0x00	
BUCK_SEQ_REG13	0x00BF	B	0x00	
BUCK_SEQ_REG14	0x00C0	B	0x00	
BUCK_SEQ_REG15	0x00C1	B	0x00	
BUCK_SEQ_REG16	0x00C2	B	0x00	
BUCK_SEQ_REG17	0x00C3	B	0x00	
BACKUP_REG7	0x00DC	B	0x00	
BACKUP_REG6	0x00E6	B	0x00	
BACKUP_REG5	0x00E7	B	0x00	
BACKUP_REG1	0x00E8	B	0x00	
BACKUP_REG2	0x00E9	B	0x00	
BACKUP_REG3	0x00EA	B	0x00	
BACKUP_REG4	0x00EB	B	0x00	
BUCK_RSERVE_REG3	0x00FD	B	0x00	
BUCK_RSERVE_REG4	0x00FE	B	0x00	

5.2 Register Description

POWER_EN0

Address: Operational Base + offset (0x00)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK4_EN_MASK BUCK4_EN_MASK: MUST write them to "1" if want to change corresponding BUCK4_EN bit，The BUCK4_EN_MASK bits should be clear when BUCK4_EN bits have been written.
6	RW	0x0	BUCK3_EN_MASK BUCK3_EN_MASK: MUST write them to "1" if want to change corresponding BUCK3_EN bit，The BUCK3_EN_MASK bits should be clear when BUCK3_EN bits have been written.
5	RW	0x0	BUCK2_EN_MASK BUCK2_EN_MASK: MUST write them to "1" if want to change corresponding BUCK2_EN bit，The BUCK2_EN_MASK bits should be clear when BUCK2_EN bits have been written.
4	RW	0x0	BUCK1_EN_MASK BUCK1_EN_MASK: MUST write them to "1" if want to change corresponding BUCK1_EN bit，The BUCK1_EN_MASK bits should be clear when BUCK1_EN bits have been written.
3	RW	OTP	BUCK4_EN BUCK4_EN: BUCK4 enable in active mode 1, Enable 0, Disable the default value is set by OTP
2	RW	OTP	BUCK3_EN BUCK3_EN: BUCK3 enable in active mode 1, Enable 0, Disable the default value is set by OTP

Bit	Attr	Reset Value	Description
1	RW	OTP	BUCK2_EN BUCK2_EN: BUCK2 enable in active mode 1, Enable 0, Disable the default value is set by OTP
0	RW	OTP	BUCK1_EN BUCK1_EN: BUCK1 enable in active mode 1, Enable 0, Disable the default value is set by OTP

POWER_EN1

Address: Operational Base + offset (0x01)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK8_EN_MASK BUCK8_EN_MASK: MUST write them to "1" if want to change corresponding BUCK8_EN bit，The BUCK8_EN_MASK bits should be clear when BUCK8_EN bits have been written.
6	RW	0x0	BUCK7_EN_MASK BUCK7_EN_MASK: MUST write them to "1" if want to change corresponding BUCK7_EN bit，The BUCK7_EN_MASK bits should be clear when BUCK7_EN bits have been written.
5	RW	0x0	BUCK6_EN_MASK BUCK6_EN_MASK: MUST write them to "1" if want to change corresponding BUCK6_EN bit，The BUCK6_EN_MASK bits should be clear when BUCK6_EN bits have been written.
4	RW	0x0	BUCK5_EN_MASK BUCK5_EN_MASK: MUST write them to "1" if want to change corresponding BUCK5_EN bit，The BUCK5_EN_MASK bits should be clear when BUCK5_EN bits have been written.
3	RW	OTP	BUCK8_EN BUCK8_EN: BUCK8 enable in active mode 1, Enable 0, Disable the default value is set by OTP

Bit	Attr	Reset Value	Description
2	RW	OTP	BUCK7_EN BUCK7_EN: BUCK7 enable in active mode 1, Enable 0, Disable the default value is set by OTP
1	RW	OTP	BUCK6_EN BUCK6_EN: BUCK6 enable in active mode 1, Enable 0, Disable the default value is set by OTP
0	RW	OTP	BUCK5_EN BUCK5_EN: BUCK5 enable in active mode 1, Enable 0, Disable the default value is set by OTP

POWER_EN2

Address: Operational Base + offset (0x02)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV RESV:Reserve
5	RW	0x0	BUCK10_EN_MASK BUCK10_EN_MASK: MUST write them to "1" if want to change corresponding BUCK10_EN bit，The BUCK10_EN_MASK bits should be clear when BUCK10_EN bits have been written.
4	RW	0x0	BUCK9_EN_MASK BUCK9_EN_MASK: MUST write them to "1" if want to change corresponding BUCK9_EN bit，The BUCK9_EN_MASK bits should be clear when BUCK9_EN bits have been written.
3:2	RW	0x0	RESV RESV:Reserve
1	RW	OTP	BUCK10_EN BUCK10_EN: BUCK10 enable in active mode 1, Enable 0, Disable the default value is set by OTP

Bit	Attr	Reset Value	Description
0	RW	OTP	BUCK9_EN BUCK9_EN: BUCK9 enable in active mode 1, Enable 0, Disable the default value is set by OTP

POWER_EN3

Address: Operational Base + offset (0x03)

Bit	Attr	Reset Value	Description
7	RW	0x0	NLDO4_EN_MASK NLDO4_EN_MASK: MUST write them to "1" if want to change corresponding NLDO4_EN bit，The NLDO4_EN_MASK bits should be clear when NLDO4_EN bits have been written.
6	RW	0x0	NLDO3_EN_MASK NLDO3_EN_MASK: MUST write them to "1" if want to change corresponding NLDO3_EN bit，The NLDO3_EN_MASK bits should be clear when NLDO3_EN bits have been written.
5	RW	0x0	NLDO2_EN_MASK NLDO2_EN_MASK: MUST write them to "1" if want to change corresponding NLDO2_EN bit，The NLDO2_EN_MASK bits should be clear when NLDO2_EN bits have been written.
4	RW	0x0	NLDO1_EN_MASK NLDO1_EN_MASK: MUST write them to "1" if want to change corresponding NLDO1_EN bit，The NLDO1_EN_MASK bits should be clear when NLDO1_EN bits have been written.
3	RW	OTP	NLDO4_EN NLDO4_EN: NLDO4 enable in active mode 1, Enable 0, Disable the default value is set by OTP
2	RW	OTP	NLDO3_EN NLDO3_EN: NLDO3 enable in active mode 1, Enable 0, Disable the default value is set by OTP

Bit	Attr	Reset Value	Description
1	RW	OTP	NLDO2_EN NLDO2_EN: NLDO2 enable in active mode 1, Enable 0, Disable the default value is set by OTP
0	RW	OTP	NLDO1_EN NLDO1_EN: NLDO1 enable in active mode 1, Enable 0, Disable the default value is set by OTP

POWER_EN4

Address: Operational Base + offset (0x04)

Bit	Attr	Reset Value	Description
7	RW	0x0	PLDO3_EN_MASK PLDO3_EN_MASK: MUST write them to "1" if want to change corresponding PLDO3_EN bit，The PLDO3_EN_MASK bits should be clear when PLDO3_EN bits have been written.
6	RW	0x0	PLDO2_EN_MASK PLDO2_EN_MASK: MUST write them to "1" if want to change corresponding PLDO2_EN bit，The PLDO2_EN_MASK bits should be clear when PLDO2_EN bits have been written.
5	RW	0x0	PLDO1_EN_MASK PLDO1_EN_MASK: MUST write them to "1" if want to change corresponding PLDO1_EN bit，The PLDO1_EN_MASK bits should be clear when PLDO1_EN bits have been written.
4	RW	0x0	PLDO6_EN_MASK PLDO6_EN_MASK: MUST write them to "1" if want to change corresponding PLDO6_EN bit，The PLDO6_EN_MASK bits should be clear when PLDO6_EN bits have been written.
3	RW	OTP	PLDO3_EN PLDO3_EN: PLDO3 enable in active mode 1, Enable 0, Disable the default value is set by OTP

Bit	Attr	Reset Value	Description
2	RW	OTP	PLDO2_EN PLDO2_EN: PLDO2 enable in active mode 1, Enable 0, Disable the default value is set by OTP
1	RW	OTP	PLDO1_EN PLDO1_EN: PLDO1 enable in active mode 1, Enable 0, Disable the default value is set by OTP
0	RW	OTP	PLDO6_EN PLDO6_EN: PLDO6 enable in active mode 1, Enable 0, Disable the default value is set by OTP

POWER_EN5

Address: Operational Base + offset (0x05)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV RESV:Reserve
6	RW	0x0	NLDO5_EN_MASK NLDO5_EN_MASK: MUST write them to "1" if want to change corresponding NLDO5_EN bit，The NLDO5_EN_MASK bits should be clear when NLDO5_EN bits have been written.
5	RW	0x0	PLDO5_EN_MASK PLDO5_EN_MASK: MUST write them to "1" if want to change corresponding PLDO5_EN bit，The PLDO5_EN_MASK bits should be clear when PLDO5_EN bits have been written.
4	RW	0x0	PLDO4_EN_MASK PLDO4_EN_MASK: MUST write them to "1" if want to change corresponding PLDO4_EN bit，The PLDO4_EN_MASK bits should be clear when PLDO4_EN bits have been written.
3	RW	0x0	RESV RESV:Reserve
2	RW	OTP	NLDO5_EN NLDO5_EN: NLDO5 enable in active mode 1, Enable 0, Disable the default value is set by OTP

Bit	Attr	Reset Value	Description
1	RW	OTP	PLDO5_EN PLDO5_EN: PLDO5 enable in active mode 1, Enable 0, Disable the default value is set by OTP
0	RW	OTP	PLDO4_EN PLDO4_EN: PLDO4 enable in active mode 1, Enable 0, Disable the default value is set by OTP

POWER_SLP_EN0

Address: Operational Base + offset (0x06)

Bit	Attr	Reset Value	Description
7	RW	OTP	BUCK8_SLP_EN BUCK8_SLP_EN: BUCK8 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp
6	RW	OTP	BUCK7_SLP_EN BUCK7_SLP_EN: BUCK7 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp
5	RW	OTP	BUCK6_SLP_EN BUCK6_SLP_EN: BUCK6 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp
4	RW	OTP	BUCK5_SLP_EN BUCK5_SLP_EN: BUCK5 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp
3	RW	OTP	BUCK4_SLP_EN BUCK4_SLP_EN: BUCK4 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp

Bit	Attr	Reset Value	Description
2	RW	OTP	BUCK3_SLP_EN BUCK3_SLP_EN: BUCK3 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp
1	RW	OTP	BUCK2_SLP_EN BUCK2_SLP_EN: BUCK2 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp
0	RW	OTP	BUCK1_SLP_EN BUCK1_SLP_EN: BUCK1 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp

POWER_SLP_EN1
Address: Operational Base + offset (0x07)

Bit	Attr	Reset Value	Description
7	RW	OTP	BUCK10_SLP_EN BUCK10_SLP_EN: BUCK10 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp
6	RW	OTP	BUCK9_SLP_EN BUCK9_SLP_EN: BUCK9 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp
5	RW	OTP	RESV RESV:Reserve
4	RW	OTP	NLDO5_SLP_EN NLDO5_SLP_EN: NLDO5 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp

Bit	Attr	Reset Value	Description
3	RW	OTP	NLDO4_SLP_EN NLDO4_SLP_EN: NLDO4 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp
2	RW	OTP	NLDO3_SLP_EN NLDO3_SLP_EN: NLDO3 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp
1	RW	OTP	NLDO2_SLP_EN NLDO2_SLP_EN: NLDO2 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp
0	RW	OTP	NLDO1_SLP_EN NLDO1_SLP_EN: NLDO1 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp

POWER_SLP_EN2
Address: Operational Base + offset (0x08)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV RESV:Reserve
5	RW	OTP	PLDO5_SLP_EN PLDO5_SLP_EN: PLDO5 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp
4	RW	OTP	PLDO4_SLP_EN PLDO4_SLP_EN: PLDO4 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp

Bit	Attr	Reset Value	Description
3	RW	OTP	PLDO3_SLP_EN PLDO3_SLP_EN: PLDO3 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp
2	RW	OTP	PLDO2_SLP_EN PLDO2_SLP_EN: PLDO2 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp
1	RW	OTP	PLDO1_SLP_EN PLDO1_SLP_EN: PLDO1 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp
0	RW	OTP	PLDO6_SLP_EN PLDO6_SLP_EN: PLDO6 enable in SLEEP mode 1, Enable 0, Disable the default value is set by otp

POWER_DISCHRG_EN0
Address: Operational Base + offset (0x09)

Bit	Attr	Reset Value	Description
7	RW	0x1	BUCK8_DISCHG_EN BUCK8_DISCHG_EN: BUCK8 discharge enable when the channel is off 0: Disable 1:enable
6	RW	0x1	BUCK7_DISCHG_EN BUCK7_DISCHG_EN: BUCK7 discharge enable when the channel is off 0: Disable 1:enable
5	RW	0x1	BUCK6_DISCHG_EN BUCK6_DISCHG_EN: BUCK6 discharge enable when the channel is off 0: Disable 1:enable
4	RW	0x1	BUCK5_DISCHG_EN BUCK5_DISCHG_EN: BUCK5 discharge enable when the channel is off 0: Disable 1:enable

Bit	Attr	Reset Value	Description
3	RW	0x1	BUCK4_DISCHG_EN BUCK4_DISCHG_EN: BUCK4 discharge enable when the channel is off 0: Disable 1:enable
2	RW	0x1	BUCK3_DISCHG_EN BUCK3_DISCHG_EN: BUCK3 discharge enable when the channel is off 0: Disable 1:enable
1	RW	0x1	BUCK2_DISCHG_EN BUCK2_DISCHG_EN: BUCK2 discharge enable when the channel is off 0: Disable 1:enable
0	RW	0x1	BUCK1_DISCHG_EN BUCK1_DISCHG_EN: BUCK1 discharge enable when the channel is off 0: Disable 1:enable

POWER_DISCHRG_EN1
Address: Operational Base + offset (0x0a)

Bit	Attr	Reset Value	Description
7	RW	0x1	BUCK10_DISCHG_EN BUCK10_DISCHG_EN: BUCK10 discharge enable when the channel is off 0: Disable 1:enable
6	RW	0x1	BUCK9_DISCHG_EN BUCK9_DISCHG_EN: BUCK9 discharge enable when the channel is off 0: Disable 1:enable
5	RW	0x0	RESV RESV:Reserve
4	RW	0x1	NLDO5_DISCHG_EN NLDO5_DISCHG_EN: NLDO5 discharge enable when the channel is off 0: Disable 1:enable
3	RW	0x1	NLDO4_DISCHG_EN NLDO4_DISCHG_EN: NLDO4 discharge enable when the channel is off 0: Disable 1:enable
2	RW	0x1	NLDO3_DISCHG_EN NLDO3_DISCHG_EN: NLDO3 discharge enable when the channel is off 0: Disable 1:enable

Bit	Attr	Reset Value	Description
1	RW	0x1	NLDO2_DISCHG_EN NLDO2_DISCHG_EN: NLDO2 discharge enable when the channel is off 0: Disable 1:enable
0	RW	0x1	NLDO1_DISCHG_EN NLDO1_DISCHG_EN: NLDO1 discharge enable when the channel is off 0: Disable 1:enable

POWER_DISCHRG_EN2
Address: Operational Base + offset (0x0b)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV RESV:Reserve
5	RW	0x1	PLDO6_DISCHG_EN PLDO6_DISCHG_EN: PLDO6 discharge enable when the channel is off 0: Disable 1:enable
4	RW	0x1	PLDO5_DISCHG_EN PLDO5_DISCHG_EN: PLDO5 discharge enable when the channel is off 0: Disable 1:enable
3	RW	0x1	PLDO4_DISCHG_EN PLDO4_DISCHG_EN: PLDO4 discharge enable when the channel is off 0: Disable 1:enable
2	RW	0x1	PLDO3_DISCHG_EN PLDO3_DISCHG_EN: PLDO3 discharge enable when the channel is off 0: Disable 1:enable
1	RW	0x1	PLDO2_DISCHG_EN PLDO2_DISCHG_EN: PLDO2 discharge enable when the channel is off 0: Disable 1:enable
0	RW	0x1	PLDO1_DISCHG_EN PLDO1_DISCHG_EN: PLDO1 discharge enable when the channel is off 0: Disable 1:enable

BUCK_FB_CONFIG
Address: Operational Base + offset (0x0c)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK10_LP_EN BUCK10_LP_EN: Low power function enable bit of BUCK10 0: disable 1:enable

Bit	Attr	Reset Value	Description
6	RW	0x0	BUCK9_LP_EN BUCK9_LP_EN: Low power function enable bit of BUCK9 0: disable 1:enable
5	RW	0x0	RESV RESV:Reserve
4	RW	0x0	PLDO_SLP_LP_EN PLDO_SLP_LP_EN: Low power function enable bit of PLDO 0: disable 1:enable
3	RW	0x0	NLDO_SLP_LP_EN NLDO_SLP_LP_EN: Low power function enable bit of NLDO 0: disable 1:enable
2	RW	0x0	BK_LDO3V_LPEN BUCK3_LP_EN: Low power function enable bit of 3VLDO 0: disable 1:enable
1	RW	0x0	BK_LDO3V_BPEN BK_LDO3V_BPEN: 3V LDO disable and short to VDD enable bit 0: disable 1:enable
0	RW	0X1	BK_LDO3V_EN BK_LDO3V_EN: enable bit of BK_LDO3V 0: disable 1:enable

SLP_LP_CONFIG

Address: Operational Base + offset (0x0d)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK8_LP_EN BUCK8_LP_EN: Low power function enable bit of BUCK8 0: disable 1:enable
6	RW	0x0	BUCK7_LP_EN BUCK7_LP_EN: Low power function enable bit of BUCK7 0: disable 1:enable
5	RW	0x0	BUCK6_LP_EN BUCK6_LP_EN: Low power function enable bit of BUCK6 0: disable 1:enable
4	RW	0x0	BUCK5_LP_EN BUCK5_LP_EN: Low power function enable bit of BUCK5 0: disable 1:enable

Bit	Attr	Reset Value	Description
3	RW	0x0	BUCK4_LP_EN BUCK4_LP_EN: Low power function enable bit of BUCK4 0: disable 1:enable
2	RW	0x0	BUCK3_LP_EN BUCK3_LP_EN: Low power function enable bit of BUCK3 0: disable 1:enable
1	RW	0x0	BUCK2_LP_EN BUCK2_LP_EN: Low power function enable bit of BUCK2 0: disable 1:enable
0	RW	0X1	BUCK1_LP_EN BUCK1_LP_EN: Low power function enable bit of BUCK1 0: disable 1:enable

POWER_FPWM_EN0

Address: Operational Base + offset (0x0e)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK8_ON_FPWM BUCK8_ON_FPWM: BUCK8 Forced PWM mode selection 1, Forced PWM mode in active mode; 0, PWM/PFM auto change mode
6	RW	0x0	BUCK7_ON_FPWM BUCK7_ON_FPWM: BUCK7 Forced PWM mode selection 1, Forced PWM mode in active mode; 0, PWM/PFM auto change mode
5	RW	0x0	BUCK6_ON_FPWM BUCK6_ON_FPWM: BUCK6 Forced PWM mode selection 1, Forced PWM mode in active mode; 0, PWM/PFM auto change mode
4	RW	0x0	BUCK5_ON_FPWM BUCK5_ON_FPWM: BUCK5 Forced PWM mode selection 1, Forced PWM mode in active mode; 0, PWM/PFM auto change mode
3	RW	0x0	BUCK4_ON_FPWM BUCK4_ON_FPWM: BUCK4 Forced PWM mode selection 1, Forced PWM mode in active mode; 0, PWM/PFM auto change mode

Bit	Attr	Reset Value	Description
2	RW	0x0	BUCK3_ON_FPWM BUCK3_ON_FPWM: BUCK3 Forced PWM mode selection 1, Forced PWM mode in active mode; 0, PWM/PFM auto change mode
1	RW	0x0	BUCK2_ON_FPWM BUCK2_ON_FPWM: BUCK2 Forced PWM mode selection 1, Forced PWM mode in active mode; 0, PWM/PFM auto change mode
0	RW	0X1	BUCK1_ON_FPWM BUCK1_ON_FPWM: BUCK1 Forced PWM mode selection 1, Forced PWM mode in active mode; 0, PWM/PFM auto change mode

POWER_FPWM_EN1

Address: Operational Base + offset (0x0f)

Bit	Attr	Reset Value	Description
7:2	RW	0x0	RESV RESV:Reserve
1	RW	0x0	BUCK10_ON_FPWM BUCK10_ON_FPWM: BUCK10 Forced PWM mode selection 1, Forced PWM mode in active mode; 0, PWM/PFM auto change mode
0	RW	0X1	BUCK9_ON_FPWM BUCK9_ON_FPWM: BUCK9 Forced PWM mode selection 1, Forced PWM mode in active mode; 0, PWM/PFM auto change mode

BUCK1_CONFIG

Address: Operational Base + offset (0x10)

Bit	Attr	Reset Value	Description
7:6	RW	0x1	BUCK1_RATE BUCK1_RATE: Voltage change rate after DVS(2M clack), 3BIT, BIT<2> at the EB Register 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;

Bit	Attr	Reset Value	Description
5:3	RW	0x4	BUCK1_ILPK BUCK1_ILPK: BUCK1 peak current limit select, MUST linkage adjustment with the BUCK1_ ILVL (write the same code) 000:6.4A 001:7.0A 010:7.6A 011:8.3A 100:9A 101:9.8A 110:10.7A 111:11.6A
2:0	RW	0x4	BUCK1_ILVL BUCK1_ILVL: BUCK1 valley current limit select, linkage adjustment with the BUCK1_ ILPK (write the same code) 000:5.0A 001:5.4A 010:5.9A 011:6.4A 100:7A 101:7.6A 110:8.3A 111:9.0A

BUCK2_CONFIG
Address: Operational Base + offset (0x11)

Bit	Attr	Reset Value	Description
7:6	RW	0x1	BUCK2_RATE BUCK2_RATE: Voltage change rate after DVS(2M clack), 3BIT, BIT<2> at the EB Register 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;
5:3	RW	0x4	BUCK2_ILPK BUCK2_ILPK: BUCK1 peak current limit select, MUST linkage adjustment with the BUCK2_ILVL (write the same code) 000:4.8A 001:5.3A 010:5.8A 011:6.4A 100:7A 101:7.7A 110:8.5A 111:9.3A
2:0	RW	0x4	BUCK2_ILVL BUCK2_ILVL: BUCK2 valley current limit select, linkage adjustment with the BUCK2_ILPK (write the same code) 000:3.4A 001:3.8A 010:4.1A 011:4.5A 100:5A 101:5.5A 110:6.1A 111:6.7A

BUCK3_CONFIG
Address: Operational Base + offset (0x12)

Bit	Attr	Reset Value	Description
7:6	RW	0x1	BUCK3_RATE BUCK3_RATE: Voltage change rate after DVS(2M clack), 3BIT, BIT<2> at the EB Register 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;
5:3	RW	0x4	BUCK3_ILPK BUCK3_ILPK: BUCK3 peak current limit select, MUST linkage adjustment with the BUCK3_ILVL (write the same code) 000:4.8A 001:5.3A 010:5.8A 011:6.4A 100:7A 101:7.7A 110:8.5A 111:9.3A
2:0	RW	0x4	BUCK3_ILVL BUCK3_ILVL: BUCK3 valley current limit select, linkage adjustment with the BUCK3_ILPK (write the same code) 000:3.4A 001:3.8A 010:4.1A 011:4.6A 100:5A 101:5.5A 110:6.1A 111:6.7A

BUCK4_CONFIG

Address: Operational Base + offset (0x13)

Bit	Attr	Reset Value	Description
7:6	RW	0x1	BUCK4_RATE BUCK4_RATE: Voltage change rate after DVS(2M clack), 3BIT, BIT<2> at the EB Register 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;
5:3	RW	0x4	BUCK4_ILPK BUCK4_ILPK: BUCK4 peak current limit select, MUST linkage adjustment with the BUCK4_ILVL (write the same code) 000:4.8A 001:5.3A 010:5.8A 011:6.4A 100:7A 101:7.7A 110:8.5A 111:9.3A
2:0	RW	0x4	BUCK4_ILVL BUCK4_ILVL: BUCK4 valley current limit select, linkage adjustment with the BUCK4_ILPK (write the same code) 000:3.4A 001:3.8A 010:4.1A 011:4.5A 100:5A 101:5.5A 110:6.1A 111:6.7A

BUCK5_CONFIG

Address: Operational Base + offset (0x14)

Bit	Attr	Reset Value	Description
7:6	RW	0x1	BUCK5_RATE BUCK5_RATE: Voltage change rate after DVS(2M clack), 3BIT, BIT<2> at the EB Register 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;
5:3	RW	0x4	BUCK5_ILPK BUCK5_ILPK: BUCK5 peak current limit select, MUST linkage adjustment with the BUCK5_ILVL (write the same code) 000:2.7A 001:3A 010:3.3A 011:3.6A 100:4A 101:4.4A 110:4.8A 111:5.3A
2:0	RW	0x4	BUCK5_ILVL BUCK5_ILVL: BUCK5 valley current limit select, linkage adjustment with the BUCK5_ILPK (write the same code) 000:2.2A 001:2.4A 010:2.6A 011:2.9A 100:3.2A 101:3.5A 110:3.9A 111:4.3A

BUCK6_CONFIG
Address: Operational Base + offset (0x15)

Bit	Attr	Reset Value	Description
7:6	RW	0x1	BUCK6_RATE BUCK6_RATE: Voltage change rate after DVS(2M clack), 3BIT, BIT<2> at the EB Register 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;
5:3	RW	0x4	BUCK6_ILPK BUCK6_ILPK: BUCK6 peak current limit select, MUST linkage adjustment with the BUCK6_ILVL (write the same code) 000:2.7A 001:3A 010:3.3A 011:3.6A 100:4A 101:4.4A 110:4.8A 111:5.3A
2:0	RW	0x4	BUCK6_ILVL BUCK6_ILVL: BUCK6 valley current limit select, linkage adjustment with the BUCK6_ILPK (write the same code) 000:2.2A 001:2.4A 010:2.6A 011:2.9A 100:3.2A 101:3.5A 110:3.9A 111:4.3A

BUCK7_CONFIG
Address: Operational Base + offset (0x16)

Bit	Attr	Reset Value	Description
7:6	RW	0x1	BUCK7_RATE BUCK7_RATE: Voltage change rate after DVS(2M clack), 3BIT, BIT<2> at the EB Register 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;
5:3	RW	0x4	BUCK7_ILPK BUCK7_ILPK: BUCK7 peak current limit select, MUST linkage adjustment with the BUCK1_ILVL (write the same code) 000:2.7A 001:3A 010:3.3A 011:3.6A 100:4A 101:4.4A 110:4.8A 111:5.3A
2:0	RW	0x4	BUCK7_ILVL BUCK7_ILVL: BUCK7 valley current limit select, linkage adjustment with the BUCK7_ILPK (write the same code) 000:2.2A 001:2.4A 010:2.6A 011:2.9A 100:3.2A 101:3.5A 110:3.9A 111:4.3A

BUCK8_CONFIG

Address: Operational Base + offset (0x17)

Bit	Attr	Reset Value	Description
7:6	RW	0x1	BUCK8_RATE BUCK8_RATE: Voltage change rate after DVS(2M clack), 3BIT, BIT<2> at the EB Register 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;
5:3	RW	0x4	BUCK8_ILPK BUCK8_ILPK: BUCK8 peak current limit select, MUST linkage adjustment with the BUCK8_ILVL (write the same code) 000:2.7A 001:3A 010:3.3A 011:3.6A 100:4A 101:4.4A 110:4.8A 111:5.3A
2:0	RW	0x4	BUCK8_ILVL BUCK8_ILVL: BUCK8 valley current limit select, linkage adjustment with the BUCK8_ILPK (write the same code) 000:2.2A 001:2.4A 010:2.6A 011:2.9A 100:3.2A 101:3.5A 110:3.9A 111:4.3A

BUCK9_CONFIG

Address: Operational Base + offset (0x18)

Bit	Attr	Reset Value	Description
7:6	RW	0x1	BUCK9_RATE BUCK9_RATE: Voltage change rate after DVS(2M clack), 3BIT, BIT<2> at the EA Register 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;
5:3	RW	0x4	BUCK9_ILPK BUCK9_ILPK: BUCK9 peak current limit select, MUST linkage adjustment with the BUCK9_ILVL (write the same code) 000:2.7A 010:3A 010:3.3A 011:3.6A 100:4A 101:4.4A 110:4.8A 111:5.3A
2:0	RW	0x4	BUCK9_ILVL BUCK9_ILVL: BUCK9 valley current limit select, linkage adjustment with the BUCK9_ILPK (write the same code) 000:2.2A 001:2.4A 010:2.6A 011:2.9A 100:3.2A 101:3.5A 110:3.9A 111:4.3A

BUCK10_CONFIG

Address: Operational Base + offset (0x19)

Bit	Attr	Reset Value	Description
7:6	RW	0x1	BUCK10_RATE BUCK10_RATE: Voltage change rate after DVS(2M clack), 3BIT, BIT<2> at the EA Register 000: 4lsb/1clk;001: 2lsb/4clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;
5:3	RW	0x4	BUCK10_ILPK BUCK10_ILPK: BUCK10 peak current limit select, MUST linkage adjustment with the BUCK10_ILVL (write the same code) 000:2.7A 001:3A 010:3.3A 011:3.6A 100:4A 101:4.4A 110:4.8A 111:5.3A
2:0	RW	0x4	BUCK10_ILVL BUCK10_ILVL: BUCK10 valley current limit select, linkage adjustment with the BUCK10_ILPK (write the same code) 000:2.2A 001:2.4A 010:2.6A 011:2.9A 100:3.2A 101:3.5A 110:3.9A 111:4.3A

BUCK1_ON_VSEL

Address: Operational Base + offset (0x1a)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK1_ON_VSEL BUCK1_ON_VSEL: BUCK1 active mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK2_ON_VSEL

Address: Operational Base + offset (0x1b)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK2_ON_VSEL BUCK2_ON_VSEL: BUCK2 active mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK3_ON_VSEL
Address: Operational Base + offset (0x1c)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK3_ON_VSEL BUCK3_ON_VSEL: BUCK3 active mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK4_ON_VSEL
Address: Operational Base + offset (0x1d)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK4_ON_VSEL BUCK4_ON_VSEL: BUCK4 active mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK5_ON_VSEL
Address: Operational Base + offset (0x1e)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK5_ON_VSEL BUCK5_ON_VSEL: BUCK5 active mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK6_ON_VSEL
Address: Operational Base + offset (0x1f)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK6_ON_VSEL BUCK6_ON_VSEL: BUCK1 active mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK7_ON_VSEL
Address: Operational Base + offset (0x20)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK7_ON_VSEL BUCK7_ON_VSEL: BUCK7 active mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK8_ON_VSEL
Address: Operational Base + offset (0x21)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK8_ON_VSEL BUCK8_ON_VSEL: BUCK8 active mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK9_ON_VSEL
Address: Operational Base + offset (0x22)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK9_ON_VSEL BUCK9_ON_VSEL: BUCK9 active mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK10_ON_VSEL
Address: Operational Base + offset (0x23)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK10_ON_VSEL BUCK10_ON_VSEL: BUCK10 active mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK1_SLP_VSEL

Address: Operational Base + offset (0x24)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK1_SLP_VSEL BUCK1_SLP_VSEL: BUCK1 SLEEP mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK2_SLP_VSEL

Address: Operational Base + offset (0x25)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK2_SLP_VSEL BUCK2_SLP_VSEL: BUCK2 SLEEP mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK3_SLP_VSEL

Address: Operational Base + offset (0x26)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK3_SLP_VSEL BUCK3_SLP_VSEL: BUCK3 SLEEP mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK4_SLP_VSEL

Address: Operational Base + offset (0x27)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK4_SLP_VSEL BUCK4_SLP_VSEL: BUCK4 SLEEP mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK5_SLP_VSEL

Address: Operational Base + offset (0x28)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK5_SLP_VSEL BUCK5_SLP_VSEL: BUCK5 SLEEP mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK6_SLP_VSEL

Address: Operational Base + offset (0x29)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK6_SLP_VSEL BUCK6_SLP_VSEL: BUCK6 SLEEP mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK7_SLP_VSEL

Address: Operational Base + offset (0x2a)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK7_SLP_VSEL BUCK7_SLP_VSEL: BUCK7 SLEEP mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK8_SLP_VSEL

Address: Operational Base + offset (0x2b)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK8_SLP_VSEL BUCK8_SLP_VSEL: BUCK8 SLEEP mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK9_SLP_VSEL

Address: Operational Base + offset (0x2c)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK9_SLP_VSEL BUCK9_SLP_VSEL: BUCK9 SLEEP mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK10_SLP_VSEL

Address: Operational Base + offset (0x2d)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	BUCK10_SLP_VSEL BUCK10_SLP_VSEL: BUCK10 SLEEP mode voltage select, 0.5V~1.5V(step=6.25mV), 1.5~3.4V(step=25mV) the detail bits decode shown in the sheet called "Decode" the default value is set by OTP.

BUCK_DEBUG13

Address: Operational Base + offset (0x3c)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK2_CMIN_ENB BUCK2_CMIN_ENB: BUCK2 min current limit enable. 0:Enable 1:Disable
6:4	RW	0x4	BUCK2_CMIN_SEL BUCK2_CMIN_SEL: BUCK2 min current limit select. 000:1.1A; 001:1A; 010:0.906A; 011:0.805A; 100:0.716A; 101:0.636A; 110:0.566A; 111:0.503A
3	RW	0x0	BUCK1_CMIN_ENB BUCK1_CMIN_ENB: BUCK1 min current limit enable. 0:Enable 1:Disable
2:0	RW	0x4	BUCK1_CMIN_SEL BUCK1_CMIN_SEL: BUCK1 min current limit select. 000:1.1A; 001:1A; 010:0.906A; 011:0.805A; 100:0.716A; 101:0.636A; 110:0.566A; 111:0.503A

BUCK_DEBUG14

Address: Operational Base + offset (0x3d)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK4_CMIN_ENB BUCK4_CMIN_ENB: BUCK4 min current limit enable. 0:Enable 1:Disable
6:4	RW	0x4	BUCK4_CMIN_SEL BUCK4_CMIN_SEL: BUCK4 min current limit select. 000:1.1A; 001:1A; 010:0.906A; 011:0.805A; 100:0.716A; 101:0.636A; 110:0.566A; 111:0.503A
3	RW	0x0	BUCK3_CMIN_ENB BUCK3_CMIN_ENB: BUCK3 min current limit enable. 0:Enable 1:Disable
2:0	RW	0x4	BUCK3_CMIN_SEL BUCK3_CMIN_SEL: BUCK3 min current limit select. 000:1.1A; 001:1A; 010:0.906A; 011:0.805A; 100:0.716A; 101:0.636A; 110:0.566A; 111:0.503A

BUCK_DEBUG15

Address: Operational Base + offset (0x3e)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK6_CMIN_ENB BUCK6_CMIN_ENB: BUCK6 min current limit enable. 0:Enable 1:Disable
6:4	RW	0x4	BUCK6_CMIN_SEL BUCK6_CMIN_SEL: BUCK6 min current limit select. 000:0.57A; 001:0.506A; 010:0.45A; 011:0.4A; 100:0.356A; 101:0.316A; 110:0.281A; 111:0.25A
3	RW	0x0	BUCK5_CMIN_ENB BUCK5_CMIN_ENB: BUCK5 min current limit enable. 0:Enable 1:Disable
2:0	RW	0x4	BUCK5_CMIN_SEL BUCK5_CMIN_SEL: BUCK5 min current limit select. 000:0.57A; 001:0.506A; 010:0.45A; 011:0.4A; 100:0.356A; 101:0.316A; 110:0.281A; 111:0.25A

BUCK_DEBUG16

Address: Operational Base + offset (0x3f)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK8_CMIN_ENB BUCK8_CMIN_ENB: BUCK8 min current limit enable. 0:Enable 1:Disable
6:4	RW	0x4	BUCK8_CMIN_SEL BUCK8_CMIN_SEL: BUCK8 min current limit select. 000:0.57A; 001:0.506A; 010:0.45A; 011:0.4A; 100:0.356A; 101:0.316A; 110:0.281A; 111:0.25A
3	RW	0x0	BUCK7_CMIN_ENB BUCK7_CMIN_ENB: BUCK7 min current limit enable. 0:Enable 1:Disable
2:0	RW	0x4	BUCK7_CMIN_SEL BUCK7_CMIN_SEL: BUCK7 min current limit select. 000:0.57A; 001:0.506A; 010:0.45A; 011:0.4A; 100:0.356A; 101:0.316A; 110:0.281A; 111:0.25A

BUCK_DEBUG17

Address: Operational Base + offset (0x40)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK10_CMIN_ENB BUCK10_CMIN_ENB: BUCK10 min current limit enable. 0:Enable 1:Disable
6:4	RW	0x4	BUCK10_CMIN_SEL BUCK10_CMIN_SEL: BUCK10 min current limit select. 000:0.57A; 001:0.506A; 010:0.45A; 011:0.4A; 100:0.356A; 101:0.316A; 110:0.281A; 111:0.25A
3	RW	0x0	BUCK9_CMIN_ENB BUCK9_CMIN_ENB: BUCK9 min current limit enable. 0:Enable 1:Disable
2:0	RW	0x4	BUCK9_CMIN_SEL BUCK9_CMIN_SEL: BUCK9 min current limit select. 000:0.57A; 001:0.506A; 010:0.45A; 011:0.4A; 100:0.356A; 101:0.316A; 110:0.281A; 111:0.25A

NLDO_IMAX

Address: Operational Base + offset (0x42)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV RESV:Reserve
6	RW	0x0	RESV RESV:Reserve
5	RW	0x0	RESV RESV:Reserve
4	RW	0x0	NLDO5_IMAX NLDO5_IMAX: NLDO5 current limit setting 0: normal, 1: 130% of normal value
3	RW	0x0	NLDO4_IMAX NLDO4_IMAX: NLDO4 current limit setting 0: normal, 1: 130% of normal value
2	RW	0x0	NLDO3_IMAX NLDO3_IMAX: NLDO3 current limit setting 0: normal, 1: 130% of normal value
1	RW	0x0	NLDO2_IMAX NLDO2_IMAX: NLDO2 current limit setting 0: normal, 1: 130% of normal value
0	RW	0x0	NLDO1_IMAX NLDO1_IMAX: NLDO1 current limit setting 0: normal, 1: 130% of normal value

NLDO1_ON_VSEL

Address: Operational Base + offset (0x43)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	NLDO1_ON_VSEL NLDO1_ON_VSEL: NLDO1 active mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

NLDO2_ON_VSEL

Address: Operational Base + offset (0x44)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	NLDO2_ON_VSEL NLDO2_ON_VSEL: NLDO2 active mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

NLDO3_ON_VSEL

Address: Operational Base + offset (0x45)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	NLDO3_ON_VSEL NLDO3_ON_VSEL: NLDO3 active mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

NLDO4_ON_VSEL

Address: Operational Base + offset (0x46)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	NLDO4_ON_VSEL NLDO4_ON_VSEL: NLDO4 active mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

NLDO5_ON_VSEL

Address: Operational Base + offset (0x47)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	NLDO5_ON_VSEL NLDO5_ON_VSEL: NLDO5 active mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

NLDO1_SLP_VSEL

Address: Operational Base + offset (0x48)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	NLDO1_SLP_VSEL NLDO1_SLP_VSEL: NLDO1 SLEEP mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

NLDO2_SLP_VSEL

Address: Operational Base + offset (0x49)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	NLDO2_SLP_VSEL NLDO2_SLP_VSEL: NLDO2 SLEEP mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

NLDO3_SLP_VSEL

Address: Operational Base + offset (0x4a)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	NLDO3_SLP_VSEL NLDO3_SLP_VSEL: NLDO3 SLEEP mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

NLDO4_SLP_VSEL

Address: Operational Base + offset (0x4b)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	NLDO4_SLP_VSEL NLDO4_SLP_VSEL: NLDO4 SLEEP mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

NLDO5_SLP_VSEL

Address: Operational Base + offset (0x4c)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	NLDO5_SLP_VSEL NLDO5_SLP_VSEL: NLDO5 SLEEP mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

PLDO_IMAX

Address: Operational Base + offset (0x4d)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV RESV:Reserve
5	RW	0x0	PLDO6_IMAX PLDO6_IMAX: PLDO6 current limit setting 0: normal, 1: 130% of normal value
4	RW	0x0	PLDO5_IMAX PLDO5_IMAX: PLDO5 current limit setting 0: normal, 1: 130% of normal value
3	RW	0x0	PLDO4_IMAX PLDO4_IMAX: PLDO4 current limit setting 0: normal, 1: 130% of normal value
2	RW	0x0	PLDO3_IMAX PLDO3_IMAX: PLDO3 current limit setting 0: normal, 1: 130% of normal value
1	RW	0x0	PLDO2_IMAX PLDO2_IMAX: PLDO2 current limit setting 0: normal, 1: 130% of normal value

Bit	Attr	Reset Value	Description
0	RW	0x0	PLDO1_IMAX PLDO1_IMAX: PLDO1 current limit setting 0: normal, 1: 130% of normal value

PLDO1_ON_VSEL

Address: Operational Base + offset (0x4e)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	PLDO1_ON_VSEL PLDO1_ON_VSEL: PLDO1 active mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

PLDO2_ON_VSEL

Address: Operational Base + offset (0x4f)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	PLDO2_ON_VSEL PLDO2_ON_VSEL: PLDO2 active mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

PLDO3_ON_VSEL

Address: Operational Base + offset (0x50)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	PLDO3_ON_VSEL PLDO3_ON_VSEL: PLDO3 active mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

PLDO4_ON_VSEL

Address: Operational Base + offset (0x51)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	PLDO4_ON_VSEL PLDO4_ON_VSEL: PLDO4 active mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

PLDO5_ON_VSEL

Address: Operational Base + offset (0x52)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	PLDO5_ON_VSEL PLDO5_ON_VSEL: PLDO5 active mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

PLDO6_ON_VSEL

Address: Operational Base + offset (0x53)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	PLDO6_ON_VSEL PLDO6_ON_VSEL: PLDO6 active mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

PLDO1_SLP_VSEL

Address: Operational Base + offset (0x54)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	PLDO1_ON_VSEL PLDO1_ON_VSEL: PLDO1 SLEEP mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

PLDO2_SLP_VSEL

Address: Operational Base + offset (0x55)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	PLDO2_ON_VSEL PLDO2_ON_VSEL: PLDO2 SLEEP mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

PLDO3_SLP_VSEL

Address: Operational Base + offset (0x56)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	PLDO3_ON_VSEL PLDO3_ON_VSEL: PLDO3 SLEEP mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

PLDO4_SLP_VSEL

Address: Operational Base + offset (0x57)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	PLDO4_ON_VSEL PLDO4_ON_VSEL: PLDO4 SLEEP mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

PLDO5_SLP_VSEL

Address: Operational Base + offset (0x58)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	PLDO5_ON_VSEL PLDO5_ON_VSEL: PLDO5 SLEEP mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

PLDO6_SLP_VSEL

Address: Operational Base + offset (0x59)

Bit	Attr	Reset Value	Description
7:0	RW	OTP	PLDO6_ON_VSEL PLDO6_ON_VSEL: PLDO6 SLEEP mode voltage select, 0.5V~3.4V(step=12.5mV). The detail bits decode shown in the sheet called "Decode" .The default value is set by OTP.

CHIP_VER

Address: Operational Base + offset (0x5a)

Bit	Attr	Reset Value	Description
7:0	RO	0x80	CHIP_NAME<11:4> CHIP_NAME<11:4>: RK806

CHIP_VER

Address: Operational Base + offset (0x5b)

Bit	Attr	Reset Value	Description
7:4	RO	0x6	CHIP_NAME<3:0> CHIP_NAME<3:0>: RK806
3:0	RO	0x2	CHIP_VER<3:0> CHIP_VER<3:0>:CHIP version

OTP_VER

Address: Operational Base + offset (0x5c)

Bit	Attr	Reset Value	Description
7:4	RO	0x0	RESV RESV:Reserve
3:0	RO	OTP	OTP_VER<3:0> OTP_VER<3:0>: OTP version

SYS_STS

Address: Operational Base + offset (0x5d)

Bit	Attr	Reset Value	Description
7	RO	0x0	PWRON_STS PWRON_STS : PWRON key status 0: PWRON not press 1:PWRON button pressed
6	RO	0x0	VDC_STS VDC_STS: 0:low level; 1:high level
5	RO	0x0	VB_UV_STS VB_UV_STS: VCC1 under voltage lockout status(shut down system if the bit=1)
4	RO	0x0	VB_LO_STS VB_LO_STS: Battery low voltage status 0: VCC1>VB_LO_SEL 1: VCC1<VB_LO_SEL
3	RO	0x0	HOTDIE_STS HOTDIE_STS: Hot-die warning
2	RO	0x0	TSD_STS TSD_STS: Thermal shut down
1	RO	0x0	RESV RESV:Reserve
0	RO	0x0	VB_OV_STS VB_OV_STS: SYS OV happens

SYS_CFG0

Address: Operational Base + offset (0x5e)

Bit	Attr	Reset Value	Description
7	RW	0x0	VB_UV_DLY VB_UV_DLY: VCC1 under voltage ,system shut down effective time 0:5us 1:50us
6：4	RW	0x0	VB_UV_SEL VB_UV_SEL: :system shut down voltage select 000~111:2.7v~3.4v
3	RW	0x1	VB_LO_ACT VB_LO_ACT: VCC1 low action 0: shut down system 1: insert interrupt
2：0	RW	0x4	VB_LO_SEL VB_LO_SEL: VCC1 low voltage threshold 000~111: 2.8V~ 3.5V, step=100mV

SYS_CFG1

Address: Operational Base + offset (0x5f)

Bit	Attr	Reset Value	Description
7	RW	0x0	ABNORDET_ENB ABNORDET_ENB: abnormal enable 0:Enable 1:Disable
6	RW	0x0	TSD_TEMP TSD_TEMP: TSD_TEMP: Thermal shutdown temperture threshold 0: 140℃; 1: 160℃

Bit	Attr	Reset Value	Description
5：4	RW	0x0	HOTDIE_TEMP HOTDIE_TEMP: Hot-die temperature threshold 00:85℃ 01:95℃ 10:105℃ 11:115℃
3	RW	0x0	SYS_OV_SD_EN SYS_OV_SD_EN: Shut down the BUCK1~10 if the VCC1 OV happens 0:Disable 1:Enable
2	RW	0x0	SYS_OV_SD_DLY_SEL SYS_OV_SD_DLY_SEL: SYS OV comparator delay time selection 0: 8uS 1:30uS
1：0	RW	0x0	DLY_ABN_SHORT DLY_ABN_SHORT: abormal detect delay 00:x1 01:x0.875 10:x0.75 11:x0.625

SYS_OPTION

Address: Operational Base + offset (0x61)

Bit	Attr	Reset Value	Description
7	RW	0x0	VBUVLOCK_EN VBUVLOCK_EN: Lock UV after startup 0:Disable 1:Enable
6	RW	0x0	BG_PW_SEL BG_PW_SEL : Internal power supply select 0：VCCRTC 1:LDO3V
5：4	RW	0x0	VCCXDET_DIS VCCXDET_DIS：OVP/UVLO/ VB_LO function action for 00:VCCA,VCC1,VCC2 01: VCCA, VCC2 10:VCCA,VCC1 11: VCCA
3	RW	0x0	RESV RESV:Reserve
2	RW	0x0	TDLY_ABN_LONG TDLY_ABN_LONG: abnormal detect delay 0: x1 1:x1.5
1	RW	0x0	2M_ENB2 2M_ENB2: Digital output 2MHz clock force enable 0:Disable 1:Enable
0	RW	0x0	32K_ENB 32K_ENB: Digital output 32KHz clock force enable 0:Disable 1:Enable

PWRCTRL_CONFIG0

Address: Operational Base + offset (0x62)

Bit	Attr	Reset Value	Description
7	RW	0x1	PWRCTRL2_POL PWRCTRL2_POL: PWRCTRL2 pin polarity 0: active low 1:active high

Bit	Attr	Reset Value	Description
6:4	RW	0x0	PWRCTRL2_FUN PWRCTRL2_FUN: PWRCTRL2 pin function selection：(Note: With this function selected, the RK806 needs 100us to response.) 000：no effect 001：sleep function：If PWRCTRL2 pin effect go to SLEEP state, If PWRCTRL2 pin no effect exit SLEEP state 010：shutdown function：If PWRCTRL2 pin effect shutdown PMIC 011：restart function: If PWRCTRL2 pin effect restart PMIC 100：voltage select function：If PWRCTRL2 pin effect then turn the power supply of group n to the value of the XX_SLP_VSEL , If PWRCTRL2 pin no effect then turn the power supply of group n to the value of the XX_ON_VSEL (Note: The XX_VSEL_CTR_SEL register must be reset before PWRCTRL2_FUN exits the voltage select function) 101：GPIO function.
3	RW	0x1	PWRCTRL1_POL PWRCTRL1_POL: PWRCTRL1 pin polarity 0: active low 1:active high
2:0	RW	0x0	PWRCTRL1_FUN PWRCTRL1_FUN：PWRCTRL1 pin function selection：(Note: With this function selected, the RK806 needs 100us to response.) 000：no effect 001：sleep function：If PWRCTRL1 pin effect go to SLEEP state, If PWRCTRL1 pin no effect exit SLEEP state 010：shutdown function：If PWRCTRL1 pin effect shutdown PMIC 011：restart function: If PWRCTRL1 pin effect restart PMIC 100：voltage regulator function：If PWRCTRL1 in effect then turn the power supply of group n to the value of the XX_SLP_VSEL , If PWRCTRL1 pin no effect then turn the power supply of group n to the value of the XX_ON_VSEL (Note: The XX_VSEL_CTR_SEL register must be reset before PWRCTRL1_FUN exits the voltage select function) 101：GPIO function.

PWRCTRL_**CONFIG1**
Address: Operational Base + offset (0x63)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	RESV RESV:Reserve
3	RW	0x1	PWRCTRL3_POL PWRCTRL3_POL: PWRCTRL3 pin polarity 0: active low 1:active high
2:0	RW	0x0	PWRCTRL3_FUN PWRCTRL3_FUN：PWRCTRL3 pin function selection：(Note: With this function selected, the RK806 needs 100us to response.) 000：no effect 001：sleep function：If PWRCTRL3 pin effect go to SLEEP state, If PWRCTRL3 pin no effect exit SLEEP state 010：shutdown function：If PWRCTRL3 pin effect shutdown PMIC 011：restart function: If PWRCTRL3 pin effect restart PMIC 100：voltage regulator function：If PWRCTRL3 pin effect then turn the power supply of group n to the value of the XX_SLP_VSEL , If PWRCTRL3 pin no effect then turn the power supply of group n to the value of the XX_ON_VSEL (Note: The XX_VSEL_CTR_SEL register must be reset before PWRCTRL3_FUN exits the voltage select function) 101：GPIO function.

VSEL_CTR_SEL0

Address: Operational Base + offset (0x64)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	BUCK2_DVS_CTR_SEL BUCK2_DVS_CTR_SEL: Power is controlled by the PWRCRTL(1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
5:4	RW	0x0	BUCK2_VSEL_CTR_SEL BUCK2_VSEL_CTR_SEL: 00：no effect 01：controlled by PWRCTRL1:（the PWRCTRL1 signal control O_BUCK2_VSEL select BUCK2_ON_VSEL or BUCK2_SLP_VSEL ,and O_ BUCK2_EN select BUCK2_EN or BUCK2_SLP_EN） 10：controlled by PWRCTRL2:（the PWRCTRL2 signal control O_BUCK2_VSEL select BUCK2_ON_VSEL or BUCK2_SLP_VSEL ,and O_ BUCK2_EN select BUCK2_EN or BUCK2_SLP_EN） 11：controlled by PWRCTRL3:（the S PWRCTRL3 signal control O_BUCK2_VSEL select BUCK2_ON_VSEL or BUCK2_SLP_VSEL ,and O_ BUCK2_EN select BUCK2_EN or BUCK2_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN
3:2	RW	0x0	BUCK1_DVS_CTR_SEL BUCK1_DVS_CTR_SEL: Power is controlled by the PWRCRTL (1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
1:0	RW	0x0	BUCK1_VSEL_CTR_SEL BUCK1_ VSEL _CTR_SEL: 00：no effect 01：controlled by PWRCTRL1:（the PWRCTRL1 signal control O_BUCK1_VSEL select BUCK1_ON_VSEL or BUCK1_SLP_VSEL ,and O_ BUCK1_EN select BUCK1_EN or BUCK1_SLP_EN） 10：controlled by PWRCTRL2:（the PWRCTRL2 signal control O_BUCK1_VSEL select BUCK1_ON_VSEL or BUCK1_SLP_VSEL ,and O_ BUCK1_EN select BUCK1_EN or BUCK1_SLP_EN） 11：controlled by PWRCTRL3:（the S PWRCTRL3 signal control O_BUCK1_VSEL select BUCK1_ON_VSEL or BUCK1_SLP_VSEL ,and O_ BUCK1_EN select BUCK1_EN or BUCK1_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN

VSEL _CTR_SEL1

Address: Operational Base + offset (0x65)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	BUCK4_DVS_CTR_SEL BUCK4_DVS_CTR_SEL: Power is controlled by the PWRCRTL (1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
5:4	RW	0x0	BUCK4_VSEL_CTR_SEL BUCK4_ VSEL _CTR_SEL: 00：no effect 01：controlled by PWRCTRL1:（the PWRCTRL1 signal control O_BUCK4_VSEL select BUCK4_ON_VSEL or BUCK4_SLP_VSEL ,and O_ BUCK4_EN select BUCK4_EN or BUCK4_SLP_EN） 10：controlled by PWRCTRL2:（the PWRCTRL2 signal control O_BUCK4_VSEL select BUCK4_ON_VSEL or BUCK4_SLP_VSEL ,and O_ BUCK4_EN select BUCK4_EN or BUCK4_SLP_EN） 11：controlled by PWRCTRL3:（the S PWRCTRL3 signal control O_BUCK4_VSEL select BUCK4_ON_VSEL or BUCK4_SLP_VSEL ,and O_ BUCK4_EN select BUCK4_EN or BUCK2_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN \
3:2	RW	0x0	BUCK3_DVS_CTR_SEL BUCK3_DVS_CTR_SEL: Power is controlled by the PWRCRTL (1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
1:0	RW	0x0	BUCK3_VSEL_CTR_SEL BUCK3_ VSEL _CTR_SEL: 00：no effect 01：controlled by PWRCTRL1:（the PWRCTRL1 signal control O_BUCK3_VSEL select BUCK3_ON_VSEL or BUCK3_SLP_VSEL ,and O_ BUCK3_EN select BUCK3_EN or BUCK3_SLP_EN） 10：controlled by PWRCTRL2:（the PWRCTRL2 signal control O_BUCK3_VSEL select BUCK3_ON_VSEL or BUCK3_SLP_VSEL ,and O_ BUCK3_EN select BUCK3_EN or BUCK3_SLP_EN） 11：controlled by PWRCTRL3:（the S PWRCTRL3 signal control O_BUCK3_VSEL select BUCK3_ON_VSEL or BUCK3_SLP_VSEL ,and O_ BUCK3_EN select BUCK3_EN or BUCK3_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN

VSEL_CTR_SEL2

Address: Operational Base + offset (0x66)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	BUCK6_DVS_CTR_SEL BUCK6_DVS_CTR_SEL: Power is controlled by the PWRCRTL (1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
5:4	RW	0x0	BUCK6_VSEL_CTR_SEL BUCK6_ VSEL _CTR_SEL: 00：no effect 01：controlled by PWRCTRL1:（the PWRCTRL1 signal control O_BUCK6_VSEL select BUCK6_ON_VSEL or BUCK6_SLP_VSEL ,and O_ BUCK6_EN select BUCK6_EN or BUCK6_SLP_EN） 10：controlled by PWRCTRL2:（the PWRCTRL2 signal control O_BUCK6_VSEL select BUCK6_ON_VSEL or BUCK6_SLP_VSEL ,and O_ BUCK6_EN select BUCK6_EN or BUCK6_SLP_EN） 11：controlled by PWRCTRL3:（the S PWRCTRL3 signal control O_BUCK6_VSEL select BUCK6_ON_VSEL or BUCK6_SLP_VSEL ,and O_ BUCK6_EN select BUCK6_EN or BUCK6_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN
3:2	RW	0x0	BUCK5_DVS_CTR_SEL BUCK5_DVS_CTR_SEL: Power is controlled by the PWRCRTL (1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
1:0	RW	0x0	BUCK5_VSEL_CTR_SEL BUCK5_VSEL_CTR_SEL: 00：no effect 01：controlled by PWRCTRL1:（the PWRCTRL1 signal control O_BUCK5_VSEL select BUCK5_ON_VSEL or BUCK5_SLP_VSEL ,and O_ BUCK5_EN select BUCK5_EN or BUCK5_SLP_EN） 10：controlled by PWRCTRL2:（the PWRCTRL2 signal control O_BUCK5_VSEL select BUCK5_ON_VSEL or BUCK5_SLP_VSEL ,and O_ BUCK5_EN select BUCK5_EN or BUCK5_SLP_EN） 11：controlled by PWRCTRL3:（the S PWRCTRL3 signal control O_BUCK5_VSEL select BUCK5_ON_VSEL or BUCK5_SLP_VSEL ,and O_ BUCK5_EN select BUCK5_EN or BUCK5_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN

VSEL_CTR_SEL3

Address: Operational Base + offset (0x67)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	BUCK8_DVS_CTR_SEL BUCK8_DVS_CTR_SEL: Power is controlled by the PWRCRTL (1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
5:4	RW	0x0	BUCK8_VSEL_CTR_SEL BUCK8_VSEL_CTR_SEL: 00：no effect 01：controlled by PWRCTRL1:（the PWRCTRL1 signal control O_BUCK8_VSEL select BUCK8_ON_VSEL or BUCK8_SLP_VSEL ,and O_ BUCK8_EN select BUCK8_EN or BUCK8_SLP_EN） 10：controlled by PWRCTRL2:（the PWRCTRL2 signal control O_BUCK8_VSEL select BUCK8_ON_VSEL or BUCK8_SLP_VSEL ,and O_ BUCK8_EN select BUCK8_EN or BUCK8_SLP_EN） 11：controlled by PWRCTRL3:（the S PWRCTRL3 signal control O_BUCK8_VSEL select BUCK8_ON_VSEL or BUCK8_SLP_VSEL ,and O_ BUCK8_EN select BUCK8_EN or BUCK8_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN
3:2	RW	0x0	BUCK7_DVS_CTR_SEL BUCK7_DVS_CTR_SEL: Power is controlled by the PWRCRTL (1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
1:0	RW	0x0	BUCK7_VSEL_CTR_SEL BUCK7_VSE _CTR_SEL: 00：no effect 01：controlled by PWRCTRL1:（the PWRCTRL1 signal control O_BUCK7_VSEL select BUCK7_ON_VSEL or BUCK7_SLP_VSEL ,and O_ BUCK7_EN select BUCK7_EN or BUCK7_SLP_EN） 10：controlled by PWRCTRL2:（the PWRCTRL2 signal control O_BUCK7_VSEL select BUCK7_ON_VSEL or BUCK7_SLP_VSEL ,and O_ BUCK7_EN select BUCK7_EN or BUCK7_SLP_EN） 11：controlled by PWRCTRL3:（the S PWRCTRL3 signal control O_BUCK7_VSEL select BUCK7_ON_VSEL or BUCK7_SLP_VSEL ,and O_ BUCK7_EN select BUCK7_EN or BUCK7_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN

VSEL_CTR_SEL4

Address: Operational Base + offset (0x68)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	BUCK10_DVS_CTR_SEL BUCK10_DVS_CTR_SEL: Power is controlled by the PWRCRTL (1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
5:4	RW	0x0	BUCK10_VSEL_CTR_SEL BUCK10_VSEL_CTR_SEL: 00：no effect 01：controlled by PWRCTRL1:（the PWRCTRL1 signal control O_BUCK10_VSEL select BUCK10_ON_VSEL or BUCK10_SLP_VSEL ,and O_ BUCK10_EN select BUCK10_EN or BUCK10_SLP_EN） 10：controlled by PWRCTRL2:（the PWRCTRL2 signal control O_BUCK10_VSEL select BUCK10_ON_VSEL or BUCK10_SLP_VSEL ,and O_ BUCK10_EN select BUCK10_EN or BUCK10_SLP_EN） 11：controlled by PWRCTRL3:（the S PWRCTRL3 signal control O_BUCK10_VSEL select BUCK10_ON_VSEL or BUCK10_SLP_VSEL ,and O_ BUCK10_EN select BUCK10_EN or BUCK10_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN
3:2	RW	0x0	BUCK9_DVS_CTR_SEL BUCK9_DVS_CTR_SEL: Power is controlled by the PWRCRTL (1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
1:0	RW	0x0	BUCK9_VSEL_CTR_SEL BUCK9_VSEL_CTR_SEL: 00：no effect 01：controlled by PWRCTRL1:（the PWRCTRL1 signal control O_BUCK9_VSEL select BUCK9_ON_VSEL or BUCK9_SLP_VSEL ,and O_ BUCK9_EN select BUCK9_EN or BUCK9_SLP_EN） 10：controlled by PWRCTRL2:（the PWRCTRL2 signal control O_BUCK9_VSEL select BUCK9_ON_VSEL or BUCK9_SLP_VSEL ,and O_ BUCK9_EN select BUCK9_EN or BUCK9_SLP_EN） 11：controlled by PWRCTRL3:（the S PWRCTRL3 signal control O_BUCK9_VSEL select BUCK9_ON_VSEL or BUCK9_SLP_VSEL ,and O_ BUCK9_EN select BUCK9_EN or BUCK9_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN

VSEL_CTR_SEL5

Address: Operational Base + offset (0x69)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	NLDO2_DVS_CTR_SEL NLDO2_DVS_CTR_SEL: Power is controlled by the PWRCRTL (1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
5:4	RW	0x0	NLDO2_VSEL_CTR_SEL NLDO2_VSEL_CTR_SEL: 00：no effect 01：controlled by PWRCRTL:（the PWRCRTL1 signal control O_ NLDO2_VSEL select NLDO2_ON_VSEL or NLDO2_SLP_VSEL ,and O_ NLDO2_EN select NLDO2_EN or NLDO2_SLP_EN） 10：controlled by PWRCRTL2:（the PWRCRTL2 signal control O_ NLDO2_VSEL select O_ NLDO2_VSEL or NLDO2_SLP_VSEL ,and O_ NLDO2_EN select NLDO2_EN or NLDO2_SLP_EN） 11：controlled by PWRCRTL3:（the PWRCRTL3 signal control O_ NLDO2_VSEL select NLDO2_ON_VSEL or NLDO2_SLP_VSEL ,and O_ NLDO2_EN select NLDO2_EN or NLDO2_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN
3:2	RW	0x0	NLDO1_DVS_CTR_SEL NLDO1_DVS_CTR_SEL: Power is controlled by the PWRCRTL(1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
1:0	RW	0x0	NLDO1_VSEL_CTR_SEL NLDO1_VSEL_CTR_SEL: 00：no effect 01：controlled by PWRCRTL1:（the PWRCRTL1 signal control O_ NLDO1_VSEL select NLDO1_ON_VSEL or NLDO1_SLP_VSEL ,and O_ NLDO1_EN select NLDO1_EN or NLDO1_SLP_EN） 10：controlled by PWRCRTL2:（the PWRCRTL2 signal control O_ NLDO1_VSEL select O_ NLDO1_VSEL or NLDO1_SLP_VSEL ,and O_ NLDO1_EN select NLDO1_EN or NLDO1_SLP_EN） 11：controlled by PWRCRTL3:（the PWRCRTL3 signal control O_ NLDO1_VSEL select NLDO1_ON_VSEL or NLDO1_SLP_VSEL ,and O_ NLDO1_EN select NLDO1_EN or NLDO1_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN

DVS_CTRL_SEL0

Address: Operational Base + offset (0x6a)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	NLDO4_DVS_CTR_SEL NLDO4_DVS_CTR_SEL: Power is controlled by the PWRCRTL (1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
5:4	RW	0x0	NLDO4_VSEL_CTR_SEL NLDO4_VSEL_CTR_SEL: 00：no effect 01：controlled by PWRCRTL1:（the PWRCRTL1 signal control O_ NLDO4_VSEL select NLDO4_ON_VSEL or NLDO4_SLP_VSEL ,and O_ NLDO4_EN select NLDO4_EN or NLDO4_SLP_EN） 10：controlled by PWRCRTL2:（the PWRCRTL2 signal control O_ NLDO4_VSEL select O_ NLDO4_VSEL or NLDO4_SLP_VSEL ,and O_ NLDO4_EN select NLDO4_EN or NLDO4_SLP_EN） 11：controlled by PWRCRTL3:（the PWRCRTL3 signal control O_ NLDO4_VSEL select NLDO4_ON_VSEL or NLDO4_SLP_VSEL ,and O_ NLDO4_EN select NLDO4_EN or NLDO4_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN
3:2	RW	0x0	NLDO3_DVS_CTR_SEL NLDO3_DVS_CTR_SEL: Power is controlled by the PWRCRTL (1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
1:0	RW	0x0	NLDO3_VSEL_CTR_SEL NLDO3_VSEL_CTR_SEL: 00：no effect 01：controlled by PWRCRTL1:（the PWRCRTL1 signal control O_ NLDO3_VSEL select NLDO3_ON_VSEL or NLDO3_SLP_VSEL ,and O_ NLDO1_EN select NLDO3_EN or NLDO3_SLP_EN） 10：controlled by PWRCRTL2:（the PWRCRTL2 signal control O_ NLDO3_VSEL select O_ NLDO3_VSEL or NLDO3_SLP_VSEL ,and O_ NLDO3_EN select NLDO3_EN or NLDO3_SLP_EN） 11：controlled by PWRCRTL3:（the PWRCRTL3 signal control O_ NLDO3_VSEL select NLDO3_ON_VSEL or NLDO3_SLP_VSEL ,and O_ NLDO3_EN select NLDO3_EN or NLDO3_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN

DVS_CTRL_SEL1

Address: Operational Base + offset (0x6b)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	RESV RESV:Reserve
3:2	RW	0x0	NLDO5_DVS_CTR_SEL NLDO5_DVS_CTR_SEL: Power is controlled by the PWRCRTL (1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
1:0	RW	0x0	NLDO5_VSEL_CTR_SEL NLDO5_VSEL_CTR_SEL: 00：no effect 01：controlled by PWRCRTL1:（the PWRCRTL1 signal control O_ NLDO5_VSEL select NLDO5_ON_VSEL or NLDO5_SLP_VSEL ,and O_ NLDO5_EN select NLDO5_EN or NLDO5_SLP_EN） 10：controlled by PWRCRTL2:（the PWRCRTL2 signal control O_ NLDO5_VSEL select O_ NLDO5_VSEL or NLDO5_SLP_VSEL ,and O_ NLDO5_EN select NLDO5_EN or NLDO5_SLP_EN） 11：controlled by PWRCRTL3:（the PWRCRTL3 signal control O_ NLDO5_VSEL select NLDO5_ON_VSEL or NLDO5_SLP_VSEL ,and O_ NLDO5_EN select NLDO5_EN or NLDO5_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN

DVS_CTRL_SEL2

Address: Operational Base + offset (0x6c)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	PLDO2_DVS_CTR_SEL PLDO2_DVS_CTR_SEL: Power is controlled by the PWRCRTL (1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
5:4	RW	0x0	PLDO2_VSEL_CTR_SEL PLDO2_VSEL_CTR_SEL: 00：no effect 01：controlled by PWRCRTL1:（the PWRCRTL1 signal control O_ PLD02_VSEL select PLDO2_ON_VSEL or PLDO2_SLP_VSEL ,and O_ PLDO2_EN select PLDO2_EN or PLDO2_SLP_EN） 10：controlled by PWRCRTL2:（the PWRCRTL2 signal control O_ PLDO2_VSEL select PLDO2_ON_VSEL or PLDO2_SLP_VSEL ,and O_ PLDO2_EN select PLDO2_EN or PLDO2_SLP_EN） 11：controlled by PWRCRTL3:（the PWRCRTL3 signal control O_ PLDO2_VSEL select PLDO2_ON_VSEL or PLDO2_SLP_VSEL ,and O_ PLDO2_EN select PLDO2_EN or PLDO2_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN
3:2	RW	0x0	PLDO1_DVS_CTR_SEL PLDO1_DVS_CTR_SEL: Power is controlled by the PWRCRTL (1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
1:0	RW	0x0	PLDO1_VSEL_CTR_SEL PLDO1_VSEL_CTR_SEL: 00：no effect 01：controlled by PWRCRTL1:（the PWRCRTL1 signal control O_ PLD01_VSEL select PLDO1_ON_VSEL or PLDO1_SLP_VSEL ,and O_ PLDO1_EN select PLDO1_EN or PLDO1_SLP_EN） 10：controlled by PWRCRTL2:（the PWRCRTL2 signal control O_ PLDO1_VSEL select PLDO1_ON_VSEL or PLDO1_SLP_VSEL ,and O_ PLDO1_EN select PLDO1_EN or PLDO1_SLP_EN） 11：controlled by PWRCRTL3:（the PWRCRTL3 signal control O_ PLDO1_VSEL select PLDO1_ON_VSEL or PLDO1_SLP_VSEL ,and O_ PLDO1_EN select PLDO1_EN or PLDO1_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN

DVS_CTRL_SEL3

Address: Operational Base + offset (0x6d)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	PLDO4_DVS_CTR_SEL PLDO4_DVS_CTR_SEL: Power is controlled by the PWRCRTL (1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
5:4	RW	0x0	PLDO4_VSEL_CTR_SEL PLDO4_VSEL_CTR_SEL: 00：no effect 01：controlled by PWRCRTL1:（the PWRCRTL1 signal control O_ PLD04_VSEL select PLDO4_ON_VSEL or PLDO4_SLP_VSEL ,and O_ PLDO4_EN select PLDO4_EN or PLDO4_SLP_EN） 10：controlled by PWRCRTL2:（the PWRCRTL2 signal control O_ PLDO4_VSEL select PLDO4_ON_VSEL or PLDO4_SLP_VSEL ,and O_ PLDO4_EN select PLDO4_EN or PLDO4_SLP_EN） 11：controlled by PWRCRTL3:（the PWRCRTL3 signal control O_ PLDO4_VSEL select PLDO4_ON_VSEL or PLDO4_SLP_VSEL ,and O_ PLDO4_EN select PLDO4_EN or PLDO4_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN
3:2	RW	0x0	PLDO3_DVS_CTR_SEL PLDO3_DVS_CTR_SEL: Power is controlled by the PWRCRTL (1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
1:0	RW	0x0	PLDO3_VSEL_CTR_SEL PLDO3_VSEL_CTR_SEL: 00：no effect 01：controlled by PWRCRTL1:（the PWRCRTL1 signal control O_ PLD03_VSEL select PLDO3_ON_VSEL or PLDO3_SLP_VSEL ,and O_ PLDO3_EN select PLDO3_EN or PLDO3_SLP_EN） 10：controlled by PWRCRTL2:（the PWRCRTL2 signal control O_ PLDO3_VSEL select PLDO3_ON_VSEL or PLDO3_SLP_VSEL ,and O_ PLDO3_EN select PLDO3_EN or PLDO3_SLP_EN） 11：controlled by PWRCRTL3:（the PWRCRTL3 signal control O_ PLDO3_VSEL select PLDO3_ON_VSEL or PLDO3_SLP_VSEL ,and O_ PLDO3_EN select PLDO3_EN or PLDO3_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN

DVS_CTRL_SEL4

Address: Operational Base + offset (0x6e)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	PLDO6_DVS_CTR_SEL PLDO6_DVS_CTR_SEL: Power is controlled by the PWRCRTL (1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
5:4	RW	0x0	PLDO6_VSEL_CTR_SEL PLDO6_VSEL_CTR_SEL: 00：no effect 01：controlled by PWRCRTL1:（the PWRCRTL1 signal control O_ PLD02_VSEL select PLDO6_ON_VSEL or PLDO6_SLP_VSEL ,and O_ PLDO2_EN select PLDO6_EN or PLDO6_SLP_EN） 10：controlled by PWRCRTL2:（the PWRCRTL2 signal control O_ PLDO6_VSEL select PLDO6_ON_VSEL or PLDO6_SLP_VSEL ,and O_ PLDO6_EN select PLDO6_EN or PLDO6_SLP_EN） 11：controlled by PWRCRTL3:（the PWRCRTL3 signal control O_ PLDO6_VSEL select PLDO6_ON_VSEL or PLDO6_SLP_VSEL ,and O_ PLDO6_EN select PLDO6_EN or PLDO6_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN
3:2	RW	0x0	PLDO5_DVS_CTR_SEL PLDO5_DVS_CTR_SEL: Power is controlled by the PWRCRTL (1~3) pin 00：no effect: write register to adjust the voltage 01：controlled by DVS_START1:write register cannot to adjust the voltage, except DVS_START1 write "1" 10：controlled by DVS_START2:write register cannot to adjust the voltage, except DVS_START2 write "1" 11：controlled by DVS_START3:write register cannot to adjust the voltage, except DVS_START3 write "1"

Bit	Attr	Reset Value	Description
1:0	RW	0x0	PLDO5_VSEL_CTR_SEL PLDO5_VSEL_CTR_SEL: 00：no effect 01：controlled by PWRCRTL1:（the PWRCRTL1 signal control O_ PLD05_VSEL select PLDO5_ON_VSEL or PLDO5_SLP_VSEL ,and O_ PLDO5_EN select PLDO5_EN or PLDO5_SLP_EN） 10：controlled by PWRCRTL2:（the PWRCRTL2 signal control O_ PLDO5_VSEL select PLDO5_ON_VSEL or PLDO5_SLP_VSEL ,and O_ PLDO5_EN select PLDO5_EN or PLDO5_SLP_EN） 11：controlled by PWRCRTL3:（the PWRCRTL3 signal control O_ PLDO5_VSEL select PLDO5_ON_VSEL or PLDO5_SLP_VSEL ,and O_ PLDO5_EN select PLDO5_EN or PLDO5_SLP_EN） NOTE：Regardless of which pin the selection is controlled by, as soon as you enter SLEEP mode, all channels O_XX_VSEL are cut to SLP_VSEL ,the same goes for O_XX_EN

DVS_START_CTRL

Address: Operational Base + offset (0x70)

Bit	Attr	Reset Value	Description
7:4	RW	0x0	RESV RESV:Reserve
3	RW	0x0	DVS_READ_DATA DVS_READ_DATA: 0: When DVS_START does not write 1, the read XX_ON_VSEL register value is the newly written value; 1: When DVS_START does not write 1, the read XX_ON_VSEL register value is the code value corresponding to the actual voltage
2	RW	0x0	DVS_START3 DVS_START3: This bit writes 1, then the synchronous DVS voltage regulator is configured as the power supply of this group
1	RW	0x0	DVS_START2 DVS_START2: This bit writes 1, then the synchronous DVS voltage regulator is configured as the power supply of this group
0	RW	0x0	DVS_START1 DVS_START1: This bit writes 1, then the synchronous DVS voltage regulator is configured as the power supply of this group

PWRCTRL_GPIO

Address: Operational Base + offset (0x71)

Bit	Attr	Reset Value	Description
7	RW	0x0	RESV RESV:Reserve
6	RW	0x0	PWRCTRL3_DATA PWRCTRL3_DATA: if PWRCTRL3 pin is GPIO function, it's the data bit
5	RW	0x0	PWRCTRL2 _DATA PWRCTRL2 _DATA: if PWRCTRL2 pin is GPIO function, it's the data bit
4	RW	0x0	SLP1_DATA SLP1_DATA: if PWRCTRL1 pin is GPIO function, it's the data bit
3	RW	0x0	RESV RESV:Reserve
2	RW	0x0	PWRCTRL3_DR PWRCTRL3_DR: PWRCTRL3 pin used as GPIO 0：input 1：output
1	RW	0x0	PWRCTRL2_DR PWRCTRL2_DR: PWRCTRL2 pin used as GPIO 0：input 1：output
0	RW	0x0	PWRCTRL1_DR PWRCTRL1_DR: PWRCTRL1 pin used as GPIO 0：input 1：output

SYS_CFG3
Address: Operational Base + offset (0x72)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RST_FUN RST_FUN: 00：restart PMU 01： Reset all the power off reset registers, forcing the state to switch to ACTIVE mode 1X： Reset all the power off reset registers, forcing the state to switch to ACTIVE mode, and simultaneously pull down the RESETB PIN for 5mS before releasing
5	RW	0x0	DEV_RST DEV_RST: Write 1 will Reset PMIC，the reset mode is determined by RST_FUN (RST_FUN: two ways to trigger reset mode ：1）DEV_RST write 1；2）PWRCTRL PIN effect and SLP_FUN=011; 3)RESETB low
4:2	RW	0x0	RESV RESV:Reserve
1	RW	0x0	SLAVE_RESTART_FUN SLAVE_RESTART_FUN: 1:When the slave chip goes through a shutdown process, it will automatically trigger a restart (the intermediate delay is 500ms) 0:no effect。
0	RW	0x0	DEV_OFF DEV_OFF: Write 1 will start an ACTIVE to OFF or SLEEP to OFF device state transition (switch-off event). This bit is cleared in OFF state.

WDT_REG

Address: Operational Base + offset (0x73)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	RESV RESV:Reserve
4	RW	0x0	WDT_ACT WDT_ACT: 0:only send interrupt；1：restart
3	RW	0x0	WDT_EN WDT_EN: watchdog enable 0:disable 1；enable
2:0	RW	0x0	WDT_SET WDT_SET：the time of watchdog set： 000：50ms；001：100ms；010：500ms； 011：resve：100：2S；101：10s；110： 1min；111：10min； Four gears in the back(100~111) should to clear the interruption of WDT after set time , otherwise the time will advance 1S.

ON_SOURCE

Address: Operational Base + offset (0x74)

Bit	Attr	Reset Value	Description
7	RW	0x0	ON_PWRON ON_PWRON: PRESS PWRON to turn on PMU
6	RW	0x0	ON_VDC ON_VDC: DVC set high to turn on PMU
5	RW	0x0	ON_ABNORMAL ON_ABNORMAL: ABNORMAL to restart the PMU
4	RW	0x0	RESTART_RESETB RESTART_RESETB: PULL LOW the NRESPWRON PIN to restart the PMU
3	RW	0x0	RESTART_PWRON_LP RESTART_PWRON_LP: Long press PWRON to restart the PMU
2	RW	0x0	RESTART_ PWRCTRL RESTART_ PWRCTRL: PWRCTRL PIN ACTIVE to restart the PMU
1	RW	0x0	RESTART_DEV_RST RESTART_DEV_RST: DEV_RST Set 1 and ST_FUN=00 to restart the PMU
0	RW	0x0	RESTART_WDT RESTART_WDT: watchdog overflowed to restart the PMU

OFF_SOURCE

Address: Operational Base + offset (0x75)

Bit	Attr	Reset Value	Description
7	RW	0x0	OFF_ PWRCTRL OFF_ PWRCTRL: PWRCTRL PIN ACTIVE to turn off PMU
6	RW	0x0	VB_SYS_OV VB_SYS_OV: SYS OV to turn off PMU
5	RW	0x0	OFF_TSD OFF_TSD:TSD to turn off PMU
4	RW	0x0	OFF_SYNC OFF_SYNC: SYNC low level to turn off PMU
3	RW	0x0	OFF_DEV_OFF OFF_DEV_OFF: I2C write DEV_OFF to turn off PMU
2	RW	0x0	OFF_PWRON_LP OFF_PWRON_LP: long press PWRON to turn off PMU
1	RW	0x0	OFF_ABNORMAL OFF_ABNORMAL: ABNORMAL turn off
0	RW	0x0	OFF_VB_LO OFF_VB_LO: SYS Low (if VB_LO_ACT=0)to turn off PMU

PWRON_KEY

Address: Operational Base + offset (0x76)

Bit	Attr	Reset Value	Description
7	RW	0x0	PWRON_ON_TIME PWRON_ON_TIME: 0：500mS; 1:20mS
6	RW	0x0	PWRON_LP_ACT PWRON_LP_ACT: PWRON long press act 0: turn off (But if USB effective, then it will be start again) 1: turn off and then restart
5:4	RW	0x0	PWRON_LP_OFF_TIME PWRON_LP_OFF_TIME: PWRON long press time: 00: 6s, 01: 8s, 10: 10s, 11: 12s
3:2	RW	0x0	PWRON_LP_TM_SEL<1:0> PWRON_LP_TM_SEL<1:0>: PWRON long press interrupt time selection: 00: 0.5S 01:1S 10:1.5S 11:2S
1:0	RW	0x0	PWRON_DB_SEL<1:0> PWRON_DB_SEL<1:0>: PWRON interrupt rebound time selection: 00: 32uS 01:10mS 10:20mS 11:40mS

INT_STS0

Address: Operational Base + offset (0x77)

Bit	Attr	Reset Value	Description
7	RW	0x0	VB_LO_INT VB_LO_INT: VCC1 under voltage alarm event interrupt status.
6	RW	0x0	VDC_FALL_INT VDC_FALL_INT: VDC falling event interrupt
5	RW	0x0	VDC_RISE_INT VDC_RISE_INT: VDC rising event interrupt
4	RW	0x0	HOTDIE_INT HOTDIE_INT: Hot die event interrupt status.
3	RW	0x0	PWRON_LP_INT PWRON_LP_INT: PWRON PIN long press event interrupt status.
2	RW	0x0	PWRON_INT PWRON_INT: PWRON event interrupt status.
1	RW	0x0	PWRON_RISE_INT PWRON_RISE_INT: PWRON rising event interrupt
0	RW	0x0	PWRON_FALL_INT PWRON_FALL_INT: PWRON falling event interrupt

INT_MSK0

Address: Operational Base + offset (0x78)

Bit	Attr	Reset Value	Description
7	RW	0x0	VB_LO_IM VB_LO_IM: 0:Do not mask interrupt 1: mask VCC1 under voltage alarm event interrupt
6	RW	0x0	VDC_FALL_INT_IM VDC_FALL_INT_IM: 0:Do not mask interrupt 1: mask VDC falling event interrupt
5	RW	0x0	VDC_RISE_IM VDC_RISE_IM: 0:Do not mask interrupt 1: mask VDC rising event interrupt
4	RW	0x0	HOTDIE_IM HOTDIE_IM: 0:Do not mask interrupt 1: mask Hot die event interrupt
3	RW	0x0	PWRON_LP_IM PWRON_LP_IM: 0:Do not mask interrupt 1: mask PWRON PIN long press event interrupt
2	RW	0x0	PWRON_IM PWRON_IM: 0:Do not mask interrupt 1: mask PWRON event interrupt
1	RW	0x0	PWRON_RISE_INT_IM PWRON_RISE_INT_IM: 0:Do not mask interrupt 1: mask PWRON rising event interrupt
0	RW	0x0	PWRON_FALL_INT_IM PWRON_FALL_INT_IM: 0:Do not mask interrupt 1: mask PWRON falling event interrupt

INT_STS1

Address: Operational Base + offset (0x79)

Bit	Attr	Reset Value	Description
7	RW	0x0	WDT_INT WDT_INT: watch dog effect event interrupt
6	RW	0x0	PWRCTRL1_GPIO_INT PWRCTRL1_GPIO_INT: PWRCTRL1 pin used as GPIO event interrupt
5	RW	0x0	PWRCTRL2_GPIO_INT PWRCTRL2_GPIO_INT: PWRCTRL2 pin used as GPIO event interrupt
4	RW	0x0	PWRCTRL3_GPIO_INT PWRCTRL3_GPIO_INT: PWRCTRL3 pin used as GPIO event interrupt
3	RW	0x0	CRC_ERROR_INT CRC_ERROR_INT: CRC proofread error event interrupt
2:0	RW	0x0	RESV RESV:Reserve

INT_MSAK1

Address: Operational Base + offset (0x7a)

Bit	Attr	Reset Value	Description
7	RW	0x0	WDT_INT_ IM WDT_INT_ IM: 0:Do not mask interrupt 1: mask watch dog effect event interrupt
6	RW	0x0	PWRCTRL1_GPIO_ IM PWRCTRL1_GPIO_ IM: 0:Do not mask interrupt 1: mask PWRCTRL1 pin used as GPIO effect event interrupt
5	RW	0x0	PWRCTRL2_GPIO_ IM PWRCTRL2_GPIO_ IM: 0:Do not mask interrupt 1: mask PWRCTRL2 pin used as GPIO effect event interrupt
4	RW	0x0	PWRCTRL3_GPIO_ IM PWRCTRL3_GPIO_ IM: 0:Do not mask interrupt 1: mask PWRCTRL3 pin used as GPIO effect event interrupt
3	RW	0x0	CRC_ERROR_ IM CRC_ERROR_ IM: 0:Do not mask interrupt 1: mask CRC proofread error event interrupt
2:0	RW	0x0	RESV RESV:Reserve

GPIO_INT_CONFIG

Address: Operational Base + offset (0x7b)

Bit	Attr	Reset Value	Description
7:3	RW	0x0	RESV RESV:Reserve
2	RW	0x0	INT_FUNCTION INT_FUNCTION: 0:only send out interrupt 1：send out interrupt and get out SLEEP mode
1	RW	0x0	INT_POL INT_POL: INT pin polarity 0: active low 1: active high
0	RW	0x0	INT_FC_EN INT_FC_EN: interrupt watchdog function enable 0:disable 1:enable

DATA_REG0

Address: Operational Base + offset (0x7c)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	DATA_REG0 DATA_REG0:Data buffer

DATA_REG1
Address: Operational Base + offset (0x7d)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	DATA_REG1 DATA_REG1:Data buffer

DATA_REG2
Address: Operational Base + offset (0x7e)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	DATA_REG2 DATA_REG2:Data buffer

DATA_REG3
Address: Operational Base + offset (0x7f)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	DATA_REG3 DATA_REG3:Data buffer

DATA_REG4
Address: Operational Base + offset (0x80)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	DATA_REG4 DATA_REG4:Data buffer

DATA_REG5
Address: Operational Base + offset (0x81)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	DATA_REG5 DATA_REG5:Data buffer

DATA_REG6
Address: Operational Base + offset (0x82)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	DATA_REG6 DATA_REG6:Data buffer

DATA_REG7
Address: Operational Base + offset (0x83)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	DATA_REG7 DATA_REG7:Data buffer

DATA_REG8
Address: Operational Base + offset (0x84)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	DATA_REG8 DATA_REG8:Data buffer

DATA_REG9

Address: Operational Base + offset (0x85)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	DATA_REG9 DATA_REG9:Data buffer

DATA_REG10

Address: Operational Base + offset (0x86)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	DATA_REG10 DATA_REG10:Data buffer

DATA_REG11

Address: Operational Base + offset (0x87)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	DATA_REG11 DATA_REG11:Data buffer

DATA_REG12

Address: Operational Base + offset (0x88)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	DATA_REG12 DATA_REG12:Data buffer

DATA_REG13

Address: Operational Base + offset (0x89)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	DATA_REG13 DATA_REG13:Data buffer

DATA_REG14

Address: Operational Base + offset (0x8a)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	DATA_REG14 DATA_REG14:Data buffer

DATA_REG15

Address: Operational Base + offset (0x8b)

Bit	Attr	Reset Value	Description
7:0	RW	0x0	DATA_REG15 DATA_REG15:Data buffer

BUCK_SEQ_REG0

Address: Operational Base + offset (0XB2)

Bit	Attr	Reset Value	Description
7:6			RESV RESV:Reserve
5:0	RW	0x0	BUCK1_SEQ<5:0> BUCK1_SEQ<5:0>:BUCK1 turn off sequence 1MS for 1 step

BUCK_SEQ_REG1

Address: Operational Base + offset (0XB3)

Bit	Attr	Reset Value	Description
7:6			RESV RESV:Reserve
5:0	RW	0x0	BUCK2_SEQ<5:0> BUCK2_SEQ<5:0>:BUCK2 turn off sequence 1MS for 1 step

BUCK_SEQ_REG2

Address: Operational Base + offset (0XB4)

Bit	Attr	Reset Value	Description
7:6			RESV RESV:Reserve
5:0	RW	0x0	BUCK3_SEQ<5:0> BUCK3_SEQ<5:0>:BUCK3 turn off sequence 1MS for 1 step

BUCK_SEQ_REG3

Address: Operational Base + offset (0XB5)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	PLDO6_SEQ<5:4> PLDO6_SEQ<5:4>:PLDO6 turn off sequence 1MS for 1 step
5:0	RW	0x0	BUCK4_SEQ<5:0> BUCK4_SEQ<5:0>:BUCK4 turn off sequence 1MS for 1 step

BUCK_SEQ_REG4

Address: Operational Base + offset (0XB6)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	PLDO6_SEQ<3:2> PLDO6_SEQ<3:2>:PLDO6 turn off sequence 1MS for 1 step
5:0	RW	0x0	BUCK5_SEQ<5:0> BUCK5_SEQ<5:0>:BUCK5 turn off sequence 1MS for 1 step

BUCK_SEQ_REG5

Address: Operational Base + offset (0XB7)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	PLDO6_SEQ<1:0> PLDO6_SEQ<1:0>:PLDO6 turn off sequence 1MS for 1 step
5:0	RW	0x0	BUCK6_SEQ<5:0> BUCK6_SEQ<5:0>:BUCK6 turn off sequence 1MS for 1 step

BUCK_SEQ_REG6

Address: Operational Base + offset (0XB8)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	PLDO1_SEQ<5:4> PLDO1_SEQ<5:4>:PLDO1 turn off sequence 1MS for 1 step
5:0	RW	0x0	BUCK7_SEQ<5:0> BUCK7_SEQ<5:0>:BUCK7 turn off sequence 1MS for 1 step

BUCK_SEQ_REG7

Address: Operational Base + offset (0XB9)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	PLDO1_SEQ<3:2> PLDO1_SEQ<3:2>:PLDO1 turn off sequence 1MS for 1 step
5:0	RW	0x0	BUCK8_SEQ<5:0> BUCK8_SEQ<5:0>:BUCK8 turn off sequence 1MS for 1 step

BUCK_SEQ_REG8

Address: Operational Base + offset (0XBA)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	PLDO1_SEQ<1:0> PLDO1_SEQ<1:0>:PLDO1 turn off sequence 1MS for 1 step
5:0	RW	0x0	BUCK9_SEQ<5:0> BUCK9_SEQ<5:0>:BUCK9 turn off sequence 1MS for 1 step

BUCK_SEQ_REG9

Address: Operational Base + offset (0XBB)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	PLDO2_SEQ<5:4> PLDO2_SEQ<5:4>:PLDO2 turn off sequence 1MS for 1 step
5:0	RW	0x0	BUCK10_SEQ<5:0> BUCK10_SEQ<5:0>:BUCK10 turn off sequence 1MS for 1 step

BUCK_SEQ_REG10

Address: Operational Base + offset (0XBC)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	PLDO2_SEQ<3:2> PLDO2_SEQ<3:2>:PLDO2 turn off sequence 1MS for 1 step
5:0	RW	0x0	NLDO1_SEQ<5:0> NLDO1_SEQ<5:0>:NLDO1 turn off sequence 1MS for 1 step

BUCK_SEQ_REG11

Address: Operational Base + offset (0XBD)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	PLDO2_SEQ<1:0> PLDO2_SEQ<1:0>:PLDO2 turn off sequence 1MS for 1 step
5:0	RW	0x0	NLDO2_SEQ<5:0> NLDO2_SEQ<5:0>:NLDO2 turn off sequence 1MS for 1 step

BUCK_SEQ_REG12

Address: Operational Base + offset (0XBE)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	PLDO3_SEQ<5:4> PLDO3_SEQ<5:4>:PLDO3 turn off sequence 1MS for 1 step
5:0	RW	0x0	NLDO3_SEQ<5:0> NLDO3_SEQ<5:0>:NLDO3 turn off sequence 1MS for 1 step

BUCK_SEQ_REG13

Address: Operational Base + offset (0XBF)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	PLDO3_SEQ<3:2> PLDO3_SEQ<3:2>:PLDO3 turn off sequence 1MS for 1 step
5:0	RW	0x0	NLDO4_SEQ<5:0> NLDO4_SEQ<5:0>:NLDO4 turn off sequence 1MS for 1 step

BUCK_SEQ_REG14
Address: Operational Base + offset (0XC0)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	PLDO3_SEQ<1:0> PLDO3_SEQ<1:0>:PLDO3 turn off sequence 1MS for 1 step
5:0	RW	0x0	NLDO5_SEQ<5:0> NLDO5_SEQ<5:0>:NLDO5 turn off sequence 1MS for 1 step

BUCK_SEQ_REG15
Address: Operational Base + offset (0XC1)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV RESV:Reserve
5:0	RW	0x0	PLDO4_SEQ<5:0> PLDO4_SEQ<5:0>:PLDO4 turn off sequence 1MS for 1 step

BUCK_SEQ_REG16
Address: Operational Base + offset (0XC2)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV RESV:Reserve
5:0	RW	0x0	PLDO5_SEQ<5:0> PLDO5_SEQ<5:0>:PLDO5 turn off sequence 1MS for 1 step

BUCK_SEQ_REG17
Address: Operational Base + offset (0XC3)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV RESV:Reserve
5:0	RW	0x0	SESET<5:0> SESET<5:0>:PLDO4 turn off sequence 1MS for 1 step

BACKUP_REG7
Address: Operational Base + offset (0XDC)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	BUCK10_SET_SST BUCK10_SET_SST:BUCK10 soft start time 00:400uS 01:200uS 10:100uS 11:50uS
5:4	RW	0x0	BUCK9_SET_SST BUCK9_SET_SST:BUCK9 soft start time 00:400uS 01:200uS 10:100uS 11:50uS
3:2	RW	0x0	BUCK8_SET_SST BUCK8_SET_SST:BUCK8 soft start time 00:400uS 01:200uS 10:100uS 11:50uS
1:0	RW	0x0	BUCK7_SET_SST BUCK7_SET_SST:BUCK7 soft start time 00:400uS 01:200uS 10:100uS 11:50uS

BACKUP_REG6

Address: Operational Base + offset (0XE6)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	BUCK4_SET_SST BUCK4_SET_SST:BUCK4 soft start time 00:400uS 01:200uS 10:100uS 11:50uS
5:4	RW	0x0	BUCK3_SET_SST BUCK3_SET_SST:BUCK3 soft start time 00:400uS 01:200uS 10:100uS 11:50uS
3:2	RW	0x0	BUCK2_SET_SST BUCK2_SET_SST:BUCK2 soft start time 00:400uS 01:200uS 10:100uS 11:50uS
1:0	RW	0x0	BUCK1_SET_SST BUCK1_SET_SST:BUCK1 soft start time 00:400uS 01:200uS 10:100uS 11:50uS

BACKUP_REG5

Address: Operational Base + offset (0XE7)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	BUCK5_SET_SST BUCK5_SET_SST:BUCK4 soft start time 00:400uS 01:200uS 10:100uS 11:50uS
5:4	RW	0x0	RESV RESV:Reserve
3:2	RW	0x0	VCC14_UVSEL VCC14_UVSEL:VCC14 input threshold select 0:0.6v 1:0.8v 10:1.0v 11:1.2V
1:0	RW	0x0	VCC13_UVSEL VCC13_UVSEL:VCC13 input threshold select 0:0.6v 1:0.8v 10:1.0v 11:1.2V

BACKUP_REG1

Address: Operational Base + offset (0XE8)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK6_SET_SST BUCK6_SET_SST:BUCK4 soft start time 00:400uS 01:200uS 10:100uS 11:50uS
6:5	RW	0x0	RESV RESV:Reserve
4	RW	0x0	VBOVLOCK_DIS VBOVLOCK_DIS: After PMIC turn on, VBOV locked 0:enable 1:disable
3	RW	0x0	SYSOV_SEL SYSOV_SEL: VCCx OVP threshold 0:6V 1:5.6V
2			SPI_4WIRE SPI_4WIRE:SPI mode select 0:3wire; 1:4wire
1:0			RESV RESV:Reserve

BACKUP_REG2

Address: Operational Base + offset (0XE9)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK_DVS_FPWM_EN BUCK_DVS_FPWM_EN: when BUCK DVS ,then turn on FPWM function 1:enable 0:disable
6	RW	0x0	LDO_DVS_RLOAD_EN LDO_DVS_RLOAD_EN: when LDO DVS ,then turn on inter internal discharge resistance 1:enable 0:disable
5	RW	0x0	MISO_PAD_OE MISO_PAD_OE: Set MISO to output pin 1:enable 0:disable
4	RW	0x0	WDT_CLR_mask: MUST write them to "1" if want to change corresponding WDT_CLR bit, The WDT_CLR _MASK bits should be clear when WDT_CLR bits have been written.
3:1	RW	0x0	RESV RESV:Reserve
0	RW	0x0	WDT_CLR: Delayed WDT trigger 1:enable 0:disable Note: The delay time depends on the time set by the watchdog. As long as the Bit is written as 1 again within the set time, the watchdog trigger will be delayed again

BACKUP_REG3

Address: Operational Base + offset (0XEA)

Bit	Attr	Reset Value	Description
7:5	RW	0x0	RESV RESV:Reserve
4:3	RW	0x0	LDO_RATE<2:0> LDO_RATE<2:0>:Voltage change rate after DVS(2M clack) 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;
1	RW	0x0	BUCK10_RATE<2> BUCK10_RATE<2>:Voltage change rate after DVS(2M clack), 3BIT, BIT<1:0> at the 19 Register 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;
0	RW	0x0	BUCK9_RATE<2> BUCK9_RATE<2>: Voltage change rate after DVS(2M clack), 3BIT, BIT<1:0> at the 18 Register 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;

BACKUP_REG4
Address: Operational Base + offset (0XEB)

Bit	Attr	Reset Value	Description
7	RW	0x0	BUCK8_RATE<2> BUCK8_RATE<2>:Voltage change rate after DVS(2M clack), 3BIT, BIT<1:0> at the 17 Register 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;
6	RW	0x0	BUCK7_RATE<2> BUCK7_RATE<2>:Voltage change rate after DVS(2M clack), 3BIT, BIT<1:0> at the 16 Register 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;
5	RW	0x0	BUCK6_RATE<2> BUCK6_RATE<2>:Voltage change rate after DVS(2M clack), 3BIT, BIT<1:0> at the 15 Register 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;
4	RW	0x0	BUCK5_RATE<2> BUCK5_RATE<2>:Voltage change rate after DVS(2M clack), 3BIT, BIT<1:0> at the 14 Register 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;
3	RW	0x0	BUCK4_RATE<2> BUCK4_RATE<2>:Voltage change rate after DVS(2M clack), 3BIT, BIT<1:0> at the 13 Register 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;
2	RW	0x0	BUCK3_RATE<2> BUCK3_RATE<2>:Voltage change rate after DVS(2M clack), 3BIT, BIT<1:0> at the 12 Register 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;

1	RW	0x0	BUCK2_RATE<2> BUCK2_RATE<2>:Voltage change rate after DVS(2M clack), 3BIT, BIT<1:0> at the 11 Register 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;
0	RW	0x0	BUCK1_RATE<2> BUCK1_RATE<2>:Voltage change rate after DVS(2M clack), 3BIT, BIT<1:0> at the 10 Register 000: 4lsb/1clk;001: 2lsb/1clk;010:1lsb/1clk; 011:1lsb/2clk;100:1lsb/4clk;101: 1lsb/8clk; 110:1lsb/13clk;111:1lsb/32clk;

BUCK_RSERVE_REG3

Address: Operational Base + offset (0XFD)

Bit	Attr	Reset Value	Description
7:6	RW	0x0	RESV RESV:Reserve
5	RW	0x0	BUCK6_EX_RES_SET BUCK6_EX_RES_SET:BUCK6 external feedback resister enable. 0:Disable 1:Enable
4	RW	0x0	BUCK5_EX_RES_SET BUCK5_EX_RES_SET:BUCK5 external feedback resister enable. 0:Disable 1:Enable
3:2	RW	0x0	RESV RESV:Reserve
1	RW	0x0	BUCK2_EX_RES_SET BUCK2_EX_RES_SET:BUCK2 external feedback resister enable. 0:Disable 1:Enable
0	RW	0x0	BUCK1_EX_RES_SET BUCK1_EX_RES_SET:BUCK1 external feedback resister enable. 0:Disable 1:Enable

BUCK_RSERVE_REG4

Address: Operational Base + offset (0XFE)

Bit	Attr	Reset Value	Description
7:1	RW	0x0	RESV RESV:Reserve
0	RW	0x0	BUCK9_EX_RES_SET BUCK9_EX_RES_SET:BUCK9 external feedback resister enable. 0:Disable 1:Enable

Chapter 6 Thermal Management

6.1 Overview

For reliability and operability concerns, the absolute maximum junction temperature of RK806 has to be below 125℃.

Depending on the thermal mechanical design (Smartphone, Tablet, Personal Navigation Device, etc), the system thermal management software and the worst case thermal applications, the junction temperature might be exposed to higher values than those specified above.

Therefore, it is recommended to perform thermal simulations at device level (Smartphone, Tablet, Personal Navigation Device, etc) with the measured power of the worst case UC of the device.

6.2 Package Thermal Characteristics

Table 6-1 provides the thermal resistance characteristics for the package used on this device.

Table 6-1 Thermal Resistance Characteristics

PACKAGE (QFN7X7-68)	POWER(W)	θ_{JA}(℃/W)	θ_{JB}(℃/W)	θ_{JC}(℃/W)
RK806	2	21.99	12	6.58

Note: The testing PCB is based on 4 layers, 114mm x 76 mm, 1.6mm thickness, Ambient temperature is 85°C.

Table 6-2 SnPb Eutectic Process-Classification Temperatures (TC)

Package Thickness	Volume mms <350	Volume mms ≥350
<2.5 mm	235 ℃	220℃
≥2.5 mm	220 ℃	220℃

Table 6-3 Pb-Free Process-Classification Temperatures (TC)

Package Thickness	Volume mmcess-C	Volume mmcess-Class	Volume mmcess-Cl
<1.6 mm	260 ℃	260 ℃	260℃
1.6 mm-2.5 mm	260℃	250 ℃	245℃
>2.5 mm	250 ℃	245 ℃	245℃

Note 1:At the discretion of the device manufacturer, but not the board assembler/user, the maximum peak package body temperature (TP) can exceed the values specified in Tables 6-2or 6-3. The use of a higher Tp does not change the classification temperature (Tc).

Note 2: Package volume excludes external terminals (e.g., balls, bumps, lands, leads) and/or nonintegral heat sinks.

Note 3: The maximum component temperature reached during reflow depends on package thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD packages may still exist.

Note 4: Moisture sensitivity levels of components intended for use in a Pb-free assembly process shall be evaluated using the Pb-free classification temperatures and profiles defined in Tables 4.2 and 6-4, whether or not Pb-free.

Note 5: SMD packages classified to a give moisture sensitivity level by using Procedures or Criteria defined within any previous version of J-STD-020, JESD22-A112(rescinded),IPC-SM-786 (rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

Table 6-4 Classification Reflow Profiles

Profile Feature	**Sn-Pb Eutectic Assembly**	**Pb-Free Assembly**
Preheat & Soak Temperature min (T smin) Temperature max(Tsmax) Time (Tsmin to Tsmax)(ts)	 100℃ 150℃ 60-120 seconds	 150℃ 200℃ 60-120 seconds
Average ramp-up rate (Tsmax to Tp)	3 ℃ /second max.	3 ℃ /second max.
Liquidous temperature (TL) Time at liquidous (tL)	183 ℃60-150 seconds	217 ℃ 60-150 seconds
Peak package body temperature (Tp)*	See classification temp in Table 6-2	See classification temp in Table 6-3
Time(tp)* * within 5℃ of the specified classification temperature (Tc)	20** seconds	30** seconds
Average ramp-down rate (Tp to Tsmax)	6℃ /second max.	6 ℃ /second max.
Time 25 ℃ to peak temperature	6 minutes max.	8 minutes max.
*Tolerance for peak profile temperature (Tp) is defined as a supplier minimum and a user maximum. ** Tolerance for time at peak profile temperature (Tp) is defined as a supplier minimum and a user maximum.		

Note 1: All temperatures refer to the center of the package, measured on the package body surface that is facing up during assembly reflow(e.g.,ive-bug). If

parts are reflowed in other than the normal ive-bug assembly reflow orientation (i.e.,dead-bug), Tp shall be within ±2℃ of the live-bug Tp and still meet the Tc requirements, otherwise, the profile shall be adjusted to achieve the latter. To accurately measure actual peak package body temperatures refer to JEP140 for recommended thermocouple use.

Note 2: Reflow profiles in this document are for classification/preconditioning and are not meant to specify board assembly profiles. Actual board assembly

profiles should be developed based on specific process needs and board designs and should not exceed the parameters in Table 6-4.

For example, if Tc is 260 ℃and time Tp is 30 seconds, this means the following for the supplier and the user.

For a supplier. The peak temperature must be at least 260 ℃.The time above 255 C must be at least 30 seconds.

For a user: The peak temperature must not exceed 260 ℃. The time above 255 ℃C must not exceed 30 seconds.

Note 3: All components in the test load shall meet the classification profile requirements.

Note 4: SMD packages classified to a given moisture sensitivity level by using Procedures or Criteria defined within any previous version of ,J-STD-020

JESD22-A112 (rescinded), IPC-SM-786(rescinded) do not need to be reclassified to the current revision unless a change in classification level or a higher peak classification temperature is desired.

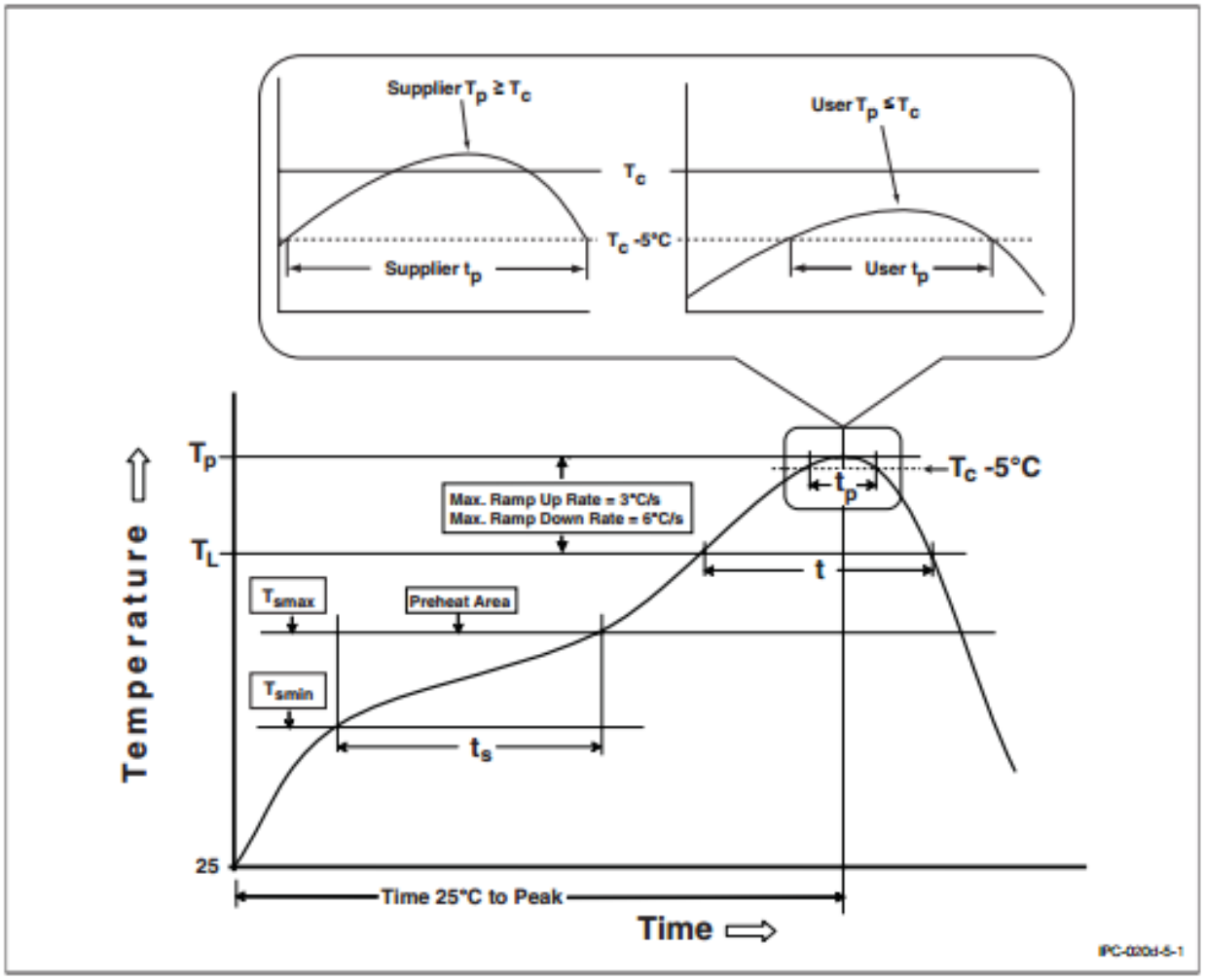


Figure 5-1 Classification Profile

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