

Operational Amplifier series



Low Noise Operational Amplifiers

BA14741F, BA14741FJ

● **General Description**

General-purpose BA14741 integrates four independent Op-Amps on a single chip. Especially, this series is suitable for any audio applications due to low noise and low distortion characteristics and is usable for other many applications by wide operating supply voltage range.

● **Features**

- High voltage gain
- Low input referred noise voltage
- low distortion
- Wide operating supply voltage

● **Application**

- Audio application
- Consumer electronics

● **Packages**

- SOP14
- SOP-J14

W(Typ.) x D(Typ.) x H(Max.)

- 8.70mm x 6.20mm x 1.71mm
- 8.65mm x 6.00mm x 1.65mm

● **Key Specification**

- Wide Operating Supply Voltage (split supply): $\pm 2.0V$ to $\pm 18.0V$
- High Slew Rate: $1V/\mu s$ (Typ.)
- Input Referred Noise Voltage: $2.0\mu V_{rms}$ (Typ.)
- Total Harmonic Distortion: 0.003% (Typ.)

● **Block Diagrams**

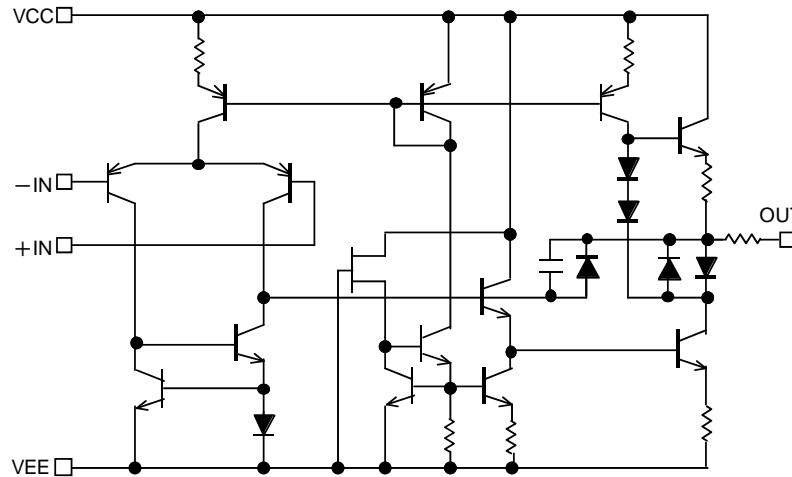
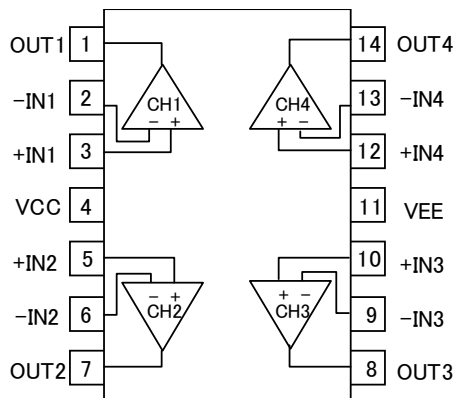


Figure 1. Simplified schematic

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

●Pin Configuration(TOP VIEW)

SOP14, SOP-J14



Package	
BA14741F	SOP14
BA14741FJ	SOP-J14

Pin No.	Symbol
1	OUT1
2	-IN1
3	+IN1
4	VCC
5	+IN2
6	-IN2
7	OUT2
8	OUT3
9	-IN3
10	+IN3
11	VEE
12	+IN4
13	-IN4
14	OUT4

●Ordering Information

B A 1 4 7 4 1 x x - E2

Part Number
BA14741

Package
F :SOP14
FJ :SOP-J14

Packaging and forming specification
E2: Embossed tape and reel
(SOP14/ SOP-J14)

●Line-up

Topr	Operating Supply Voltage (split supply)	Supply Current (Typ.)	Slew Rate (Typ.)	Package		Orderable Part Number
				SOP14	Reel of 2500	
-40°C~+85°C	±2.0V~±18.0V	3mA	1V/μs	SOP14	Reel of 2500	BA14741F-E2
				SOP-J14	Reel of 2500	BA14741FJ-E2

● Absolute Maximum Ratings (Ta=25°C)

OBA14741

Parameter	Symbol	Ratings	Unit	
Supply Voltage	VCC-VEE	+36	V	
Power dissipation	Pd	SOP14	450 ^{*1*3}	mW
		SOP-J14	820 ^{*2*3}	mW
Differential Input Voltage ^{*4}	Vid	VCC - VEE	V	
Input Common-mode Voltage Range	Vicm	VEE - VCC	V	
Operating Supply Voltage	Vopr	4 to 36 (±2 to ±18)	V	
Operating Temperature	Topr	-40 to +85	°C	
Storage Temperature	Tstg	-55 to +125	°C	
Maximum Junction Temperature	Tjmax	+125	°C	
Output Short Time ^{*5}	Ts	unlimited (only 1CH short)	Sec	

Note: Absolute maximum rating item indicates the condition which must not be exceeded.

Application of voltage in excess of absolute maximum rating or use out absolute maximum rated temperature environment may cause deterioration of characteristics.

*1 To use at temperature above Ta=25°C reduce 4.5mW/°C

*2 To use at temperature above Ta=25°C reduce 8.2mW/°C

*3 Mounted on a FR4 glass epoxy PCB(70mm×70mm×1.6mm).

*4 The voltage difference between inverting input and non-inverting input is the differential input voltage. Then input terminal voltage is set to more than VEE.

*5 To short Output to VCC or VEE, Limited within Pd.

● Electrical Characteristics

OBA14741 (Unless otherwise specified VCC=+15V, VEE=-15V, Ta=25°C)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Input Offset Voltage ^{*6}	Vio	-	1.0	5.0	mV	RS ≤ 10kΩ
Input Offset Current ^{*6}	Iio	-	10	50	nA	-
Input Bias Current ^{*7}	Ib	-	60	300	nA	-
Large Signal Voltage Gain	Av	20	100	-	V/mV	RL ≥ 2kΩ, OUT=±10V
Common-mode Rejection Ratio	CMRR	80	100	-	dB	-
Input Common-mode Voltage Range	Vicm	±12	±13.5	-	V	-
Power Supply Rejection Ratio	PSRR	80	100	-	dB	-
Supply Current	ICC	-	3.0	7.0	mA	RL=∞, All Op-Amps
Maximum Output Voltage	VOM	±10	±12.5	-	V	RL=2kΩ
Output Source Current	Isource	10	20	-	mA	Vin+=1V, Vin-=0V, OUT=0V
Output Sink Current	Isink	5	10	-	mA	Vin+=0V, Vin-=1V, OUT=0V
Slew Rate	SR	-	1.0	-	V/μs	Av=1, RL=2kΩ
Gain Bandwidth Product	GBW	-	2.2	-	MHz	f=100kHz
Unity Gain Frequency	fT	-	2.2	-	MHz	0dB cross frequency
Input Referred Noise Voltage	Vn	-	2.0	4.0	μVrms	RIAA, RS=2.2kΩ, 10Hz to 30kHz
		-	10	-	nV/√Hz	RIAA, RS=2.2kΩ, f=1kHz
Total Harmonic Distortion + Noise	THD+N	-	0.003	-	%	Av=20dB, RL=2kΩ, OUT=1Vrms f=1kHz, DIN-AUDIO
Channel Separation	CS	-	100	-	dB	f=1kHz, input referred

*6 Absolute value.

*7 Current direction: Since first input stage is composed with PNP transistor, input bias current flows out of IC.

Description of electrical characteristics

Described here are the terms of electric characteristics used in this datasheet. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacture's document or general document.

1. Absolute maximum ratings

Absolute maximum rating item indicates the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

1.1 Power supply voltage (VCC-VEE)

Indicates the maximum voltage that can be applied between the positive power supply terminal and negative power supply terminal without deterioration or destruction of characteristics of internal circuit.

1.2 Differential input voltage (V_{id})

Indicates the maximum voltage that can be applied between non-inverting terminal and inverting terminal without deterioration and destruction of characteristics of IC.

1.3 Input common-mode voltage range (V_{icm})

Indicates the maximum voltage that can be applied to non-inverting terminal and inverting terminal without deterioration or destruction of characteristics. Input common-mode voltage range of the maximum ratings not assures normal operation of IC. When normal operation of IC is desired, the input common-mode voltage of characteristics item must be followed.

1.4 Power dissipation (P_d)

Indicates the power that can be consumed by specified mounted board at the ambient temperature 25°C(normal temperature). As for package product, P_d is determined by the temperature that can be permitted by IC chip in the package (maximum junction temperature)and thermal resistance of the package.

2. Electrical characteristics item

2.1 Input offset voltage (V_{io})

Indicates the voltage difference between non-inverting terminal and inverting terminal. It can be translated into the input voltage difference required for setting the output voltage at 0 V .

2.2 Input offset current (I_{io})

Indicates the difference of input bias current between non-inverting terminal and inverting terminal.

2.3 Input bias current (I_b)

Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias current at non-inverting terminal and input bias current at inverting terminal.

2.4 Large signal voltage gain (A_v)

Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and Inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.

$$A_v = (\text{Output voltage fluctuation}) / (\text{Input offset fluctuation})$$

2.5 Common-mode rejection ratio (CMRR)

Indicates the ratio of fluctuation of input offset voltage when in-phase input voltage is changed. It is normally the fluctuation of DC.

$$\text{CMRR} = (\text{Change of Input common-mode voltage}) / (\text{Input offset fluctuation})$$

2.6 Input common-mode voltage range(V_{icm})

Indicates the input voltage range where IC operates normally.

2.7 Power supply rejection ratio (PSRR)

Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed. It is normally the fluctuation of DC. PSRR = (Change of power supply voltage) / (Input offset fluctuation)

2.8 Circuit current (I_{CC})

Indicates the IC current that flows under specified conditions and no-load steady status.

2.9 Maximum Output Voltage(V_{OM})

Indicates the voltage range that can be output by the IC under specified load condition. It is typically divided into maximum output voltage high and maximum output voltage low. maximum output voltage high indicates the upper limit of output voltage. maximum output voltage low indicates the lower limit.

2.10 Output source current/ output sink current (I_{source}/I_{sink})

The maximum current that can be output under specific output conditions, it is divided into output source current and output sink current. The output source current indicates the current flowing out of the IC, and the output sink current the current flowing into the IC.

2.11 Slew Rate (SR)

SR is a parameter that shows movement speed of operational amplifier. It indicates rate of variable output voltage as unit time.

2.12 Gain Band Width (GBW)

Indicates to multiply by the frequency and the gain where the voltage gain decreases 6dB/octave.

2.13 Unity gain frequency (f_T)

Indicates a frequency where the voltage gain of operational amplifier is 1.

2.14 Total harmonic distortion + Noise (THD+N)

Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

2.15 Input referred noise voltage (V_n)

Indicates a noise voltage generated inside the operational amplifier equivalent by ideal voltage source connected in series with input terminal.

2.16 Channel separation (CS)

Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

● Typical Performance Curves

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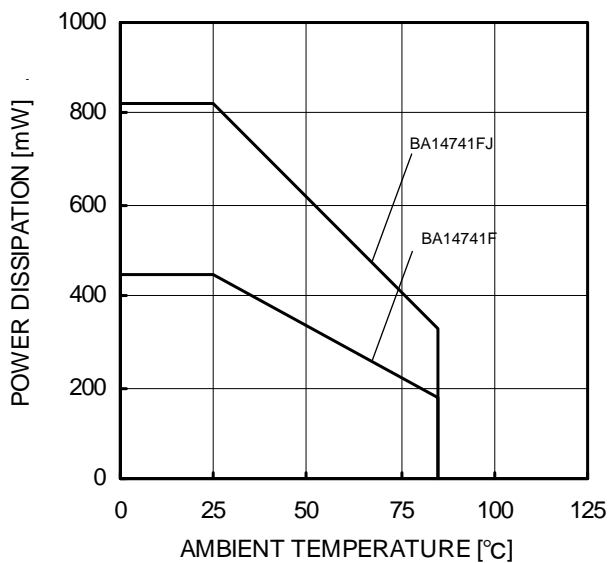


Figure 2.
Derating Curve

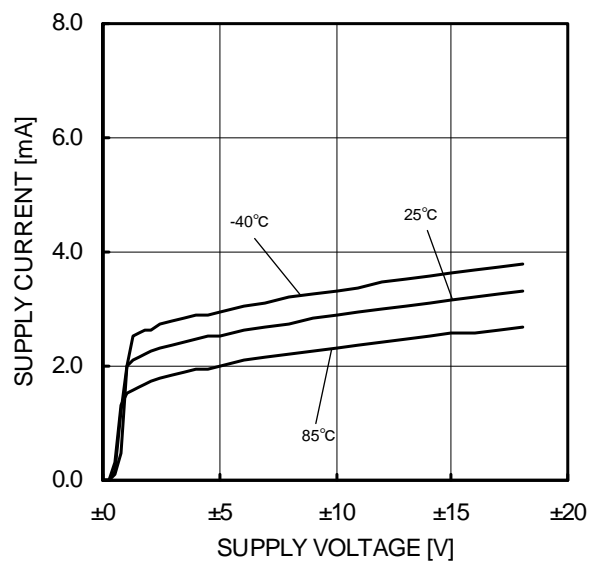


Figure 3.
Supply Current - Supply Voltage

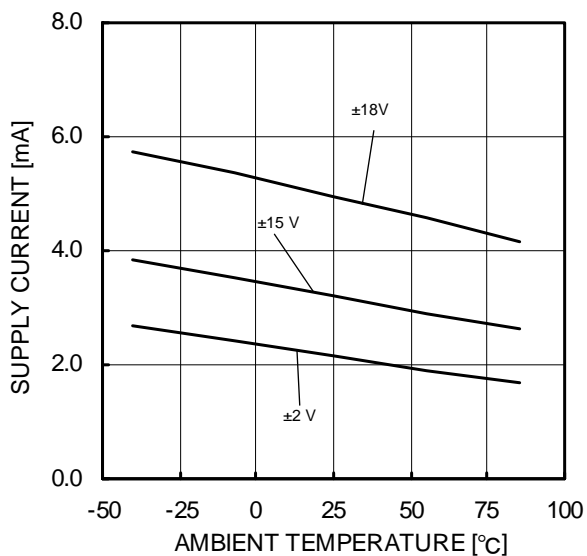


Figure 4.
Supply Current - Ambient Temperature

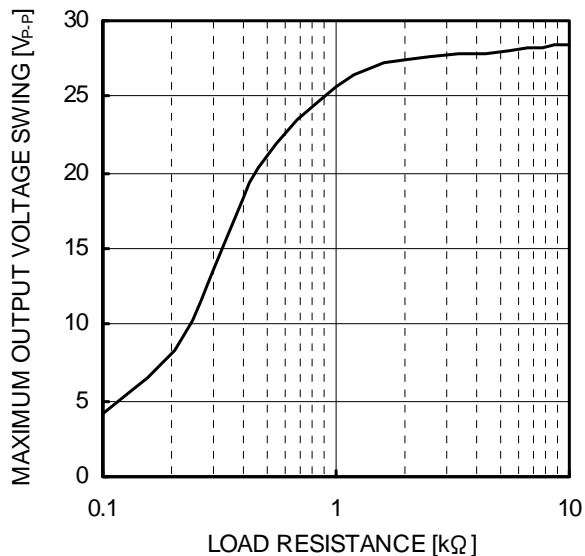


Figure 5.
Maximum Output Voltage Swing
- Load Resistance
(VCC/VEE=±15V/-15V, Ta=25°C)

(*)The above data is measurement value of typical sample, it is not guaranteed.

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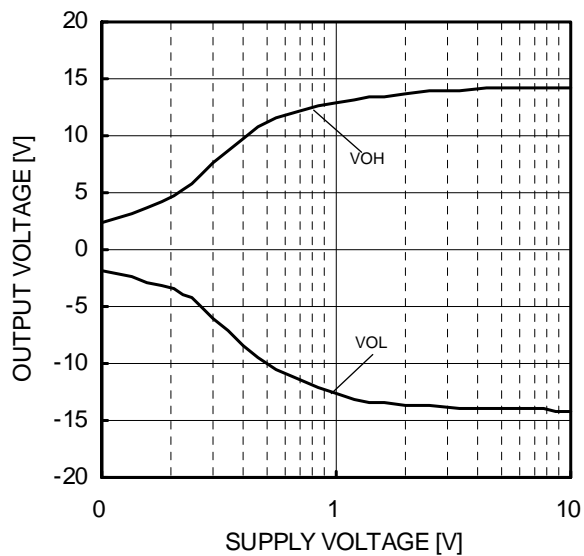


Figure 6.
Maximum Output Voltage
- Load Resistance
(VCC/VEE=+15V/-15V, Ta=25°C)

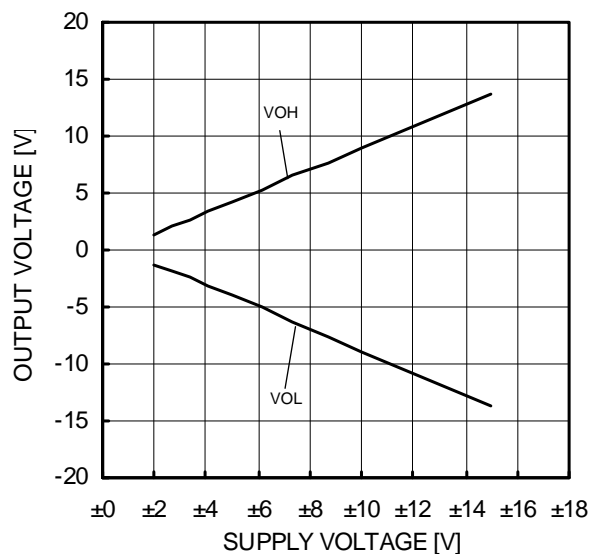


Figure 7.
Maximum Output Voltage
- Supply Voltage
(RL=2kΩ, Ta=25°C)

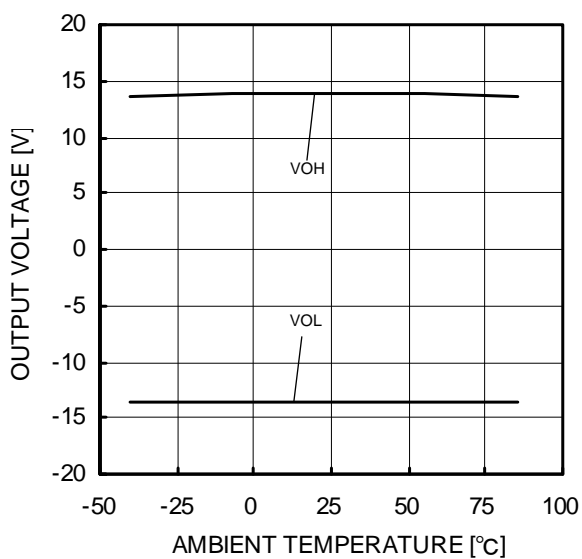


Figure 8.
Maximum Output Voltage
- Ambient Temperature
(VCC/VEE=+15V/-15V, RL=2kΩ)

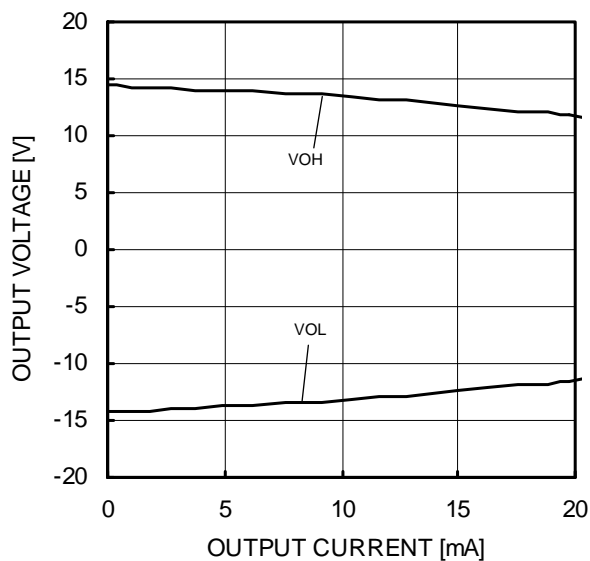


Figure 9.
Maximum Output Voltage
- Output Current
(VCC/VEE=+15V/-15V, Ta=25°C)

(*)The above data is measurement value of typical sample, it is not guaranteed.

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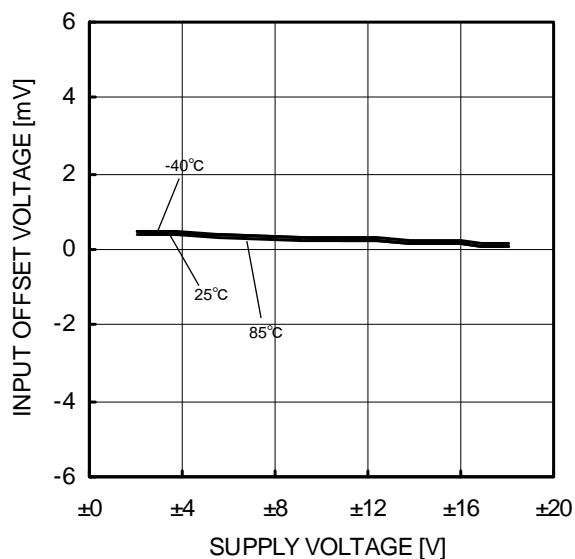


Figure 10.
Input Offset Voltage - Supply Voltage
(Vicm=0V, OUT=0V)

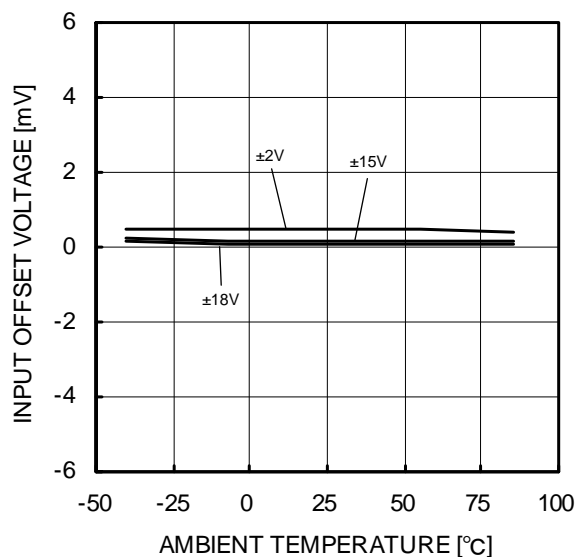


Figure 11.
Input Offset Voltage - Ambient Temperature
(Vicm=0V, OUT=0V)

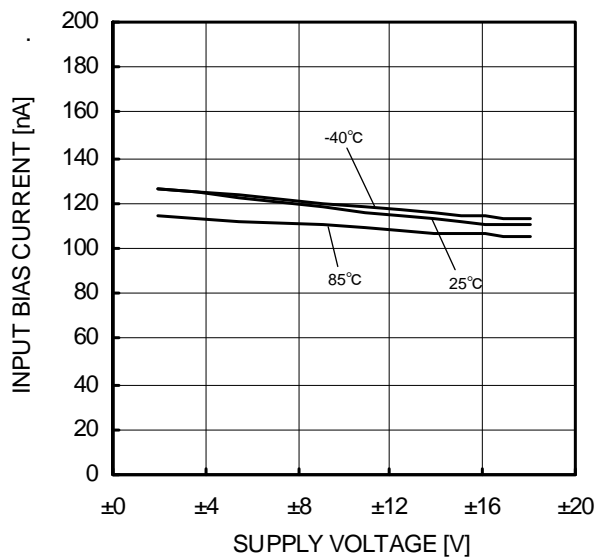


Figure 12.
Input Bias Current - Supply Voltage
(Vicm=0V, OUT=0V)

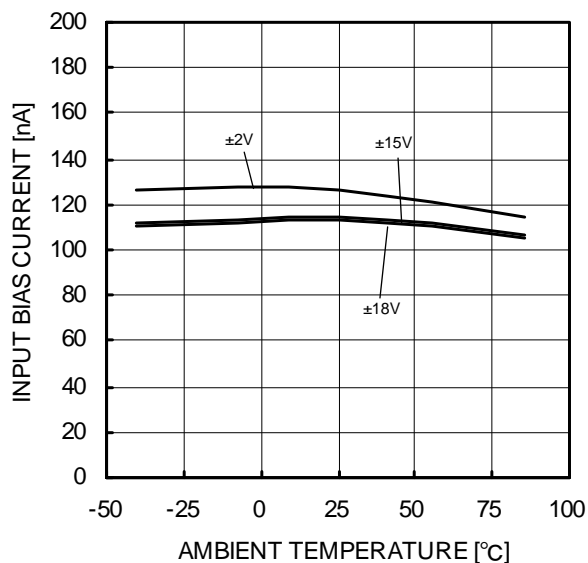


Figure 13.
Input Bias Current - Ambient Temperature
(Vicm=0V, OUT=0V)

(*The above data is measurement value of typical sample, it is not guaranteed.

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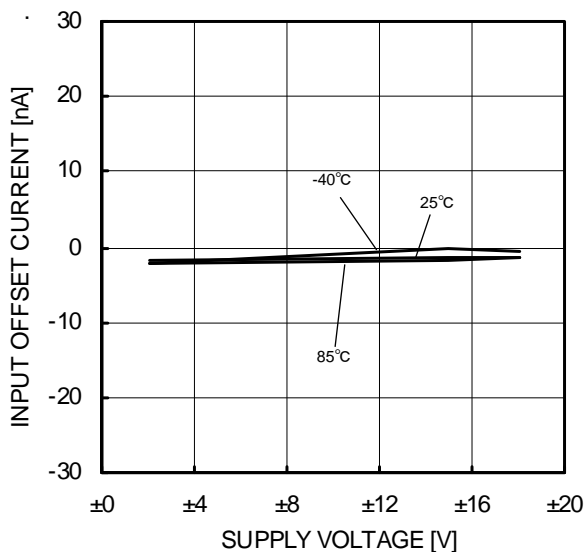


Figure 14.
Input Offset Current - Supply Voltage
(Vicm=0V, OUT=0V)

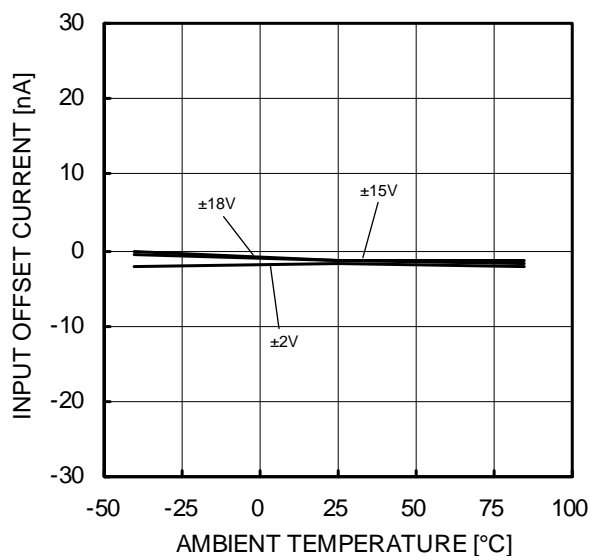


Figure 15.
Input Offset Current - Ambient Temperature
(Vicm=0V, OUT=0V)

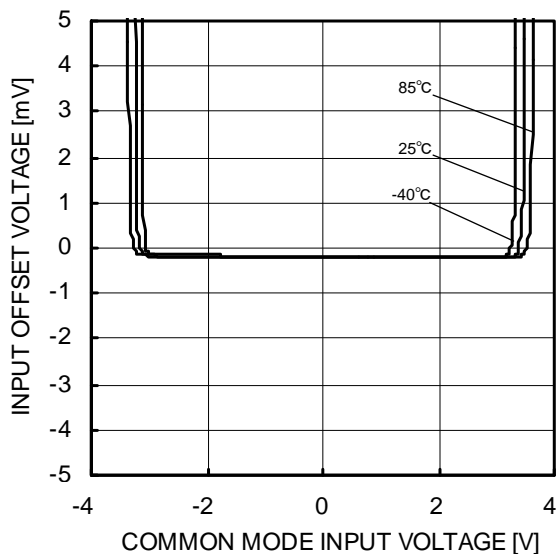


Figure 16.
Input Offset Voltage
- Common Mode Input Voltage
(VCC/VEE=+4V/-4V, OUT=0V)

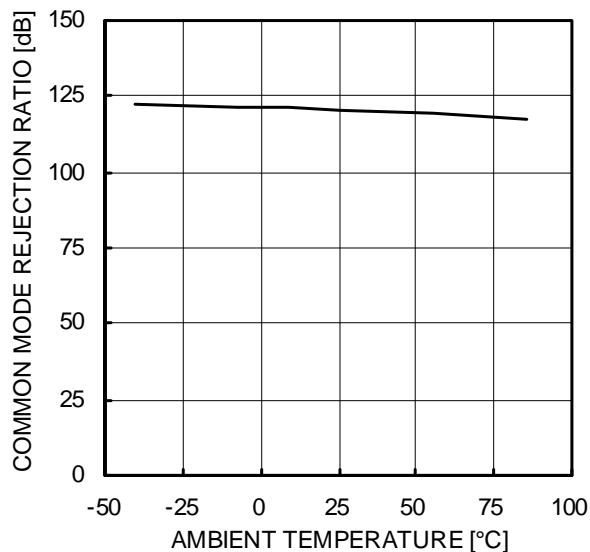


Figure 17.
Common Mode Rejection Ratio
- Ambient Temperature
(VCC/VEE=+15V/-15V, Vicm=-12V to +12V)

(*)The above data is measurement value of typical sample, it is not guaranteed.

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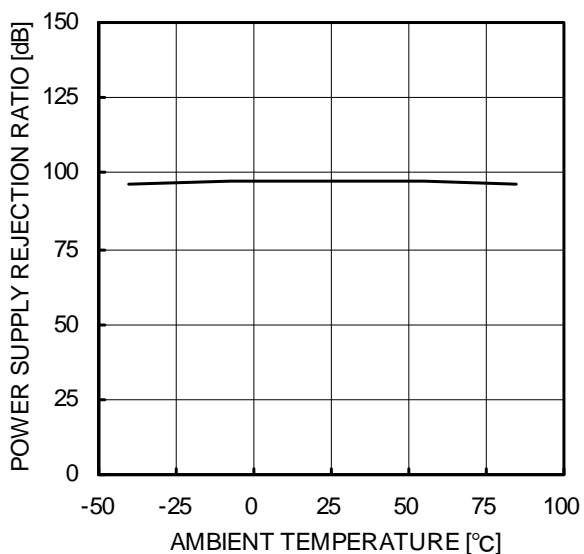


Figure 18.
Power Supply Rejection Ratio
- Ambient Temperature
(VCC/VEE=+2V/-2V to +15V/-15V)

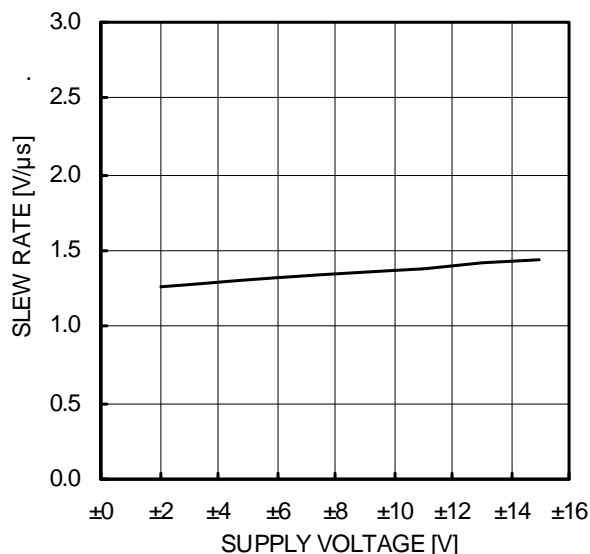


Figure 19.
Slew Rate - Supply Voltage
(CL=100pF, RL=2kΩ, Ta=25°C)

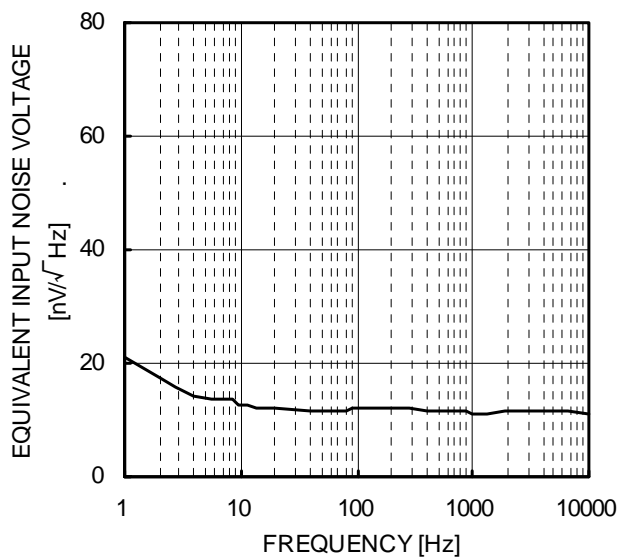


Figure 20.
Equivalent Input Noise Voltage - Frequency
(VCC/VEE=+15V/-15V, RS=100Ω, Ta=25°C)

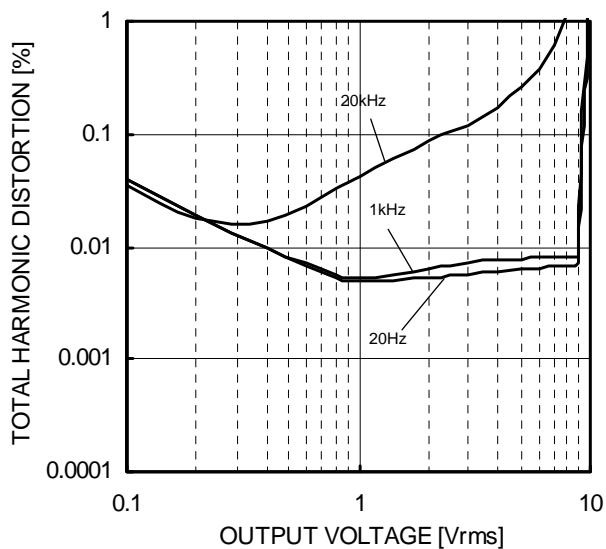


Figure 21.
Total Harmonic Distortion - Output Voltage
(VCC/VEE=+15V/-15V, Av=20dB, RL=2kΩ, 80kHz-LPF, Ta=25°C)

(*)The above data is measurement value of typical sample, it is not guaranteed.

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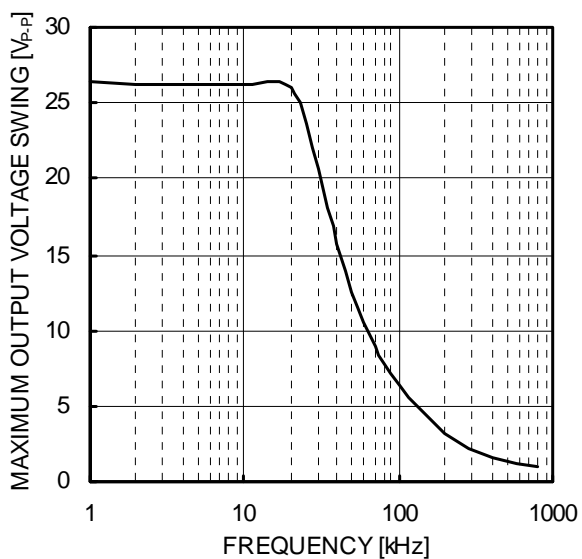


Figure 22.
Maximum Output Voltage Swing - Frequency
(VCC/VEE=+15V/-15V, RL=2kΩ, Ta=25°C)

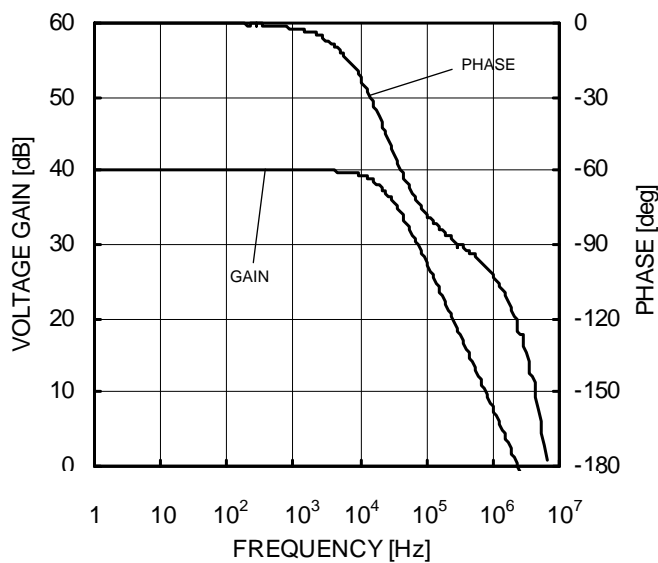


Figure 23.
Voltage Gain - Phase - Frequency
(VCC/VEE=+15V/-15V,
Av=40dB, RL=2kΩ, Ta=25°C)

(*)The above data is measurement value of typical sample, it is not guaranteed.

●Application Information
Test circuit1 NULL method

VCC, VEE, EK, Vicm Unit: V

Parameter	VF	S1	S2	S3	BA14741				calculation
					VCC	VEE	EK	Vicm	
Input Offset Voltage	VF1	ON	ON	OFF	15	-15	0	0	1
Input Offset Current	VF2	OFF	OFF	OFF	15	-15	0	0	2
Input Bias Current	VF3	OFF	ON	OFF	15	-15	0	0	3
	VF4	ON	OFF						
Large Signal Voltage Gain	VF5	ON	ON	ON	15	-15	-10	0	4
	VF6				15	-15	10	0	
Common-mode Rejection Ratio (Input common-mode Voltage Range)	VF7	ON	ON	OFF	3	-27	12	0	5
	VF8				27	-3	-12	0	
Power Supply Rejection Ratio	VF9	ON	ON	OFF	2	-2	0	0	6
	VF10				15	-15	0	0	

-Calculation-

1. Input Offset Voltage (Vio)

$$V_{io} = \frac{|VF1|}{1+RF/RS} \text{ [V]}$$

2. Input Offset Current (Iio)

$$I_{io} = \frac{|VF2 - VF1|}{R_i \times (1+RF/RS)} \text{ [A]}$$

3. Input Bias Current (Ib)

$$I_b = \frac{|VF4 - VF3|}{2 \times R_{ix} (1+RF/RS)} \text{ [A]}$$

4. Large Signal Voltage Gain (Av)

$$A_v = 20 \times \text{Log} \frac{\Delta EK \times (1+RF/RS)}{|VF5 - VF6|} \text{ [dB]}$$

5. Common-mode Rejection Ration (CMRR)

$$CMRR = 20 \times \text{Log} \frac{\Delta Vicm \times (1+RF/RS)}{|VF8 - VF7|} \text{ [dB]}$$

6. Power supply rejection ratio (PSRR)

$$PSRR = 20 \times \text{Log} \frac{\Delta V_{cc} \times (1+RF/RS)}{|VF10 - VF9|} \text{ [dB]}$$

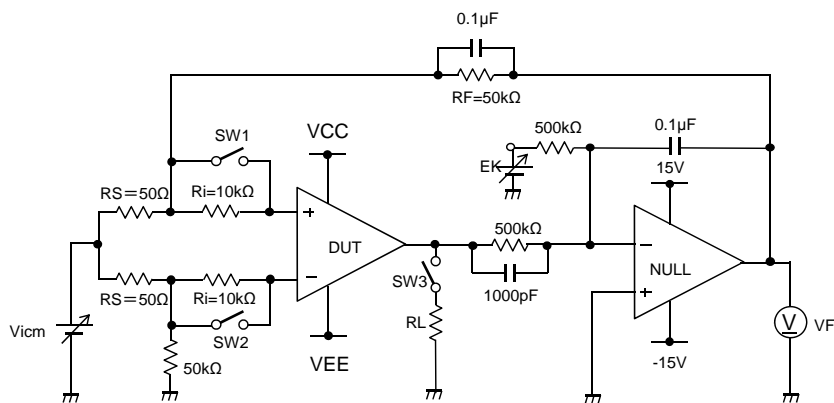


Figure 24. Test circuit1 (one channel only)

Test Circuit 2 Switch Condition

SW No.	SW1	SW2	SW3	SW4	SW5	SW6	SW7	SW8	SW9	SW10	SW11	SW12	SW13	SW14
Supply Current	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
Maximum Output Voltage High	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON
Maximum Output Voltage Low	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
Output Source Current	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
Output Sink Current	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
Slew Rate	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
Gain Bandwidth Product	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Equivalent Input Noise Voltage	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF

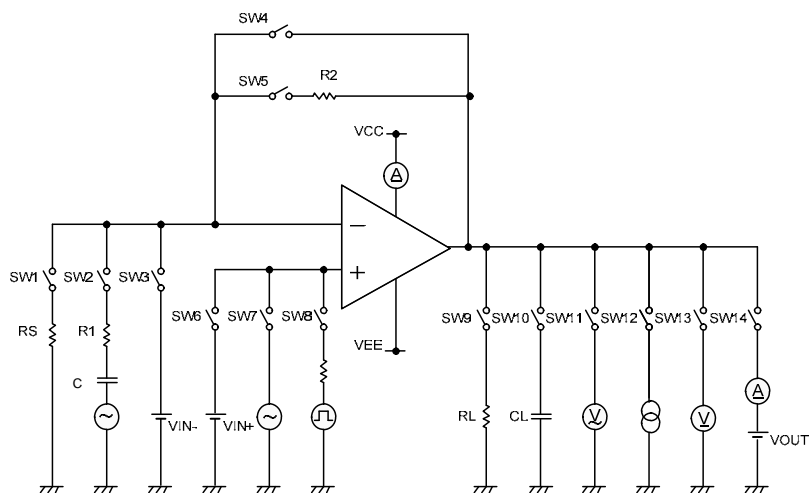


Figure 25. Test Circuit 2 (each Op-Amp)

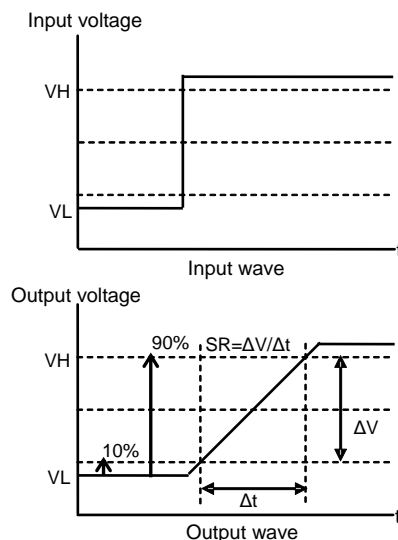
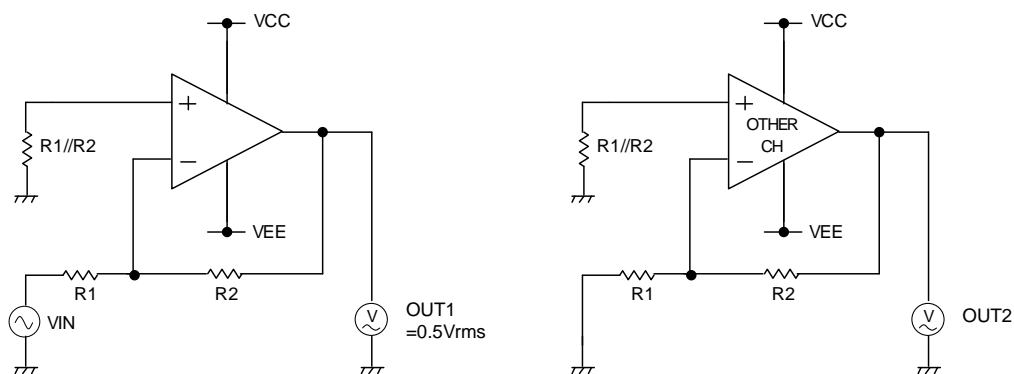


Figure 26. Slew Rate Input Waveform



$$CS = 20 \times \log \frac{100 \times OUT1}{OUT2}$$

Figure 27. Test Circuit 3 (Channel Separation)
(VCC=+15V, VEE=-15V, R1=1kΩ, R2=100kΩ)

● Power Dissipation

Power dissipation(total loss) indicates the power that can be consumed by IC at Ta=25°C(normal temperature). IC is heated when it consumed power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip(maximum junction temperature) and thermal resistance of package(heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead frame of the package. The parameter which indicates this heat dissipation capability(hardness of heat release)is called thermal resistance, represented by the symbol θ_{ja} °C/W. The temperature of IC inside the package can be estimated by this thermal resistance. Figure 28. (a) shows the model of thermal resistance of the package. Thermal resistance θ_{ja} , ambient temperature Ta, maximum junction temperature Tjmax, and power dissipation Pd can be calculated by the equation below:

$$\theta_{ja} = (T_{jmax} - T_a) / P_d \quad \text{°C/W} \quad \dots \dots \dots (I)$$

Derating curve in Figure 28. (b) indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θ_{ja} . Thermal resistance θ_{ja} depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used. Thermal reduction curve indicates a reference value measured at a specified condition. Figure 29. (c) show a derating curve for an example of BA 14741.

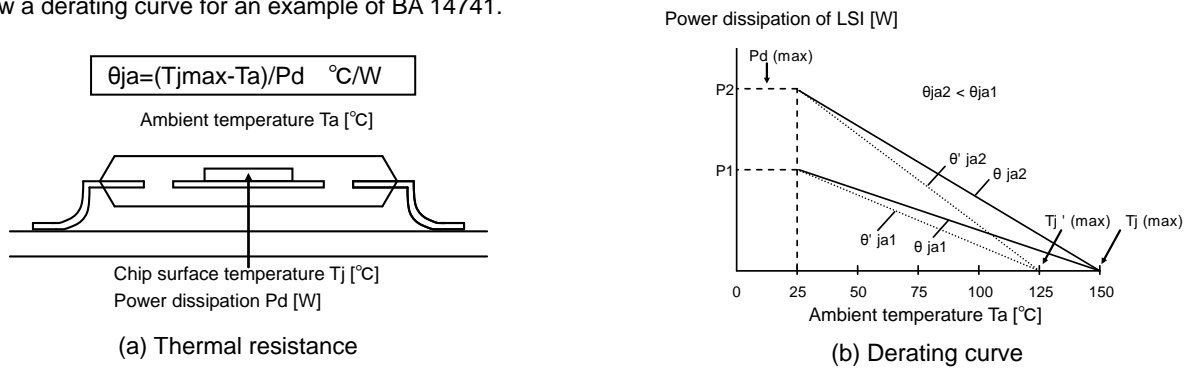
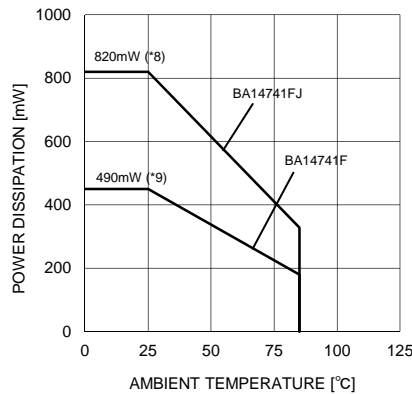


Figure 28. Thermal resistance and derating curve



(c)BA14741

(*8)	(*9)	Unit
8.2	4.5	mW/°C

When using the unit above Ta=25°C, subtract the value above per degree°C. Permissible dissipation is the value. Permissible dissipation is the value when FR4 glass epoxy board 70mm x70mm x1.6mm (cooper foil area below 3%) is mounted.

Figure 29. Derating curve

Application examples

○Voltage follower

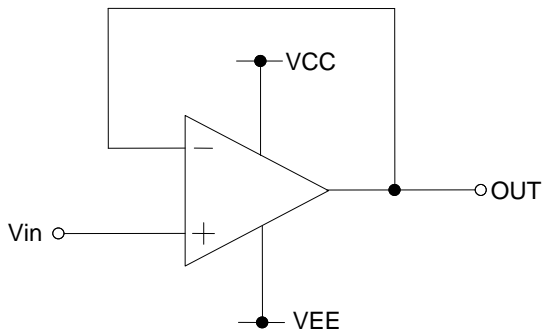


Figure 30. Voltage follower circuit

Voltage gain is 0 dB.
 This circuit controls output voltage (OUT) equal input voltage (Vin), and keeps OUT with stable because of high input impedance and low output impedance.
 OUT is shown next formula.
 $OUT = Vin$

○Inverting amplifier

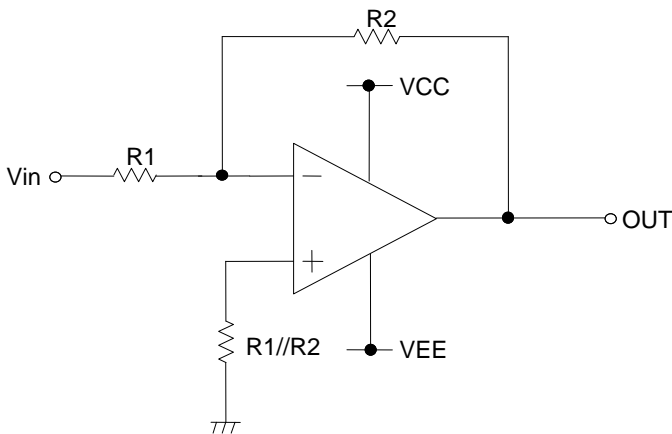


Figure 31. Inverting amplifier circuit

For inverting amplifier, Vin is amplified by voltage gain decided R1 and R2, and phase reversed voltage is outputted.
 OUT is shown next formula.
 $OUT = -(R2/R1) \cdot Vin$
 Input impedance is R1.

○Non-inverting amplifier

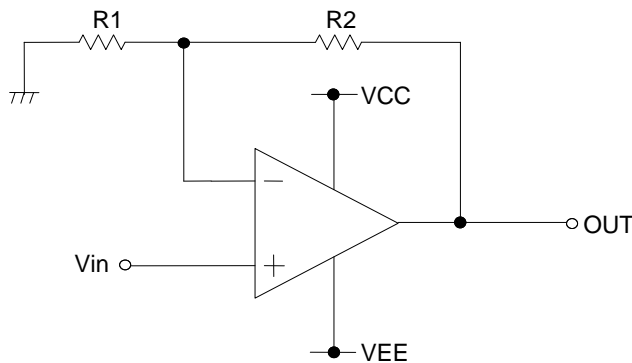


Figure 32. Non-inverting amplifier circuit

For non-inverting amplifier, Vin is amplified by voltage gain decided R1 and R2, and phase is same with Vin.
 OUT is shown next formula.
 $OUT = (1 + R2/R1) \cdot Vin$
 This circuit realizes high input impedance because Input impedance is operational amplifier's input Impedance.

●Operational Notes

- 1) Processing of unused circuit
It is recommended to apply connection (see the Figure 33.) and set the non-inverting input terminal at the potential within input common-mode voltage range (Vicm), for any unused circuit.
- 2) Input voltage
Applying VEE to VCC to the input terminal is possible without causing deterioration of the electrical characteristics or destruction, irrespective of the supply voltage. However, this does not ensure normal circuit operation. Please note that the circuit operates normally only when the input voltage is within the common mode input voltage range of the electric characteristics.
- 3) Maximum output voltage
Because the output voltage range becomes narrow as the output current increases, design the application with margin by considering changes in electrical characteristics and temperature characteristics.
- 4) Short-circuit of output terminal
When output terminal and VCC or VEE terminal are shorted, excessive Output current may flow under some conditions, and heating may destroy IC. It is necessary to connect a resistor as shown in Figure 34, thereby protecting against load shorting.
- 5) Power supply (split supply / single supply) in used
Op-amp operates when specified voltage is applied between VCC and VEE. Therefore, the single supply Op-Amp can be used for double supply Op-Amp as well.
- 6) Power dissipation (Pd)
Use a thermal design that allows for a sufficient margin in light of the power dissipation (Pd) in actual operating conditions.
- 7) Short-circuit between pins and wrong mounting
Pay attention to the assembly direction of the ICs. Wrong mounting direction or shorts between terminals, GND, or other components on the circuits, can damage the IC.
- 8) Use in strong electromagnetic field
Using the ICs in strong electromagnetic field can cause operation malfunction.
- 9) Radiation
This IC is not designed to be radiation-resistant.
- 10) IC handling
When stress is applied to IC because of deflection or bend of board, the characteristics may fluctuate due to piezo resistance effects.
- 11) Inspection on set board
During testing, turn on or off the power before mounting or dismounting the board from the test Jig. Do not power up the board without waiting for the output capacitors to discharge. The capacitors in the low output impedance terminal can stress the device. Pay attention to the electro static voltages during IC handling, transportation, and storage.
- 12) Output capacitor
When VCC terminal is shorted to VEE (GND) potential and an electric charge has accumulated on the external capacitor, connected to output terminal, accumulated charge may be discharged VCC terminal via the parasitic element within the circuit or terminal protection element. The element in the circuit may be damaged (thermal destruction). When using this IC for an application circuit where there is oscillation, output capacitor load does not occur, as when using this IC as a voltage comparator. Set the capacitor connected to output terminal below 0.1 μ F in order to prevent damage to IC.

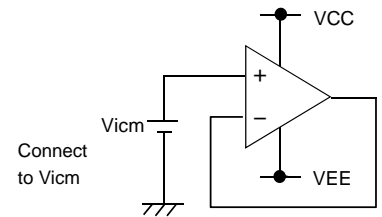


Figure 33. The example of application circuit for unused op-amp

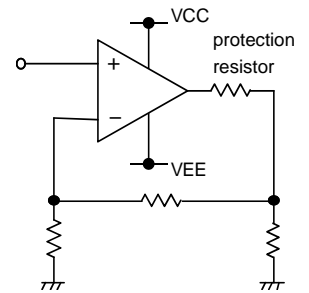


Figure 34. The example of output short protection

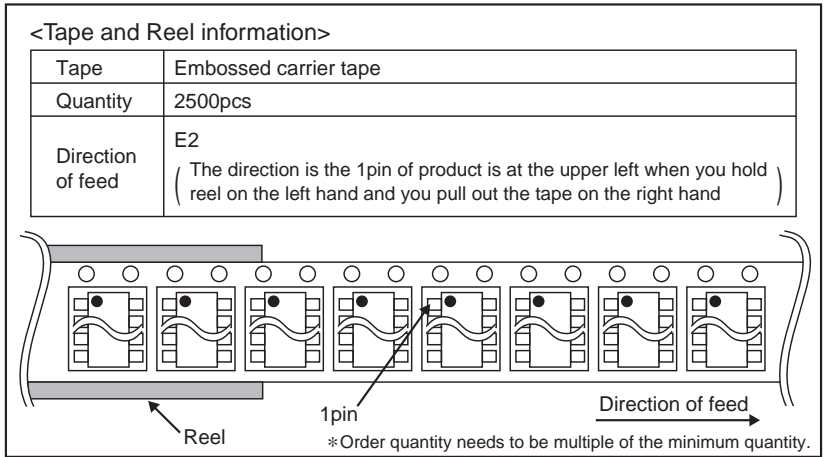
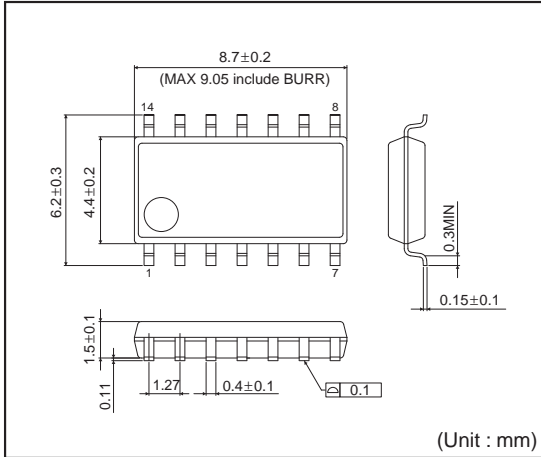
Status of this document

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

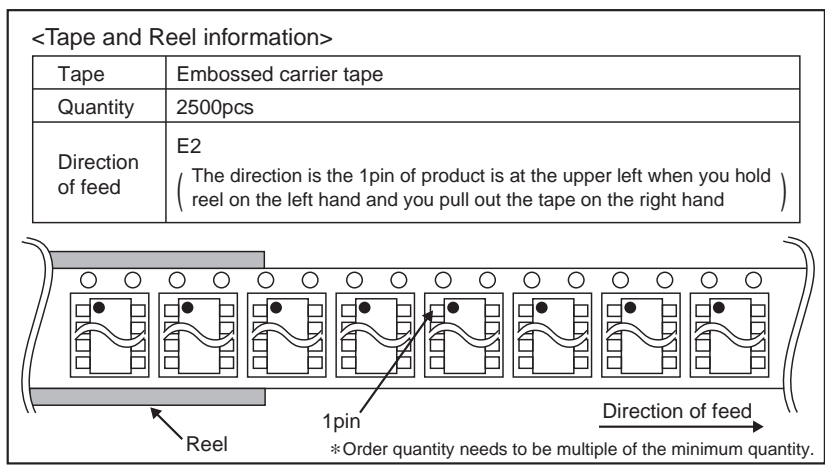
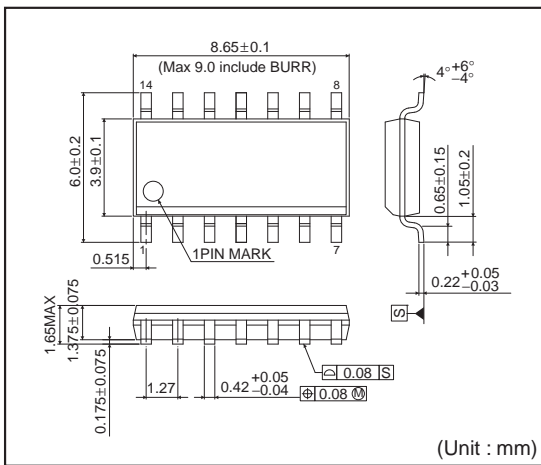
If there are any differences in translation version of this document formal version takes priority.

●Physical Dimensions Tape and Reel Information

SOP14

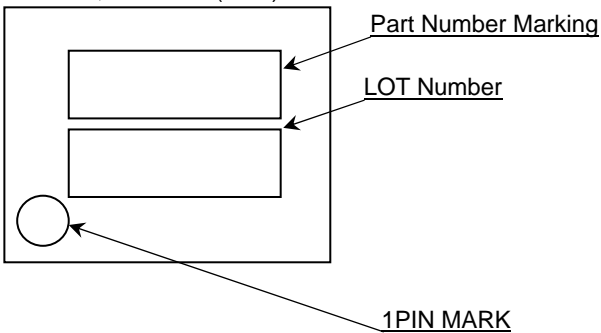


SOP-J14



●Marking Diagrams

SOP14, SOP-J14 (TOP)

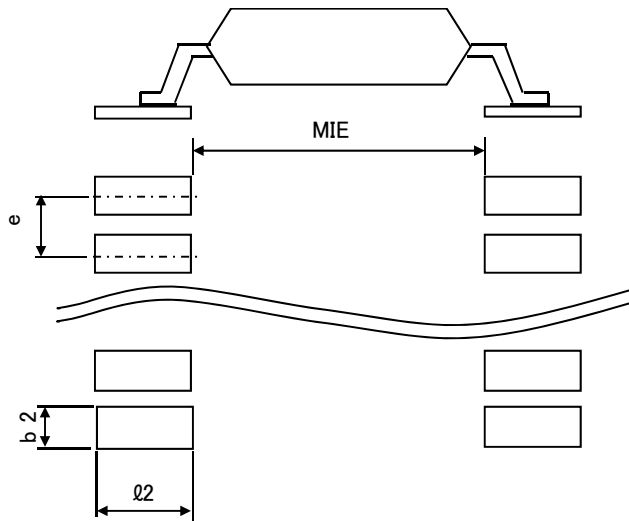


Product Name		Package Type	Marking
BA14741	F	SOP14	BA14741F
	FJ	SOP-J14	BA14741

●Land pattern data

all dimensions in mm

PKG	Land pitch e	Land space MIE	Land length $\geq \ell 2$	Land width b2
SOP14	1.27	4.60	1.10	0.76
SOP-J14	1.27	3.90	1.35	0.35



●Revision History

Date	Revision	Changes
2012.11.9	001	New Release

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
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 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
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- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
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 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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