

Operational Amplifiers Series

Ground Sense Operational Amplifiers



BA3404xxx

● **General Description**

BA3404 is a dual operational amplifier with input and output ground sense. Especially, BA3404 have wide operating voltage range +4V to +36V (single supply). BA3404 have a good performance of slew rate and cross over distortion compare with BA2904.

● **Features**

- Operable with a single power supply
- Wide operating supply voltage
- Input and output are operable GND sense
- Low supply current
- High open loop voltage gain
- Internal ESD protection circuit

● **Application**

- Current sense application
- Buffer application amplifier
- Active filter
- Consumer electronics

● **Block Diagrams**

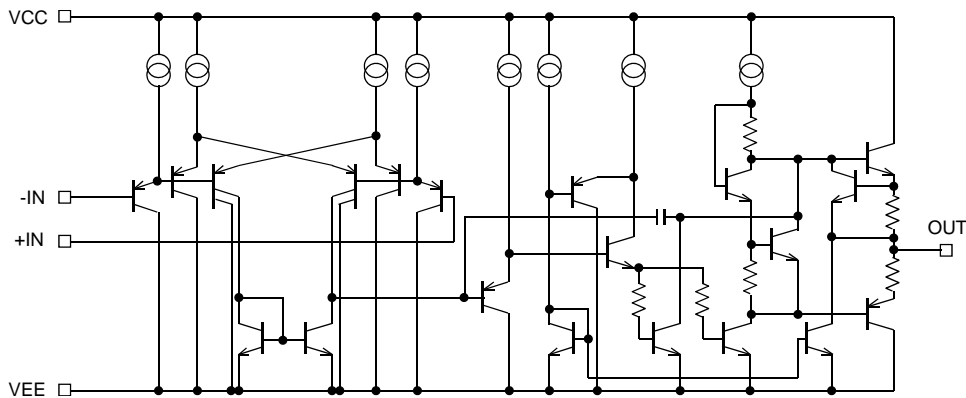


Figure 1. Simplified schematic

● **Packages**

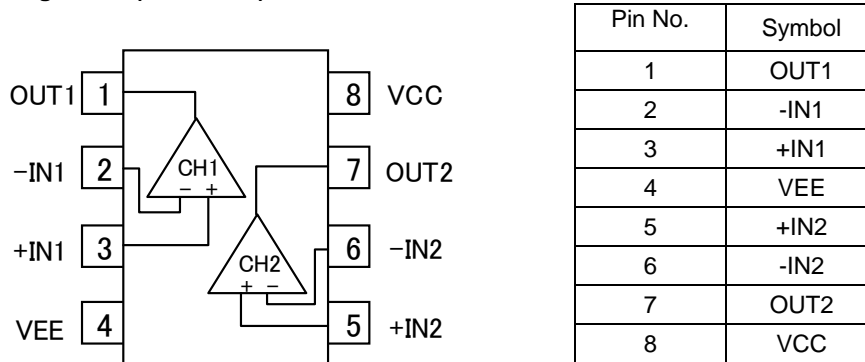
Package	W(Typ.)xD(Typ.) xH(Max.)
SOP8	5.00mm x 6.20mm x 1.71mm
SOP-J8	4.90mm x 6.00mm x 1.65mm
MSOP8	2.90mm x 4.00mm x 0.90mm

● **Key Specification**

- Wide Operating Supply Voltage
(single supply): +4.0V to +36.0V
(split supply): ±2.0V to ±18.0V
- Slew Rate: 1.2V/μs(Typ.)
- Wide Temperature Range: -40°C to +85°C
- Input Offset Current: 5nA (Typ.)
- Input Offset Voltage: 5mV (Max.)

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

●Pin Configuration(TOP VIEW)



Package		
SOP8	SOP-J8	MSOP8
BA3404F	BA3404FJ	BA3404FVM

●Ordering Information

B	A	3	4	0	4	x	x	x	-	x	x	
Part Number. BA3404xxx									Package F : SOP8 FJ : SOP-J8 FVM : MSOP8		Packaging and forming specification E2: Embossed tape and reel (SOP8/SOP-J8) TR: Embossed tape and reel (MSOP8)	

●Line-up

Topr	Supply Current (Typ.)	Slew Rate (Typ.)	Package		Orderable Part Number
-40°C to +85°C	2.0mA	1.2V/μs	SOP8	Reel of 2500	BA3404F-E2
			SOP-J8	Reel of 2500	BA3404FJ-E2
			MSOP8	Reel of 3000	BA3404FVM-TR

●Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Ratings	Unit	
Supply Voltage	VCC-VEE	+36	V	
Power dissipation	Pd	SOP8	780 ^{*1*4}	mW
		SOP-J8	675 ^{*2*4}	
		MSOP8	590 ^{*3*4}	
Differential Input Voltage ^{*5}	Vid	+36	V	
Input Common-mode Voltage Range	Vicm	(VEE-0.3) to (VEE+36)	V	
Operating Temperature Range	Topr	-40 to +85	°C	
Storage Temperature Range	Tstg	-55 to +150	°C	
Maximum Junction Temperature	Tjmax	+150	°C	

Note: Absolute maximum rating item indicates the condition which must not be exceeded.

Application if voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

*1 To use at temperature above Ta=25°C reduce 6.2mW/°C

*2 To use at temperature above Ta=25°C reduce 5.4mW/°C

*3 To use at temperature above Ta=25°C reduce 4.8mW/°C

*4 Mounted on a FR4 glass epoxy PCB(70mm×70mm×1.6mm).

*5 The voltage difference between inverting input and non-inverting input is the differential input voltage. Then input terminal voltage is set to more than VEE.

●Electrical Characteristics

OBA3404 (Unless otherwise specified VCC=+15V, VEE=-15V, Ta=25°C)

Parameter	Symbol	Limits			Unit	Condition
		Min.	Typ.	Max.		
Input Offset Voltage *6	Vio	-	2	5	mV	VOUT=0V, Vicm=0V
Input Offset Current *6	Iio	-	5	50	nA	VOUT=0V, Vicm=0V
Input Bias Current *6	Ib	-	70	200	nA	VOUT=0V, Vicm=0V
Large Signal Voltage Gain	Av	88	100	-	dB	RL ≥ 2kΩ VOUT=±10V, Vicm=0V
Maximum Output Voltage	VOM	±13	±14	-	V	RL ≥ 2kΩ
Input Common-mode Voltage Range	Vicm	-15	-	13	V	VOUT=0V
Common-mode Rejection Ratio	CMRR	70	90	-	dB	VOUT=0V Vicm=-15V to +13V
Power Supply Rejection Ratio	PSRR	80	94	-	dB	Ri ≤ 10kΩ VCC=+4V to +30V
Supply Current	ICC	-	2.0	3.5	mA	RL=∞, All Op-Amps VIN+=0V
Output Source Current	Isource	20	30	-	mA	VIN+=1V, VIN-=0V VOUT=+12V Output of one channel only
Output Sink Current	Isink	10	20	-	mA	VIN+=0V, VIN-=1V VOUT=-12V Output of one channel only
Slew rate	SR	-	1.2	-	V/μs	Av=0dB, RL=2kΩ CL=100pF
Unity Gain Frequency	f _T	-	1.2	-	MHz	RL=2kΩ
Gain Band Width	GBW	-	1.2	-	MHz	f=100kHz
Total Harmonic Distortion	THD+N	-	0.1	-	%	VOUT=10V _{p,p} , f=20kHz Av=0dB, RL=2kΩ
Channel Separation	CS	-	100	-	dB	f=1kHz, input referred

*6 Absolute value

Description of Electrical Characteristics

Described here are the terms of electric characteristics used in this datasheet. Items and symbols used are also shown. Note that item name and symbol and their meaning may differ from those on another manufacture's document or general document.

1. Absolute maximum ratings

Absolute maximum rating item indicates the condition which must not be exceeded. Application of voltage in excess of absolute maximum rating or use out of absolute maximum rated temperature environment may cause deterioration of characteristics.

1.1 Power supply voltage (VCC-VEE)

Indicates the maximum voltage that can be applied between the positive power supply terminal and negative power supply terminal without deterioration or destruction of characteristics of internal circuit.

1.2 Differential input voltage (Vid)

Indicates the maximum voltage that can be supplied between the non-inverting and inverting terminals without damaging the IC.

1.3 Input common-mode voltage range (Vicm)

Indicates the maximum voltage that can be applied to non-inverting terminal and inverting terminal without deterioration or destruction of characteristics. Input common-mode voltage range of the maximum ratings not assures normal operation of IC. When normal Operation of IC is desired, the input common-mode voltage of characteristics item must be followed.

1.4 Power dissipation (Pd)

Indicates the power that can be consumed by specified mounted board at the ambient temperature 25°C(normal temperature). As for package product, Pd is determined by the temperature that can be permitted by IC chip in the package (maximum junction temperature) and thermal resistance of the package.

2. Electrical characteristics

2.1 Input offset voltage (Vio)

Indicates the voltage difference between non-inverting terminal and inverting terminal. It can be translated into the input voltage difference required for setting the output voltage at 0 V.

2.2 Input offset current (Iio)

Indicates the difference of input bias current between the non-inverting and inverting terminals.

2.3 Input bias current (Ib)

Indicates the current that flows into or out of the input terminal. It is defined by the average of input bias current at non-inverting terminal and input bias current at inverting terminal.

2.4 Large signal voltage gain (Av)

Indicates the amplifying rate (gain) of output voltage against the voltage difference between non-inverting terminal and inverting terminal. It is normally the amplifying rate (gain) with reference to DC voltage.

$$A_v = (\text{Output voltage fluctuation}) / (\text{Input offset fluctuation})$$

2.5 Maximum Output Voltage (VOM)

Signifies the voltage range that can be output under specific output conditions.

2.6 Input common-mode voltage range (Vicm)

Indicates the input voltage range under which the IC operates normally.

2.7 Common-mode rejection ratio (CMRR)

Indicates the ratio of fluctuation of input offset voltage when in-phase input voltage is changed. It is normally the fluctuation of DC.

$$CMRR = (\text{Change of Input common-mode voltage}) / (\text{Input offset fluctuation})$$

2.8 Power supply rejection ratio (PSRR)

Indicates the ratio of fluctuation of input offset voltage when supply voltage is changed. It is normally the fluctuation of DC. PSRR= (Change of power supply voltage)/(Input offset fluctuation)

2.9 Circuit current (ICC)

Indicates the IC current that flows under specified conditions and no-load steady status.

2.10 Output source current/ output sink current (Isource/Isink)

The maximum current that can be output under specific output conditions, it is divided into output source current and output sink current. The output source current indicates the current flowing out of the IC, and the output sink current the current flowing into the IC.

2.11 Slew Rate (SR)

SR is a parameter that shows movement speed of operational amplifier. It indicates rate of variable output voltage as unit time.

2.12 Unity gain frequency (f_T)

Indicates a frequency where the voltage gain of operational amplifier is 1.

2.13 Total harmonic distortion + Noise (THD+N)

Indicates the fluctuation of input offset voltage or that of output voltage with reference to the change of output voltage of driven channel.

2.14 Gain Band Width (GBW)

Indicates to multiply by the frequency and the gain where the voltage gain decreases 6dB/octave.

● Typical Performance Curves

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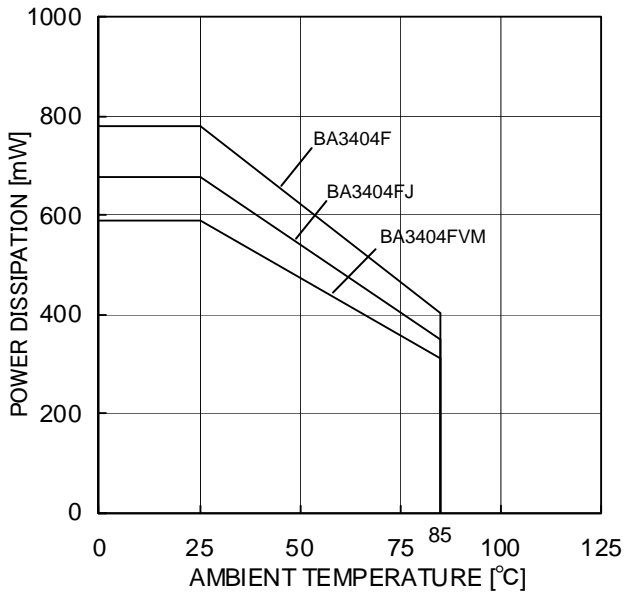


Figure 2.
Derating Curve

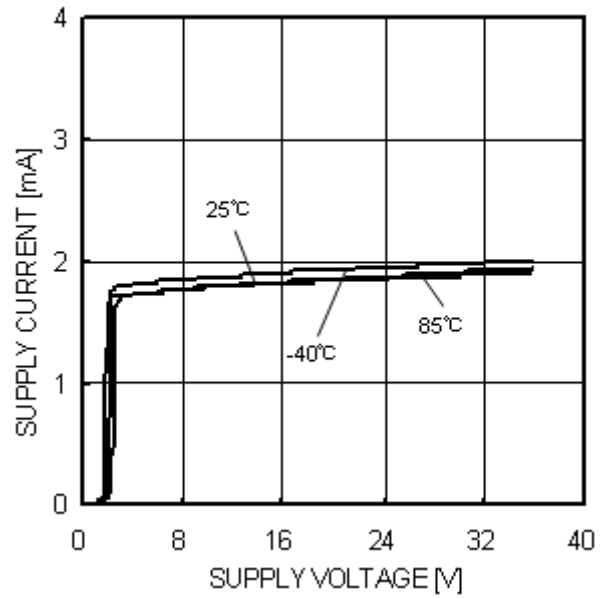


Figure 3.
Supply Current - Supply Voltage

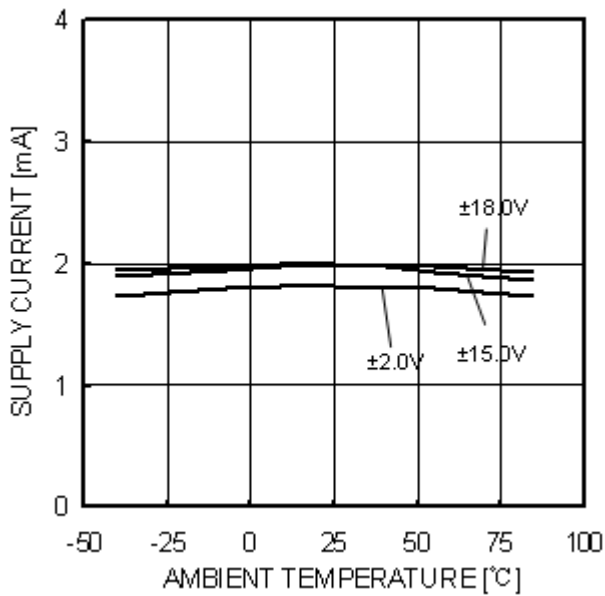


Figure 4.
Supply Current - Ambient Temperature

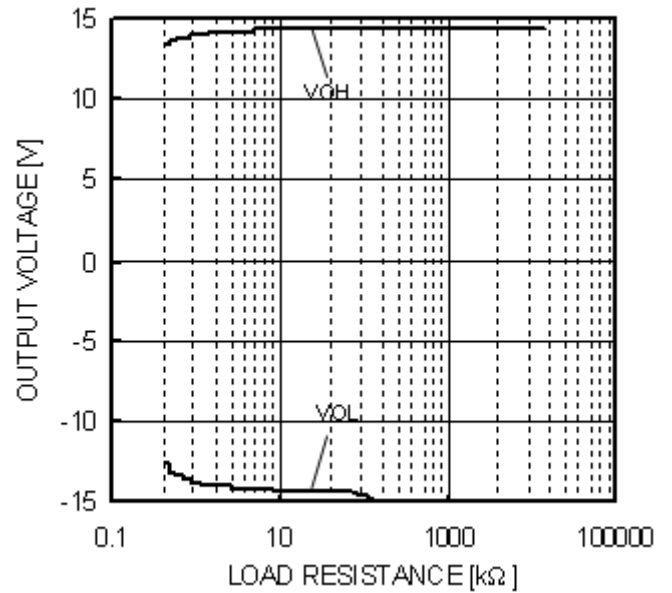


Figure 5.
Maximum Output Voltage - Load Resistance
(VCC/VEE=+15V/-15V, Ta=25°C)

(*The above data is measurement value of typical sample, it is not guaranteed.

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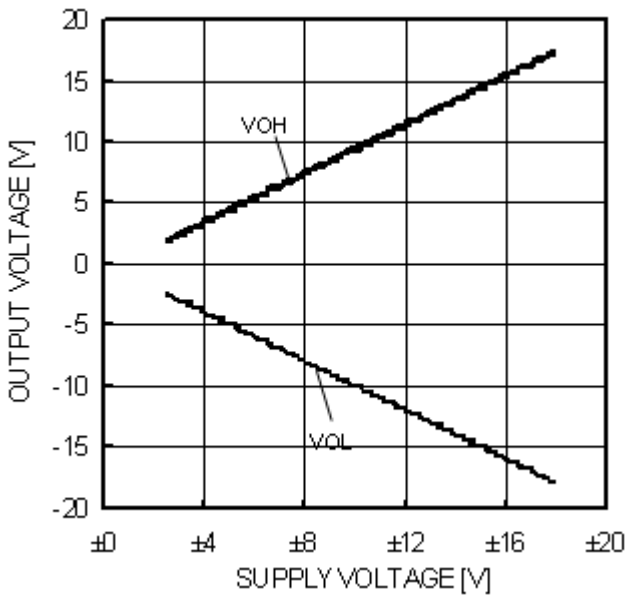


Figure 6.
Maximum Output Voltage – Supply Voltage

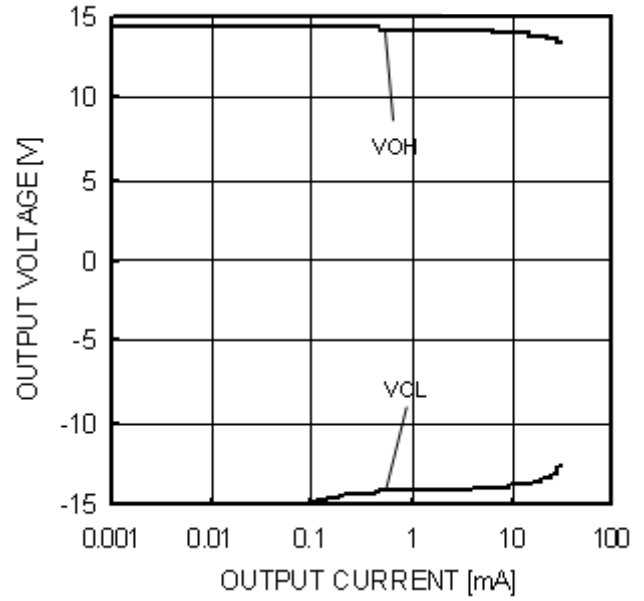


Figure 7.
Output Voltage - Output Current
(VCC/VEE=+15V/-15V, Ta=25°C)

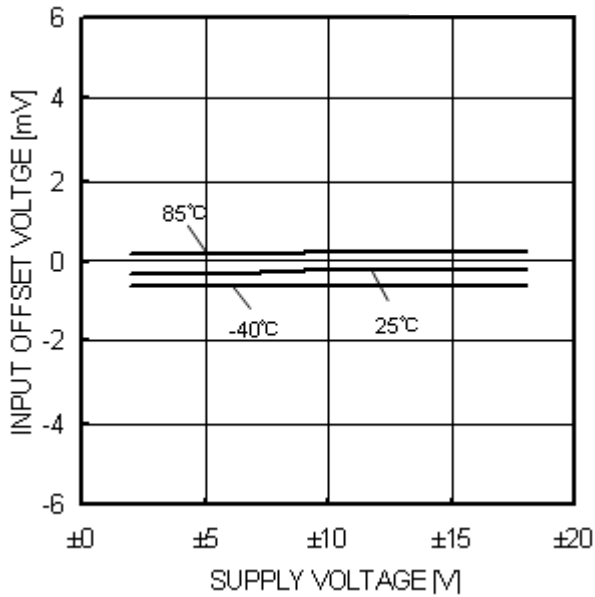


Figure 8.
Input Offset Voltage - Supply voltage
(Vicm=0V, VOUT=0V)

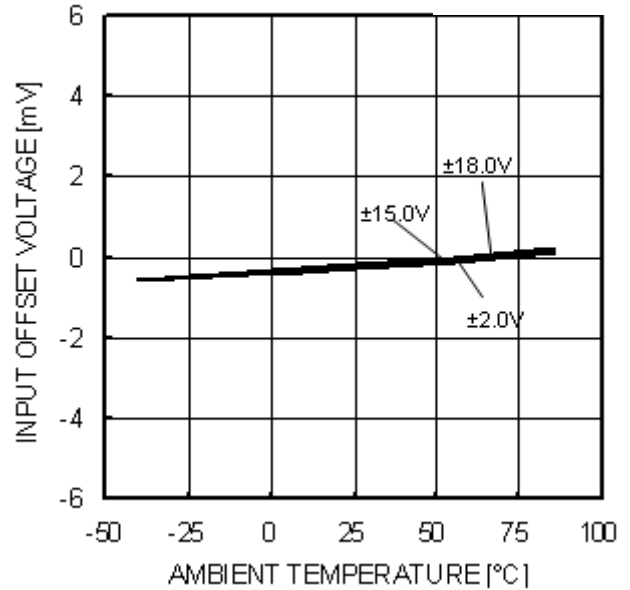


Figure 9.
Input Offset Voltage - Ambient Temperature
(Vicm=0V, VOUT=0V)

(*)The above data is measurement value of typical sample, it is not guaranteed.

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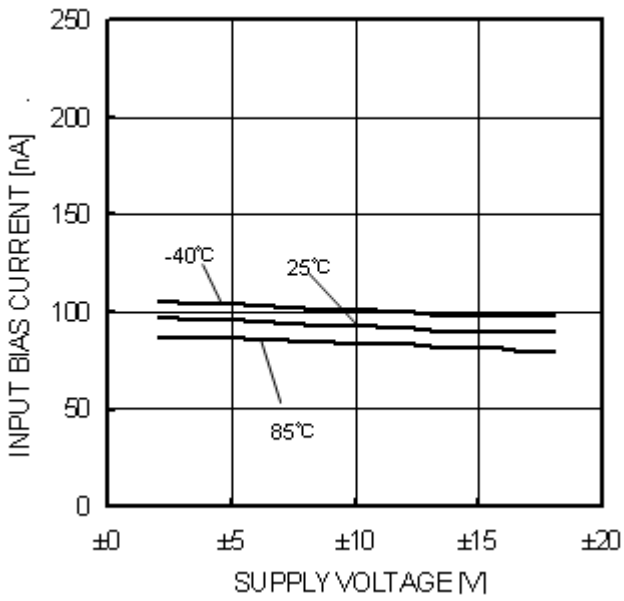


Figure 10.
Input Bias Current - Supply Voltage
($V_{icm}=0V$, $V_{OUT}=0V$)

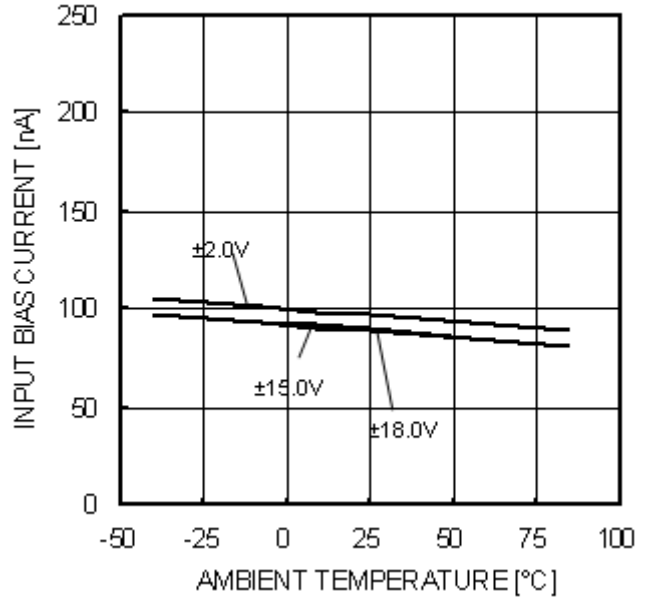


Figure 11.
Input Bias Current - Ambient Temperature
($V_{icm}=0V$, $V_{OUT}=0V$)

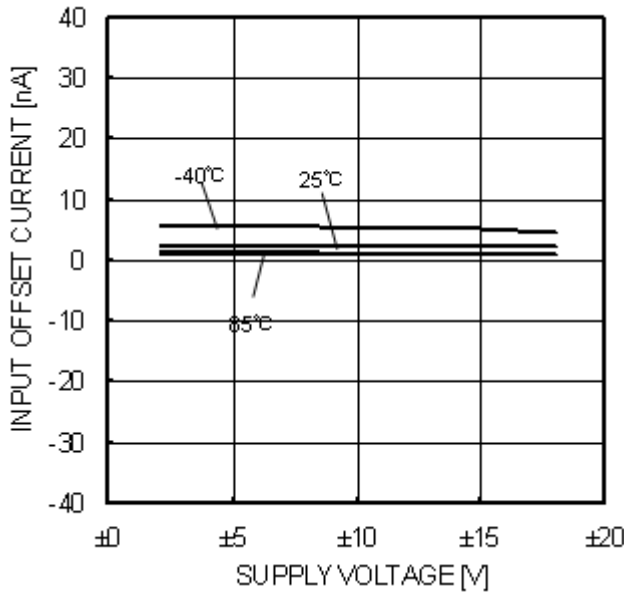


Figure 12.
Input Offset Current - Supply Voltage
($V_{icm}=0V$, $V_{OUT}=0V$)

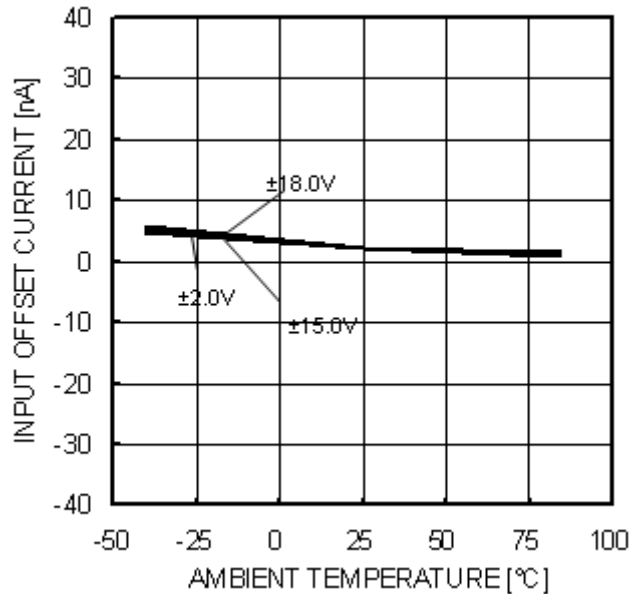


Figure 13.
Input Offset Current - Ambient Temperature
($V_{icm}=0V$, $V_{OUT}=0V$)

(*The above data is measurement value of typical sample, it is not guaranteed.

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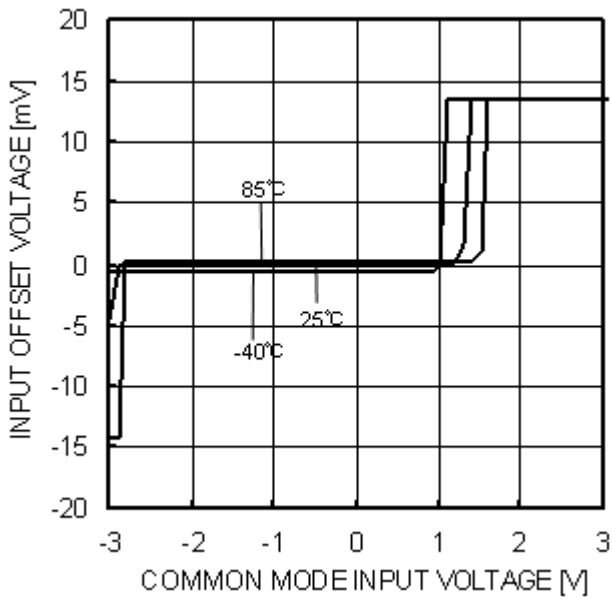


Figure 14.
Input Offset Voltage
- Common Mode Input Voltage
(VCC/VEE=+2.5V/-2.5V)

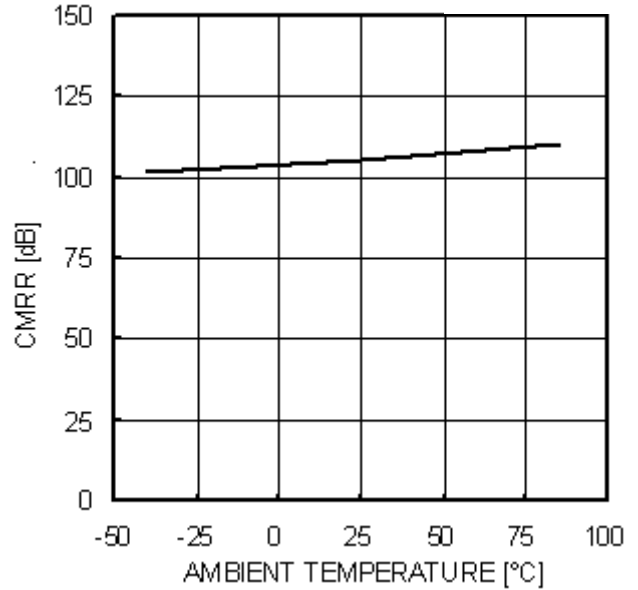


Figure 15.
Common Mode Rejection Ratio
- Ambient Temperature
(VCC/VEE=+15V/-15V)

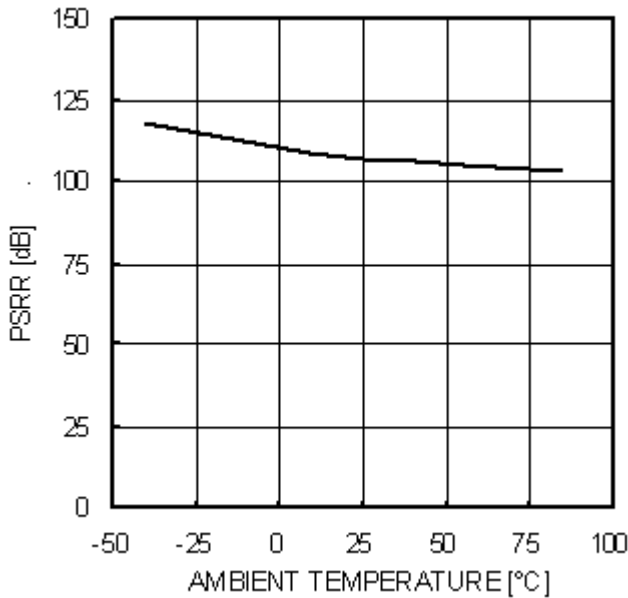


Figure 16.
Common Mode Rejection Ratio
- Ambient Temperature
(VCC/VEE=+15V/-15V)

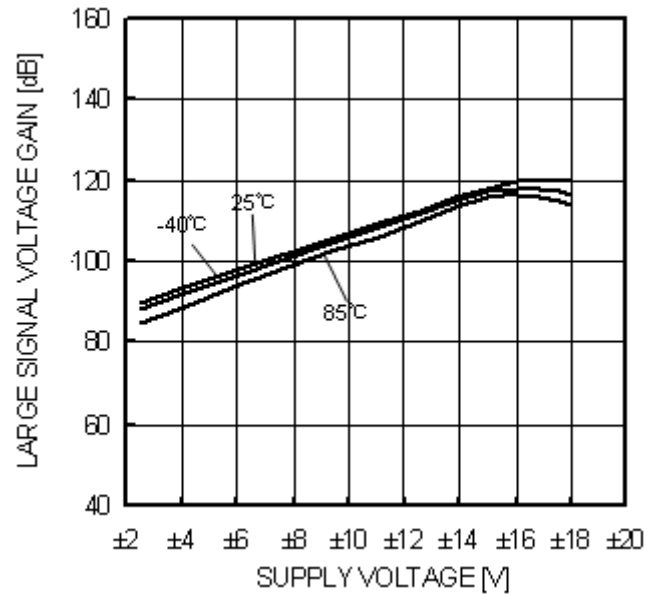


Figure 17.
Large Signal Voltage Gain
- Supply Voltage (RL=2kΩ)

(*)The above data is measurement value of typical sample, it is not guaranteed.

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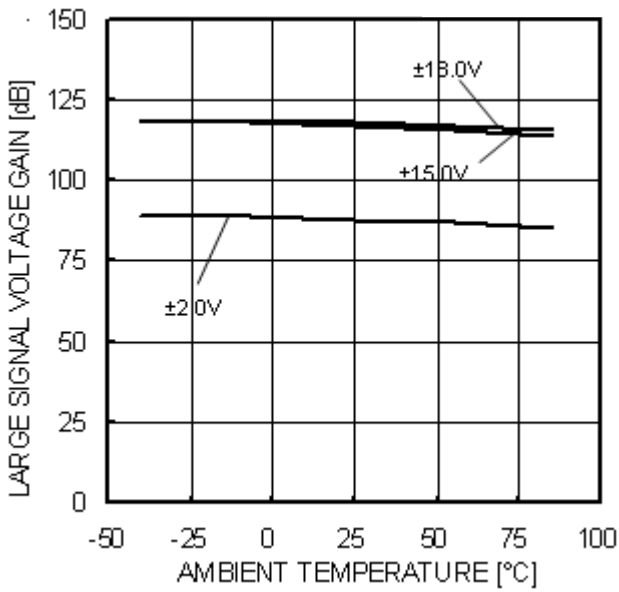


Figure 18.
Large Signal Voltage Gain
- Ambient Temperature (RL=2kΩ)

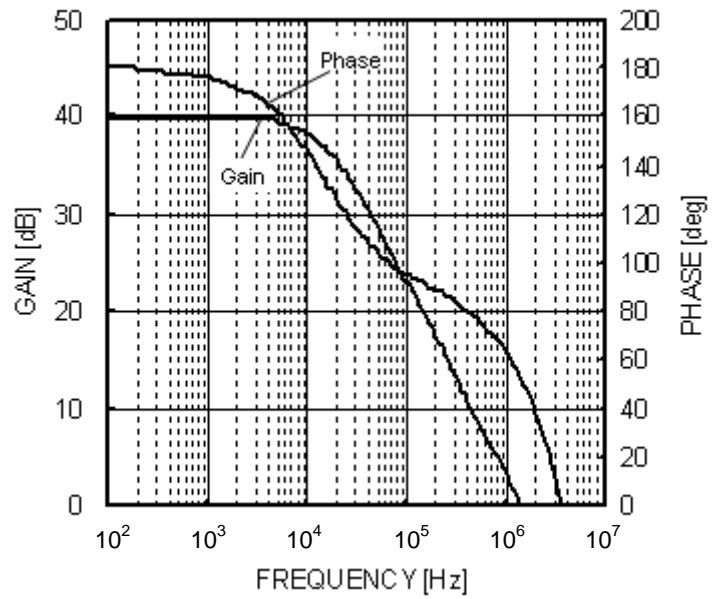


Figure 19.
Voltage Gain · Phase - Frequency
(VCC=±15V)

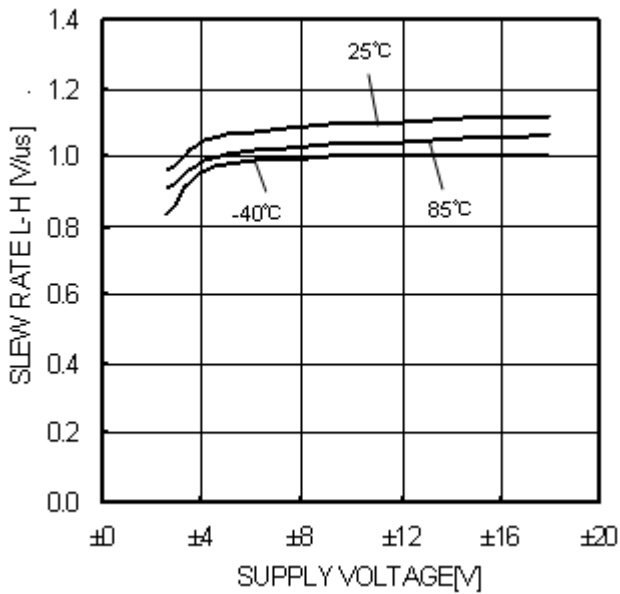


Figure 20.
Slew Rate L-H - Supply Voltage

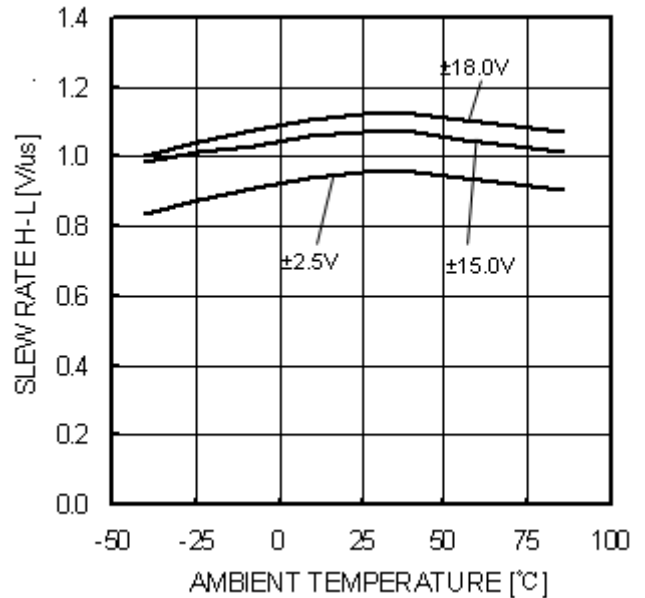


Figure 21.
Slew Rate H-L - Ambient Temperature

(*The above data is measurement value of typical sample, it is not guaranteed.

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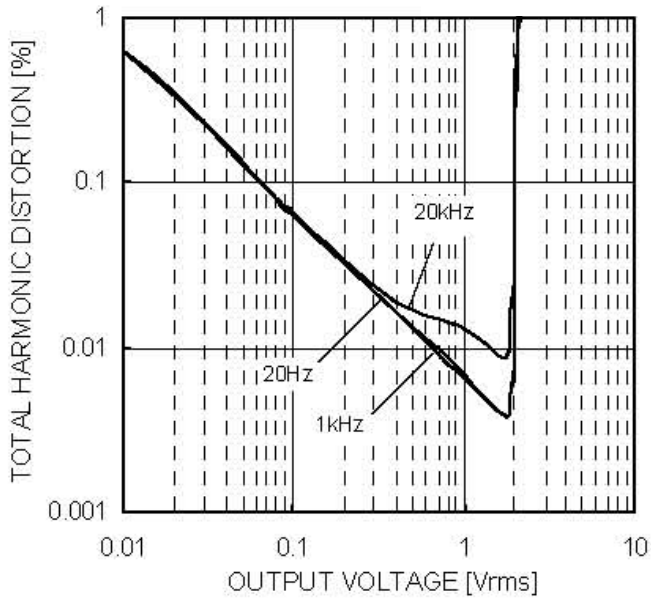


Figure 22.
Total Harmonic Distortion - Output Voltage
(VCC/VEE=+4V/-4V, Av=0dB,
RL=2kΩ, 80kHz-LPF, Ta=25°C)

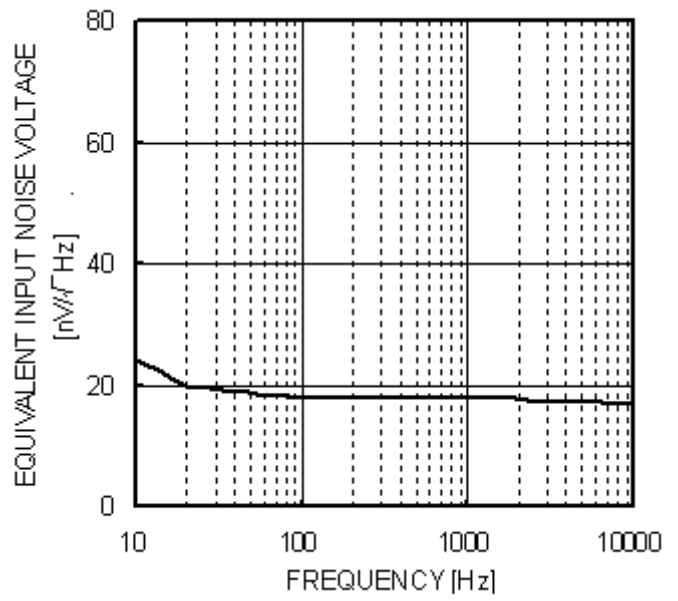


Figure 23.
Equivalent Input Noise Voltage - Frequency
(VCC/VEE=+15V/-15V, RS=100Ω, Ta=25°C)

(*The above data is measurement value of typical sample, it is not guaranteed.

●Application Information

NULL method condition for Test Circuit 1

VCC,VEE,EK,Vicm Unit: V

Parameter	VF	S1	S2	S3	VCC	VEE	EK	Vicm	calculation
Input Offset Voltage	VF1	ON	ON	OFF	15	-15	0	0	1
Input Offset Current	VF2	OFF	OFF	OFF	15	-15	0	0	2
Input Bias Current	VF3	OFF	ON	OFF	15	-15	0	0	3
	VF4	ON	OFF						
Large Signal Voltage Gain	VF5	ON	ON	ON	15	-15	10	0	4
	VF6				15	-15	-10	0	
Common-mode Rejection Ratio (Input common-mode Voltage Range)	VF7	ON	ON	OFF	15	-15	0	-15	5
	VF8				15	-15	0	13	
Power Supply Rejection Ratio	VF9	ON	ON	OFF	2	-2	0	0	6
	VF10				15	-15	0	0	

-Calculation-

1. Input Offset Voltage (Vio)

$$V_{io} = \frac{|VF1|}{1 + R_f / R_s} \quad [V]$$

2. Input Offset Current (Iio)

$$I_{io} = \frac{|VF2 - VF1|}{R_i \times (1 + R_f / R_s)} \quad [A]$$

3. Input Bias Current (Ib)

$$I_b = \frac{|VF4 - VF3|}{2 \times R_i \times (1 + R_f / R_s)} \quad [A]$$

4. Large Signal Voltage Gain (Av)

$$A_v = 20 \times \text{Log} \frac{\Delta E_k \times (1 + R_f / R_s)}{|VF5 - VF6|} \quad [dB]$$

5. Common-mode Rejection Ration (CMRR)

$$CMRR = 20 \times \text{Log} \frac{\Delta V_{icm} \times (1 + R_f / R_s)}{|VF8 - VF7|} \quad [dB]$$

6. Power supply rejection ratio (PSRR)

$$PSRR = 20 \times \text{Log} \frac{\Delta V_{cc} \times (1 + R_f / R_s)}{|VF10 - VF9|} \quad [dB]$$

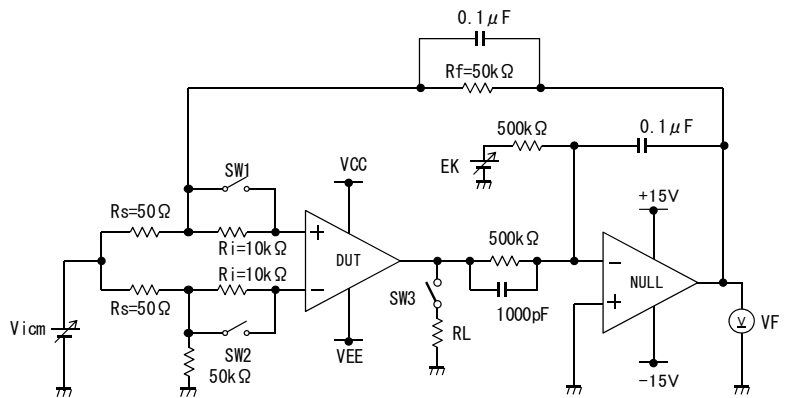


Figure 24. Test circuit 1 (one channel only)

Switch Condition for Test Circuit 2

SW No.	SW 1	SW 2	SW 3	SW 4	SW 5	SW 6	SW 7	SW 8	SW 9	SW 10	SW 11	SW 12	SW 13	SW 14
Supply Current	OFF	OFF	OFF	ON	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	OFF
High Level Output Voltage	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	ON	OFF
Low Level Output Voltage	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	ON	OFF
Output Source Current	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
Output Sink Current	OFF	OFF	ON	OFF	OFF	ON	OFF	OFF	OFF	OFF	OFF	OFF	OFF	ON
Slew Rate	OFF	OFF	OFF	ON	OFF	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF
Gain Bandwidth Product	OFF	ON	OFF	OFF	ON	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF
Equivalent Input Noise Voltage	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	OFF	OFF	OFF

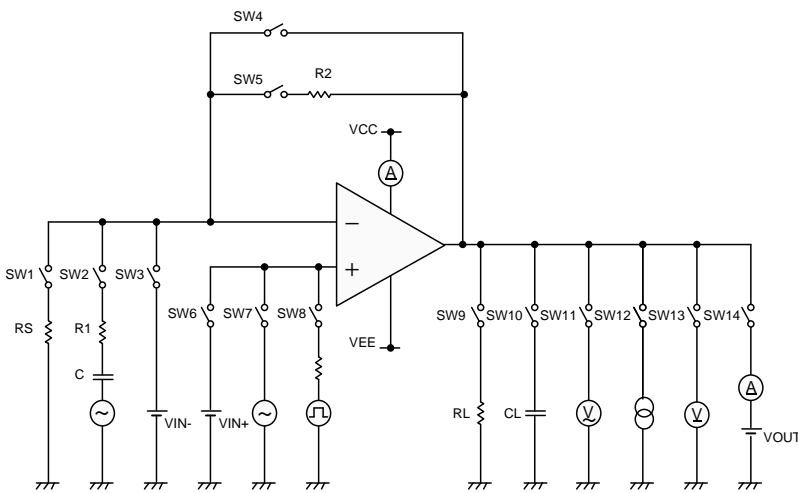


Figure 25. Test Circuit 2 (each Op-Amp)

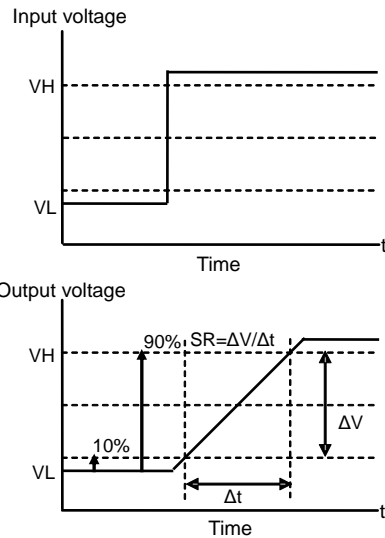


Figure 26. Slew Rate Input Waveform

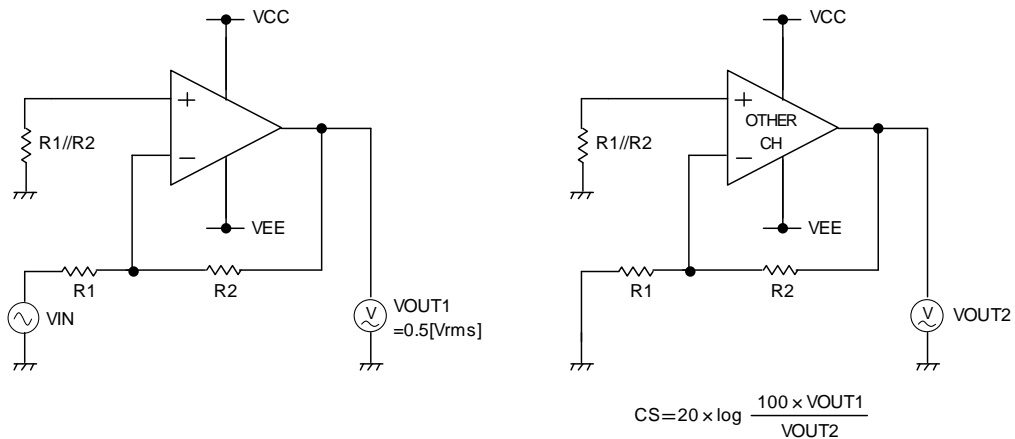


Figure 27. Test Circuit 3 (Channel Separation)

Application example

○Voltage follower

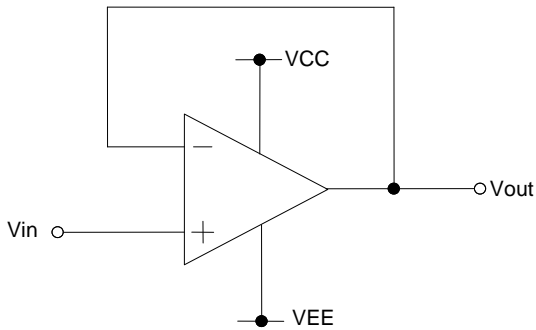


Figure 28. Voltage follower circuit

Voltage gain is 0 dB.
 This circuit controls output voltage (Vout) equal input voltage (Vin), and keeps Vout with stable because of high input impedance and low output impedance.
 Vout is shown next formula.
 $V_{out}=V_{in}$

○Inverting amplifier

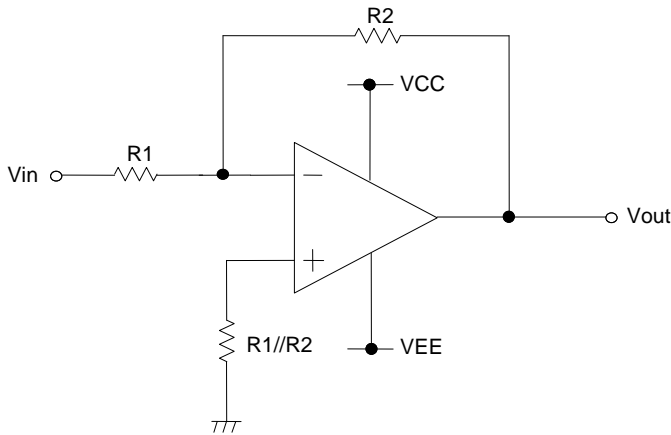


Figure 29. Inverting amplifier circuit

For inverting amplifier, Vin is amplified by voltage gain decided R1 and R2, and phase reversed voltage is output.
 Vout is shown next expression.
 $V_{out}=-\left(\frac{R_2}{R_1}\right) \cdot V_{in}$
 Input impedance is R1.

○Non-inverting amplifier

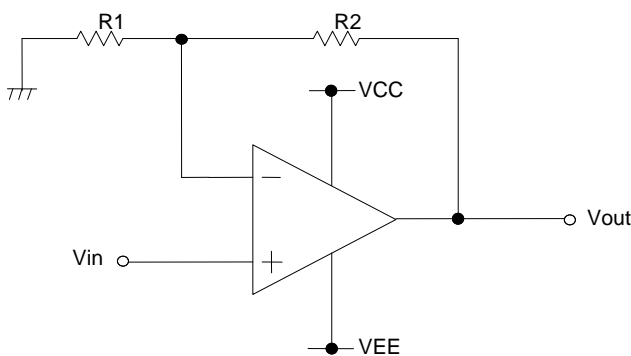


Figure 30. Non-inverting amplifier circuit

For non-inverting amplifier, Vin is amplified by voltage gain decided R1 and R2, and phase is same with Vin.
 Vout is shown next expression.
 $V_{out}=\left(1+\frac{R_2}{R_1}\right) \cdot V_{in}$
 This circuit performs high input impedance because Input impedance is operational amplifier's input Impedance.

●Power Dissipation

Power dissipation (total loss) indicates the power that can be consumed by IC at Ta=25°C(normal temperature). IC is heated when it consumed power, and the temperature of IC chip becomes higher than ambient temperature. The temperature that can be accepted by IC chip depends on circuit configuration, manufacturing process, and consumable power is limited. Power dissipation is determined by the temperature allowed in IC chip (maximum junction temperature) and thermal resistance of package (heat dissipation capability). The maximum junction temperature is typically equal to the maximum value in the storage temperature range. Heat generated by consumed power of IC radiates from the mold resin or lead

frame of the package. The parameter which indicates this heat dissipation capability (hardness of heat release) is called thermal resistance, represented by the symbol θ_{ja} °C/W.The temperature of IC inside the package can be estimated by this thermal resistance. Figure 31. (a) shows the model of thermal resistance of the package. Thermal resistance θ_{ja} , ambient temperature Ta, maximum junction temperature Tjmax, and power dissipation Pd can be calculated by the equation below:

$$\theta_{ja} = (T_{jmax} - T_a) / P_d \quad \text{°C/W} \quad \dots \dots \dots (I)$$

Derating curve in Figure 31. (b) indicates power that can be consumed by IC with reference to ambient temperature. Power that can be consumed by IC begins to attenuate at certain ambient temperature. This gradient is determined by thermal resistance θ_{ja} . Thermal resistance θ_{ja} depends on chip size, power consumption, package, ambient temperature, package condition, wind velocity, etc even when the same of package is used.

Thermal reduction curve indicates a reference value measured at a specified condition. Figure 32. (c) show a derating curve for an example of BA3404.

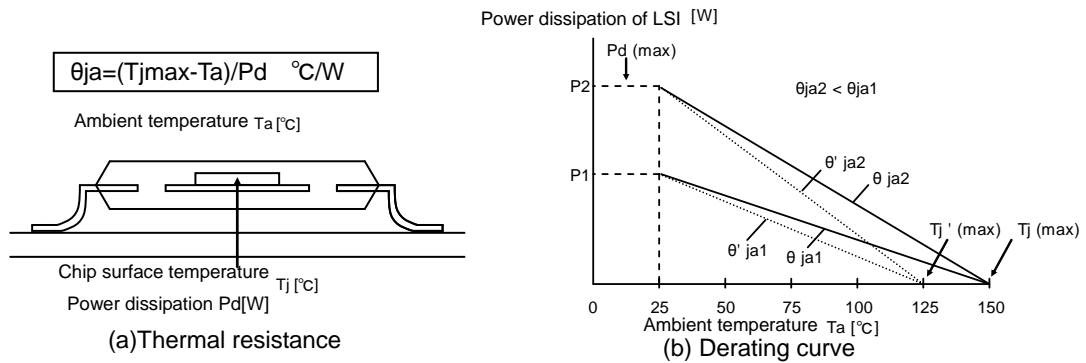
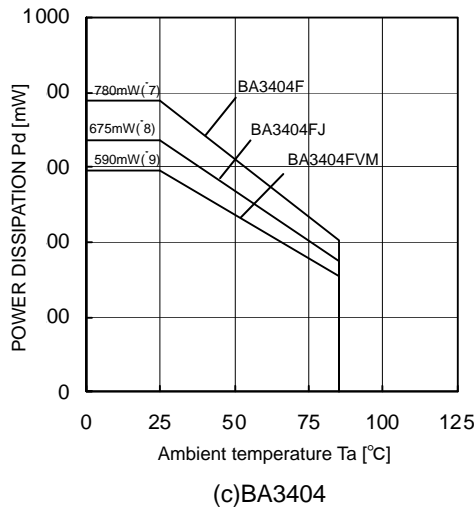


Figure 31. Thermal resistance and derating



(c)BA3404

(*7)	(*8)	(*9)	Unit
6.2	5.4	4.8	mW/°C

When using the unit above Ta=25°C, subtract the value above per degree °C.
Permissible dissipation is the value when FR4 glass epoxy board 70mm x70mm x1.6mm (cooper foil area below 3%) is mounted.

Figure 32. Derating curve

●Operational Notes

1) Unused circuits

When there are unused circuits, it is recommended that they be connected as in Figure 33. setting the non-inverting input terminal to a potential within the in-phase input voltage range (V_{icm}).

2) Input voltage

Applying $VEE+36V$ (BA3404) to the input terminal is possible without causing deterioration of the electrical characteristics or destruction, irrespective of the supply voltage. However, this does not ensure normal circuit operation. Please note that the circuit operates normally only when the input voltage is within the common mode input voltage range of the electric characteristics.

3) Power supply (single / dual)

The op-amp operates when the voltage supplied is between VCC and VEE Therefore, the single supply op-mp can be used as a dual supply op-amp as well.

4) Power dissipation (P_d)

Using the unit in excess of the rated power dissipation may cause deterioration in electrical characteristics due to the rise in chip temperature, including reduced current capability. Therefore, please take into consideration the power dissipation (P_d) under actual operating conditions and apply a sufficient margin in thermal design. Refer to the thermal derating curves for more information.

5) Short-circuit between pins and erroneous mounting

Incorrect mounting may damage the IC. In addition, the presence of foreign substances between the outputs, the output and the power supply, or the output and GND may result in IC destruction.

6) Operation in a strong electromagnetic field

Operation in a strong electromagnetic field may cause malfunctions.

7) Radiation

This IC is not designed to withstand radiation.

8) IC handling

Applying mechanical stress to the IC by deflecting or bending the board may cause fluctuation of the electrical characteristics due to piezo resistance effects.

9) IC operation

The output stage of the IC is configured using Class C push-pull circuits. Therefore, when the load resistor is connected to the middle potential of VCC and VEE, crossover distortion occurs at the changeover between discharging and charging of the output current. Connecting a resistor between the output terminal and GND, and increasing the bias current for Class A operation will suppress crossover distortion.

10) Board inspection

Connecting a capacitor to a pin with low impedance may stress the IC. Therefore, discharging the capacitor after every process is recommended. In addition, when attaching and detaching the jig during the inspection phase, ensure that the power is turned OFF before inspection and removal. Furthermore, please take measures against ESD in the assembly process as well as during transportation and storage.

11) Output capacitor

Discharge of the external output capacitor to VCC is possible via internal parasitic elements when VCC is shorted to VEE, causing damage to the internal circuitry due to thermal stress. Therefore, when using this IC in circuits where oscillation due to output capacitive load does not occur, such as in voltage comparators, use an output capacitor with a capacitance less than $0.1\mu F$.

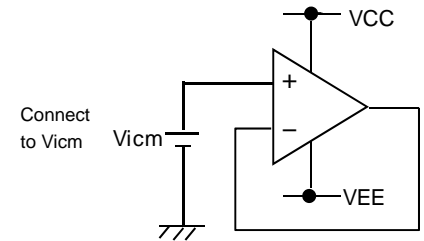


Figure 33. The example of application circuit for unused op-amp

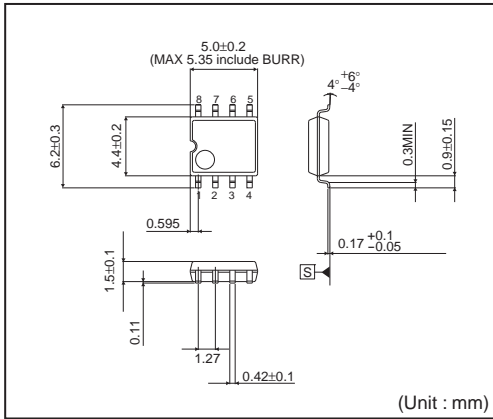
Status of this document

The Japanese version of this document is formal specification. A customer may use this translation version only for a reference to help reading the formal version.

If there are any differences in translation version of this document formal version takes priority.

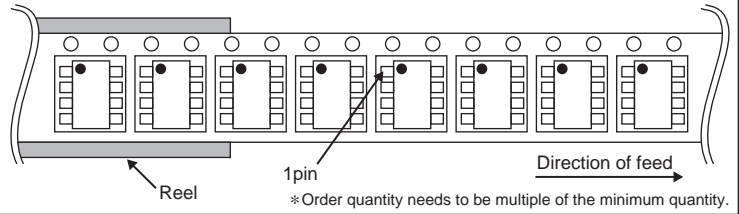
●Physical Dimensions Tape and Reel Information

SOP8

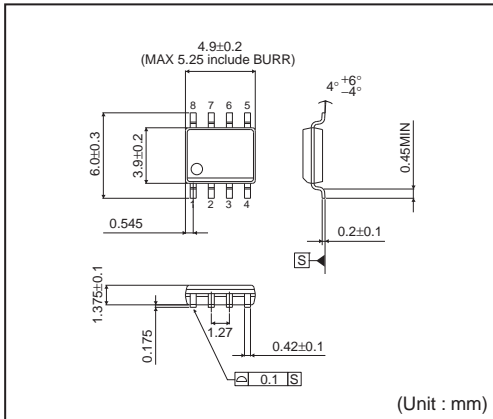


<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

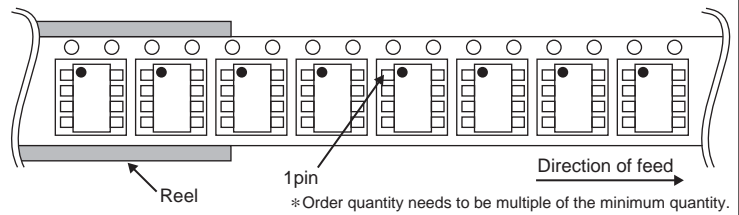


SOP-J8

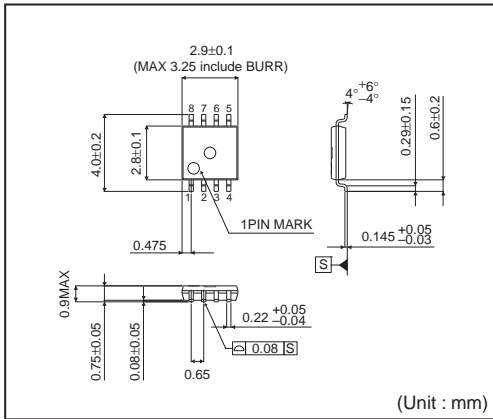


<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)

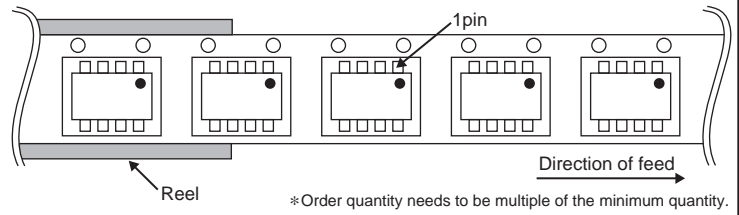


MSOP8

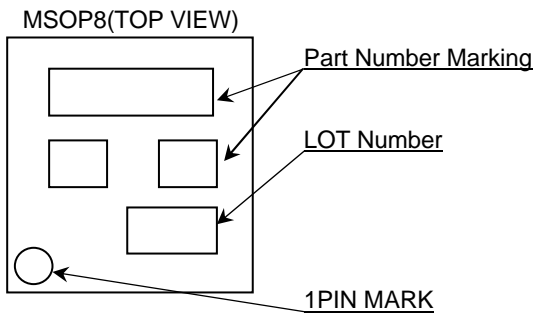
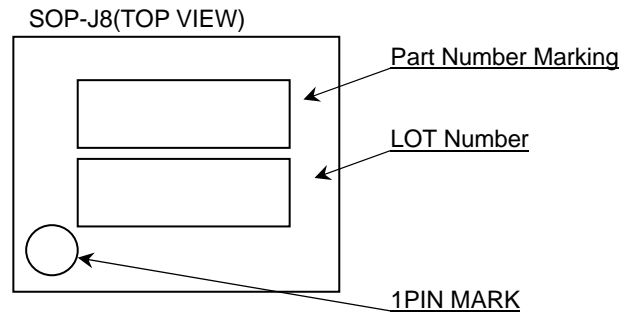
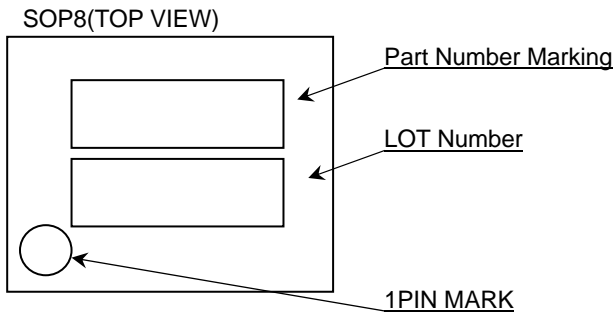


<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	TR (The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand)



●Marking Diagrams

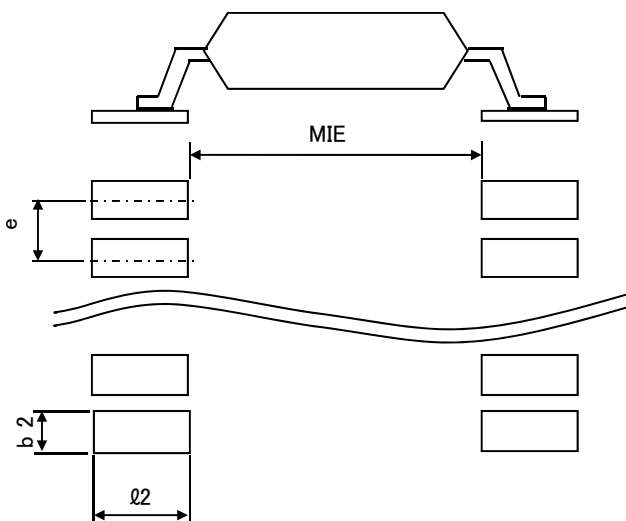


Product Name		Package Type	Marking
BA3404	F	SOP8	3404
	FJ	SOP-J8	
	FVM	MSOP8	

●Land pattern data

all dimensions in mm

PKG	Land pitch e	Land space MIE	Land length $\geq l_2$	Land width b2
SOP8	1.27	4.60	1.10	0.76
SOP-J8	1.27	3.90	1.35	0.76
MSOP8	0.65	2.62	0.99	0.35



●Revision History

Date	Revision	Changes
2012.10.22	001	New Release

Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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 - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used; if flow soldering method is preferred, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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