

100mA Variable Output LDO Regulator

BD00FA1WEFJ

General Description

BD00FA1WEFJ is an LDO regulator with output current capability of 0.1A. The Output voltage can be varied from 3.0V to 12.0V using external resistors with $\pm 1\%$ reference voltage accuracy. The HTSOP-J8 package can be used in wide variety of digital appliances. As protective function to prevent IC from destruction, this chip has built-in over current protection circuit to protect the device when output is shorted, zero μA shutdown mode, and built-in thermal shutdown circuit to protect the IC during thermal over load conditions. This product can be used in wide variety of digital appliances. This regulator can use ceramic capacitor, which have smaller size and longer life than other capacitors.

Features

- Built-in high accuracy reference voltage circuit
- Built-in Over current protection circuit (OCP)
- Built-in Temperature protection circuit (TSD)
- Zero μA shutdown mode
- Soft start function

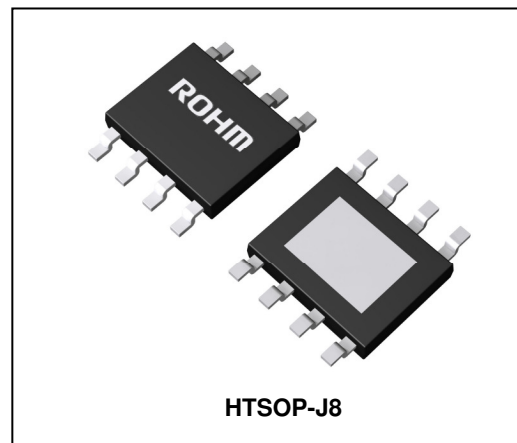
Key Specifications

- Input power supply voltage range: $V_{\text{in}}+3.0\text{V}$ to 25.0V
- Output voltage: 3.0V to 12.0V
- Output current: 0.1A (Max)
- Shutdown current: 0 μA (Typ)
- Operating temperature range: -25°C to $+85^\circ\text{C}$

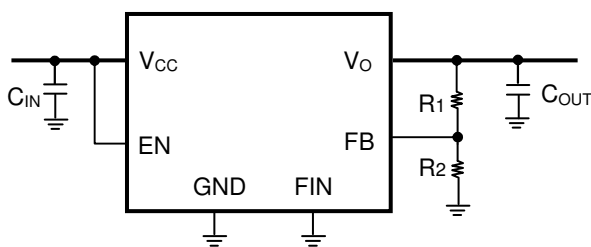
Package

HTSOP-J8

W(Typ) D(Typ) H(Max)
4.90mm x 6.00mm x 1.00mm



Typical Application Circuit



$C_{\text{IN}}, C_{\text{OUT}}$: Ceramic Capacitor

Ordering Information

B D 0 0 F A 1 W E F J - **E 2**

Part Number	Output voltage	Input Voltage	Output Current	Shutdown Mode	Package	Packaging and forming specification
	00:Variable	F:30V	A1:0.1A	"W":Included	EFJ:HTSOP-J8	E2:Emboss tape reel

○ Product structure : Silicon monolithic integrated circuit ○ This product is not designed to have protection against radioactive rays.

Block Diagram
BD00FA1WEFJ

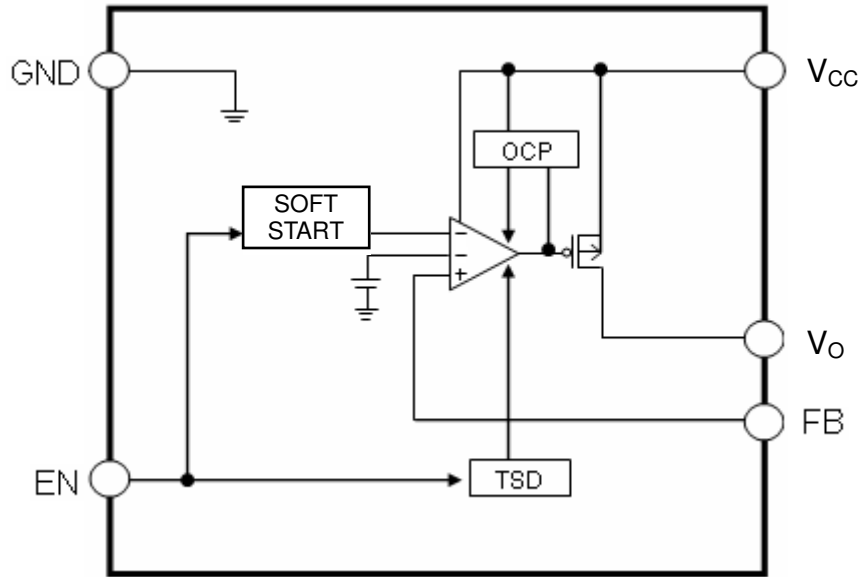
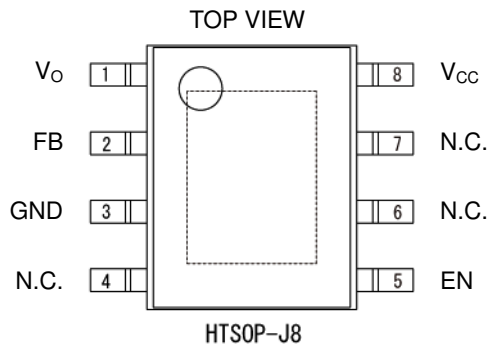


Figure 1. Block Diagram

Pin Configuration



Pin Description

Pin No.	Pin Name	Pin Function
1	V _O	Output pin
2	FB	Feedback pin
3	GND	GND pin
4	N.C.	No Connection (Connect to GND or leave OPEN)
5	EN	Enable pin
6	N.C.	No Connection (Connect to GND or leave OPEN)
7	N.C.	No Connection (Connect to GND or leave OPEN)
8	V _{CC}	Input pin
Reverse	FIN	Substrate(Connect to GND)

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit
Power supply voltage	V _{CC}	30.0 * ¹	V
EN voltage	V _{EN}	30.0	V
Power dissipation	HTSOP-J8 Pd* ²	2110 * ²	mW
Operating temperature range	T _{opr}	-25 to + 85	°C
Storage temperature range	T _{stg}	-55 to + 150	°C
Maximum junction temperature	T _{jmax}	+150	°C

*1 Not to exceed Pd.

*2 In case Ta ≥ 25°C (When mounted on a two-layer glass epoxy board with 70mm × 70mm × 1.6mm dimension) is reduced by 16.9mW/°C

Recommended Operating Conditions (Ta=25°C)

Parameter	Symbol	Min	Max	Unit
Input power supply voltage	V _{CC}	V _o +3.0	25.0	V
EN voltage	V _{EN}	0.0	25.0	V
Output voltage setting range	V _O	3.0	12.0	V
Output current	I _O	0.0	0.1	A

Recommended Operating Condition

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Output Capacitor	C _{OUT}	1.0 * ³	2.2	-	μF	Ceramic capacitor recommended

*3 The minimum value of capacitor must met this specification over full operating conditions. (Ex: Temperature, DC bias)

Electrical Characteristics (Unless otherwise specified, V_{CC}=10V, EN=3V, R1=52.5kΩ, R2=10kΩ, Ta=25°C)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Circuit current at shutdown mode	I _{SD}	-	0	5	μA	V _{EN} =0V, OFF mode
Bias current	I _{CC}	-	300	450	μA	
Line Regulation	Reg. _I	-1	0.5	1	%	V _{CC} =(V _o +3V)→25.0V
Load Regulation	Reg. _{I_O}	-1.5	0.5	1.5	%	I _O =0→0.1A
Minimum dropout voltage	V _{CO}	-	2.0	3.0	V	I _O =0.1A
Output reference voltage	V _{FB}	0.792	0.800	0.808	V	I _O =0A
EN Low voltage	V _{EN} (Low)	0	-	0.8	V	
EN High voltage	V _{EN} (High)	2.4	-	25.0	V	
EN Bias current	I _{EN}	1	3	9	μA	

Performance Curve (Reference Data)

(Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{cc}=10\text{V}$, $V_{EN}=3\text{V}$, $R_1=52.5\text{k}\Omega$, $R_2=10\text{k}\Omega$, $C_{IN}=C_{OUT}=2.2\mu\text{F}$)

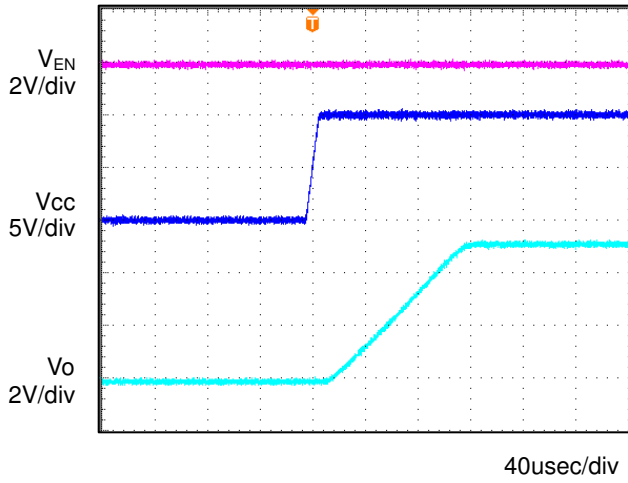


Figure 2. Input sequence
($C_{OUT} = 1\mu\text{F}$)

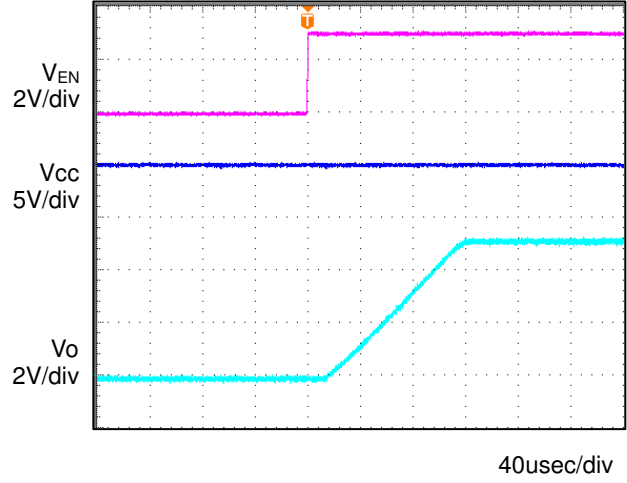


Figure 3. Input sequence
($C_{OUT} = 1\mu\text{F}$)

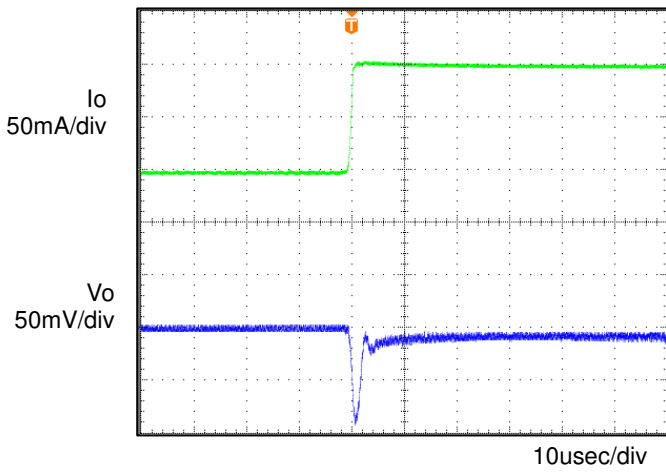


Figure 4. Transient Response
($I_o = 0\text{A} \rightarrow 0.1\text{A}$)
($C_{OUT} = 1\mu\text{F}$)

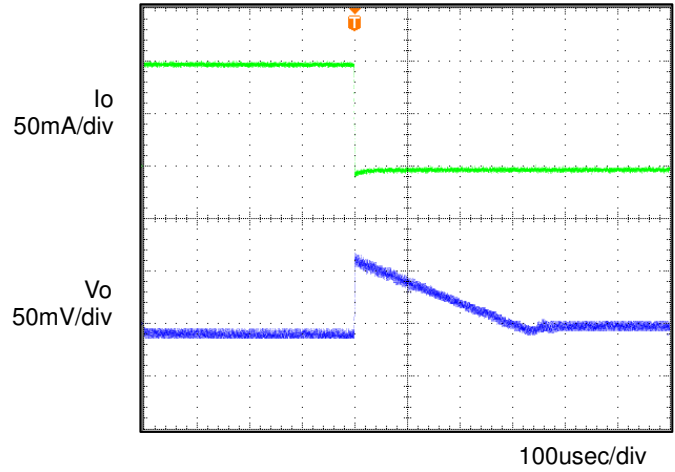


Figure 5. Transient Response
($I_o = 0.1\text{A} \rightarrow 0\text{A}$)
($C_{OUT} = 1\mu\text{F}$)

Performance Curve (Reference Data)

(Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{cc}=10\text{V}$, $V_{EN}=3\text{V}$, $R_1=52.5\text{k}\Omega$, $R_2=10\text{k}\Omega$, $C_{IN}=C_{OUT}=2.2\mu\text{F}$)

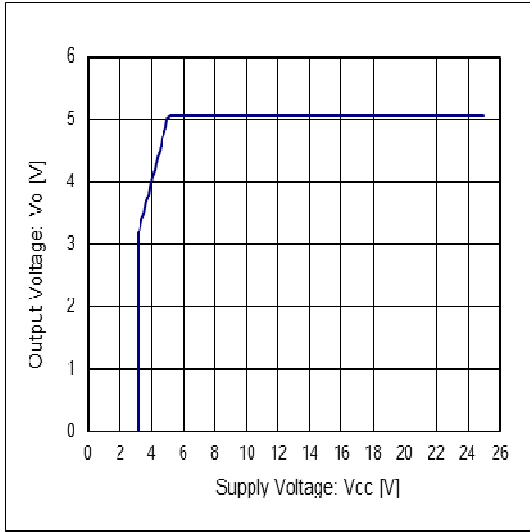


Figure 6. Vo - Vcc

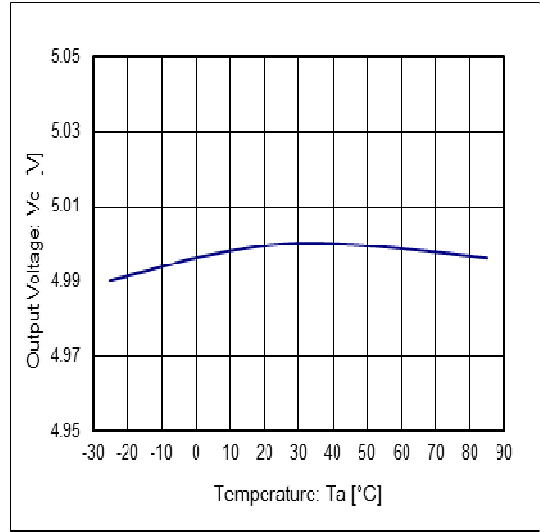


Figure 7. Vo - Ta
(Io = 0mA)

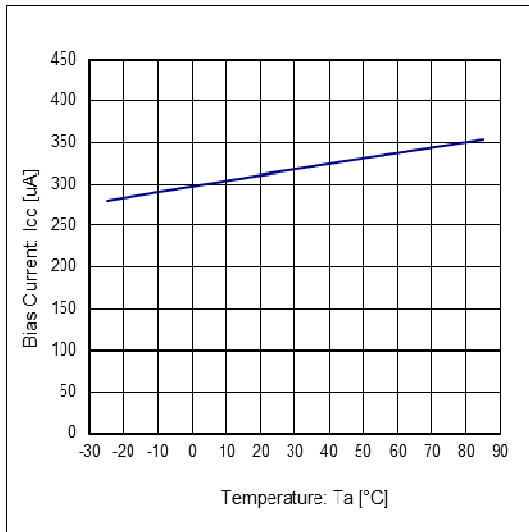


Figure 8. Icc - Ta

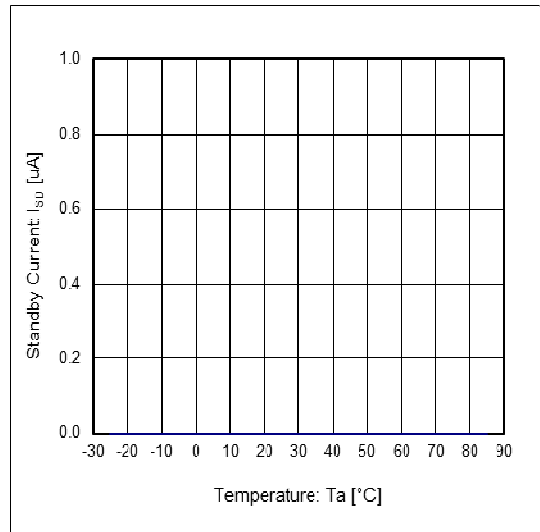


Figure 9. Isd - Ta
(VEN=0V)

Performance Curve (Reference Data)

(Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{cc}=10\text{V}$, $EN=3\text{V}$, $R_1=52.5\text{k}\Omega$, $R_2=10\text{k}\Omega$, $C_{IN}=C_{OUT}=2.2\mu\text{F}$)

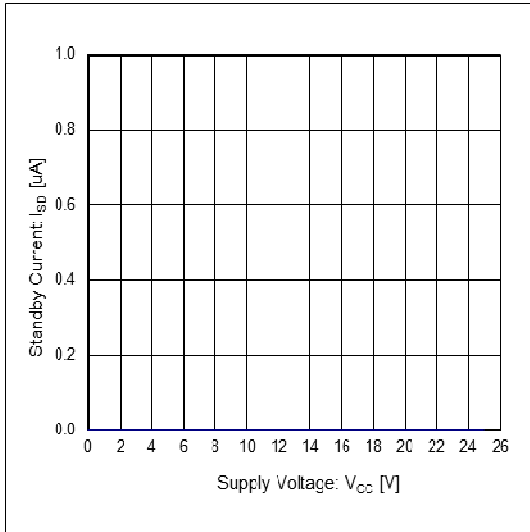


Figure 10. I_{SD} - V_{CC}
($V_{EN}=0\text{V}$)

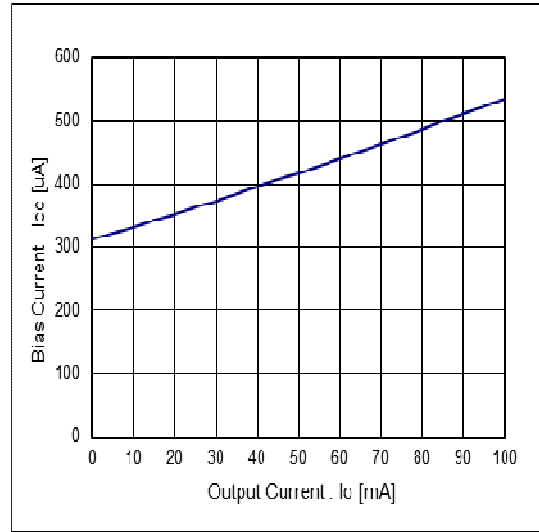


Figure 11. I_{CC} - I_O

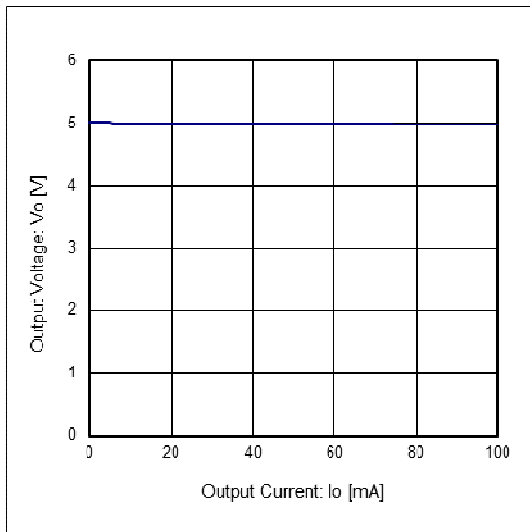


Figure 12. V_O - I_O

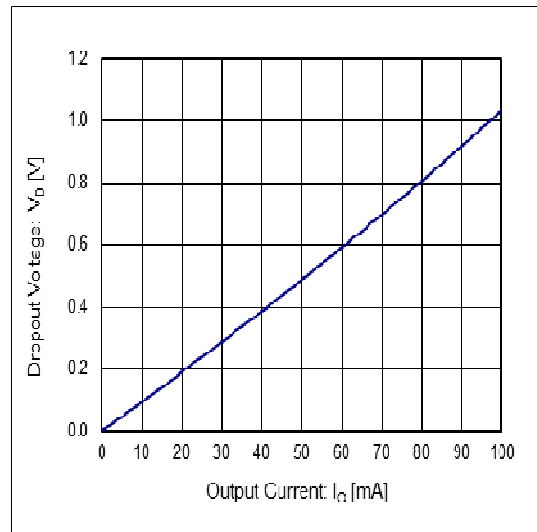


Figure 13. Minimum Dropout Voltage

Performance Curve (Reference Data)

(Unless otherwise specified, $T_a=25^\circ\text{C}$, $V_{cc}=10\text{V}$, $E_N=3\text{V}$, $R_1=52.5\text{k}\Omega$, $R_2=10\text{k}\Omega$, $C_{IN}=C_{OUT}=2.2\mu\text{F}$)

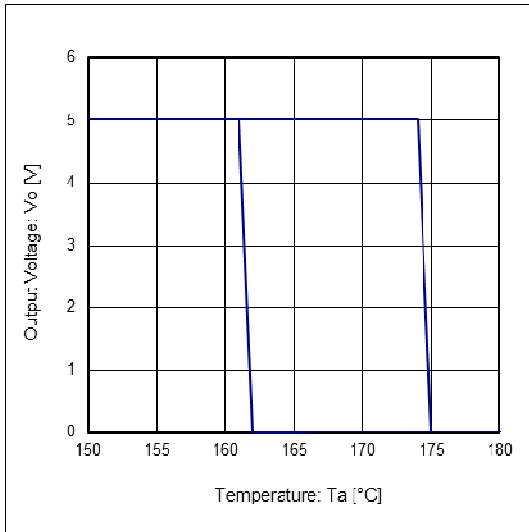


Figure 14. TSD
($I_o = 0\text{mA}$)

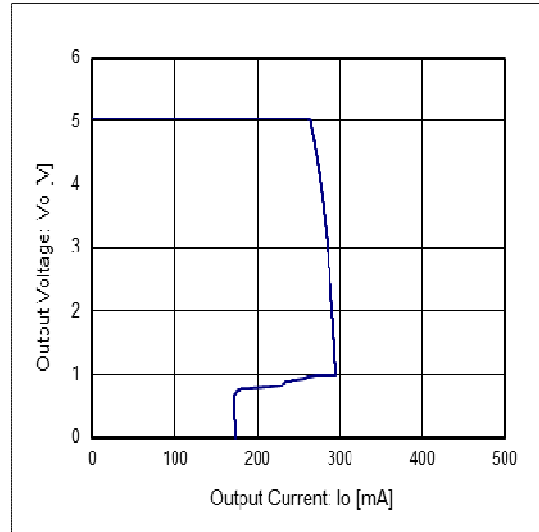


Figure 15. OCP

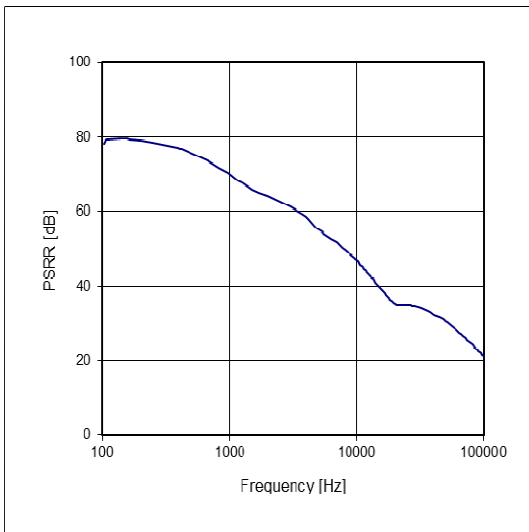
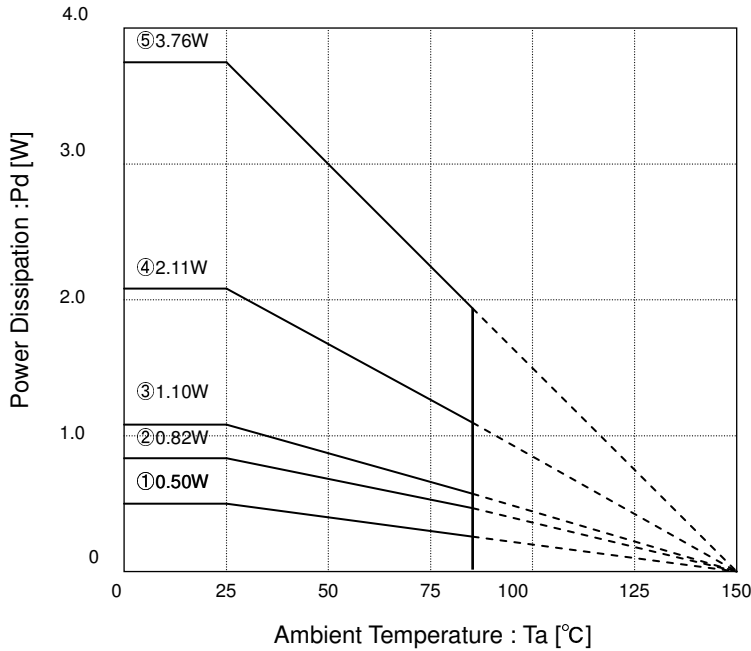


Figure 16. PSRR
($I_o = 0\text{mA}$)

Power Dissipation

ⓄHTSOP-J8



Measurement condition: mounted on a ROHM board

PCB size: 70mm × 70mm × 1.6mm
(PCB with thermal via)

- Solder the thermal pad to Ground

- ① IC only
 $\theta_{j-a}=249.5^{\circ}\text{C/W}$
- ② 1-layer (copper foil : 0mm × 0mm)
 $\theta_{j-a}=153.2^{\circ}\text{C/W}$
- ③ 2-layer (copper foil : 15mm × 15mm)
 $\theta_{j-a}=113.6^{\circ}\text{C/W}$
- ④ 2-layer (copper foil : 70mm × 70mm)
 $\theta_{j-a}=59.2^{\circ}\text{C/W}$
- ⑤ 4-layer (copper foil : 70mm × 70mm)
 $\theta_{j-a}=33.3^{\circ}\text{C/W}$

When considering thermal design, operation should be maintained within the following conditions.
(The temperature mentioned below is a guaranteed temperature, therefore, margins must be considered.)

1. Ambient temperature T_a is 85°C and below.
2. Junction temperature T_j is 150°C and below.

The junction temperature T_j can be determined as follows:
Calculation based on ambient temperature T_a

$$T_j = T_a + \theta_{j-a} \times W$$

<Reference Value>

θ_{j-a} : HTSOP-J8	153.2°C/W	1-layer PCB (copper foil density 0mm × 0mm)
	113.6°C/W	2-layer PCB (copper foil density 15mm × 15mm)
	59.2°C/W	2-layer PCB (copper foil density 70mm × 70mm)
	33.3°C/W	4-layer PCB (copper foil density 70mm × 70mm)
		PCB size: 70mm × 70mm × 1.6mm (PCB with thermal via)

Most of the heat loss that occurs in BD00FA1WEFJ is generated from the output Pch FET. Power loss is determined by the product of voltage drop across $V_{cc}-V_o$ and the output current. Check the conditions of output voltage and output current to be used between $V_{cc}-V_o$ and compare with the power dissipation characteristics.

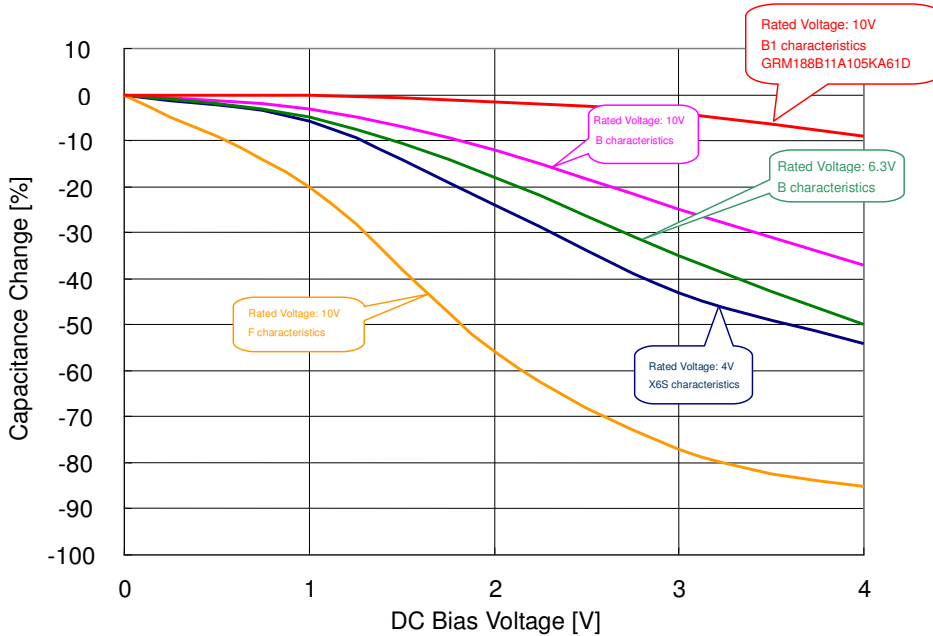
In addition, power dissipation may change significantly due to board conditions because BD00FA1WEFJ uses power package. It is important to consider the board size to be used before proceeding with the design.

$$\text{Power consumption [W]} = \{ \text{Input voltage (Vcc)} - \text{Output voltage (Vo)} \} \times \text{Output current (Io: Ave)}$$

Input / Output Capacitor

It is recommended that a capacitor is placed close to pin between input pin and GND as well as output pin and GND. The input capacitor becomes more necessary when the power supply impedance is high or when the PCB trace has significant length. Moreover, the higher the capacitance of the output capacitor the more stable the output will be, even with load and line voltage variations. However, please check the actual functionality by mounting on a board for the actual application. Also, ceramic capacitors usually have different thermal and equivalent series resistance characteristics and may degrade gradually over continued use.

For additional details, please check with the manufacturer and select the best ceramic capacitor for your application.



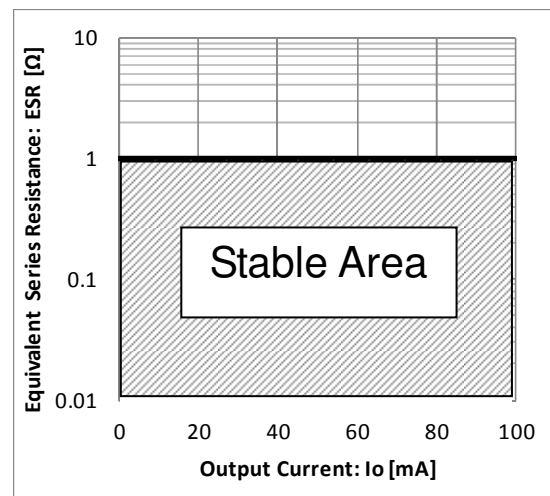
Ceramic Capacitor Capacitance Value— DC Bias Characteristics (Characteristics Example)

Output Capacitor Equivalent Series Resistance

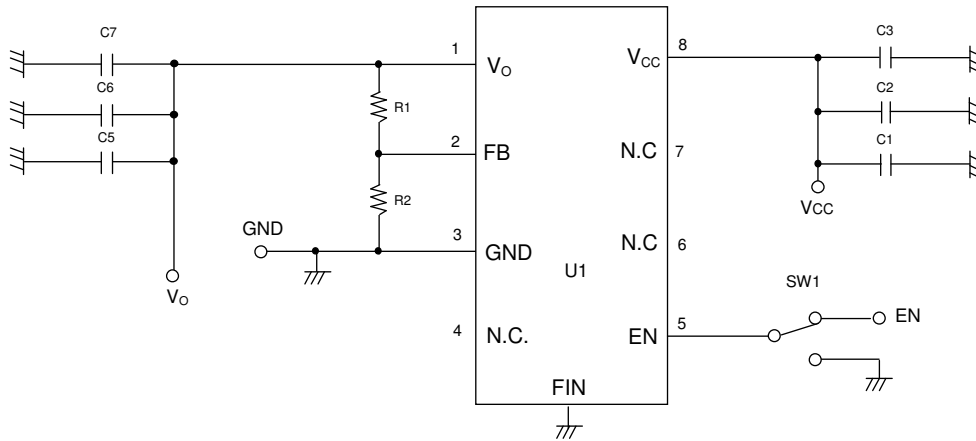
To prevent oscillation, please attach a capacitor between V_O and GND. Generally, capacitor has ESR (Equivalent Series Resistance). Operation will be stable in ESR-lo range shown in the right.

The 2.2 μ F ceramic capacitor and resistor at output in this characteristic data are connected in series and measured. Generally, ESR of ceramic capacitor, tantalum capacitor and electrolytic capacitor is different. Check the ESR of capacitor to be used and use it within the range of stable region.

However, please take note that for the same value of capacitance of different electrolytic capacitor, ESR are not always the same. In addition, ESR characteristics may also change due to wiring impedance of board, input power impedance and load impedance; therefore check the behavior in actual application.



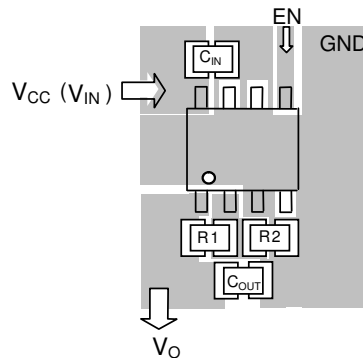
Evaluation Board Circuit



Evaluation Board Parts List

Designation	Value	Part No.	Company	Designation	Value	Part No.	Company
R1	52.5k Ω	-	-	C4	-	-	-
R2	10k Ω	-	-	C5	2.2 μ F	CM21CH222J50AT	KYOCERA
R3	-	-	-	C6	-	-	-
R4	-	-	-	C7	-	-	-
R5	-	-	-	C8	-	-	-
R6	-	-	-	C9	-	-	-
C1	2.2 μ F	CM21CH222J50AT	KYOCERA	C10	-	-	-
C2	-	-	-	U1	-	BD00FA1WEFJ	ROHM
C3	-	-	-	U2	-	-	-

Board Layout

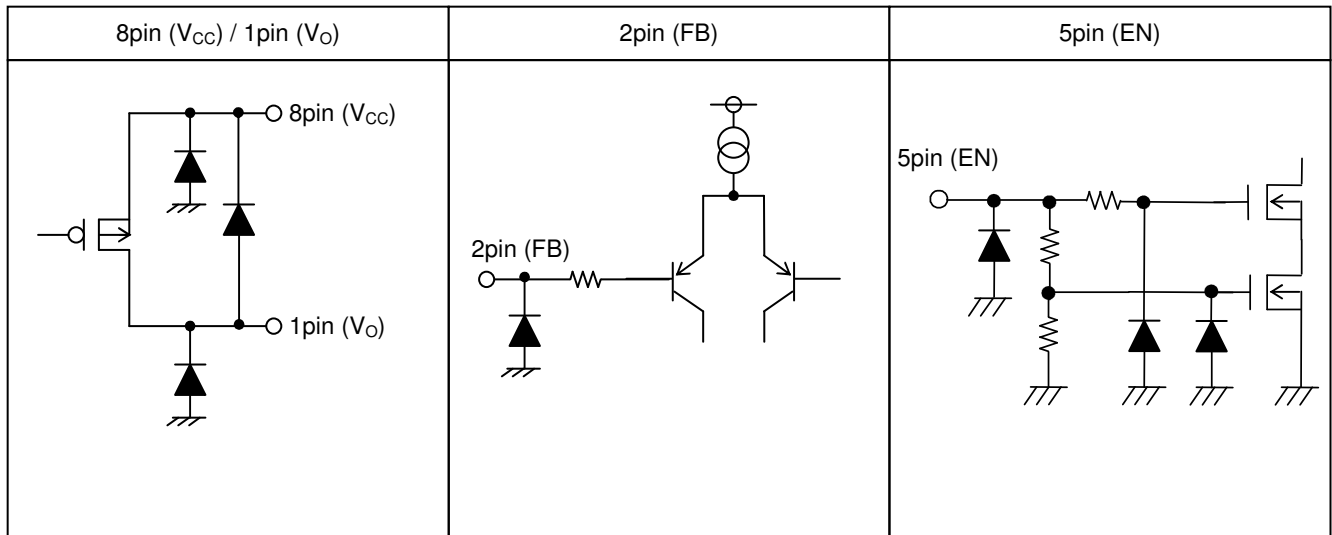


- Input capacitor C_{IN} connected to $V_{CC} (V_{IN})$ should be placed as close as possible to $V_{CC}(V_{IN})$ pin and use wide layout. Output capacitor C_{OUT} should also be placed as close as possible to IC pin. In case connected to inner layer GND plane, please use several through hole.
- FB pin has comparatively high impedance and can be affected by noise, so floating capacitance should be small as possible. Please be careful of this during layout.
- Please make GND pattern wide enough to handle the power dissipation of the chip.
- For output voltage setting, Output voltage can be set by FB pin voltage (0.800V typ.) and external resistance R1, R2.

$$V_O = V_{FB} \times \frac{R_1 + R_2}{R_2}$$

(The use of resistor $R_2 = 5k\Omega$ to $15k\Omega$ is recommended)

Input/Output Equivalent Circuits



Operational Notes

- (1) **Absolute Maximum Value Rate**
Operating the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. Therefore, it is important to consider circuit protection measures, like adding a fuse, in case the IC is operated in a special mode exceeding the absolute maximum ratings.
- (2) **Reverse connection of power supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.
- (3) **Power supply line**
Design the PCB layout pattern to provide low impedance ground and supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.
- (4) **Ground voltage**
The voltage of the ground pin must be the lowest voltage of all pins of the IC at all operating conditions. Ensure that no pins are at a voltage below the ground pin at any time, even during transient condition.
- (5) **Thermal consideration**
Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions.
- (6) **Recommended Operating Conditions**
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.
- (7) **Short between pins and mounting errors**
Be careful when mounting the IC on printed circuit boards. The IC may be damaged if it is mounted in a wrong orientation or if pins are shorted together. Short circuit may be caused by conductive particles caught between the pins.
- (8) **Operation under strong electromagnetic field**
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.
- (9) **ASO**
Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).
- (10) **Thermal shutdown circuit**
The IC incorporates a built-in thermal shutdown circuit, which is designed to turn off the IC when the internal temperature of the IC reaches a specified value. It is not designed to protect the IC from damage or guarantee its operation. Do not continue to operate the IC after this function is activated. Do not use the IC in conditions where this function will always be activated.

	TSD ON Temperature [°C] (typ)	Hysteresis Temperature [°C] (typ)
BD00FA1WEFJ	175	10

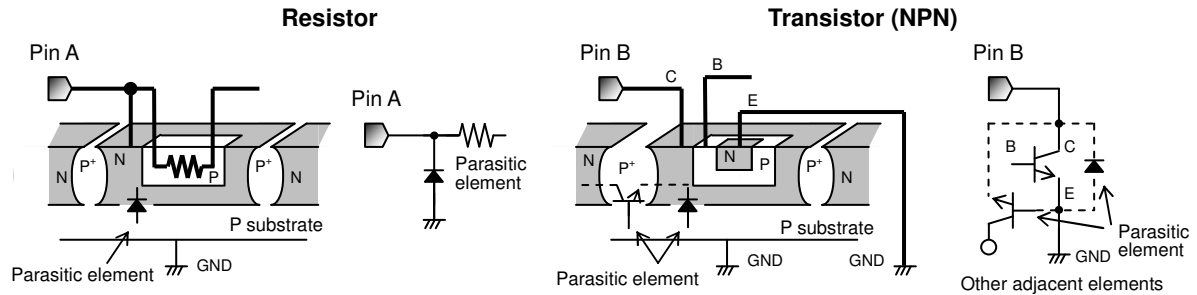
- (11) **Testing on application boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from electro static discharge, ground the IC during assembly and use similar precautions during transport and storage.

(12) Regarding input pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
 When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



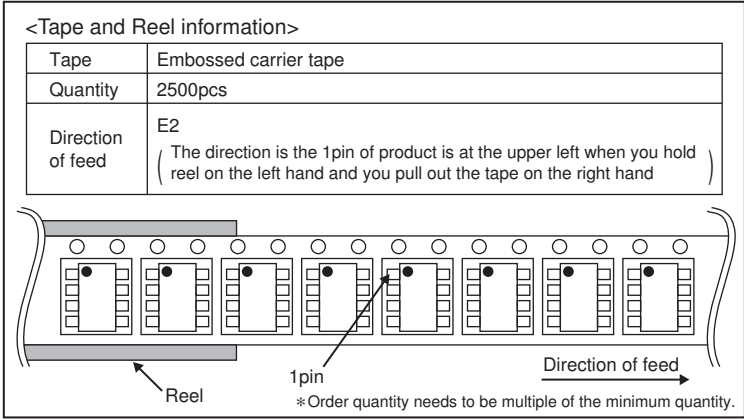
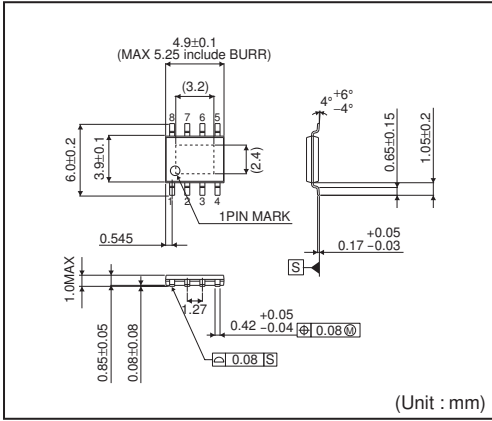
Example of monolithic IC structure

(13) Ground wiring pattern

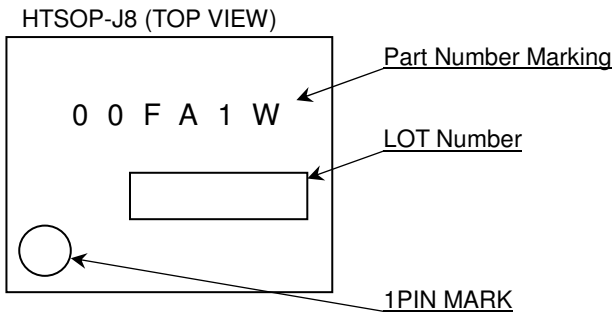
When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on the GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

Physical Dimension Tape and Reel Information

HTSOP-J8



Marking Diagram



Revision History

Date	Revision	Revision contents
2014.10.09	001	New release
2015.01.20	002	In Board Layout, "R1 = 5k Ω to 15k Ω " was changed to "R2 = 5k Ω to 15k Ω " (page 10)

Notice

Precaution on using ROHM Products

- Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment ^(Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

- ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
 - Installation of protection circuits or other protective devices to improve system safety
 - Installation of redundant circuits to reduce the impact of single or multiple circuit failure
- Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc. prior to use, must be necessary:
 - Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
 - Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
 - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.
2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
 - [a] the Products are exposed to sea winds or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - [b] the temperature or humidity exceeds those recommended by ROHM
 - [c] the Products are exposed to direct sunshine or condensation
 - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

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