Datasheet

Constant Current LED Drivers

Constant Current Controller for Automotive LED Lamps

BD18342FV-M

General Description

BD18342FV-M is 70V-withstanding constant current controller for automotive LED lamps. It is able to drive at maximum 10 rows of PNP transistors. It can also contribute to reduction in the consumption power of the set as it has the built-in standby function. The IC provides high reliability because it has LED open detection, short circuit protection, over voltage mute function and LED failure input/output function.

Features

- AEC-Q100 Qualified(Note 1)
- PWM Dimming Function
- LED Open Detection
- Short Circuit Protection (SCP)
- Over Voltage Mute Function (OVM)
- Disable LED Open Detection Function at Reduced-Voltage
- LED Failure Input/Output Functions (PBUS)

(Note 1) Grade1

Applications

- Automotive LED Exterior Lamp (Rear Lamp, Turn Lamp, DRL/Position Lamp, Fog Lamp etc.)
- Automotive LED Interior Lamp (Air Conditioner Lamp, Interior Lamp, Cluster Light etc.)

Key Specifications

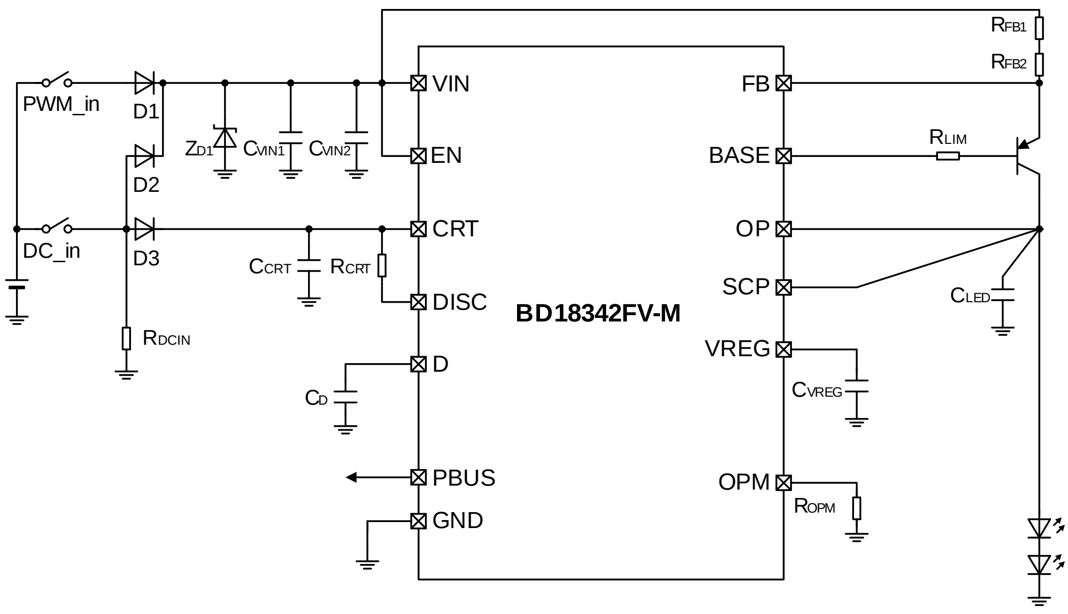
- Input Voltage Range: 4.5 V to 19 V
- FB Pin Voltage Accuracy: 650 mV ±3 % @Ta=25 °C to 125 °C
- Stand-by Current: 0 µA (Typ)
- Operating Temperature Range: -40 °C to +125 °C

Package

Package	W (Typ) x D (Typ) x H (Max)
SSOP-B16	5.00 mm x 6.40 mm x 1.35 mm

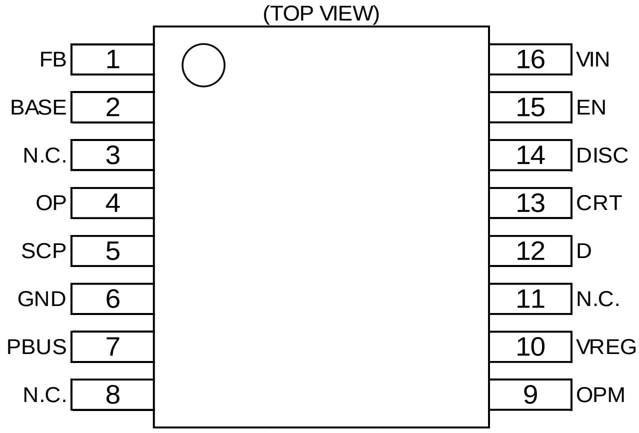
SSOP-B16

Typical Application Circuit



〇Product structure : Silicon integrated circuit 〇This product has no designed protection against radioactive rays

Pin Configuration

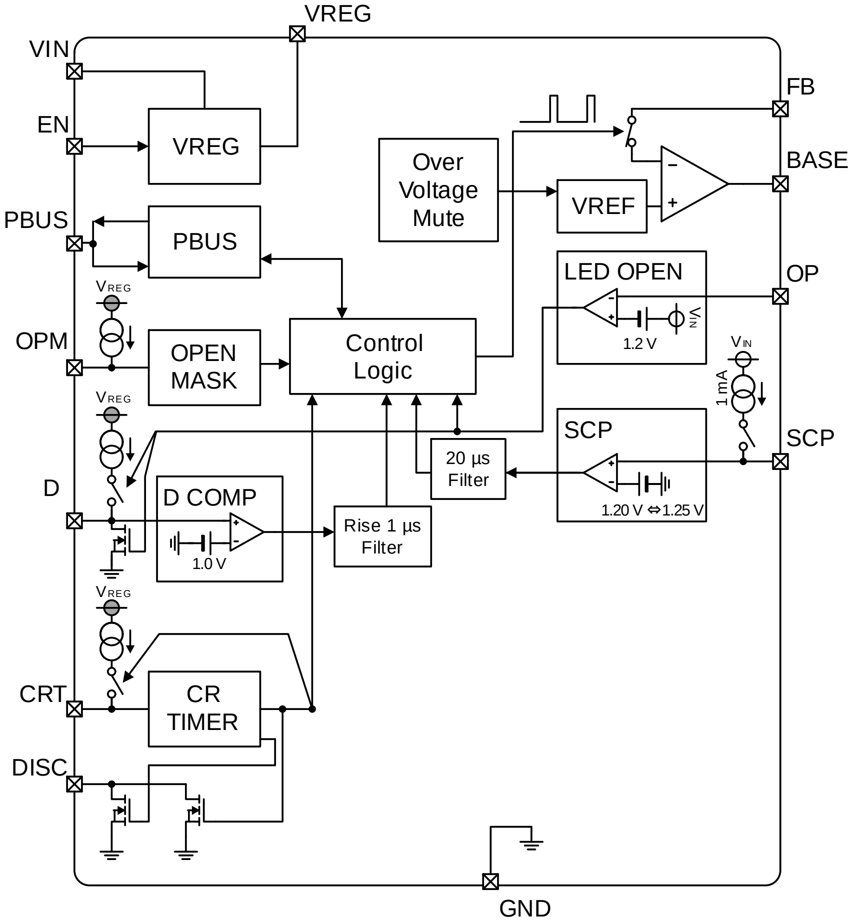


Pin Description

Pin No.	Pin Name	Function
1	FB	Feedback voltage input
2	BASE	Connecting PNP Tr. BASE
3	N.C.	No internal connection *(Note 1)*
4	OP	LED open detection input
5	SCP	Short circuit protection input
6	GND	GND
7	PBUS	Output for fault flag / Input to disable Output current
8	N.C.	No internal connection *(Note 1)*
9	OPM	Connecting resistor for disable LED open detection voltage setting at reduced voltage
10	VREG	Internal reference voltage output
11	N.C.	No internal connection *(Note 1)*
12	D	Connecting capacitor for disable LED open detection time setting
13	CRT	Connect capacitor and resistor to set output current ON Duty
14	DISC	Connecting resistor to set output current on time
15	EN	Enable input
16	VIN	Power supply input

(Note 1) Leave this pin unconnected

Block Diagram



Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating	Unit
Power Supply Voltage(VIN)	V_{IN}	-0.3 to +70.0	V
EN, CRT, DISC Pin Voltage	V_{EN}, V_{CRT}, V_{DISC}	-0.3 to +70.0	V
FB, BASE, OP, SCP Pin Voltage	V_{FB}, V_{BASE}, V_{OP},V_{SCP}	-0.3 to V_{IN}+0.3	V
VIN-FB, VIN-BASE Inter-Pin Voltage	V_{IN_FB}, V_{IN_BASE}	-0.3 to +5.0	V
PBUS, VREG Pin Voltage	V_{PBUS}, V_{REG}	-0.3 to +7.0	V
OPM, D Pin Voltage	V_{OPM}, V_{D}	-0.3 to V_{REG}+0.3	V
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
SSOP-B16				
Junction to Ambient	θ_{JA}	140.9	77.2	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	6	5	°C/W

(Note 1) Based on JESD51-2A(Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage(Note 1) (Note 2)	V_{IN}	4.5	13.0	19.0	V
CR TIMER Frequency Range	f_{PWM}	100	-	5000	Hz
PWM Minimum Pulse Width(Note 3)	t_{MIN}	10	-	-	µs
Operating Temperature	Topr	-40	-	+125	°C

(Note 1) ASO should not be exceeded
(Note 2) At start-up time, please apply a voltage 5 V or more once. The value is the voltage range after the temporary rise to 5 V or more.
(Note 3) At connecting the external PNP Tr. (2SAR573DFHG (ROHM), 1 pcs). That is the same when the pulse input to the CRT pin.

Operating Conditions

Parameter	Symbol	Min	Max	Unit
Capacitor Connecting VIN Pin 1	C_{VIN1}	1.0	-	µF
Capacitor Connecting VIN Pin 2	C_{VIN2}(Note 4)	0.047	-	µF
Capacitor Connecting VREG Pin	C_{VREG}(Note 5)	1.0	4.7	µF
Capacitor Connecting LED Anode	C_{LED}	0.10	0.68	µF
Capacitor for Setting CRT Timer	C_{CRT}	0.01	0.22	µF
Resistor for Setting CRT Timer	R_{CRT}	0.1	50.0	kΩ
Resistor for Setting LED Current	R_{FB1}, R_{FB2}(Note 6)	0.8	6.5	Ω
Resistor for Disable LED Open Detection Voltage Setting at Reduced Voltage	R_{OPM}	25	55	kΩ
Resistor for DCIN Pull-down	R_{DCIN}	-	10	kΩ
Capacitor for Setting Disable LED Open Detection Time	C_D(Note 5)	0.001	0.100	µF
Resistor for Limiting Base Pin Current	R_{LIM}	See Features Description 5		Ω
External PNP Transistor	Q_1	*(Note 7)*		-

(Note 4) Recommended ceramic capacitor. ROHM Recommended Value (0.1 µF GCM155R71H104KE37 murata)
(Note 5) Recommended ceramic capacitor. Please setting the Disable LED Open Detection Time less than PWM minimum pulse width.
(Note 6) At connecting the external PNP Tr. 2SAR573DFHG (ROHM), 1 pcs.
(Note 7) For external PNP transistor, please use the recommended device 2SAR573DFHG for this IC.
While using non-recommended part device, validate the design on actual board.
Please check hfe of the part to design base current limit resistor. (See Features Description, section 5).
As for parasitic capacitance, please evaluate over shoot of I_{LED} on actual board. (See Features Description, Section 8 -Evaluation example, I_{LED} pulse width at PWM Dimming operation).

Electrical Characteristics

(Unless otherwise specified Ta=-40 °C to +125 °C, V_{IN}=13 V, C_{VREG}=1.0 µF, Transistor PNP=2SAR573DFHG)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Circuit Current I_{VIN}]						
Circuit Current at Stand-by Mode	I_{VIN1}	-	0	10	µA	V_{EN}=0 V V_{FB}=V_{IN}
Circuit Current at Normal Mode	I_{VIN2}	-	2.0	5.0	mA	V_{EN}=V_{IN}, V_{FB}=V_{IN}-1.0 V Base Current Subtracted
Circuit Current at LED Open Detection	I_{VIN3}	-	2.0	5.0	mA	V_{EN}=V_{IN}, V_{FB}=V_{IN}-1.0 V
Circuit Current at PBUS=Low	I_{VIN4}	-	2.0	5.0	mA	V_{EN}=V_{IN}, V_{FB}=V_{IN}-1.0 V V_{PBUS}=0 V
[VREG Voltage]						
VREG Pin Voltage	V_{REG}	4.85	5.00	5.15	V	I_{VREG}=-100 µA Ta=25 °C to 125 °C
		4.75	5.00	5.25	V	I_{VREG}=-100µA Ta=-40 °C to +125 °C
VREG Pin Current Capability	I_{VREG}	-1.0	-	-	mA	
[DRV]						
FB Pin Voltage	V_{FBREG}	630	650	670	mV	V_{FBREG}=V_{IN}-V_{FB} R_{FB1}=R_{FB2}=1.8 Ω, Ta=25 °C to 125 °C
		617	650	683	mV	V_{FBREG}=V_{IN}-V_{FB} R_{FB1}=R_{FB2}=1.8 Ω, Ta=-40 °C to +125 °C
FB Pin Input Current	I_{FB}	7.5	15	30	µA	V_{FB}=V_{IN}
BASE Pin Sink Current Capability	I_{BASE}	10	-	-	mA	V_{FB}=V_{IN}, V_{BASE}=V_{IN}-1.5 V Ta=25 °C
BASE Pin Pull-up Resistor	R_{BASE}	0.5	1.0	1.5	kΩ	V_{CRT}=0 V V_{FB}=V_{IN}, V_{BASE}=V_{IN}-1.0 V
[Over Voltage Mute Function (OVM)]						
Over Voltage Mute Start Voltage	V_{OVMS}	20.0	22.0	24.0	V	ΔV_{FB}=10.0 mV ΔV_{FB}=V_{FB}(@V_{IN}=13 V)- V_{FB}(@V_{IN}=V_{OVMS})
Over Voltage Mute Gain	V_{OVMG}	-	-25	-	mV/V	$\Delta V_{FB}/\Delta V_{IN}$

Electrical Characteristics – continued

(Unless otherwise specified Ta=-40 °C to +125 °C, V_{IN}=13 V, C_{VREG}=1.0 µF, Transistor PNP=2SAR573DFHG)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[CR TIMER]						
CRT Pin Charge Current	I_{CRT}	36	40	44	µA	
CRT Pin Charge Voltage	V_{CRT_CHA}	0.72	0.80	0.88	V	
CRT Pin Discharge Voltage 1	V_{CRT_DIS1}	1.80	2.00	2.20	V	
CRT Pin Discharge Voltage 2	V_{CRT_DIS2}	2.10	2.40	3.00	V	When V_{CRT} > V_{CRT_DIS2}, R_{D1} → R_{D2}
CRT Pin Charge Resistor	R_{CHA}	28.5	30.0	31.5	kΩ	R_{CHA}= (V_{CRT_DIS1}-V_{CRT_CHA})/I_{CRT}
CR Timer Discharge Constant	V_{CRT_CHA}/ V_{CRT_DIS1}	0.38	0.40	0.42	V/V	
DISC Pin ON Resistor 1	R_{DISC1}	20	50	100	Ω	I_{DISC}=10 mA
DISC Pin ON Resistor 2	R_{DISC2}	2.5	5.0	10	kΩ	I_{DISC}=100 µA
CRT Pin Leakage Current	I_{CRT_LEAK}	-	-	10	µA	VCRT=V_{IN}
[LED Open Detection]						
LED Open Detection Voltage	V_{OPD}	1.1	1.2	1.3	V	V_{OPD}=V_{IN}-V_{OP}
OP Pin Input Current	I_{OP}	19	21	23	µA	V_{OP}=V_{IN}-0.5 V
[Disable LED Open Detection Function at Reduced-Voltage]						
OPM Pin Source Current	I_{OPM}	38	40	42	µA	
VIN Pin Disable LED Open Detection Voltage at Reduced-Voltage	V_{IN_OPM}	V_{OPM} x 5.9	V_{OPM} x 6.0	V_{OPM} x 6.1	V	
OPM Pin Input Voltage Range	V_{OPM_R}	1.0	-	2.2	V	
[Disable LED Open Detection Time Setting D Function]						
Input Threshold Voltage	V_{DH}	0.9	1.0	1.1	V	
D Pin Source Current	$I_{DSOURCE}$	100	230	400	µA	
D Pin ON Resistor	R_D	-	-	950	Ω	I_{D_EXT}=100 µA

Electrical Characteristics – continued
(Unless otherwise specified Ta=-40 °C to +125 °C, V_{IN}=13 V, C_{VREG}=1.0 µF, Transistor PNP=2SAR573DFHG)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
[Short Circuit Protection (SCP)]						
Short Circuit Protection Voltage	V_{SCPD}	1.10	1.20	1.30	V	
Short Circuit Protection Release Voltage	V_{SCPR}	1.15	1.25	1.35	V	
Short Circuit Protection Hysteresis Voltage	V_{SCPHYS}	-	50	-	mV	
SCP Pin Source Current	I_{SCP}	0.2	1.0	2.0	mA	
SCP Pin Source Current ON Voltage	V_{SCP2}	1.15	1.30	1.45	V	
SCP Delay Time	t_{SCP}	10	20	45	µs	
[PBUS]						
Input High Voltage	V_{PBUSH}	2.4	-	-	V	
Input Low Voltage	V_{PBUSL}	-	-	0.6	V	
Hysteresis Voltage	$V_{PBUSHYS}$	-	200	-	mV	
PBUS Pin Source Current	I_{PBUS}	75	150	300	µA	V_{EN}=5 V
PBUS Pin Output Low Voltage	V_{PBUS_OL}	-	-	0.6	V	I_{PBUS_EXT}=3 mA
PBUS Pin Output High Voltage	V_{PBUS_OH}	3.5	4.5	5.5	V	I_{PBUS_EXT}=-10 µA
PBUS Pin Leakage Current	I_{PBUS_LEAK}	-	-	10	µA	V_{PBUS}=7 V
[EN]						
Input High Voltage	V_{ENH}	2.4	-	-	V	
Input Low Voltage	V_{ENL}	-	-	0.6	V	
Hysteresis Voltage	V_{ENHYS}	-	60	-	mV	
Pin Input Current	I_{EN}	-	7	15	µA	V_{EN}=5 V
[UVLO VIN]						
UVLO Detection Voltage	V_{UVLOD}	3.88	4.10	4.32	V	V_{IN}: Sweep down
UVLO Release Voltage	V_{UVLOR}	4.25	4.50	4.75	V	V_{IN}: Sweep up, V_{REG} > 3.75 V
UVLO Hysteresis Voltage	V_{HYS}	-	0.4	-	V	

Typical Performance Curves (Reference Data)
(Unless otherwise specified Ta=25 °C, V_{IN}=13 V, C_{VREG}=1.0 µF, Transistor PNP=2SAR573DFHG)

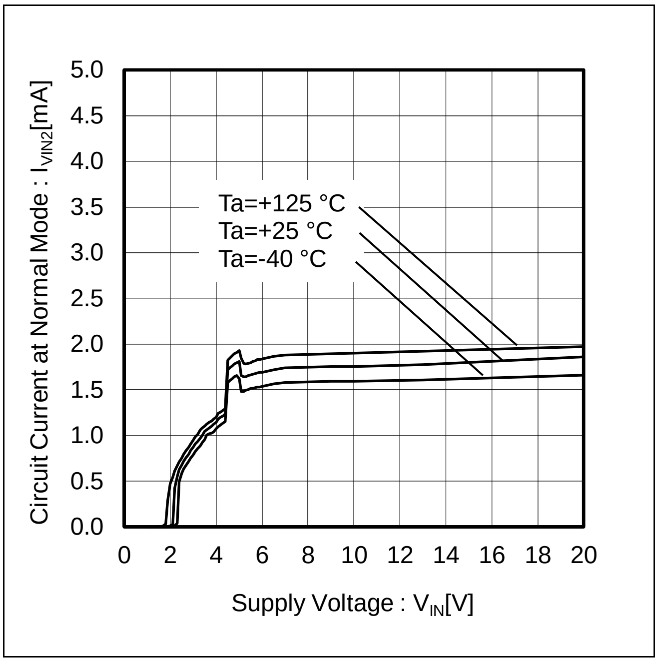


Figure 1. Circuit Current at Normal Mode vs Supply Voltage

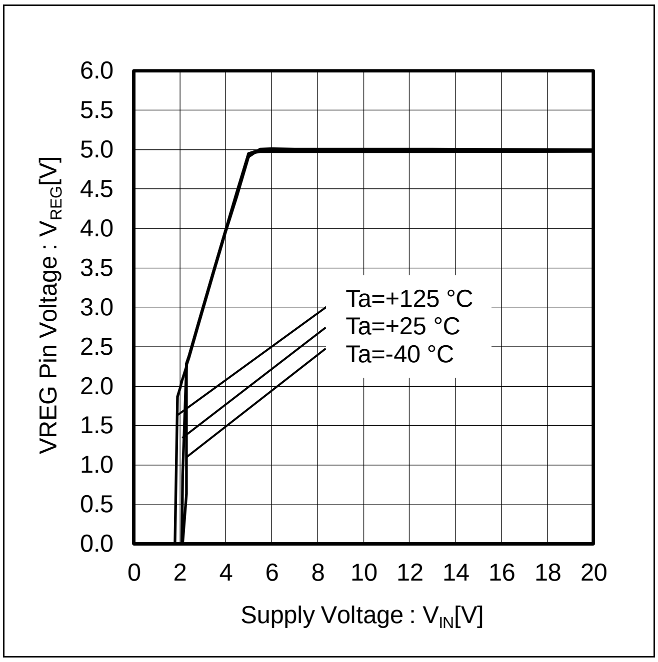


Figure 2. VREG Pin Voltage vs Supply Voltage

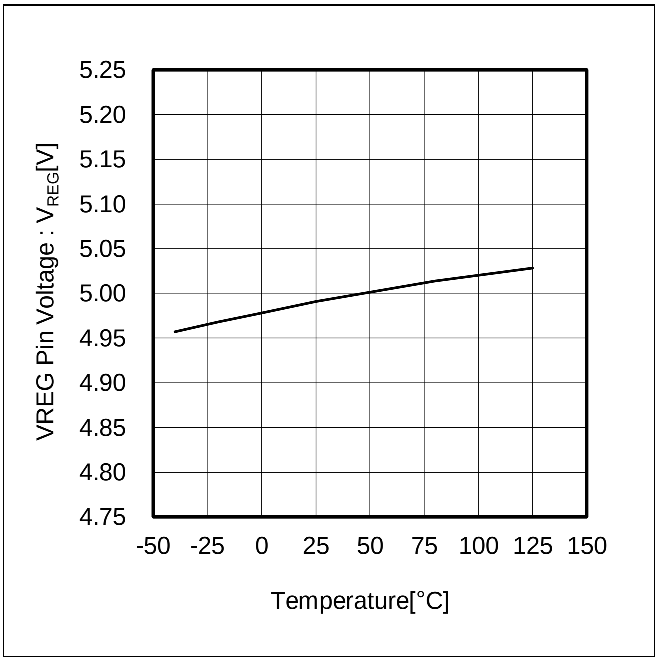


Figure 3. VREG Pin Voltage vs Temperature

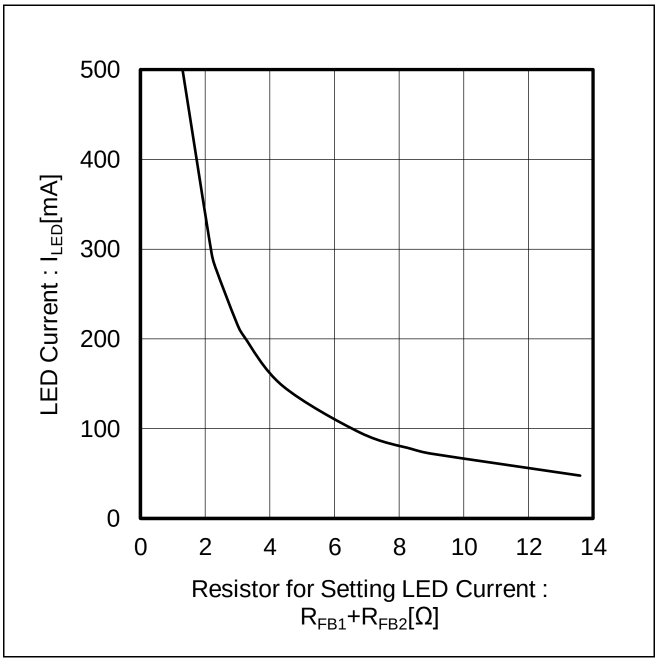


Figure 4. LED Current vs Resistor for Setting LED Current

Typical Performance Curves (Reference Data) **– continued**
(Unless otherwise specified Ta=25 °C, V_{IN}=13 V, C_{VREG}=1.0 µF, Transistor PNP=2SAR573DFHG)

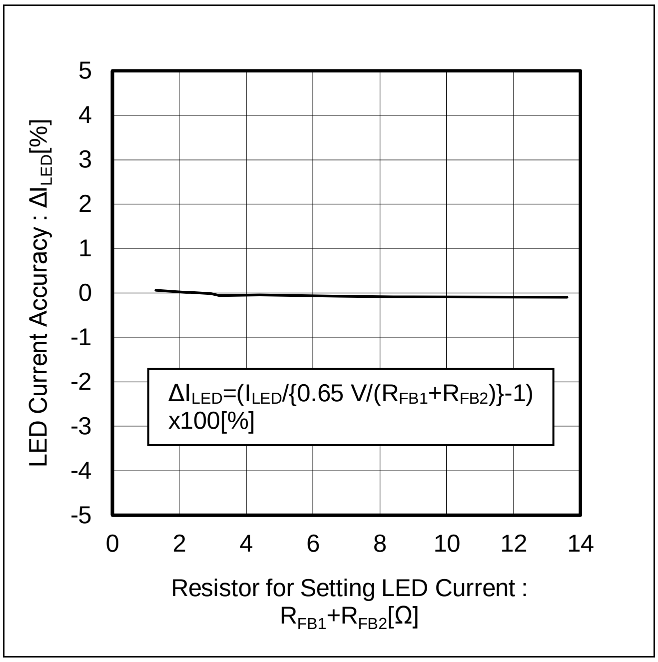


Figure 5. LED Current Accuracy vs Resistor for Setting LED Current

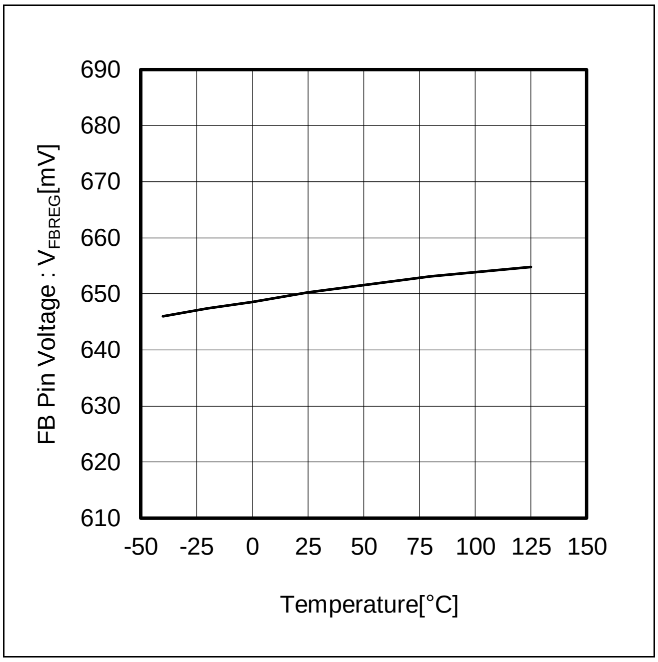


Figure 6. FB Pin Voltage vs Temperature

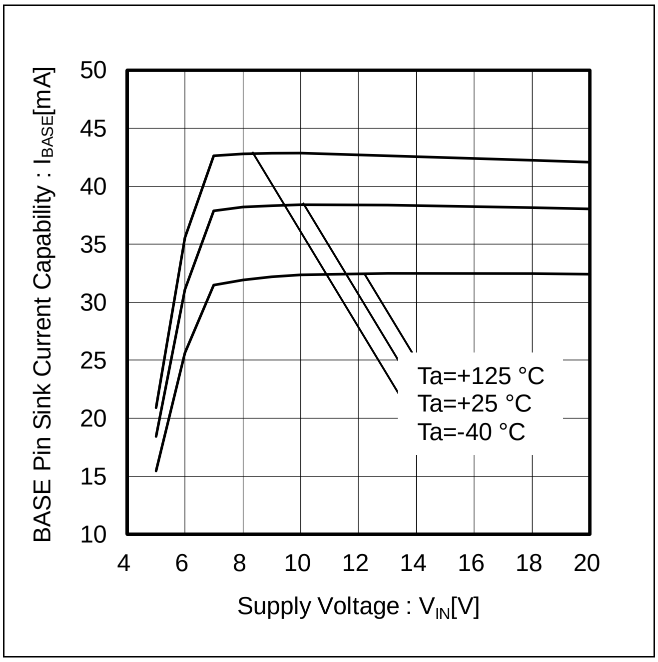


Figure 7. BASE Pin Sink Current Capability vs Supply Voltage

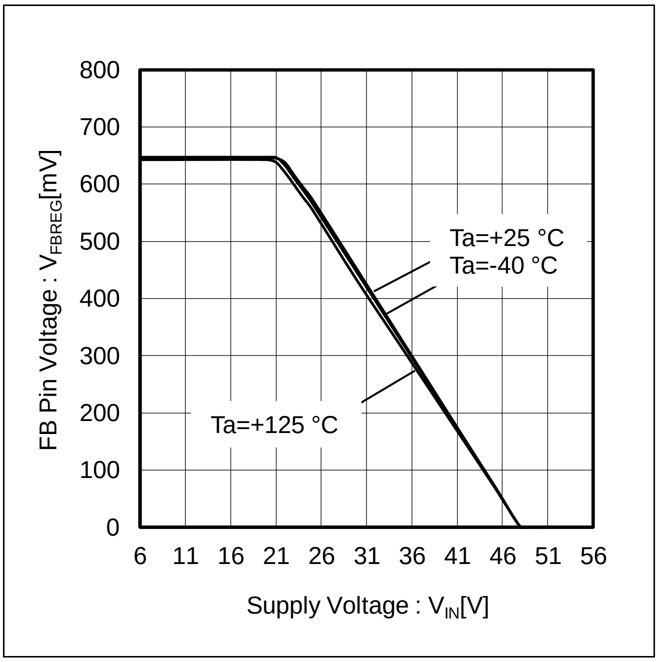


Figure 8. FB Pin Voltage vs Supply Voltage

Typical Performance Curves (Reference Data) **– continued**
(Unless otherwise specified Ta=25 °C, V_{IN}=13 V, C_{VREG}=1.0 µF, Transistor PNP=2SAR573DFHG)

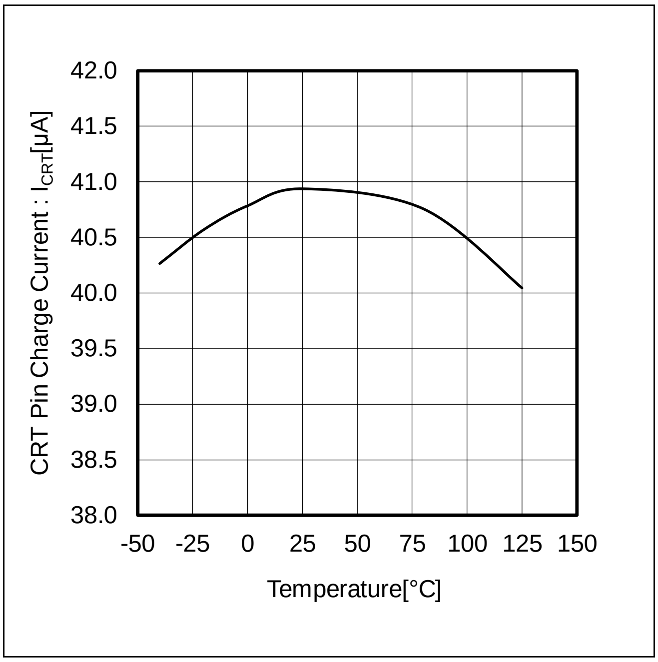


Figure 9. CRT Pin Charge Current vs Temperature

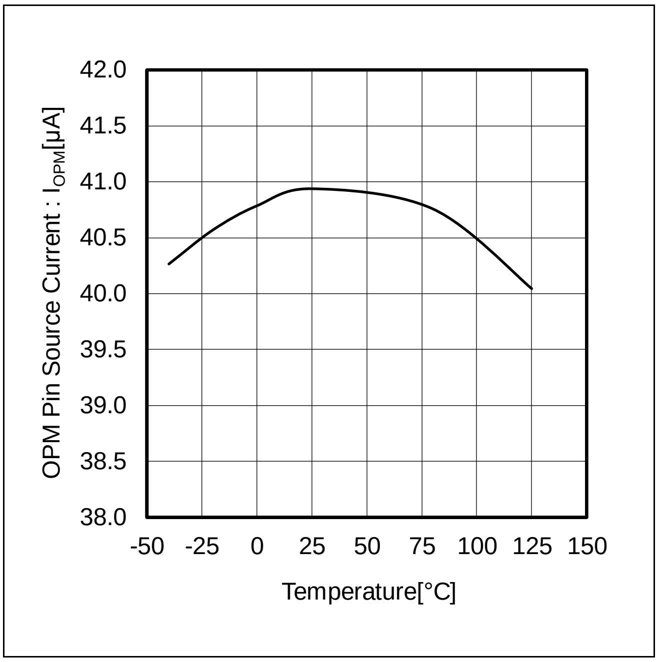


Figure 10. OPM Pin Source Current vs Temperature

Description of Function

(Unless otherwise specified, Ta=25 °C, V_{IN}=13 V, Transistor PNP=2SAR573DFHG, and numbers are "Typical" values.)

1. LED Current Setting
   LED current I_{LED} can be defined by setting resistances R_{FB1} and R_{FB2}.

$$I_{LED} = \frac{V_{FBREG}}{R_{FB1}+R_{FB2}} \quad \text{[A]}$$

where:

V_{FBREG} is the FB pin voltage 650 mV (Typ).

●How to connect LED current setting resistors

LED current setting resistors must always be connected at least two or more in series as below.
<u>If only one current setting resistor is used, then in case of a possible resistor short (pattern short on the board etc.), the external PNP Tr. and LED may be broken due to large current flow.</u>
PNP Tr. rating current, LED rating current, R_{FB1} and R_{FB2} must have the following relations:

$$I_{LED\_MAX} > I_{PNP\_MAX} > \frac{V_{FBREG}}{Min(R_{FB1},R_{FB2})} \quad \text{[A]}$$

where:

I_{LED_MAX}	is the LED rating current.
I_{PNP_MAX}	is the PNP Tr. rating current.
V_{FBREG}	is the FB pin voltage 650 mV (Typ).
$Min(R_{FB1}, R_{FB2})$	is the lowest value of R_{FB1} and R_{FB2}.

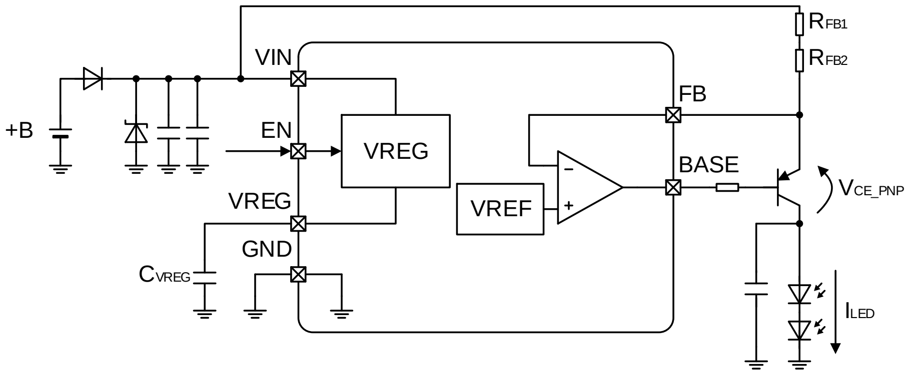


Figure 11. LED Current Setting

●Constant current control dynamic range

Constant current control dynamic range of LED current I_{LED} can be calculated as follows.

$$V_{IN} \geq V_{f\_LED} \times N + V_{CE\_PNP} + V_{FBREG} \quad \text{[V]}$$

where:

V_{IN}	is the VIN pin voltage.
V_{f_LED}	is the LED Vf.
N	is the number of rows of LED.
V_{CE_PNP}	is the external PNP Tr. collector-emitter saturation voltage.
V_{FBREG}	is the FB pin voltage 650 mV (Typ).

2. Reference voltage (VREG)
   Reference voltage VREG 5.0 V (Typ) is generated from VIN input voltage. This voltage is used as power source for the internal circuit, and also used to fix the voltage of pins outside LSI to HIGH side. The VREG pin must be connected with C_{VREG}=1.0 µF to 4.7 µF to ensure capacity for the phase compensation. If C_{VREG} is not connected, the circuit behavior would become extraordinarily unstable, for example with the oscillation of the reference voltage.
   The VREG pin voltage must not be used as power source for other devices than this LSI.
   VREG circuit has a built-in UVLO function. The IC is activated when the VREG pin voltage rises to 4.00 V (Typ) or higher, and shut down when the VREG pin voltage drops to 3.75 V (Typ) or lower.

Description of Function – continued

3. Table of Operations
   The PWM dimming mode switches to DC control depending on the CRT pin voltage.
   The switching conditions are as shown in the table below. When V_{IN} > 22.0 V (Typ), LED current is limited to reduce the heat dissipation of external PNP Tr..
   Depending on the OP pin and the SCP pin voltage status, detect LED open or short circuit then LED current is turned OFF. LED current is also turned OFF when Low signal is input to the PBUS pin.
   In addition, UVLO and TSD further increases system reliability.
   For each functions, please refer to Description of Function.

Operation Mode	CRT Pin	Detecting Condition		LED Current (I_{LED})	PBUS Pin
		[Detect]	[Release]		
Stand-by Mode(Note 1)	-	V_{EN} ≤ 0.6 V	V_{EN} ≥ 2.4 V	OFF(Note 3)	Hi-Z
DC	V_{CRT} ≥ 2.0 V (Typ)	-	-	50 mA to 400 mA	High 4.5 V (Typ)
PWM Dimming	See Features Description 4	-	-	See Features Description 4	High 4.5 V (Typ)
Over Voltage Mute	-	V_{IN} > 22.0 V (Typ)	V_{IN} ≤ 22.0 V (Typ)	See Features Description 10	High 4.5 V (Typ)
LED Open Detection(Note 2)	-	V_{OP} ≥ V_{IN} –1.2 V (Typ)	V_{OP} < V_{IN} – 1.2 V (Typ)	OFF(Note 3)	Low
Short Circuit Protection (SCP)	-	V_{SCP} ≤ 1.20 V (Typ)	V_{SCP} ≥ 1.25 V (Typ)	OFF(Note 3)	Low
PBUS Control OFF	-	V_{PBUS} ≤ 0.6 V	V_{PBUS} ≥ 2.4 V	OFF(Note 3)	Input V_{PBUS} ≤ 0.6 V
UVLO	-	V_{IN} ≤ 4.10 V (Typ) or V_{REG} ≤ 3.75 V (Typ)	V_{IN} ≥ 4.50 V (Typ) or V_{REG} ≥ 4.00 V (Typ)	OFF(Note 3)	High
TSD	-	Tj ≥ 175 °C (Typ)	Tj ≤ 150 °C(Typ)	OFF(Note 3)	Hi-Z

(Note 1) Circuit current 0 µA (Typ)
(Note 2) In regard to the sequence of LED current OFF, see Features Description 5.
(Note 3) The BASE pin sink current: OFF, and LED current(I_{LED}): OFF.

Description of Function – continued

4. PWM Dimming Operation
PWM Dimming is performed with the following circuit.
The dimming cycle and ON Duty Width, can be set by values of the external components (C_{CRT}, R_{CRT}).
Connect the CRT pin to VIN and the DISC pin to GND or open if it is not used.

The CR timer function is activated if DC SW is OPEN. To perform PWM dimming of LED current, a triangular waveform is generated at the CRT pin. The **LED current (I_{LED}) is turned OFF** while CRT voltage is ramp up, and **LED current(I_{LED}) is turned ON** while CRT voltage is ramp down.

When $V_{CRT} \geq V_{CRT\_DIS1}$(2.0 V(Typ)), dimming mode turns to DC Control. When $V_{CRT} > V_{CRT\_DIS2}$(2.4 V(Typ)), the DISC pin ON resister changes from R_{DISC1}(50 Ω(Typ)) to R_{DISC2}(5 kΩ(Typ)), and the power consumption of the IC is reduced by reducing the inflow current of the DISC pin.

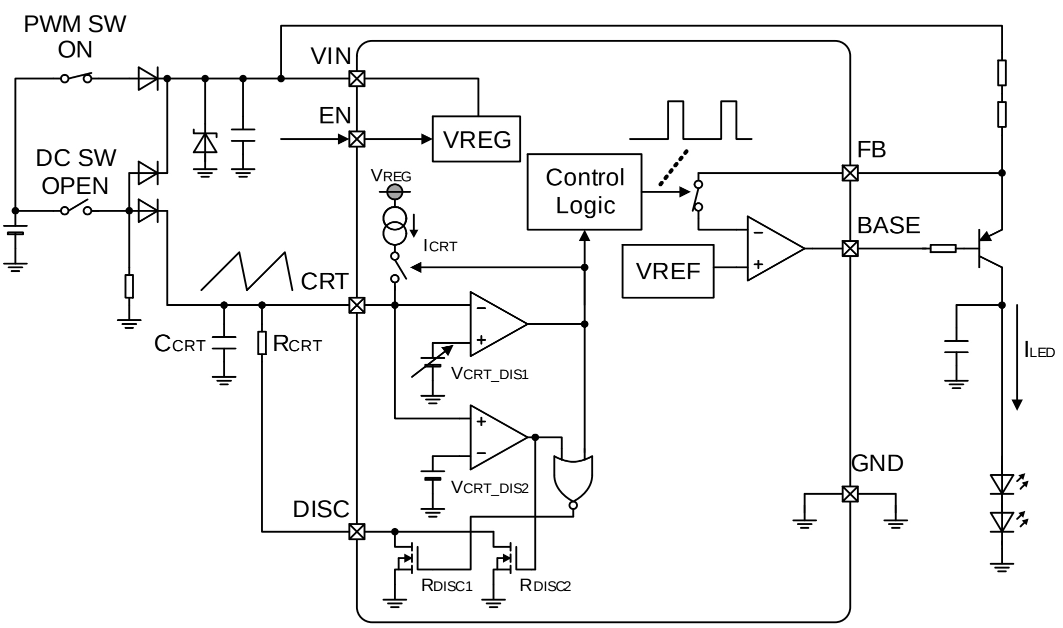


Figure 12. PWM Dimming Operation

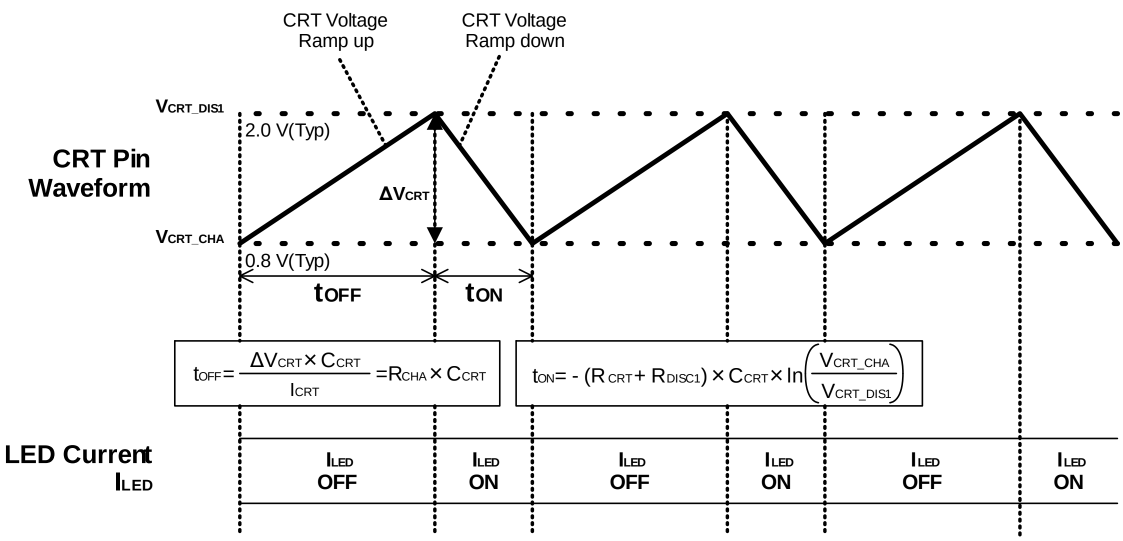


Figure 13. PWM Dimming Operation

4. PWM Dimming Operation – continued

(1) CRT ramp up Time t_{OFF} and CRT ramp down Time t_{ON}
CRT ramp up Time t_{OFF} and CRT ramp down Time t_{ON} can be defined from the following equations.
Make sure that t_{ON} is set PWM Minimum Pulse Width t_{MIN} 10 µs or more.

$$t_{OFF}=\frac{\Delta V_{CRT}\times C_{CRT}}{I_{CRT}}=R_{CHA}\times C_{CRT}\quad [s]$$

$$t_{ON}=-(R_{CRT}+R_{DISC1})\times C_{CRT}\times In\left(\frac{V_{CRT\_CHA}}{V_{CRT\_DIS1}}\right)\quad [s]$$

where:

I_{CRT}	is the CRT pin charge current, 40 µA (Typ).
R_{CHA}	is the CRT pin charge resistor, 30 kΩ (Typ).
R_{DISC1}	is the DISC pin ON resistor1, 50 Ω (Typ).
V_{CRT_CHA}	is the CRT pin charge voltage, 0.8 V (Typ).
V_{CRT_DIS1}	is the CRT pin discharge voltage1, 2.0 V (Typ).

(2) PWM Dimming Frequency f_{PWM}
PWM frequency is defined by t_{ON} and t_{OFF}.

$$f_{PWM}=\frac{1}{t_{ON}+t_{OFF}}\quad [Hz]$$

(3) ON Duty(D_{ON})
PWM ON duty is defined by t_{ON} and t_{OFF}.

$$D_{ON}=\frac{t_{ON}}{t_{ON}+t_{OFF}}\quad [\%]$$

(Example) In case of R_{CRT}=3.6 kΩ, C_{CRT}=0.1 µF (Typ)

$$t_{OFF}=R_{CHA}\times C_{CRT}=30\times 0.1=3.0\quad [ms]$$

$$t_{ON}=-(R_{CRT}+R_{DISC1})\times C_{CRT}\times In(V_{CRT\_CHA}/V_{CRT\_DIS1})$$
$$=-(3.6+50)\times 0.1\times In(0.8/2.0)=0.334\quad [ms]$$

$$f_{PWM}=1/(t_{ON}+t_{OFF})=1/(3.0+0.334)=300\quad [Hz]$$

$$D_{ON}=t_{ON}/(t_{ON}+t_{OFF})=0.334/(3.0+0.334)=10.0\quad [\%]$$

[PWM Dimming Operation Using External Signal]
In case external PWM input to the CRT pin, make sure that input pulse high voltage ≥ **2.2 V** and pulse low voltage ≤ **0.6 V**. Also please open the DISC pin or connect to GND.

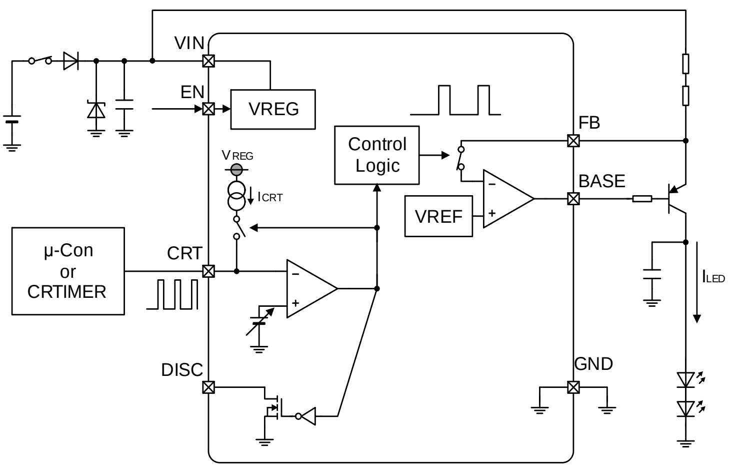


Figure 14. PWM Dimming Operation Using External Signal

4. PWM Dimming Operation – continued

●About deviation of CRT ramp up/down time with a reverse connection protection diode

If this LSI is used to drive LED like below schematic, there is a possibility of occur CRT ramp up/down time deviation due to characteristics of reverse current Ir diode (D2, D3) .
Consider to choose a diode (D2, D3) which is recommended by Rohm or Ir value 1 μA (Max) or less.
Since reverse current flows even with the recommended diodes, connect a resistor of R_{DCIN} of 10 kΩ or less between Point A and GND so that the voltage at point A does not rise.

Mechanism of deviation of CRT ramp up/down time from set values.

① During the PWM dimming operation mode, Point A on Figure 15 is Hi-Z.
↓
② Reverse current Ir of D2 and D3 goes to Point A.
(Power supply voltage is being input into the cathode of D2, so mainly reverse current of D2 goes into C1.)
→**Reverse current Ir of D3 is added to the CRT pin charge current and discharge current, so CRT ramp up/down time deviates from the settings.**
↓
③ C1 gets charged, voltage at Point A rises.
↓
④ Point A voltage ≥ the CRT pin voltage of each IC.
↓
⑤ Vf occurs in the diodes D3.
↓
⑥ D3 circulate forward current If
→**Forward current If of D3 is added to the CRT pin charge current and discharge current, so CRT ramp up/down time deviates from the settings.**
↓
⑦ Repetition of ② to ⑥.

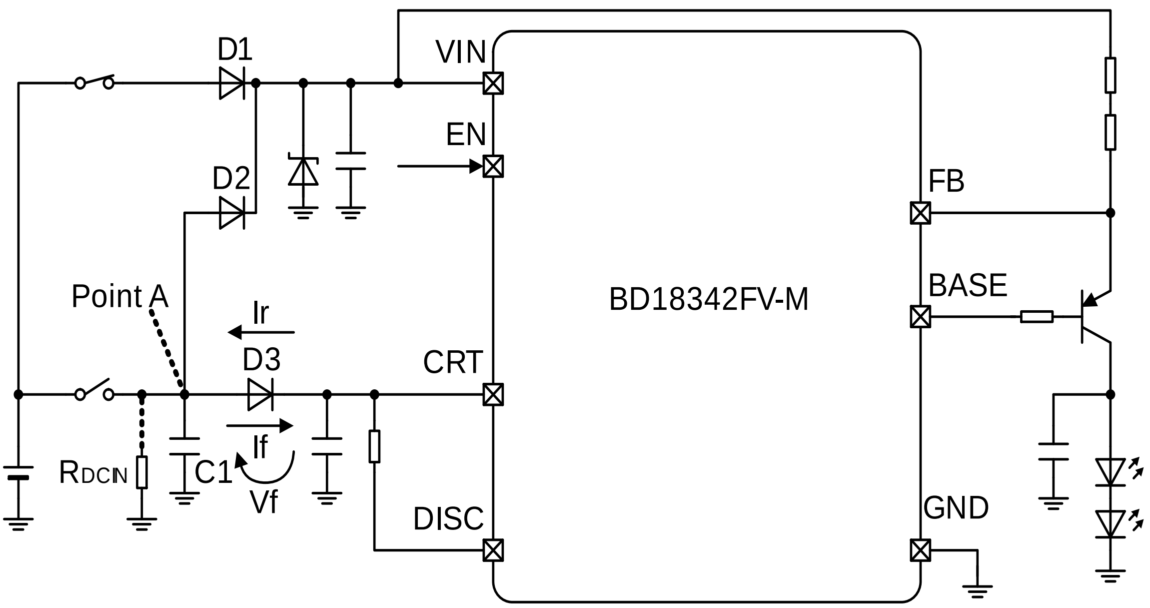


Figure 15. How Reverse Protection Diode Affects the CRT Pin Ramp Up/Down Time

Description of Function – continued

5. LED Open Detection Function

In case any one of the LEDs is in the open state, the IC can detect LED open condition when the OP pin voltage (V_{OP}) meets the following condition: V_{OP} ≥ V_{IN}-1.2 V (Typ). As soon as V_{OP} ≥ V_{IN}-1.2 V (Typ) condition is achieved, the D pin source current (230 μA (Typ)) turns on and starts charging the disable LED open detection time setting capacitor (C_D). Once the D pin voltage (V_{DH}) becomes 1.0 V (Typ) or more and 1 μs (Typ) elapses, the BASE pin sink current (I_{BASE}) is latched OFF and the PBUS pin voltage (V_{PBUS}) is switched to Low.

[Base Current Limit Resistance (R_{LIM})]

The OP pin voltage V_{OP} at LED open is defined by the following formula:
(Note that the external PNP Tr. goes into the saturation mode when the collector is open, it becomes the following formula.)

$$V_{OP} = V_{IN} - \{(R_{FB1} + R_{FB2}) \times I_{BASE_{MAX}} + V_{CE_{PNP}}\} \quad \text{[V]}$$

$$I_{BASE\_MAX} = 6.0V/R_{LIM} \quad \text{[A]}$$

$$(I_{BASE\_MAX} < 80\ mA)$$

where:

R_{FB1}, R_{FB2} is the LED current setting resistance.
I_{BASE_MAX} is the maximum BASE pin sink current.
R_{LIM} is the resistor for limiting BASE pin current.
V_{CE_PNP} is the external PNP Tr. Collector-emitter voltage (Note: I_{CE}=I_{OP} (23 μA (Max))).

Please determine the BASE current limit resistance R_{LIM} to ensure that the OP pin voltage when the LED is open should meet the following condition: V_{OP} > V_{IN}-1.2 V (Typ).
Also note that the BASE current limit resistance must meet the following condition in order to obtain the BASE current to be needed during normal LED operation.

$$4.0/R_{LIM} > I_{LED}/hfe_{\_MIN} \quad \text{[A]}$$

where:

$hfe_{\_MIN}$ is the minimum external PNP Tr. hfe.

For the D pin, it is possible to set the disable time t_D from when the OP pin voltage meets the condition "V_{OP} > V_{IN}-1.2 V (Typ)" until the BASE pin sink current (I_{BASE}) is latched off, according to the following formula. **Note that the disable time must be shorter than or equal to the ON pulse width of the PWM dimming t_{ON}.**

$$t_{ON} > t_D = \frac{C_D \times V_{DH}}{I_{DSOURCE}} \quad \text{[s]}$$

where:

t_{ON} is the ON pulse width of the PWM dimming(CRT ramp down time).
C_D is the disable LED open detection time setting capacitor.
V_{DH} is the D pin input threshold voltage, 1.0 V (Typ).
$I_{DSOURCE}$ is the D pin source current, 230 μA (Typ).

To reset the latched off LED current, EN must be turned-on again (The time when the EN Pin is "L" since the power is turned on again: 50 μs or more) or the condition "UVLO (V_{IN} ≤ 4.10 V or V_{REG} ≤ 3.75 V)" must be fulfilled.

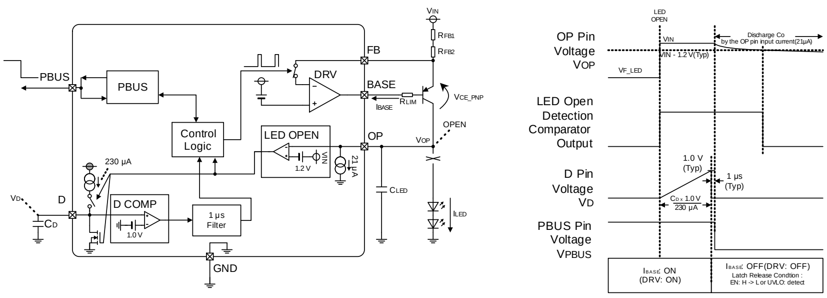


Figure 16. LED Open Detection Timing Chart

Description of Function – continued

6. Disable LED Open Detection Function at Reduced-Voltage
The disable LED open detection function serves to prevent false detection of LED open at the reduced-voltage during the ramp-up/ramp-down of the VIN pin voltage. Even though LED is in the open state, LED open will not be detected until the VIN pin voltage becomes more than Disable Open Detection Voltage at Reduced-Voltage (V_{IN_OPM}). Once V_{IN_OPM} is surpassed, the LED current will be latched OFF (The BASE pin sink current (I_{BASE}) is latched OFF) and the PBUS voltage will be switched to Low following the sequence explained in Description of Function 5.
V_{IN_OPM} must be defined by the following formula. (The OPM pin voltage must be set between 1.0 V and 2.2 V.)

$$V_{IN\_OPM} \geq V_{IN\_OPERR} \quad [V]$$

where:
V_{IN_OPM} is the VIN pin disable open detection voltage at reduced-voltage.
V_{IN_OPERR} is the VIN pin open erroneous detection voltage at reduced-voltage.

$$V_{IN\_OPM} = V_{OPM} \times 6.0\ (Typ) \quad [V]$$

$$V_{OPM} = I_{OPM} \times R_{OPM} \quad [V]$$

$$V_{IN\_OPERR} = V_{f\_LED} \times N + V_{OPD} \quad [V]$$

where:
V_{OPM} is the OPM pin voltage.
I_{OPM} is the pin source current, 40 μA (Typ)
R_{OPM} is the OPM pin connection resistance.
V_{f_LED} is the LED Vf.
N is the number of rows of LED.
V_{OPD} is the LED open-circuit detection voltage, 1.2 V (Typ)

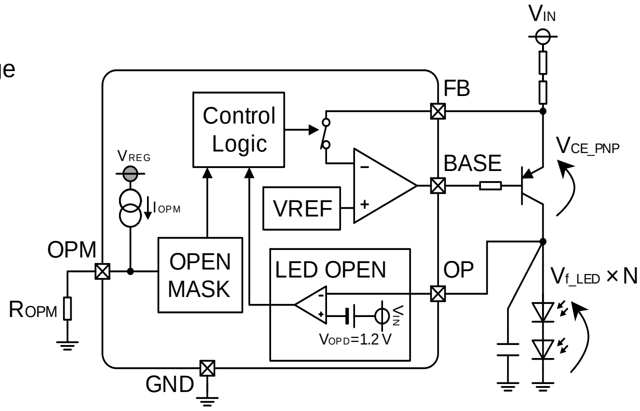


Figure 17. Disable LED Open Detection Function at Reduced-Voltage

●When connecting resistor for heat dispersion, or connecting resistor or diodes between the OP pin and LED anode

The formula to calculate V_{IN_OPERR} will be different from the one above when the current flowing the LED is large and it is necessary to connect a resistor for heat dispersion in series with the LED to reduce the heat generation from the external PNP Tr., when multiple rows of the LEDs are driven, or when connecting a resistor to adjust the threshold voltage for detecting the LED open-circuit. Please read the Application Note of BD1834xFV-M series for details.

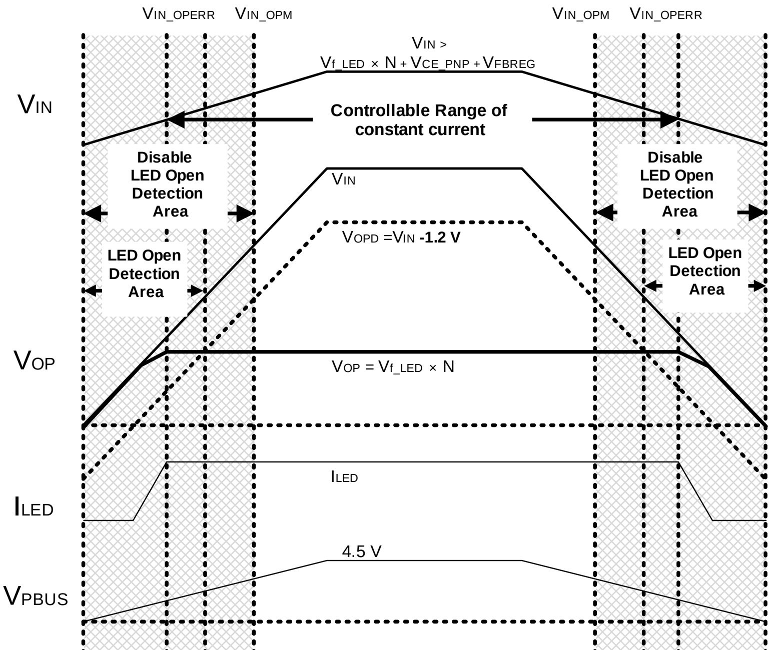


Figure 18. VIN Pin Disable LED Open Detection Voltage at Reduced-Voltage and LED Open Erroneous Detection Voltage at Reduced-Voltage

Description of Function – continued

7. Short Circuit Protection (SCP)
   Short Circuit Protection function will be activated by decreasing the SCP pin voltage when the collector of the external PNP Tr. is short to GND. After a lapse of the short circuit protection delay time(t_{SCP})(20 µs(Typ)) following the drop of the SCP pin voltage(V_{SCP}) is 1.2 V(Typ) or less, the external PNP Tr. is turned OFF to prevent its thermal destruction, and it can be notify the abnormally to the outside by changing the PBUS pin output to low.
   In order to avoid malfunction since the power is turned on, the Short Circuit Protection function will not be activated until V_{CRT} > 2.0 V(Typ) after UVLO is reset.
   If it is in the short circuit state (V_{SCP} < 1.2 V(Typ)) since the power is turned on, the Short Circuit Protection function will be activated when V_{CRT} > 2.0 V(Typ) condition is reached and 60 µs(Typ) passes, after UVLO is reset.

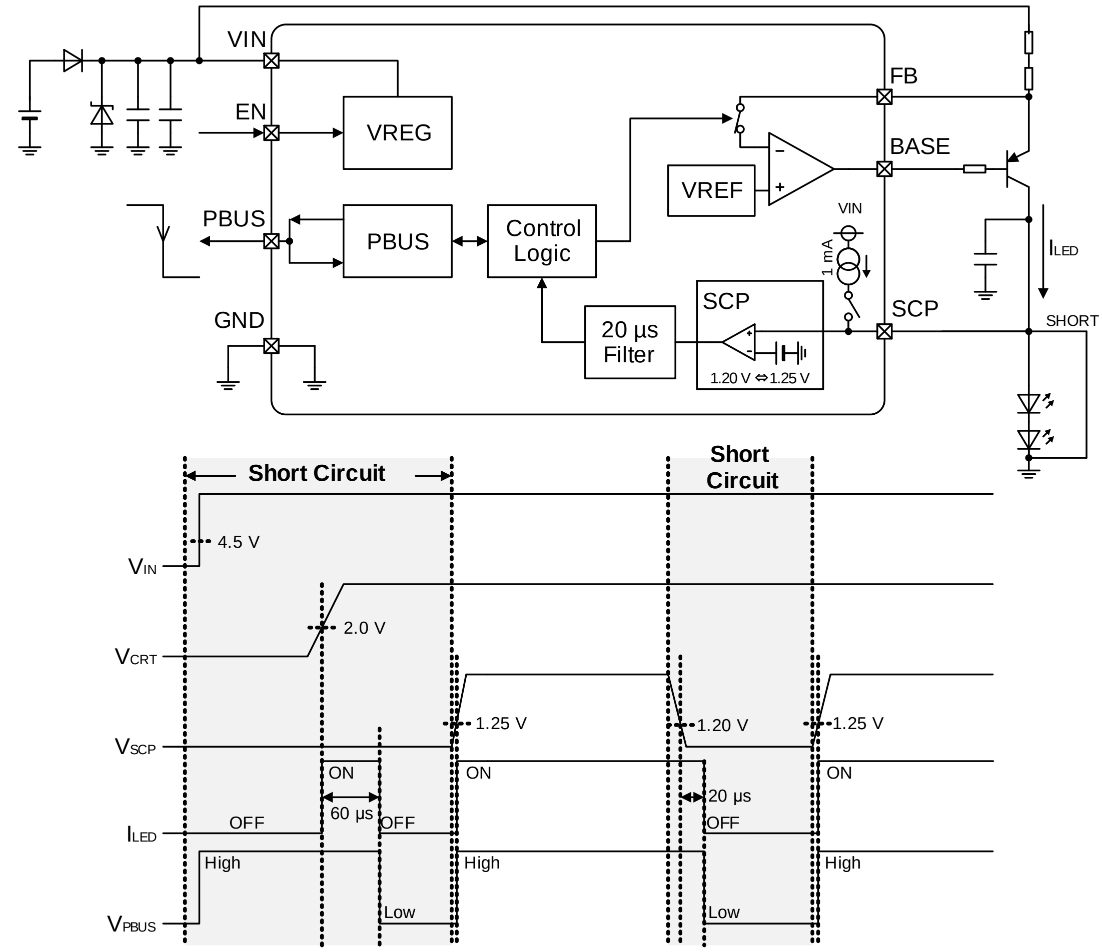


Figure 19. Short Circuit Protection (SCP)

●SCP Pin Source Current
The SCP pin sources the current (1 mA(Typ)) once its voltage (V_{SCP}) drops under 1.3 V in order to prevent the malfunction of the short circuit protection.

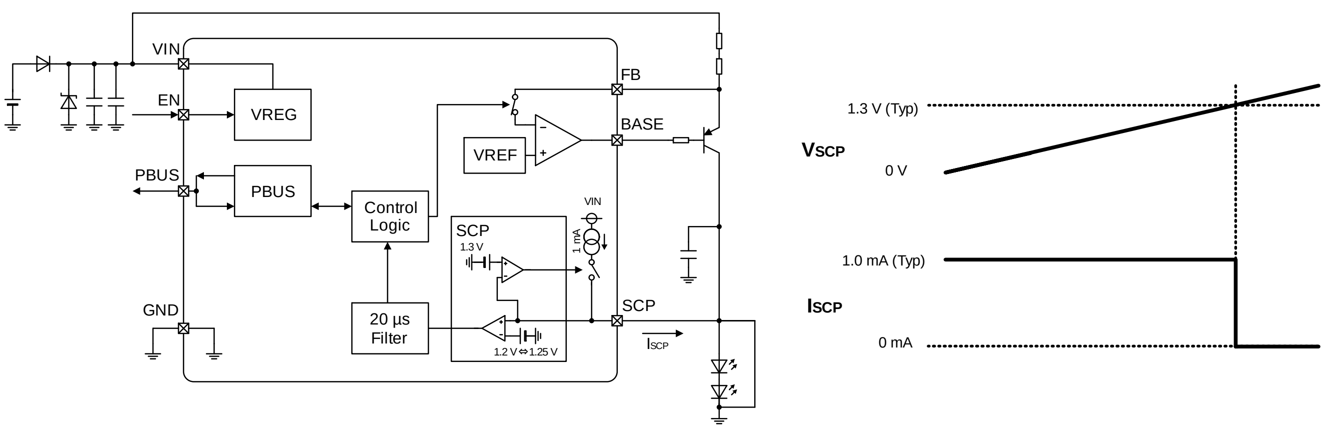


Figure 20. SCP Pin Source Current

Description of Function – continued

8. About the Capacitor of Connecting LED Anode
   There is a zone which the output (LED anode) will become high impedance (Hi-Z) at PWM dimming Mode. During this time noise(Note 1) can couple on to this pin and cause false detection of SHORT condition.
   To prevent this, **it is necessary to connect a Capacitor C_{LED} between LED anode and GND pin nearby pin.**

   Make sure that the capacitor of connecting LED anode is the following equation:

$$0.1 \leq C_{LED} \leq 0.68 \quad [\mu F]$$

   In case C_{LED} is set the range from 0.1 μF to 0.68 μF, the I_{LED} current becomes dull, so please evaluate I_{LED} waveform in PWM mode operation.

   About the example of evaluation, please see evaluation example on page 21.

   In case a capacitor exceeding the recommended range is connected to LED anode, there is a possibility that delay time of start-up will reach about several ten ms, so special attention is needed.

   (Note 1) Conducted noise, Radiated noise, Crosstalk of connecter and PCB pattern etc…

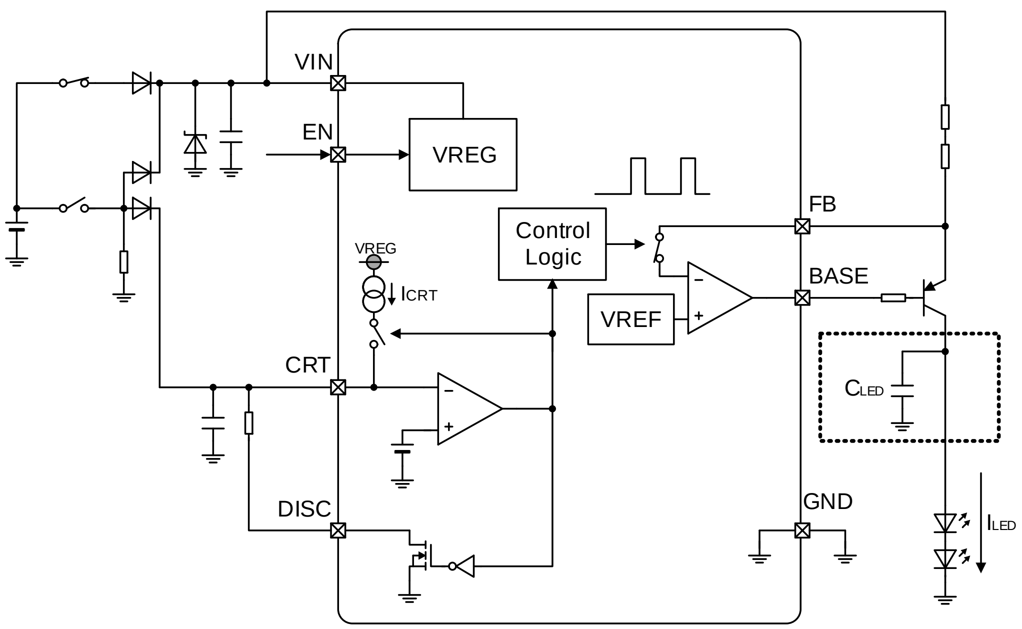
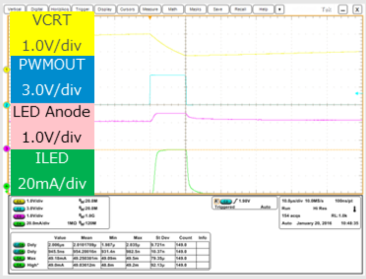
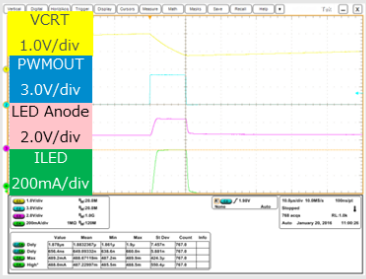
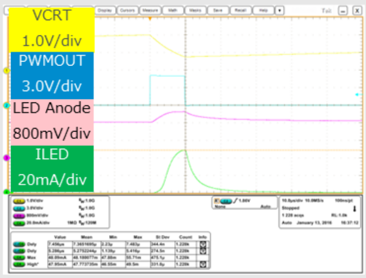
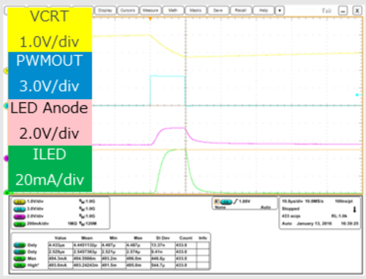


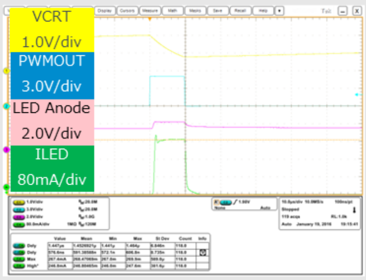
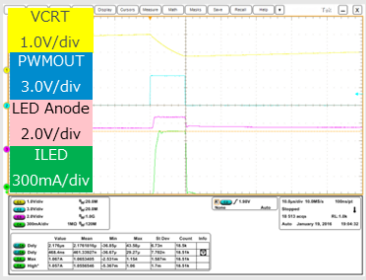
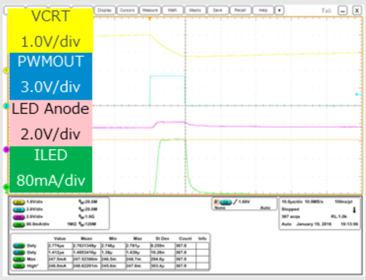
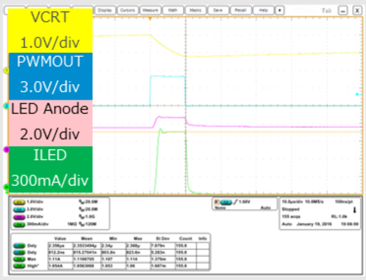
Figure 21. About the Capacitor of Connecting LED Anode

Description of Function – continued

Evaluation example (I_{LED} pulse width at PWM Dimming operation)

Condition: +B=13 V
Ta=25 °C
LED=1 Strings
C_{CRT}=0.01 µF
R_{DISC}=1.0 kΩ
PWM Dimming Mode

PNP Tr. : 1parallel	I_{LED}=50 mA			I_{LED}=500 mA		
C_{LED}=0.1 µF		Rise Time	2.0µs		Rise Time	1.9µs
		Fall Time	0.9µs		Fall Time	0.7µs
		OverShoot	≒0mA		OverShoot	1mA (0.2%)
C_{LED}=0.47 µF		Rise Time	7.4µs		Rise Time	4.4µs
		Fall Time	5.3µs		Fall Time	2.5µs
		OverShoot	≒0mA		OverShoot	≒0mA

PNP Tr. : 5parallel	I_{LED}=50 mA			I_{LED}=200 mA		
C_{LED}=0.1 µF		Rise Time	1.5µs		Rise Time	2.2µs
		Fall Time	0.6µs		Fall Time	0.5µs
		OverShoot	22mA (4.4%)		OverShoot	10mA (1%)
C_{LED}=0.47 µF		Rise Time	2.8µs		Rise Time	2.4µs
		Fall Time	1.4µs		Fall Time	0.8µs
		OverShoot	≒0mA		OverShoot	56mA (5.6%)

Description of Function – continued

9. PBUS Function
   The PBUS pin is the pin to input and output an error signal.
   When abnormality such as LED open or output ground fault occurs, it can notify the abnormality to the outside by changing the PBUS pin output from high to low. In addition, by externally controlling the PBUS pin from high to low, the LED current is turned off. When using multiple LSIs to drive multiple LEDs, it is possible to turn off all LED lines at once by connecting the PBUS pins of each CH as shown in the figure below, even if LED open or output ground fault occurs.

   Caution of using the PBUS pin
   Do not connect to the PBUS pins other than BD1834xFV-M series due to the difference of ratings, internal threshold voltages, and so on.

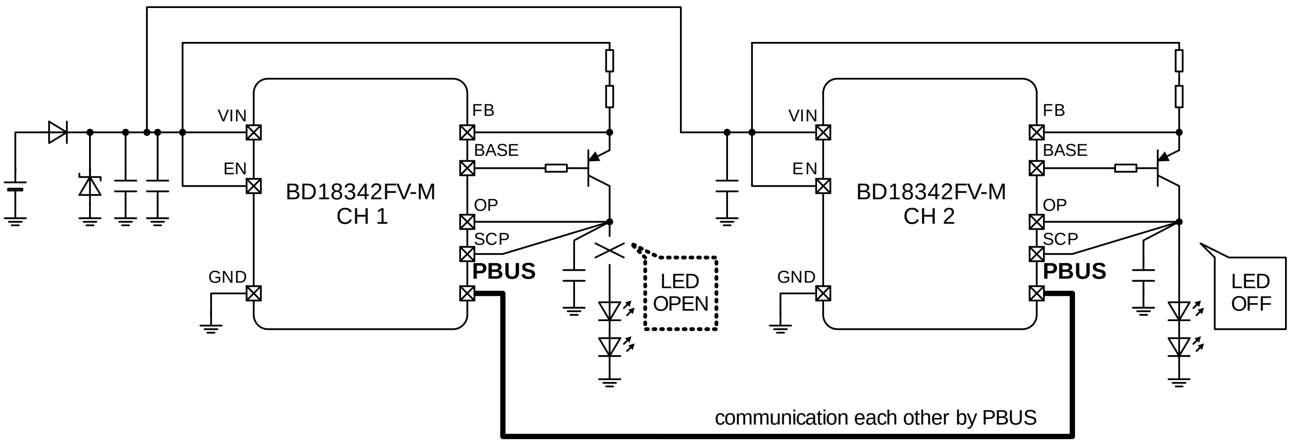


Figure 22. PBUS Function

▼Example of Protective Operation due to LED Open Circuit

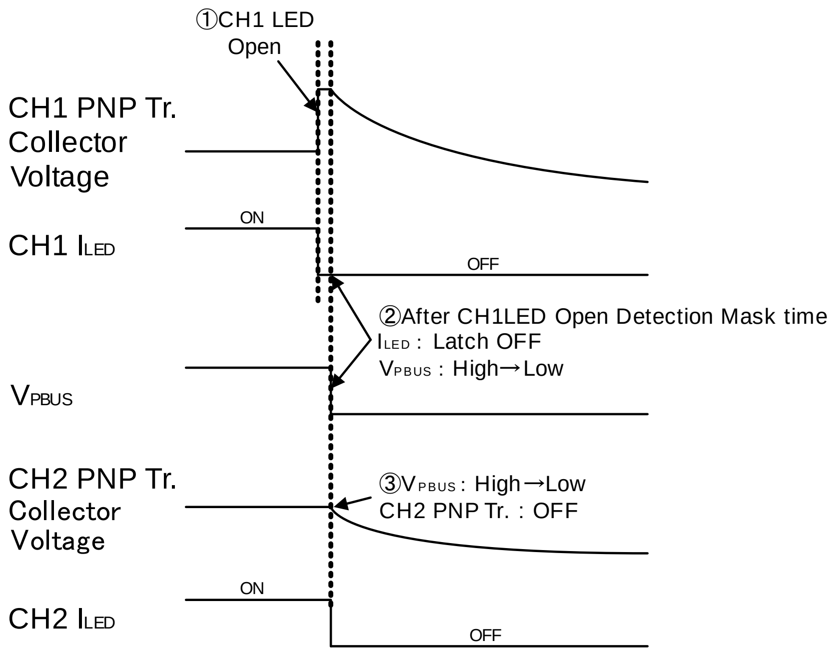


Figure 23. Example of Protective Operation

If LED OPEN occurs, the PBUS pin of CH1 is switched from High to Low output. As the PBUS pin becomes Low, LED drivers of other CH detect the condition and turns OFF their own LEDs. The collector voltage of PNP transistor clamps to 1.3 V (Typ) during the OFF period, in order to prohibit ground fault detection.

Description of Function – continued

10. Over Voltage Mute Function (OVM)
    Once the VIN pin voltage (V_{IN}) goes above 22.0 V (Typ), the over voltage mute function is activated to decrease the LED current (I_{LED}) in order to suppress heat generation from the external PNP Tr.
    The FB pin voltage V_{FBREG} which controls the LED current (I_{LED}) will decay at -25 mV/V (Typ).

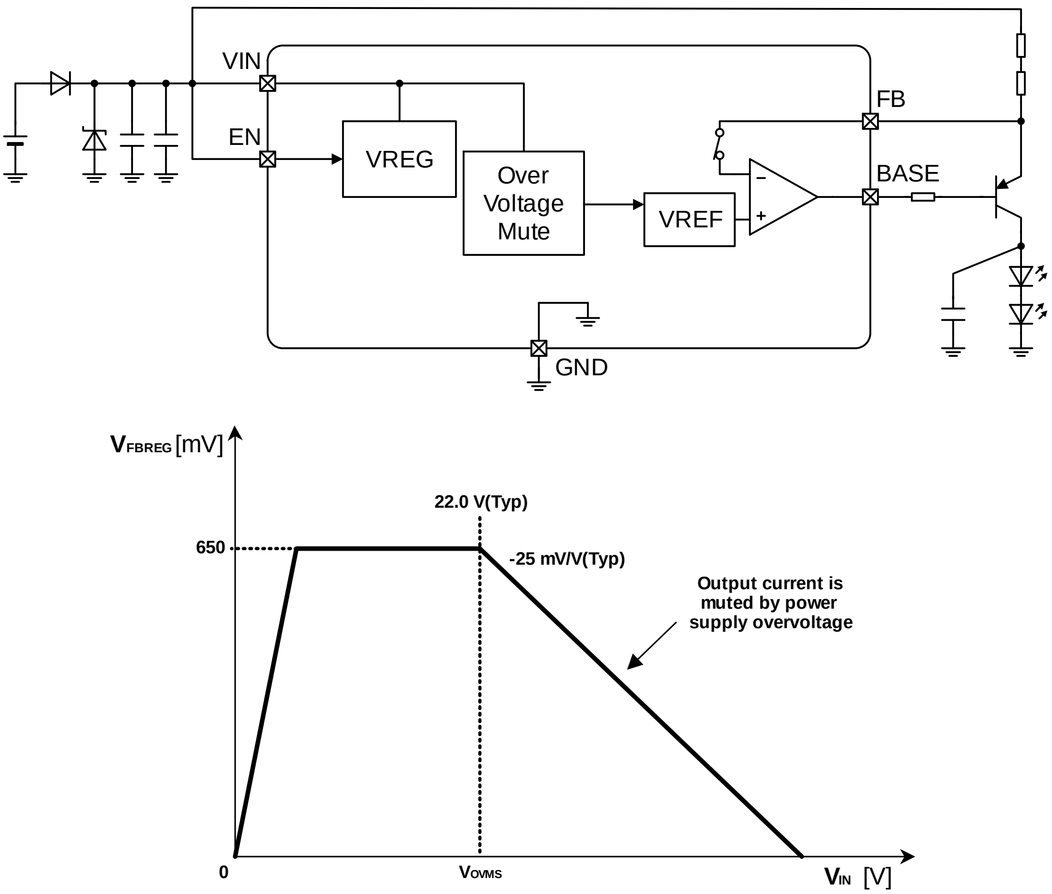


Figure 24. Overvoltage Mute Function (OVM)

11. Under Voltage Lockout (UVLO)
    UVLO is a protection circuit to prevent malfunction of the IC when the power is turned on or when the power is suddenly shut off.
    This IC has two UVLO circuits; UVLO VIN for V_{IN} and UVLO VREG for V_{REG}.
    As soon as UVLO status is detected, the BASE pin sink current will be turned off and switch OFF the LED current (I_{LED}).
    The following shows the threshold conditions of both UVLO circuits.

Operating Mode	Detection Conditions		LED Current (I_{LED})	PBUS Pin
	[Detect]	[Release]		
UVLO VIN	V_{IN} ≤ 4.10 V (Typ)	V_{IN} ≥ 4.50 V (Typ)	OFF *(Note 1)*	High 4.5 V (Typ)
UVLO VREG	V_{REG} ≤ 3.75 V (Typ)	V_{REG} ≥ 4.00 V (Typ)	OFF *(Note 1)*	High 4.5 V (Typ)

(Note 1) The BASE pin sink current is turned OFF to switch OFF the LED current (I_{LED}).

Timing Chart

(Unless otherwise specified Ta=25 °C, VIN=13 V, Transistor PNP=2SAR573DFHG, LED 2 strings, and values are Typical.)

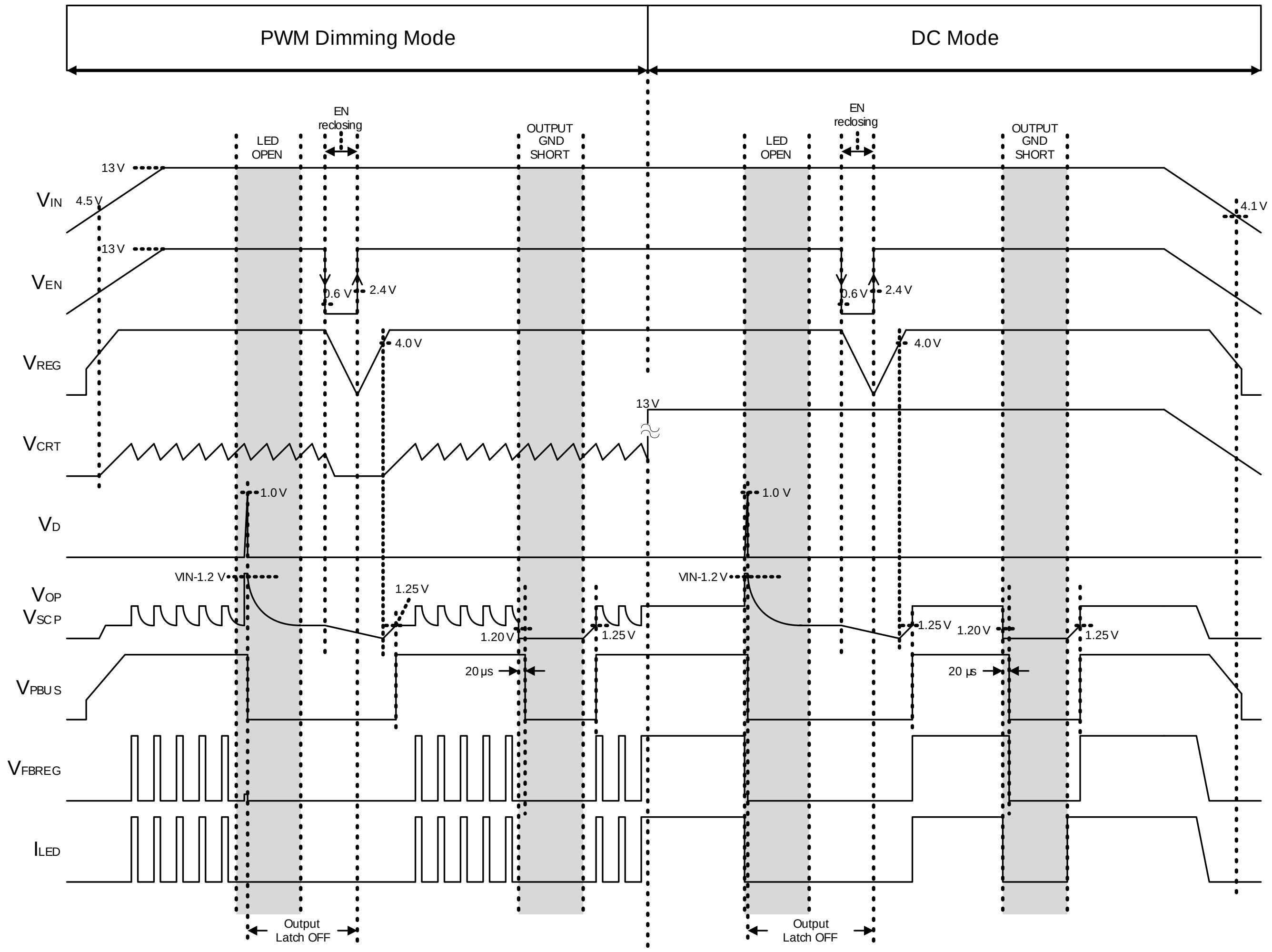


Figure 25. Timing Chart

Application Examples

(1) I_{LED}=120 mA

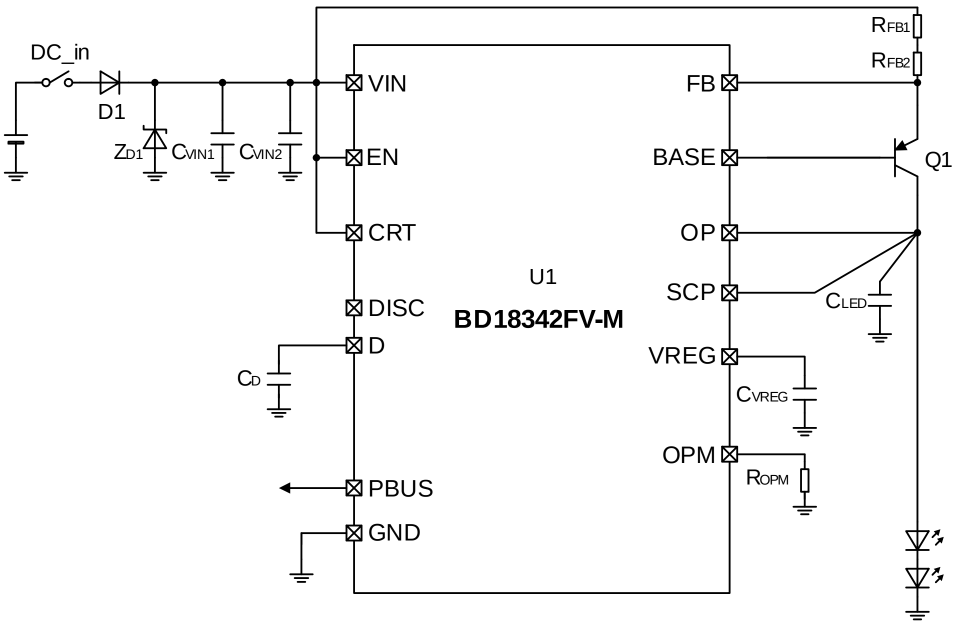


Figure 26. Application Example 1
(I_{LED} 120 mA, LED white 2 strings)

Recommended Parts List 1 (I_{LED} 120 mA, LED white 2 strings)

Parts	No	Parts Name	Value	Unit	Product Maker
IC	U1	BD18342FV-M	-	-	ROHM
Diode	D1	RFN2LAM6STF	-	-	ROHM
	Z_{D1}	TND12H-220KB00AAA0	-	-	NIPPON CHEMICON
Transistor PNP	Q1	2SAR573DFHG	-	-	ROHM
Resistor	R_{FB1}	LTR10EVHFL2R70	2.7	Ω	ROHM
	R_{FB2}	LTR10EVHFL2R70	2.7	Ω	ROHM
	R_{OPM}	MCR03EZPFX3902	39	kΩ	ROHM
Capacitor	C_{VIN1}	GCM32ER71H475KA40	4.7	µF	murata
	C_{VIN2}	GCM155R71H104KE37	0.1	µF	murata
	C_{VREG}	GCM188R71E105KA49	1.0	µF	murata
	C_D	GCM155R11H103KA40	0.01	µF	murata
	C_{LED}	GCM155R71H104KE37	0.1	µF	murata

(Note 1) About Z_{D1}, please place according to test standard of battery line.

Please note the following

1. **External PNP transistor**
For external PNP transistor, please use the recommended device 2SAR573DFHG for this IC.
While using non-recommended device, validate the design on actual board with sufficient confirmation of the parts specifications (hfe, parasitic capacitance).
Please check hfe of the part when designing base current limit resistor. (See Features Description, section 5). As for parasitic capacitance (C_{LED} connected at LED anode), the smaller it is, the smaller its overshoot is. Use devices that has smaller parasitic capacitance than that of recommended device. Also parasitic capacitance is possible to be varied by PCB layout so please evaluate overshoot of I_{LED} on actual board. (See Features Description, Section 8 -Evaluation example, I_{LED} pulse width at PWM Dimming operation).

2. **Power supply steep variation**
This IC is validated with test conditions as per ISO7637-2 standards.
There is possibility of unexpected LED regulation (peak current of output etc.) due to sudden transients outside the specification range standards in input power supply. Please check the maximum ratings of LED and evaluate on actual board for any unexpected LED regulation.

Application Examples - continued

(2) I_{LED}=120 mA, PWM ON Duty=10 %

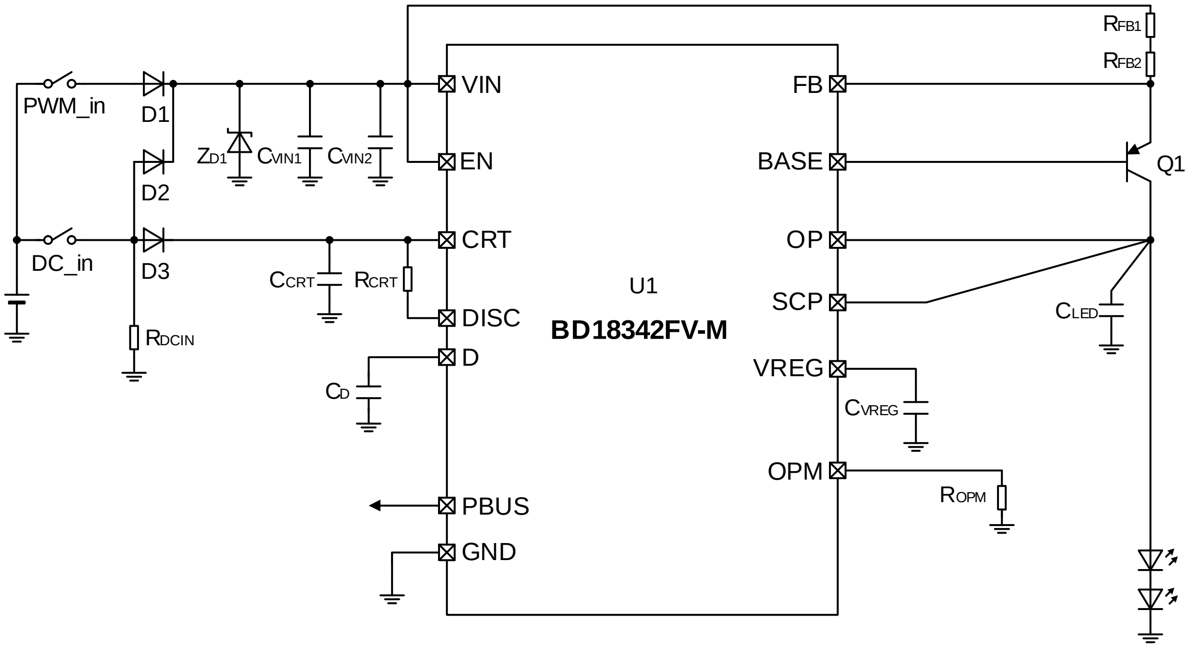


Figure 27. Application Example 2
(I_{LED} 120 mA, LED white 2 strings, PWM ON Duty: 10 %(Pulse width: 0.334 ms), PWM frequency: 300 Hz)

Recommended Parts List 2
(I_{LED} 120 mA, LED white 2 strings, PWM ON Duty: 10 %(Pulse width: 0.334 ms), PWM frequency: 300 Hz)

Parts	No	Parts Name	Value	Unit	Product Maker
IC	U1	BD18342FV-M	-	-	ROHM
Diode	D1, D2	RFN2LAM6STF	-	-	ROHM
	D3	RFN1LAM6STF	-	-	ROHM
	Z_{D1}	TND12H-220KB00AAA0	-	-	NIPPON CHEMICON
Transistor PNP	Q1	2SAR573DFHG	-	-	ROHM
Resistor	R_{FB1}	LTR10EVHFL2R70	2.7	Ω	ROHM
	R_{FB2}	LTR10EVHFL2R70	2.7	Ω	ROHM
	R_{CRT}	MCR03EZPFX3601	3.6	kΩ	ROHM
	R_{OPM}	MCR03EZPFX3902	39	kΩ	ROHM
	R_{DCIN}	ESR10EZPF2001	2	kΩ	ROHM
Capacitor	C_{VIN1}	GCM32ER71H475KA40	4.7	μF	murata
	C_{VIN2}	GCM155R71H104KE37	0.1	μF	murata
	C_{VREG}	GCM188R71E105KA49	1.0	μF	murata
	C_{CRT}	GCM155R71H104KE37	0.1	μF	murata
	C_D	GCM155R11H103KA40	0.01	μF	murata
	C_{LED}	GCM155R71H104KE37	0.1	μF	murata

(Note 1) About Z_{D1}, please place according to test standard of battery line.

Application Examples - continued

(3) I_{LED}=524 mA, PWM ON Duty=10 %

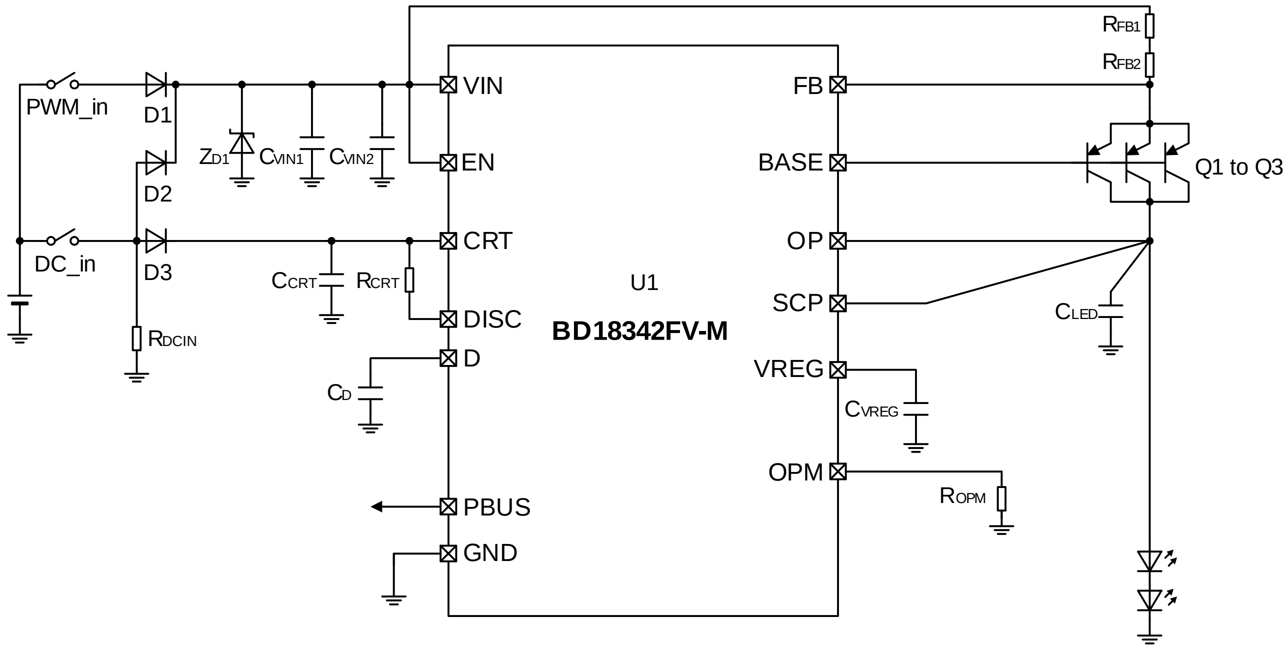


Figure 28. Application Example 3
(I_{LED} 524 mA, LED white 2 strings, PWM ON Duty: 10 %(pulse width: 0.334 ms), PWM frequency: 300 Hz)

Recommended Parts List 3
(I_{LED} 524 mA, LED white 2 strings, PWM ON Duty: 10 %(pulse width: 0.334 ms), PWM frequency: 300 Hz)

Parts	No	Parts Name	Value	Unit	Product Maker
IC	U1	BD18342FV-M	-	-	ROHM
Diode	D1, D2	RFN2LAM6STF	-	-	ROHM
	D3	RFN1LAM6STF	-	-	ROHM
	Z_{D1}	TND12H-220KB00AAA0	-	-	NIPPON CHEMICON
Transistor PNP	Q1 to Q3	2SAR573DFHG	-	-	ROHM
Resistor	R_{FB1}	LTR10EVHFLR620	0.62	Ω	ROHM
	R_{FB2}	LTR10EVHFLR620	0.62	Ω	ROHM
	R_{CRT}	MCR03EZPFX3601	3.6	kΩ	ROHM
	R_{OPM}	MCR03EZPFX3902	39	kΩ	ROHM
	R_{DCIN}	ESR10EZPF2001	2	kΩ	ROHM
Capacitor	C_{VIN1}	GCM32ER71H475KA40	4.7	µF	murata
	C_{VIN2}	GCM155R71H104KE37	0.1	µF	murata
	C_{VREG}	GCM188R71E105KA49	1.0	µF	murata
	C_{CRT}	GCM155R71H104KE37	0.1	µF	murata
	C_D	GCM155R11H103KA40	0.01	µF	murata
	C_{LED}	GCM155R71H104KE37	0.1	µF	murata

(Note 1) About Z_{D1}, please place according to test standard of battery line.

Application Examples - continued

(4) I_{LED}=150 mA, Three Rows Drive, PWM ON Duty=10 %

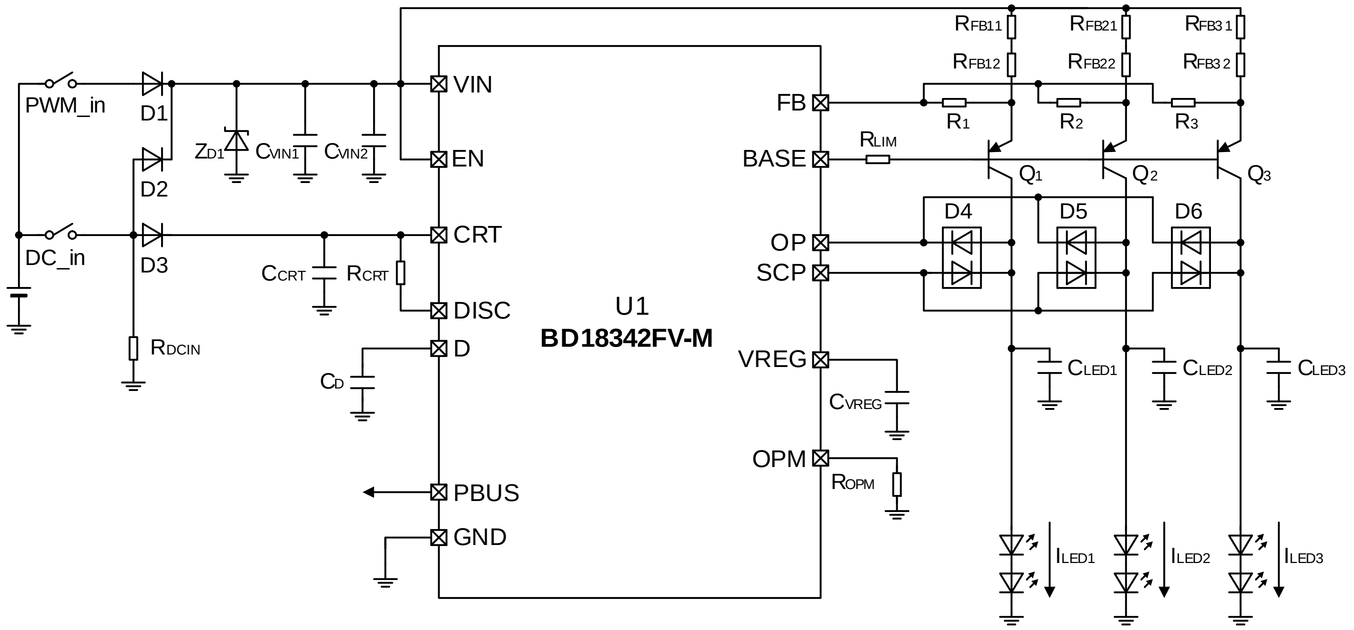


Figure 29. Application Example 4
(I_{LED1} to I_{LED3} 150 mA, LED white 2 strings x 3, PWM ON Duty: 10 %(pulse width: 0.334 ms), PWM frequency: 300 Hz)

Refer to Application Note of BD1834xFV-M series for details about the multiple rows drive such as the one above.

Power Dissipation

Thermal design should meet the following equation.

$$P_d > P_C$$

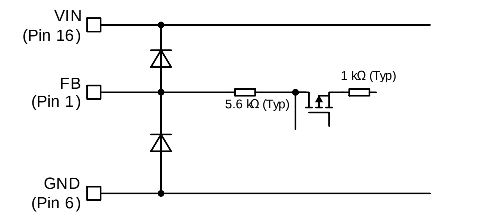
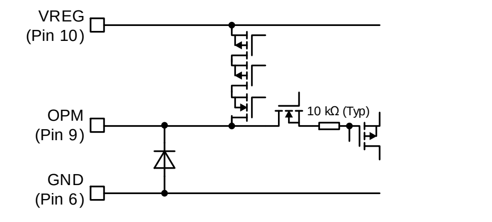
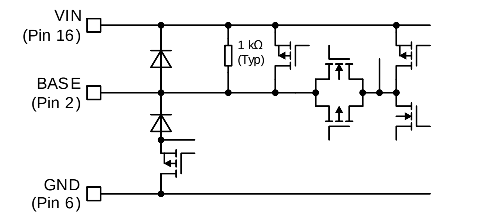
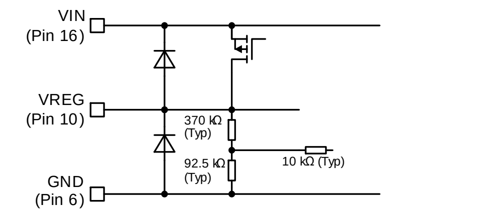
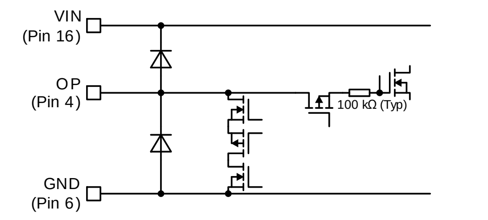
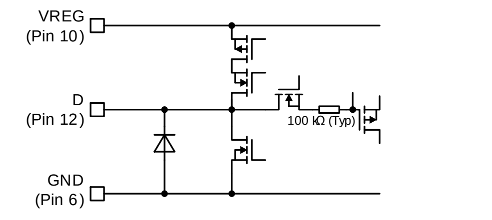
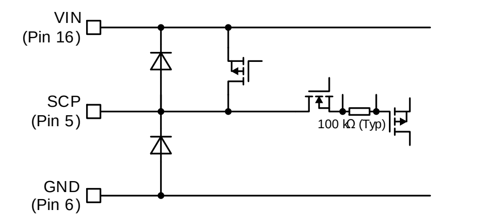
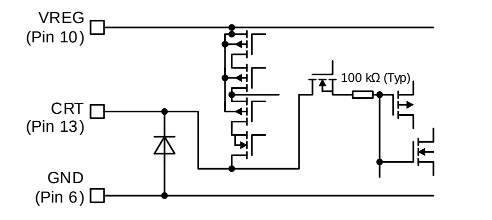
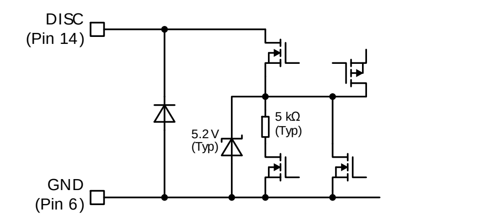
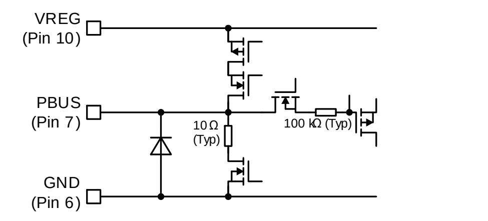
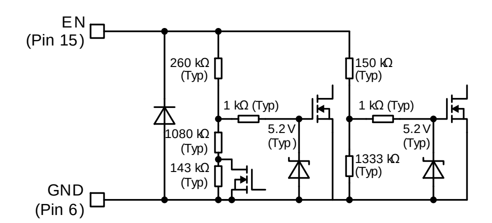
$$P_d = (1/\theta_{JA}) \times (T_{jmax} - T_a) or (1/\Psi_{JT}) \times (T_{jmax} - T_T)$$

$$P_C = V_{IN} \times I_{VIN2} + V_{BASE} \times I_{BASE}$$

where:

P_d is the power dissipation.
P_C is the power consumption.
V_{IN} is the VIN pin voltage.
I_{VIN2} is the circuit current at normal mode.
V_{BASE} is the BASE pin voltage.
I_{BASE} is the BASE pin sink current.
θ_{JA} is the thermal resistance of junction to ambient.
Ψ_{JT} is the thermal characterization parameter of junction to center case surface.
T_{jmax} is the maximum junction temperature(150 °C).
T_a is the ambient temperature.
T_T is the case surface temperature.

I/O Equivalence Circuits

<table>
<tr><th>No.</th><th>Pin Name</th><th>I/O Equivalence Circuit</th><th>No.</th><th>Pin Name</th><th>I/O Equivalence Circuit</th></tr>
<tr><td>1</td><td>FB</td><td></td><td>9</td><td>OPM</td><td></td></tr>
<tr><td>2</td><td>BASE</td><td></td><td>10</td><td>VREG</td><td></td></tr>
<tr><td>3</td><td>N.C.</td><td></td><td>11</td><td>N.C.</td><td></td></tr>
<tr><td>4</td><td>OP</td><td></td><td>12</td><td>D</td><td></td></tr>
<tr><td>5</td><td>SCP</td><td></td><td>13</td><td>CRT</td><td></td></tr>
<tr><td>6</td><td>GND</td><td>-</td><td>14</td><td>DISC</td><td></td></tr>
<tr><td>7</td><td>PBUS</td><td></td><td>15</td><td>EN</td><td></td></tr>
<tr><td>8</td><td>N.C</td><td></td><td>16</td><td>VIN</td><td>-</td></tr>
</table>

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

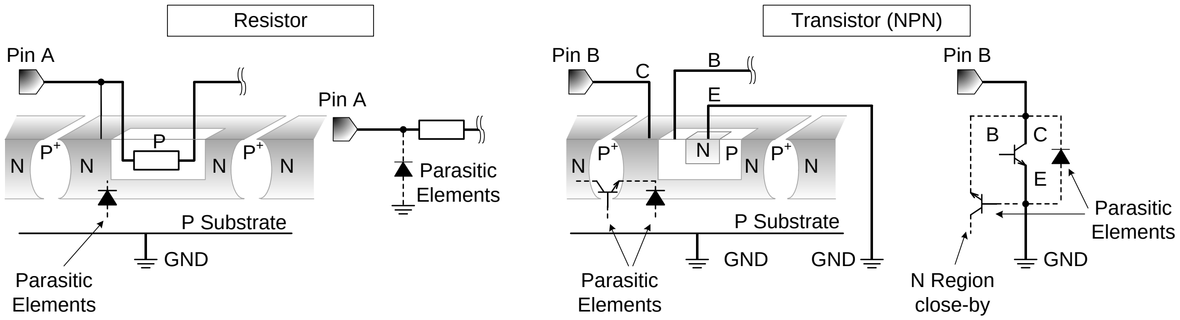


Figure 30. Example of Monolithic IC Structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

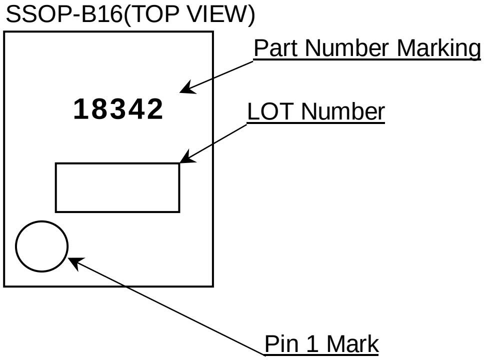
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

B D 1 8 3 4 2 F V - M E 2

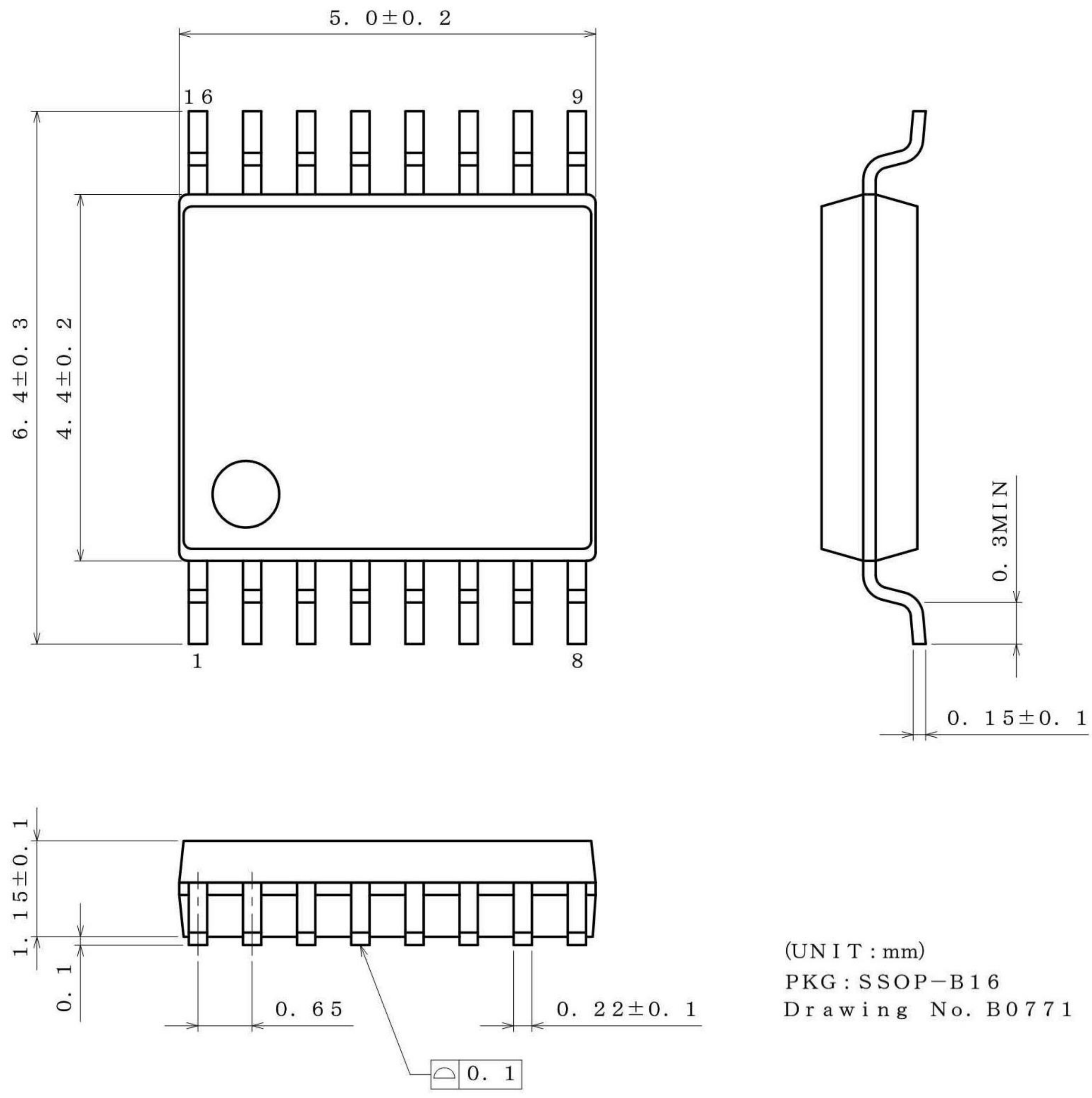
- Product Name: BD18342
- Package: FV: SSOP-B16
- Product Rank: M: for Automotive
- Packaging and forming specification: E2: Embossed tape and reel

Marking Diagram



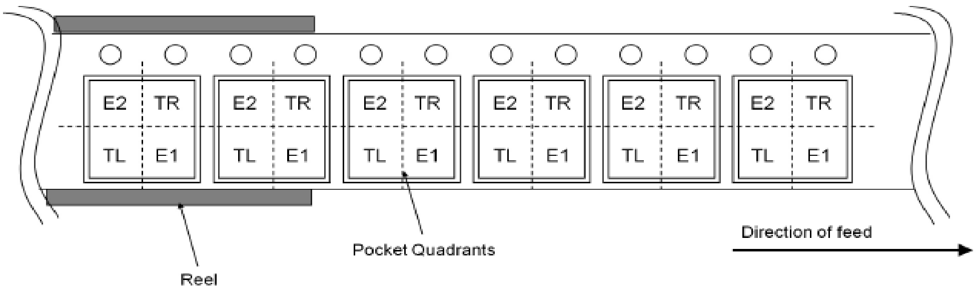
Physical Dimension and Packing Information

Package Name	SSOP-B16



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



Revision History

Date	Revision	Changes
18.Sep.2018	001	New Release

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

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Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

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