LED driver IC series for Automotive lamps

LED Driver with Built-in PWM Signal Generation Circuit

BD18351EFV-M

General Description

BD18351EFV-M is an LED driver with built-in 1ch boost controller. It is an optimal IC for LED drive for head lamp / DRL, tail lamp and turn lamp capable of realizing boost and buck boost with high-side detection of LED current setting against output voltage.
Further, cost saving and downsizing of the set can be realized, since it contains CRTIMER which enables PWM dimming without microcomputer for applications requiring PWM dimming of DRL, etc.

Key Specifications

- Input Voltage Range: 4.5 V to 65 V
- Output Voltage Range: 6.0 V to 65 V
- Absolute Maximum Input / Output Voltage: 70 V
- Minimum PWM Dimming Pulse Width: 50 µs

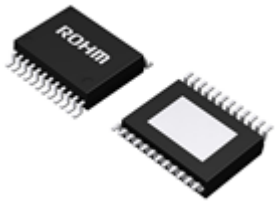
Features

- AEC-Q100 Qualified *(Note 1)*
- Built-in Switching DC / DC Controller.
- LED Current Setting High Side Detection Method
- LED Current Precision: ±3.0% (–40 °C to 125 °C)
- PWM Signal Generation Circuit with Built-in CRTIMER (External PWM Dimming Control is possible.)
- Built-in Spread Spectrum Function
- Built-in LED Open Detection Function
- Built-in LED Anode to Ground Short Function

(Note 1) Grade1

Package

Package	W(Typ) × D(Typ) × H(Max)
HTSSOP-B24	7.80 mm × 7.60 mm × 1.00 mm



HTSSOP-B24

Applications

Head lamp, DRL, front position lamp, tail lamp, turn lamp

Typical Application Circuit

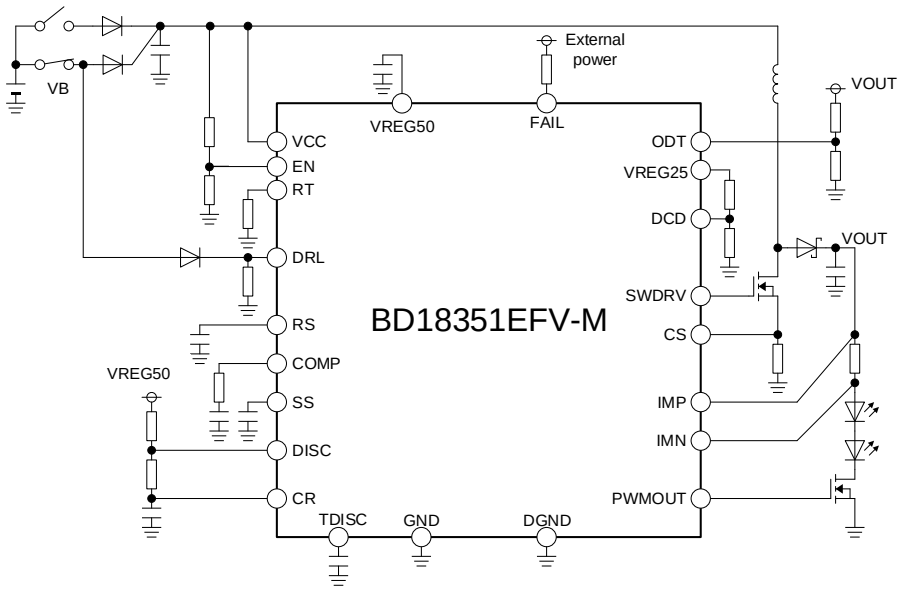


Figure 1. Typical Application Circuit

Pin Configuration

HTSSOP-B24

(TOP VIEW)

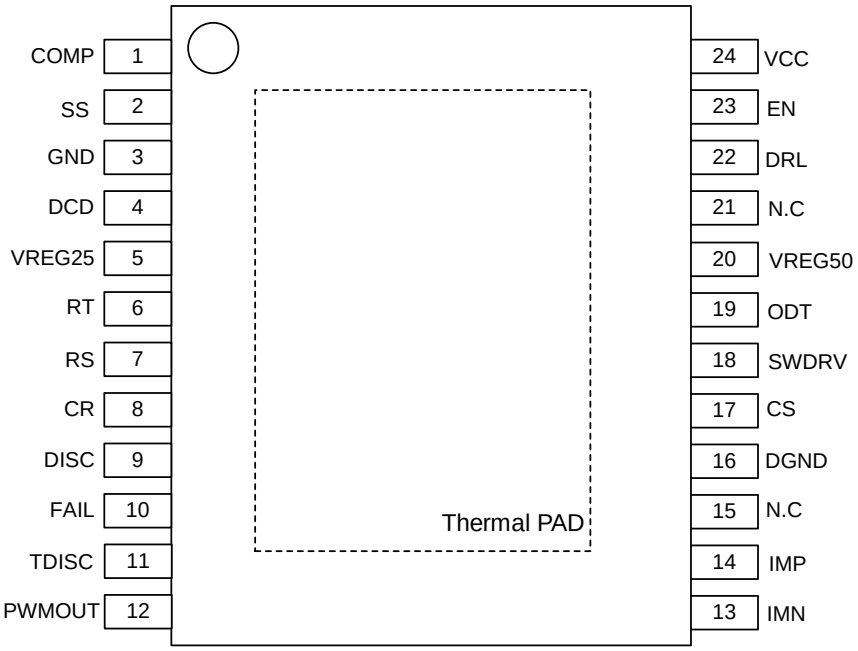


Figure 2. Pin Configuration

Pin Description

Terminal No.	Symbol	Function	Terminal No.	Symbol	Function
1	COMP	Error amplifier output phase compensation terminal	13	IMN	LED current detection terminal (-)
2	SS	Soft start setting terminal	14	IMP	LED current detection terminal (+)
3	GND	Small signal GND	15	N.C.	-
4	DCD	DC dimming terminal	16	DGND	Power GND
5	VREG25	2.5V standard voltage (DCD Exclusive terminal)	17	CS	Over current detection setting terminal
6	RT	DC / DC oscillation frequency setting terminal	18	SWDRV	External FET gate drive terminal
7	RS	Spread spectrum frequency setting terminal	19	ODT	LED open detection setting terminal
8	CR	Built-in CRTIMER PWM dimming frequency / Duty setting terminal	20	VREG50	Internal constant voltage 5.0 V output terminal
9	DISC	Built-in CRTIMER Discharge setting terminal	21	N.C.	-
10	FAIL	Error flag output terminal	22	DRL	Terminal for DRL control switching (High: 100 % mode)
11	TDISC	Discharge time setting terminal	23	EN	EN control terminal (High: Active)
12	PWMOUT	External for PWM dimming FET gate drive terminal	24	VCC	Power voltage terminal

(Pay attention that it does not correspond to reverse insertion.)

Block Diagram

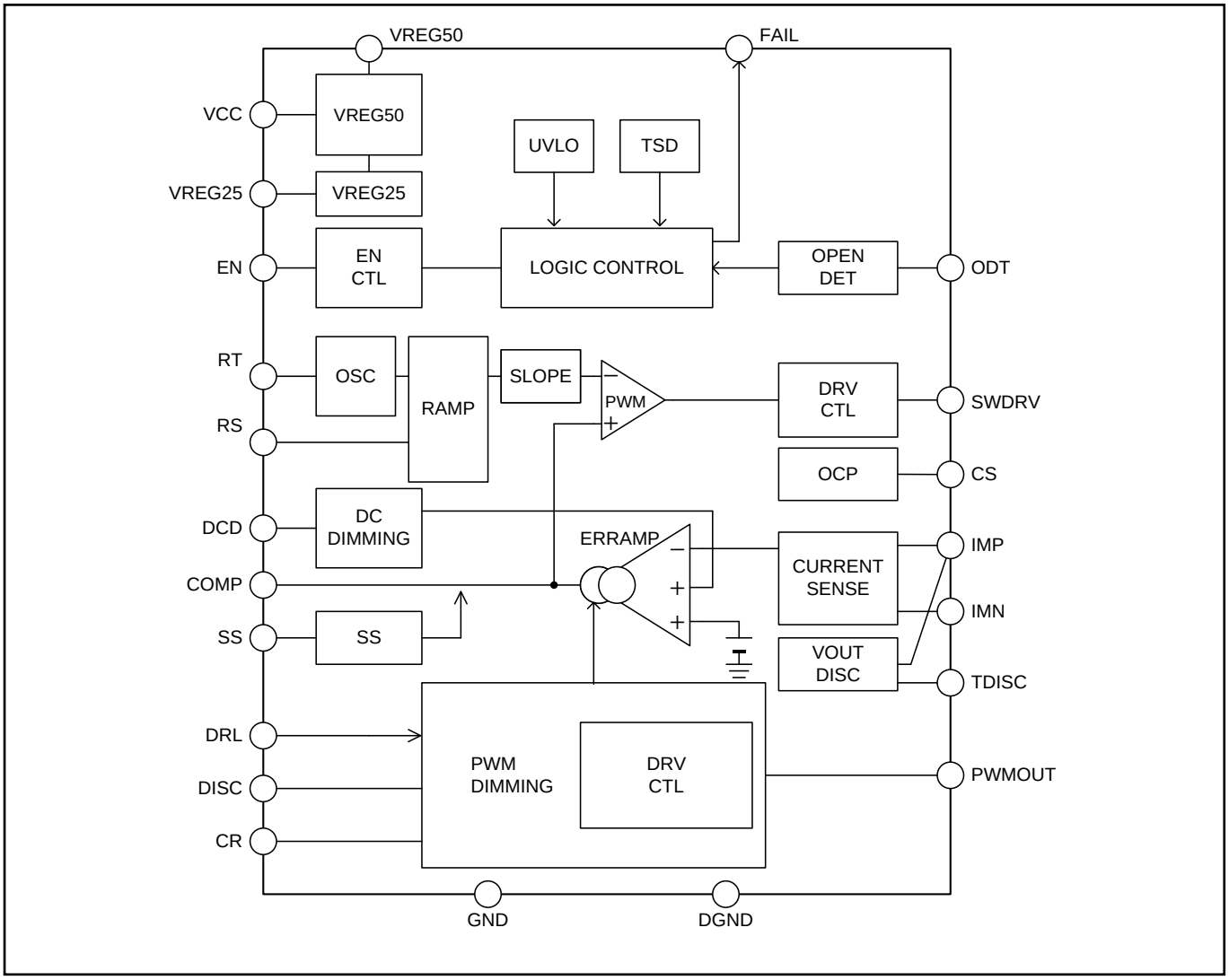


Figure 3. Block Diagram

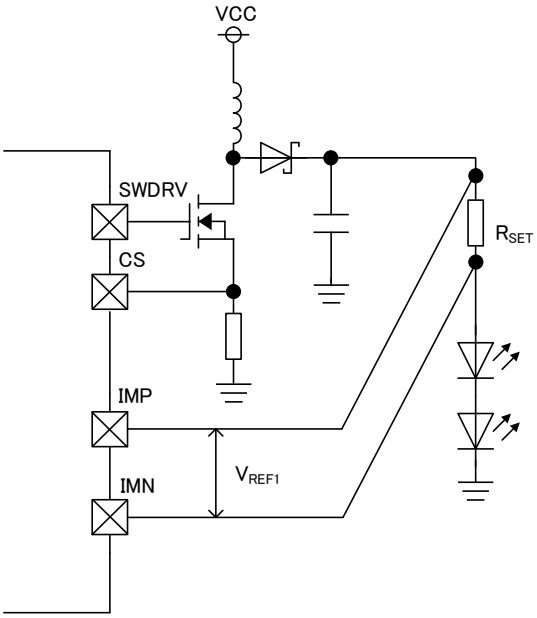
Description of Blocks

1. Standard voltage (VREG50)

5 V (Typ) is generated from VCC input voltage. This voltage (VREG) is used as power supply for internal circuit, and is also used to fix terminal at high voltage outside the IC. Please connect C_{VREG50} = 2.2 µF (Typ) as phase compensation capacity for VREG50 terminal. If C_{VREG50} is not connected, circuit operation will become markedly unstable. In addition, please do not use VREG50 as a power supply except this IC.

2. Concerning LED current setting and luminance adjustment(CURRENTSENSE)

(1) Concerning LED current setting method



LED current can be calculated by the following formula.

$$I_{LED} = \frac{V_{REF1}}{R_{SET}} \times \frac{V_{DCD}}{1.21V}$$

However, assign V_{DCD} = 1.21 V in the case of V_{DCD} > 1.21 V.

(Example)
In the case of connection of R_{SET} = 0.4 Ω, V_{DCD} = 0.6 V,

$$I_{LED} = \frac{0.2V}{0.4\Omega} \times \frac{0.6V}{1.21V} \fallingdotseq 0.25A$$

I_{LED}: LED current
V_{REF1}: Standard voltage for LED current setting (200 mV (Typ)
R_{SET}: Resistance for LED current setting
V_{DCD}: DCD terminal voltage

Figure 4. LED Current Setting Method

(2) Concerning luminance adjustment by PWM dimming control(PWM DIMMING)

PWM dimming control with built-in CR timer

PWM dimming is operated in 100 % by connecting Di to DRL terminal and turning DRL terminal to High as shown in Figure 1 On the other hand, when DRL terminal is turned low and configuration is made as shown in Figure 5, internal CR timer will operate, triangle wave is generated by CR terminal, PWMOUT terminal will be controlled to turn LED current off in CR voltage rise zone and turn LED current on in CR voltage fall zone. CR voltage rise / fall time can be set by the values of external parts (C_{CR}, R_{DISC1}, R_{DISC2}). Refer to the next page for setting method. In addition, the recommended operation frequency is 100 Hz to 2 kHz, On Duty 2 % to 45 %, and the recommended range of the external component values are 0.01 µF to 1.0 µF for C_{CR} and 10 kΩ to 33 kΩ for R_{DISC2}.(PWM min pulse width=50 µs)

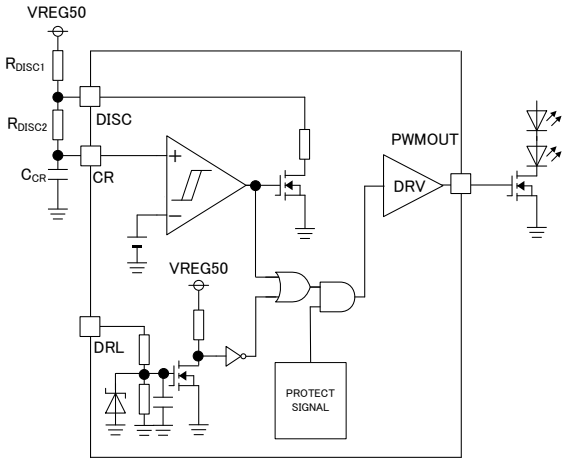
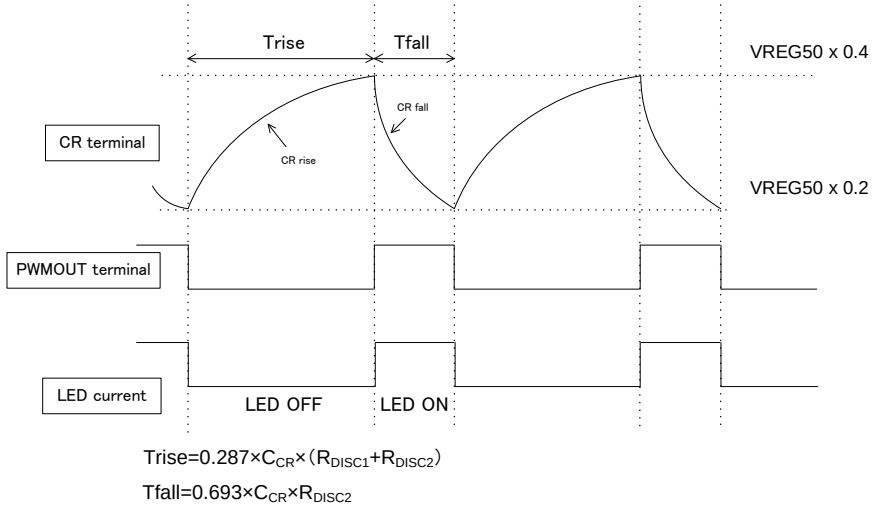


Figure 5. Example of Application Using Built-in CR Timer



Trise=0.287×C_{CR}×(R_{DISC1}+R_{DISC2})

Tfall=0.693×C_{CR}×R_{DISC2}

Figure 6. PWM Dimming Operation

CR terminal rise / fall time can be calculated as shown below.

1. CR terminal rise time T_{rise}

$$T_{rise} = 0.287 \times C_{CR} \times (R_{DISC1} + R_{DISC2}) \ [s]$$

2. CR terminal fall time T_{fall}

$$T_{fall} = 0.693 \times C_{CR} \times R_{DISC2} \ [s]$$

3. PWM dimming frequency F_{PWM}
PWM frequency is determined by T_{rise} and T_{fall}.

$$F_{PWM} = \frac{1}{(T_{rise} + T_{fall})} \ [Hz]$$

4. PWM dimming ON Duty (D_{PWM})
ON Duty of PWM is determined by T_{rise} and T_{fall} as shown in the description above.

$$D_{PWM} = \frac{T_{fall}}{(T_{rise} + T_{fall})} \times 100 \ [\%]$$

(Example) when C_{CR} = 0.1 µF, R_{DISC1} = 100 kΩ, R_{DISC2} = 20 kΩ (Typ)

$$T_{rise} = 0.287 \times C_{CR} \times (R_{DISC1} + R_{DISC2}) = 3.444 \ [ms]$$

$$T_{fall} = 0.693 \times C_{CR} \times R_{DISC2} = 1.386 \ [ms]$$

$$F_{PWM} = \frac{1}{(T_{rise} + T_{fall})} = 207 \ [Hz]$$

$$D_{PWM} = \frac{T_{fall}}{(T_{rise} + T_{fall})} \times 100 = 28.7 \ [\%]$$

PWM dimming control with external signal (microcomputer, etc.)

Dimming is possible by direct input of PWM signal from external microcomputer, etc. Input PWM signal in CR terminal. Set 'High' level voltage of input signal from microcomputer at no less than 2.5 V for CR threshold voltage, and set 'Low' level voltage at no more than 0.5 V of CR threshold voltage. Recommended input frequency range is 100 Hz to 2 kHz. Minimum pulse width is 50 µs. It's necessary that 51kΩ resister need between µ-con and CR terminal like Figure 7. When filter is required, configure filter in high side of Figure 7 51kΩ.
However verification with actual application is required as filter may cause difference between Input signal to CR terminal and PWMOUT terminal.

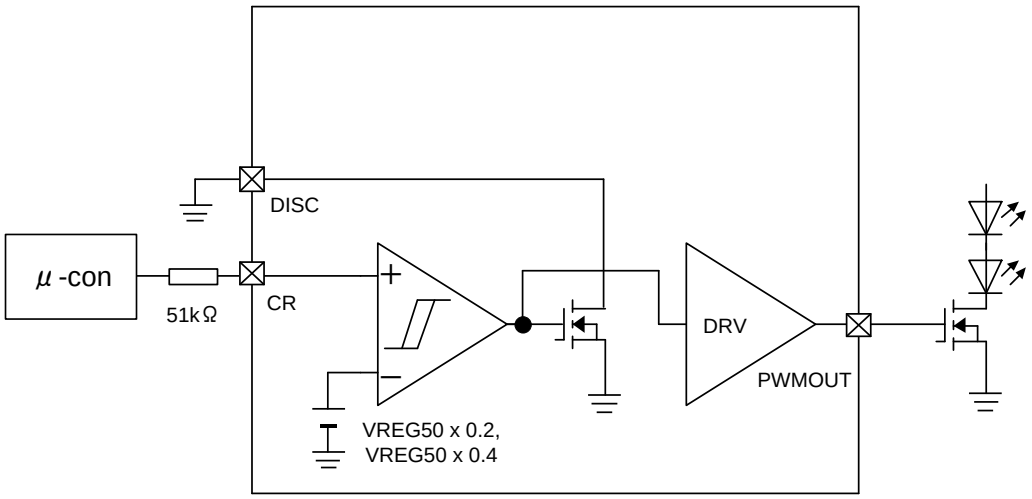


Figure 7. External Input of PWM Signal

(3) PWM Dimming with PchMOS

PWM dimming can be performed by PchMOS (Figure 8 (a) Q3) with Figure 8 configuration. In this configuration, RPWM1 / RPWM2 / RPWM3 controls gate voltage of PchMOS. If RPWM2, RPWM3 are bigger and gate capacitance of Q3 is high, this result in discrepancy in PWM ON width generated by PWMOUT pin output and LED current ON width controlled by Q3 . Please thereby perform the evaluation with the actual equipment by the constitution using PchMOS enough because it may cause instable operation such as high brightness lighting or the acoustic noise of capacitor and inductor.

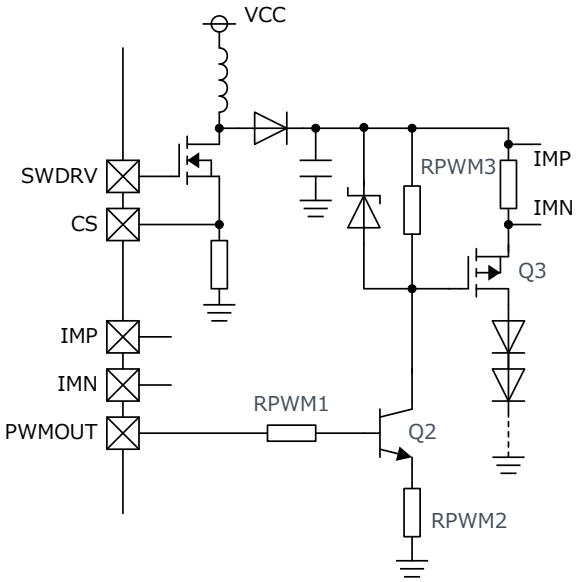


Figure 8 (a). PWM Dimming with PchMOS

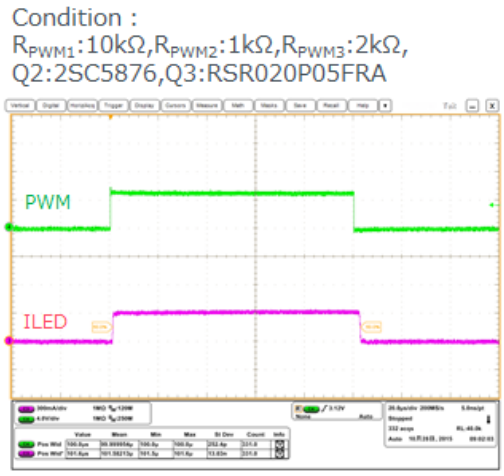
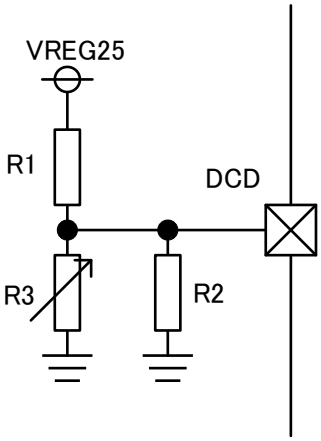
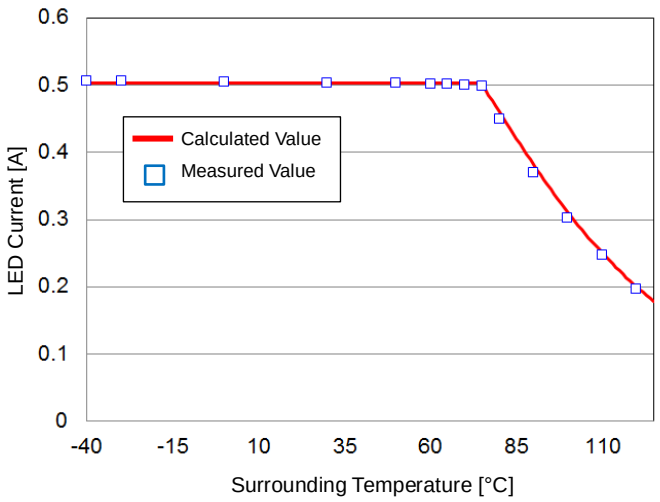


Figure 8 (b). PWM Dimming with PchMOS

(4) Brightness control by DC dimming control(DC DIMMING / VREG25)

LED current is linearly controllable corresponding to DCD terminal voltage. DCD terminal is mainly used for derating, and is used to control deterioration of LED at high temperature or to limit over current to external parts under conditions which power supply voltage fluctuates by idling stop functions, etc. (Refer to Figure 9). Recommended input range is $0.4 \leq V_{DCD} \leq$ VREG25 and LED current control starts in $V_{DCD} \leq 1.21$ V. In addition, the power supply voltage to control DCD can be controlled with high precision by using VREG25. When DC dimming is not used, short to VREG25 terminal directly.





R1: 12kΩ
R2: 100 kΩ
R3: NTCG104EF104F

Figure 9. Example of Derating Setting Using Thermistor Resistance

3. Boost DC / DC controller

(1) Concerning open detection voltage setting(OPEN DET)

Open of LED is detectable by inputting resistance division connected to anode side of LED (DC / DC output V_{OUT}) in ODT terminal. LED open detection voltage is detectable by connecting external resistors (R_{ODT1}, R_{ODT2}) as shown in Figure 10, and output voltage V_{OUT_ODT} at the time of LED open detection voltage is calculable as shown below.

$$V_{OUT\_ODT} = \frac{(R_{ODT1} + R_{ODT2})}{R_{ODT2}} \times 1.5V(Typ)$$

(Example)
LED open detection will operate with V_{OUT_ODT} = 34.5 V when R_{ODT1} = 660 kΩ and R_{ODT2} = 30 kΩ.

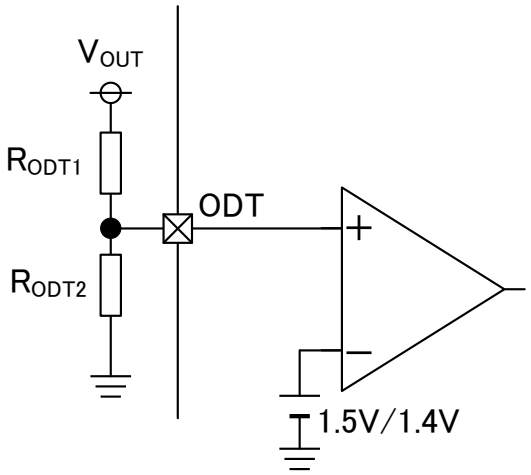


Figure 10. ODT terminal Equivalent Circuit

LED open detection voltage needs higher voltage setting than overshoot of output voltage at start up to avoid start up failure.
ODT resistor will be the current discharge path for the output capacitor when PWM = Low. Recommended value for R_{ODT1} is 600 kΩ to 1000 kΩ as Vout ripple may be large and cause LED flickering when PWM = Low with inadequate ohmic value range. Moreover, the behavior differs by characteristic of output capacitor or LED, therefore sufficient verification with actual application is required.(Vout drop can be prevented by inserting bigger output capacitor or ODT resistance.)

(2) Concerning number of LED series stages

As shown in Figure 11, although IMP terminal is connected to boost DC / DC output at highest voltage among applications.
The number of the steps of the LED which can be driven is decided by the LED opening detection voltage instead of 65V that is withstand voltage. For example, when the ODT terminal voltage V_{ODT} = 1.35 V at driving a normal LED, the maximum output voltage V_{OUT_MAX} is as follows.

$$65V \times \frac{1.35V}{1.575V} \fallingdotseq 55.7V$$

In other words, drivable LED series stage N is calculable by the formula below.

$$V_{F\_MAX} \times N + V_{REF\_MAX} < 55.7V$$

VF_MAX: maximum value of VF of LED
N: number of LED series stages
VREF_MAX: maximum value of standard voltage for LED current setting

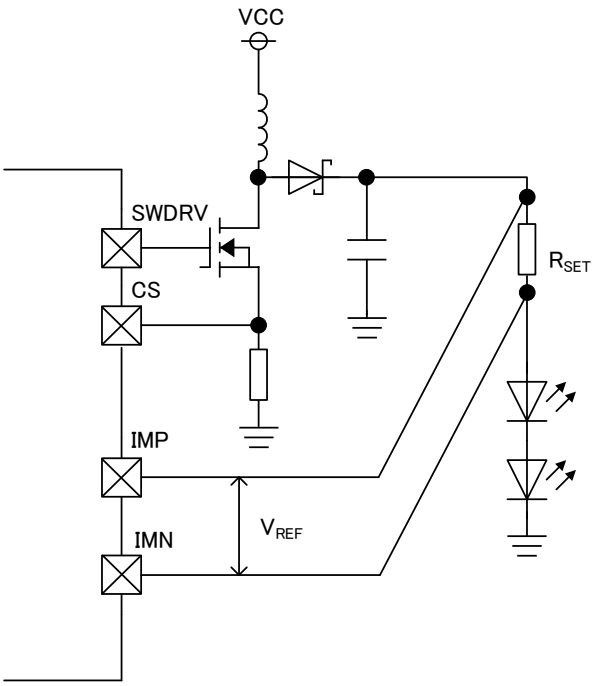


Figure 11. Example of Application Circuit

(Example)
When V_{F_MAX} = 3.5 V and V_{REF_MAX} = 0.206 V, number of drivable LED series stages N is as shown below.

$$N < (55.7V - 0.206V) / 3.5V = 15.86$$

LED drivable number of LED stages is 15.

(3) Concerning oscillation frequency F_{osc}(OSC)

Connection of resistance with RT terminal enables setting of oscillation frequency as shown in Figure 12. Connection of R_{RT} decides charge and discharge current for internal capacitor and changes DC / DC oscillation frequency. Set R_{RT} by reference to the theoretical formula below. Recommended range is 14 kΩ to 51 kΩ. Pay attention that switching may stop if recommended frequency setting range is exceeded, and operation assurance is not possible.

$$F_{OSC}[kHz] = \frac{99 \times 10^2}{R_{RT}[k\Omega]}$$

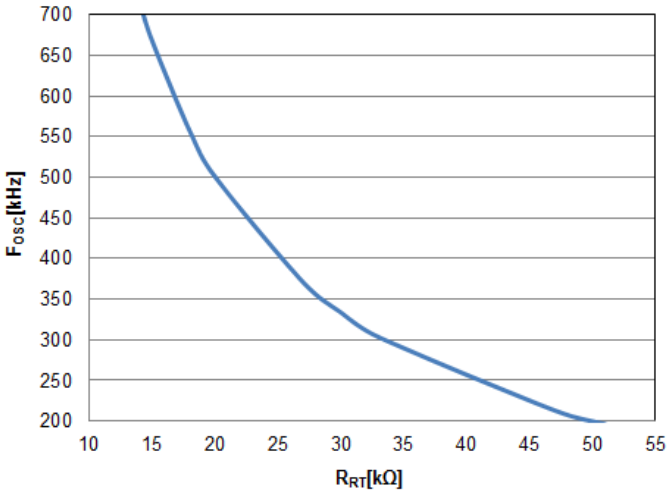


Figure 12. R_{RT} vs DC / DC Oscillation Frequency F_{OSC}

(4) Concerning spread spectrum setting(RAMP)

Connection of capacitor to RS terminal enables operation in Spread spectrum mode (SSCG mode). Comparator of 0.6 V (Typ) / 0.75 V (Typ) standard voltage is built in RS terminal, and DC / DC oscillation frequency is diffused by changing RT terminal voltage to triangle waveform with the capacitor connected to RS terminal in SSCG mode. Theoretical attenuation ΔD [dB] is calculable by the formula below.

$$\Delta D[dB] = 10 \times \log\left(\frac{F_{RS}\,[kHz]}{F_{OSC\_RAMP}[kHz] \times 0.222}\right)$$

F_{OSC_RAMP}: oscillation frequency when SSCG mode is ON (Center)
F_{OSC}: oscillation frequency when SSCG mode is OFF
C_{RS}: RS terminal connection capacitor
R_{RT}: RT terminal connection resistance

However, setting value of DC / DC oscillation frequency differs depending on ON / OFF of SSCG mode. In order to operate when SSCG mode is ON in the same frequency zone as when SSCG mode is OFF, select from Figure 12 RT resistance for 1.18 times as high DC / DC oscillation frequency as the DC / DC oscillation frequency. When SSCG mode is not used, short-circuit RS terminal and VREG50 terminal.

Further, F_{RS} can be calculated by the formula below. Setting should satisfy the formula of 0.3 kHz ≤ F_{RS} ≤ 10 kHz.

$$F_{RS}[kHz] = \frac{9}{8 \times R_{RT}[k\Omega] \times C_{RS}[\mu F]}$$

(Example) When using at DC / DC oscillation frequency (F_{OSC_RAMP}) of 300 kHz with SSCG mode is ON, select RRT ≈ 28 kΩ from Figure 12 to make DC / DC oscillation frequency (F_{OSC}) to be 354 kHz. When operating under this condition with connection of CRS = 0.047μF and with SSCG mode ON, effect of ΔD = -18.9 dB can be predicted.

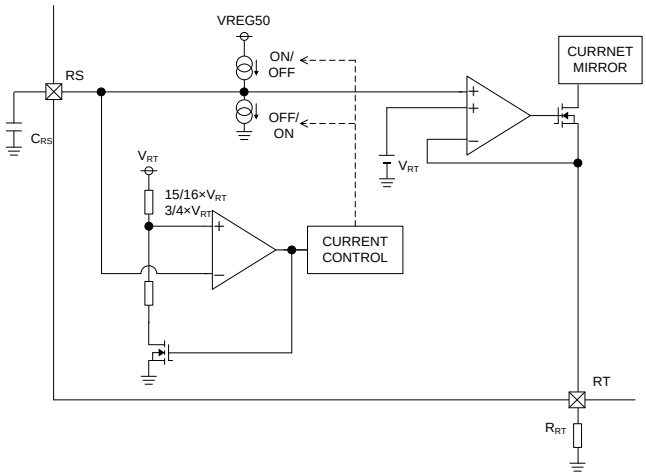


Figure 13. Equivalent Circuit Diagram of RS and RT terminals

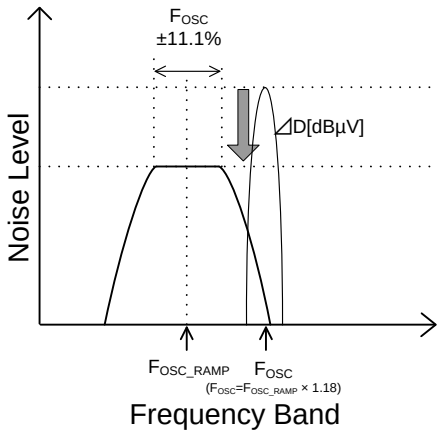


Figure 14. Noise Level Comparison with SSCG Mode ON / OFF

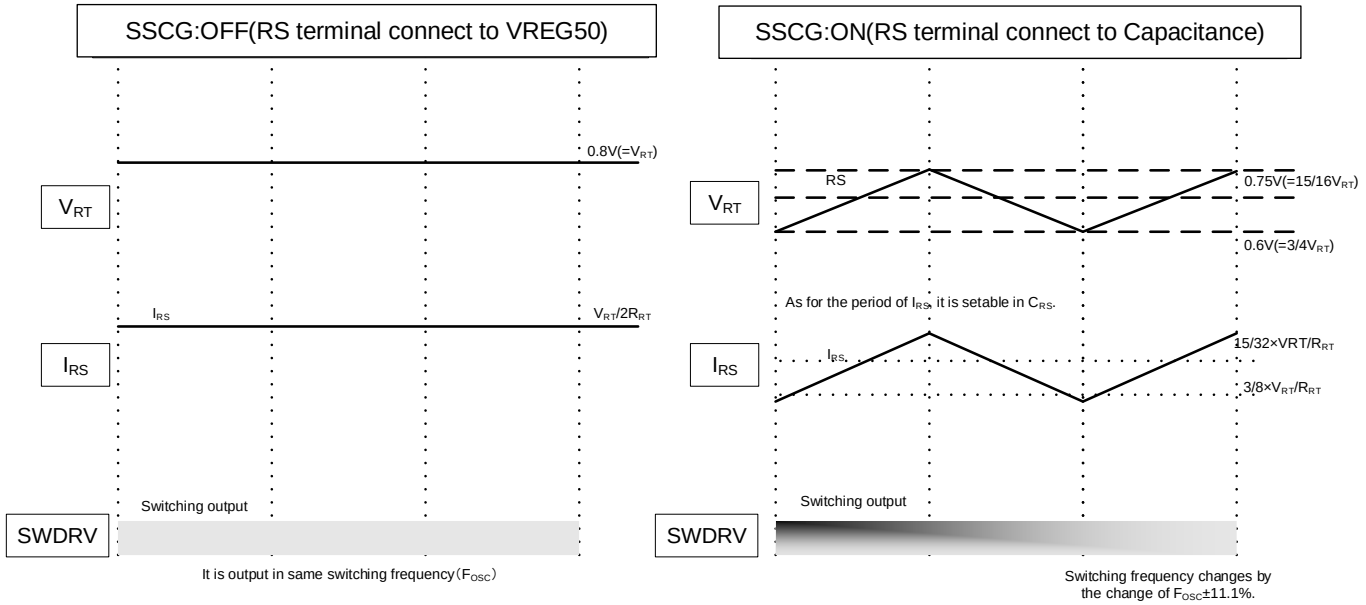


Figure 15. Timing Chart when SSCG Mode is ON / OFF

Because switching frequency changes in High section of the PWM like Figure 16 when spectrum spreading is controlled in a PWM dimming, an output voltage ripple changes in A and B. In addition, the LED current is also affected by the ripple as it may seem that LED flickers when this occurs periodically, please thoroughly verify with the actual equipment. As countermeasures, make the frequency of the RS pin fast to reduce a ripple in High section of the PWM.

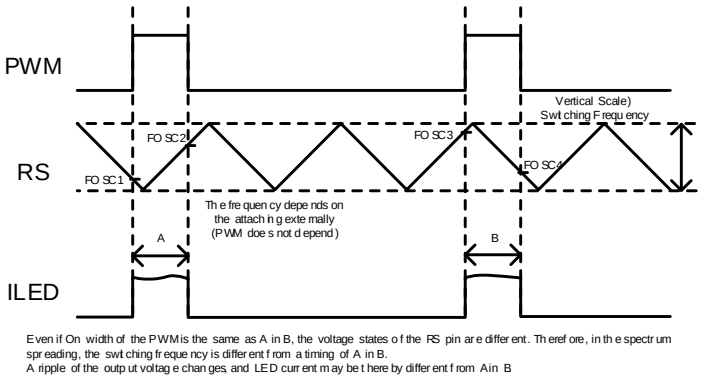


Figure 16. Spectrum Spread Action in the PWM Dimming

(5) Soft start function(SS)

Soft start function is built-in so that incoming current can be prevented by insertion of external capacitor. The charge current of the soft start is 5 μA (Typ) and will be as Figure 17 independent to PWM. The inrush current can be suppressed by increasing soft start capacity, but boot-time becomes longer. On the other hand, as for the boot-time, it becomes faster by lowering soft start capacity, attention is necessary because an inrush current becomes bigger, and may cause acoustic noise of the coil during the startup. The soft start capacity is recommended to be 0.01 μF to 1 μF to suspend the overshoot of the LED current during start up.

The RS terminal is pulled up by VREG50 until SS terminal arrives at 70%of VREG50 as soon as EN terminal is inputted High voltage . After that, RS terminal starts to be controlled.
(See the timing chart of SS terminal and RS terminal in the P.28 Figure.44)
Therefore, Spread spectrum don't operate as soon as EN terminal is inputted High voltage, even if connect a capacitor to RS terminal

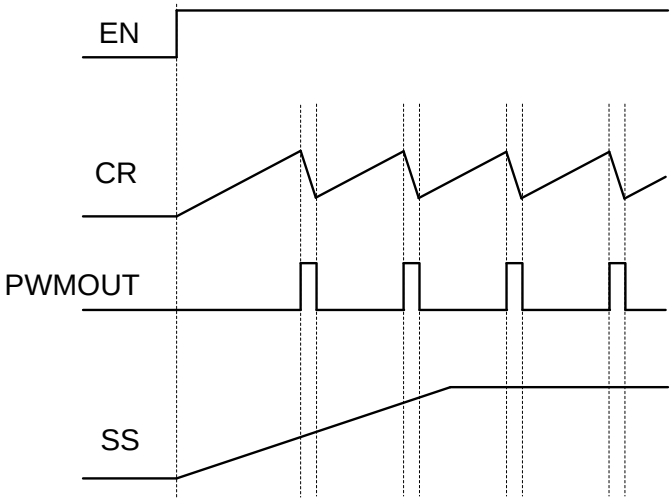


Figure 17. SS Operation Timing Chart

(6) Concerning start up time(ERRAMP)

Startup time difference between PWM = 100 % (DRL = High) and PWM dimming control is described in this paragraph

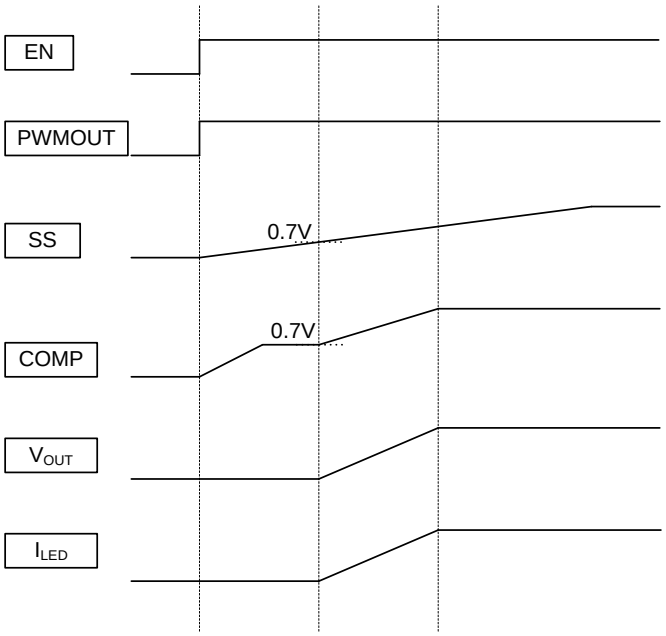


Figure 18 (a). PWM = 100% start up

SS terminal and COMP terminal is charged, When EN is inputted. Until SS terminal reaches 0.7 V, COMP terminal is fixed at 0.7 V. When SS terminal exceeds 0.7V, COMP terminal starts to rise up to voltage which can output required switching duty determined by input/output voltage difference.

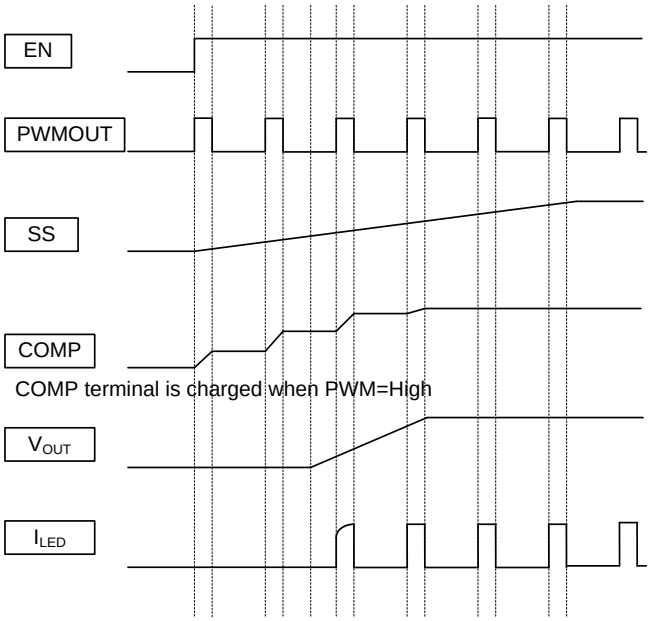


Figure 18 (b). PWM Dimming start up

During PWM control, SS terminal is charged synchronized with EN while COMP terminal is charged synchronized with PWM. Startup time is basically same with previous description but as charge of COMP terminal is synchronized with PWM, COMP voltage rise to the voltage which can output required switching duty will be slower resulting In longer start up time compared with PWM = 100 % operation. Especially by reducing PWM dimming rate, start up time will be longer.

Figure 19 describes actual measurement result of startup time.
Measurement Condition: V_{CC} = 12 V, F_{PWM} = 200 Hz, V_{OUT} = 25 V (LED 7series), Ta = 27deg, other condition as described in P.38.
(Startup time will be from UVLO release to V_{OUT} reaching 90 %.)

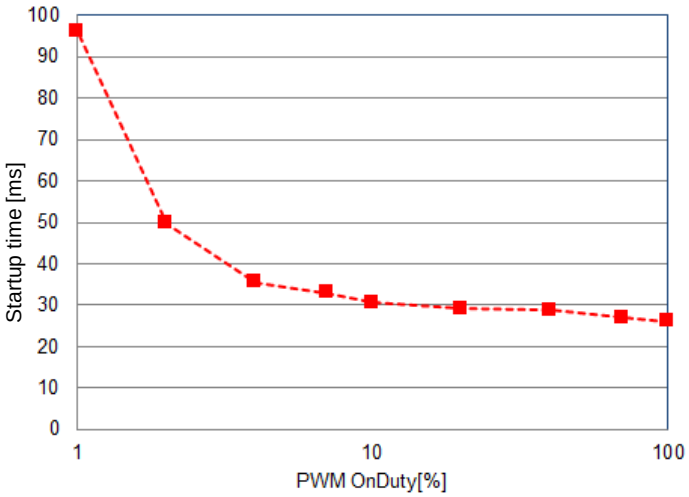


Figure 19. Startup time measurement data

Larger the C_{PC} constant is, and smaller D_{PWM} is, start up time will be longer. Startup time shall be sufficiently evaluated in actual application.

4. Self-assessment function

Table 1. Concerning detection condition and operation after detection of each protection function (when VCC = 13 V)

Protection function	Detection condition		Operation after detection	Error flag output (Note 1)
	[Detection]	[Release]		
UVLO	V_{CC} < 3.9 V	V_{CC} > 4.25 V	Shut down of all blocks (Other than VREG50 / VREG25)	At time of detection: FAIL High→Low At time of recovery: FAIL Low→High
TSD	Tj > 175 °C	Tj < 150 °C	Shut down of all blocks (VREG50 / VREG25 are included)	-
OCP	V_{CS} ≥ 300 mV	V_{CS} < 300 mV	Switching output is Off	-
SCP	V_{IMP}-V_{IMN} ≥ 0.3 V	V_{IMP} - V_{IMN} < 0.3 V (Timer time depends on TDISC setting)	Shut down of all blocks (Other than VREG50 / VREG25)	At time of detection: FAIL High→Low At time of recovery: FAIL Low→High
LED open detection	V_{ODT} > 1.5 V	V_{ODT} < 1.4 V	Shut down of all blocks (Other than VREG50 / VREG25)	At time of detection: FAIL High→Low At time of recovery: FAIL Low→High

(Note1) FAIL output shown above is FAIL terminal voltage in the case of pull-up resistance such ad external power.

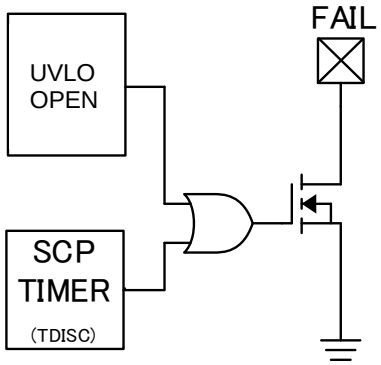


Figure 20. Protection Flag Output Part Block Diagram

(1)Low voltage malfunction protection function (UVLO)

The UVLO shuts down all the circuits except VREG50, VREG25 when V_{CC} < 3.9V (Typ) And UVLO is released by Vcc > 4.25 V (Typ).

(2) Temperature protection function (TSD)

TSD shuts circuits other than VREG at 175 °C (Typ) and recovers them at 150 °C (Typ).

(3) Over current protection function (OCP)

Over current is detected by the detection resistance with which current flowing in power FET is connected to source side. Over current protection function operates when CS terminal voltage is no less than 300 mV (Typ).The over current protection function controls DC / DC switching outputs.

(4) Output ground detection function (SCP)

When, in an application circuit such as Figure 45, LED Anode- GND short-circuits, the potential difference of IMP terminal and the IMN terminal is more than 0.3 V (Typ), and a ground detection function works, and the output is off. When ground protection is activated, charge (11 μA (Typ)) is started to a capacitor connected to TDISC terminal (recommend range: 0.01μF to 0.47μF). After TDISC terminal voltage arrived at 1.0V (Typ), the TDISC terminal discharges and Low → High outputs SWDRV / PWMOUT again. A ground detection function works again afterwards when the potential difference of IMP terminal and the IMN terminal becomes than 0.3 V (Typ). In addition, it works normally when TDISC terminal voltage becomes less than 0.3V (Typ), and the potential differences of IMP terminal and the IMN terminal become less than 0.3 V (Typ). As for the details, please refer to Figure 21. (Note that GND short-circuit of the IMP terminal cannot be detected.)

(5) LED open detection function

When ODT terminal voltage is above 1.5 V (Typ), LED open detection operates to reset SWDRV / PWMOUT = Low, and discharges SS again, outputs Fail High → Low, and the output voltage decreases by ODT resistance. When ODT terminal voltage is less than 1.4 V (Typ), begins to recharge SS, re-starts DC / DC operation and outputs FAIL Low→High.

Timing chart at the time of protection circuit operation (DRL = High)

Output ground short protection function

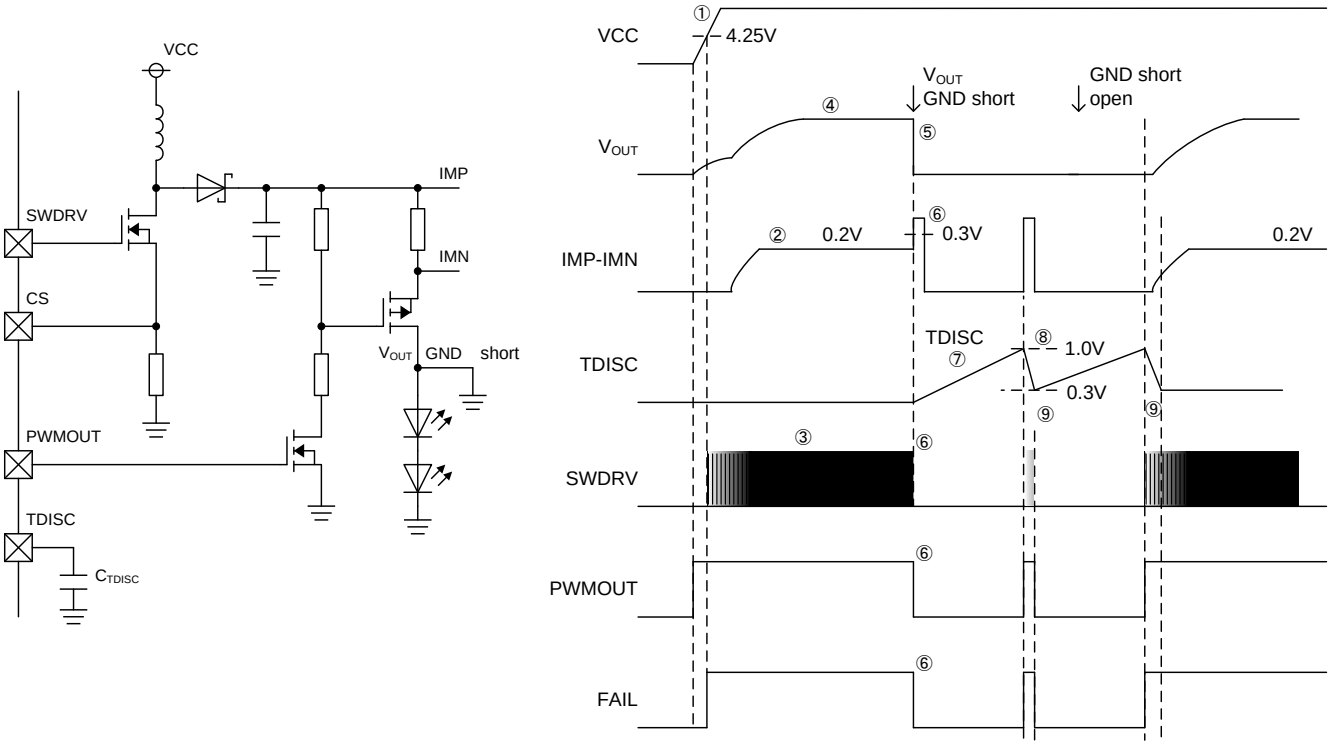


Figure 21. Output Ground short protection operation timing chart

When GND short circuit occurs in such conformation as shown in Figure 1, large current continues to flow from VCC.

① UVLO is cancelled when VCC > 4.25 V (Typ).
② IMP-IMN terminal voltage rises to become 200 mV.
③ Switching Duty gradually expands and is stabilized at IMP-IMN of 200 mV.
④ Output voltage is stabilized.
⑤ LED Anode-GND short-circuits.
⑥ It becomes IMP-IMN ≥ 0.3 V (Typ) and performs output Short circuit detection (SCP) and outputs SWDRV / PWMOUT = Low. Discharges an SS terminal and the FAIL terminal changes into High → Low.
⑦ When SCP is detected, capacitor connected to TDISC will be charged (11 µA (Typ)) until V_{TDISC} becomes 1.0 V (Typ).
⑧ Once SCP detection is released at V_{TDISC} ≥ 1.0 V (Typ), capacitor connected to TDISC starts to discharge, and SS charging, SWDRV / PWMOUT operate normally.
⑨ If SCP condition V_{TDISC} ≥ 0.3 V (Typ) is fulfilled restarts from condition “6” operates normally if SCP condition is not fulfilled.

Operation described above is performed in the LED anode ground short fault. However, even if SCP is detected by the potential difference of IMP pin and the IMN pin, there is delay time of internal circuit after detection and require time before PchMOS is off. Therefore allowable current of PchMOS may be exceeded transiently.(It may be exceeded in “8” of the timing mentioned above.) Therefore, like Figure 22, PMOS can be turned off on an expressway by adding PNP Tr externally.
When Output shorts to ground while supply voltage dropping, Gate voltage may not be turned off. If sufficient Gate voltage cannot be secured SCP may not be detected.

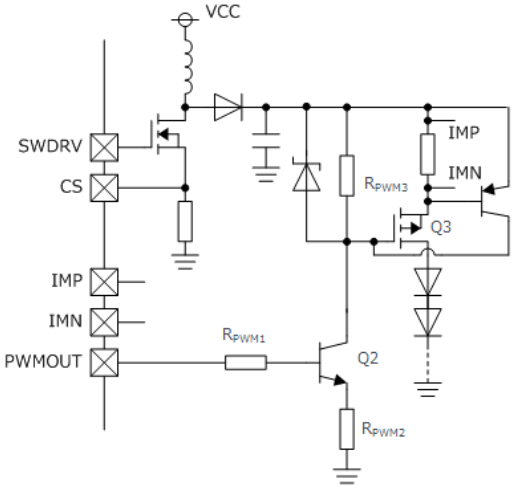


Figure 22. LED Anode Ground Fault Protection Attaching Externally Circuitry

LED open protection function (DRL = High)

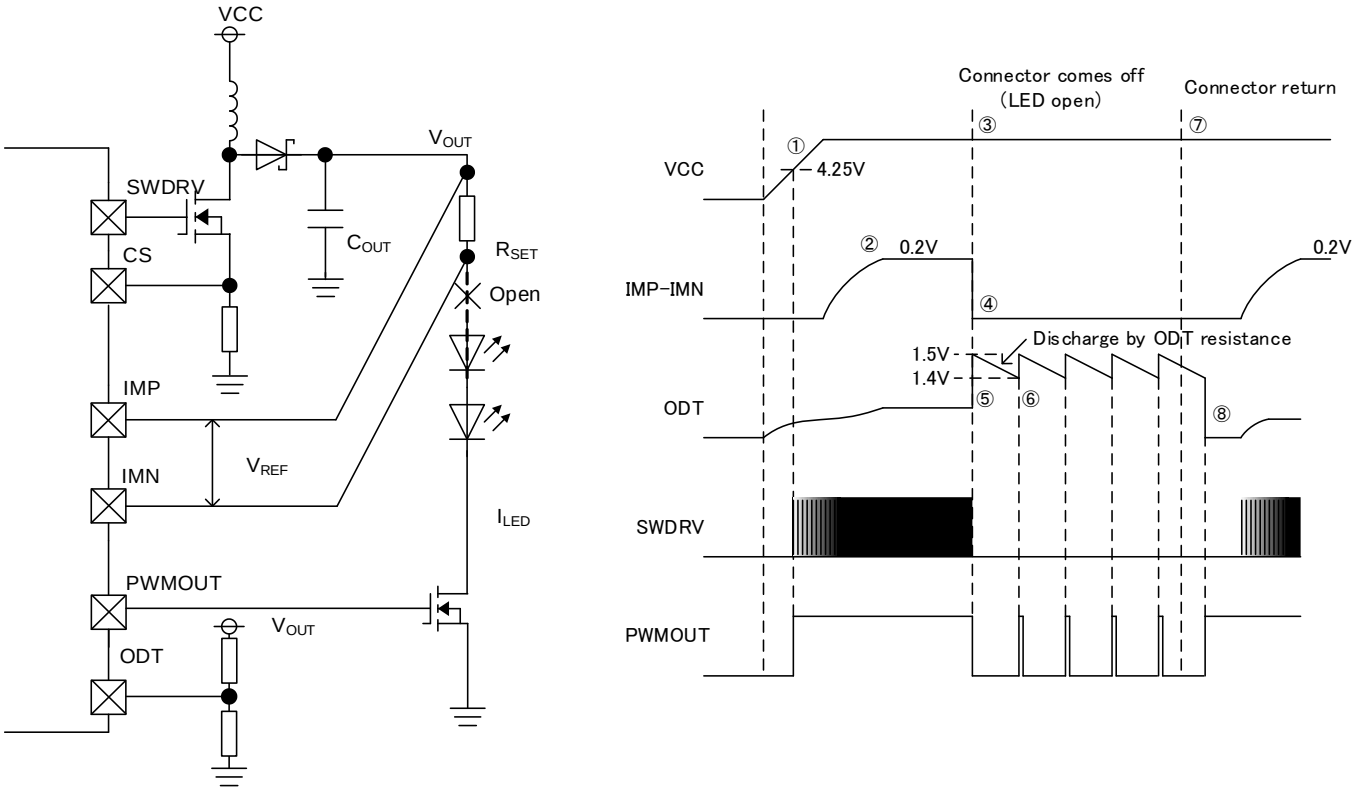


Figure 23. Output Ground Short Protection Operation Timing Chart

① UVLO is released when VCC > 4.25 V (Typ).
② IMP-IMN terminal voltage rises to become 200 mV.
③ Connector of LED opens.
④ Output voltage over boost due to IMP-IMN ≈ 0 V. (ODT which is resistor divided voltage of output voltage will steeply rise.)
⑤ When ODT ≥ 1.5 V, LED open is detected and SWDRV / PWMOUT becomes Low. Also, SS pin will be discharged and Fail pin becomes High → Low.
⑥ The LED open detection is released at ODT ≤ 1.4 V, and the FAIL terminal becomes Low → High.
Then DC / DC restarts the operation, however due to LED open condition voltage will be over boosted again.
⑦ LED is connected again.
⑧ When ODT ≤ 1.4 V, will be re-started and resumes to normal operation.
(During “8” condition if PWMOUT = High is applied while capacitors are still charged above nominal Vout, it could detect SCP detection due to IMP-IMN ≥ 0.3 V. After T_{TDISC} resumes to normal operation.)

5. Output electric charge electric discharge circuit (VOUTDISC)

When supply voltage of LSI is turned off in such configuration as shown in Figure 24, output capacitor may not be fully discharged and may remain charged in some cases. When power is supplied again while output capacitor is charged,transient current flows through the route of output capacitor→R_{SET}→LED→PWM dimming FET→GND which cause LED flashing. Later, when switching duty is output, LED is lit. In order to suppress such a flash phenomenon, this LSI incorporates output charge discharge circuit.

In order for output discharge circuit to operate, discharge of output capacitor starts when either one of the conditions of UVLO is detected (VCC ≤ 3.9 V) or V_{EN} ≤ 1.35 V are satisfied. (Output discharge circuit is also operated at LED open detection.)

Turn off PWM after EN turned off power supply OFF sequence when PWM input is controlled with an external signal.

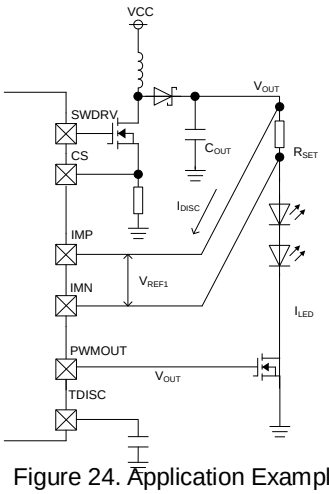
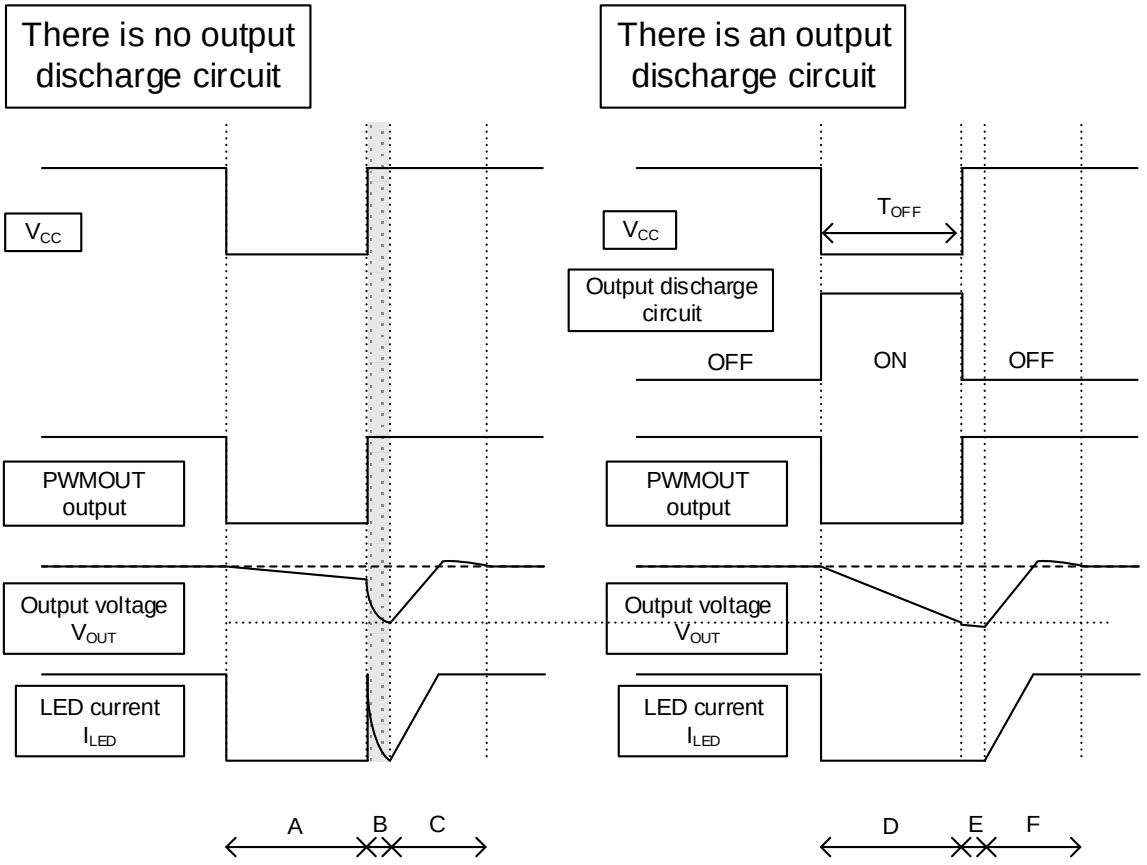


Figure 24. Application Example



A. Because V_{CC} is off, and the PWMOUT terminal is off, the LED current does not flow. Because PWMOUT terminal is OFF, output capacitor C_{OUT} is discharged by resistance connected to ODT terminal, and output voltage V_{OUT} gradually decreases.

B. When V_{CC} is turned on again, getting started of output voltage V_{OUT} is late by a soft start function. On the other hand, the PWMOUT terminal is turned on in sync with a reintroduction of V_{CC}. Therefore LED current flows from an output capacitor transiently, and LED shines for an instant, and LED darkens when the electric charge of the output capacitor is discharged besides.

C. Output voltage stands up, and LED turns on again.

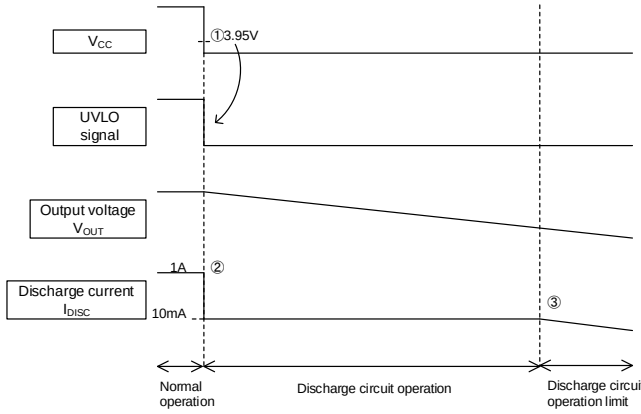
D. Because V_{CC} is off, and the PWMOUT terminal is off, the LED current does not flow. Because PWMOUT terminal is OFF, output capacitor COUT is discharged by resistance connected to ODT terminal. However, the output electric charge electric discharge circuit in the IMP terminal works, and output voltage V_{OUT} greatly decreases.

E. When V_{CC} is turned on again, getting started of output voltage V_{OUT} is late by a soft start function. On the other hand, the PWMOUT terminla is turned on in sync with a reintroduction of V_{CC}, but the LED does not shine because V_F cannot open.

F. Output voltage stands up, and LED turns on.

Figure 25. Output Discharge Circuit Operation Explanation at the time of the VCC Drop

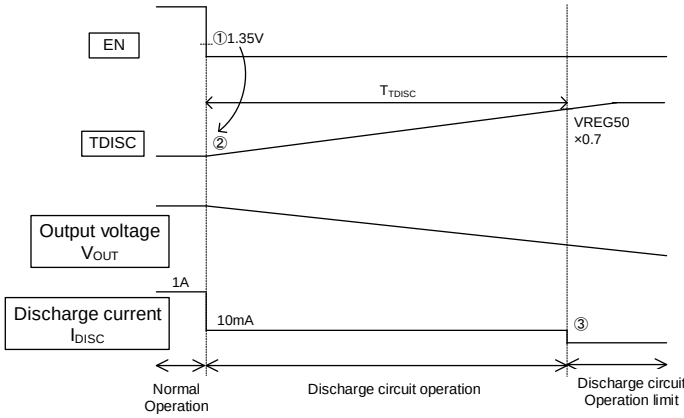
Concerning output discharge circuit operation at the time of UVLO detection



① UVLO is detected when VCC < 3.95 V.
② When UVLO is detected, discharge circuit is turned on to discharge charge accumulated in output capacitor, and output voltage falls by I_{DISC}.
③ I_{DISC} falls accompanying fall of output voltage.
(Refer to electric properties of output voltage V_{OUT} and discharge current I_{DISC}.)

Figure 26. Explanation of Output Discharge Circuit Operation at UVLO Detection

Concerning output discharge circuit operation by EN control



① When EN ≤ 1.35 V, EN is turned off.
② Output is discharged during output discharge time (T_{TDISC}) set by capacitor connected to TDISC.

$$T_{\mathrm{TDISC}} = \frac{VREG50 \times 0.7 \times C_{TDISC}}{11\mu A}$$

③ When discharge time T_{TDISC} elapsed, output discharge circuit stops operation.

Figure 27. Explanation of Output Discharge Circuit Operation when EN is off

The recommended capacitance value for this function is 0.01 μF to 0.47 μF, Please do not to connect TDISC to GND. Caution that even if the values are within recommended range, when output voltage is higher and C_{TISC} is higher heat dissipation by discharge is to be considered. Sufficient verification by actual application is required.
Flash phenomena is affected by Vf characteristic of LED and time to re-enter power supply. This is also to be sufficiently verified with actual application.

6. About EN terminal setting (EN CTL)

ON / OFF of the LSI can be controlled by applying resistor devided voltage from power supply to EN terminal. Setting of the EN terminal voltage to control ON / OFF of the LSI is as follows.

$$V_{CCON} = \frac{(R_{EN1} + R_{EN2})}{R_{EN2}} \times 1.45V(Typ)$$

$$V_{CCOFF} = \frac{(R_{EN1} + R_{EN2})}{R_{EN2}} \times 1.35V(Typ)$$

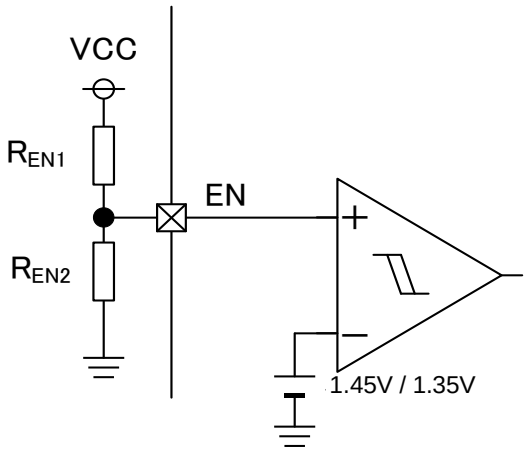


Figure 28. About EN terminal setting

Ex)
The VCC terminal voltage to stop / start operation is as follows with REN1 = 150 kΩ, REN2 = 51 kΩ condition

The operation start voltage

$$V_{CCON} = \frac{(150k\Omega + 51k\Omega)}{51k\Omega} \times 1.45V(Typ) = 5.71V$$

The operation stop voltage

$$V_{CCOFF} = \frac{(150k\Omega + 51k\Omega)}{51k\Omega} \times 1.35V(Typ) = 5.32V$$

For PWM dimming, do not control PWM with the EN terminal as it may result in unstable operation.
PWM dimming, is to be controlled with CR terminal. (Please refer to P.4 to 6 for the details.)

Absolute Maximum Ratings (Ta = 25 °C)

Parameter	Symbol	Rating	Unit
Power Voltage	V_{CC}	-0.3 to 70	V
EN, DRL Terminal Voltage	V_{EN}, V_{DRL}	-0.3 to VCC+0.3	V
IMP, IMN Terminal Voltage	V_{IMP}, V_{IMN}	-0.3 to 70	V
The Voltage between IMP and IMN	V_{IMP} - V_{IMN}	3	V
VREG50, CS, RS, RT, VREG25, DISC, ODT, PWMOUT, DCD, SS COMP, SWDRV, FAIL , TDISC terminal voltage	V_{VREG50}, V_{CS}, V_{RS}, V_{RT}, V_{VREG25} V_{CR}, V_{DISC}, V_{ODT}, V_{PWMOUT}, V_{DCD}, V_{SS}, V_{COMP}, V_{SWDRV}, V_{FAIL}, V_{TDISC}	-0.3 to 7 < VCC	V
Operation Temperature Range	Topr	-40 to 125	°C
Storage Temperature Range	Tstg	-55 to 150	°C
Junction Temperature	Tjmax	150	°C

Caution: Deterioration or break may occur when absolute maximum ratings of applied voltage, operation temperature range, etc. are exceeded. Also, breaking situation such as short circuit mode or open mode cannot be assumed. If special mode exceeding absolute maximum rating is assumed, please consider physical safety measures such as fuse.

Thermal Resistance *(Note 1)*

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s *(Note 3)*	2s2p *(Note 4)*	
HTSSOP-B24				
Junction to Ambient	θ_{JA}	143.8	26.4	°C/W
Junction to Top Characterization Parameter *(Note 2)*	Ψ_{JT}	7	2	°C/W

(Note 1) Based on JESD51-2A (Still-Air)
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via *(NOTE 5)*	
			Pitch	Diameter
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ0.30mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

(Note 5) This thermal via connects with the copper pattern of all layers.

Recommended Operating Ratings (Ta = 25 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Power Voltage *(Note 1)*	V_{CC}	4.5	12	65	V
Output Voltage *(Note 2)*	V_{IMP}	6.0	40	65	V
DC / DC Switching Frequency (With Spread Spectrum Control OFF)	F_{OSC1}	200	-	700	kHz
DC / DC Switching Frequency (With Spread Spectrum Control ON)	F_{OSC2}	200	-	600	kHz
CRTIMER Frequency	F_{PWM}	100	-	2000	Hz
CRTIMER Output Duty	F_{DUTY}	2	-	45	%
Spectrum Spread Frequency	F_{RS}	0.3	-	10	kHz

(Note 1) Apply voltage of no less than 5 V once at the time of stat-up. The value is voltage range after once setting at no less than 5 V.
(Note 2) When become the condition mentioned above except for startup at Boost application, it's possible that large current flow in LED.

Recommended External Constant Range

Parameter	Symbol	Min	Max	Unit
Capacitance for CRTIMER Frequency/Duty Setting *(Note 3)*	C_{CR}	0.01	1.0	μF
Resistance for CRTIMER Frequency/Duty Setting *(Note 3)*	R_{DISC2}	10	33	kΩ
Resistance for DC/DC Frequency	R_{RT}	14	51	kΩ
Capacitance for Soft-Start Setting *(Note 4)*	C_{SS}	0.01	1.0	μF
Capacitance for TDISC Setting *(Note 5)*	C_{TDISC}	0.01	0.47	μF
Resistance of OVP Setting of VOUT Side *(Note 3)*	R_{OVP1}	600	1000	kΩ

(Note 3) Since the above values are reference values, when using constants outside the range, please thoroughly check the PWM dimming characteristics.
(Note 4) Since the above values are reference values, when using constants outside the range, please thoroughly check the characteristics at startup (rush current etc.).
(Note 5) Since the above values are reference values, when using a capacitor outside the range, the hiccup time of SCP operation changes, so please fully check the heat generation of the external FET during SCP operation.

Electrical Characteristics (Unless otherwise specified V_{CC} = 13 V, V_{IMP} = 40 V, Ta = -40 °C to 125 °C)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
Circuit Current	I_{CC}	-	3	6	mA	C_{VREG} = 2.2 µF, V_{CS} = V_{ODT} = 0 V V_{EN} = V_{DRL} = V_{CR} = GND V_{RS} = V_{VREG50} V_{DCD} = V_{RT} = V_{VREG25}
[VREG]						
VREG50 Standard Voltage	V_{VREG50}	4.5	5.0	5.5	V	C_{VREG50} = 2.2 µF Load current = 0mA to 20 mA No switching
VREG25 Standard Voltage	V_{VREG25}	2.425	2.50	2.575	V	I_{VREG25} = 0µA
VREG25 Load Regulation Voltage	ΔV_{VREG25}	-	50	100	mV	I_{VREG25} = 0µA to 250 µA
[SWDRV]						
SWDRV Upper Side ON Resistance	R_{SWP}	-	4	8	Ω	I_{ON} = -10 mA
SWDRV Lower Side ON Resistance	R_{SWN}	-	3	6	Ω	I_{ON} = 10 mA
Overcurrent Protection Voltage	V_{OCP}	250	300	350	mV	V_{CS}: Sweep up
[LED Current Setting Block]						
LED Current Setting Standard Voltage	V_{REF1}	194	200	206	mV	Voltage between V_{IMP} - V_{IMN} terminals.
LED Ground Short Detection Voltage	V_{SCPON}	0.24	0.3	0.36	V	$V_{SCP} \geq V_{IMP} - V_{IMN}$
LED Open Detection Voltage	V_{OPEN}	1.42	1.5	1.575	V	V_{ODT}: Sweep up
LED Open Hysteresis Voltage	$V_{HYSOPEN}$	-	0.1	-	V	V_{ODT}: Sweep down
TDISC Charge Current	I_{TDISC}	4	11	18	µA	V_{TDISC} = 0V
TDISC Short Timer Detection Voltage	V_{DTDISC}	0.9	1.0	1.1	V	V_{TDISC}: Sweep up
TDISC Short Timer Release Voltage	V_{RTDISC}	0.2	0.3	0.4	V	V_{TDISC}: Sweep down
EN OFF TDISC Discharge Stop Voltage	V_{TDISC}	V_{VREG50} × 0.55	V_{VREG50} × 0.7	V_{VREG50} × 0.85	V	
Vout Discharge Time	T_{TDISC}	20	35	55	ms	C_{TDISC} = 0.1 µF
Output Charge Discharge Current	I_{DISC}	3	10	-	mA	V_{IMP} = 12 V
[CR TIMER]						
CR Threshold Voltage 1	V_{CRTH1}	V_{VREG50} × 0.18	V_{VREG50} × 0.20	V_{VREG50} × 0.22	V	
CR Threshold Voltage 2	V_{CRTH2}	V_{VREG50} × 0.36	V_{VREG50} × 0.40	V_{VREG50} × 0.44	V	
PWM Minimum Pulse Width	T_{PWM}	50	-	-	µs	
PWMOUT Upper Side ON Resistance	$R_{PWMOUTP}$	-	20	40	Ω	I_{ON} = -10 mA
PWMOUT Lower Side ON Resistance	$R_{PWMOUTN}$	-	5	10	Ω	I_{ON} = 10 mA

Electrical Characteristics (Unless otherwise specified V_{CC} = 13 V, V_{IMP} = 40 V, Ta = -40 °C to 125 °C)

Parameter	Symbol	Limit			Unit	Condition
		Min	Typ	Max		
[ERRAMP]						
COMP Source Current	I_{COMPSO}	-90	-60	-30	µA	V_{COMP} = 1.2 V, V_{DCD} = VREG25 V_{IMP} - V_{IMN} = 0 mV
COMP Sink Current	I_{COMPSI}	30	60	90	µA	V_{COMP} = 1.2 V, V_{DCD} = VREG25 V_{IMP} - V_{IMN} = 400 mV
[Soft start]						
Soft Start Charge Current	I_{SS}	3	5	7	µA	V_{SS} = 0 V
[Oscillator]						
DC / DC Switching Frequency	F_{OSC}	270	300	330	kHz	R_{RT} = 33 kΩ
Max Duty Output	D_{MAX}	-	95	-	%	R_{RT} = 33 kΩ
[RAMP]						
RS Frequency	F_{RS}	-	0.75	-	kHz	R_{RT} = 33 kΩ, C_{RS} = 0.047 µF
RS Terminal High Voltage	V_{RSH}	-	0.75	-	V	V_{RS}: Sweep up
RS Terminal Low Voltage	V_{RSL}	-	0.60	-	V	V_{RS}: Sweep down
[UVLO]						
UVLO Detection Voltage	V_{UVLO}	3.6	3.9	4.2	V	V_{CC}: Sweep down
UVLO Hysteresis Width	V_{UHYS}	250	350	450	mV	V_{CC}: Sweep up
[EN/DRL]						
EN Terminal ON Threshold Voltage	V_{ENON}	1.35	1.45	1.55	V	V_{EN}: Sweep up
EN Terminal Hysteresis Voltage Width	V_{HYSEN}	-	100	-	mV	V_{EN}: Sweep down
DRL Terminal Input Current	I_{DRL}	4	13	22	µA	V_{DRL} = 13 V
DRL Terminal ON Threshold Voltage	V_{DRLON}	3	-	-	V	V_{DRL}: Sweep up
DRL Terminal OFF Threshold Voltage	V_{DRLOFF}	-	-	0.8	V	V_{DRL}: Sweep down

Typical Performance Curves (Reference Data)

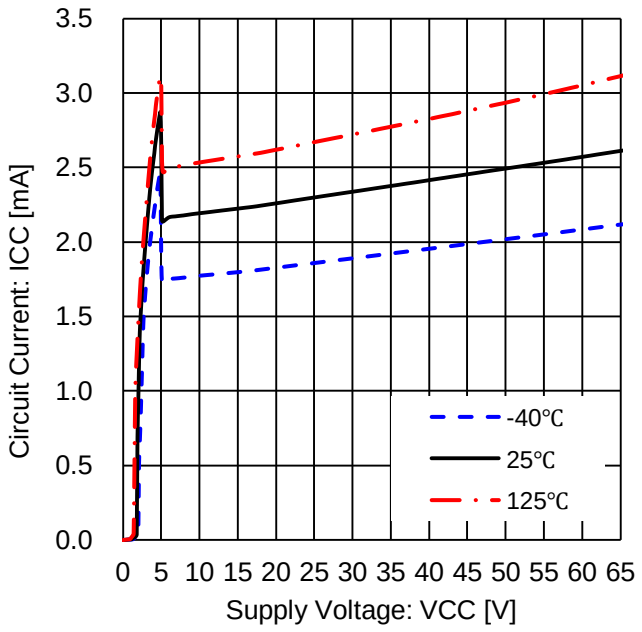


Figure 29. Circuit Current vs Supply Voltage

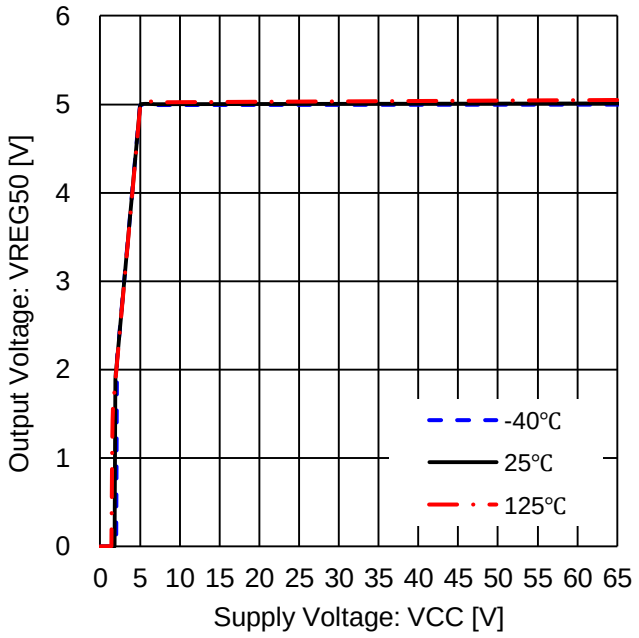


Figure 30. Output Voltage vs Supply Voltage (VREG50)

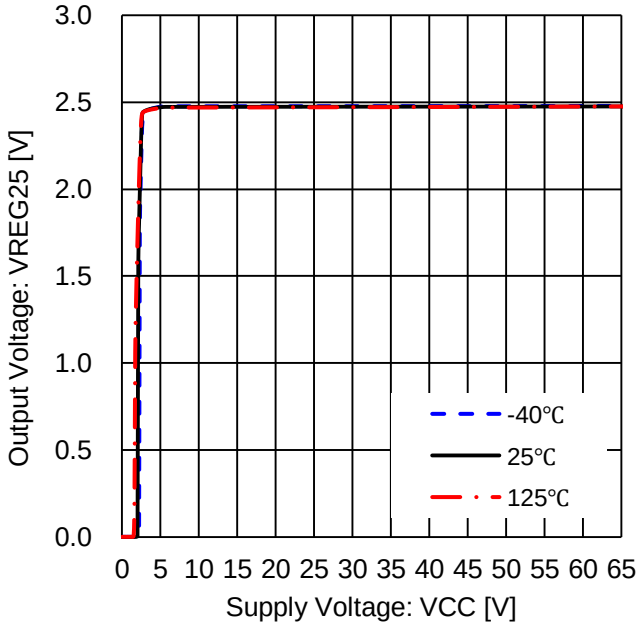


Figure 31. Output Voltage vs Supply Voltage (VREG25)

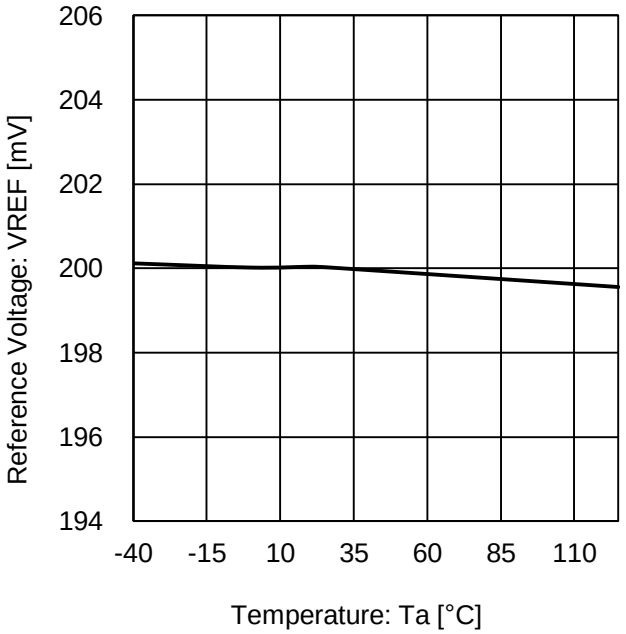


Figure 32. Reference voltage vs Temperature

Typical Performance Curves (Reference Data) - Continued

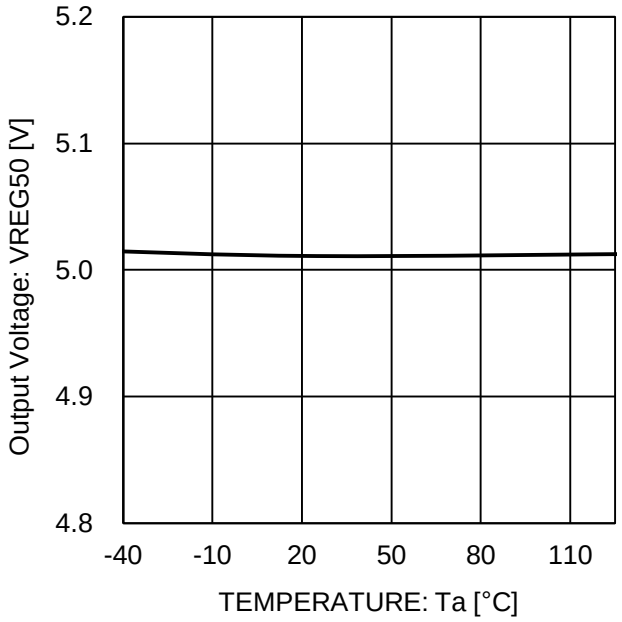


Figure 33. Output Voltage vs Temperature (VREG50)

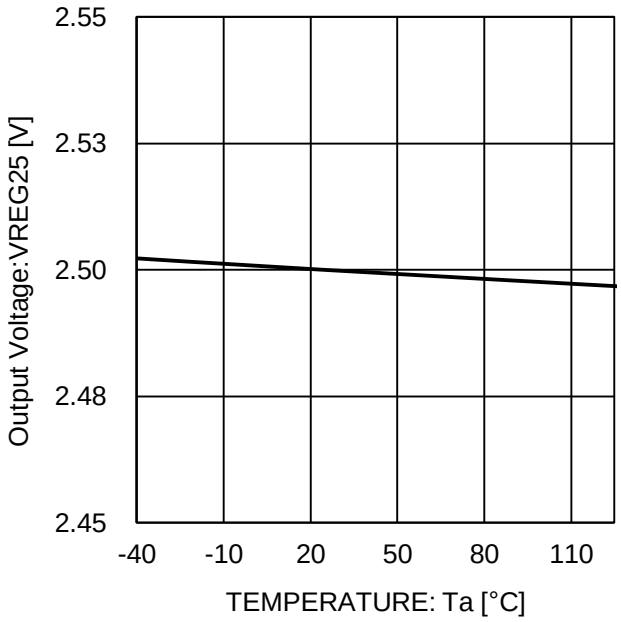


Figure 34. Output Voltage vs Temperature (VREG25)

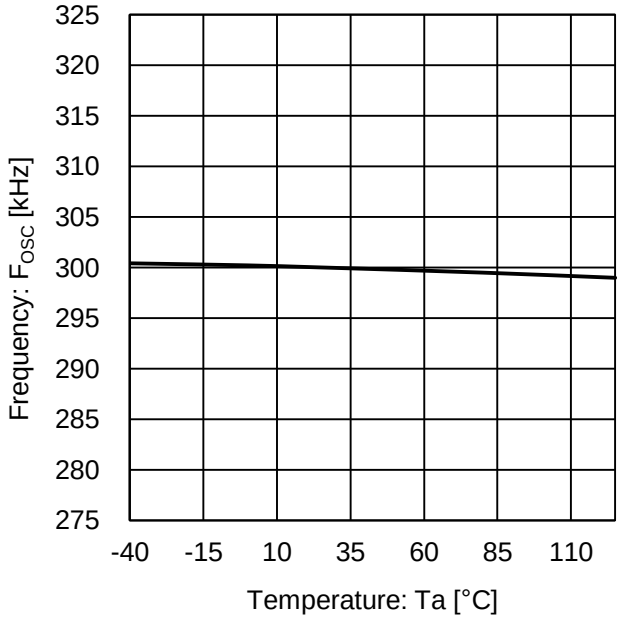


Figure 35. Frequency vs Temperature

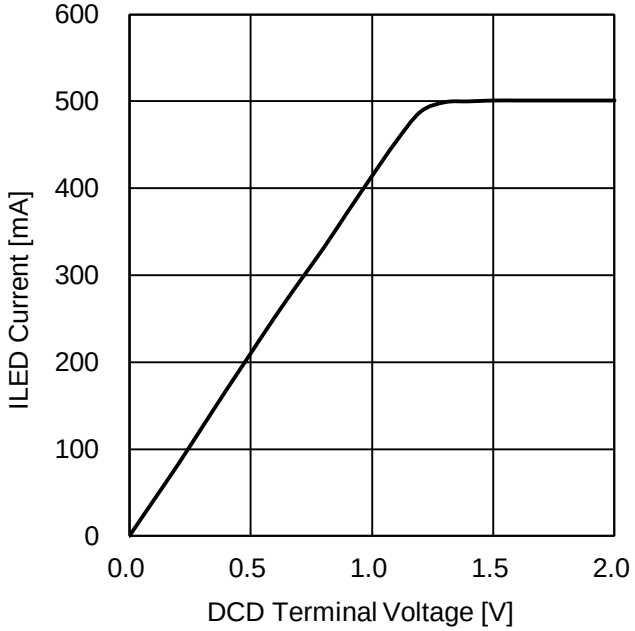


Figure 36. ILED Current vs DCD Terminal Voltage

Typical Performance Curves (Reference Data) - Continued

Figure 37. Spectrum Spread (ON)

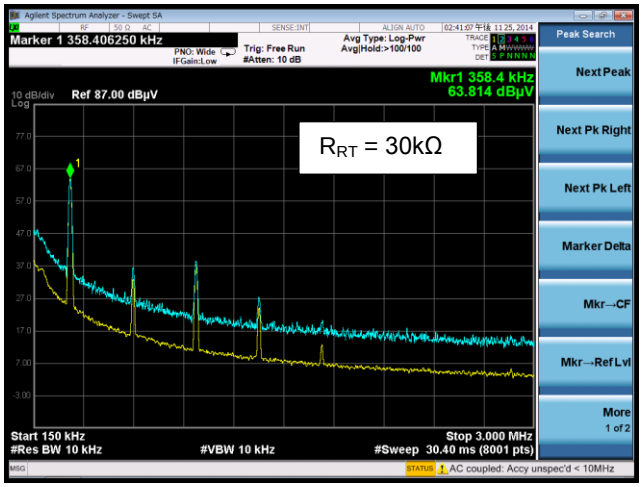


Figure 38. Spectrum Spread (OFF)
(RS = VREG50 Short)

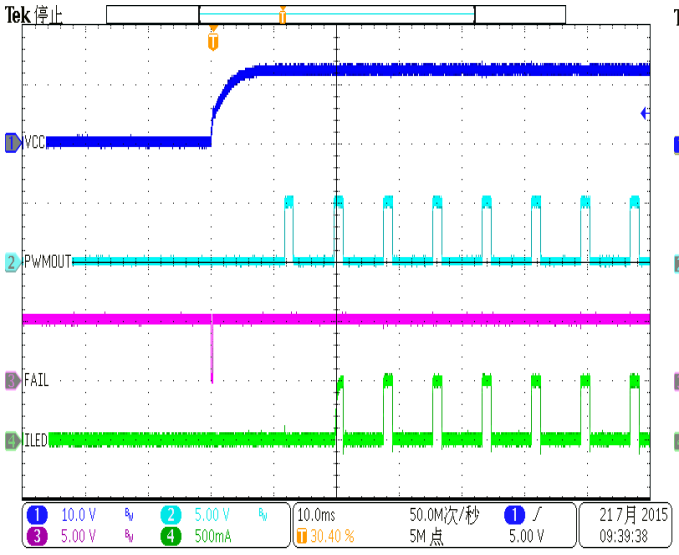


Figure 39. PWM Control Operation Start (DRL = Low)

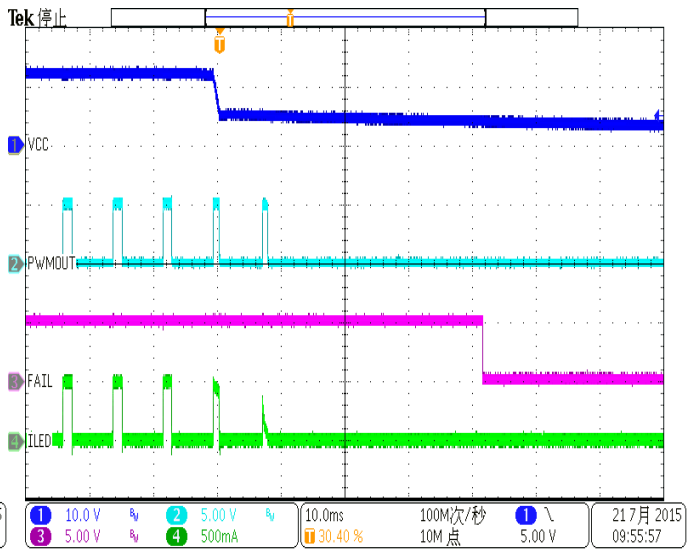


Figure 40. PWM Control Start (DRL = Low)

Typical Performance Curves (Reference Data) - Continued

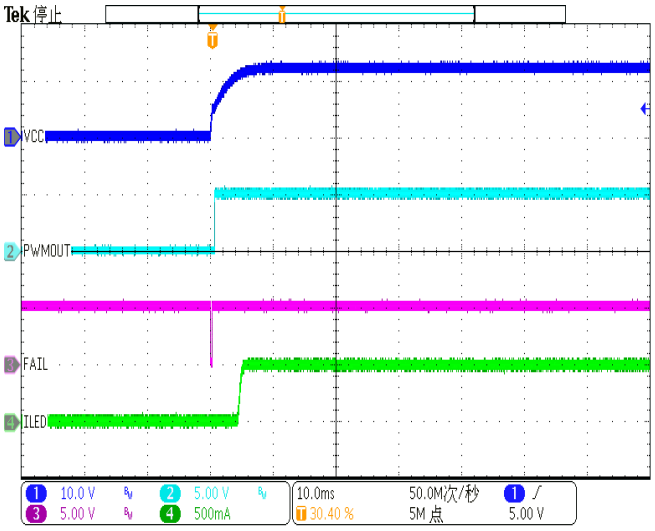


Figure 41. PWM Control Operation Start (DRL = High)

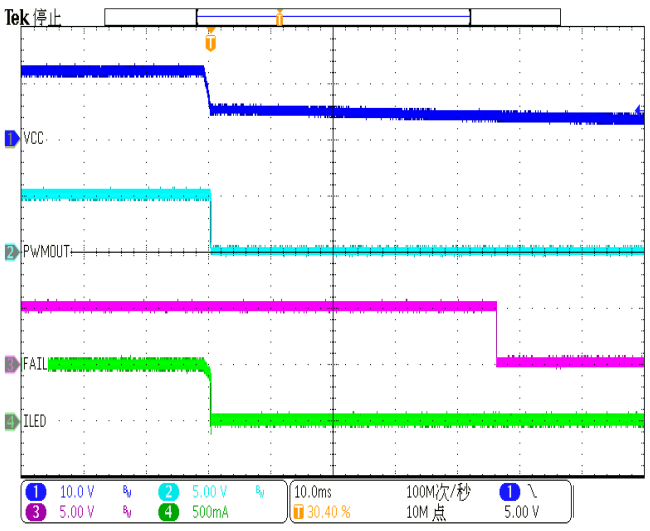


Figure 42. PWM Control Operation Stop (DRL = High)

Timing Chart 1

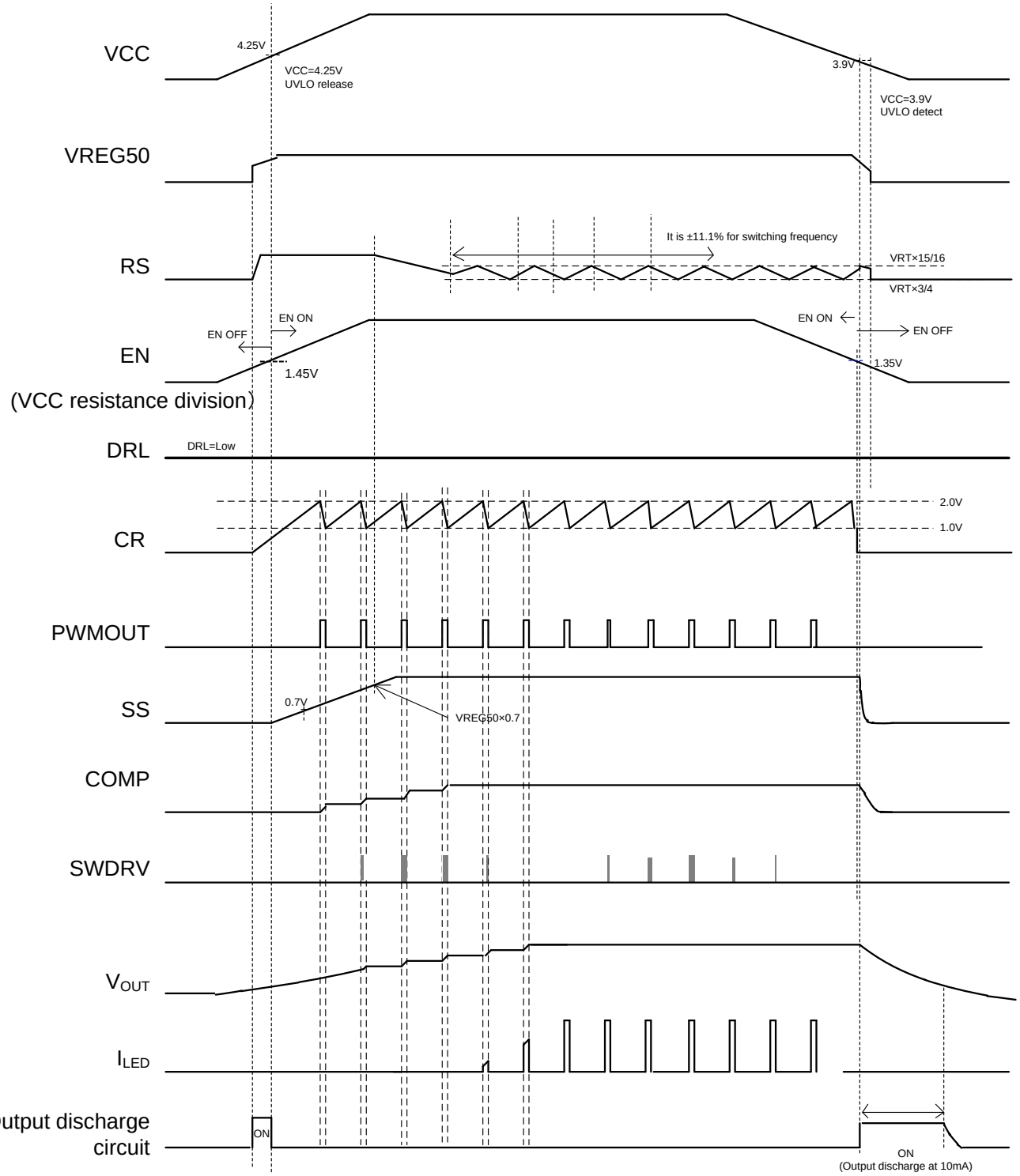


Figure 43. Start / Stop Sequence Timing chart (At time of PWM Control)

Timing Chart 2

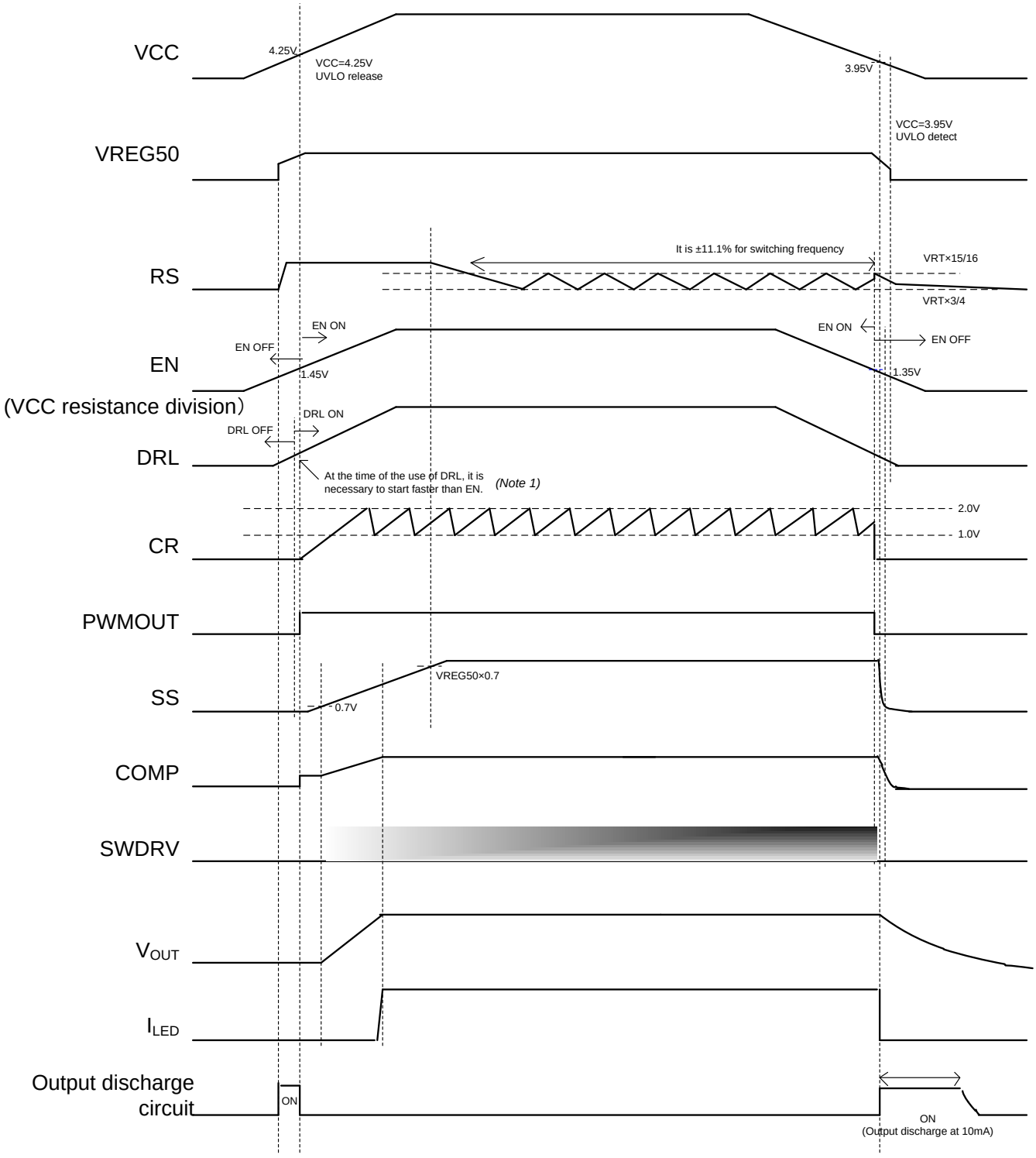


Figure 44. Start / Stop Sequence Timing chart (At time of PWM 100 % Control)

(Note 1) Please apply the logic fix possible voltage to the Hi side before EN by all means when DRL terminal is used on the High side (PWM 100 % state).

Application Examples

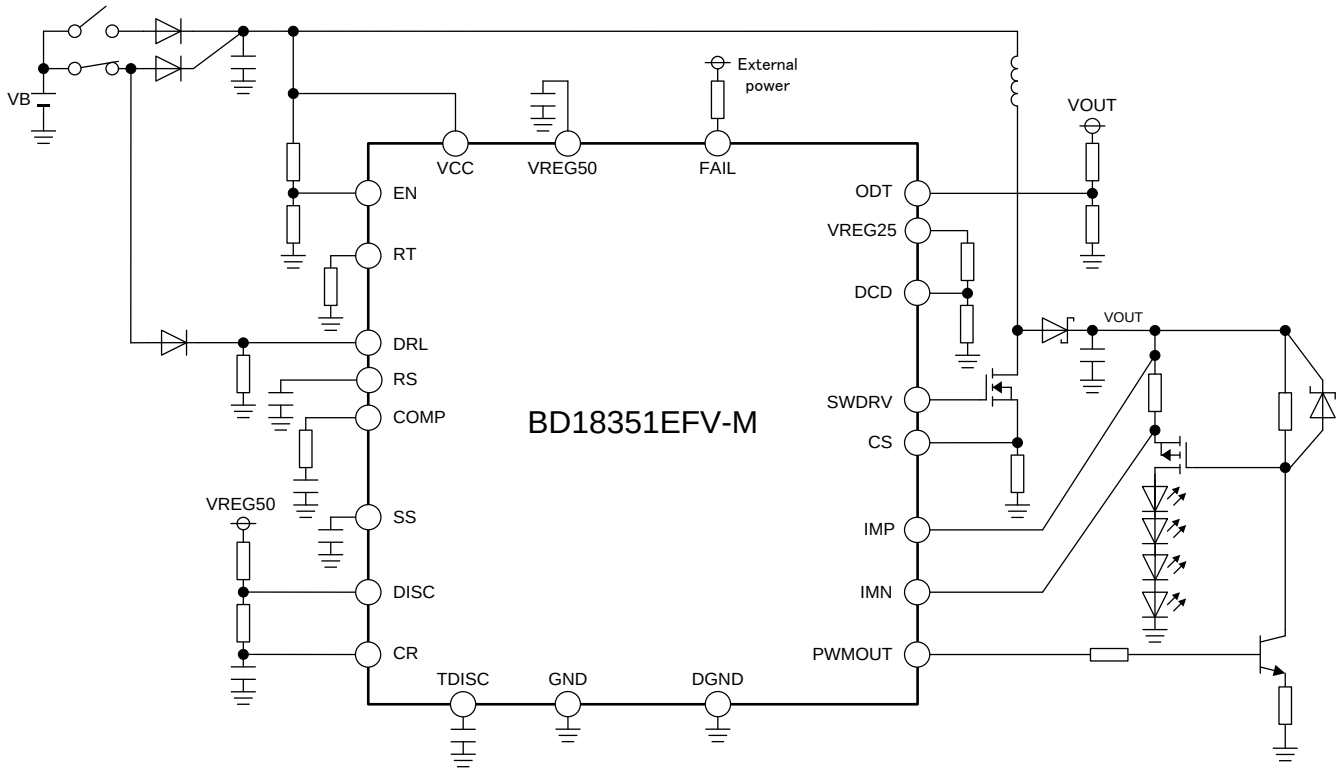


Figure 45. Boost Application (with PchMOS)

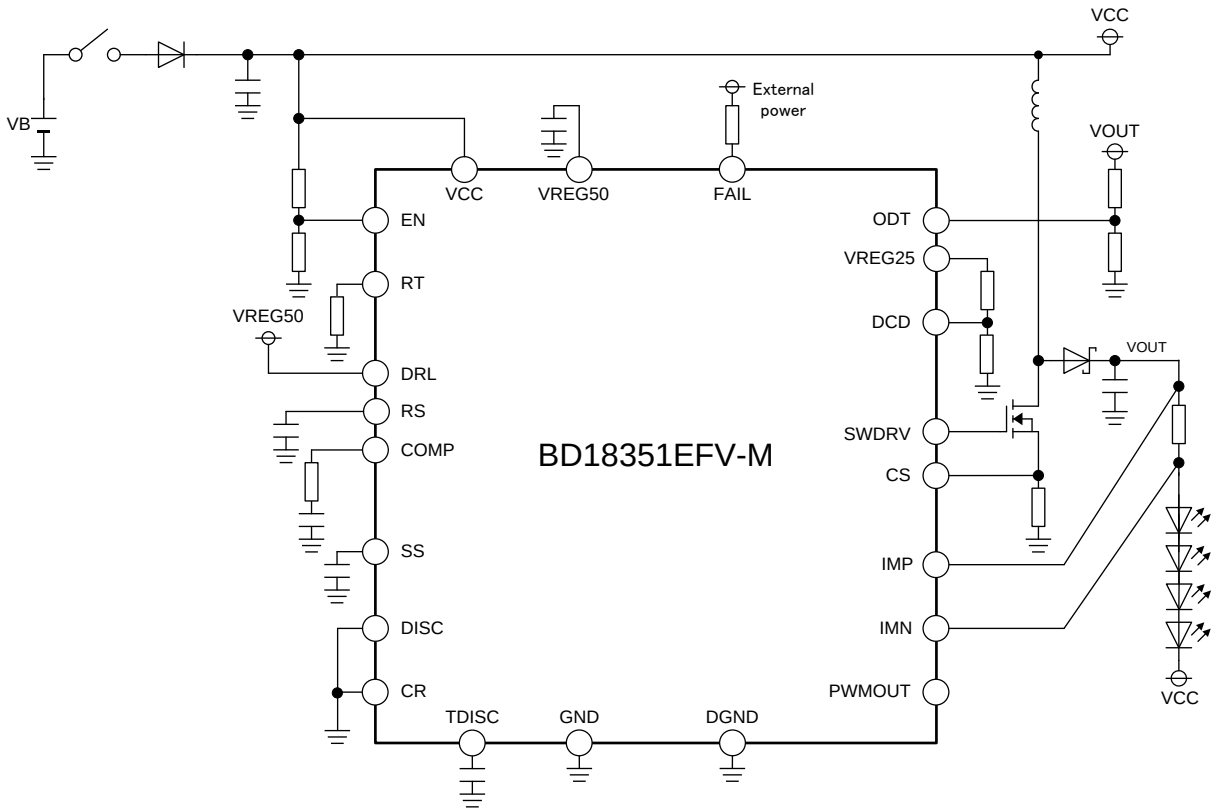
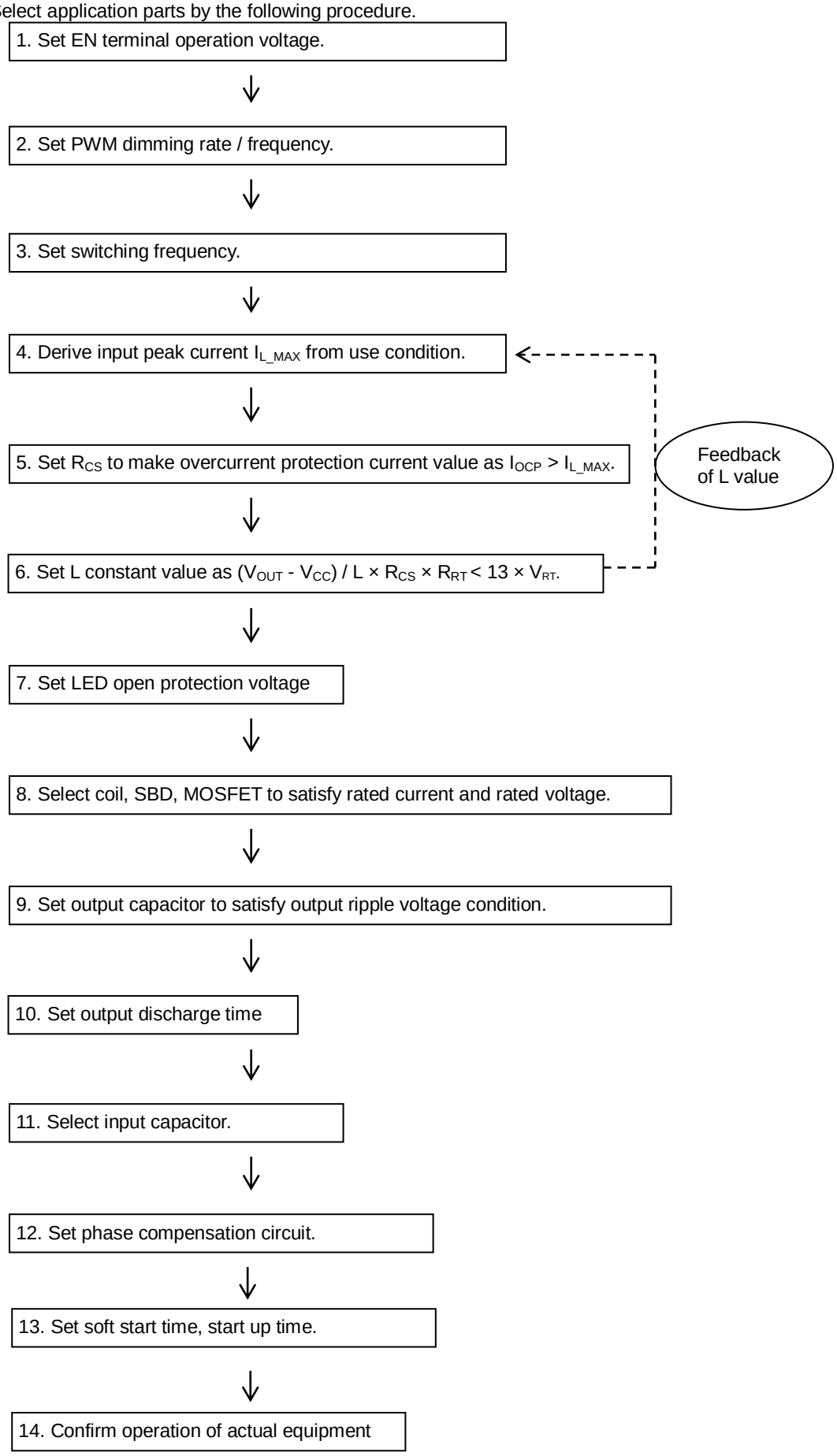


Figure 46. The application returning LED cathode to the power supply

Application Parts Selection Method (Boost mode Application)

Select application parts by the following procedure.



1. Setting of EN terminal operation voltage

This device can be turned ON / OFF by inputting resistor divided voltage to EN terminal.
EN terminal voltage to controls ON / OFF can be set as shown below.

$$V_{CCON} = \frac{(R_{EN1} + R_{EN2})}{R_{EN2}} \times 1.45V(Typ)$$

$$V_{CCOFF} = \frac{(R_{EN1} + R_{EN2})}{R_{EN2}} \times 1.35V(Typ)$$

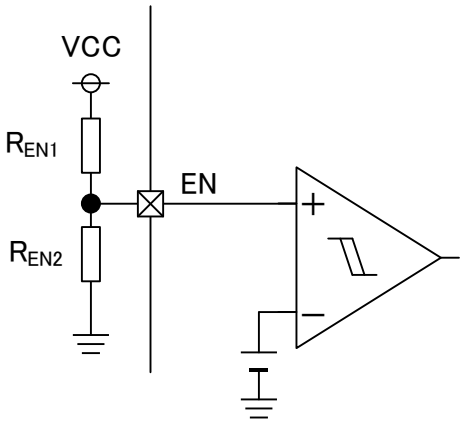


Figure 47. Concerning EN terminal Setting Method

2. Setting of PWM dimming rate / frequency

PWM dimming frequency (F_{PWM}) and PWM dimming ON Duty (D_{PWM}) can be set with resistance and capacitor by means of CR timer function which is built in this device. PWM dimming is 100 % dimming when DRL terminal voltage ≥ 3.0 V and is controlled by dimming rate set with external C and R in the other range. Also, In addition, the recommended operating frequency is 100 Hz to 2 kHz. The recommended external components values are; DISC2 to be between 10kΩ to 33 kΩ, C_{CR} to be between 0.01 µF to 1.0 µF.

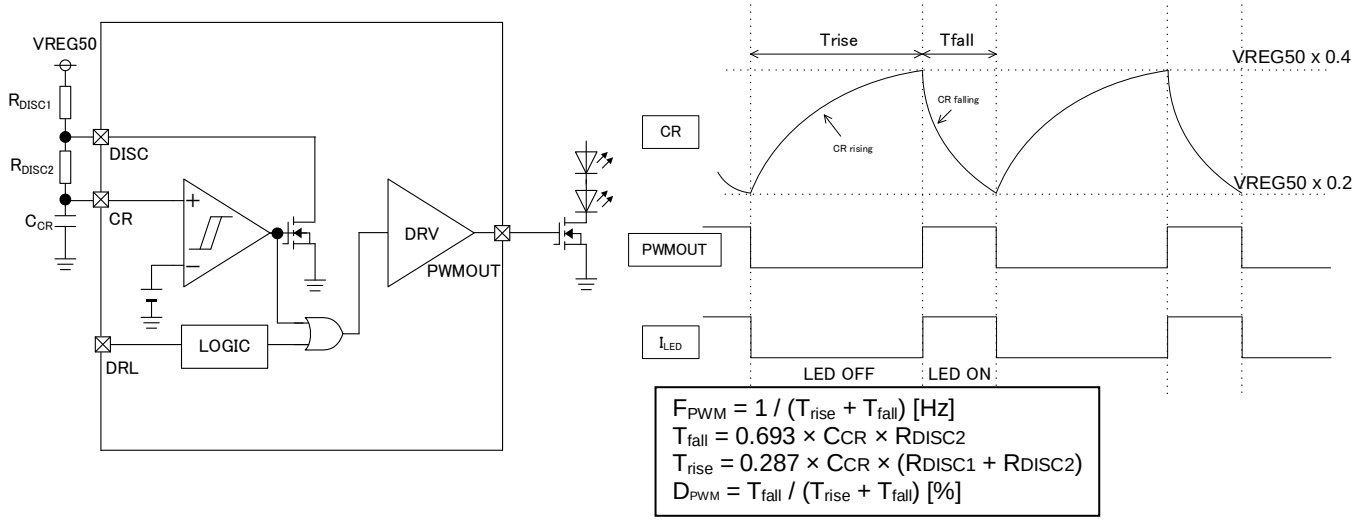


Figure 48. Concerning CR Timer Setting Method

3. Setting of switching frequency

A noise can be reduced using a spread spectrum function built-in the device. When spread spectrum is controlled, the switching does not work in frequency F_{OSC1} decided by RT resistance shown in P.9 Figure 12 and Frequency of F_{OSC1} × 0.84 as a center, it works at the frequency that modulated 11.1 %. The quantity of modulation frequency F_{RS} and noise decrement can be calculated from formula listed in P.10. (Because frequency is modulated at the time of the spread spectrum, it becomes maximum when frequency including the coil current is low. When each fixed number is calculated, please use it. (Please refer to P.10, 11 for the details.)) When a spread spectrum function is not used, please short-circuit with VREG50 terminal with RS terminal. Because the frequency setting changes, please be careful.

4. Derivation of input peak current IL_MAX (V_{DCD} > 1.21 V)

1. Calculation of output voltage (V_{OUT})

$$V_{OUT} = V_F \times N + V_{REF1}$$

V_F of LED for driving: V_F
LED current setting standard voltage: V_{REF1}
ON resistance of FET for PWM dimming: R_{ON_PWMFET}
LED current: I_{LED}
Resistance for LED current setting: R_{SET}
Maximum coil current: I_{L_MAX}
Coil mean current: I_{L_AVE}
Ripple current: ΔI_L
Power voltage: V_{CC}
Output voltage: V_{OUT}
Efficiency: η
DC / DC oscillation frequency: F_{OSC}

2. Calculation of output current I_{LED}

$$I_{LED} = \frac{V_{REF1}}{R_{SET}}$$

3. Calculation of input peak current I_{L_MAX}

$$I_{L\_MAX} = I_{L\_AVE} + \frac{1}{2}\Delta I_L$$

$$I_{L\_MIN} = I_{L\_AVE} - \frac{1}{2}\Delta I_L$$

$$I_{L\_AVE} = \frac{V_{OUT} \times I_{LED}}{\eta \times V_{CC}}$$

$$\Delta I_L = \frac{V_{CC}}{L} \times \frac{(V_{OUT} - V_{CC})}{V_{OUT}} \times \frac{1}{F_{OSC}}$$

- Since minimum input voltage is the worst case of $V_{CC,}$ assign minimum input voltage for calculation.
- BD18351EFV-M adopts current mode DC / DC converter control. When I_{L_Min} is positive, it becomes to be in the consecutive modes, and it will be in the discontinuity mode when I_{L_MIN} is negative. Phase characteristics are easy to become insufficient in the discontinuous mode, and responsiveness turns worse, and a switching wave pattern becomes irregular, and stability is easy to turn worse. Therefore it is sufficient validation of phase characteristics are recommended.
- η (efficiency) is about 90 %.
- In the case of V_{DCD} <1.21 V, please calculate I_{LED} using the formula which lists P.4 2(1) in "about a setting method of the LED current".

5. Setting of overcurrent protection current value

Select R_{CS} (resistance for overcurrent detection) to realize below.

$$I_{OCP\_MIN} = \frac{V_{OCP\_MIN}}{R_{CS}} > IL_{\_MAX}$$

Since values of coil L may vary about ±30 %, set with sufficient margin.

6. Selection of coil L constant value

For the purpose of stabilizing current mode DCDC converter operation, adjustment of L value within the following condition is recommended.

$$\frac{(V_{OUT} - V_{CC}) \times R_{CS} \times R_{RT} \times 10^{-3}}{L \times 10^{6}} < 13 \times V_{RT}$$

Reduction of calculated value will increase stability, but may reduce responsiveness such as power voltage variation. Bigger values which do not satisfy the above formula may cause sub-harmonic oscillation, destabilize switching duty and cause blinking of LED.
Further, assign V_{RT} = 0.8 V when RS terminal short-circuits with VREG and spread spectrum is not used, and assign V_{RT} = 0.675 V when capacitor is connected to RS terminal and spectrum is diffused.

7. Setting of LED open protection voltage

LED open detection voltage needs higher voltage setting than overshoot of output voltage at start up to avoid start up failure. Further, output voltage at the time of LED open detection (V_{OUT_ODT}) is calculable as shown below by setting R_{ODT1} and R_{ODT2}.

$$V_{OUT\_ODT} = \frac{(R_{ODT1} + R_{ODT2})}{R_{ODT2}} \times 1.5V(Typ)$$

ODT resistor will be the current discharge path for the output capacitor when PWM = Low Recommended value for R_{ODT1} is 600 kΩ to 1000 kΩ as Vout ripple may be large and cause LED flickering when PWM = Low with inadequate ohmic value range.
Sufficient verification for LED flickering is required with actual application as behavior differs by characteristic of output capacitor and LED.
(Vout drop can be prevented by inserting bigger output capacitor or ODT resistance.)

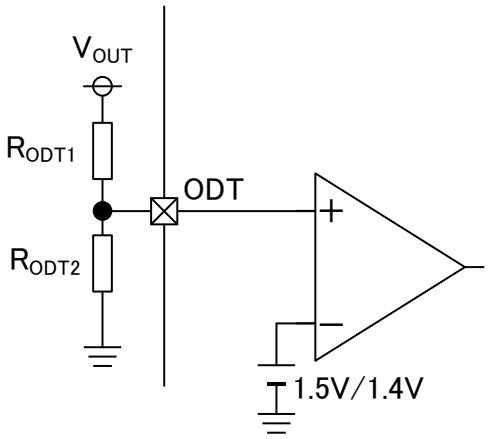


Figure 49. ODT terminal Equivalent Circuit

8. Selection of power element, diode D1, MOSFET Q1 and Q2

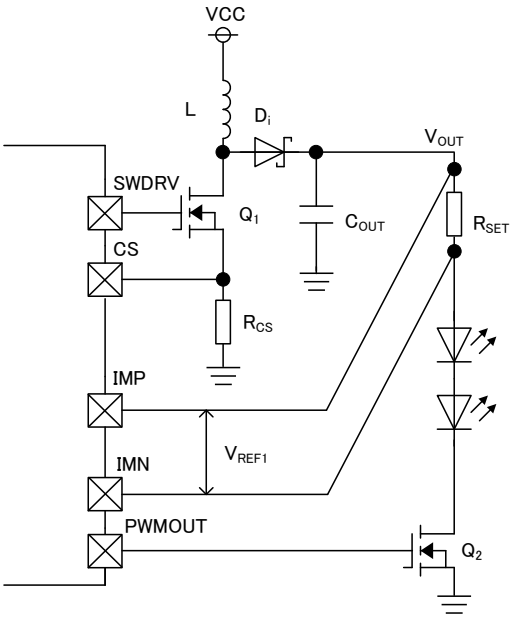


Figure 50. Boost Application Circuit

Selection of MOSFET Q1

Select MOSFET (Q1) to have V_{DS} rating higher than the Max output voltage which LED open function is activated.

$$V_{OUT\_ODT\_MAX} > \frac{(R_{ODT1}+R_{ODT2})}{R_{ODT2}} \times 1.575V(Max)$$

V_{DS}: Voltage between drain and source

In addition, the RMS current limit flowing between drain - sources of Q1 can be calculated as follows.

$$I_{DS\_RMS} = 1.3 \times \sqrt{(IL_{\_AVE})\text{^}2 \times D_{SW}}$$

D_{SW}: Switching Duty

A loss of Q1 is calculated next. The loss of Q1 will be the Ploss2 which is switching loss and Ploss1 the On resistance of Q1. Switching loss Ploss1 and Q1 On resistance loss Ploss2 can be calculated as follows.

$$P_{loss1} = \frac{(T_r+T_f)}{2} \times F_{OSC} \times (V_{OUT} + V_{Di}) \times I_{L\_AVE}$$

$$P_{loss2} = {I_{L\_AVE}}^2 \times R_{on} \times D_{SW}$$

Tr / Tf: Drain source rise / fall time
Ron: Ron of Q1

Selection of rectifier diode Di

For power consumption reduction, please use a Schottky Barrier diode for rectification diode Di. The withstand voltage rating of the diode shall be higher than the LED Open protection voltage. In addition, Schottky Barrier diode with low leakage current shall be selected if PWM dimming is used. Because the leakage current increases with higher temperature environment, the output capacitor can be discharged in PWM = Low which may result that LED current will be unstable. The current limit of Di can be calculated in following formula.

$$I_{Di} = I_{L\_AVE} \times (1 - D_{SW}) \times 1.5$$

Selection of MOSFET Q2

Consider margin and set the rated voltage rather higher than the actual usage condition for LED current and output voltage.

9. Selection of output capacitor C_{OUT}

Output capacity includes two purposes. The first is to reduce output ripple. The second is to supply current to LED when MOSFET (Q1) is switched on. The output voltage ripple is influenced by both bulk capacity and ESR. (When a ceramic capacitor is used, bulk capacity causes most of the ripple.) Bulk capacity and the ESR can be calculated in lower formula.

$$C_{OUT} \geq I_{LED} \times \frac{Dsw}{\Delta V_{COUT} \times F_{OSC}}$$

ΔV_{COUT}: influence with the capacitor among output ripple
ΔV_{ESR}: Ripple which occurs in the ESR of the output capacitor

$$R_{ESR} < \frac{\Delta V_{ESR}}{I_{L\_MAX}}$$

The total output ripple permitted here can be expressed as product of LED current ripple and the equivalent resistance of the LED. This equivalent resistance is defined as "ΔV / ΔI of the LED current", and it is necessary to calculate from I-V properties in the data sheet of the selected LED. Assuming that number of the driven LED = 8 pcs (equivalent resistance 0.2 Ω / LED), LED current = 1 A (IL_MAX = 4.5 A), switching Duty = 60 %, switching frequency = 300 kHz, it is supposed that LED current ripple is 5%.Then the total output ripple can be calculated as follows.

$$V_{OUT\_ripple} = 1A \times 5\% \times (0.2\Omega \times 8) = 80mV$$

If bulk capacity causes 95 % among total output ripple, the output capacitor is calculated as follows.

$$C_{OUT} \geq 1 \times \frac{0.6}{0.08 \times 0.95} \times \frac{1}{300kHz} = 26.4\mu F$$

$$R_{ESR} < \frac{V_{OUT\_ripple}}{IL_{\_MAX}} = \frac{(0.08 \times 0.05)}{4.5} = 0.88m\Omega$$

However the capacitance of output capacitor mentioned above is minimum capacitance. Therefore please select components considering the tolerance of the capacitor and DC bias properties. Furthermore, because small external component connected to output may lead to bigger ripple on output voltage, which may result in LED flickering, sufficient verification of the actual application is required. Increase output capacitors if judged to be required from the verification. In addition, an acoustic noise may be produced by the piezoelectric effect of the ceramic capacitor during PWM dimming. Electrolytic capacitor used together with a ceramic capacitor may reduce this noise. But capacitance may largely decrease with a change of the voltage with the ceramic capacitor and may not accord with the numerical value calculated from theory. Thorough consideration is required.

10. Setting of TDISC terminal

Output discharge time and Output short protection time can be set by connecting capacitor to TDISC terminal. Recommended range of capacitor will be 0.01 μF to 0.47 μF, however if capacitor at TDISC (C_{TDISC}) is smaller, output discharge time will be short which may result in LED flashing when restarting the supply voltage. On the other hand if C_{TDISC} is large discharge time will be longer. If Vout is high and discharge time is longer, heat generation of LSI will be larger therefore verification with actual application is required with caution.

11. Selection of input capacitor

In DC / DC converter, since peak current flows between input and output, a capacitor is also required in the input side. Therefore, low ESR capacitors with capacitor of no less than 10 μF and ESR component of no more than 100 mΩ are recommended as input capacitors. Selection of capacitors out of the range may cause malfunction of IC because excessive ripple voltage will overlap input voltage.

12. Setting of phase compensation circuit

●Concerning stability condition of application
Stability condition for system with negative feedback is as shown below.
Phase-lag when gain is 1 (0 dB) is no more than 150 ° (namely, phase margin is no less than 30 °).
Further, since DC / DC converter application is sampled by switching frequency, GBW of the entire system is set to be no more than 1 / 10 of switching frequency. To wrap up, target characteristics of application are as shown below.
●Phase-lag when gain is 1 (0 dB) is no more than 150 ° (namely, phase margin is no less than 30 °)
●GBW at the time (namely, frequency when gain is 0 dB) is no more than 1/10 of switching frequency. Therefore, in order to raise responsiveness by limiting GBW, higher switching frequency is required.

The knack for securing stability by phase compensation is to insert phase-lead F_{Z1} near GBW. GBW is determined by C_{OUT} and phase-lag fp1 due to output impedance RL (= V_{OUT} / I_{LED}).
They are shown in the following formulae.

Phase-lead

$$F_{Z1} = \frac{1}{2\pi \times C_{PC} \times R_{PC}}$$

Phase-lag

$$F_P = \frac{1}{2\pi \times R_L \times C_{OUT}}$$

$$R_L = \frac{V_{OUT}}{I_{LED}}$$

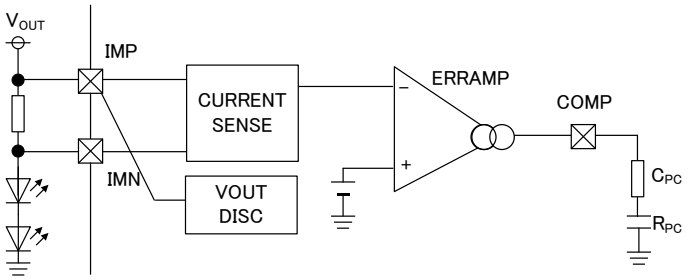


Figure 51. ERRAMP Equivalent Circuit

As described above, please secure phase margin. For R_L value at max load should be inserted. In addition, with boost DC/DC, right half plane zero (RHP zero) is to be considered. This zero has a characteristic of zero as a gain and as the pole with phase. Because it causes an oscillation when this zero effects on a control loop, it is necessary to bring GBW just before RHP zero. RHP zero can be calculated with an equation below and shows good characteristic by setting GBW to be lower than 1 / 10 of RHP zero.

$$F_{Z2} = \frac{R_L \times (\frac{V_{CC}}{V_{OUT}})^2}{2\pi \times L}$$

Particularly when supply voltage rises and gets close to output voltage, the switching output becomes irregular and ripple of the output voltage increases. Ripple of the LED current may thereby get bigger.

Since this setting is obtained by simplified, not strict, calculation, adjustment by actual equipment may be required in some cases.
Further, since these characteristics will vary depending upon substrate layout, load condition, etc., confirm satisfactorily with actual equipment when planning mass production.

13. Soft start time and confirmation of the boot-time

A soft start function is incorporated, and an inrush current can be prevented by inserting an external capacitor. Charge current of the soft start is 5 μA (Typ) and charges it without depending on PWM. The inrush current can be suppressed by increasing soft start capacity, but boot-time becomes longer. On the other hand, as for the boot-time, it becomes faster by lowering soft start capacity, but an inrush current grows bigger and it leads to the sound rumble of the coil in the startup, therefore attention is necessary. 0.01 μF to 1 μF is recommended to control overshoot of the LED current in the startup.
In addition, the boot-time varies according to PWM dimming control condition. Refer to details described in P11 and 12.

14. Confirmation of actual equipment operation

Select external components based on verification with actual equipment since characteristics will vary depending on various factors such as load current, input voltage, output voltage, inductor value, load capacity, switching frequency and mounting pattern.

PCB Application Circuit diagram

VCC = 9 V to 16 V, LED drive stage number: 7 (V_{OUT} ≈ 23 V), LED current: 500 mA, DC / DC oscillation frequency: 280 kHz, SSCG mode ON

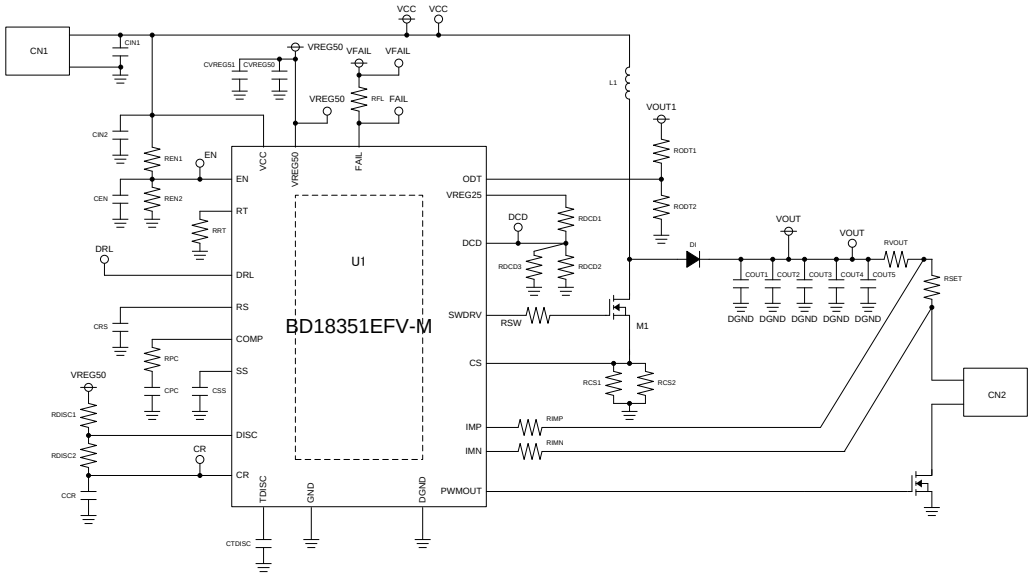
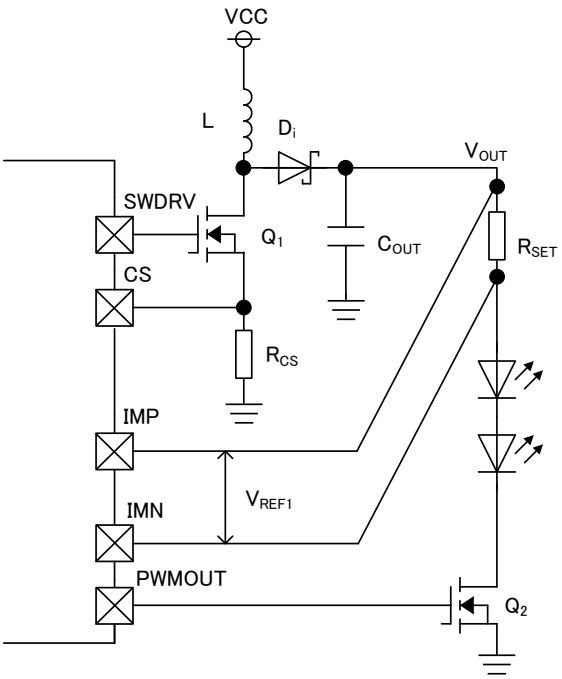


Figure 52. Boost application (PWM Dimming Application)

About the attention point at the time of the PCB layout



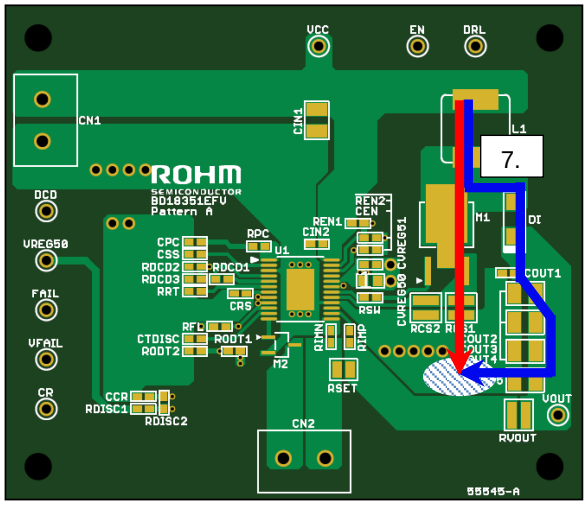


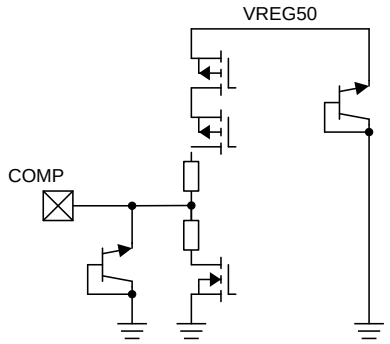
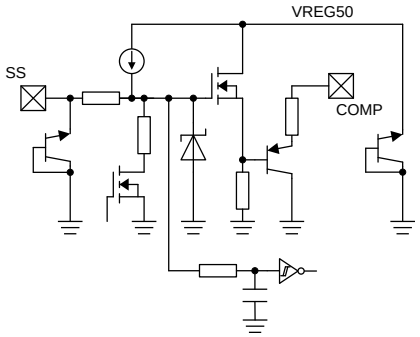
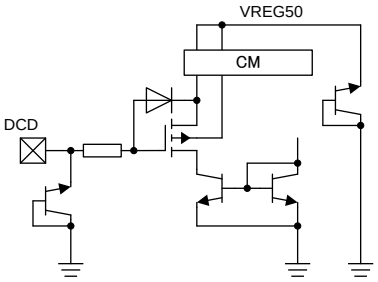
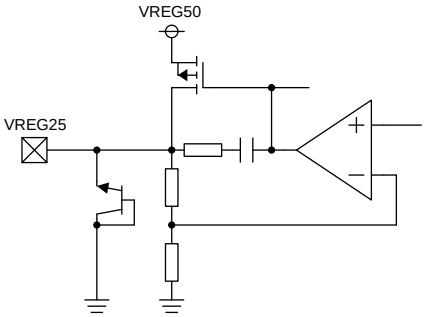
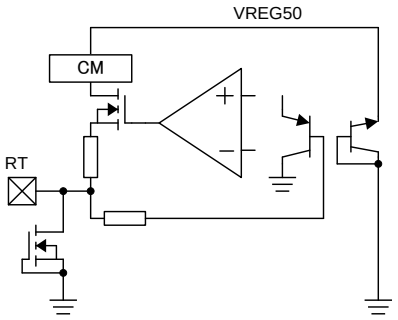
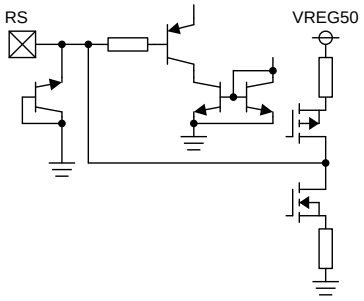
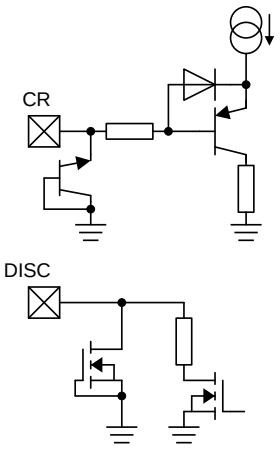
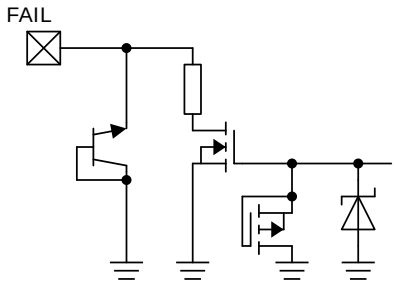
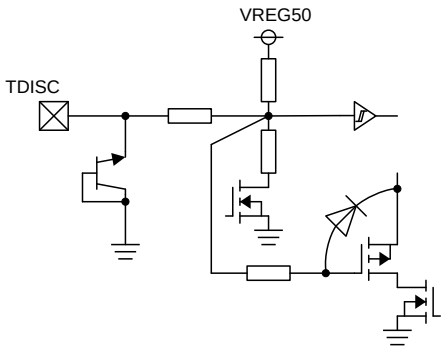
Figure 53. Boost High Side PWM Dimming Application

1. Please locate the decoupling capacitor of C_{IN2}, C_{VREG50}, C_{VREG51} close to an LSI pin as much as possible
2. R_{RT} locates it close to RT pin, and prevent there from being capacity
3. Because high current may flow in DGND, please lower impedance.
4. Prevent noise to be applied to EN, DRL, COMP, SS, RT, DCD, IMP, and IMN terminals.
5. As the CR, DISC, RS, SWDRV, PWMOUT terminals are switching, please be careful not to affect the neighboring patterns.
6. There is heat dissipation PAD on the back side of the package.
7. For noise reduction, DGND of R_{CS1}, R_{CS2} and DGND of C_{OUT} recommend to have one common grounds. In addition, consider the PCB layout so that the current path of M1 → R_{CS1}, R_{CS2} → DGND and the current path of Di → C_{OUT} → DGND are the shortest and with the lowest impedance.

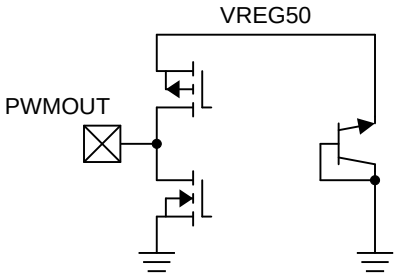
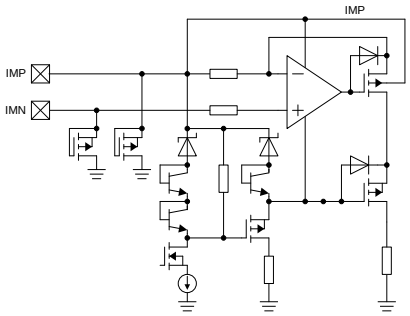
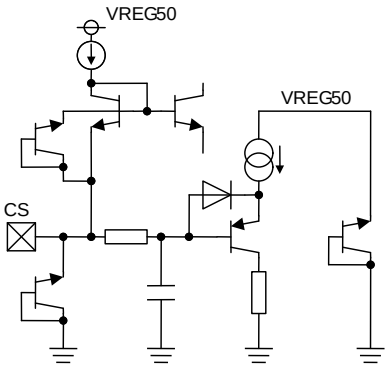
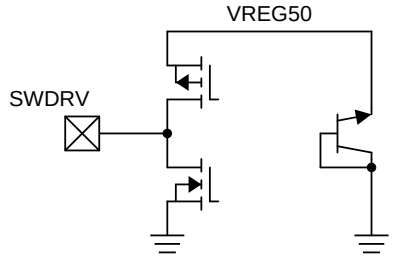
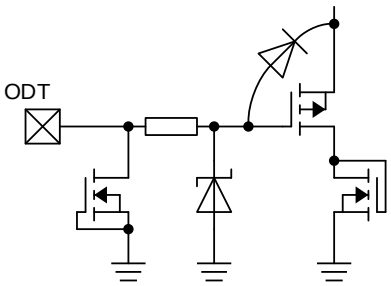
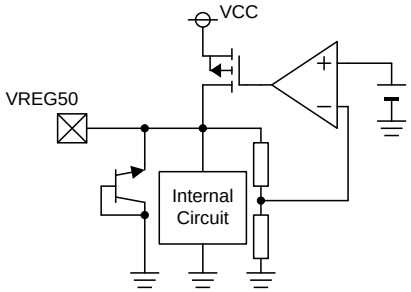
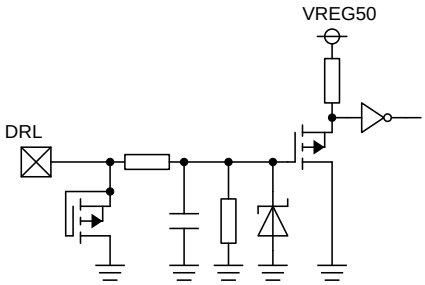
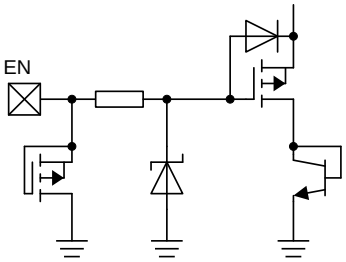
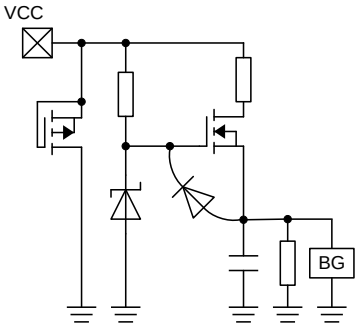
List of PCB board attaching externally parts

Bom_No	Value	Parts No	Product Maker
CIN1	10µF	GCM32EC71H106KA01	Murata
CIN2	0.1µF	GCM188R11H104KA01	Murata
CVREG50	2.2µF	GCM21BR71C225KA49	Murata
CVREG51	1000pF	GCM155R11H102KA01	Murata
REN1	100kΩ	MCR03	Rohm
REN2	39kΩ	MCR03	Rohm
CEN	1000pF	GCM155R11H102KA01	Murata
RRT	30kΩ	MCR03	Rohm
CRS	0.047µF	GCM188R11H473KA01	Murata
RPC	5.1kΩ	MCR03	Rohm
CPC	0.047µF	GCM188R11H473KA01	Murata
RDISC1	100kΩ	MCR03	Rohm
RDISC2	20kΩ	MCR03	Rohm
CCR	0.1µF	GCM188R11H104KA01	Murata
CSS	0.1µF	GCM188R11H104KA01	Murata
CTDISC	0.1µF	GCM188R11H104KA01	Murata
RFL	100kΩ	MCR03	Rohm
L1	10µH	IHLP-3232DZ-11	Vishay
RODT1	680kΩ	MCR03	Rohm
RODT2	33kΩ	MCR03	Rohm
RDCD1	12kΩ	MCR03	Rohm
RDCD2	100kΩ	MCR03	Rohm
RDCD3	100kΩ	NTCG104EF104F	TDK
M1	-	RSD150N06FRA	Rohm
RSW	22Ω	MCR03	Rohm
RCS1	150mΩ	LTR18	Rohm
RCS2	150mΩ	LTR18	Rohm
Di	-	RB058L150	Rohm
RIMP	0Ω	MCR03	Rohm
RIMN	0Ω	MCR03	Rohm
COUT1	0.1µF	GCM188R11H104KA01	Murata
COUT2	10µF	GCM32EC71H106KA01	Murata
COUT3	10µF	GCM32EC71H106KA01	Murata
COUT4	10µF	GCM32EC71H106KA01	Murata
COUT5	10µF	GCM32EC71H106KA01	Murata
RVOUT	0Ω	LTR18	Rohm
RSET	680mΩ	LTR10	Rohm
M2	-	RTR020N05	Rohm
IC	-	BD18351EFV-M	Rohm

I/O Equivalent Circuits

1. COMP	2. SS	4. DCD
		
5. VREG25	**6. RT**	**7. RS**
		
8. CR, 9. DISC	**10. FAIL**	**11. TDISC**
		

I/O Equivalent Circuits - Continued

12. PWMOUT	13. IMN, 14. IMP	17. CS
		
18. SWDRV	**19. ODT**	**20. VREG50**
		
22. DRL	**23. EN**	**24. VCC**
		

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

Operational Notes – continued

11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

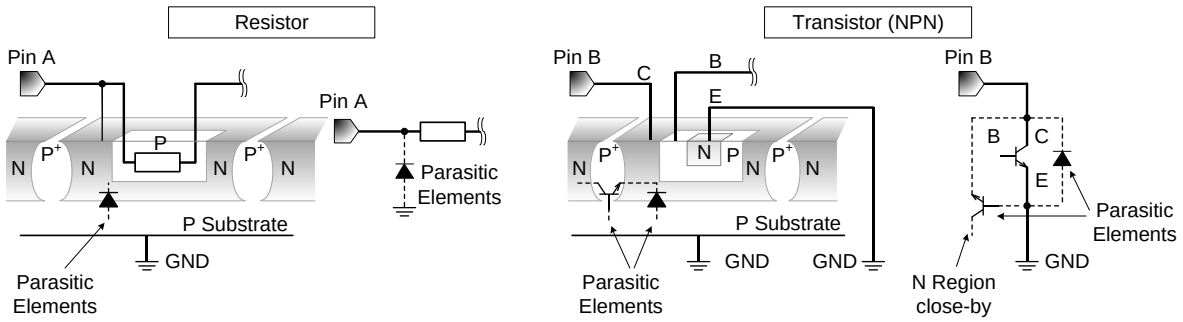


Figure 54. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and power dissipation are all within the Area of Safe Operation (ASO).

15. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

16. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

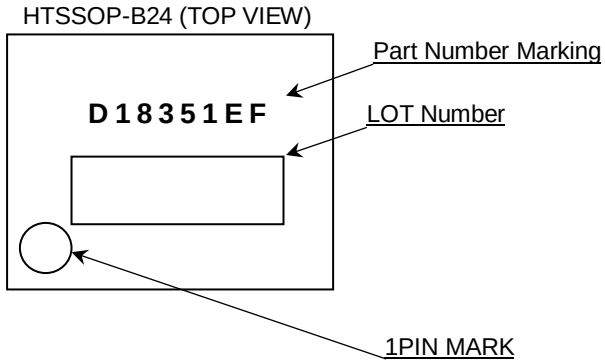
B	D	1	8	3	5	1	E	F	V	-	M	E	2

Part Number

Package
EFV: HTSSOP-B24

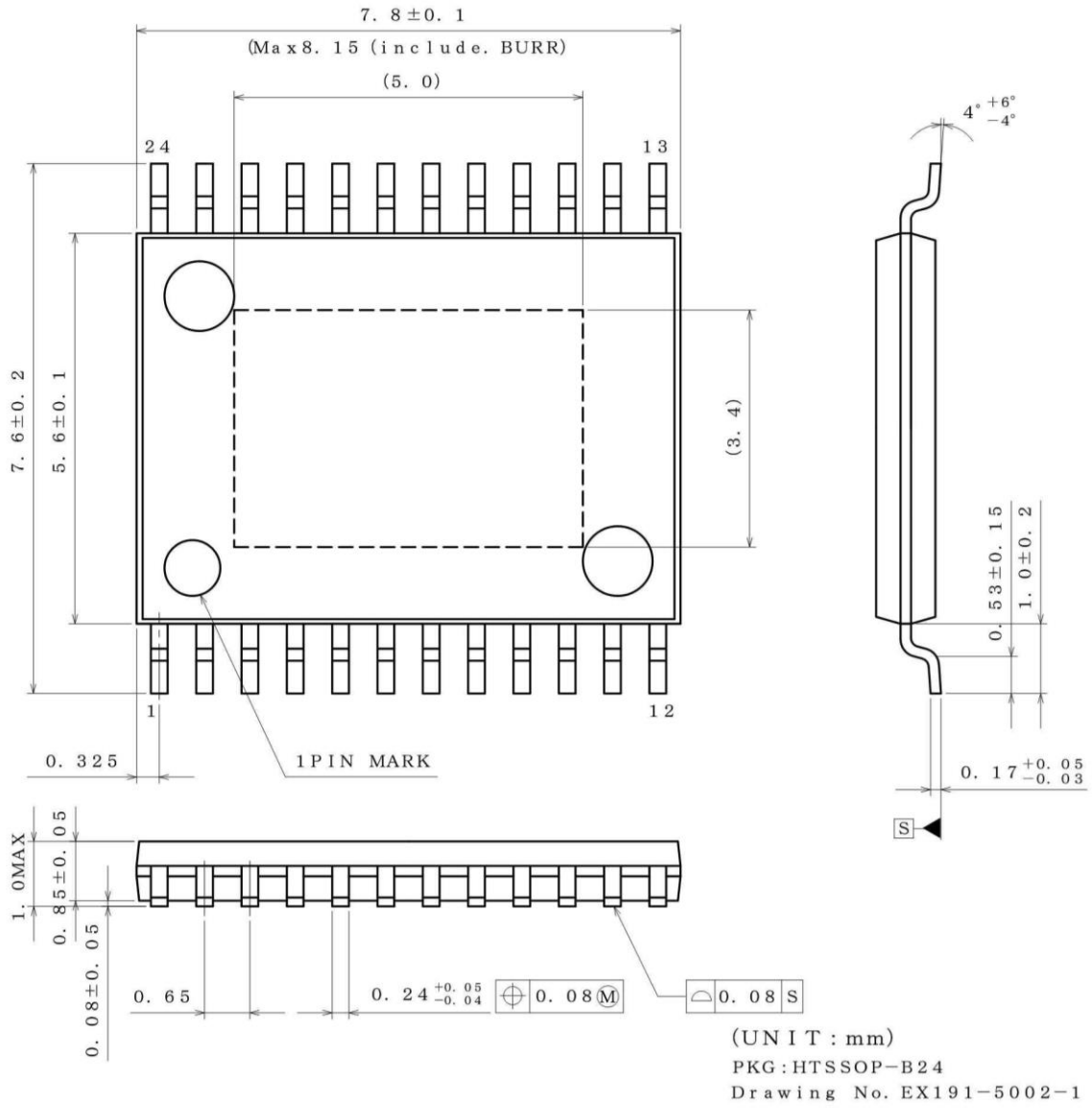
Packaging and forming specification
M : High reliability
E2 : Embossed tape and reel
(HTSSOP-B24)

Marking Diagrams



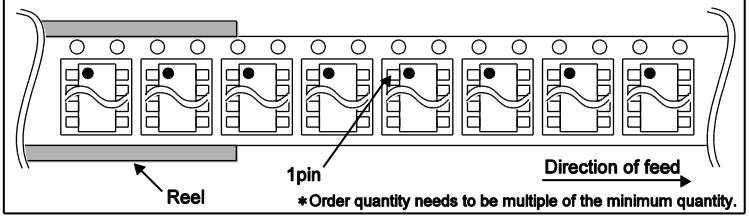
Physical Dimension, Tape and Reel Information

Package Name	HTSSOP-B24



<Tape and Reel information>

Tape	Embossed carrier tape (with dry pack)
Quantity	2000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



∗Order quantity needs to be multiple of the minimum quantity.

Revision history

Date	Revision	Changes
2016.3.4	001	New Release
2016.5.12	002	P.11 Figure 16. Erratum modified P.13 (4), P14 Output short detection function (SCP) Previous rev. ”IMN terminal GND short-circuits”→ Revised ”When LED anode short to GND” P.19 Thermal resistance Previous74.2mm(square) → Revised 74.2mm x 74.2mm P.20 Recommended operation condition CRTIMER output Duty Min Previous rev. ”5%”→ Revised ”2%” P.27 Figure 43. Erratum modified P.31 Figure 48. Erratum modified P.39,40 Modified equivalent circuit
2018.11.7	003	P.1 Previous rev. “Minimum PWM Dimming Pulse Width: 100 µs” Revised “Minimum PWM Dimming Pulse Width: 50 µs” P.4 Previous rev. “(PWM min pulse width=100 µs)” Revised “(PWM min pulse width=50 µs)” P.6 Previous rev. “Minimum pulse width is 100 µs” Revised “Minimum pulse width is 50 µs” P.8 V_{OUT_MAX}, V_{F_MAX}, The number of drivable LED series stages Formula revised. P.20 Previous rev. “Operating Condition (External Constant Range)” Revised “Recommended External Constant Range” P.20 Add (Note3), (Note4), (Note5). P.21 Electrical Characteristics LED Open Detection Voltage Min Previous rev. ”1.35” Revised ”1.42”. P.21 Electrical Characteristics LED Open Detection Voltage Max Previous rev. ”1.65” Revised ”1.575”. P.21 Electrical Characteristics PWM Minimum Pulse Width Min Previous rev. ”100” Revised “50”. P.33 $V_{OUT\_ODT\_MAX}$ Formula revised.
2019.09.02	004	P.21 Output short detection function (SCP) Previous rev. ”C_{VREG50} = 2.2 µF”→ Revised ” C_{VREG50} = 2.2 µF I_{VREG50} = 0mA to 20 mA ” P.32 6. Selection of coil L constant value Formula revised.

Notice

Precaution on using ROHM Products

1. If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), aircraft/spacecraft, nuclear power controllers, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

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   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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