Power Supply Selector Switch IC for SD Cards

BD2204GUL

General Description

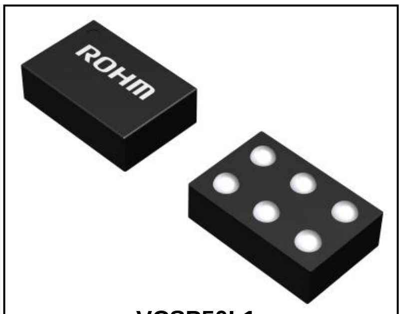
BD2204GUL is high side switch IC that has built-in 2 circuits of MOSFET. Switch has achieved 120mΩ(Typ) on-resistance. 3.3V power supply and 1.8V power supply for memory card can be selected by SEL terminal. Moreover, it has built-in simultaneous-on prevention function at power switching, reverse-current protection function to prevent reverse-current from output terminal to input terminal at power-off, and discharge circuit to discharge electricity in output terminal.

Key Specifications

■ Input voltage range:	VIN1=2.7 to 4.5V VIN2=1.2 to 2.4V
■ ON resistance:	120mΩ(Typ)
■ Operating current:	25µA(Typ)
■ Standby current:	0.01µA(Typ)
■ Operating temperature range:	-40 to +85 °C

Package

Package	W(Typ) x D(Typ) x H(Max)
VCSP50L1	1.50mm x 1.00mm x 0.55mm



VCSP50L1

Features

- Dual channel of low on resistance (Typ = 120mΩ) N-channel MOSFET built in.
- 3.3V and 1.8V are chosen and an output is possible.
- 0.5A Continuous Current load.
- Reverse-current protection when power switch off.
- Prevent VIN1 and VIN2 from simultaneous-on.
- Output Discharge Circuit
- Thermal Shutdown
- Active-High Control Logic
- VCSP50L1 package

Applications

- Digital cameras
- Digital video camera
- SD cards slot

Typical Application Circuit

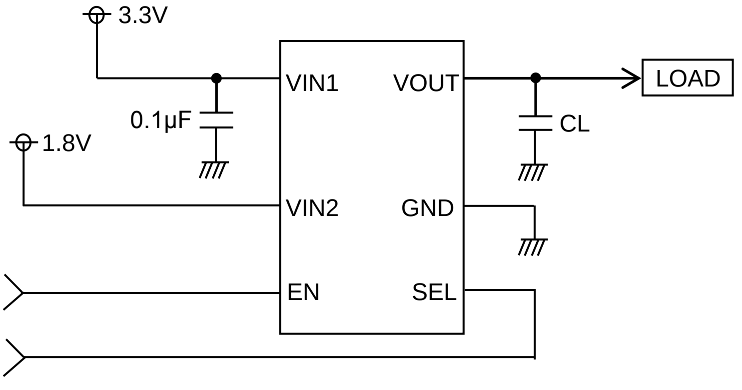


Figure 1. Typical application circuit

〇Product structure : Silicon monolithic integrated circuit 〇This product has no designed protection against radioactive rays

Block Diagram

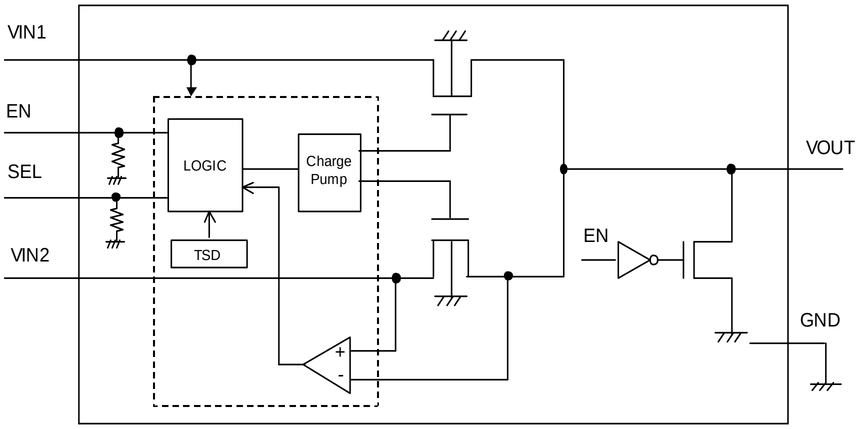


Figure 2. Block Diagram

Pin Configuration

Figure 3. Pin Configuration

Pin Description

Pin No.	Symbol	I / O	Pin function
A1	VIN1	I	Switch1 input and supply voltage for IC
A2	VIN2	I	Switch2 input
A3	EN	I	Active-high enable input with pull-down resistance (Typ 700kΩ)
B1	VOUT	O	Switch output
B2	GND	-	Ground
B3	SEL	I	Output selector input with pull-down resistance (Typ 700kΩ) As SEL=L, VOUT=3.3V output, as SEL=H, VOUT=1.8V output

Absolute Maximum Ratings (Ta = 25°C)

Parameter	Symbol	Ratings	Unit
Switch1 input voltage	V_{IN1}	-0.3 to 6.0	V
Switch2 input voltage	V_{IN2}	-0.3 to 6.0	V
EN voltage	V_{EN}	-0.3 to 6.0	V
SEL voltage	V_{SEL}	-0.3 to 6.0	V
VOUT voltage	V_{OUT}	-0.3 to 6.0	V
Output current	I_{OUT}	1.0	A
Storage temperature	T_{STG}	-55 to 150	°C
Power dissipation	Pd	0.57 (Note 1)	W

(Note 1) In the case of exceeding Ta > 25°C, 4.6mW should be reduced per 1°C (Mount on 50mm x 58mm x 1.75mm Glass Epoxy Board)

Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions (Ta= -40°C to +85°C)

Parameter	Symbol	Ratings			Unit
		Min	Typ	Max	
Switch1 input voltage	V_{IN1}	2.7	3.3	4.5	V
Switch2 input voltage	V_{IN2}	1.2	1.8	2.4	V
Output current	I_{OUT}	-	-	0.5	A

Electrical Characteristics

(VIN1= 3.3V, VIN2= 1.8V, Ta= 25°C, unless otherwise specified.)

Parameter	Symbol	Limits			Unit	Condition
		Min	Typ	Max		
Operating current1	I_{DD1}	-	30	45	µA	V_{EN} = 1.2V, V_{SEL} = 0V VOUT = OPEN
Operating current2	I_{DD2}	-	35	52.5	µA	V_{EN} = V_{SEL} = 1.2V VOUT = OPEN
Standby current	I_{STB}	-	0.01	1	µA	V_{EN} = 0V, VOUT = OPEN
EN, SEL input voltage	V_{ENH} V_{SELH}	1.2	-	-	V	High input
	V_{ENL} V_{SELL}	-	-	0.4	V	Low input
EN, SEL input H current	I_{ENH} I_{SELH}	2.3	4.7	11.0	µA	V_{EN} = V_{SEL} = 3.3V with pull-down resistance
EN, SEL input L current	I_{ENL} I_{SELL}	-1.0	-	1.0	µA	V_{EN} = V_{SEL} = 0V
Pull-down resistance	Rpd	300	700	1400	kΩ	EN and SEL PIN pull-down resistance
On-resistance1	R_{ON1}	-	120	200 *2	mΩ	I_{OUT} = 500mA
On-resistance2	R_{ON2}	-	120	200 *2	mΩ	I_{OUT} = 500mA
Switch leakage current	I_{LEAK}	-	0.01	1	µA	V_{EN} = 0V, VOUT = 0V
Output rise time1	T_{ON1}	-	60	300	µs	SEL = L, RL = 10Ω VOUT : 10% → 90%
Output fall time1	T_{OFF1}	-	0.1	1	µs	SEL = L, RL = 10Ω VOUT : 90% → 10%
Output fall time1DISC	T_{OFF1D}	-	300	1000	µs	EN = SEL = L, CL = 1µF VOUT : 90% → 10%
Output rise time2	T_{ON2}	-	30	150	µs	SEL = H, RL = 10Ω VOUT : 10% → 90%
Output fall time2	T_{OFF2}	-	0.1	1	µs	SEL = H, RL = 10Ω VOUT : 90% → 10%
Output fall time2DISC	T_{OFF2D}	-	220	1000	µs	EN = L, SEL = H, CL = 1µF VOUT : 90% → 10%
Discharge on-resistance	R_{DISC}	-	80	150	Ω	I_{OUT} = -1mA, V_{EN} = 0V
Discharge current	I_{DISC}	-	10	15	mA	VOUT = 3.3V, V_{EN} = 0V
VOUT drop voltage*3	Voutdrop1	-	-	0.4	V	CL = 15µF, I_{OUT} = 500mA VOUT = VIN1→VIN2
	Voutdrop2	-	-	0.4	V	CL = 15µF, I_{OUT} = 500mA VOUT = VIN2→VIN1

*2 Not 100% tested at the time of shipment.

*3 When the switch changes from VIN1 to VIN2 or from VIN2 to VIN1, it is possible that VOUT voltage drops.
Dropped voltage of VOUT is specified as Voutdrop1 and Voutdrop2.
That voltage drop is caused by the function which prevents VIN1 and VIN2 from turning on simultaneously.
This function generates the period which both VIN1and VIN2 are turned off, and prevents the penetration current between VIN1 and VIN2.

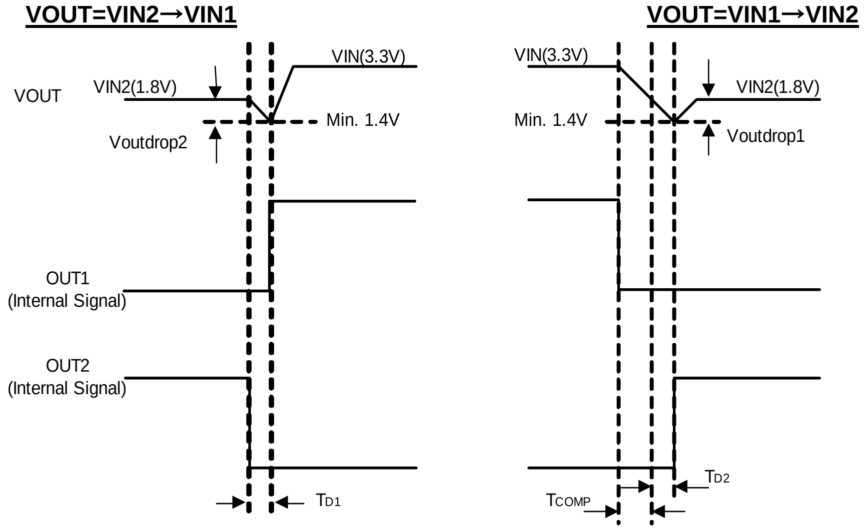
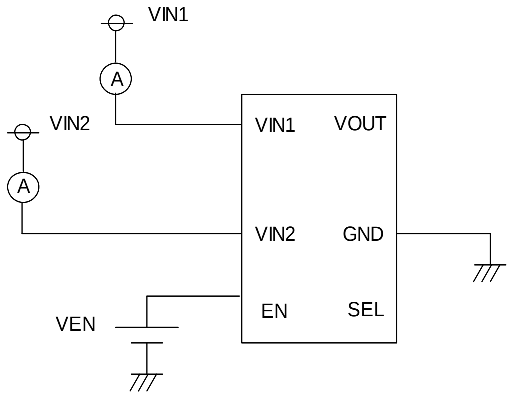


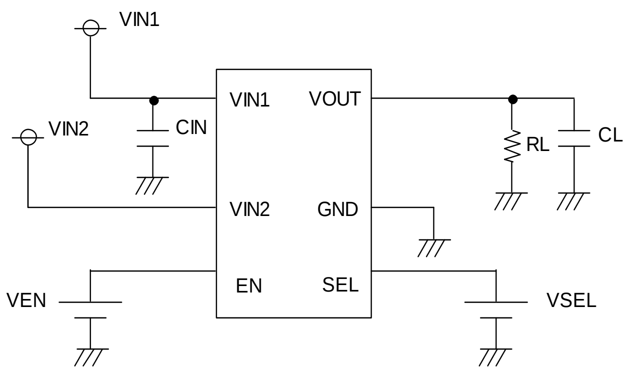
Figure 4. VOUTIdrop voltage

*T_{D1} and T_{D2} + T_{COMP} are period of Simultaneous-Off.
*T_{COMP} is period of VOUT becoming same voltage as VIN2.
*The value of Min. is in condition of I_{OUT}=500mA and CL=15uF.

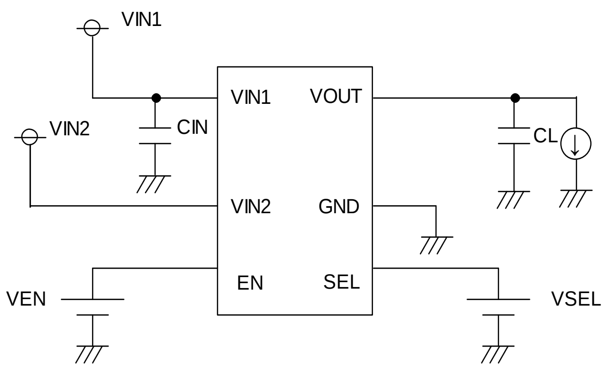
Measurement Circuit



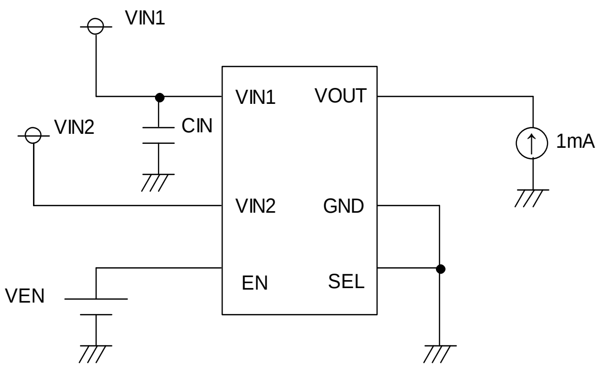
Operating current, Standby current



EN, SEL input voltage, Output rise, fall time



On-resistance, VOUT drop voltage



Discharge resistance

Figure 5. Measurement circuit

Typical Performance Curves

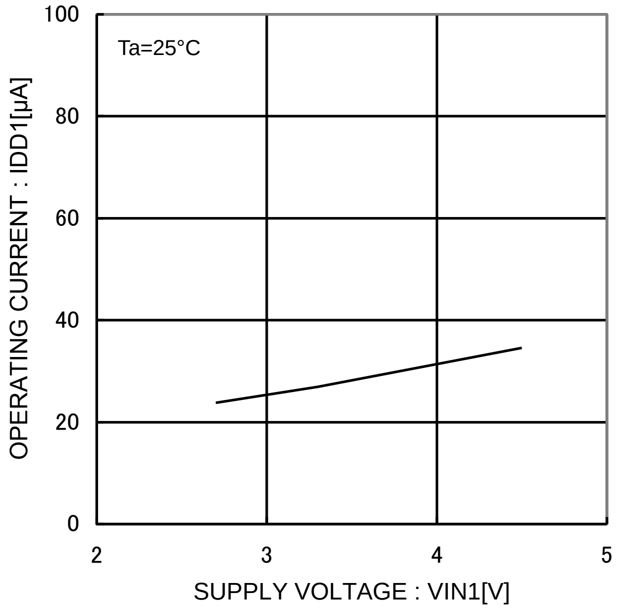


Figure 6. Operating current1
EN Enable

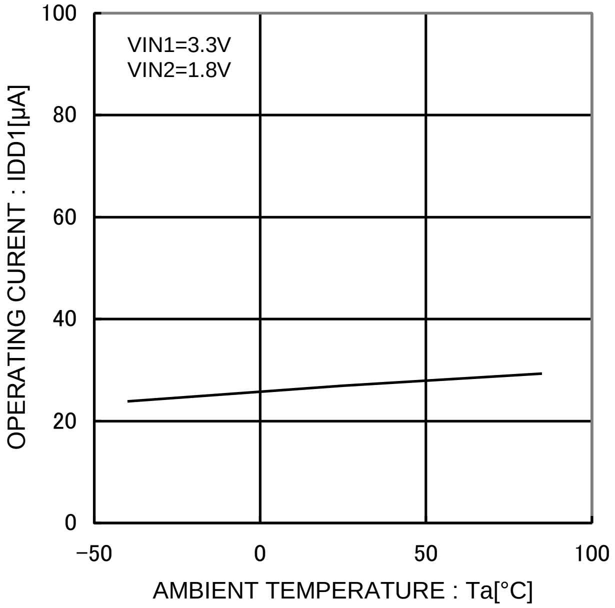


Figure 7. Operating current1
EN Enable

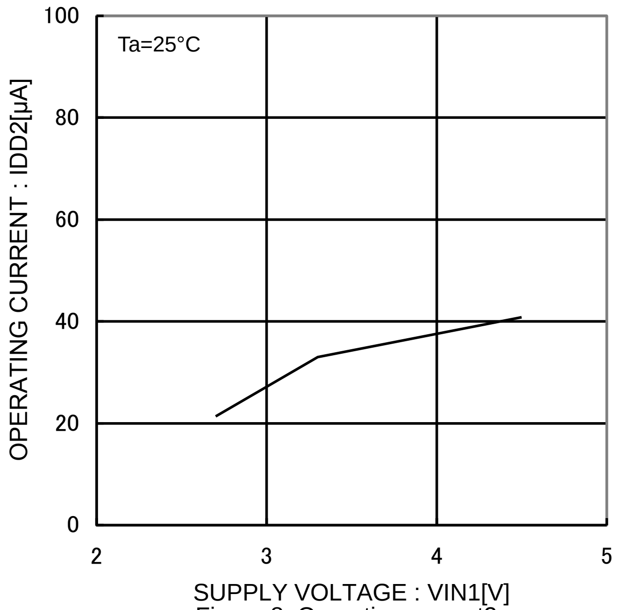


Figure 8. Operating current2
EN Enable

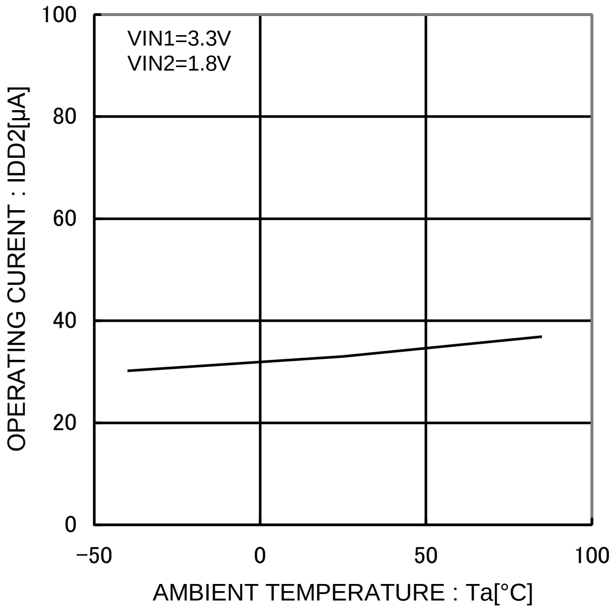


Figure 9. Operating current2
EN Enable

Typical Performance Curves - continued

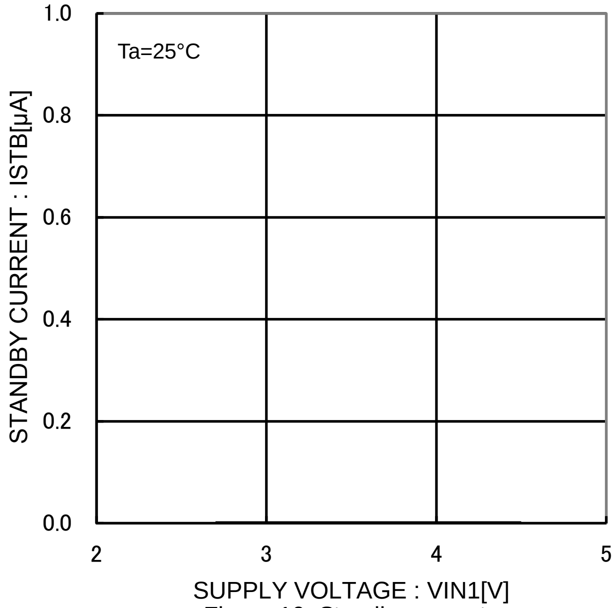


Figure 10. Standby current

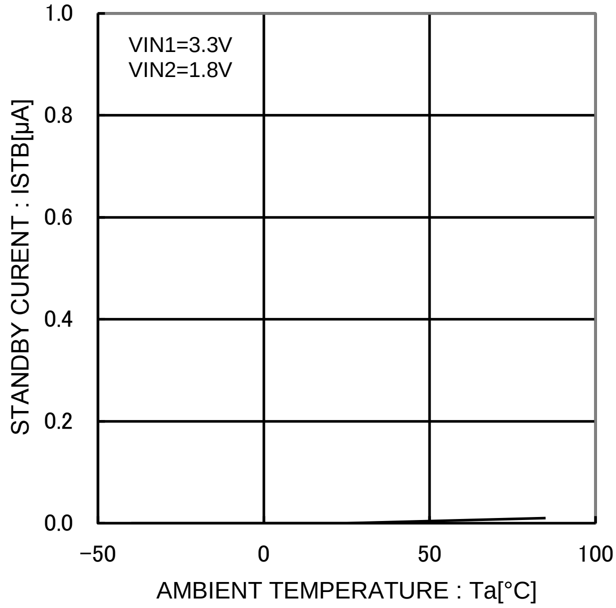


Figure 11. Standby current

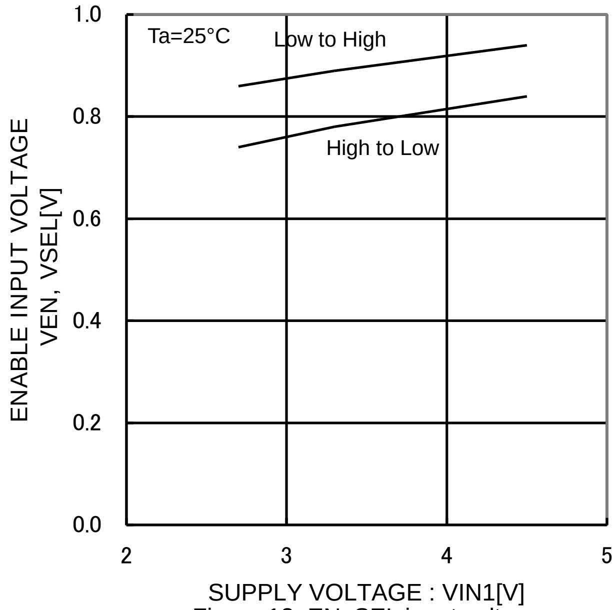


Figure 12. EN, SEL input voltage

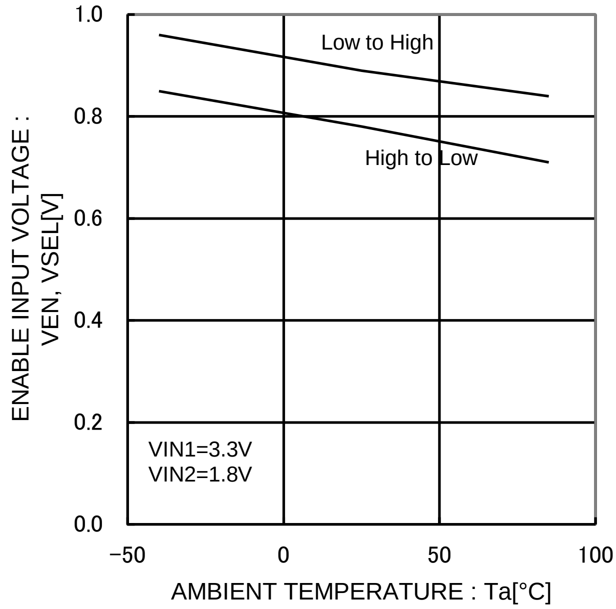


Figure 13. EN, SEL input voltage

Typical Performance Curves - continued

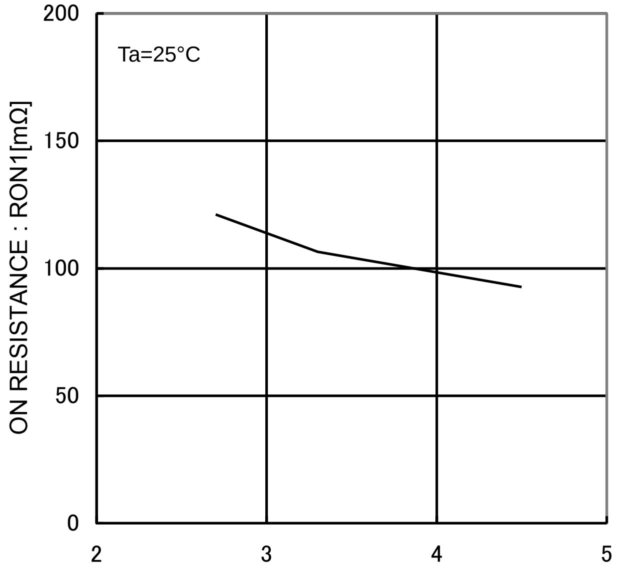


Figure 14. On-resistance1

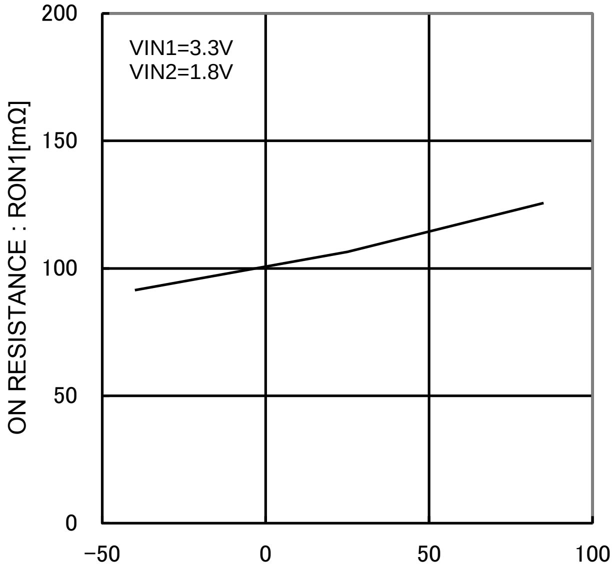


Figure 15. On-resistance1

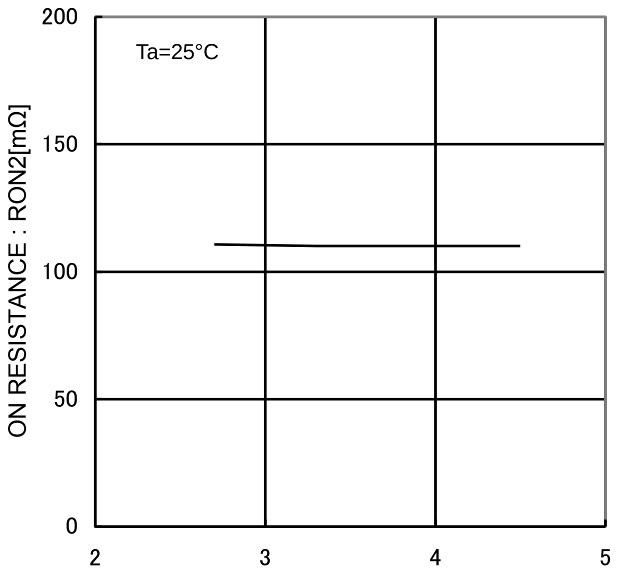


Figure 16. On-resistance2

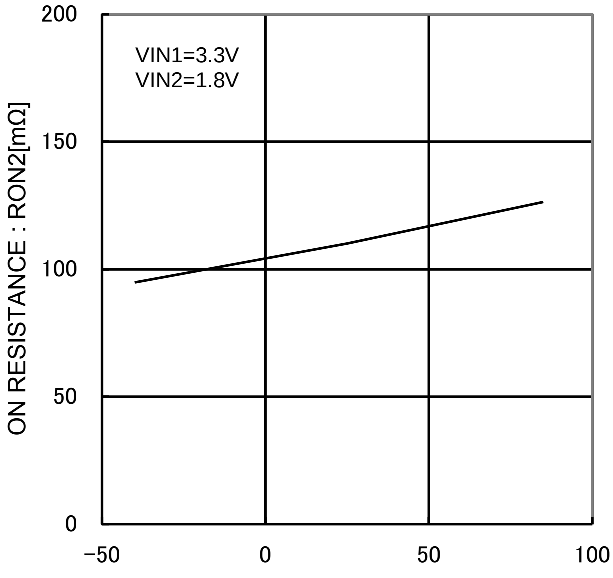


Figure 17. On-resistance2

Typical Performance Curves - continued

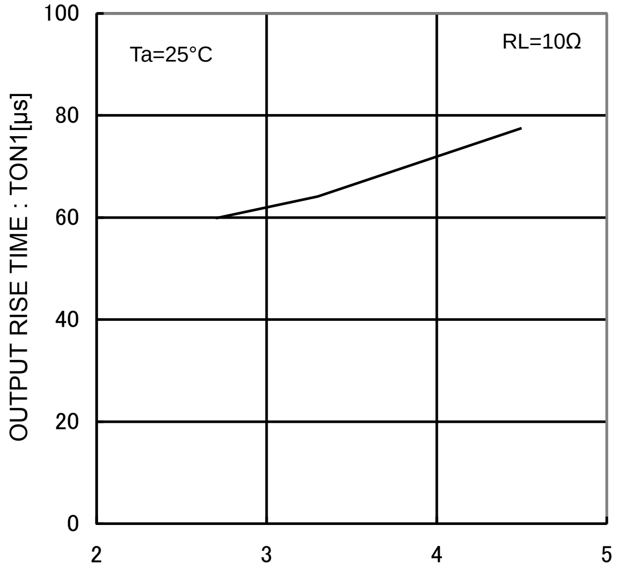


Figure 18. Output rise time1

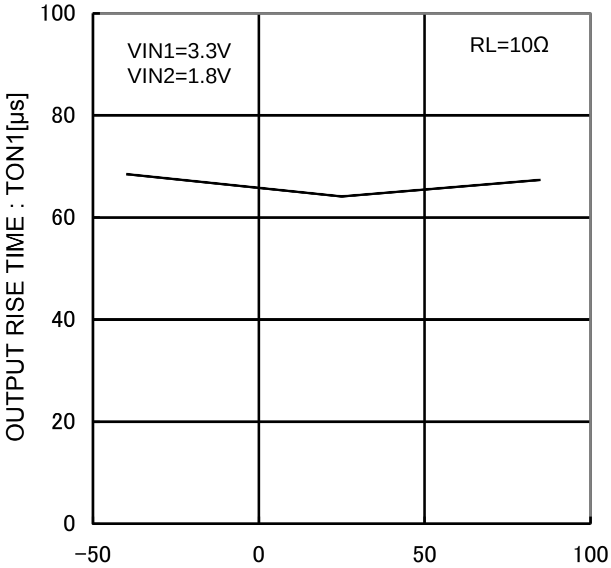


Figure 19. Output rise time1

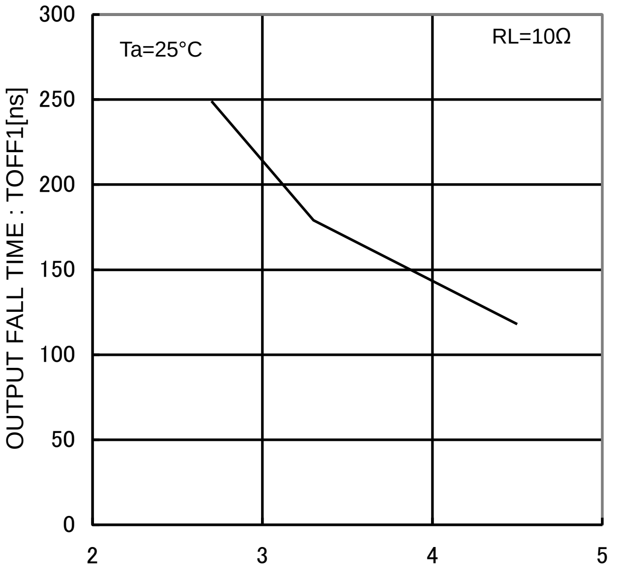


Figure 20. Output fall time1

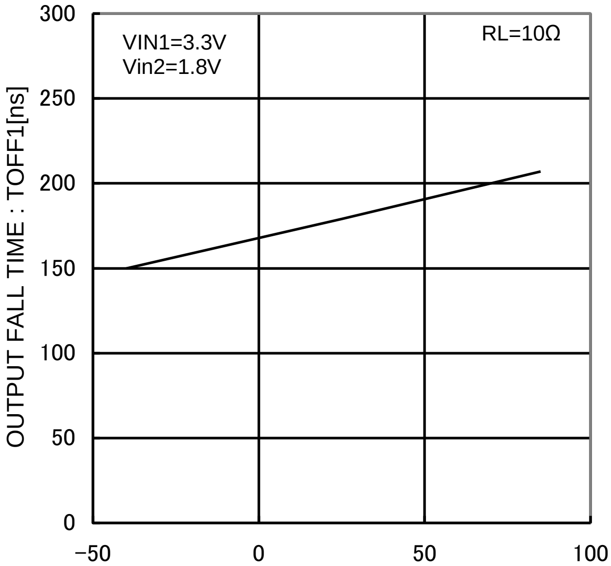


Figure 21. Output fall time1

Typical Performance Curves - continued

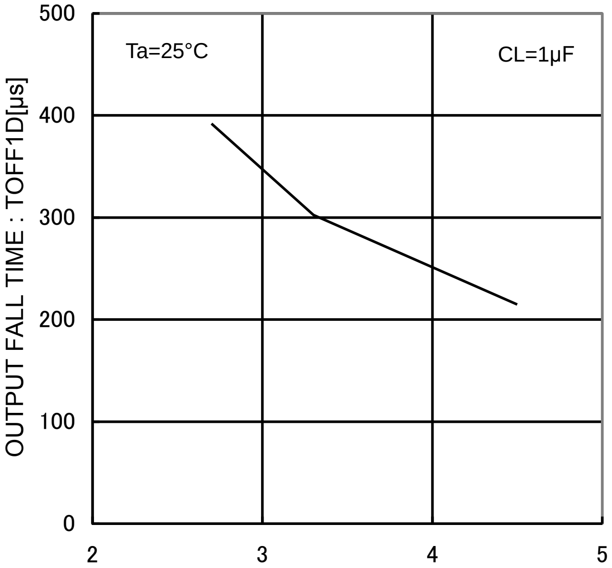


Figure 22. Output fall time1DISC

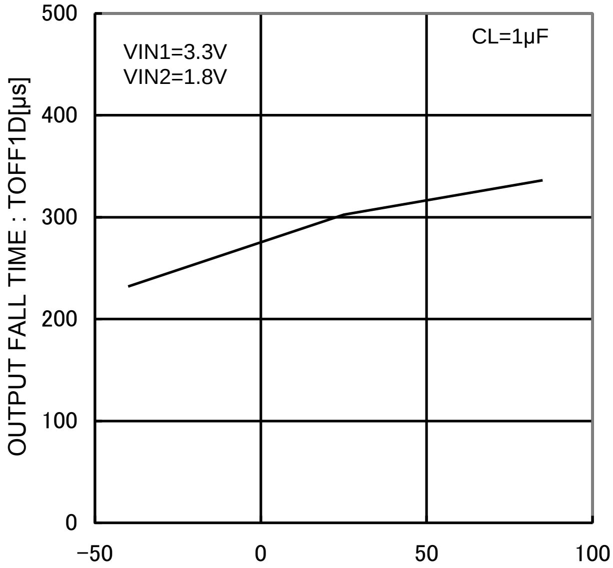


Figure 23. Output fall time1 DISC

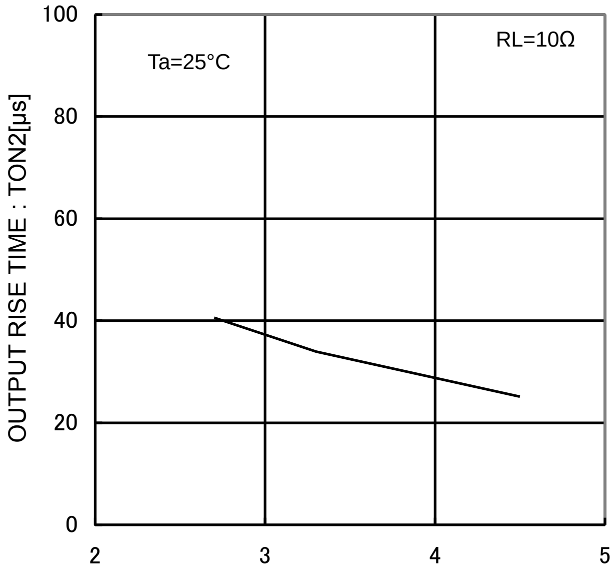


Figure 24. Output rise time2

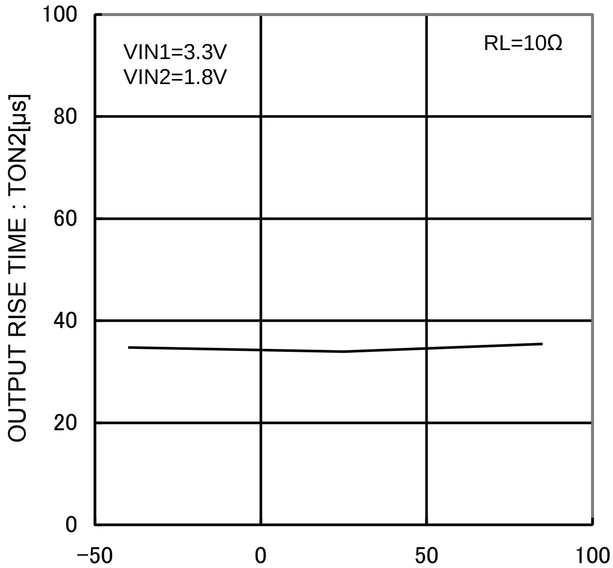


Figure 25. Output rise time2

Typical Performance Curves - continued

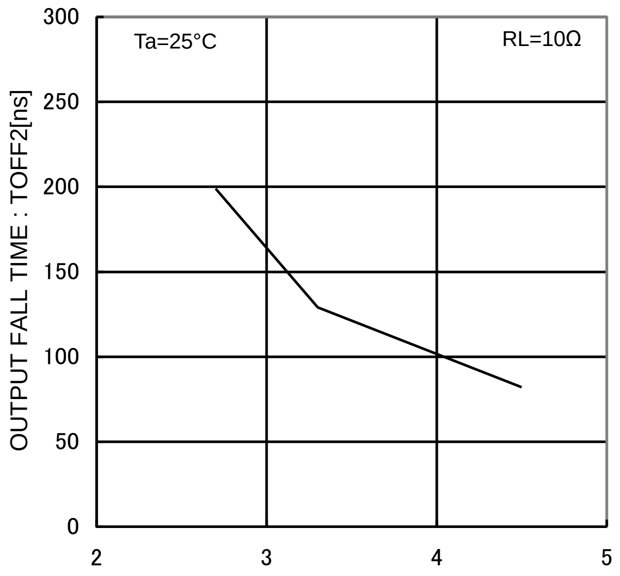


Figure 26. Output fall time2

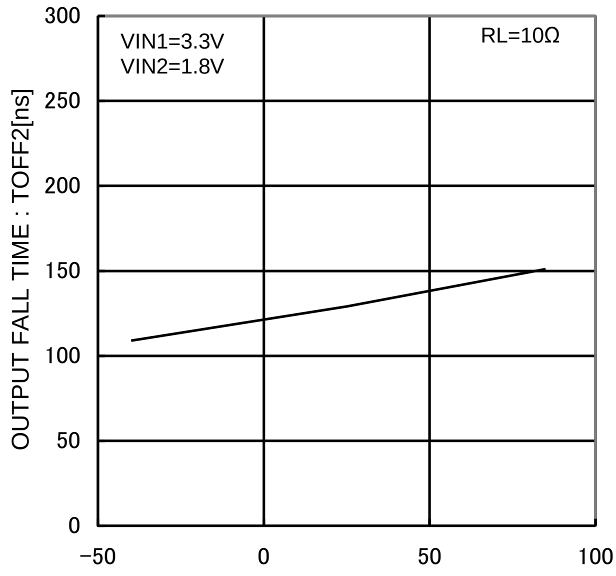


Figure 27. Output fall time2

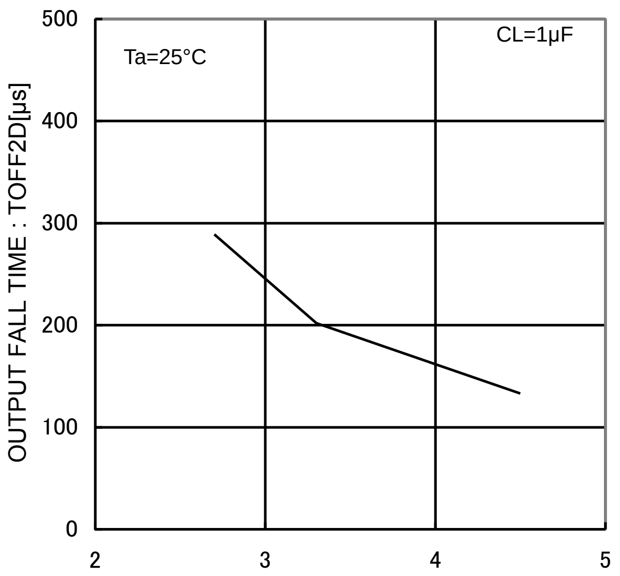


Figure 28. Output fall time2 DISC

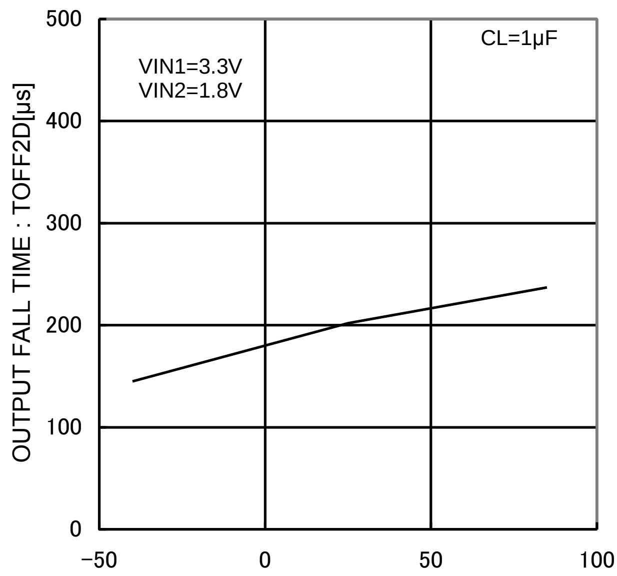


Figure 29. Output fall time2 DISC

Typical Performance Curves - continued

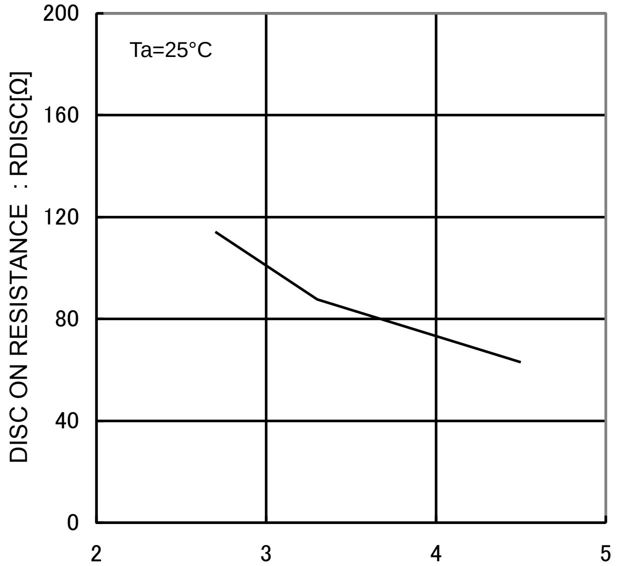


Figure 30. Discharge resistance

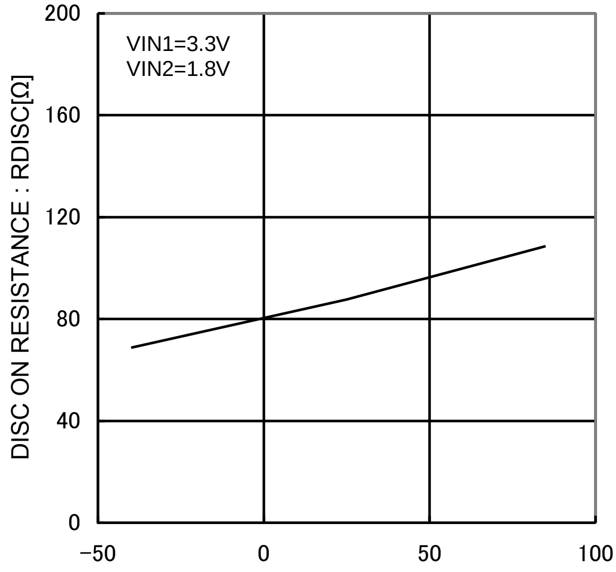


Figure 31. Discharge resistance

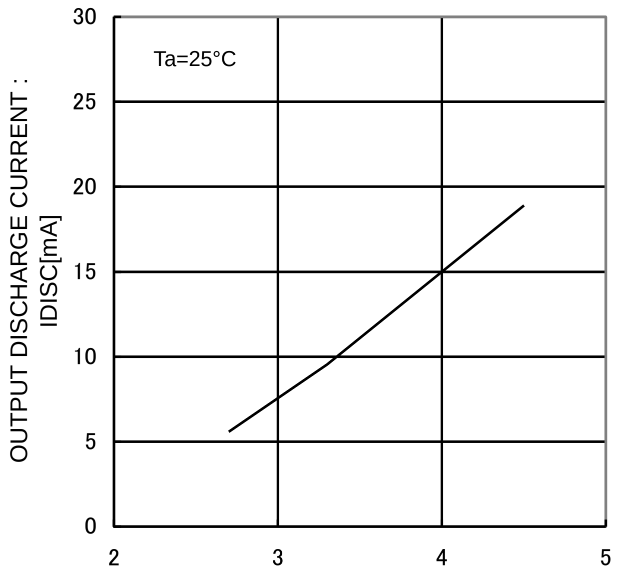


Figure 32. Discharge current

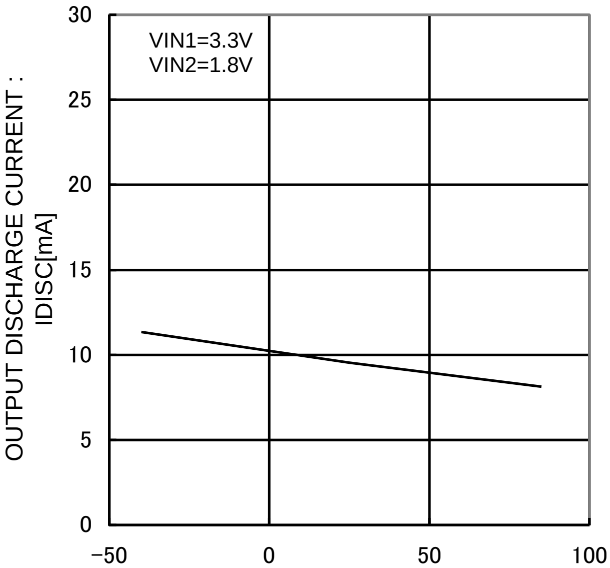


Figure 33. Discharge current

Typical Performance Curves - continued

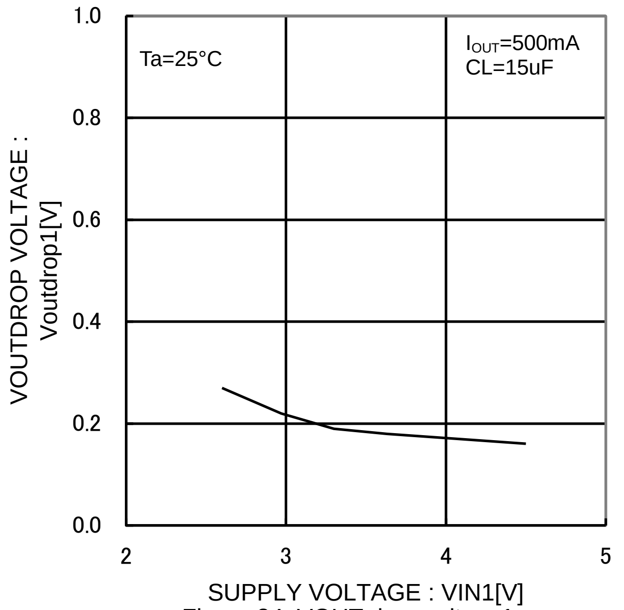


Figure 34. VOUT drop voltage1

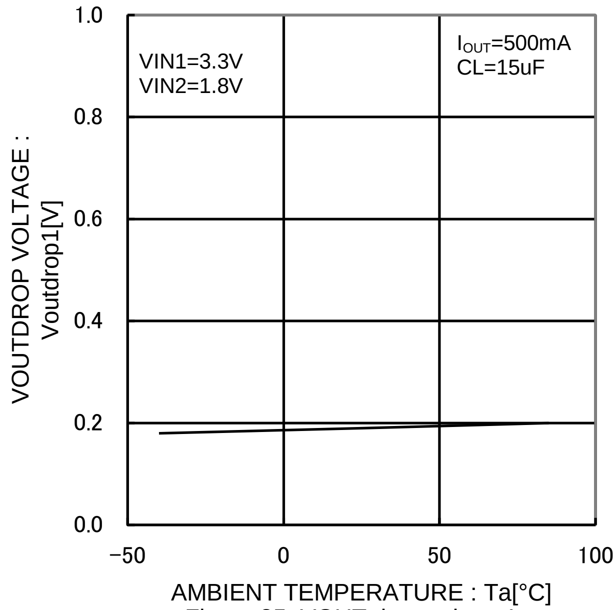


Figure 35. VOUT drop voltage1

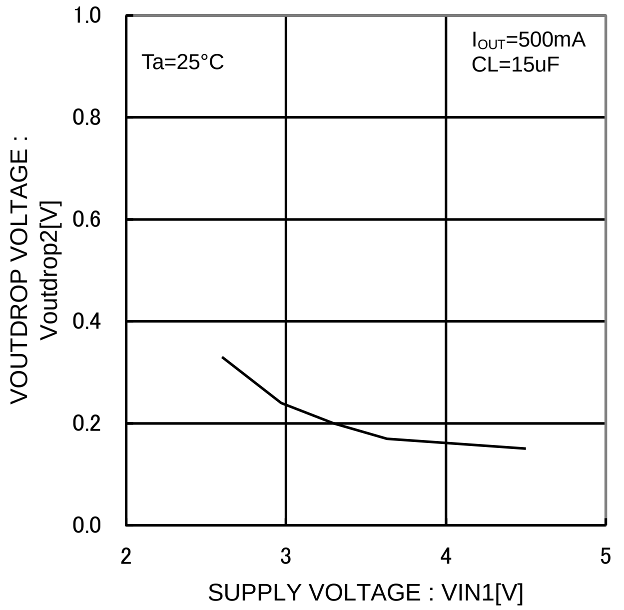


Figure 36. VOUT drop voltage2

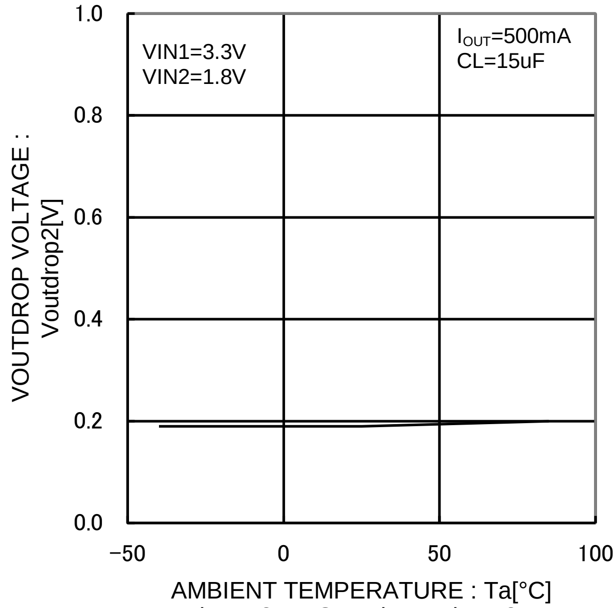


Figure 37. VOUT drop voltage2

Typical Performance Curves - continued

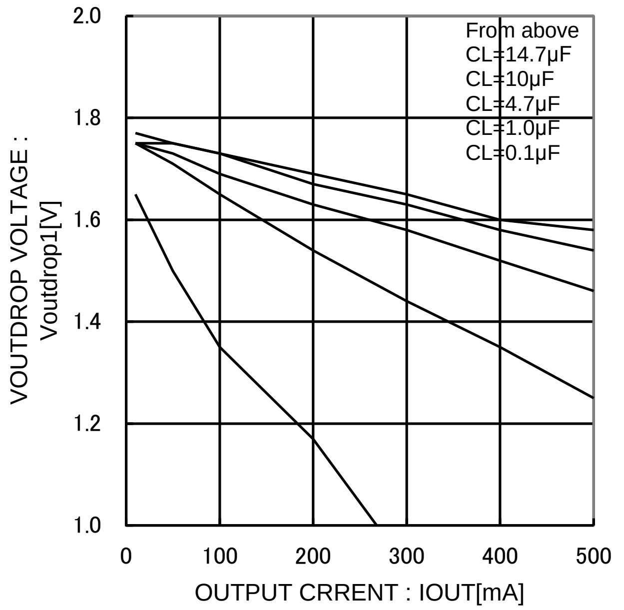


Figure 38. VOUT voltage drop
Switch over from VIN1 to VIN2

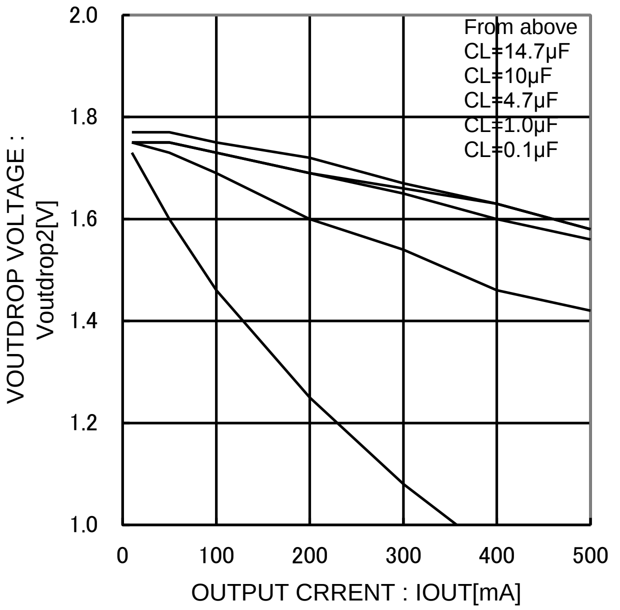


Figure 39. VOUT voltage drop
Switch over from VIN2 to VIN1

Typical Wave Forms

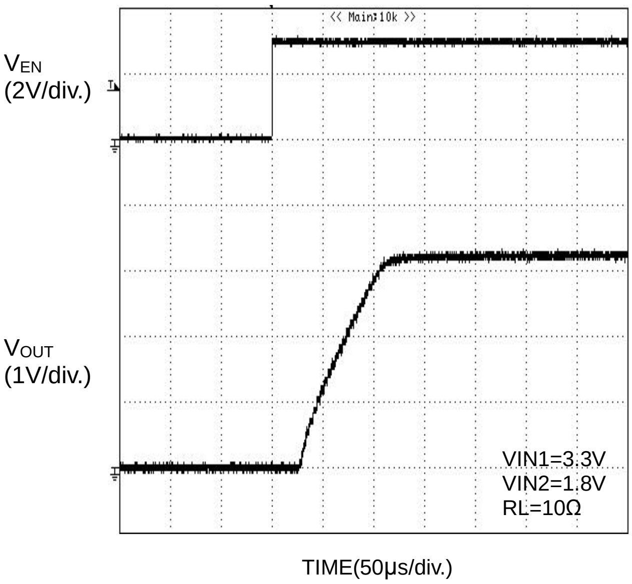


Figure 40. Output rise characteristic
SEL=L

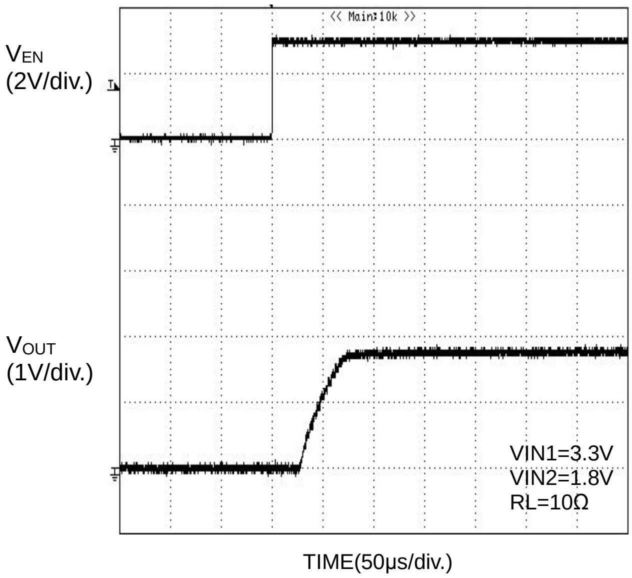


Figure 41. Output rise characteristic
SEL=H

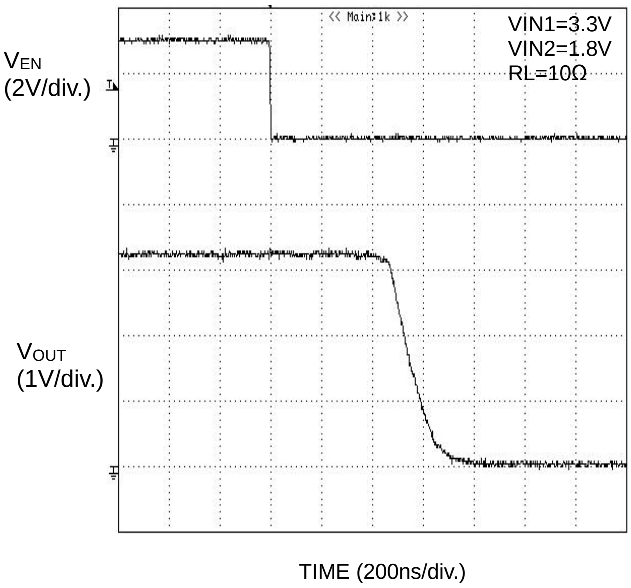


Figure 42. Output fall characteristic
SEL=L

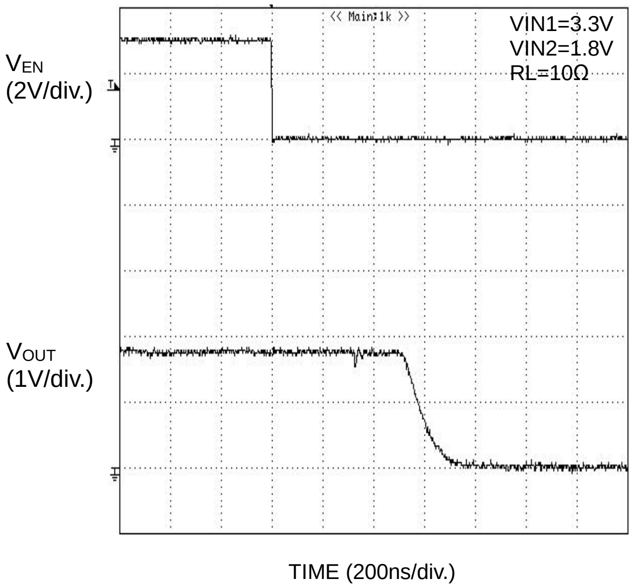


Figure 43. Output fall characteristic
SEL=H

Typical Wave Forms - continued

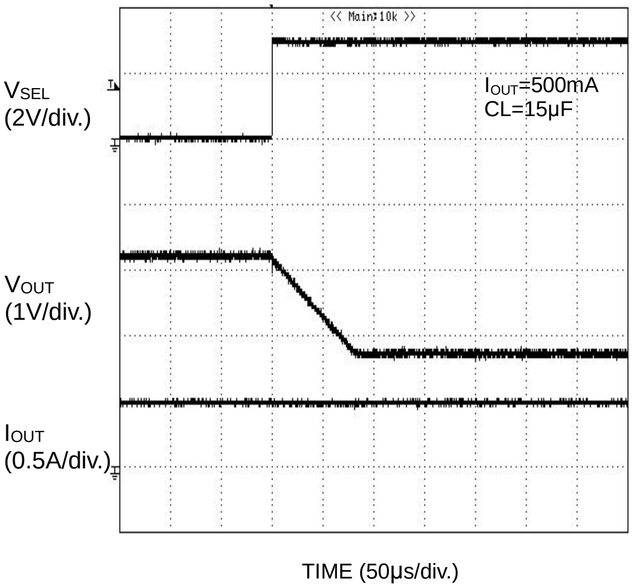


Figure 44. Power switch over characteristic from VIN1 to VIN2

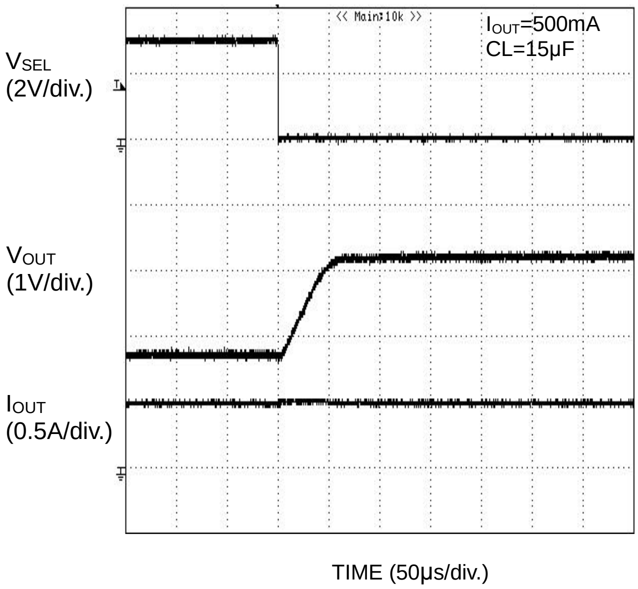


Figure 45. Power switch over characteristic from VIN2 to VIN1

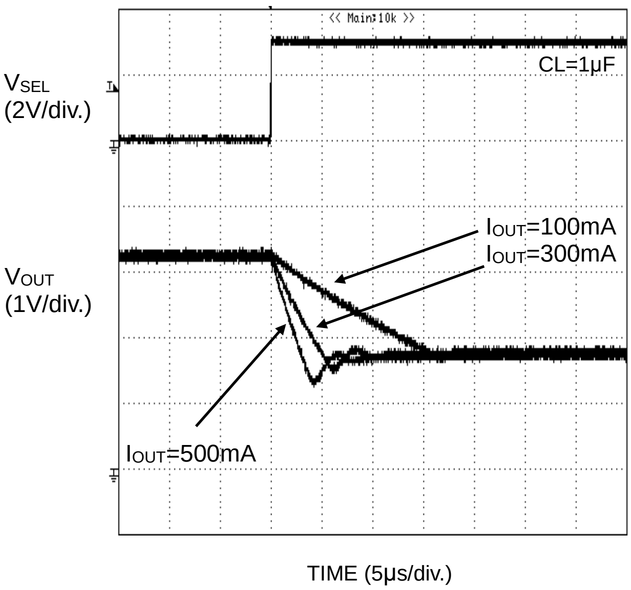


Figure 46. Power switch over characteristic from VIN1 to VIN2

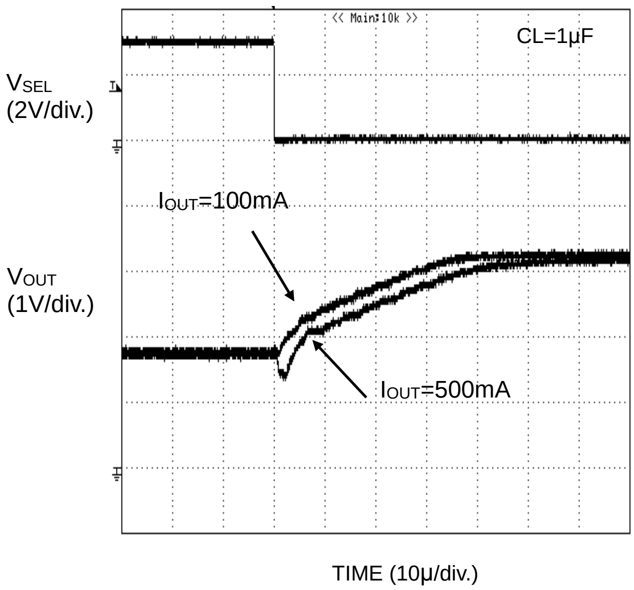


Figure 47. Power switch over characteristic from VIN2 to VIN1

Application Example

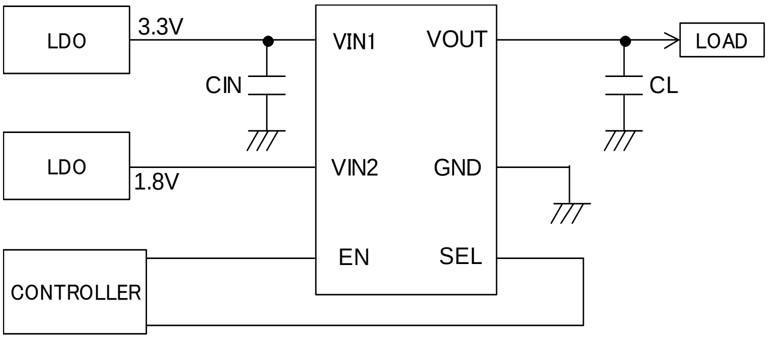


Figure 48. Application circuit example

Application Information

When ringing occurs power source line to IC, and may cause bad influences upon IC actions. In order to avoid this case, connect a low ESR bypath capacitor which than 0.1µF, nearby VIN1 terminal and GND terminal of IC.

When SEL pin worked, the load current (I_{OUT}) and the load capacity (CL) of output give a change in VOUT drop voltage and change over time. Decide load capacity (CL) suited to load current (I_{OUT}).

The external circuit constant and so on is changed and it uses, in which there are adequate margins by taking into account external parts or dispersion of IC including not only static characteristics but also transient characteristics.

Functional Description

1. Switch operation

VIN1 terminal, VIN2 terminal and VOUT terminal are connected to the drain and the source of switch MOSFET respectively. And the VIN1 terminal is used also as power source input to internal control circuit.

When the switch is turned on from EN control input at SEL=L (SEL=H) input, VIN1 (VIN2) terminal and VOUT terminal are connected by a 120mΩ switch. In ON status, the switch is bi-directional. Therefore, when the potential of VOUT terminal is higher than that of VIN1 (VIN2) terminal, current flows from VOUT terminal to VIN1 (VIN2) terminal.

Since a parasitic diode between the drain and the source of switch MOSFET is canceled, in the OFF status, it is possible to prevent current from flowing reversely from VOUT to VIN1 (VIN2).

2. Change over operation

When H is input to SEL terminal while VIN1 voltage has been output to VOUT terminal, VIN2 voltage is output to VOUT terminal after detecting that VOUT terminal becomes lower than VIN2 voltage in order to prevent current from flowing reversely. In this case, the load current (I_{OUT}) and the load capacity (CL) of output give a change in VOUT drop voltage and change over time. When L is input to SEL terminal while VIN2 voltage has been output to VOUT terminal, VIN1 voltage is output to VOUT terminal immediately.

3. Thermal shutdown circuit (TSD)

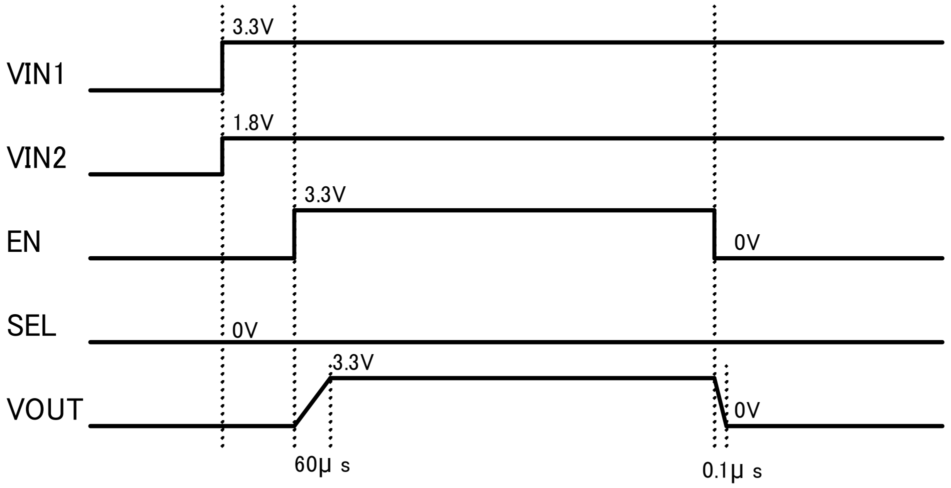
If over current would continue, the temperature of the IC would increase drastically. If the junction temperature were beyond 135°C (Typ), thermal shutdown circuit operates and makes power switch turn off. Then, when the junction temperature decreases lower than 115°C (Typ), power switch is turned on. Unless the fact of the increasing chips temperature is removed or the output of power switch is turned off, this operation repeats.
The thermal shutdown circuit operates when the switch is on (EN signal is active).

4. Discharge Circuit

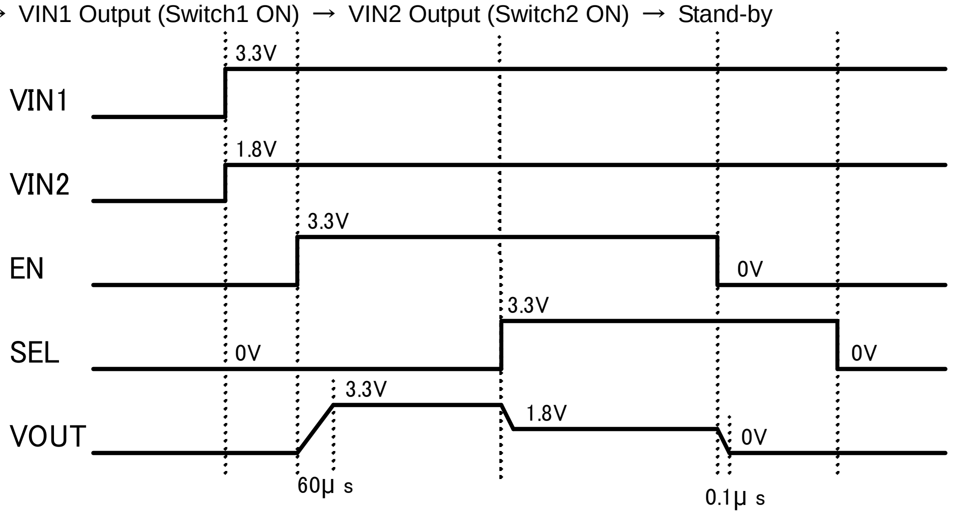
Discharge circuit operates when switch off. When discharge circuit operates, 80Ω(Typ) resistor is connected between VOUT pin and GND pin. This discharges the electrical charge quickly.

Timing Chart

1) Stand-by → Switch1 ON → Stand-by



2) Stand-by → VIN1 Output (Switch1 ON) → VIN2 Output (Switch2 ON) → Stand-by



3) Stand-by → VIN2 Output (Switch2 ON) → VIN1 Output (Switch1 ON) → Stand-by

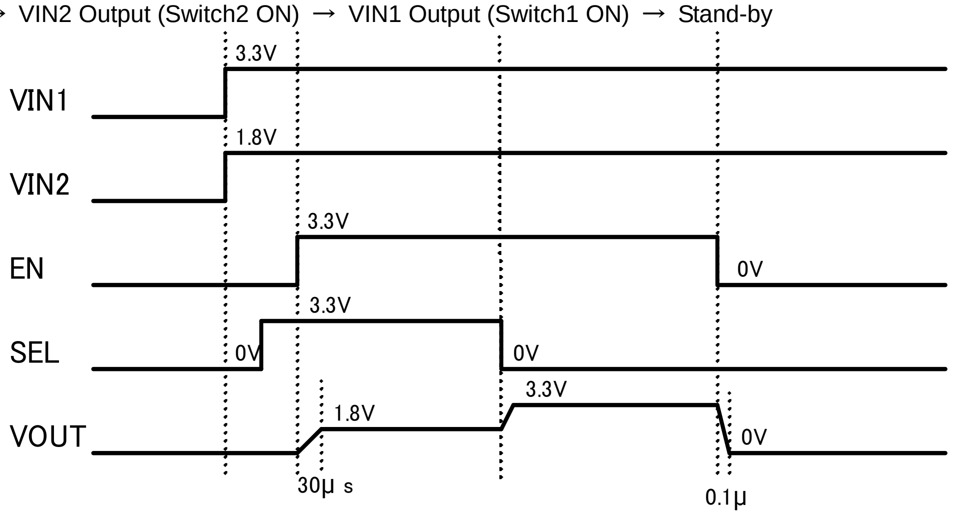
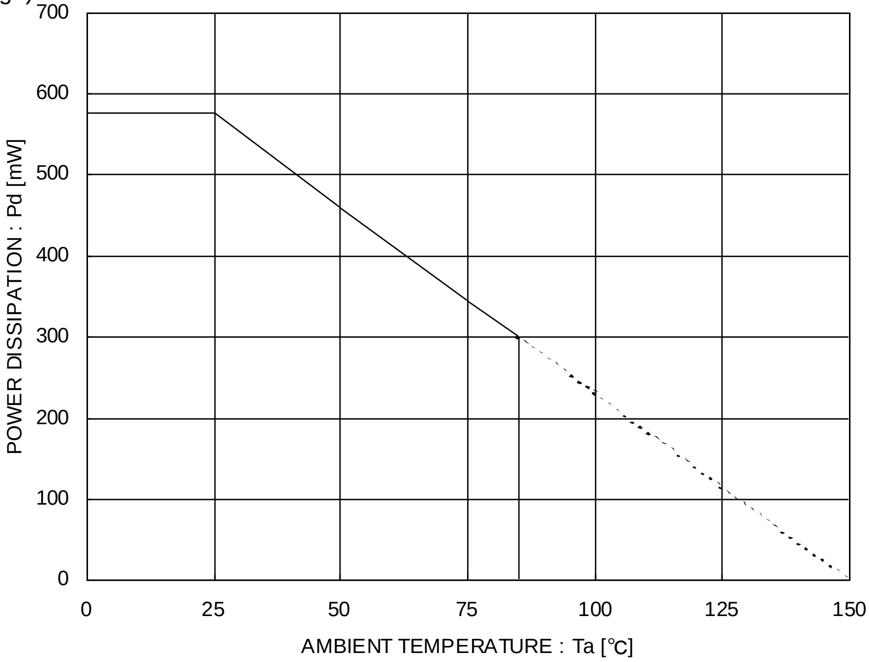


Figure 49. Timing Chart

Power Dissipation

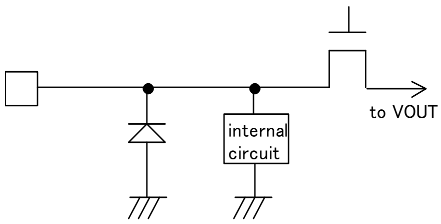
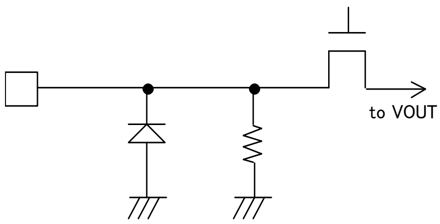
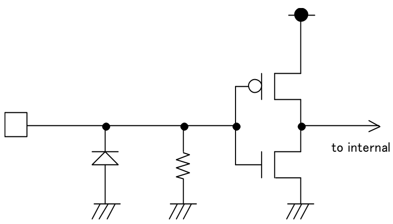
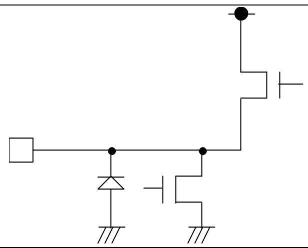
(VCSP50L1 package)



* 50mm x 58mm x 1.75mm Glass Epoxy Board

Figure 50. Power dissipation curve (Pd-Ta Curve)

I/O Equivalence Circuit

Symbol	Pin No	Equivalent circuit
VIN1	A1	
VIN2	A2	
EN, SEL	A3, B3	
VOUT	B1	

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Thermal Consideration**
   Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.

6. **Recommended Operating Conditions**
   These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.

7. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

8. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

9. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

10. **Inter-pin Short and Mounting Errors**
    Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.
Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

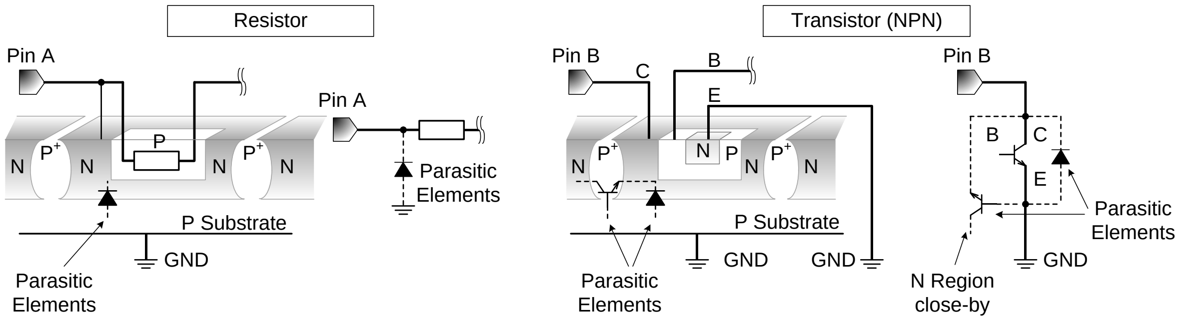


Figure 51. Example of monolithic IC structure

13. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

14. Thermal Shutdown Circuit(TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

15. Disturbance light

In a device where a portion of silicon is exposed to light such as in a WL-CSP, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

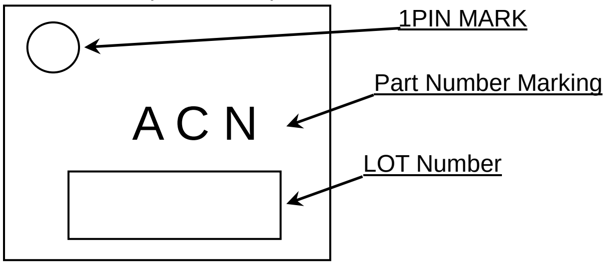
Ordering Information

B	D	2	2	0	4	G	U	L	-	E2

- Part Number
- Package
  GUL:VCSP50L1
- Packaging and forming specification
  E2: Embossed tape and reel

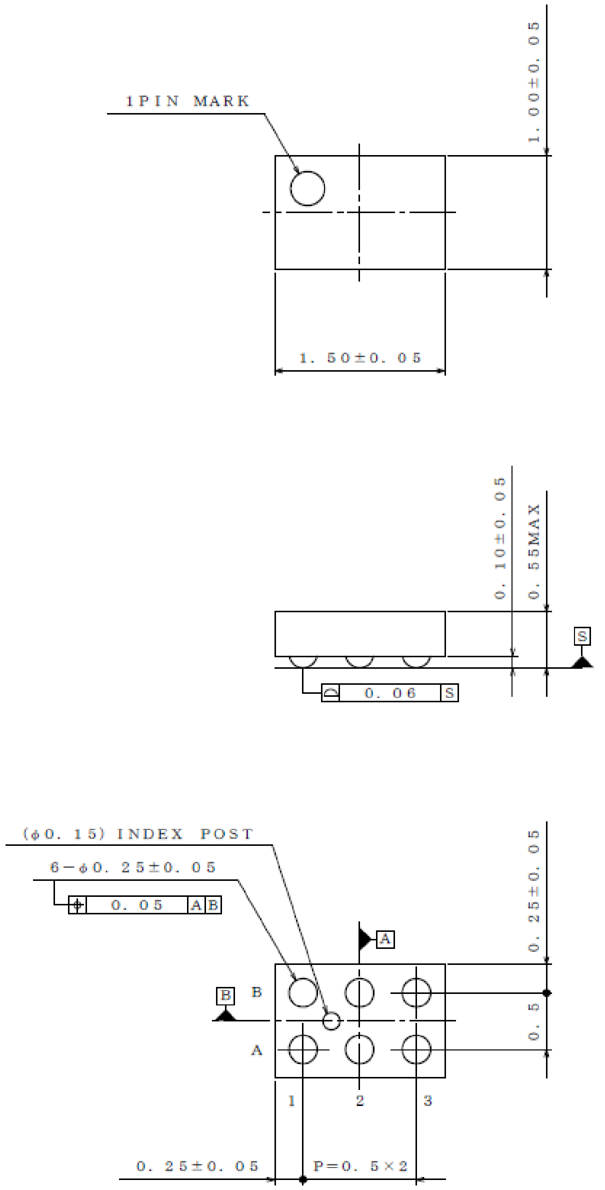
Marking Diagrams

VCSP50L1 (TOP VIEW)



Physical Dimension, Tape and Reel Information

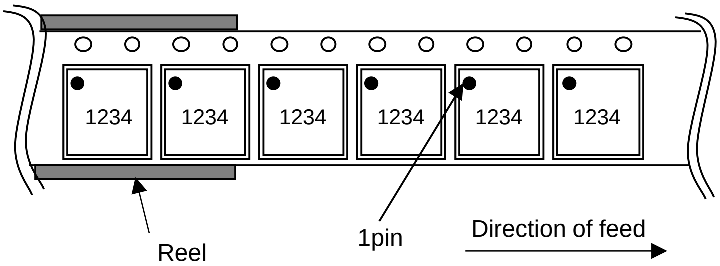
Package Name	VCSP50L1(BD2204GUL)



(UNIT : mm)

< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
07.Aug.2012	001	New Release
20.Feb.2015	002	Revised pull-down resistance value of Pin Description and Operational Notes.
25.Sep.2015	003	Add Top View of Pin Configuration Revised Figure 38, 39

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<table>
<tr><th>JAPAN</th><th>USA</th><th>EU</th><th>CHINA</th></tr>
<tr><td>CLASSⅢ</td><td rowspan="2">CLASSⅢ</td><td>CLASSⅡb</td><td rowspan="2">CLASSⅢ</td></tr>
<tr><td>CLASSⅣ</td><td>CLASSⅢ</td></tr>
</table>

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   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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   [b] the temperature or humidity exceeds those recommended by ROHM
   [c] the Products are exposed to direct sunshine or condensation
   [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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