Power Management Integrated Circuit

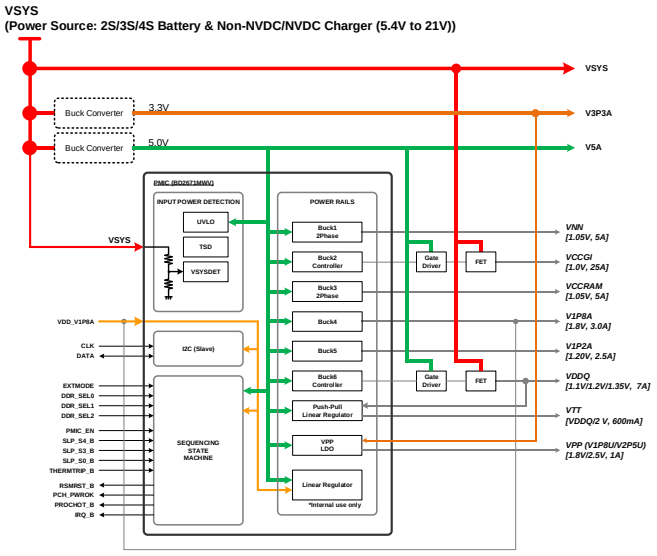
BD2671MWV

●General Description

The BD2671MWV is an integrated Power Management IC available in 68-pin 0.40-mm pitch QFN package and dedicated to application powered by a 5V input. The device provides two Buck controller, four Buck converters, two LDOs, and is designed to support the specific power requirements of Intel®Gemini Lake™ platform to achieve the low BOM-cost for cost-competitive solutions with addition of the smallest number of external components leading to minimum failure for higher system reliability.

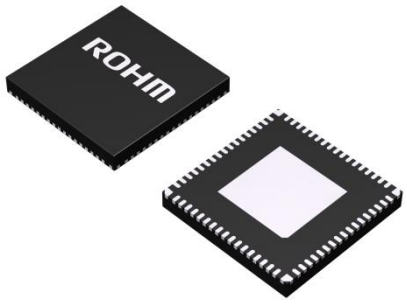
●Key Features

- 4.5V to 5.25V VSYS_V5A Ranges
- 5.4V to 21V VSYS Ranges
- 2ch Buck Controller for External Drivers
  - VCCGI:0.50V-1.45V (VID adjustable),I_{OMAX} = 25A
  - VDDQ: 1.1V/1.2V/1.35V, I_{OMAX} = 7.0A
  - Switching Frequency
    VCCGI: 666kHz, VDDQ: 750kHz
  - Adjustable current-limit threshold allowing optimization for different applications with different load currents
  - Dynamic Voltage Scaling in 10mV steps for processor cores(VCCGI)
  - DDR_SEL0,1,2 dedicated pins for VDDQ voltage select for DDR3L/LPDDR3/LPDDR4/DDR4 support
  - VDDQ output voltage fine adjustment registers
  - VDDQ output voltage on-the-fly change between different DDR modes
- 2ch 2-multi-phase Buck Regulators with Integrated Switching FETs
  - VNN: 0.50V-1.45V (VID adjustable), I_{OMAX} = 5.0A
  - VCCRAM: 1.05V, I_{OMAX} = 5.0A
  - Dynamic Voltage Scaling in 10mV steps for processor cores(VNN)
  - Programmable Voltage control by I2C(VCCRAM)
- 2ch low power consumption Buck Regulators with Integrated Switching FETs
  - V1P8A: 1.80V, I_{OMAX} = 3.0A
  - V1P2A: 1.20V, I_{OMAX} = 2.5A
  - Programmable Voltage control by I2C
- 2ch Linear Regulator
  - VDDQ_VTT : VDDQ/2, I_{OMAX} = 600mA
  - LDO_VPP: 1.8V/2.5V automatic select by DDR_SEL pin configuration
    2.5V output supporting DDR4
    I_{OMAX} = 1000mA
- LDO_VPP can be optionally used as an output enable control of an external switch for low-heat applications on LPDDR3 or LPDDR4
- Programmable discharge resistance for each VRs
- Seamless transition between PWM and PFM Mode enabling maximum efficiency performance
- Forced PWM mode function by I2C control
- Host Interface
  - Interrupt Controller with Maskable Interrupts
  - Dedicated IRQ_B Interrupt output pin
  - DetectorsPROCHOT_B pin (Open Drain) for signaling PMIC hot to host
- Detectors
  - Under Voltage Lock Out
  - Over Current Protection
  - Thermal Shutdown Protection and hot-die detection
  - Power Good Monitoring on all Buck Supply Outputs
- I2C interface provides access to configuration registers.
- Internal registers having a complete set of status information enabling easy diagnostics and host-controlled handling of fault conditions.
- Flexible use of External Regulators for VCCGI and VNN which the internal VCCGI and VNN can be easily disabled by EXTMODE pin
- Features equipped for VCCRAM and V1P2A that can be merged independently to VNN and VDDQ as well when BOM-cost is more sensitive than power efficiency



●Package

- **UQFN68AV8080**
  W(typ)=8.00mm, L(typ)=8.00mm, H(max)=1.00mm



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1 Introduction

1-1 Terminology

Table 1-1 defines the acronyms, conventions, and terminology that are used throughout this design guide.

Table 1-1 Acronyms, Conventions and Terminology

Term	Definition
BOM	Bill Of Materials
DAC	Digital to Analog Converter
FET	Field Effect Transistor
I2C	Inter-Integrated Circuit
IRQ	Interrupt Request
LDO	Low Drop-Out regulator
NTC	Negative Temperature Coefficient. (a type of thermistor)
OCP	Over Current Protection
OTP	One Time Programmable memory
OVP	Over Voltage protection
PFM	Pulse-Frequency Modulation
POR	Power On Reset
PWM	Pulse-Width Modulation
SMPS	Switched Mode Power Supply
SOC	System-On-a-Chip
UVLO	Under Voltage-LockOut
VID	Voltage IDentification
VR	Voltage Regulator

1-2 Typical Application Circuit

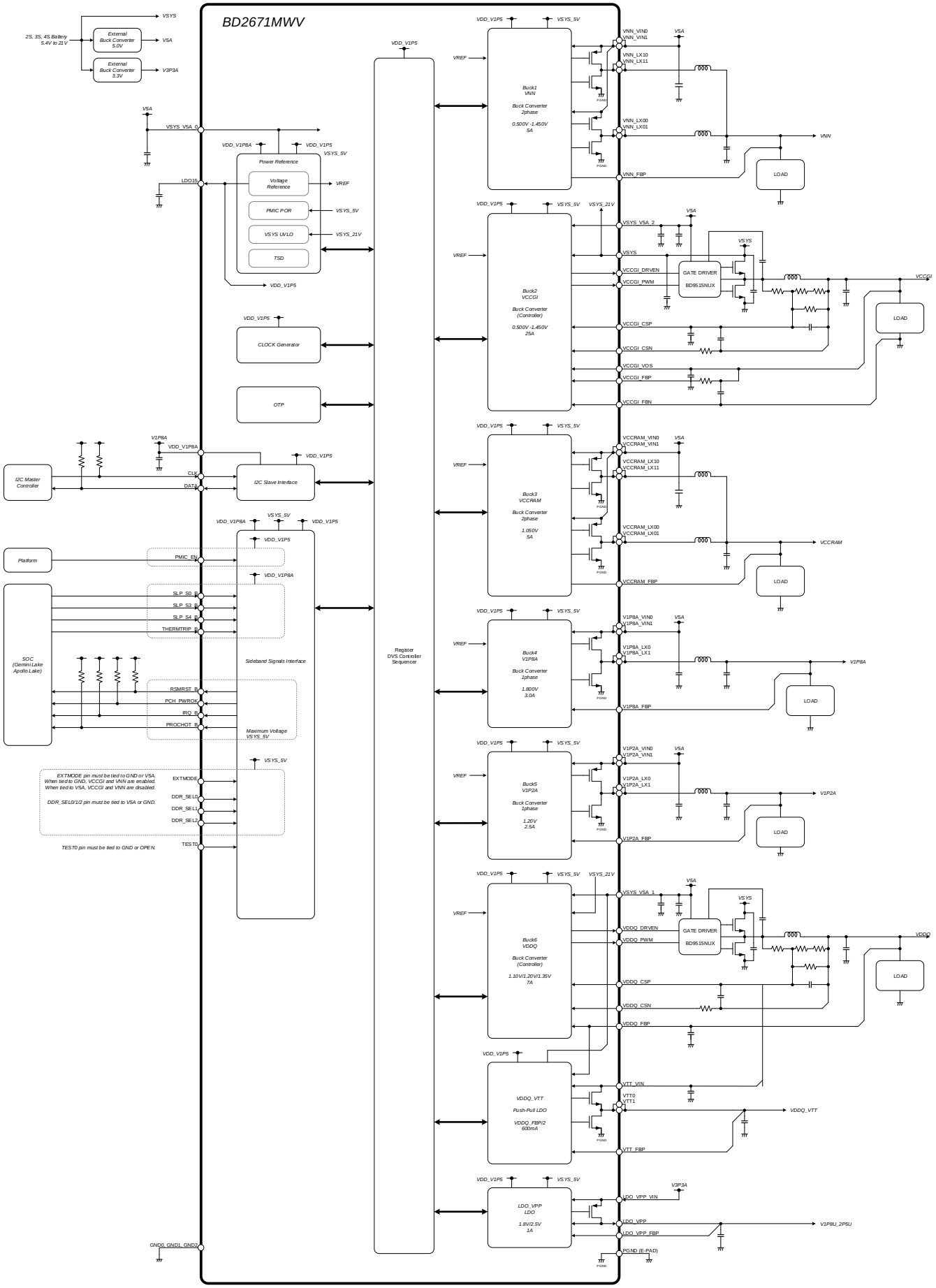
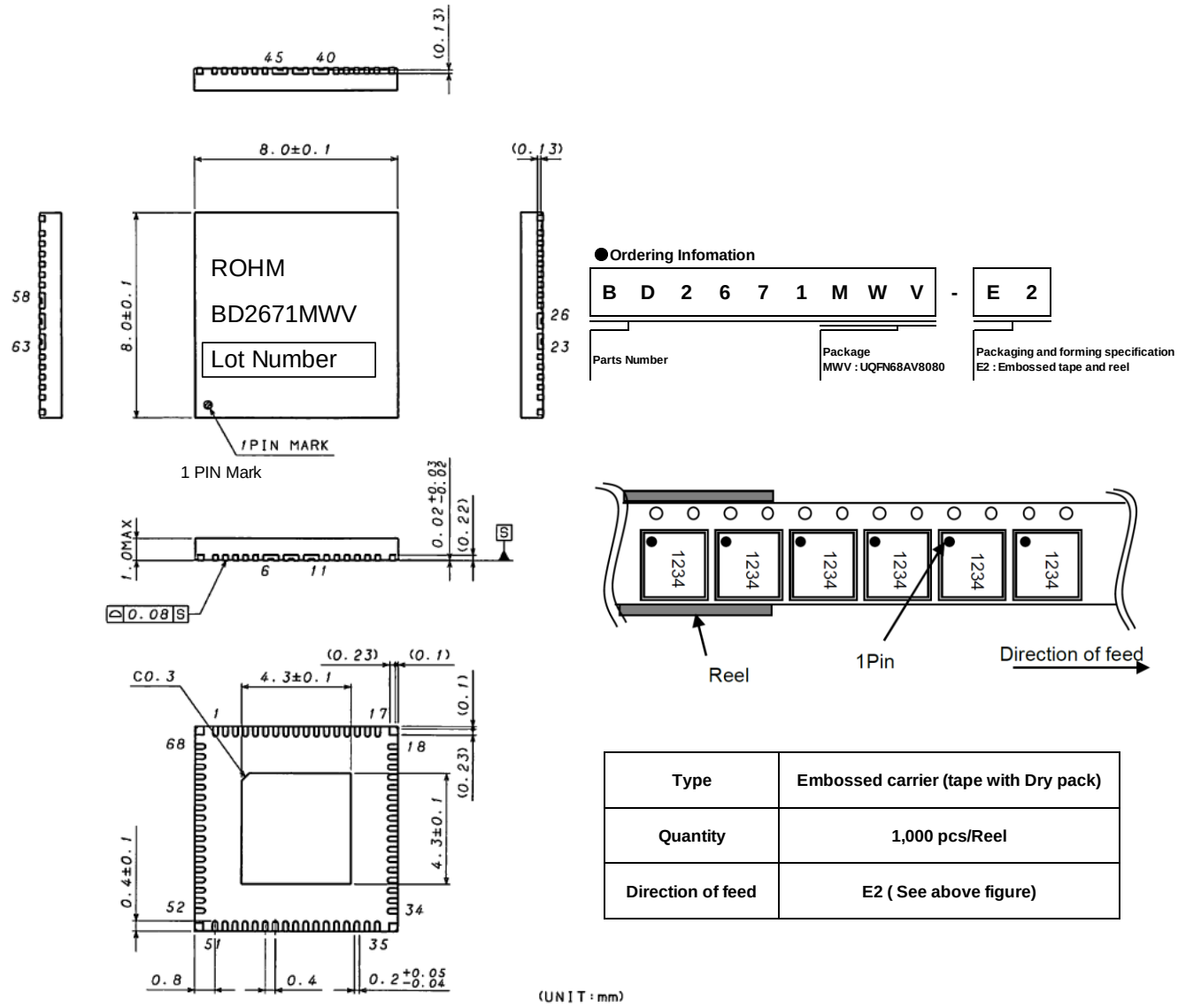


Figure 1-1 Typical Application Circuit

1-3 Package Dimension

UQFN68AV8080



Type	Embossed carrier (tape with Dry pack)
Quantity	1,000 pcs/Reel
Direction of feed	E2 (See above figure)

Figure 1-2 Package Dimension

1-4 Thermal Infomation

Table 1-2 Thermal Resistance (UQFN68AV8080)

Parameter	Symbol	Thermal Resistance (typ)	Unit
UQFN68AV8080 Thermal Resistance[*1]			
Junction to ambient thermal resistance	θ_{JA}	28.1[*3]	ºC/W
Junction to top characterization parameter[*2]	Ψ_{JT}	6[*3]	ºC/W

Note 1: Based on JESD51-2A (Still-Air)
Note 2: The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside furface of the componenst package.
Note 3: Using a PCB board based on JESD51-9. Layer number of measurement board is 4 layers. The material is FR-4. Boad size is 114.3mm x 76.2mm x 1.6mmt.

1-5 Pin Configuration

< TOP VIEW >

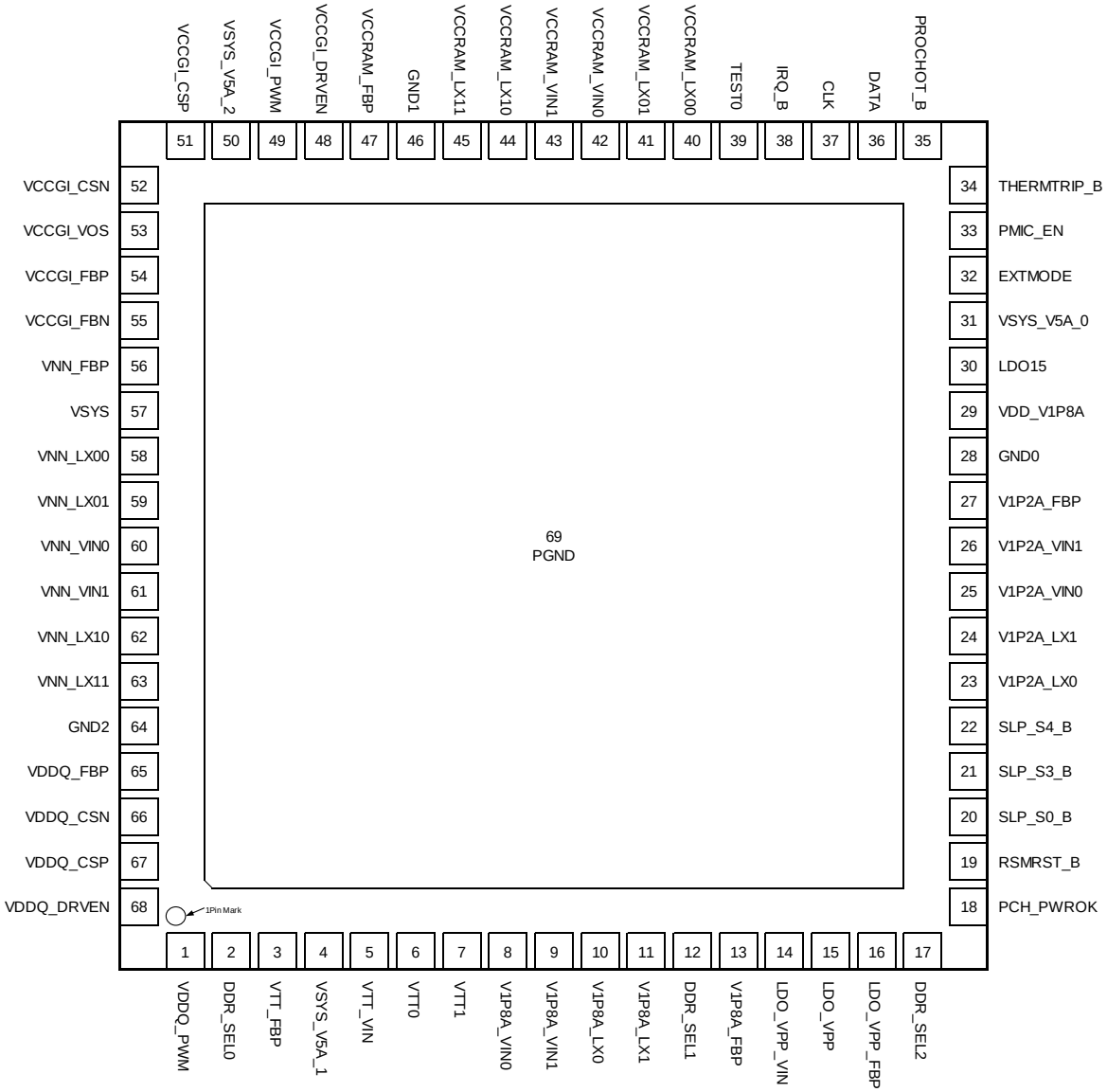


Figure 1-3 Pin Configuration

1-6 Pin List

Table 1-3 Pin List

Pin	Pin Name	Dir	Pin Description	PWR/GND	Voltage Level from	PIN I/O Circuit
1	VDDQ_PWM	O	VDDQ PWM output for external driver	-	5V (VSYS_V5A_1)	O
2	DDR_SEL0	I	Configuration pin for VDDQ and LDO_VPP nominal voltage level and Boot/OFF Sequence	-	5V (VSYS_V5A_0)	A
3	VTT_FBP	I	VDDQ_VTT sense feedback	-	VDDQ/2	I
4	VSYS_V5A_1	I	5V power supply for VDDQ and VDDQ_VTT	PWR	5V	J
5	VTT_VIN	I	VDDQ_VTT Vin input	PWR	VDDQ	H
6	VTT0	O	VDDQ_VTT output	-	VDDQ/2	H
7	VTT1	O				
8	V1P8A_VIN0	I	V1P8A Vin input	PWR	5V	F
9	V1P8A_VIN1	I				
10	V1P8A_LX0	O	V1P8A Switch node	-	V1P8A_VIN	F
11	V1P8A_LX1	O				
12	DDR_SEL1	I	Configuration pin for VDDQ and LDO_VPP nominal voltage level and Boot/OFF Sequence	-	5V (VSYS_V5A_0)	A
13	V1P8A_FBP	I	V1P8A sense feedback	-	V1P8A	G
14	LDO_VPP_VIN	I	LDO_VPP Vin input	PWR	V3P3A	R
15	LDO_VPP	O	LDO_VPP output		LDO_VPP	R
16	LDO_VPP_FBP	I	LDO_VPP sense feedback		LDO_VPP	S
17	DDR_SEL2	I	Configuration pin for VDDQ and LDO_VPP nominal voltage level and Boot/OFF Sequence	-	5V (VSYS_V5A_0)	A
18	PCH_PWROK	O (OD)	Open drain output asserted when all PMIC rail's power are good	-	5V tolerant *1	D
19	RSMRST_B	O (OD)	Always ON rail Power Good pin	-	5V tolerant *1	D
20	SLP_S0_B	I	Power state control pin	-	VDD_V1P8A (5V tolerant *1)	B
21	SLP_S3_B	I	Power state control pin	-	VDD_V1P8A (5V tolerant *1)	B
22	SLP_S4_B	I	Power state control pin	-	VDD_V1P8A (5V tolerant *1)	B
23	V1P2A_LX0	O	V1P2A Switch node	-	V1P2A_VIN	F
24	V1P2A_LX1	O				
25	V1P2A_VIN0	I	V1P2A Vin input	PWR	5V	F
26	V1P2A_VIN1	I				
27	V1P2A_FBP	I	V1P2A sense feedback	-	V1P2A	G
28	GND0	I	Analog Ground	AGND	-	-
29	VDD_V1P8A	I	1.8V input pin	PWR	V1P8A	J
30	LDO15	O	Power supply for PMIC internal use	-	1.5V	K
31	VSYS_V5A_0	I	5V power supply for PMIC reference	PWR	5V (VSYS_V5A_0)	J
32	EXTMODE	I	Configuration pin for VNN and VCCGI external mode	-	5V (VSYS_V5A_0)	A
33	PMIC_EN	I	PMIC enable	-	5V (VSYS_V5A_0)	E
34	THERMTRIP_B	I	Thermal shutdown input pin	-	VDD_V1P8A (5V tolerant *1)	B
35	PROCHOT_B	O (OD)	Indicate PMIC thermal events	-	5V tolerant *1	D
36	DATA	I/O	I2C data	-	VDD_V1P8A (5V tolerant *1)	C
37	CLK	I	I2C clock	-	VDD_V1P8A (5V tolerant *1)	B

Pin	Pin Name	Dir	Pin Description	PWR/GND	Voltage Level from	PIN I/O Circuit
38	IRQ_B	O (OD)	PMIC active low interrupt pin	-	5V tolerant *1	D
39	TEST0	I	Test pin for PMIC (Tie to GND or OPEN)	-	5V	A
40	VCCRAM_LX00	O	VCCRAM Switch node 0	-	VCCRAM_VIN	F
41	VCCRAM_LX01	O				
42	VCCRAM_VIN0	I	VCCRAM Vin input	PWR	5V	F
43	VCCRAM_VIN1	I				
44	VCCRAM_LX10	O	VCCRAM Switch node 1	-	VCCRAM_VIN	F
45	VCCRAM_LX11	O				
46	GND1	I	Analog Ground	AGND	-	-
47	VCCRAM_FBP	I	VCCRAM sense feedback	-	VCCRAM	G
48	VCCGI_DRVEN	O	VCCGI output to enable external driver	-	VSYS_V5A_2	O
49	VCCGI_PWM	O	VCCGI PWM output for external driver	-	VSYS_V5A_2	O
50	VSYS_V5A_2	I	5V power supply for VCCGI	PWR	5V	J
51	VCCGI_CSP	I	VCCGI positive current sense	-	5V	N
52	VCCGI_CSN	I	VCCGI negative current sense	-	5V	M
53	VCCGI_VOS	I	VCCGI output voltage sense	-	VCCGI	G
54	VCCGI_FBP	I	VCCGI positive feedback	-	VCCGI	Q
55	VCCGI_FBN	I	VCCGI negative feedback	-	-	P
56	VNN_FBP	I	VNN sense feedback	-	VDDQ	G
57	VSYS	I	System voltage detection & voltage sense	-	21V	L
58	VNN_LX00	O	VNN Switch Node 0	-	VNN_VIN	F
59	VNN_LX01	O				
60	VNN_VIN0	I	VNN VIN input	PWR	5V	F
61	VNN_VIN1	I				
62	VNN_LX10	O	VNN Switch Node 1	-	VNN_VIN	F
63	VNN_LX11	O				
64	GND2	I	Analog Ground	AGND	-	-
65	VDDQ_FBP	I	VDDQ sense feedback	-	VDDQ	G
66	VDDQ_CSN	I	VCCGI negative current sense	-	5V	M
67	VDDQ_CSP	I	VCCGI positive current sense	-	5V	N
68	VDDQ_DRVEN	O	VDDQ output to enable external driver	-	5V (VSYS_V5A_1)	O
69	PGND	I	Power Ground	PGND	-	F

Note 1: “5V tolerant” means that it is possible to exceed the VSYS_V5A voltage level.

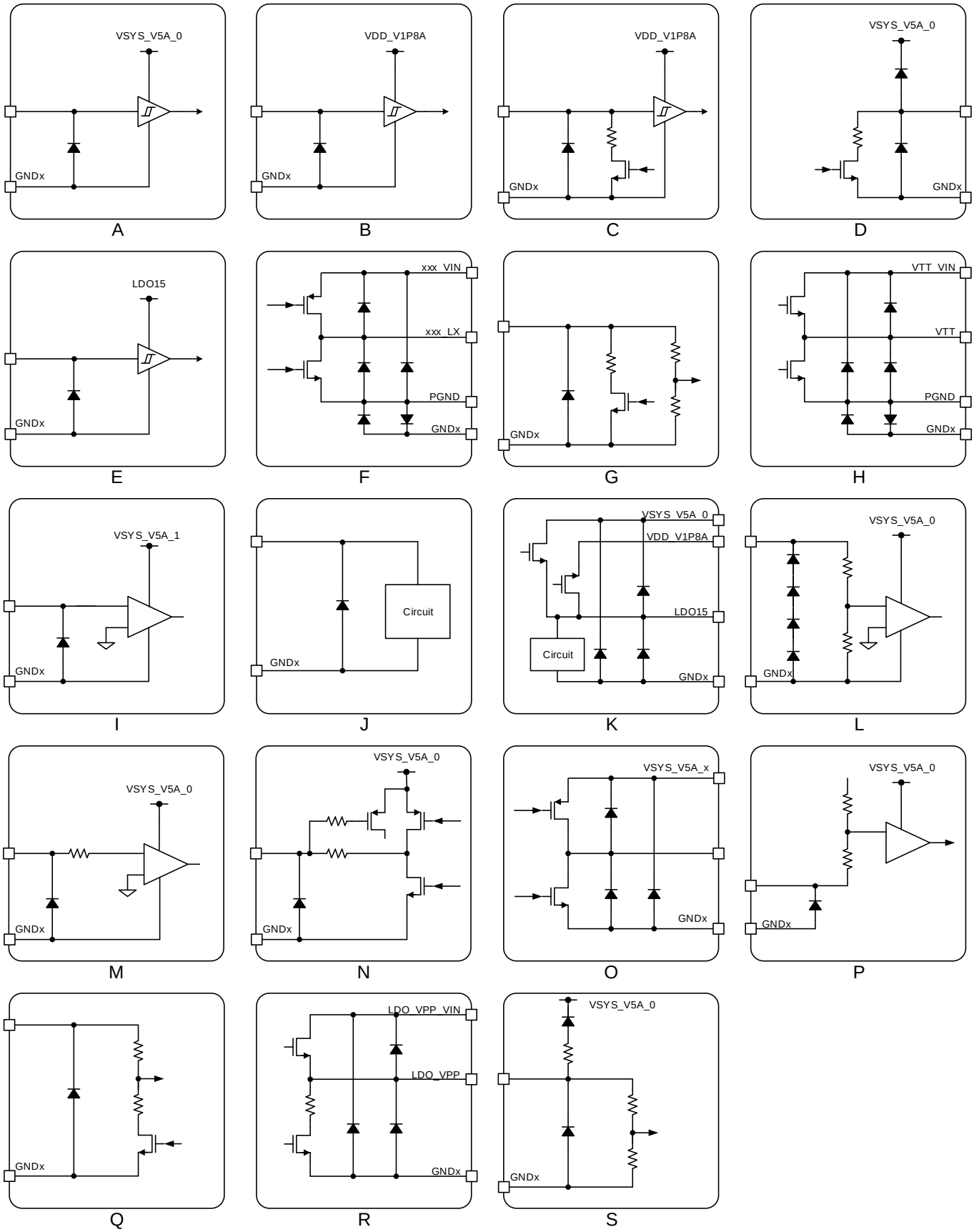


Figure 1-4 Terminal Equivalent Circuit

1-7 Absolute Maximum Ratings (Ta=25°C)

Table 1-4 Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Rating		Unit
		Min	Max	
Voltage range in PIN : VSYS	VCC1	-0.3	28	V
Voltage range in PINs : VSYS_V5A_0, VSYS_V5A_1, VSYS_V5A_2, VNN_VIN0, VNN_VIN1, VCCRAM_VIN0, VCCRAM_VIN1, V1P8A_VIN0, V1P8A_VIN1, V1P2A_VIN0, V1P2A_VIN1, VTT_VIN, LDO_VPP_VIN	VCC2	-0.3	6.0	V
Voltage range in PIN : VDD_V1P8A	VCC3	-0.3	3.6	V
Voltage range in PIN : LDO15	VCC4	-0.3	2.1	V
Voltage range in PINs : VNN_LX00, VNN_LX01, VNN_LX10, VNN_LX11, VCCRAM_LX00, VCCRAM_LX01, VCCRAM_LX10, VCCRAM_LX11, V1P8A_LX0, V1P8A_LX1, V1P2A_LX0, V1P2A_LX1	VLX	-1.0 (DC) -2.0 (10ns)	7.0	V
Voltage range in PINs : DDR_SEL0, DDR_SEL1, DDR_SEL2, PROCHOT_B, VTT, VTT_FBP, SLP_S0_B, SLP_S3_B, SLP_S4_B, LDO_VPP, PMIC_EN, EXTMODE, CLK, DATA, THERMTRIP_B, VCCGI_VOS, VCCGI_CSN, VCCGI_CSP, VCCGI_PWM, VCCGI_DRVEN, VDDQ_CSN, VDDQ_CSP, VDDQ_PWM, VDDQ_DRVEN, IRQ_B, PCH_PWROK, RSMRST_B	VPIN1	-0.3	6.0	V
Voltage range in PINs : VNN_FBP, VCCGI_FBP, VCCGI_FBN, VCCRAM_FBP, V1P8A_FBP, V1P2A_FBP, VDDQ_FBP	VPIN2	-0.3	2.1	V
Maximum Jumction Temperature	Tjmax	-	150	°C
Storage Temperature	Tstg	-50	150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.

1-8 Operating Ratings

Table 1-5 Operating Ratings

Parameter	Symbol	Limit			Unit
		Min	Typ	Max	
VSYS Supply Voltage	VSYS	5.4	12.6	21	V
VSYS_V5A Supply Voltage	VSYS_V5A	4.5	5.0	5.25	V
VDD_V1P8A Supply Voltage	VDD_V18	1.71	1.80	1.89	V
VPP_VIN Supply Voltage	VPP_VIN	3.1	3.3	3.6	V
Operating Temperature Range	TOPR	-40	25	85	°C

1-9 ESD

Table 1-6 ESD

Parameter	Minimum Limit	Unit
Human Body Model (HBM)	+/-2000	V
Charged Device Model (CDM)	+/-500	V

2 Power References and Thermal Monitoring thresholds

2-1 Current Consumption

The current consumption of each state is shown Table 2-1.

Table 2-1 Current Consumption

Unless otherwise specified, Ta=25°C, VSYS=12.6V, VSYS_V5A_x=VNN_VINx=VCCRAM_VINx=V1P8A_VINx=V1P2A_VINx=5.0V, VDD_V1P8A=V1P8A, VTT_VIN=VDDQ, DDR_SEL2,1,0=(LLL), EXTMODE=L, PMIC_EN=L, SLP_S0_B=L, SLP_S3_B=L, SLP_S4_B=L, THERMTRIP_B=H, All VRs no load.

Parameter	Symbol	Limit.			Unit	Remarks
		Min	Typ	Max		
Current Consumption : VSYS						
VSYS Current Consumption	I_{DDVSYS}	-	15	-	μA	
Current Consumption : VSYS_V5A_x, VNN_VINx, VCCRAM_VINx, V1P8A_VINx, V1P2A_VINx						
PMIC G3 state Current Consumption	I_{DDG3}	-	30	-	μA	
S4/S5 state Current Consumption	I_{DDS4}	-	60	-	μA	PMIC_EN=H
S3 state Current Consumption	I_{DDS3}	-	285	-	μA	PMIC_EN=H SLP_S4_B=H
S0IX state Current Consumption	I_{DDS0IX}	-	285	-	μA	PMIC_EN=H, SLP_S3_B=H, SLP_S4_B=H
S0 state Current Consumption	I_{DDS0}	-	685	-	μA	PMIC_EN=H, SLP_S0_B=H, SLP_S3_B=H, SLP_S4_B=H,

2-2 Power Reference and Detectors

BD2671MWV incorporates reference of internal use and 2 voltage detectors of VSYS and VSYS_V5A and 2 thermal detectors.

2-2-1 Power Reference and Detectors Block Diagram

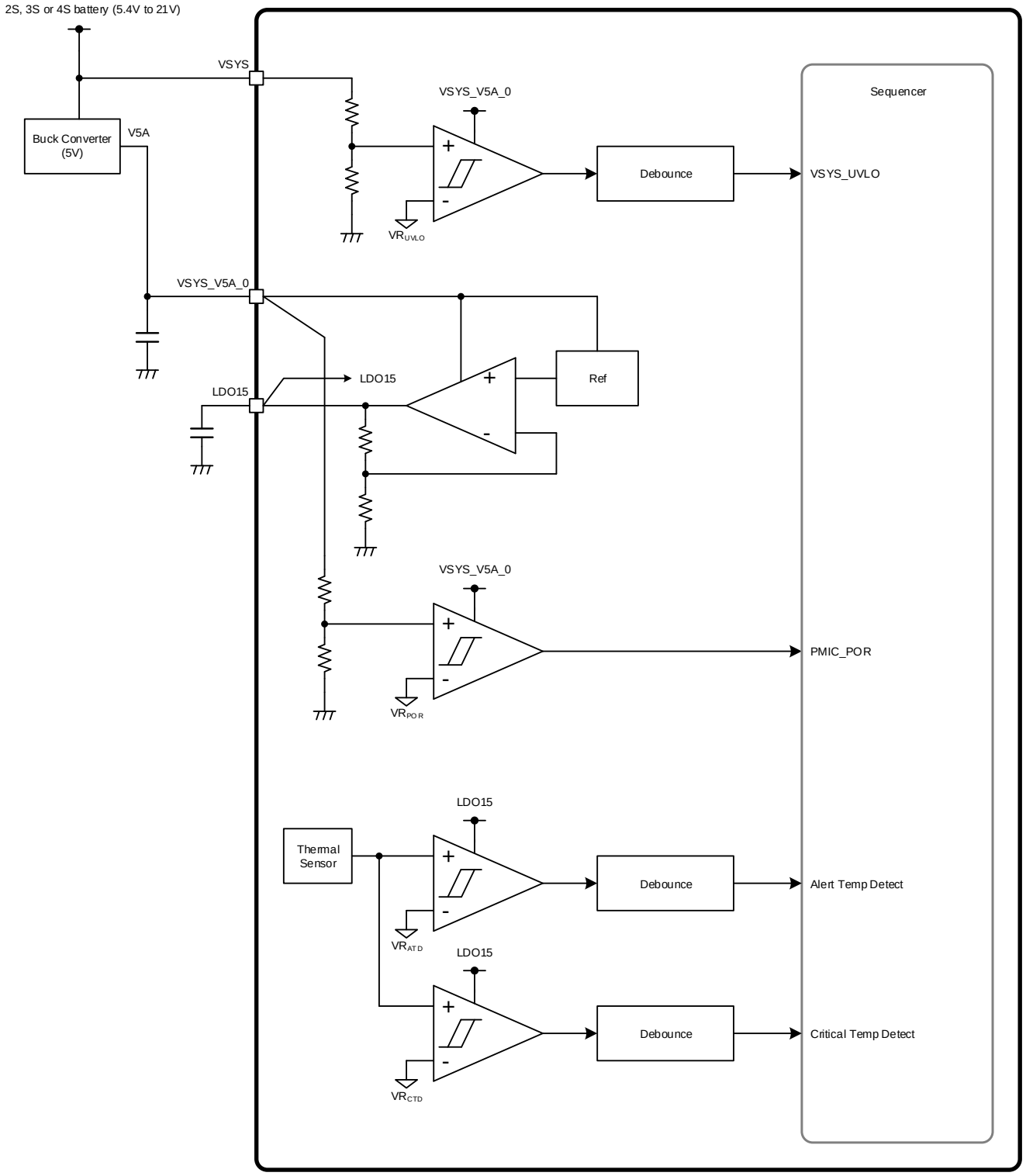


Figure 2-1 Power Reference and Detectors Block Diagram

2-2-2 Power Reference and Detectors Electrical Characteristics

Table 2-2 Power Reference and Detectors Electrical Characteristics

Unless otherwise specified, Ta=25°C, VSYS=12.6V, VSYS_V5A_x=5.0V

Parameter	Symbol	Limit.			Unit	Remarks
		Min	Typ	Max		
PMIC POR (PMIC Power On Reset Detector)						
Release Voltage	V_{UVLORL}	-	4.000	-	V	VSYS_V5A_0=Sweep up
Detect Voltage	V_{UVLODT}	3.800	3.900	4.000	V	VSYS_V5A_0=Sweep down
Hysteresis Voltage	$V_{UVLOHYS}$	-	100	-	mV	
VSYS UVLO (VSYS Voltage Detector)						
Release Voltage	V_{VDETRL}	-	5.600	-	V	VSYS=Sweep up
Detect Voltage	V_{VDETDT}	5.265	5.400	5.535	V	VSYS=Sweep down
Hysteresis Voltage	$V_{VDETHYS}$	-	200	-	mV	
PMIC Die Alert Temperature Detector (PROCHOT_B assert factor)						
Detect Temperature	T_{TAD}	-	130	-	ºC	Die Temperature=Sweep up
PMIC Die Critical Temperature Detector (Thermal Shutdown factor)						
Detect Temperature	T_{CTD}	-	150	-	ºC	Die Temperature=Sweep up
Power Reference						
LDO15 Output Voltage	V_{LDO15}	-	1.550	-	V	

3 Voltage Regulators

3-1 Voltage Regulators OverView

BD2671MWV incorporates 4 buck converters (VNN, VCCRAM, V1P8A and V1P2A), 2 buck controllers (VCCGI and VDDQ), 1 push-pull linear regulator (VDDQ_VTT) and 1 linear regulator (LDO_VPP).

3-1-1 Voltage Regulators Power Map

Voltage power map is shown in Figure 3-1.

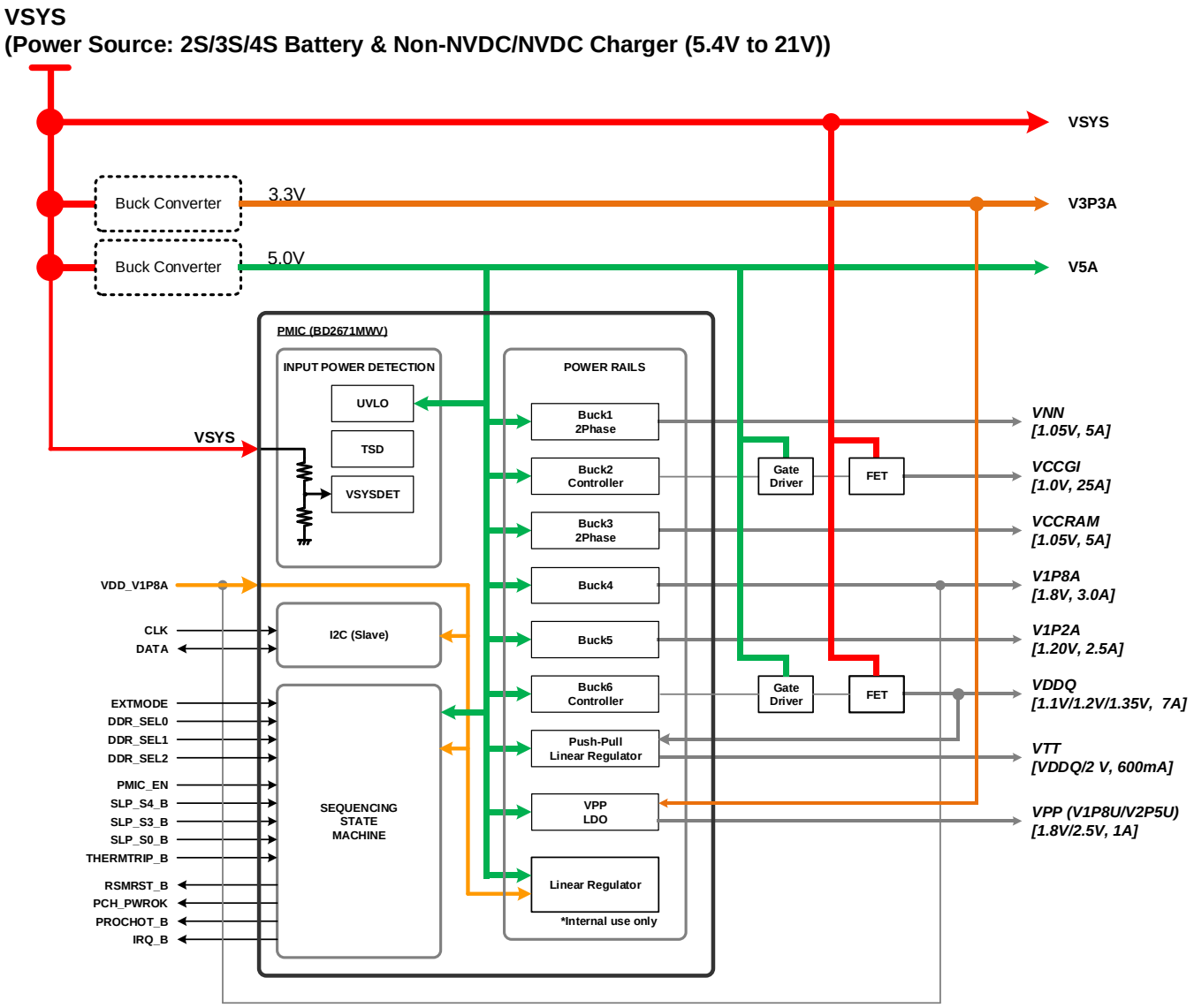


Figure 3-1 Power Map

3-1-2 Output Voltage and Maximum Current

Every voltage rail has an integrated Over Current Protection (OCP) function. If the output current exceeds the OCP threshold, it will limit the current to protect BD2671MWV damaged from heat. OCP threshold for regulators are ≥ 1.3 x Imax.

Table 3-1 Voltage Rails Output Voltage List

Voltage Rail	Type	Phase	Input Voltage	Output Voltage	Max Current	Over Current Protection Min [mA]
BUCK1 VNN	SMPS with internal FETs	2	5V	0.500V – 1.450V 10mV/step (DVS)	5000mA	6500mA
BUCK2 VCCGI	SMPS with external power stage	1	Internal 5V External 5.4V to 21V	0.500V – 1.450V 10mV/step (DVS)	25000mA	35500mA *1 (Typ)
BUCK3 VCCRAM	SMPS with internal FETs	2	5V	1.050V	5000mA	6500mA
BUCK4 V1P8A	SMPS with internal FETs	1	5V	1.800V	3000mA	3900mA
BUCK5 V1P2A	SMPS with internal FETs	1	5V	1.200V	2500mA	3250mA
BUCK6 VDDQ	SMPS with external power stage	1	Internal 5V External 5.4V to 21V	1.100V / 1.200V / 1.350V	7000mA	16000mA *2 (Typ)
LDO_VPP	Linear regulator	-	3.3V	1.800V / 2.500V	1000mA	1100mA
VDDQ_VTT	Push-Pull linear regulator	-	VDDQ	VDDQ/2	600mA	780mA

Note 1: It is capable of changing the VCCGI OCP threshold level by the I2C register (refer to Section “4-2-9 VCCGI OCP and Switching Frequency Adjust Registers”).
Note 2: It is capable of changing the VDDQ OCP threshold level by the I2C register (refer to Section “4-2-11 VDDQ OCP and Switching Frequency Adjust Registers”).

3-2 Buck1 - VNN

VNN is a high-efficiency 2 multi-phase buck converter with integrated FETs that converts the V5A voltage (5V) to a regulated voltage. This voltage regulator can dynamically change its output voltage setting using the I2C interface. VNN output voltage range is from 0.500V to 1.450V (10mV/step). The output voltage slew rate while ramping up/down is 3.125mV/µsec.
VNN control registers are shown in Section “4-2-2 VNN & VCCGI Control Registers”.

3-2-1 VNN Block Diagram

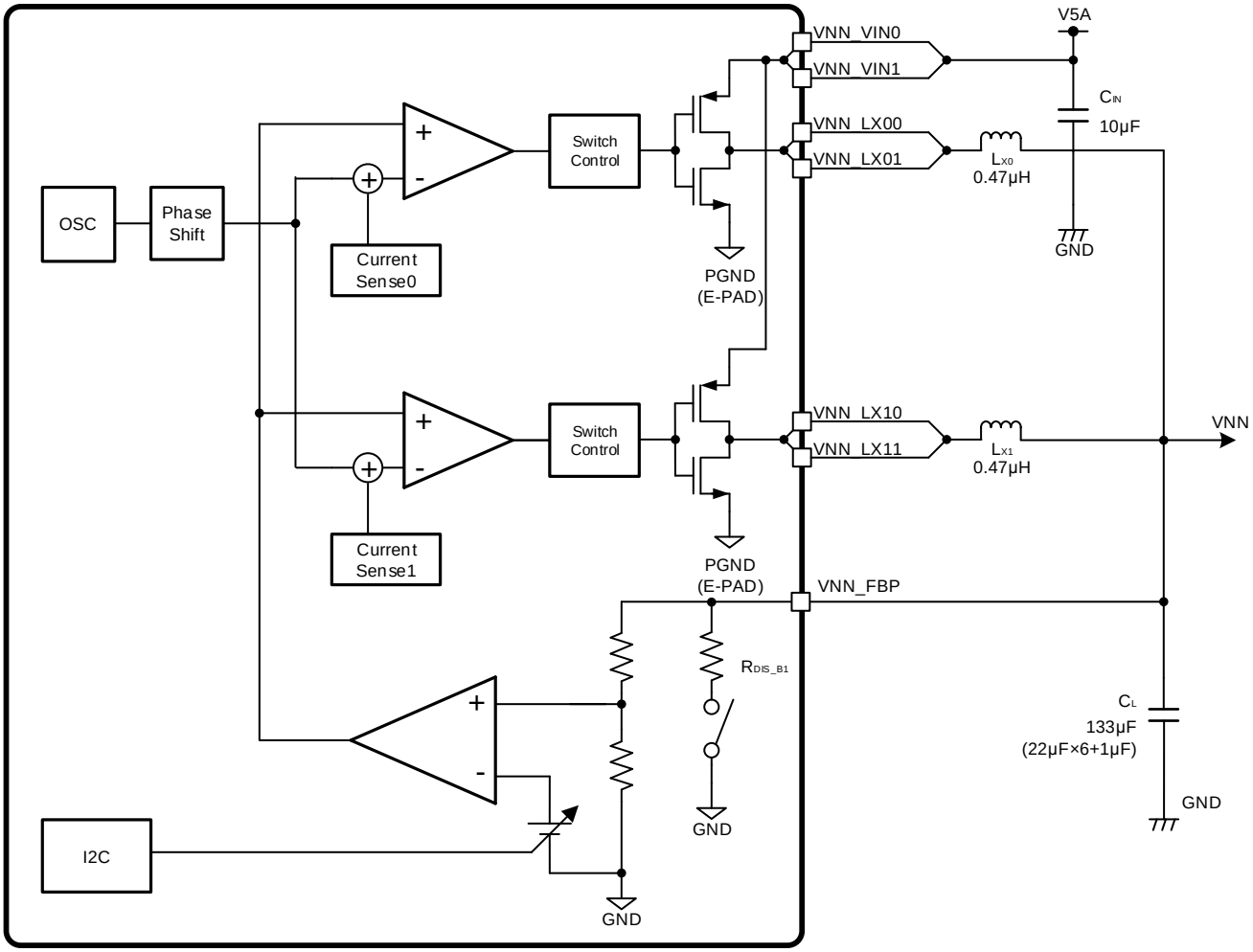


Figure 3-2 VNN Block Diagram

3-2-2 VNN Electrical Characteristics

Table 3-2 VNN Electrical Characteristics

Unless otherwise specified, Ta=25°C, VSYS_V5A_x=VNN_VINx=5.0V, BUCK1_VID=1.050V setting, C_L=133µF (22µFx6+1µF), L_{X0}=L_{X1}=0.47µH, C_{IN}=10µF

Parameter	Symbol	Limit.			Unit	Remarks
		Min	Typ	Max		
Switching Frequency 1	f_{SW1_B1}	-	1.0	-	MHz	PWM mode, BUCK1_VID<0.640V
Switching Frequency 2	f_{SW2_B1}	-	2.0	-	MHz	PWM mode, BUCK1_VID≥0.640V
Output Voltage VID=1.05V	V_{O1_B1}	1.039	1.050	1.061	V	PWM mode
Ripple Voltage *1	V_{RP_B1}	-	5	21	mV_{P-P}	PFM mode, I_{OUT}=10mA
Transient Droop Voltage 1 *1 *2	V_{DRP_B1}	-	-	42	mV	T_R=1000ns, I_{OUT}=1500mA to 5000mA
Transient Overshoot Voltage 1 *1 *2	V_{OVS_B1}	-	-	42	mV	T_F=1000ns, I_{OUT}=5000mA to 1500mA
Maximum Output Current *1	I_{MAX_B1}	5000	-	-	mA	
Efficiency 1 *1	Eff_{1_B1}	-	80	-	%	I_{OUT}=100mA
Efficiency 2 *1	Eff_{2_B1}	-	84	-	%	I_{OUT}=300mA
Output Voltage slew Rate *1	SR_{B1}	2.5	3.125	3.75	mV/µs	V_{OUT}=20% to 80% BUCK1_VID=0.5V to 1.05V and 1.05V to 0.5V
Discharge Resistance 1	R_{DIS1_B1}	-	100	-	Ω	BUCK1_DIS[1:0]=01
Discharge Resistance 2	R_{DIS2_B1}	-	200	-	Ω	BUCK1_DIS[1:0]=10
Discharge Resistance 3	R_{DIS3_B1}	-	500	-	Ω	BUCK1_DIS[1:0]=11
Load Capacitance *3	C_{LMIN_B1}	-	133	-	µF	

Note 1: These parameters are determined as reference data without pre-shipping inspection.
Note 2: Including ripple voltage and load regulation.
Note 3: The effective load capacitance value considering accuracy, temperature characteristic and DC bias characteristic of output capacitors should not be less than 95µF.

3-3 Buck2 – VCCGI

VCCGI is a high-efficiency buck controller that converts the VSYS voltage (5.4V to 21V) to a regulated voltage. This voltage regulator can dynamically change its output voltage setting using the I2C interface. VCCGI output voltage range is from 0.500V to 1.450V (10mV/step). The output voltage slew rate while ramping up/down is 3.125mV/usec. VCCGI control registers are shown in Section “4-2-2 VNN & VCCGI Control Registers”.

3-3-1 VCCGI Block Diagram

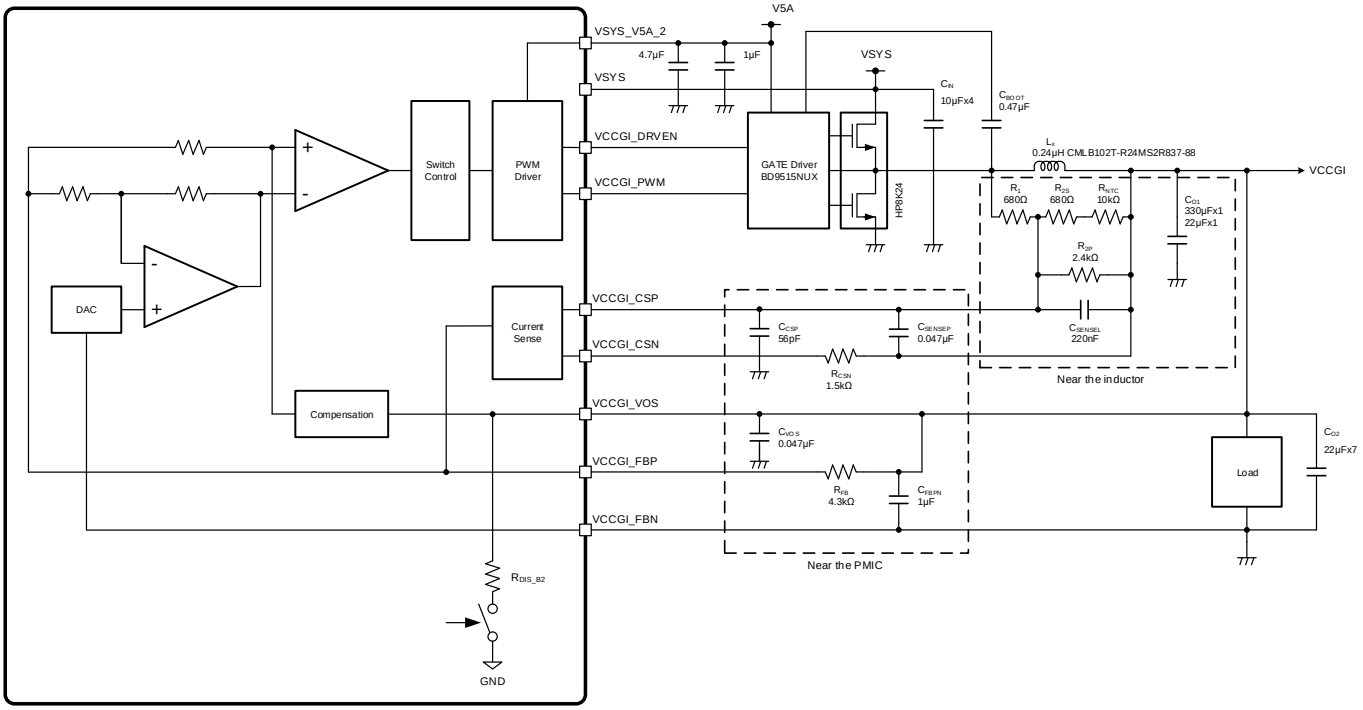


Figure 3-3 VCCGI Block Diagram

3-3-2 VCCGI_PWM and VCCGI_DRVEN

VCCGI_PWM and VCCGI_DRVEN pins are signals used for controlling the external gate driver or DrMOS.

VCCGI_PWM is a pulse width modulated three state output controlling the external gate driver. When the output is high (VSYS_V5A_2 level), the external gate driver controls to turn ON the high-side FET. When the output is low (GND level), the external gate driver controls to turn ON the low-side FET. When the output level is at the middle (half of VSYS_V5A_2), the external gate driver controls to go into diode mode (both high and low side FETs are turned OFF).
BD2671MWV recommends using BD9515NUX or any other functional compatible driver solution.

VCCGI_DRVEN is an output enable to the external gate driver. When the output is high (VSYS_V5A_2 level), the external gate driver turns ON. When the output is low (GND level), the external gate driver turns OFF.

Table 3-3 VCCGI_DRVEN and VCCGI_PWM Truth Table

VCCGI_DRVEN	VCCGI_PWM	High-side FET Control	Low-side FET Control
L	Middle of VSYS_V5A_2	OFF	OFF
H	Middle of VSYS_V5A_2	OFF	OFF
H	L	OFF	ON
H	H	ON	OFF

The timing chart of VCCGI_DRVEN and VCCGI_PWM is shown on Figure 3-4.

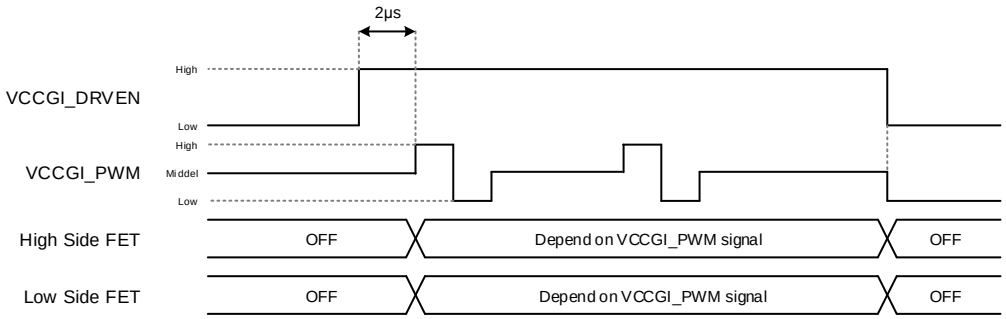


Figure 3-4 VCCGI_DRVEN and VCCGI_PWM Timing Chart

3-3-3 Inductor Current Sensing

The VCCGI_CSP and VCCGI_CSN pins are the input to the differential current sense amplifier. The positive current sense (VCCGI_CSP) pin is connected to the non-inverting input, and the negative current sense (VCCGI_CSN) pin is connected to the inverting input. Figure 3-3 shows the circuit for monitoring the current of the power stage using the inductor DCR. BD2671MWV recommends using an inductor which DCR is larger than 1mΩ.

3-3-4 VCCGI Electrical Characteristics

Table 3-4 VCCGI Electrical Characteristics

Unless otherwise specified, Ta=25°C, VSYS=12.6V, VSYS_V5A_x=5.0V, BUCK2_VID=1.000V setting, C_L=330µF+22µFx8, L_X=0.24µH, C_{IN}=10µFx4

Parameter	Symbol	Limit.			Unit	Remarks
		Min	Typ	Max		
Switching Frequency	f_{SW_B2}	-	0.66	-	MHz	PWM mode, VCCGI_CLKSEL[1:0]=01
Output Voltage VID=1.00V	V_{O1_B2}	0.990	1.000	1.010	V	PWM mode
PWM Output High Level	V_{PWMH_B2}	4.8	-	-	V	I_{OUT}=1mA
PWM Output Low Level	V_{PWML_B2}	-	-	0.2	V	I_{IN}=1mA
PWM Tri-State Leakage	I_{PWMZ_B2}	-1	-	1	uA	V_{IN}=2.5V
DRVEN Output High Level	V_{DRVENH_B2}	4.8	-	-	V	I_{OUT}=1mA
DRVEN Output Low Level	V_{DRVENL_B2}	-	-	0.2	V	I_{IN}=1mA
Min On Time	Ton_{MIN_B2}	40	-	-	ns	
Min Off Time	$Toff_{MIN\_B2}$	40	-	-	ns	
Output Voltage slew Rate *1	SR_{B2}	2.5	3.125	3.75	mV/µs	VOUT=20% to 80% of Target Voltage BUCK2_VID=0.5V to 1.00V and 1.00V to 0.5V
Maximum Output Current *1	I_{MAX_B2}	25	-	-	A	VCCGI_LIMSEL[2:0]=100
Discharge Resistance 1	R_{DIS1_B2}	-	100	-	Ω	BUCK2_DIS[1:0]=01
Discharge Resistance 2	R_{DIS2_B2}	-	200	-	Ω	BUCK2_DIS[1:0]=10
Discharge Resistance 3	R_{DIS3_B2}	-	500	-	Ω	BUCK2_DIS[1:0]=11

Note 1: These parameters are determined as reference data without pre-shipping inspection.

3-4 Buck3 – VCCRAM

VCCRAM is a high-efficiency 2 multi-phase buck converter with integrated FETs that converts the V5A voltage (5V) to a regulated voltage of 1.050V. The output voltage is possible to be changed between 1.000V to 1.100V through the I2C interface. VCCRAM control register is shown in Section “4-2-3 VCCRAM, V1P8A, V1P2A Control Registers”.

VCCRAM can always be kept OFF by the OTP setting and VCCRAM can be supplied from VNN as 1.050V default. When using the VCCRAM merged mode with VNN, no external components are required for VCCRAM, and all VCCRAM load should be connected to VNN. Note that any fine tuning or on-the-fly voltage change on VNN would reflect the VCCRAM load in such situations.

3-4-1 VCCRAM Block Diagram

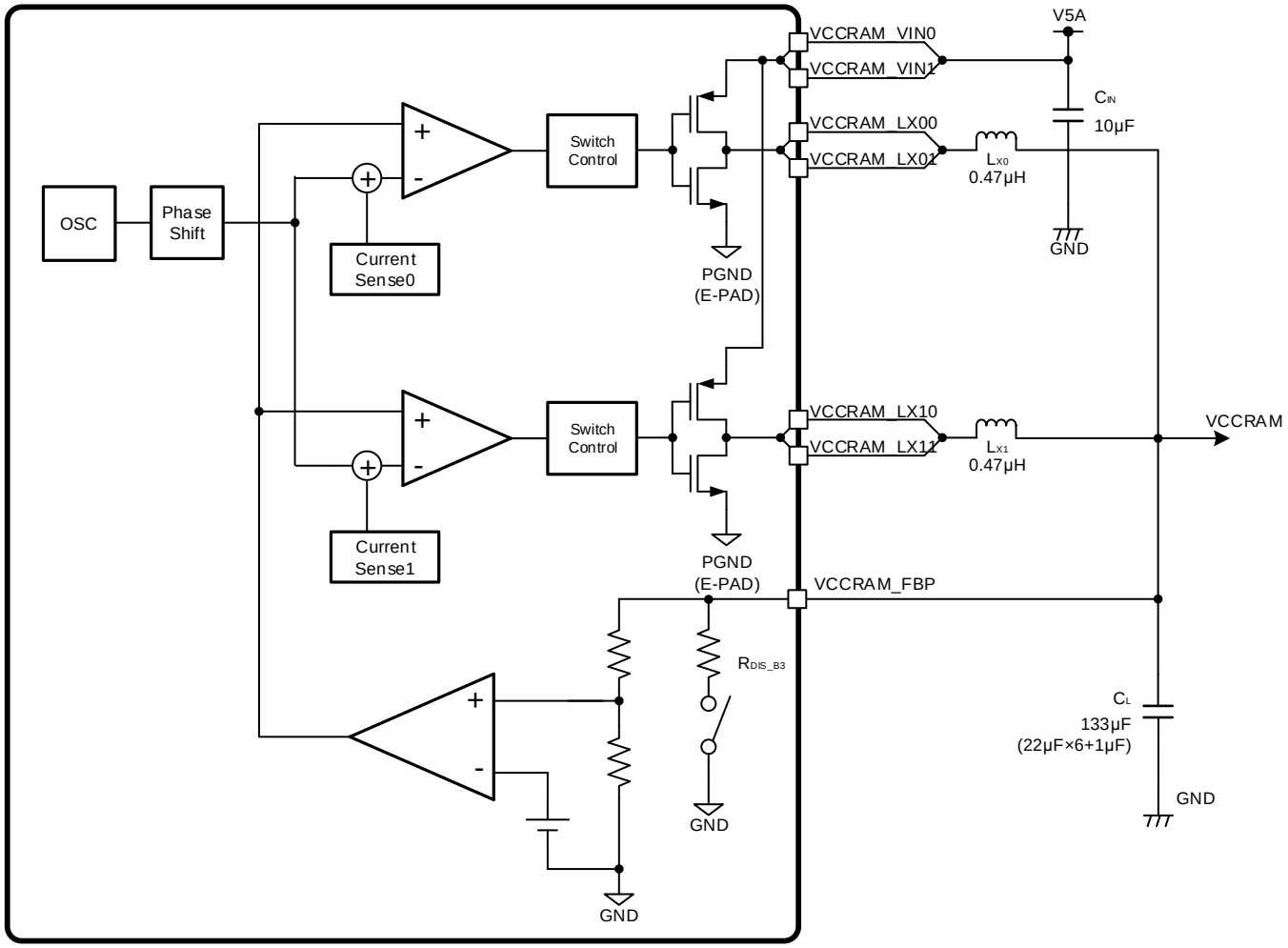


Figure 3-5 VCCRAM Block Diagram

3-4-2 VCCRAM Electrical Characteristics

Table 3-5 VCCRAM Electrical Characteristics

Unless otherwise specified, Ta=25°C, VSYS=12.6V, VSYS_V5A_x=VCCRAM_VINx=5.0V, BUCK3_VID=1.050V setting, C_L=133µF (22µFx6+1µF), L_{X0}=L_{X1}=0.47µH, C_{IN}=10µF

Parameter	Symbol	Limit.			Unit	Remarks
		Min	Typ	Max		
Switching Frequency	f_{SW_B3}	-	2.0	-	MHz	PWM mode
Output Voltage 1	V_{O1_B3}	1.039	1.050	1.061	V	PWM mode, BUCK3_VID[1:0]=11
Output Voltage 2	V_{O2_B3}	1.089	1.100	1.111	V	PWM mode, BUCK3_VID[1:0]=00
Output Voltage 3	V_{O3_B3}	1.064	1.075	1.086	V	PWM mode, BUCK3_VID[1:0]=01
Output Voltage 4	V_{O4_B3}	0.990	1.000	1.010	V	PWM mode, BUCK3_VID[1:0]=10
Transient Droop Voltage 1 *1 *2	V_{DRP_B3}	-	-	42	mV	Slew Rate=2.5A/µs, I_{OUT}=900mA to 5000mA
Transient Overshoot Voltage 1 *1 *2	V_{OVS_B3}	-	-	42	mV	Slew Rate=2.5A/µs, I_{OUT}=5000mA to 900mA
Maximum Output Current *1	I_{MAX_B3}	5000	-	-	mA	
Efficiency 1 *1	Eff_{1_B3}	-	83	-	%	I_{OUT}=10mA
Efficiency 2 *1	Eff_{2_B3}	-	88	-	%	I_{OUT}=50mA
Startup Time	ST_{B3}	-	110	300	µs	During EN to 90% of Vnominal Voltage
Discharge Resistance 1	R_{DIS1_B3}	-	100	-	Ω	BUCK3_DIS[1:0]=01
Discharge Resistance 2	R_{DIS2_B3}	-	200	-	Ω	BUCK3_DIS[1:0]=10
Discharge Resistance 3	R_{DIS3_B3}	-	500	-	Ω	BUCK3_DIS[1:0]=11
Load Capacitance *3	C_{LMIN_B3}	-	133	-	µF	

Note 1: These parameters are determined as reference data without pre-shipping inspection.
Note 2: Including ripple voltage and load regulation.
Note 3: The effective load capacitance value considering accuracy, temperature characteristic and DC bias characteristic of output capacitors should not be less than 95µF.

3-5 Buck4 - V1P8A

V1P8A is a high-efficiency buck regulator with an integrated FET that converts the V5A voltage (5V) to a regulated voltage of 1.830V. The output voltage is possible to be changed between 1.800V to 1.880V. V1P8A control register is shown in Section “4-2-3 VCCRAM, V1P8A, V1P2A Control Registers”.

3-5-1 V1P8A Block Diagram

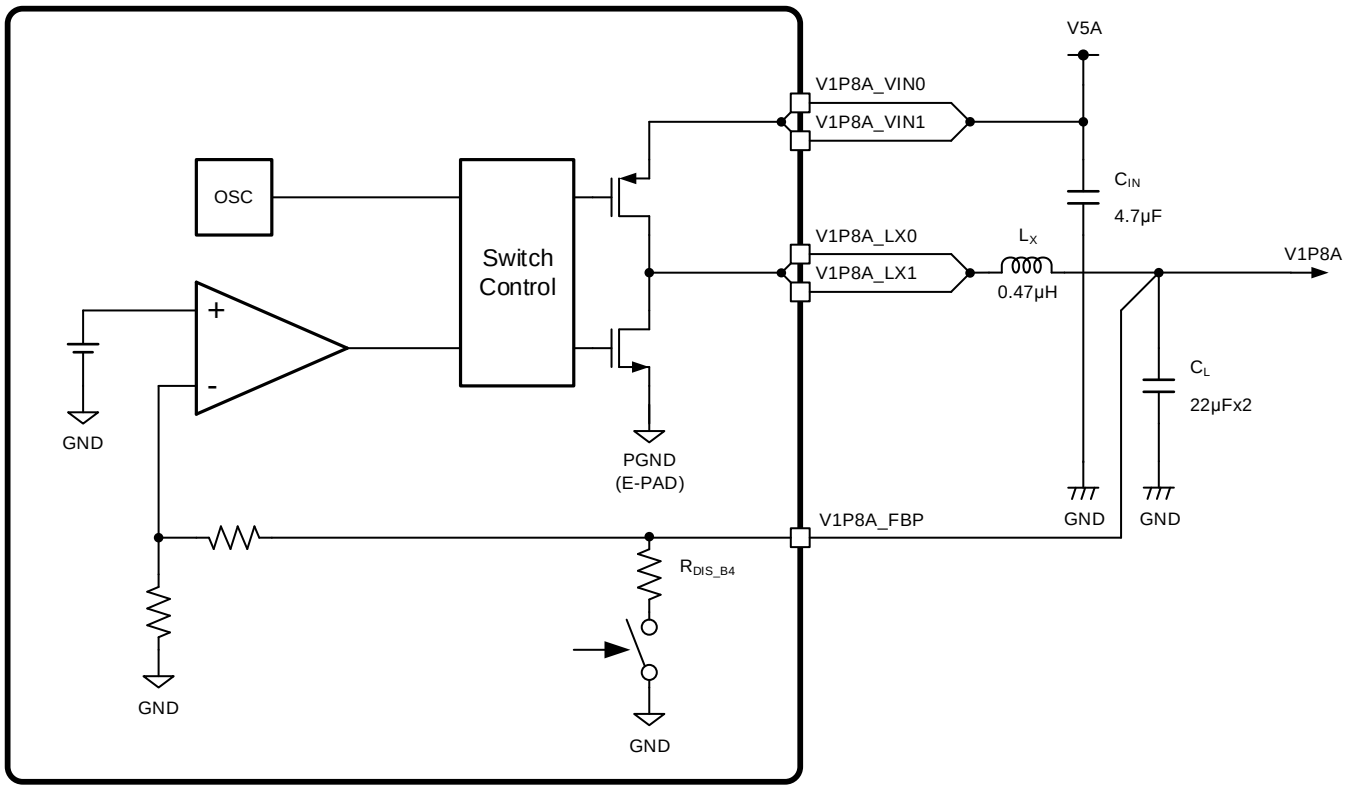


Figure 3-6 V1P8A Block Diagram

3-5-2 V1P8A Electrical Characteristics

Table 3-6 V1P8A Electrical Characteristics

Unless otherwise specified, Ta=25°C, VSYS=12.6V, VSYS_V5A_x=V1P8A_VINx=5.0V, BUCK4_VID=1.800V setting, C_L=44µF (22µF x 2), L_X=0.47µH, C_{IN}=4.7µF

Parameter	Symbol	Limit.			Unit	Remarks
		Min	Typ	Max		
Switching Frequency	f_{SW_B4}	-	2.0	-	MHz	PWM mode
Output Voltage 1	V_{O1_B4}	1.782	1.800	1.818	V	PWM mode, BUCK4_VID[1:0]=11
Output Voltage 2	V_{O2_B4}	1.861	1.880	1.899	V	PWM mode, BUCK4_VID[1:0]=00
Output Voltage 3	V_{O3_B4}	1.831	1.850	1.869	V	PWM mode, BUCK4_VID[1:0]=01
Output Voltage 4	V_{O4_B4}	1.811	1.830	1.849	V	PWM mode, BUCK4_VID[1:0]=10
Transient Droop Voltage 1 *1 *2	V_{DRP_B4}	-	-	72	mV	Slew Rate=2.5A/µs, I_{OUT}=450mA to 3000mA
Transient Overshoot Voltage 1 *1 *2	V_{OVS_B4}	-	-	72	mV	Slew Rate=2.5A/µs, I_{OUT}=3000mA to 450mA
Maximum Output Current *1	I_{MAX_B4}	3000	-	-	mA	
Efficiency 1 *1	Eff_{1_B4}	-	92	-	%	I_{OUT}=50mA
Efficiency 2 *1	Eff_{2_B4}	-	89	-	%	I_{OUT}=100mA
Startup Time	ST_{B4}	-	180	300	µs	During EN to 90% of Vnominal Voltage
Discharge Resistance 1	R_{DIS1_B4}	-	100	-	Ω	BUCK4_DIS[1:0]=01
Discharge Resistance 2	R_{DIS2_B4}	-	200	-	Ω	BUCK4_DIS[1:0]=10
Discharge Resistance 3	R_{DIS3_B4}	-	500	-	Ω	BUCK4_DIS[1:0]=11
Load Capacitance *3	C_{LMIN_B4}	-	44	-	µF	

Note 1: These parameters are determined as reference data without pre-shipping inspection.
Note 2: Including ripple voltage and load regulation.
Note 3: The effective load capacitance value considering accuracy, temperature characteristic and DC bias characteristic of output capacitors should not be less than 23µF.

3-6 Buck5 - V1P2A

V1P2A is a high-efficiency buck regulator with an integrated FET that converts the V5A voltage (5V) to a regulated voltage of 1.200V. The output voltage is possible to be changed between 1.100V to 1.240V through the I2C interface. V1P2A control register is shown in Section “4-2-3 VCCRAM, V1P8A, V1P2A Control Registers”.
V1P2A is always kept OFF at modes DDR_SEL2,1,0=(HLL) and (HHH) which are LPDDR3 or DDR4 optional modes that V1P2A is supplied from VDDQ as 1.200V.
When using the V1P2A merged mode with VDDQ, no external components are required for V1P2A, and all V1P2A load should be connected to VDDQ. Note that any fine tuning or on-the-fly voltage change on VDDQ would reflect the V1P2A load in such situations.

3-6-1 V1P2A Block Diagram

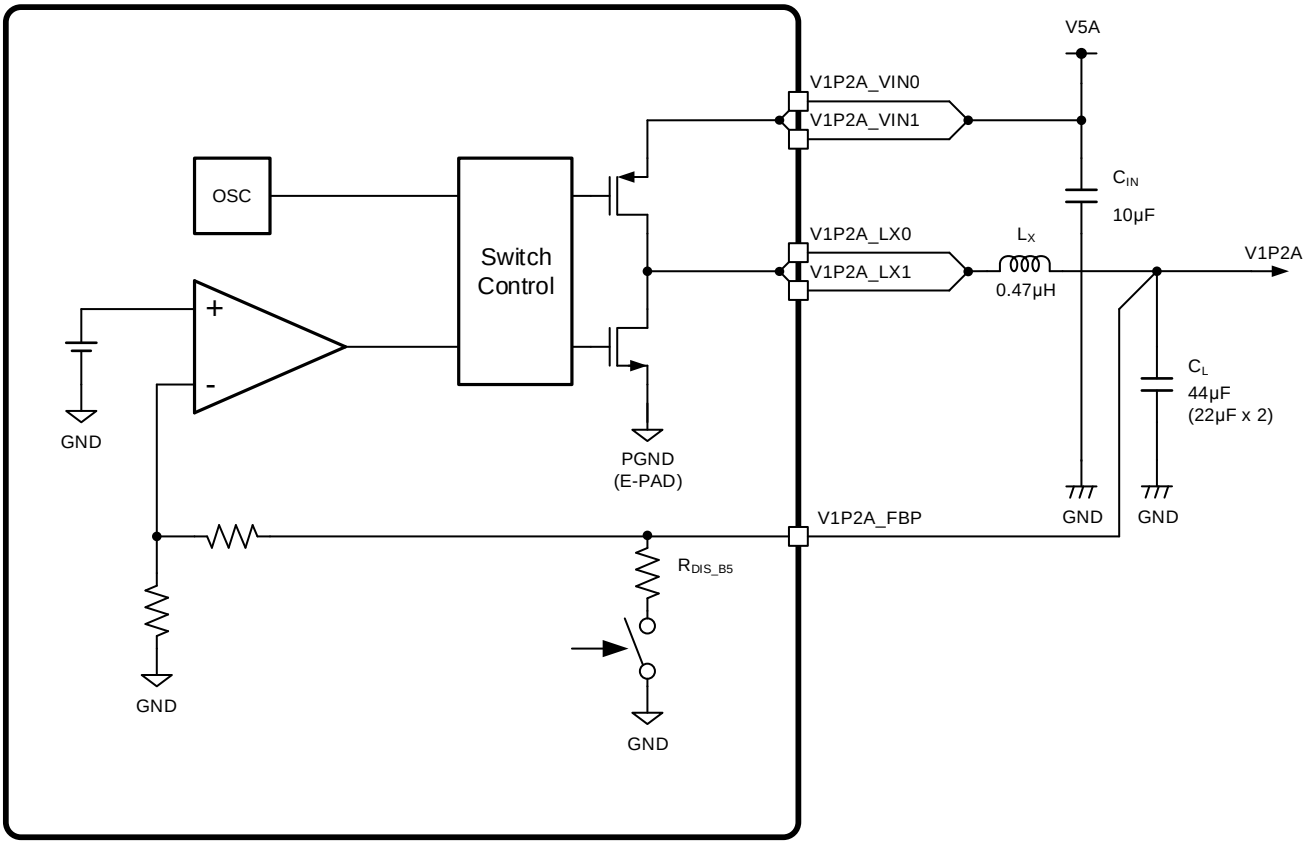


Figure 3-7 V1P2A Block Diagram

3-6-2 V1P2A Electrical Characteristics

Table 3-7 V1P2A Electrical Characteristics

Unless otherwise specified, Ta=25°C, VSYS_V5A_x=V1P2A_VIN=5.0V, BUCK5_VID=1.200V setting, C_L=44µF (22µFx2), L_X=0.47µH, C_{IN}=10µF

Parameter	Symbol	Limit.			Unit	Remarks
		Min	Typ	Max		
Switching Frequency	f_{SW_B5}	-	2.0	-	MHz	PWM mode
Output Voltage 1	V_{O1_B5}	1.227	1.240	1.253	V	PWM mode, BUCK5_VID[1:0]=10
Output Voltage 2	V_{O2_B5}	1.089	1.100	1.111	V	PWM mode, BUCK5_VID[1:0]=00
Output Voltage 3	V_{O3_B5}	1.138	1.150	1.162	V	PWM mode, BUCK5_VID[1:0]=01
Output Voltage 4	V_{O4_B5}	1.188	1.200	1.212	V	PWM mode, BUCK5_VID[1:0]=11
Transient Droop Voltage 1 *1 *2	V_{DRP_B5}	-	-	48	mV	Slew Rate=2.5A/µs, I_{OUT}=750mA to 2500mA
Transient Overshoot Voltage 1 *1 *2	V_{OVS_B5}	-	-	48	mV	Slew Rate=2.5A/µs, I_{OUT}=2500mA to 750mA
Maximum Output Current *1	I_{MAX_B5}	2500	-	-	mA	
Efficiency 1 *1	Eff_{1_B5}	-	85	-	%	I_{OUT}=10mA
Efficiency 2 *1	Eff_{2_B5}	-	85	-	%	I_{OUT}=50mA
Startup Time	ST_{B5}	-	200	300	µs	During EN to 90% of Vnominal Voltage
Discharge Resistance 1	R_{DIS1_B5}	-	100	-	Ω	BUCK5_DIS[1:0]=01
Discharge Resistance 2	R_{DIS2_B5}	-	200	-	Ω	BUCK5_DIS[1:0]=10
Discharge Resistance 3	R_{DIS3_B5}	-	500	-	Ω	BUCK5_DIS[1:0]=11
Load Capacitance *3	C_{LMIN_B5}	-	44	-	µF	

Note 1: These parameters are determined as reference data without pre-shipping inspection.
Note 2: Including ripple voltage and load regulation.
Note 3: The effective load capacitance value considering accuracy, temperature characteristic and DC bias characteristic of output capacitors should not be less than 29µF.

3-7 Buck6 – VDDQ and VDDQ_VTT

VDDQ is a high-efficiency buck controller that converts the VSYS voltage (5.4V to 21V) to a regulated voltage of 1.200V, 1.350V or 1.100V. VDDQ voltage is able to be controlled by the DDR_SEL0, DDR_SEL1 and DDR_SEL2 pins as shown in Section “4-3-11 DDR_SEL0, DDR_SEL1, DDR_SEL2”.
VDDQ control registers are shown in Section “4-2-4 VDDQ Control Register”.
Also, VDDQ is capable of fine tuning the output voltage in the range of +40mV from -30mV as a 10mV resolution to achieve the most appropriate target voltage which may differ between various PCB environments and DDR memory components. Refer to Section “4-2-13 VDDQ Voltage Adjust Registers” for more details.

VDDQ_VTT is a linear regulator that is capable of sink and source. The regulator delivers half of the VDDQ voltage and is always tracking VDDQ_FBP. It is used to center the voltage line for DRAM application. The maximum current capability is 600mA for sink and source.

In normal use cases, VDDQ and VDDQ_VTT voltage is set by DDR_SEL2, 1, 0 pins which corresponds to each DDR memory selection. However, there may be cases in which the DDR voltage might wanted to be changed On-the-fly, and VDDQ_DDR registers can be used to fulfill the request. Refer to Section “4-2-12 VDDQ and VPP On-The-Fly DDR Voltage Change Registers” for more details.

3-7-1 VDDQ and VDDQ_VTT Block Diagram

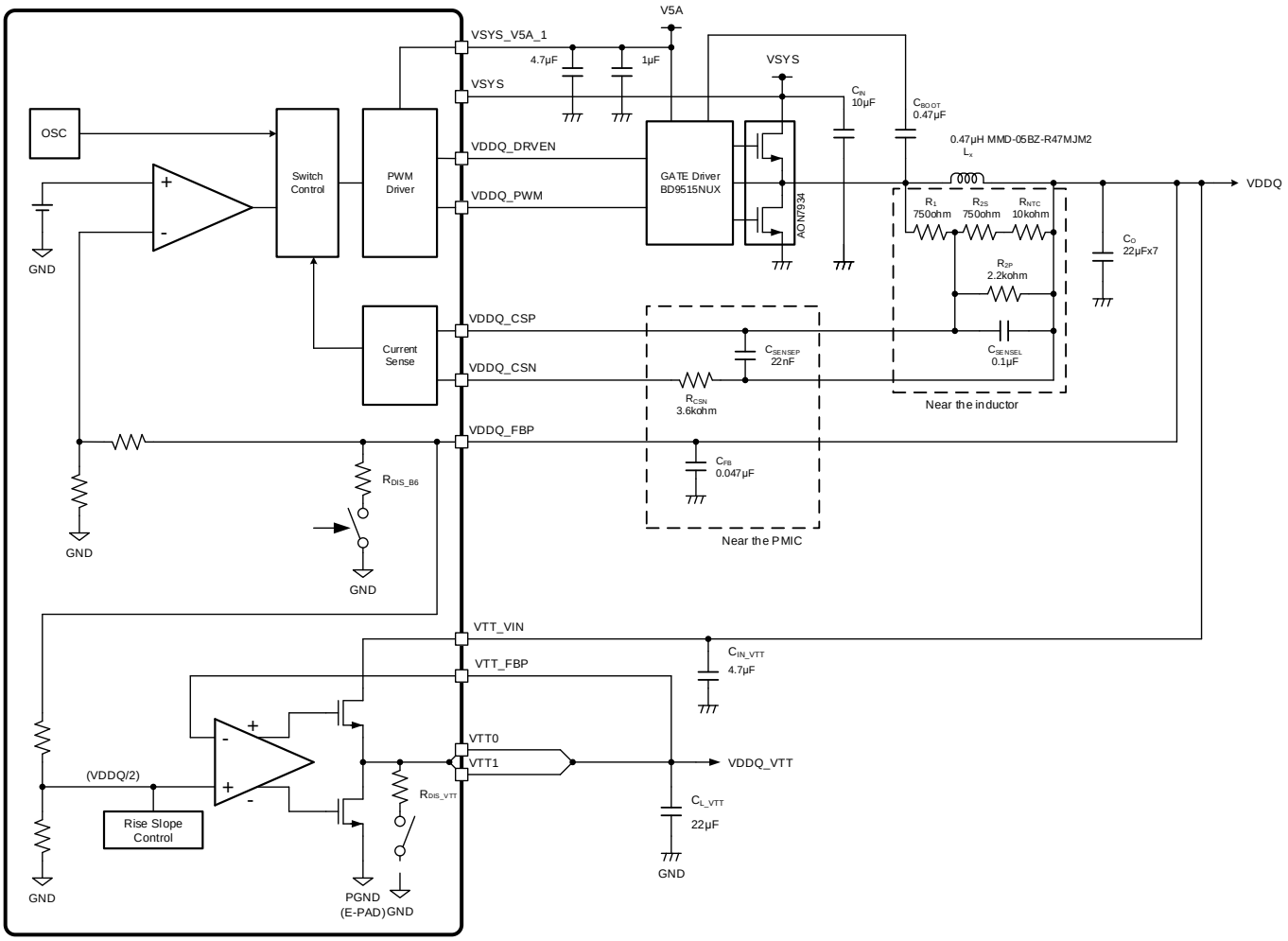


Figure 3-8 VDDQ and VDDQ_VTT Block Diagram

3-7-2 VDDQ_PWM and VDDQ_DRVEN

VDDQ_PWM and VDDQ_DRVEN pins are singals for controlling the external gate driver or DrMOS.

VDDQ_PWM is a pulse width modulated three state output controlling the external gate driver. When the output is high (VSYS_V5A_1 level), the external gate driver controls to turn ON the high-side FET. When the output is low (GND level), the external gate driver controls to turn ON the low-side FET. When the output is at the middle (half of VSYS_V5A_1), the external gate driver controls to go into diode mode (both high and low side FETs are turned off).
BD2671MWV recommends using BD9515NUX or any other functional compatible driver solution.

VDDQ_DRVEN is an output enable to the external gate driver. When the output is high (VSYS_V5A_1 level), the external gate driver turns ON. When the output is low (GND level), the external gate driver turns OFF.

Table 3-8 VDDQ_DRVEN and VDDQ_PWM Truth Table

VDDQ_DRVEN	VDDQ_PWM	High-side FET Control	Low-side FET Control
L	Middle of VSYS_V5A_1	OFF	OFF
H	Middle of VSYS_V5A_1	OFF	OFF
H	L	OFF	ON
H	H	ON	OFF

The timing chart of VDDQ_DRVEN and VDDQ_PWM is shown on Figure 3-9.

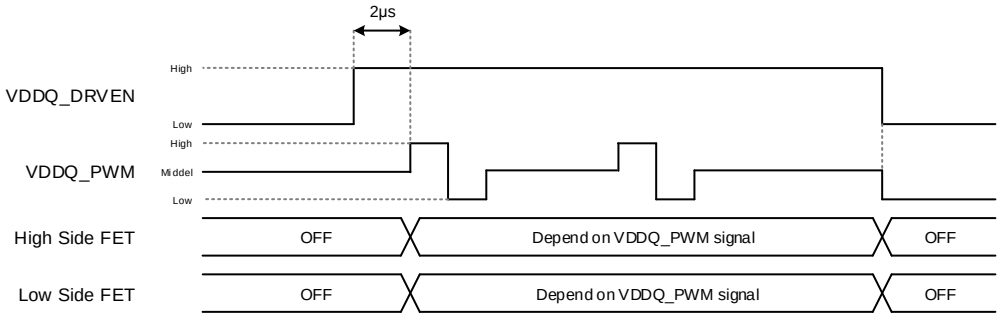


Figure 3-9 VDDQ_DRVEN and VDDQ_PWM Timing Chart

3-7-3 Inductor Current Sensing

The VDDQ_CSP and VDDQ_CSN pins are the input to the differential current sense amplifier. The positive current sense (VDDQ_CSP) pin is connected to the non-inverting input, and the negative current sense (VDDQ_CSN) pin is connected to the inverting input. Figure 3-8 shows the circuit for monitoring the current of the power stage using the inductor DCR.
BD2671MWV recommends using the inductor which DCR is larger than 3mΩ.

3-7-4 VDDQ and VDDQ_VTT Electrical Characteristics

Table 3-9 VDDQ and VDDQ_VTT Electrical Characteristics

Unless otherwise specified, Ta=25°C, VSYS=12.6V, VSYS_V5A_x=5.0V, C_L=22µFx7, L_X=0.47µH, C_{IN}=10µFx2, C_{L_VTT}=22µF, DDR_SEL2,1,0="000"

Parameter	Symbol	Limit.			Unit	Remarks
		Min	Typ	Max		
VDDQ						
Switching Frequency	f_{SW_B6}	-	0.75	-	MHz	PWM mode, VDDQ_CLKSEL[1:0]=10
Output Voltage 1	V_{O1_B6}	1.188	1.200	1.212	V	PWM mode, DDR_SEL2,1,0=(LLL), (LHH), (HLL), (HHH)
Output Voltage 2	V_{O2_B6}	1.337	1.350	1.364	V	PWM mode, DDR_SEL2,1,0=(LLH), (HLH)
Output Voltage 3	V_{O3_B6}	1.089	1.100	1.111	V	PWM mode, DDR_SEL2,1,0=(LHL), (HHL)
Transient Droop Voltage 1 *1 *2 *4	V_{DRP_B6}	-	-	48	mV	Slew Rate=2.5A/µs, I_{OUT}=2100mA to 7000mA
Transient Overshoot Voltage 1 *1 *2 *4	V_{OVS_B6}	-	-	48	mV	Slew Rate=2.5A/µs, I_{OUT}=7000mA to 2100mA
PWM Output High Level	V_{PWMH_B6}	4.8	-	-	V	I_{OUT}=1mA
PWM Output Low Level	V_{PWML_B6}	-	-	0.2	V	I_{IN}=1mA
PWM Tri-State Leakage	I_{PWMZ_B6}	-1	-	1	uA	V_{IN}=2.5V
DRVEN Output High Level	V_{DRVENH_B6}	4.8	-	-	V	I_{OUT}=1mA
DRVEN Output Low Level	V_{DRVENL_B6}	-	-	0.2	V	I_{IN}=1mA
Min On Time	Ton_{MIN_B6}	50	-	-	ns	
Min Off Time	$Toff_{MIN\_B6}$	50	-	-	ns	
Startup Time *1	ST_{B6}	-	150	200	µs	During EN to 90% of Vnominal Voltage
Maximum Output Current *1	I_{MAX_B6}	7	-	-	A	VDDQ_LIMSEL[2:0]=001
Discharge Resistance 1	R_{DIS1_B6}	-	100	-	Ω	BUCK6_DIS[1:0]=01
Discharge Resistance 2	R_{DIS2_B6}	-	200	-	Ω	BUCK6_DIS[1:0]=10
Discharge Resistance 3	R_{DIS3_B6}	-	500	-	Ω	BUCK6_DIS[1:0]=11
VDDQ_VTT						
Output Voltage 1	V_{O1_VTT}	0.588	0.600	0.612	V	DDR_SEL2,1,0=(LLL), (LHH), (HLL), (HHH) (VDDQ_FBP=1.200V)
Output Voltage 2	V_{O2_VTT}	0.662	0.675	0.688	V	DDR_SEL2,1,0=(LLH), (HLH) (VDDQ_FBP=1.350V)
Transient Droop Voltage 1 *1 *2	V_{DRP_VTT}	-	-	18	mV	Slew Rate=2.5A/µs, I_{OUT}=150mA to 600mA, -600mA to -150mA
Transient Overshoot Voltage 1 *1 *2	V_{OVS_VTT}	-	-	18	mV	Slew Rate=2.5A/µs, I_{OUT}=600mA to 150mA, -150mA to -600mA
Maximum Output Current *1	I_{MAX_VTT}	-600	-	600	mA	
Startup Time	ST_{VTT}	-	25	100	µs	During EN to 90% of Vnominal Voltage
Discharge Resistance	R_{DIS_VTT}	-	100	-	Ω	
Load Capacitance *3	C_{LMIN_VTT}	-	22	-	µF	

Note 1: These parameters are determined as reference data without pre-shipping inspection.
Note 2: Including ripple voltage and load regulation.
Note 3: The effective load capacitance value considering accuracy, temperature characteristic and DC bias characteristic of output capacitors should not be less than 17µF and larger than 30µF.
Note 4: These parameters are design values when using ROHM recommended external parts and values as defined in Figure 3-8.

3-8 LDO_VPP

LDO_VPP is a linear regulator that is outputting 1.8V or 2.5V from 3.3V. This is mainly used for the VPP power supply of the DRAM. LDO_VPP voltage is able to be controlled by the DDR_SEL0, DDR_SEL1 and DDR_SEL2 pins as shown in Section “4-3-11 DDR_SEL0, DDR_SEL1, DDR_SEL2”.
The maximum current capability is 1000mA.

LDO_VPP is capable of fine tuning the output voltage in the range of +3% from -2% to achieve the most appropriate target voltage which may differ between various PCB environments and DDR memory components.
Refer to Section “4-2-14 VPP Voltage Adjust Registers” for more details.

On applications which higher power efficiency is more important than lowering the BOM cost, the LDO_VPP output can be used for enabling an external Switch which is powered by V1P8A. This is capable in systems which the VPP output is set for 1.8V in LPDDR3, DDR3L and LPDDR4.

3-8-1 LDO_VPP Block Diagram

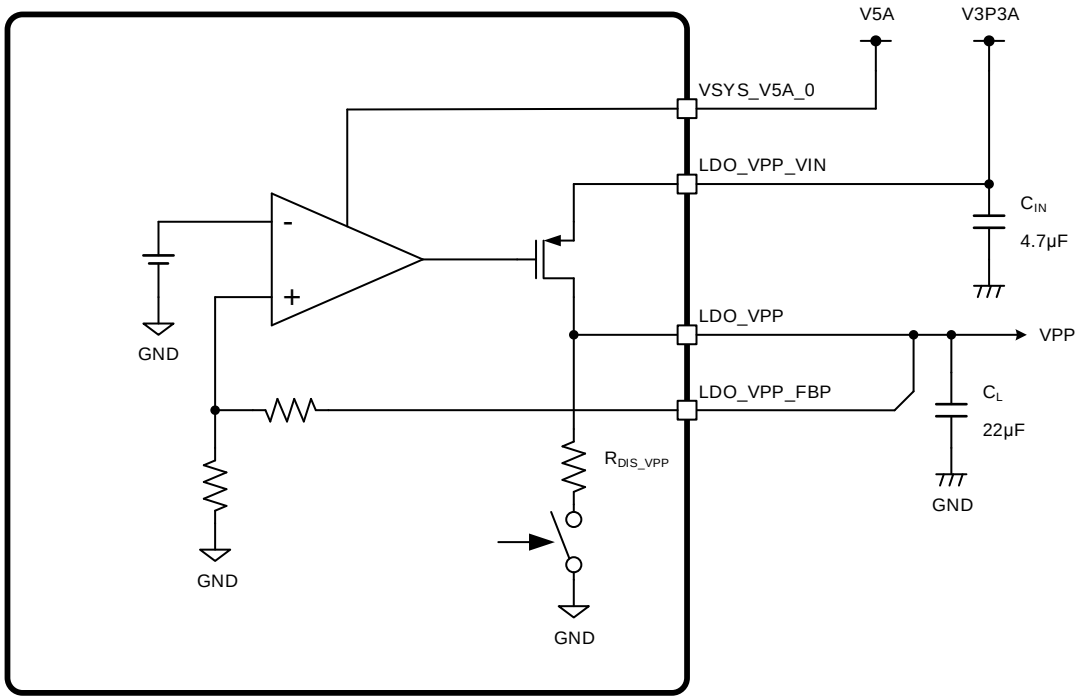


Figure 3-10 VPP Block Diagram

3-8-2 LDO_VPP Electrical Characteristics

Table 3-10 LDO_VPP Electrical Characteristics

Unless otherwise specified, Ta=25°C, VSYS=12.6V, VSYS_V5A_x=5.0V, LDO_VPP_VIN=3.3V, C_L=22µF, C_{IN}=4.7µF, C_L=22µF, DDR_SEL2,1,0=(LLL)

Parameter	Symbol	Limit.			Unit	Remarks
		Min	Typ	Max		
LDO_VPP_VIN voltage	f_{SW_B6}	3.1	3.3	3.6	V	
Output Voltage 1	V_{O1_VPP}	1.782	1.800	1.818	V	DDR_SEL2,1,0=(LLL), (LHL), (HLL), (HLH) and (HHL), Io=1mA
Output Voltage 2	V_{O2_VPP}	2.475	2.500	2.525	V	DDR_SEL2,1,0=(LHH) and (HHH), Io=1mA
Transient Droop Voltage 1 *1 *2	V_{DRP_VPP}	-	-	72	mV	Slew Rate=2.5A/µs, I_{OUT}=300mA to 1000mA DDR_SEL2,1,0=(LLL), (LHL), (HLL), (HLH) and (HHL)
Transient Overshoot Voltage 1 *1 *2	V_{OVS_VPP}	-	-	72	mV	Slew Rate=2.5A/µs, I_{OUT}=1000mA to 300mA DDR_SEL2,1,0=(LLL), (LHL), (HLL), (HLH) and (HHL)
Transient Droop Voltage 2 *1 *2	V_{DRP_VPP}	-	-	100	mV	Slew Rate=2.5A/µs, I_{OUT}=300mA to 1000mA DDR_SEL2,1,0=(LHH) and (HHH)
Transient Overshoot Voltage 2 *1 *2	V_{OVS_VPP}	-	-	100	mV	Slew Rate=2.5A/µs, I_{OUT}=1000mA to 300mA DDR_SEL2,1,0=(LHH) and (HHH)
Maximum Output Current *1	I_{MAX_VPP}	1000	-	-	mA	
Startup Time	ST_{VPP}	-	100	400	µs	During EN to 90% of Vnominal Voltage
Discharge Resistance	R_{DIS_VPP}	-	500	-	Ω	
Load Capacitance *3	C_{LMIN_VPP}	-	22	-	µF	

Note 1: These parameters are determined as reference data without pre-shipping inspection.
Note 2: Including ripple voltage and load regulation.
Note 3: The effective load capacitance value considering accuracy, temperature characteristic and DC bias characteristic of output capacitors should not be less than 10µF.

4 Host Interface and Control

4-1 I2C (Slave)

BD2671MWV is a slave-only device that is mastered by the SOC. Operating frequencies which is supported are in the range of 100kHz – 1.0MHz. BD2671MWV is being accessed using a 7-bit addressing scheme. I2C slave does not support clock-stretching.

4-1-1 I2C (Slave) Block Diagram

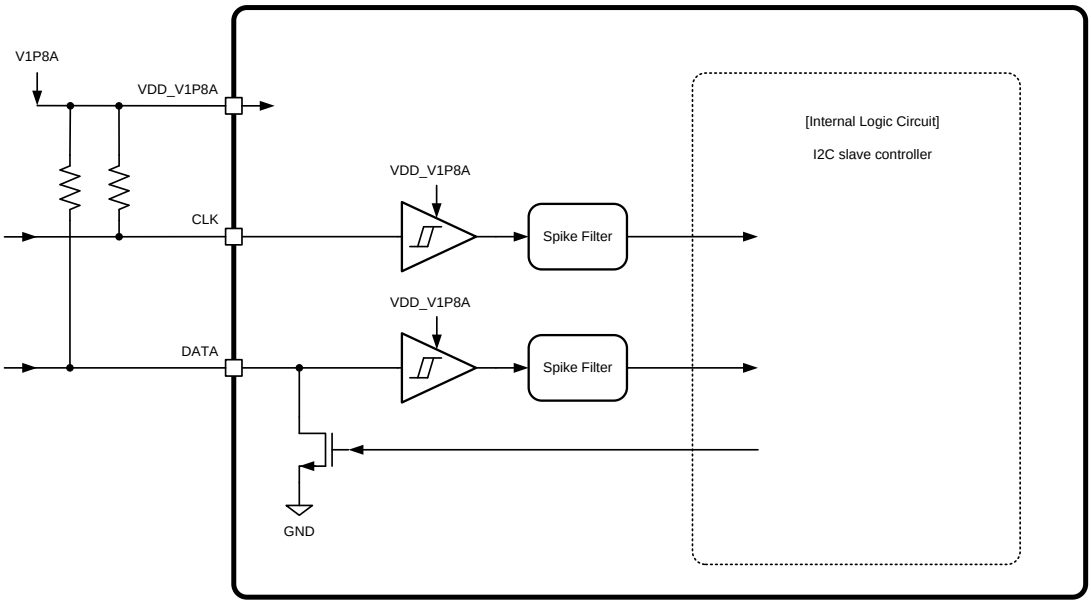


Figure 4-1 I2C (Slave) Block Diagram

4-1-2 I2C (Slave) Electrical Characteristics

Table 4-1 I2C (Slave) DC - Electrical Characteristics

Unless otherwise specified, Ta=25°C, VSYS=12.6V, VSYS_V5A_x=5.0V, VDD_V1P8A=1.800V

Parameter	Symbol	Limit.			Unit	Remarks
		Min	Typ	Max		
CLK						
Input Low Voltage	V_{IL_CLK}	-0.3	-	VDD x 0.3	V	VDD=VDD_V1P8A
Input High Voltage	V_{IH_CLK}	VDD x 0.7	-	VDD + 0.3	V	VDD=VDD_V1P8A
Input Hysteresis	V_{HYS_CLK}	0.1	-	-	V	VDD=VDD_V1P8A
DATA						
Input Low Voltage	V_{IL_DAT}	-0.3	-	VDD x 0.3	V	VDD=VDD_V1P8A
Input High Voltage	V_{IH_DAT}	VDD x 0.7	-	VDD + 0.3	V	VDD=VDD_V1P8A
Input Hysteresis	V_{HYS_DAT}	0.1	-	-	V	VDD=VDD_V1P8A
Output Low Voltage	V_{OL_DAT}	-	-	0.36	V	I_{IN}=3mA
Leak Current	I_{LK_DAT}	-	-	1	µA	Vin=VDD_V1P8A, Nch Open Drain=OPEN

Table 4-2 I2C (Slave) AC Timing

Unless otherwise specified, Ta=25°C, VSYS=12.6V, VSYS_V5A_x=5.0V, VDD_V1P8A=1.800V

Parameter	Symbol	Limit. Fast mode		Limit. Fast mode plus		Unit
		Min	Max	Min	Max	
I2C_CLK clock frequency	f_{SCL}	0	400	0	1000	kHz
Hold time START condition	$t_{HD;STA}$	0.6	-	0.26	-	µs
LOW period of the I2C_CLK clock	t_{LOW}	1.3	-	0.5	-	µs
HIGH period of the I2C_CLK clock	t_{HIGH}	0.6	-	0.26	-	µs
Set-up time for a repeated START condition	$t_{SU;STA}$	0.6	-	0.26	-	µs
Data hold time	$t_{HD;DAT}$	0	-	0	-	ns
Data set-up time	$t_{SU;DAT}$	100	-	50	-	ns
Set-up time for STOP condition	$t_{SU;STO}$	0.6	-	0.26	-	µs
Bus free time between a STOP and START condition	t_{BUF}	1.3	-	0.5	-	µs
Fall time of I2C_DATA signal	t_{fDA}	-	300	-	120	ns
Capacitive load for each bus line	C_b	-	400	-	550	pF
Pulse width of spikes that is suppressed by the input filter	t_{SP}	0	50	0	50	ns
Data valid time	$t_{VD;DAT}$	-	0.9	-	0.45	µs
Data valid acknowledge time	$t_{VD;ACK}$	-	0.9	-	0.45	µs

Note: This table is determined as reference data without pre-shipping inspection.

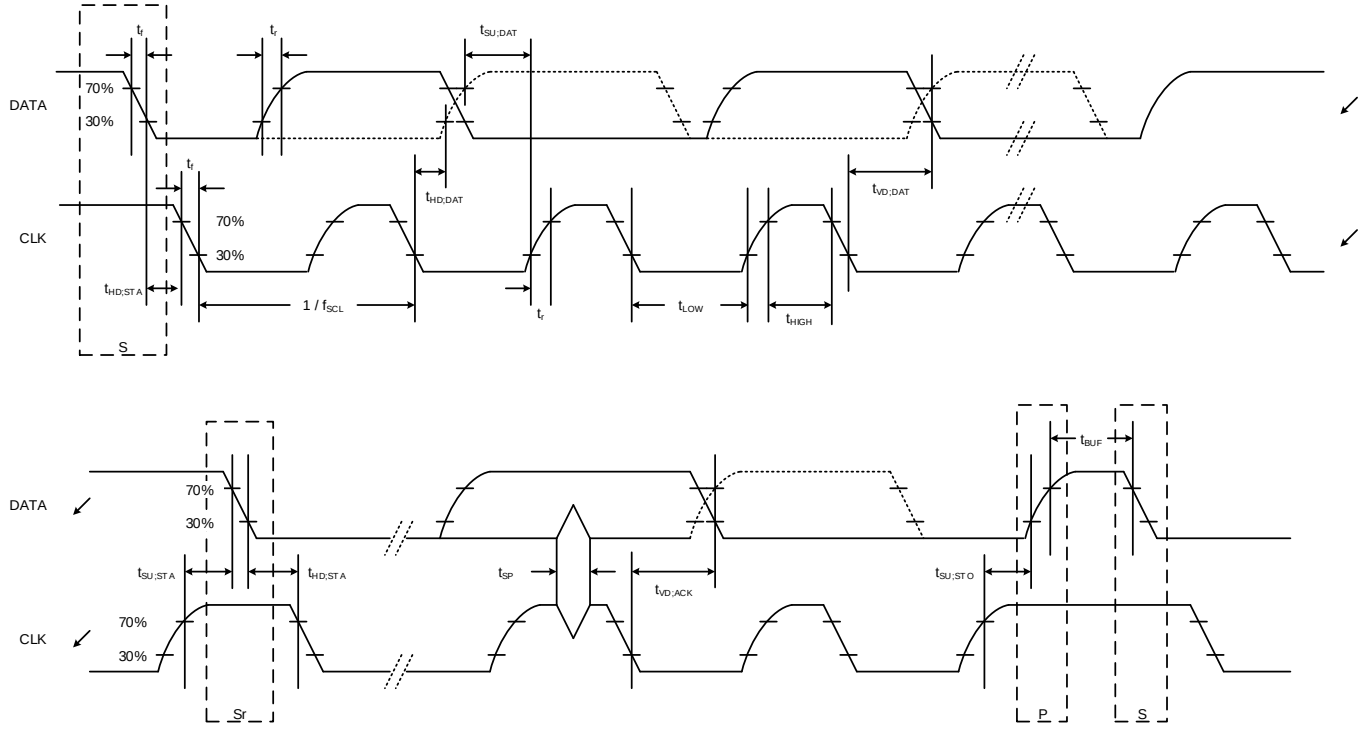


Figure 4-2 I2C (Slave) AC Timing

4-1-3 I2C (Slave) Protocol

BD2671MWV supports the standard I2C read and write functions as described in the I2C specification. Refer to the I2C-bus specification and user manual Rev. 03 -- 19 June 2007. The configuration register space is divided into two 256-byte partitions. BD2671MWV supports two 7-bit device addresses, fixed as 0x5E (1011110) and 0x6E (1101110), to access each of the 256 byte partitions, respectively. Note that in 8-bit format, these addresses correspond to 0xBC and 0xDC for writes, and 0xBD and 0xDD for reads.

Table 4-3 I2C Addresses

Device address	7-bit	8-bit (Write)	8-bit (Read)
Device address 1	0x5E	0xBC	0xBD
Device address 2 (Fully for internal test only)	0x6E	0xDC	0xDD

Reads from the registers follow the "combined protocol" as described in the I2C specification, in which the first byte written is the register address to be read, and the first byte read (after a repeat START condition) is the data from that register address.

The following diagrams capture write/read transaction format/protocol.

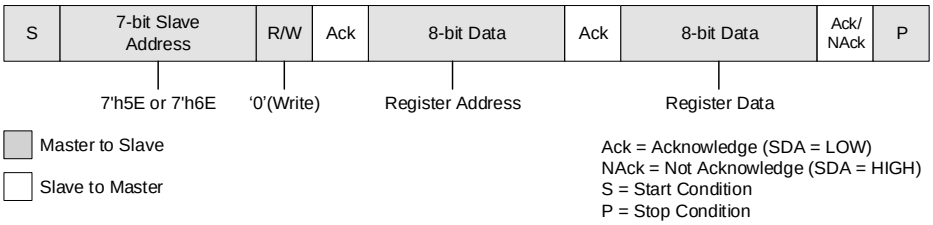


Figure 4-3 I2C Fast Speed Write

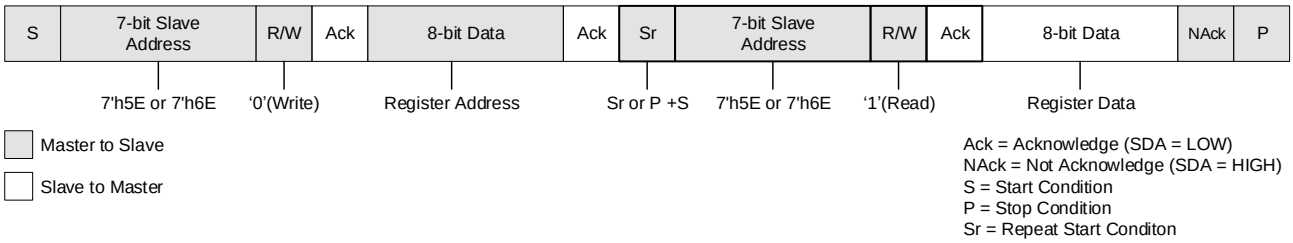


Figure 4-4 I2C Fast Speed Read

4-2 Register map (Device Address 0x5E)

Table 4-4 Register Map

Address (Hex)	Reset upon Entering	Register Name	D7	D6	D5	D4	D3	D2	D1	D0	Initial Value	Access (R, W, WR)	Locked
00	NA	VENDORID	VENDORID[7:0]								0x1F	R	-
01	NA	REVID	-	-	MAJREV[2:0]			MINREV[2:0]			0x00	R	-
02	VSYS_POR	IRQ	VRFAULT	-	-	-	-	ONOFFSRC	-	DIETEMP	0x00	R/W	-
03	VSYS_POR	IRQ_MASK	MVRFAULT	-	-	-	-	MONOFFSRC	-	MDIETEMP	0x85	R/W	-
04	VSYS_POR	PMICSTAT	-	-	-	-	-	-	-	SDIETEMP	0x00	R	-
05	VSYS_POR	OFFONSRC	-	-	-	-	COLDOFF	UVLO	OCP	CRITTEMP	0x00	R/W	-
20	SLP_S0#=H->L SLP_S3#=H->L PMIC_G3	BUCK1CTRL	-	BUCK1_VID[6:0]							0x38	R/W	-
21	SLP_S0#=H->L SLP_S3#=H->L PMIC_G3	BUCK2CTRL	-	BUCK2_VID[6:0]							0x00	R/W	-
22	PMIC_G3	BUCK3CTRL	-	-	-	-	BUCK3_VID[1:0]		BUCK3_MODE	-	0x0C	R/W	-
25	PMIC_G3	BUCK4CTRL	-	-	-	-	BUCK4_VID[1:0]		BUCK4_MODE	-	0x08	R/W	-
26	PMIC_G3	BUCK5CTRL	-	-	-	-	BUCK5_VID[1:0]		BUCK5_MODE	-	0x0C	R/W	-
27	PMIC_G3	BUCK6CTRL	-	-	-	-	-	-	BUCK6_MODE	-	0x00	R/W	-
40	VSYS_POR	DISCHCTRL1	BUCK4_DIS[1:0]		BUCK3_DIS[1:0]		BUCK2_DIS[1:0]		BUCK1_DIS[1:0]		0x55	R/W	-
41	VSYS_POR	DISCHCTRL2	-	-	-	-	BUCK6_DIS[1:0]		BUCK5_DIS[1:0]		0x05	R/W	-
43	PMIC_G3	POK_DELAY	-	-	-	-	-	PWROKDELAY[2:0]			0x07	R/W	-
80	VSYS_POR	VCCGI_CLIM	-	-	-	-	-	VCCGI_LIMSEL[2:0]			0x04	R/W	UNLOCK=L
81	VSYS_POR	VCCGI_FSW	-	-	-	-	-	-	VCCGI_CLKSEL[1:0]		0x01	R/W	UNLOCK=L
82	VSYS_POR	UNLOCK	-	-	-	-	-	-	-	UNLOCK	0x00	R/W	-
83	VSYS_POR	VRFAULT_INT	-	-	VDDQ_FAULT	V1P2A_FAULT	V1P8A_FAULT	VCCRAM_FAULT	VCCGI_FAULT	VNN_FAULT	0x00	R/W	-
85	VSYS_POR	VDDQ_CLIM	-	-	-	-	-	VDDQ_LIMSEL[2:0]			0x01	R/W	UNLOCK=L
86	VSYS_POR	VDDQ_FSW	-	-	-	-	-	-	VDDQ_CLKSEL[1:0]		0x02	R/W	UNLOCK=L
88	PMIC_G3	VDDQ_DDR	-	-	-	-	VPP_DDR_SYNC	VDDQ_DDR_REGEN	VDDQ_DDR[1:0]		0x00	R/W	UNLOCK=L
89	VSYS_POR	VDDQ_VSEL	-	-	-	-	-	VDDQ_VSEL[2:0]			0x04	R/W	UNLOCK=L
8A	VSYS_POR	VPP_VSEL	-	-	-	-	-	-	VPP_VSEL[1:0]		0x02	R/W	UNLOCK=L

Reading any register addresses not assigned in Table 4-4 (Device Address 0x5E: Addresses 0x00-0x83, 0x85-0x86, 0x88-0x8A), it will return 0xFF as read data.

All dashed boxes are “Reserved” registers which are all “0” read and not applicable for writing to these registers.
When accessing to the vendor specific register area (0x80-0x8A), do not write to any register address which is not defined in this register map.

Table 4-5 Register address assignment

Device Address	Register Address	Area	Write access
0x5E	0x00-0x7F	User control	Enabled
	0x80-0x8A	Vendor Specific control	Enabled when UNLOCK=1
	0x8B-0xFF	Factory Test	Disabled
0x6E	0x00-0xFF	Factory Test	Disabled

4-2-1 Voltage ID Encoding

VNN and VCCGI support dynamic voltage scaling (DVS) using the 7 bits voltage ID (VID) table with a 10mV resolution shown in Table 4-6. VNN and VCCGI accept only valid VID settings. VNN and VCCGI reject (NACK) any attempt to write a RSVD VID to VNN or VCCGI control registers, and VNN and VCCGI control register VID will stay at the last valid programmed VID value, with no change in output voltage and register value. The read value from the I2C will always show the previous valid value.

Table 4-6 VNN and VCCGI VID DAC Table

VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	Voltage [V]	VID 7	VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	Voltage [V]
0	0	0	0	0	0	0	OFF	1	0	0	0	0	0	0	1.130
0	0	0	0	0	0	1	0.500	1	0	0	0	0	0	1	1.140
0	0	0	0	0	1	0	0.510	1	0	0	0	0	1	0	1.150
0	0	0	0	0	1	1	0.520	1	0	0	0	0	1	1	1.160
0	0	0	0	1	0	0	0.530	1	0	0	0	1	0	0	1.170
0	0	0	0	1	0	1	0.540	1	0	0	0	1	0	1	1.180
0	0	0	0	1	1	0	0.550	1	0	0	0	1	1	0	1.190
0	0	0	0	1	1	1	0.560	1	0	0	0	1	1	1	1.200
0	0	0	1	0	0	0	0.570	1	0	0	1	0	0	0	1.210
0	0	0	1	0	0	1	0.580	1	0	0	1	0	0	1	1.220
0	0	0	1	0	1	0	0.590	1	0	0	1	0	1	0	1.230
0	0	0	1	0	1	1	0.600	1	0	0	1	0	1	1	1.240
0	0	0	1	1	0	0	0.610	1	0	0	1	1	0	0	1.250
0	0	0	1	1	0	1	0.620	1	0	0	1	1	0	1	1.260
0	0	0	1	1	1	0	0.630	1	0	0	1	1	1	0	1.270
0	0	0	1	1	1	1	0.640	1	0	0	1	1	1	1	1.280
0	0	1	0	0	0	0	0.650	1	0	1	0	0	0	0	1.290
0	0	1	0	0	0	1	0.660	1	0	1	0	0	0	1	1.300
0	0	1	0	0	1	0	0.670	1	0	1	0	0	1	0	1.310
0	0	1	0	0	1	1	0.680	1	0	1	0	0	1	1	1.320
0	0	1	0	1	0	0	0.690	1	0	1	0	1	0	0	1.330
0	0	1	0	1	0	1	0.700	1	0	1	0	1	0	1	1.340
0	0	1	0	1	1	0	0.710	1	0	1	0	1	1	0	1.350
0	0	1	0	1	1	1	0.720	1	0	1	0	1	1	1	1.360
0	0	1	1	0	0	0	0.730	1	0	1	1	0	0	0	1.370
0	0	1	1	0	0	1	0.740	1	0	1	1	0	0	1	1.380
0	0	1	1	0	1	0	0.750	1	0	1	1	0	1	0	1.390
0	0	1	1	0	1	1	0.760	1	0	1	1	0	1	1	1.400
0	0	1	1	1	0	0	0.770	1	0	1	1	1	0	0	1.410
0	0	1	1	1	0	1	0.780	1	0	1	1	1	0	1	1.420
0	0	1	1	1	1	0	0.790	1	0	1	1	1	1	0	1.430
0	0	1	1	1	1	1	0.800	1	0	1	1	1	1	1	1.440
0	1	0	0	0	0	0	0.810	1	1	0	0	0	0	0	1.450
0	1	0	0	0	0	1	0.820	1	1	0	0	0	0	1	RSVD
0	1	0	0	0	1	0	0.830	1	1	0	0	0	1	0	RSVD
0	1	0	0	0	1	1	0.840	1	1	0	0	0	1	1	RSVD
0	1	0	0	1	0	0	0.850	1	1	0	0	1	0	0	RSVD
0	1	0	0	1	0	1	0.860	1	1	0	0	1	0	1	RSVD
0	1	0	0	1	1	0	0.870	1	1	0	0	1	1	0	RSVD
0	1	0	0	1	1	1	0.880	1	1	0	0	1	1	1	RSVD
0	1	0	1	0	0	0	0.890	1	1	0	1	0	0	0	RSVD
0	1	0	1	0	0	1	0.900	1	1	0	1	0	0	1	RSVD
0	1	0	1	0	1	0	0.910	1	1	0	1	0	1	0	RSVD
0	1	0	1	0	1	1	0.920	1	1	0	1	0	1	1	RSVD
0	1	0	1	1	0	0	0.930	1	1	0	1	1	0	0	RSVD
0	1	0	1	1	0	1	0.940	1	1	0	1	1	0	1	RSVD
0	1	0	1	1	1	0	0.950	1	1	0	1	1	1	0	RSVD
0	1	0	1	1	1	1	0.960	1	1	0	1	1	1	1	RSVD
0	1	1	0	0	0	0	0.970	1	1	1	0	0	0	0	RSVD
0	1	1	0	0	0	1	0.980	1	1	1	0	0	0	1	RSVD
0	1	1	0	0	1	0	0.990	1	1	1	0	0	1	0	RSVD
0	1	1	0	0	1	1	1.000	1	1	1	0	0	1	1	RSVD
0	1	1	0	1	0	0	1.010	1	1	1	0	1	0	0	RSVD
0	1	1	0	1	0	1	1.020	1	1	1	0	1	0	1	RSVD
0	1	1	0	1	1	0	1.030	1	1	1	0	1	1	0	RSVD
0	1	1	0	1	1	1	1.040	1	1	1	0	1	1	1	RSVD
0	1	1	1	0	0	0	1.050	1	1	1	1	0	0	0	RSVD
0	1	1	1	0	0	1	1.060	1	1	1	1	0	0	1	RSVD
0	1	1	1	0	1	0	1.070	1	1	1	1	0	1	0	RSVD
0	1	1	1	0	1	1	1.080	1	1	1	1	0	1	1	RSVD
0	1	1	1	1	0	0	1.090	1	1	1	1	1	0	0	RSVD
0	1	1	1	1	0	1	1.100	1	1	1	1	1	0	1	RSVD
0	1	1	1	1	1	0	1.110	1	1	1	1	1	1	0	RSVD
0	1	1	1	1	1	1	1.120	1	1	1	1	1	1	1	RSVD

4-2-2 VNN & VCCGI Control Registers

VNN and VCCGI VID control is capable by I2C registers shown in Table 4-7 and Table 4-8.

Table 4-7 BUCK1CTRL – VNN VID Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK1CTRL	R/W	-	BUCK1_VID[6:0]							0x38	0x20

Bit	Name	Function	Initial
D[6:0]	BUCK1_VID[6:0]	This field sets the VNN nominal regulator operating voltage. VNN can be set to 0V by setting 0x00 to the VID register. At that time, VNN will be turned OFF, and the power good circuit will always recognize VNN running as nominal voltage. This will maintain the PCH_PWROK and RSMRST_B to the OK state for VNN. This is also applied when VNN is turned OFF by the power sequence to S0IX state. Reset condition for this register is SLP_S3_B H → L edge or SLP_S0_B H → L edge or PMIC SHUTDOWN. This register can be over-written by the SOC to boot up as a different voltage than the initial register value. For example, if it is written to 0x33(1.000V) after transitioning from S0 to S0IX, the VNN will bootup to 1.000V when transitioning up to S0.	0111000

Table 4-8 BUCK2CTRL – VCCGI VID Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK2CTRL	R/W	-	BUCK2_VID[6:0]							0x00	0x21

Bit	Name	Function	Initial
D[6:0]	BUCK2_VID[6:0]	This field sets the VCCGI nominal regulator operating voltage. VCCGI can be set to 0V by setting 0x00 to the VID register. At that time, VCCGI will be turned OFF, and the power good circuit will always recognize VCCGI running as nominal voltage. This will maintain the PCH_PWROK and RSMRST_B to the OK state for VNN. This is also applied when VCCGI is turned OFF by the power sequence to S0IX state. Reset condition for this register is SLP_S3_B H → L edge or SLP_S0_B H → L edge or PMIC SHUTDOWN. This register can be over-written by the SOC to boot up as a different voltage than the initial register value which is default 0V. For example, if it is written to 0x33(1.000V) after transitioning from S0 to S0IX, the VCCGI will bootup to 1.000V when transitioning up to S0 and PCH_PWROK is asserted.	0000000

4-2-3 VCCRAM, V1P8A, V1P2A Control Registers

Table 4-9 BUCK3CTRL – VCCRAM Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK3CTRL	R/W	-	-	-	-	BUCK3_VID[1:0]		MODE	-	0x0C	0x22

Bit	Name	Function	Initial
D[3:2]	BUCK3_VID[1:0]	This field sets the VCCRAM nominal regulator operating voltage. 00 – 1.100 V 01 – 1.075 V 10 – 1.000 V 11 – 1.050 V (Initial)	11
D[1]	MODE	VR MODE bit 0 – AUTO PWM/PFM mode (Initial) VR adjusts the operating mode (PFM/PWM) automatically based on the load current to maximize power efficiency. 1 – Forced PWM Mode VR operates in PWM mode only.	0

Table 4-10 BUCK4CTRL – V1P8A Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK4CTRL	R/W	-	-	-	-	BUCK4_VID[1:0]		MODE	-	0x08	0x25

Bit	Name	Function	Initial
D[3:2]	BUCK4_VID[1:0]	This field sets the V1P8A nominal regulator operating voltage. 00 – 1.880 V 01 – 1.850 V 10 – 1.830 V (Initial) 11 – 1.800 V	10
D[1]	MODE	VR MODE bit 0 – AUTO PWM/PFM mode (Initial) VR adjusts the operating mode (PFM/PWM) automatically based on the load current to maximize power efficiency. 1 – Forced PWM Mode VR operates in PWM mode only.	0

Table 4-11 BUCK5CTRL – V1P2A Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK5CTRL	R/W	-	-	-	-	BUCK5_VID[1:0]		MODE	-	0x0C	0x26

Bit	Name	Function	Initial
D[3:2]	BUCK5_VID[1:0]	This field sets the V1P2A nominal regulator operating voltage. 00 – 1.100 V 01 – 1.150 V 10 – 1.240 V 11 – 1.200 V (Initial)	11
D[1]	MODE	VR MODE bit 0 – AUTO PWM/PFM mode (Initial) VR adjusts the operating mode (PFM/PWM) automatically based on the load current to maximize power efficiency. 1 – Forced PWM Mode VR operates in PWM mode only.	0

4-2-4 VDDQ Control Register

Table 4-12 BUCK6CTRL – VDDQ Control Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
BUCK6CTRL	R/W	-	-	-	-	-	-	MODE	-	0x00	0x27

Bit	Name	Function	Initial
D[1]	MODE	VR MODE bit 0 – AUTO PWM/PFM mode (Initial) VR adjusts the operating mode (PFM/PWM) automatically based on the load current to maximize power efficiency. 1 – Forced PWM Mode VR operates in PWM mode only.	0

4-2-5 Discharge Circuit Registers

BD2671MWV supports discharge resistance values of 100Ω, 200Ω, 500Ω and high impedance settings and the resistance is independently programmable on every rail. Every discharge resistance is enabled only when the corresponding rail is disabled.

Table 4-13 DISCHCTRL1 – Discharge Control Register 1

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
DISCHCTRL1	R/W	BUCK4_DIS[1:0]		BUCK3_DIS[1:0]		BUCK2_DIS[1:0]		BUCK1_DIS[1:0]		0x55	0x40

Bit	Name	Function	Initial
D[7:6]	BUCK4_DIS[1:0]	V1P8A discharge resistance setting when V1P8A is disabled. 00 – function disabled 01 – 100 Ω (Initial) 10 – 200 Ω 11 – 500 Ω	01
D[5:4]	BUCK3_DIS[1:0]	VCCRAM discharge resistance setting when VCCRAM is disabled. 00 – function disabled 01 – 100 Ω (Initial) 10 – 200 Ω 11 – 500 Ω	01
D[3:2]	BUCK2_DIS[1:0]	VCCGI discharge resistance setting when VCCGI is disabled. 00 – function disabled 01 – 100 Ω (Initial) 10 – 200 Ω 11 – 500 Ω	01
D[1:0]	BUCK1_DIS[1:0]	VNN discharge resistance setting when VNN is disabled. 00 – function disabled 01 – 100 Ω (Initial) 10 – 200 Ω 11 – 500 Ω	01

Table 4-14 DISCHCTRL2 – Discharge Control Register 2

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
DISCHCTRL2	R/W	-	-	-	-	BUCK6_DIS[1:0]		BUCK5_DIS[1:0]		0x05	0x41

Bit	Name	Function	Initial
D[3:2]	BUCK6_DIS[1:0]	VDDQ discharge resistance setting when VDDQ is disabled. 00 – function disabled 01 – 100 Ω (Initial) 10 – 200 Ω 11 – 500 Ω	01
D[1:0]	BUCK5_DIS[1:0]	V1P2A discharge resistance setting when V1P2A is disabled. 00 – function disabled 01 – 100 Ω (Initial) 10 – 200 Ω 11 – 500 Ω	01

4-2-6 Power OK Delay Register

BD2671MWV supports programmable delays on PCH_PWROK assert timing which would wait for all the rails to be stable on various platforms.

Table 4-15 POK_DELAY – PCH_PWROK Power OK Delay

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
POK_DELAY	R/W	-	-	-	-	-	PWROKDELAY[2:0]			0x07	0x43

Bit	Name	Function	Initial
D[2:0]	PWROKDELAY[2:0]	Programmable wait time until all rails are stable to PCH_PWROK assert. 000 – 2.5 ms (This setting may violate the Gemini Lake SOC requirements. Minimum requirement is 5ms from Powergood OK to PCH_PWROK assertion.) 001 – 5.0 ms 010 – 10 ms 011 – 15 ms 100 – 20 ms 101 – 50 ms 110 – 75 ms 111 – 100 ms (Initial)	111

4-2-7 Interrupt & Status Registers

BD2671MWV supports an interrupt function asserting the IRQ_B pin. First and second level interrupt bits are allocated on each interrupt source to quickly determine the cause of the interrupt. Each first level interrupt bits are equipped with a mask register to mask the output to the IRQ_B pin. All first level registers are masked by default.
First and second level interrupt registers are not cleared by PMIC Shutdown and are capable of reading after the emergency shutdown for helping diagnostics caused by unexpected system failures. Any first or second level interrupt register can only be cleared by a write 1 or by PMIC POR.

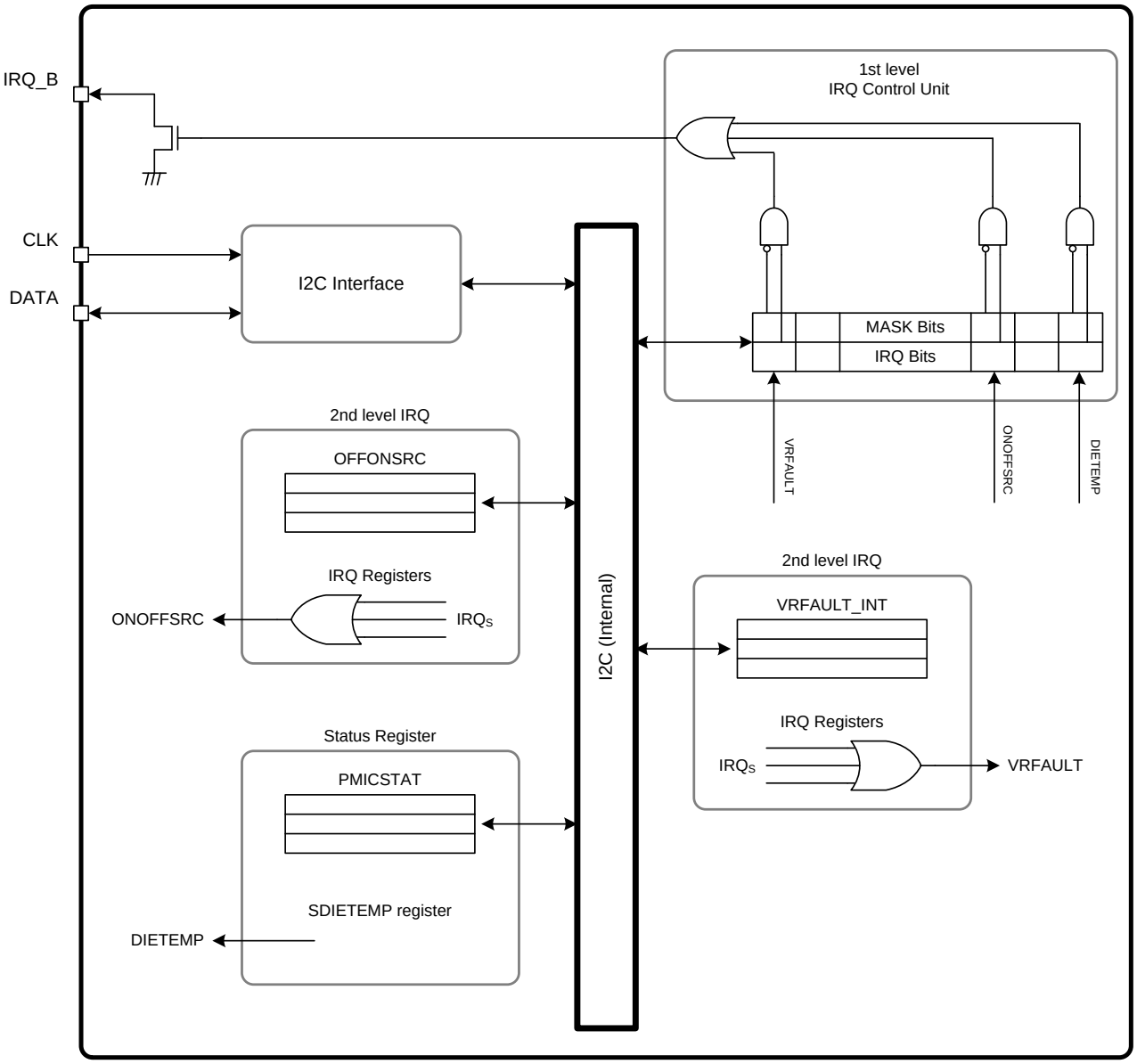


Figure 4-5 IRQ Architecture Block Diagram

Table 4-16 IRQ – PMIC First level Interrupt Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
IRQ	R/W	VRFAULT	-	-	-	-	ONOFFSRC	-	DIETEMP	0x00	0x02

Bit	Name	Function	Initial
D[7]	VRFAULT	PMIC Emergency Shutdown Event Interrupt. VRFAULT is set to 1 whenever the PMIC shuts down on VR voltage failure which is asserted by the VRFAULT_INT second level interrupt showing that the VR voltage has violated the nominal voltage range. 0 – Cleared or no interrupt 1 – PMIC Emergency Shutdown asserted by VRFAULT_INT second level interrupt. If the MVRFAULT bit is set to 0, this bit will result in the assertion of the IRQ_B pin, signaling an interrupt to the host. The host can clear this bit to 0 by writing a 1 to this register. Writing a 0 to this bit has no effect.	0
D[2]	ONOFFSRC	PMIC Emergency Shutdown Event Interrupt. ONOFFSRC is set to 1 whenever the PMIC shuts down on any cause which is asserted by the OFFONSRC second level interrupt. 0 – Cleared or no interrupt 1 – PMIC Emergency Shutdown asserted by OFFONSRC second level interrupt. If the MONOFFSRC bit is set to 0, this bit will result in the assertion of the IRQ_B pin, signaling an interrupt to the host. The host can clear this bit to 0 by writing a 1 to this register. Writing a 0 to this bit has no effect.	0
D[0]	DIETEMP	PMIC Die Temp Interrupt. DIETEMP is set to 1 whenever the PMIC Die Temp crosses the PMIC Die Temperature alert threshold (SDIETEMP register value changes, rising and falling). 0 – Cleared or no interrupt 1 – PMIC Die Temperature alert threshold crossed (SDIETEMP register value changes, rising and falling) If the MDIETEMP bit is set to 0, this bit will result in the assertion of the IRQ_B pin, signaling an interrupt to the host. The host can clear this bit to 0 by writing a 1 to this register. Writing a 0 to this bit has no effect.	0

Table 4-17 IRQ_MASK – PMIC First level Interrupt Mask Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
IRQ_MASK	R/W	MVRFAULT	-	-	-	-	MONOFFSRC	-	MDIETEMP	0x85	0x03

Bit	Name	Function	Initial
D[7]	MVRFAULT	PMIC Emergency Shutdown Event Interrupt Mask. Setting this bit to 1 masks the VRFAULT interrupt and prevents the assertion of the PMIC interrupt IRQ_B pin. 0 – Interrupt unmasked 1 – Interrupt masked (Initial) When the VRFAULT interrupt is asserted, setting the MVRFAULT bit to 1 can mask the interrupt factor to the IRQ_B pin so that the host can concentrate on other tasks.	1
D[2]	MONOFFSRC	PMIC Emergency Shutdown Event Interrupt Mask. Setting this bit to 1 masks the ONOFFSRC interrupt and prevents the assertion of the PMIC interrupt IRQ_B pin. 0 – Interrupt unmasked 1 – Interrupt masked (Initial) When the ONOFFSRC interrupt is asserted, setting the MONOFFSRC bit to 1 can mask the interrupt factor to the IRQ_B pin so that the host can concentrate on other tasks.	1
D[0]	MDIETEMP	PMIC Die Temp Interrupt Mask. Setting this bit to 1 masks the DIETEMP interrupt and prevents the assertion of the PMIC interrupt IRQ_B pin. 0 – Interrupt unmasked 1 – Interrupt masked (Initial) When the DIETEMP interrupt is asserted, setting the MDIETEMP bit to 1 can mask the interrupt factor to the IRQ_B pin so that the host can concentrate on other tasks.	1

Table 4-18 PMICSTAT – PMIC Status Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
PMICSTAT	R	-	-	-	-	-	-	-	SDIETEMP	0x00	0x04

Bit	Name	Function	Initial
D[0]	SDIETEMP	PMIC Die Temp status. The PMIC reflects the Die Temperature status to this register at all times. 0 – PMIC temperature is below Die Temp alert threshold. (Including hysterysis) 1 – PMIC temperature is above Die Temp alert threshold. When SDIETEMP is set to 1, PROCHOT_B is asserted immediately without any delay indicating the PMIC has crossed over the PMIC Die Temp alert threshold. PROCHOT_B is de-asserted the same time the SDIETEMP is cleared back to 0. This bit is a read only bit and cannot be cleared by the host.	0

Table 4-19 OFFONSRC – PMIC Power Transition Event Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
OFFONSRC	R/W	-	-	-	-	COLDOFF	UVLO	OCP	CRITTEMP	0x00	0x05

Bit	Name	Function	Initial
D[3]	COLDOFF	PMIC_EN coldoff assert Interrupt. COLDOFF is set to 1 when the PMIC emergency shutdown is asserted by the PMIC_EN Coldoff sequence. 0 – Cleared or no interrupt 1 – PMIC shutdown due to PMIC_EN Coldoff sequence detect When this bit is set to 1, it also sets 1 to the ONOFFSRC bit in the IRQ first level interrupt register. Ths host can clear this bit to 0 by writing a 1 to this register. Writing a 0 to this bit has no effect.	0
D[2]	UVLO	VSYS UVLO Interrupt. UVLO is set to 1 when the PMIC emergency shutdown is asserted by the VSYS UVLO detect. 0 – Cleared or no interrupt 1 – PMIC shutdown due to VSYS UVLO event (VSYS is below 5.4V) When this bit is set to 1, it also sets 1 to the ONOFFSRC bit in the IRQ first level interrupt register. Ths host can clear this bit to 0 by writing a 1 to this register. Writing a 0 to this bit has no effect.	0
D[1]	OCP	VR OCP Interrupt. OCP is set to 1 when the PMIC emergency shutdown is asserted by the VR OCP fault detect. 0 – Cleared or no interrupt 1 – PMIC shutdown due to VR OCP fault event When this bit is set to 1, it also sets 1 to the ONOFFSRC bit in the IRQ first level interrupt register. Ths host can clear this bit to 0 by writing a 1 to this register. Writing a 0 to this bit has no effect.	0
D[0]	CRITTEMP	PMIC Critical Temp Interrupt. CRITTEMP is set to 1 when the PMIC emergency shutdown is asserted by the PMIC Critical Temperature detect. 0 – Cleared or no interrupt 1 – PMIC shutdown due to PMIC Critical Temp event When this bit is set to 1, it also sets 1 to the ONOFFSRC bit in the IRQ first level interrupt register. Ths host can clear this bit to 0 by writing a 1 to this register. Writing a 0 to this bit has no effect.	0

Table 4-20 VRFAULT_INT – PMIC VR Voltage Failure Event Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
VRFAULT_INT	R/W	-	-	VDDQFAULT	V1P2A_FAULT	V1P8A_FAULT	VCCRAM_FAULT	VCCGI_FAULT	VNN_FAULT	0x00	0x83

Bit	Name	Function	Initial
D[5]	VDDQ_FAULT	VDDQ Voltage Regulation Failure Event. VDDQ_FAULT is set to 1 when the PMIC emergency shutdown is asserted by the VDDQ Voltage violation. 0 – Cleared or no interrupt 1 – PMIC shutdown due to VDDQ Voltage violation detect When this bit is set to 1, it also sets 1 to the VRFAULT bit in the IRQ first level interrupt register. Ths host can clear this bit to 0 by writing a 1 to this register. Writing a 0 to this bit has no effect.	0
D[4]	V1P2A_FAULT	V1P2A Voltage Regulation Failure Event. V1P2A_FAULT is set to 1 when the PMIC emergency shutdown is asserted by the V1P2A Voltage violation. 0 – Cleared or no interrupt 1 – PMIC shutdown due to V1P2A Voltage violation detect When this bit is set to 1, it also sets 1 to the VRFAULT bit in the IRQ first level interrupt register. Ths host can clear this bit to 0 by writing a 1 to this register. Writing a 0 to this bit has no effect.	0
D[3]	V1P8A_FAULT	V1P8A Voltage Regulation Failure Event. V1P8A_FAULT is set to 1 when the PMIC emergency shutdown is asserted by the V1P8A Voltage violation. 0 – Cleared or no interrupt 1 – PMIC shutdown due to V1P8A Voltage violation detect When this bit is set to 1, it also sets 1 to the VRFAULT bit in the IRQ first level interrupt register. Ths host can clear this bit to 0 by writing a 1 to this register. Writing a 0 to this bit has no effect.	0
D[2]	VCCRAM_FAULT	VCCRAM Voltage Regulation Failure Event. VCCRAM_FAULT is set to 1 when the PMIC emergency shutdown is asserted by the VCCRAM Voltage violation. 0 – Cleared or no interrupt 1 – PMIC shutdown due to VCCRAM Voltage violation detect When this bit is set to 1, it also sets 1 to the VRFAULT bit in the IRQ first level interrupt register. Ths host can clear this bit to 0 by writing a 1 to this register. Writing a 0 to this bit has no effect.	0
D[1]	VCCGI_FAULT	VCCGI Voltage Regulation Failure Event. VCCGI_FAULT is set to 1 when the PMIC emergency shutdown is asserted by the VCCGI Voltage violation. 0 – Cleared or no interrupt 1 – PMIC shutdown due to VCCGI Voltage violation detect When this bit is set to 1, it also sets 1 to the VRFAULT bit in the IRQ first level interrupt register. Ths host can clear this bit to 0 by writing a 1 to this register. Writing a 0 to this bit has no effect.	0
D[0]	VNN_FAULT	VNN Voltage Regulation Failure Event. VNN_FAULT is set to 1 when the PMIC emergency shutdown is asserted by the VNN Voltage violation. 0 – Cleared or no interrupt 1 – PMIC shutdown due to VNN Voltage violation detect When this bit is set to 1, it also sets 1 to the VRFAULT bit in the IRQ first level interrupt register. Ths host can clear this bit to 0 by writing a 1 to this register. Writing a 0 to this bit has no effect.	0

4-2-8 Vendor and Revision ID Registers

Table 4-21 VENDORID – PMIC Vendor ID Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
VENDORID	R	VENDORID[7:0]								0x1F	0x00

Bit	Name	Function	Initial
D[7:0]	VENDORID[7:0]	8-bit specific Vendor ID register.	00011111

Table 4-22 REVID – PMIC Revision ID Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
REVID	R	-	-	MAJREV[2:0]			MINREV[2:0]			0x00	0x01

Bit	Name	Function	Initial
D[5:3]	MAJREV[2:0]	Major Silicon revision ID. 000 – A 001 – B 010 – C 011 – D 100 – E 101 – F 110 – G 111 – H	000
D[2:0]	MINREV[2:0]	Minor Silicon revision ID. 000 – 0 001 – 1 010 – 2 011 – 3 100 – 4 101 – 5 110 – 6 111 – 7	000

4-2-9 VCCGI OCP and Switching Frequency Adjust Registers

Table 4-23 VCCGI_CLIM – VCCGI OCP Trip Point Threshold Adjust Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
VCCGI_CLIM	R/W	-	-	-	-	-	VCCGI_LIMSEL[2:0]			0x04	0x80

Bit	Name	Function	Initial
D[2:0]	VCCGI_LIMSEL[2:0]	VCCGI OCP Trip Point Threshold 000 – 9.5A 001 – 16.0A 010 – 22.5A 011 – 29.0A 100 – 35.5A (Initial) 101 – 42.0A 110 – 48.5A 111 – 55.0A Needs to unlock the register to overwrite by setting the UNLOCK register to 1. (0x82 D[0]) Prohibited to change the value when VCCGI is operating.	100

Table 4-24 VCCGI_FSW – VCCGI Switching Frequency Adjust Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
VCCGI_FSW	R/W	-	-	-	-	-	-	VCCGI_CLKSEL[1:0]		0x01	0x81

Bit	Name	Function	Initial
D[1:0]	VCCGI_CLKSEL[1:0]	VCCGI Switching Frequency control 00, 11, 10 – This mode is not supported. Do not use this setting. 01 – 666kHz (Initial) Needs to unlock the register to overwrite by setting the UNLOCK register to 1. (0x82 D[0]) Prohibited to change the value when VCCGI is operating.	01

4-2-10 UNLOCK register for Vendor Specific Registers Write Protect

Table 4-25 UNLOCK – Vendor Specific Register Unlock Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
UNLOCK	R/W	-	-	-	-	-	-	-	UNLOCK	0x00	0x82

Bit	Name	Function	Initial
D[0]	UNLOCK	Used for unlocking the write protect on VCCGI_CLIM, VCCGI_FSW, VDDQ_CLIM, VDDQ_FSW, VDDQ_DDR, VDDQ_VSEL and VPP_VSEL registers. 0 – Vendor Registers are write protected (Initial) 1 – Vendor Registers are unlocked and capable of writing This register is to avoid unexpected behaviors when there is any unwanted or malicious writing to the Vendor Specific Registers.	0

4-2-11 VDDQ OCP and Switching Frequency Adjust Registers

Table 4-26 VDDQ_CLIM – VDDQ OCP Trip Point Threshold Adjust Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
VDDQ_CLIM	R/W	-	-	-	-	-	VDDQ_LIMSEL[2:0]			0x01	0x85

Bit	Name	Function	Initial
D[2:0]	VDDQ_LIMSEL[2:0]	VDDQ OCP Trip Point Threshold 000 – 9.5A 001 – 16.0A (Initial) 010 – 22.5A 011 – 29.0A 100, 101, 110, 111 - This setting is not supported. Do not use this setting. Needs to unlock the register to overwrite by setting the UNLOCK register to 1. (0x82 D[0]) Prohibited to change the value when VDDQ is operating.	001

Table 4-27 VDDQ_FSW – VDDQ Switching Frequency Adjust Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
VDDQ_FSW	R/W	-	-	-	-	-	-	VDDQ_CLKSEL[1:0]		0x02	0x86

Bit	Name	Function	Initial
D[1:0]	VDDQ_CLKSEL[1:0]	VDDQ Switching Frequency control 00, 01, 11 – This mode is not supported. Do not use this setting. 10 – 750kHz (Initial) Needs to unlock the register to overwrite by setting the UNLOCK register to 1. (0x82 D[0]) Prohibited to change the value when VDDQ is operating.	10

4-2-12 VDDQ and VPP On-The-Fly DDR Voltage Change Registers

Table 4-28 VDDQ_DDR – VDDQ and VPP On-The-Fly DDR Voltage Change Register

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
VDDQ_DDR	R/W	-	-	-	-	VPP_DDR_SYNC	VDDQ_DDR_REGEN	VDDQ_DDR[1:0]		0x00	0x88

Bit	Name	Function	Initial
D[3]	VPP_DDR_SYNC	VPP On-The-Fly Voltage Change register control enable 0 – VPP voltage is set by the DDR_SEL2,1,0 pin configuration (Initial) 1 – VPP voltage corresponds to the VDDQ_DDR[1:0] register setting when VDDQ_DDR_REGEN=1 VPP voltage is set to 1.800V when VDDQ_DDR[1:0]=”00”,”01”,”10” and 2.500V when VDDQ_DDR[1:0]=”11”. This register is valid only when VDDQ_DDR_REGEN=1. Needs to unlock the register to overwrite by setting the UNLOCK register to 1. (0x82 D[0]) This register is resetted to its initial value when the power state is down to PMIC_G3.	0
D[2]	VDDQ_DDR_REGEN	VDDQ On-The-Fly Voltage Change register control enable 0 – VDDQ voltage control by DDR_SEL2,1,0 pin configuration (Initial) 1 – VDDQ voltage control by VDDQ_DDR[1:0] register Needs to unlock the register to overwrite by setting the UNLOCK register to 1. (0x82 D[0]) This register is resetted to its initial value when the power state is down to PMIC_G3.	0
D[1:0]	VDDQ_DDR[1:0]	VDDQ On-The-Fly Voltage Change control 00 – 1.200V (LPDDR3) (Initial) 01 – 1.350V (DDR3L) 10 – 1.100V (LPDDR4) 11 – 1.200V (DDR4) Needs to unlock the register to overwrite by setting the UNLOCK register to 1. (0x82 D[0]) This register is resetted to its initial value when the power state is down to PMIC_G3.	00

4-2-13 VDDQ Voltage Adjust Registers

Table 4-29 VDDQ_VSEL – VDDQ Voltage Adjust Registers

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
VDDQ_VSEL	R/W	-	-	-	-	-	VDDQ_VSEL[2:0]			0x04	0x89

Bit	Name	Function	Initial
D[2:0]	VDDQ_VSEL[2:0]	VDDQ output voltage adjust The Vnom voltage level depends on the DDR_SEL2, 1, 0 pin configuration. 000 = Vnom +40mV 001 = Vnom +30mV 010 = Vnom +20mV 011 = Vnom +10mV 100 = Vnom (Initial) 101 = Vnom -10mV 110 = Vnom -20mV 111 = Vnom -30mV Needs to unlock the register to overwrite by setting the UNLOCK register to 1. (0x82 D[0])	100

4-2-14 VPP Voltage Adjust Registers

Table 4-30 VPP_VSEL – VPP Voltage Adjust Registers

Register Name	R/W	D7	D6	D5	D4	D3	D2	D1	D0	Initial	Address
VPP_VSEL	R/W	-	-	-	-	-	-	VPP_VSEL[1:0]		0x02	0x8A

Bit	Name	Function	Initial
D[1:0]	VPP_VSEL[1:0]	VPP output voltage adjust The Vnom voltage level depends on the DDR_SEL2, 1, 0 pin configuration. (1.8V / 2.5V) 00 = Vnom +3% 01 = Vnom +2% 10 = Vnom (Initial) 11 = Vnom -2% Needs to unlock the register to overwrite by setting the UNLOCK register to 1. (0x82 D[0])	10

4-3 Sideband Signals

4-3-1 Sideband Signals Block Diagram

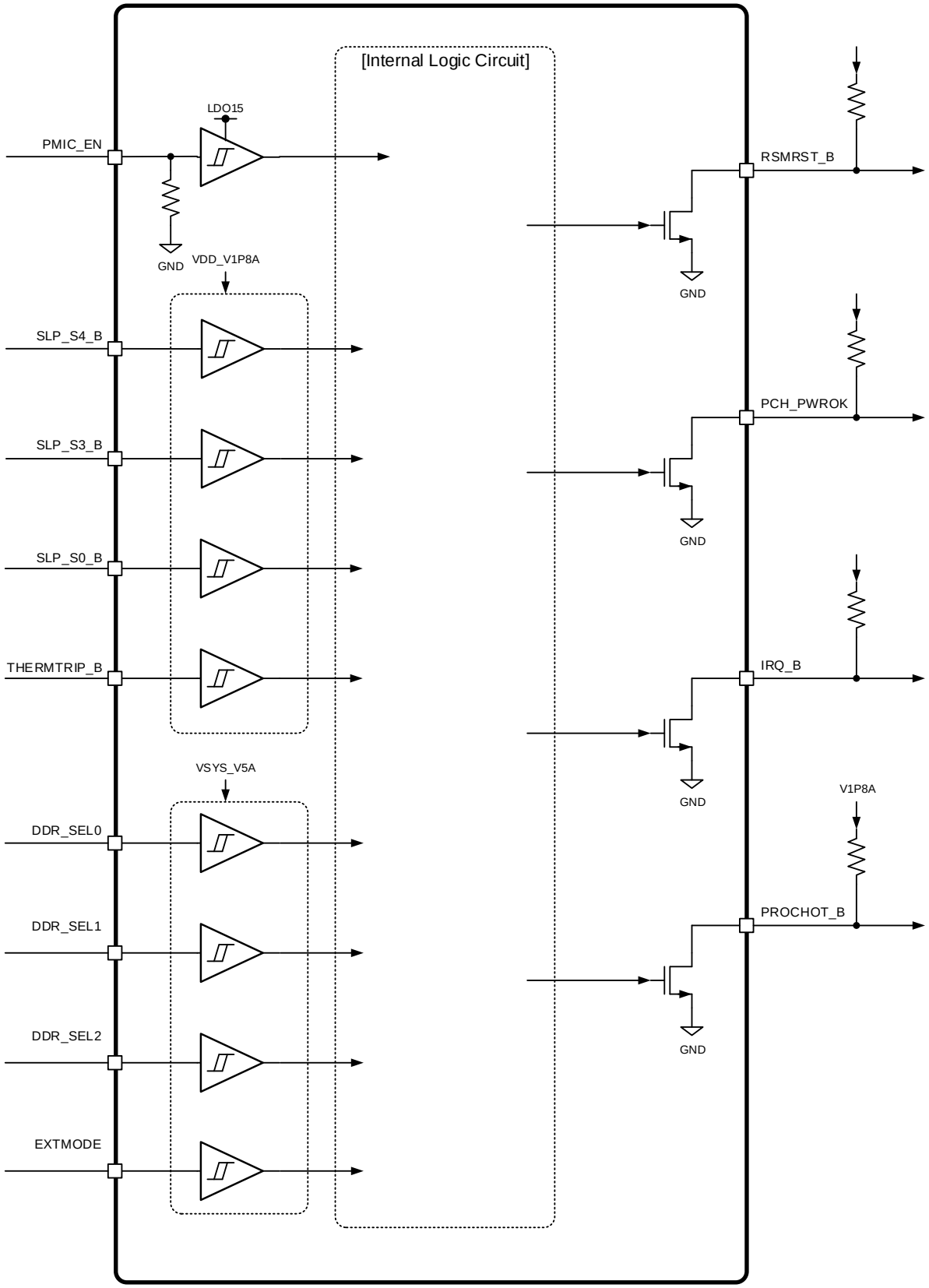


Figure 4-6 Sideband Signals Block Diagram

4-3-2 Sideband Signals Electrical Characteristics

Table 4-31 Sideband Signals Electrical Characteristics

Unless otherwise specified, Ta=25°C, VSYS=12.6V, VSYS_V5A=5.0V, VDD_V1P8A=V1P8A=1.800V

Parameter	Symbol	Limit.			Unit	Remarks
		Min	Typ	Max		
PMIC_EN						
Input Low Voltage	V_{IL_PEN}	-0.3	-	0.63	V	VDD=VSYS_V5A
Input High Voltage	V_{IH_PEN}	1.17	-	VDD +0.3	V	VDD=VSYS_V5A
Input Pull-down resistance	Z_{IN_PEN}	-	5	-	MΩ	
SLP_S0_B, SLP_S3_B, SLP_S4_B, THERMTRIP_B						
Input Low Voltage	V_{IL}	-0.3	-	VDD x 0.35	V	VDD=VDD_V1P8A
Input High Voltage	V_{IH}	VDD x 0.65	-	5.5	V	VDD=VDD_V1P8A
Input Hysteresis	V_{HYS}	0.1	-	-	V	
DDR_SEL0, DDR_SEL1, DDR_SEL2, EXTMODE						
Input Low Voltage	V_{IL}	-0.3	-	VDD x 0.35	V	VDD=VSYS_V5A
Input High Voltage	V_{IH}	VDD x 0.65	-	VDD + 0.3	V	VDD=VSYS_V5A
RSMRST_B, PCH_PWROK, IRQ_B (Open Drain)						
Output Low Voltage	V_{OL}	-	-	0.36	V	I_{IN}=3mA
Leak Current	I_{LK}	-	-	1	μA	Vin=5V, Nch Open Drain=OPEN
PROCHOT_B (Open Drain)						
Output Low Voltage	V_{OL_PRC}	-	-	0.36	V	I_{IN}=18mA (1.8V/100Ω)
Leak Current	I_{LK_PRC}	-	-	1	μA	Vin=5V, Nch Open Drain=OPEN

4-3-3 RSMRST_B

RSMRST_B is an active low dedicated output pin. RSMRST_B is actively driven to low in PMIC G3 state. The nominal voltage of RSMRST_B is 0V when asserted, 1.8V-3.3V (Depending on the external pullup voltage) when de-asserted.
When any rail detects a fault or if any other emergency shutdown event is detected, RSMRST_B is asserted immediately.

4-3-4 PCH_PWROK

PCH_PWROK is an active high dedicated output pin. PCH_PWROK is actively driven to high in S0IX or S0 state when there are no faults in the system. The nominal voltage of PCH_PWROK is 0V when de-asserted, 1.8V-3.3V (Depending on the external pullup voltage) when asserted.
When any rail detects a fault or any other emergency shutdown event is detected, PCH_PWROK is de-asserted immediately.

4-3-5 SLP_S0_B

SLP_S0_B is an active low dedicated input signal from the SOC that indicates S0IX state entry upon assertion (SLP_S0_B=LOW) and exit upon de-assertion (SLP_S0_B=HIGH). The assertion of the SLP_S0_B signal from the SOC launches S0IX state entry.
It is valid after the first PCH_PWROK is asserted. It is treated as H when invalid. The nominal voltage of SLP_S0_B is 0V when asserted, 1.8V (3.3V tolerant) when de-asserted.

4-3-6 SLP_S3_B

SLP_S3_B is an active low dedicated input signal from the SOC that indicates S3 state entry upon assertion (SLP_S3_B=LOW) and exit upon de-assertion (SLP_S3_B=HIGH). The assertion of the SLP_S3_B signal from the SOC launches S3 state entry.
It is valid when RSMRST_B is de-asserted. It is treated as L when invalid. The nominal voltage of SLP_S3_B is 0V when asserted, 1.8V (3.3V tolerant) when de-asserted.

4-3-7 SLP_S4_B

SLP_S4_B is an active low dedicated input signal from the SOC that indicates S4/S5 state entry upon assertion (SLP_S4_B=LOW) and exit upon de-assertion (SLP_S4_B=HIGH). The assertion of the SLP_S4_B signal from the SOC launches S4/S5 state entry.
It is valid when RSMRST_B is de-asserted. It is treated as L when invalid. The nominal voltage of SLP_S4_B is 0V when asserted, 1.8V (3.3V tolerant) when de-asserted.

4-3-8 THERMTRIP_B

THERMTRIP_B is an active low dedicated input signal that indicates that the SOC is thermally hot. The assertion of the THERMTRIP_B signal will immediately launch an emergency shutdown.
It is valid when RSMRST_B is de-asserted. It is treated as H when invalid. The nominal voltage of THERMTRIP_B is 0V when asserted, 1.8V (3.3V tolerant) when de-asserted.

4-3-9 IRQ_B

IRQ_B is an active low dedicated output pin that generates interrupts to the SOC. It is asserted when at least one unmasked interrupt bit is set in the 1st level interrupt register. It is valid when RSMRST_B is de-asserted. The nominal voltage of IRQ is 0V when asserted, 1.8V-3.3V (Depending on the external pullup voltage) when de-asserted.

4-3-10 PROCHOT_B

PROCHOT_B is an active low dedicated output pin used to notify the SOC a PMIC thermal event. PROCHOT_B is asserted if the BD2671MWV die temperature rises above the internal warning alert threshold, for 130ºC, to prevent the PMIC from reaching the critical temperature which leads to an emergency shutdown. It is valid when RSMRST_B is de-asserted. The nominal voltage of PROCHOT_B is 0V when asserted, 1.8V-3.3V (depending on the external pullup voltage) when de-asserted. The SOC should go into a lower power state and stay until the BD2671MWV thermal status register SDIETEMP is cleared to 0 and the PROCHOT_B pin is de-asserted.

4-3-11 DDR_SEL0, DDR_SEL1, DDR_SEL2

DDR_SEL0,1,2 are dedicated input pins used to select the VDDQ operating voltage to meet the LPDDR3, DDR3L, LPDDR4 and DDR4 voltage specifications. The VDDQ voltage can either be set to 1.200V(LPDDR3, DDR4), 1.350V(DDR3L) or 1.100V(LPDDR4).
Also, DDR_SEL0,1,2 can be used to change the operation of LDO_VPP control, V1P2A merge to VDDQ modes and VTT control options.
LDO_VPP can be selected to be controlled by SLP_S3_B which can be used as an optional LDO output when selecting DDR3L(DDR_SEL2,1,0=H,L,H) since LDO_VPP is not required in DDR3L systems.
V1P2A can be merged with VDDQ when selecting LPDDR3 or DDR4 for BOM cost savings. (DDR_SEL=H,L,L or H,H,H)
VTT can be selected to be OFF at LPDDR4. (DDR_SEL=H,H,L)

The nominal voltage of DDR_SEL0,1,2 is 0V when L, VSYS_V5A level as H.
Any dynamic change in DDR_SEL0,1,2 is not supported by BD2671MWV during operation and may violate VDDQ, VDDQ_VTT and LDO_VPP transient specifications. It is strongly recommended to always be connected to the GND or Power plane.

Table 4-32 DDR_SEL0,1 selection on VDDQ and LDO_VPP

DDR_SEL2,1,0	DDR selection	VDDQ voltage	LDO_VPP voltage	V1P2A Voltage	VTT Voltage	Description
(L,L,L)	LPDDR3	1.200V	1.800V	1.200V	0.600V	-
(L,L,H)	DDR3L	1.350V	OFF	1.200V	0.675V	LDO_VPP unused
(L,H,L)	LPDDR4	1.100V	1.800V	1.200V	0.550V	-
(L,H,H)	DDR4	1.200V	2.500V	1.200V	0.600V	-
(H,L,L)	LPDDR3	1.200V (V1P2A boot timing)	1.800V	OFF	0.600V	V1P2A merged to VDDQ
(H,L,H)	DDR3L	1.350V	1.800V (SLP_S3_B control)	1.200V	0.675V	LDO_VPP can be used as optional LDO
(H,H,L)	LPDDR4	1.100V	1.800V	1.200V	OFF	VTT unused
(H,H,H)	DDR4	1.200V (V1P2A boot timing)	2.500V	OFF	0.600V	V1P2A merged to VDDQ

4-3-12 EXTMODE

EXTMODE is a dedicated input pin used to select the VNN and VCCGI operation modes. Whenever there are cases when external VRs are used instead of the BD2671MWV internal VNN and VCCGI, BD2671MWV VNN and VCCGI can be disabled by setting EXTMODE as H. When set to L, the BD2671MWV VNN and VCCGI are both enabled.
The nominal voltage of EXTMODE is 0V when L, VSYS_V5A level as H. Any dynamic change in EXTMODE is not supported by BD2671MWV during operation and is strongly recommended to always be connected to the GND or Power plane to avoid any unexpected behavior.

Table 4-33 EXTMODE pin table

EXTMODE	VCCGI	VNN
L	Turn-on/off by I2C command	Turn-on/off by sequence or I2C command
H	VCCGI Disabled	VNN Disabled

When then VNN and VCCGI is disabled by the EXTMODE pin, no external components are required for VNN and VCCGI terminals.

5 Power Sequencing

5-1 Regulator Control Signal Summary

Table 5-1 Regulator Control Signal Summary

VR Control Signal	Rail Suffix	Power States when Rails Active
PMIC_EN	V1P8A V1P2A	S4/S5 - S0
SLP_S4_B	LDO_VPP VDDQ	S3 - S0
SLP_S0_B AND SLP_S3_B	VDDQ_VTT VCCRAM VNN VCCGI(Initial OFF, Power ON by I2C)	S0(off in S0IX)

When the BD2671MWV is first enabled by PMIC_EN, SLP_S4_B and SLP_S3_B are treated as if they are low and THERMTRIP_B treated as high until the de-assertion of RSMRST_B. BD2671MWV will honor the state of SLP_S4_B, SLP_S3_B and THERMTRIP_B after the de-assertion of RSMRST_B.

When the BD2671MWV is first enabled by PMIC_EN, SLP_S0_B is to be treated as if it is high until the first assertion of PCH_PWROK. BD2671MWV will honor the state of SLP_S0_B after the first assertion of PCH_PWROK.

This is to wait for the host to be able to take control of SLP_S3_B, SLP_S4_B, THERMTRIP_B and SLP_S0_B pins and assure there is no unintended power control to BD2671MWV.

SLP_S4_B, SLP_S3_B, THERMTRIP_B and SLP_S0_B are all re-masked again when BD2671MWV shuts down to PMIC_G3 state by any cause.

5-2 Power States

Figure 5-1 defines various system level power states. The sequencing for the transitions between these power states are defined in Section “5-5 G3 to S5/S4 & S5/S4 to S0 Power Sequence” through Section “5-15 PMIC_EN Emergency Shutdown Sequence and quick reboot by PMIC_EN”.

Table 5-2 Power State Summary

Power State	Host to PMIC					PMIC to Host	
	PMIC_EN	SLP_S4_B	SLP_S3_B	SLP_S0_B	THERMTRIP_B	RSMRST_B	PCH_PWROK
G3	-	-	-	-	-	-	-
PMIC_G3	L	-	-	-	-	L	L
S4/S5	H	L	-	-	H	H	L
S3	H	H	L	-	H	H	L
S0IX	H	H	H	L	H	H	H
S0	H	H	H	H	H	H	H

Power State transitions are consisted of PMIC_EN, SLP_S4_B, SLP_S3_B, SLP_S0_B and THERMTRIP_B pin controls. The Power State always honors the lower-state pin. The lower state pin is described in the order of PMIC_EN < SLP_S4_B < SLP_S3_B < SLP_S0_B which the SLP_S0_B is the highest state pin.
For example, if SLP_S3_B=H and SLP_S4_B=L, SLP_S4_B is honored and the Power State will transition to S4/S5 state.
At any Power State, PMIC_EN, THERMTRIP_B is always honored as the highest priority pins which either L will start the PMIC Shutdown immediately.

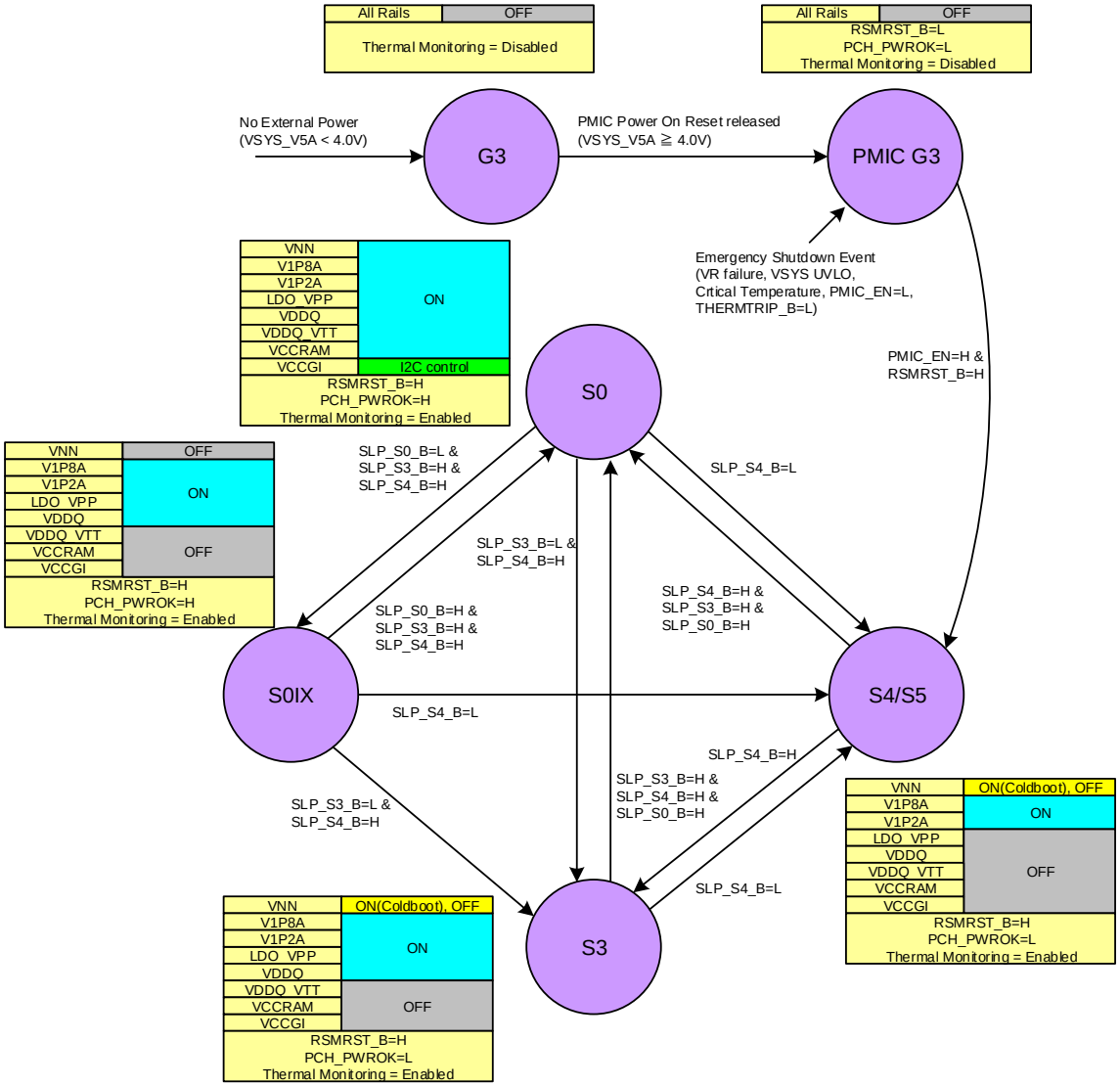


Figure 5-1 Power State transition diagram

To describe the BD2671MWV power management, six conceptual BD2671MWV states are defined. These states are characterized by the behavior of platform power rails, SOC sideband signals and internal state machines.

G3:

No valid platform power sources exist.
VSYS_V5A voltage is below Power-ON Reset level.

PMIC G3:

The BD2671MWV internal logic is powered.
PMIC is ready to boot by PMIC_EN.
This state is entered from G3 by inserting valid power sources or from other power states by either PMIC_EN=L or THERMTRIP_B=L or any other Emergency Shutdown event.

S4/S5:

Low power platform state which will be entered by asserting SLP_S4_B or Cold-boot sequence by the assertion of PMIC_EN.
VNN, V1P8A, V1P2A is ON. (VNN is only ON at the first cold-boot.)
RSMRST_B is de-asserted.
PCH_PWROK is de-asserted.

S3:

Low power platform state which will be entered by asserting SLP_S3_B.
VNN, V1P8A, V1P2A, LDO_VPP and VDDQ is ON. (VNN is only ON at the first cold-boot.)
RSMRST_B is de-asserted.
PCH_PWROK is de-asserted.

S0IX:

Low power platform state which will be entered by asserting SLP_S0_B.
V1P8A, V1P2A, LDO_VPP, VDDQ is ON.
RSMRST_B is de-asserted.
PCH_PWROK is asserted.

S0:

All rails have been powered up.
SLP_S3_B=H, SLP_S4_B=H, SLP_S0_B=H.
VNN, VCCGI, VCCRAM, V1P8A, V1P2A, VDDQ, VDDQ_VTT, LDO_VPP is ON.
(The host may choose to power up/down VNN or VCCGI by I2C. VCCGI is set to 0V as default and needs an I2C command to turn ON.)
RSMRST_B is de-asserted.
PCH_PWROK is asserted.

5-2-1 G3 State

In the “G3” state, the BD2671MWV is completely powered off, with no valid power source available on the platform. To enter this state, all power sources must have been removed from the system or VSYS_V5A < POR.

In this state, no rails are in regulation. No BD2671MWV logic is alive. In this state, the device appears to be “off” to the user. Exiting from this state is triggered by the application of a valid power source. Transitions out of this state are summarized in Table 5-3.

The event causing a transition out of the G3 state is shown in the table below.

Table 5-3 G3 State Transition Table

Event Trigger	Conditions (All must be satisfied)	Next State	Notes
VSYS_V5A Insertion	VSYS_V5A > POR	PMIC G3	

5-2-2 PMIC G3 State

In the “PMIC G3” state, only internal voltage regulators in the BD2671MWV are ON.
This is the lowest power consumption state with the valid power source supplied.
PMIC is ready to boot by PMIC_EN.
PMIC internal thermal monitoring is disabled.
SLP_S3_B, SLP_S4_B is masked to L, THERMTRIP_B, SLP_S0_B is masked to H.
RSMRST_B and PCH_PWROK are both set to L output.
I2C interface is not available since the I2C I/O is not powered.

The events causing a transition out of the PMIC G3 state are shown in the table below.

Table 5-4 PMIC G3 State Transition Table

Event Trigger	Conditions (All must be satisfied)	Next State	Notes
Removal / Depletion of VSYS_V5A	VSYS_V5A < POR	G3	-
Cold boot trigger	PMIC_EN=H RSMRST_B=H	S4/S5	V1P8A, V1P2A Power good signals needs to be at OK state.

5-2-3 S4/S5 State

The entering and exiting of the S4/S5 state is controlled by a signal which is delivered to the BD2671MWV by the SOC via SLP_S4_B.

Rails that are “ON” :
- VNN=ON (Only ON during the first cold boot)
- V1P8A=ON
- V1P2A=ON (V1P2A is OFF when set in V1P2A to VDDQ merged mode)

Interfaces available :
- I2C is always available in S4/S5.

Interrupts active and IRQ_B operational.
PMIC internal thermal monitoring enabled and PROCHOT_B operational.
SLP_S3_B, SLP_S4_B, THERMTRIP_B mask is removed and the signals are honored.
SLP_S0_B is masked to H during the first cold boot. (Once PCH_PWROK is asserted, SLP_S0_B is always honored until PMIC shutdown)
RSMRST_B=H, PCH_PWROK=L.

The events causing a transition out of the S4/S5 state are shown in the table below.

Table 5-5 S4/S5 State Transition Table

Event Trigger	Conditions (All must be satisfied)	Next State	Notes
Removal / Depletion of VSYS_V5A	VSYS_V5A < POR	G3	-
Emergency shutdown (PMIC_EN)	PMIC_EN=L	PMIC G3	Interrupt factors are read from OFFONSRC (COLDOFF) register.
Emergency shutdown (THERMTRIP_B)	THERMTRIP_B=L		-
Emergency shutdown (Critical Temperature)	Critical Temperature failure		Interrupt factors are read from OFFONSRC (CRITTEMP) register.
Emergency shutdown (VSYS UVLO)	VSYS < 5.4V		Interrupt factors are read from OFFONSRC (UVLO) register.
Emergency shutdown (VR OCP failure)	V1P8A OCP failure or V1P2A OCP failure		Interrupt factors are read from OFFONSRC (OCP) register.
Emergency shutdown (VR Voltage failure)	V1P8A Voltage failure or V1P2A Voltage failure		Interrupt factors are read from VRFAULT (VRFAULT_INT) register.
Exit S4/S5 state	SLP_S4_B=H SLP_S3_B=L	S3	-
Exit S4/S5 state	SLP_S4_B=H SLP_S3_B=H SLP_S0_B=H	S0	SLP_S0_B is masked to H until the first PCH_PWROK assertion after the cold boot.

5-2-4 S3 State

The entering and exiting of the S3 state is controlled by a signal which is delivered to the BD2671MWV by the SOC via SLP_S3_B.

Rails that are “ON”:
- VNN=ON (Only ON during the first cold boot)
- V1P8A=ON
- V1P2A=ON (V1P2A is OFF when set in V1P2A to VDDQ merged mode)
- LDO_VPP=ON
- VDDQ=ON

Interfaces available:
- I2C is always available in S3.

Interrupts active and IRQ_B operational.
PMIC internal thermal monitoring enabled and PROCHOT_B operational.
SLP_S3_B, SLP_S4_B, THERMTRIP_B mask is removed and the signals are honored.
SLP_S0_B is masked to H during the first cold boot. (Once PCH_PWROK is asserted, SLP_S0_B is always honored until PMIC shutdown)
RSMRST_B=H, PCH_PWROK=L.

The events causing a transition out of the S3 state are shown in the table below.

Table 5-6 S3 State Transition Table

Event Trigger	Conditions (All must be satisfied)	Next State	Notes
Removal / Depletion of VSYS_V5A	VSYS_V5A < POR	G3	-
Emergency shutdown (PMIC_EN)	PMIC_EN=L	PMIC G3	Interrupt factors are read from OFFONSRC (COLDOFF) register.
Emergency shutdown (THERMTRIP_B)	THERMTRIP_B=L		-
Emergency shutdown (Critical Temperature)	Critical Temperature failure		Interrupt factors are read from OFFONSRC (CRITTEMP) register.
Emergency shutdown (VSYS UVLO)	VSYS < 5.4V		Interrupt factors are read from OFFONSRC (UVLO) register.
Emergency shutdown (VR OCP failure)	V1P8A OCP failure or V1P2A OCP failure or VDDQ OCP failure		Interrupt factors are read from OFFONSRC (OCP) register.
Emergency shutdown (VR Voltage failure)	V1P8A Voltage failure or V1P2A Voltage failure or VDDQ Voltage failure		Interrupt factors are read from VRFAULT (VRFAULT_INT) register.
Enter S4/S5 state	SLP_S4_B=L	S4/S5	-
Exit S3 state	SLP_S4_B=H SLP_S3_B=H SLP_S0_B=H	S0	SLP_S0_B is masked to H until the first PCH_PWROK assertion after the cold boot.

5-2-5 S0IX State

The entering and exiting of the S0IX state is controlled by a signal which is delivered to the BD2671MWV by the SOC via SLP_S0_B.

Rails that are “ON”:
- V1P8A=ON
- V1P2A=ON (V1P2A is OFF when set in V1P2A to VDDQ merged mode)
- LDO_VPP=ON
- VDDQ=ON

Interfaces available:
- I2C is always available in S0IX.

Interrupts active and IRQ_B operational.
PMIC internal thermal monitoring enabled and PROCHOT_B operational.
SLP_S3_B, SLP_S4_B, THERMTRIP_B, SLP_S0_B mask is removed and all signals are honored.
RSMRST_B=H, PCH_PWROK=H.

The events causing a transition out of the S0IX state are shown in the table below.

Table 5-7 S0IX State Transition Table

Event Trigger	Conditions (All must be satisfied)	Next State	Notes
Removal / Depletion of VSYS_V5A	VSYS_V5A < POR	G3	-
Emergency shutdown (PMIC_EN)	PMIC_EN=L	PMIC G3	Interrupt factors are read from OFFONSRC (COLDOFF) register.
Emergency shutdown (THERMTRIP_B)	THERMTRIP_B=L		-
Emergency shutdown (Critical Temperature)	Critical Temperature failure		Interrupt factors are read from OFFONSRC (CRITTEMP) register.
Emergency shutdown (VSYS UVLO)	VSYS < 5.4V		Interrupt factors are read from OFFONSRC (UVLO) register.
Emergency shutdown (VR OCP failure)	V1P8A OCP failure or V1P2A OCP failure or VDDQ OCP failure		Interrupt factors are read from OFFONSRC (OCP) register.
Emergency shutdown (VR Voltage failure)	V1P8A Voltage failure or V1P2A Voltage failure or VDDQ Voltage failure		Interrupt factors are read from VRFAULT (VRFAULT_INT) register.
Enter S4/S5 state	SLP_S4_B=L	S4/S5	-
Enter S3 state	SLP_S4_B=H SLP_S3_B=L	S3	-
Exit S0IX state	SLP_S4_B=H SLP_S3_B=H SLP_S0_B=H	S0	-

5-2-6 S0 State

In the S0 State, the BD2671MWV has completed bringing up the platform, and the reset is released for the SOC.
All rails are fully operational, and the SOC has full control of the system through commands issued over the I2C interface and sideband signals.
In this state, the device will appear “ON” to the user.

Rails that are “ON”:
- VNN=ON
- V1P8A=ON
- V1P2A=ON (V1P2A is OFF when set in V1P2A to VDDQ merged mode)
- LDO_VPP=ON
- VDDQ=ON
- VCCRAM=ON
- VDDQ_VTT=ON
- VCCGI=ON (Host needs to turn ON by I2C)

Interfaces available:
- I2C is always available in S0.

Interrupts active and IRQ_B operational.
PMIC internal thermal monitoring enabled and PROCHOT_B operational.
SLP_S3_B, SLP_S4_B, THERMTRIP_B, SLP_S0_B mask is removed and all signals are honored.
RSMRST_B=H, PCH_PWROK=H.

The events causing a transition out of the S0 state are shown in the table below.

Table 5-8 S0 State Transition Table

Event Trigger	Conditions (All must be satisfied)	Next State	Notes
Removal / Depletion of VSYS_V5A	VSYS_V5A < POR	G3	-
Emergency shutdown (PMIC_EN)	PMIC_EN=L	PMIC G3	Interrupt factors are read from OFFONSRC (COLDOFF) register.
Emergency shutdown (THERMTRIP_B)	THERMTRIP_B=L		-
Emergency shutdown (Critical Temperature)	Critical Temperature failure		Interrupt factors are read from OFFONSRC (CRITTEMP) register.
Emergency shutdown (VSYS UVLO)	VSYS < 5.4V		Interrupt factors are read from OFFONSRC (UVLO) register.
Emergency shutdown (VR OCP failure)	VNN OCP failure or VCCGI OCP failure or VCCRAM OCP failure or V1P8A OCP failure or V1P2A OCP failure or VDDQ OCP failure		Interrupt factors are read from OFFONSRC (OCP) register.
Emergency shutdown (VR Voltage failure)	VNN Voltage failure or VCCGI Voltage failure or VCCRAM Voltage failure or V1P8A Voltage failure or V1P2A Voltage failure or VDDQ Voltage failure		Interrupt factors are read from VRFAULT (VRFAULT_INT) register.
Enter S4/S5 state	SLP_S4_B=L	S4/S5	-
Enter S3 state	SLP_S4_B=H SLP_S3_B=L	S3	-
Exit S0IX state	SLP_S4_B=H SLP_S3_B=H SLP_S0_B=L	S0IX	-

5-3 Cold Boot

A cold boot sequence is followed whenever BD2671MWV is fully turning on the system from PMIC G3 state. As such, a cold boot sequence begins at the “PMIC G3” state, and terminates at the “S0” state.

PMIC_EN is used to trigger the BD2671MWV to bring up the VNN, V1P8A and V1P2A rails and de-assert the RSMRST_B. During this cold boot transition, the sleep signal (SLP_S3_B, SLP_S4_B) is masked to an asserted position and THERMTRIP_B signal is masked to a non-asserted position until the first RSMRST_B is de-asserted. The host needs to take complete control to go higher than S4/S5 state. Once it reaches the S0 state and the VCCRAM turns on, after a register defined delay the PCH_PWROK signal will assert. This will effectively turn on the SOC in order to begin executing codes for controlling the system.
Also the SLP_S0_B signal is masked to a non-asserted position until the first PCH_PWROK is asserted so that the system is ensured to come up to the S0 state for the first cold boot.

5-4 Power Good Definitions

Table 5-9 defines the various PMIC Power Good signals.

Table 5-9 Power Good Summary

Power Good	PMIC Qualifying Signals (Logical AND)	Notes
RSMRST_B	PMIC POR released (VSYS_V5A > 4.0V) No PMIC Critical Thermal errors VSYS voltage OK (> 5.6V) THERMTRIP_B=H (Masked to H during the first cold boot until RSMRST_B becomes H) PMIC_EN=H VNN Power Good (Masked to H when OFF and until the first PCH_PWROK is asserted) V1P8A Power Good V1P2A Power Good VCCRAM Power Good (Masked to H when OFF) VCCGI Power Good (Masked to H when OFF) VDDQ Power Good (Masked to H when OFF)	PCH_PWROK will immediately de-assert at the loss of any of the qualifying signals, or at the occurrence of a fault condition and follows with an emergency shutdown. If VNN, VCCGI is kept OFF by the EXTMODE pin setting or by an I2C command, each Power Good signal is masked to H and will not be a part of the RSMRST_B power good tree.
PCH_PWROK	PMIC POR released (VSYS_V5A > 4.0V) No PMIC Critical Thermal errors VSYS voltage OK (> 5.6V) THERMTRIP_B=H PMIC_EN=H SLP_S4_B=H SLP_S3_B=H VNN Power Good (Masked to H when in S0IX state and until the first PCH_PWROK is asserted) V1P8A Power Good V1P2A Power Good VCCRAM Power Good (Masked to H when in S0IX state) VCCGI Power Good (Masked to H when in S0IX state or OFF) VDDQ Power Good	RSMRST_B will immediately assert at the loss of any of the qualifying signals, or at the occurrence of a fault condition and follows with an emergency shutdown. If VNN, VCCGI is kept OFF by the EXTMODE pin setting or by an I2C command, each Power Good signal is masked to H and will not be a part of the PCH_PWROK power good tree. In S0IX state, VNN, VCCRAM and VCCGI is being sequentially turned OFF and the Power Good masks will be removed from the PCH_PWROK power good tree.

Table 5-10 Power Good Summary when V1P2A is supplied from VDDQ 1.2V at V1P2A merged mode

Power Good	PMIC Qualifying Signals (Logical AND)	Notes
RSMRST_B	PMIC POR released (VSYS_V5A > 4.0V) No PMIC Critical Thermal errors VSYS voltage OK (> 5.6V) THERMTRIP_B=H (Masked to H during the first cold boot until RSMRST_B becomes H) PMIC_EN=H VNN Power Good (Masked to H when OFF and until the first PCH_PWROK is asserted) V1P8A Power Good VCCRAM Power Good (Masked to H when OFF) VCCGI Power Good (Masked to H when OFF) VDDQ Power Good	PCH_PWROK will immediately de-assert at the loss of any of the qualifying signals, or at the occurrence of a fault condition and follows with an emergency shutdown. If VNN, VCCGI is kept OFF by the EXTMODE pin setting or by an I2C command, each Power Good signal is masked to H and will not be a part of the RSMRST_B power good tree.
PCH_PWROK	PMIC POR released (VSYS_V5A > 4.0V) No PMIC Critical Thermal errors VSYS voltage OK (> 5.6V) THERMTRIP_B=H PMIC_EN=H SLP_S4_B=H SLP_S3_B=H VNN Power Good (Masked to H when in S0IX state and until the first PCH_PWROK is asserted) V1P8A Power Good VCCRAM Power Good (Masked to H when in S0IX state) VCCGI Power Good (Masked to H when in S0IX state or OFF) VDDQ Power Good	RSMRST_B will immediately assert at the loss of any of the qualifying signals, or at the occurrence of a fault condition and follows with an emergency shutdown. If VNN, VCCGI is kept OFF by the EXTMODE pin setting or by an I2C command, each Power Good signal is masked to H and will not be a part of the PCH_PWROK power good tree. In S0IX state, VNN, VCCRAM and VCCGI is being sequentially turned OFF and the Power Good masks will be removed from the PCH_PWROK power good tree.

5-5 G3 to S5/S4 & S5/S4 to S0 Power Sequence (DDR_SEL2,1,0=”000”,”010”,”011”)

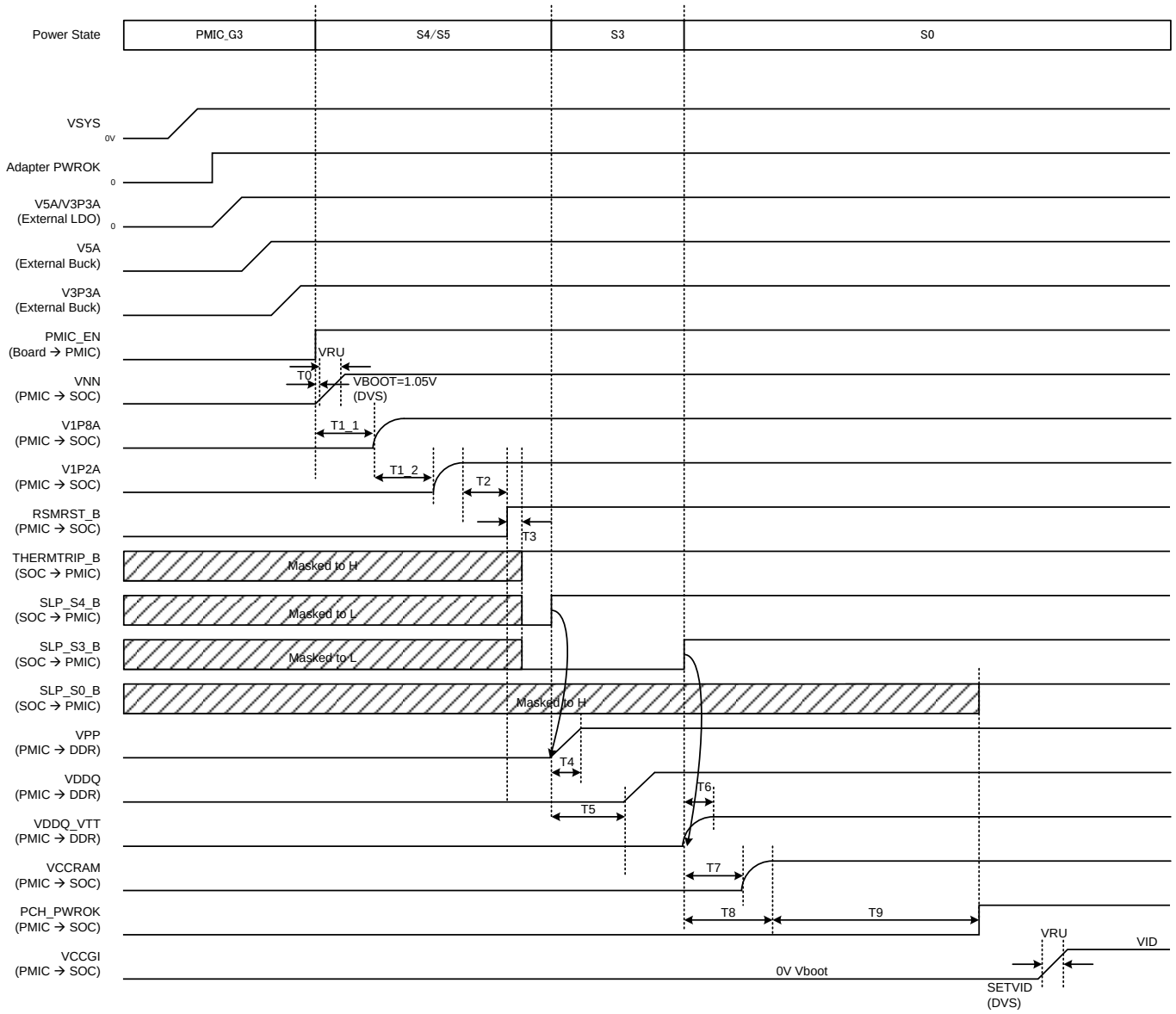


Figure 5-2 G3 to S5/S4 & S5/S4 to S0 Power Sequence

Table 5-11 G3 to S5/S4 & S5/S4 to S0 Power Sequence Timing Specification

Parameter	Description	Min	Typ	Max	Unit
T0	PMIC_EN assert to VNN turn on (20%) delay	-	70	100	µs
T1_1	PMIC_EN assert to V1P8A turn on (10%) delay	0.9	1	1.1	ms
T1_2	V1P8A turn on(10%) to V1P2A turn on (10%) delay	0.9	1	1.1	ms
T2	V1P2A valid (90%) to RSMRST_B de-assert	13.5	15	16.5	ms
T3	RSMRST_B de-assert to SLP_S3_B, SLP_S4_B, THERMTRIP_B valid	0	-	-	µs
T4	SLP_S4_B de-assert to LDO_VPP valid (90%) delay	0	-	2	ms
T5	SLP_S4_B de-assert to VDDQ turn on (10%) delay	2.7	3	3.3	ms
T6	SLP_S3_B de-assert to VDDQ_VTT valid (90%) delay (When VDDQ is already valid)	-	-	100	µs

Parameter	Description	Min	Typ	Max	Unit
T7	SLP_S3_B de-assert to VCCRAM turn on (10%) delay	3.1	3.5	3.9	ms
T8	SLP_S3_B de-assert to VCCRAM valid (90%) delay	-	-	5	ms
T9	VCCRAM valid (90%) to PCH_PWROK assert	TYP x 90%	PWROK DELAY	TYP x 110%	ms
VRU *1	VR ramp up rate for VNN, VCCGI	2.5	3.125	3.75	mV/µs

Note 1: Refer VNN and VCCGI Electrical Characteristics Table 3-2, Table 3-4 for details.

5-6 G3 to S5/S4 & S5/S4 to S0 Power Sequence (DDR_SEL2,1,0=”100”, ”111” : V1P2A supply from VDDQ 1.2V)

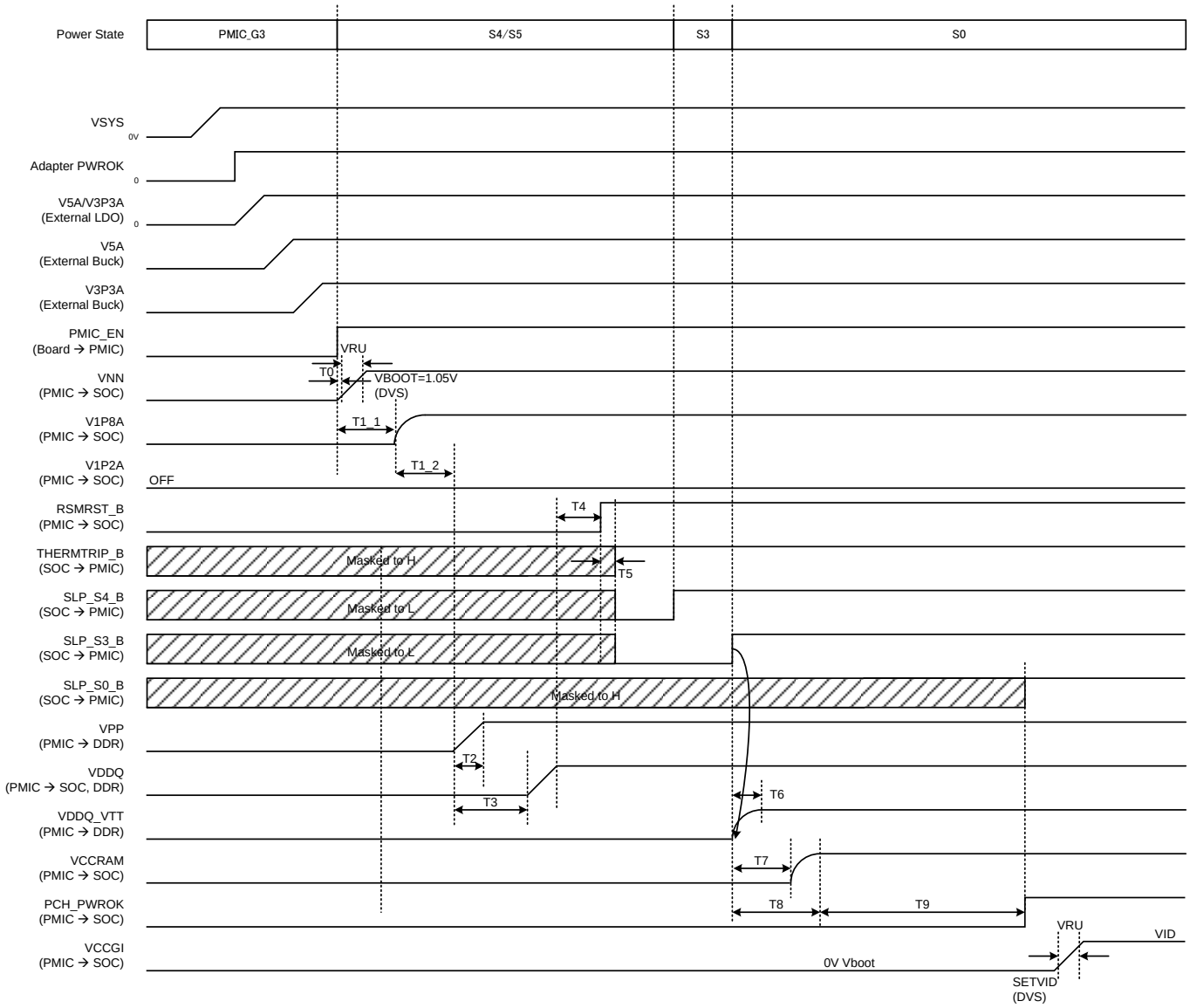


Figure 5-3 G3 to S5/S4 & S5/S4 to S0 Power Sequence (V1P2A supply from VDDQ 1.2V)

Table 5-12 G3 to S5/S4 & S5/S4 to S0 Power Sequence Timing Specification

Parameter	Description	Min	Typ	Max	Unit
T0	PMIC_EN assert to VNN turn on (20%) delay	-	70	100	µs
T1_1	PMIC_EN assert to V1P8A turn on (10%) delay	0.9	1	1.1	ms
T1_2	V1P8A turn on(10%) to VPP turn on (10%) delay	0.9	1	1.1	ms
T2	VPP turn on(10%) to VPP valid (90%) delay	0	-	2	ms
T3	VPP turn on(10%) to VDDQ turn on (10%) delay	2.7	3	3.3	ms
T4	VDDQ valid (90%) to RSMRST_B de-assert	13.5	15	16.5	ms
T5	RSMRST_B de-assert to SLP_S3_B, SLP_S4_B, THERMTRIP_B valid	0	-	-	µs
T6	SLP_S3_B de-assert to VDDQ_VTT valid (90%) delay (When VDDQ is already valid)	-	-	100	µs

Parameter	Description	Min	Typ	Max	Unit
T7	SLP_S3_B de-assert to VCCRAM turn on (10%) delay	3.1	3.5	3.9	ms
T8	SLP_S3_B de-assert to VCCRAM valid (90%) delay	-	-	5	ms
T9	VCCRAM valid (90%) to PCH_PWROK assert	TYP x 90%	PWROK DELAY	TYP x 110%	ms
VRU *1	VR ramp up rate for VNN, VCCGI	2.5	3.125	3.75	mV/µs

Note 1: Refer VNN and VCCGI Electrical Characteristics Table 3-2, Table 3-4 for details.

5-7 S0IX Entry and Exit Power Sequence (VNN and VCCGI SetVID to 0V before entering S0IX)

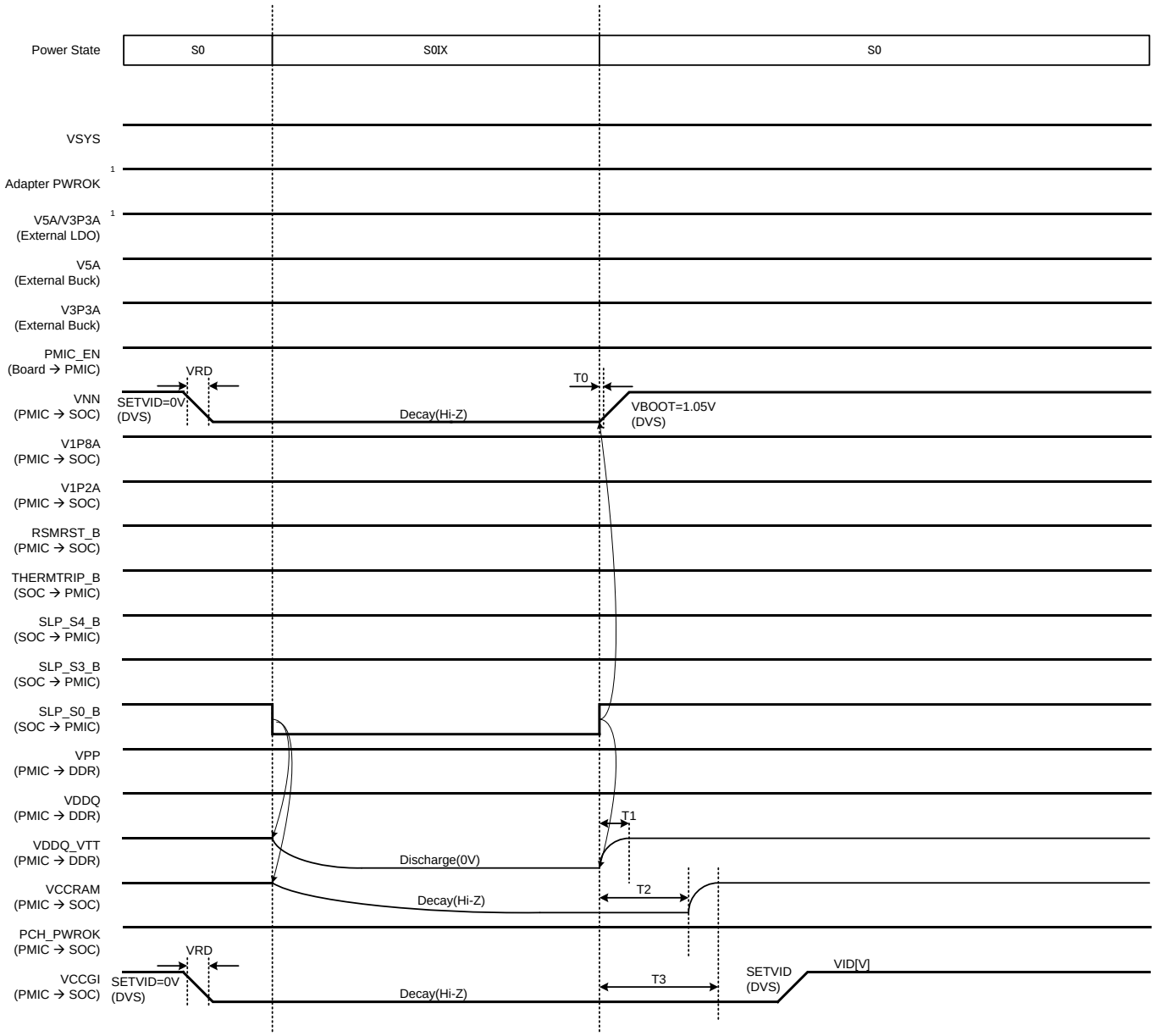


Figure 5-4 S0IX Entry and Exit Power Sequence (VNN and VCCGI SetVID to 0V before entering S0IX)

Table 5-13 S0IX Entry and Exit Power Sequence Timing Specification

Parameter	Description	Min	Typ	Max	Unit
T0	SLP_S0_B de-assert to VNN turn on (20%) delay	-	70	100	µs
T1	SLP_S0_B de-assert to VDDQ_VTT valid (90%) delay	-	-	100	µs
T2	SLP_S0_B de-assert to VCCRAM turn on (10%) delay	3.1	3.5	3.9	ms
T3	SLP_S0_B de-assert to VCCRAM valid (90%) delay	-	-	5	ms
VRD *1	VR ramp down rate for VNN, VCCGI	2.5	3.125	3.75	mV/µs

Note 1: Refer VNN and VCCGI Electrical Characteristics Table 3-2, Table 3-4 for details.

5-8 S0IX Entry and Exit Power Sequence

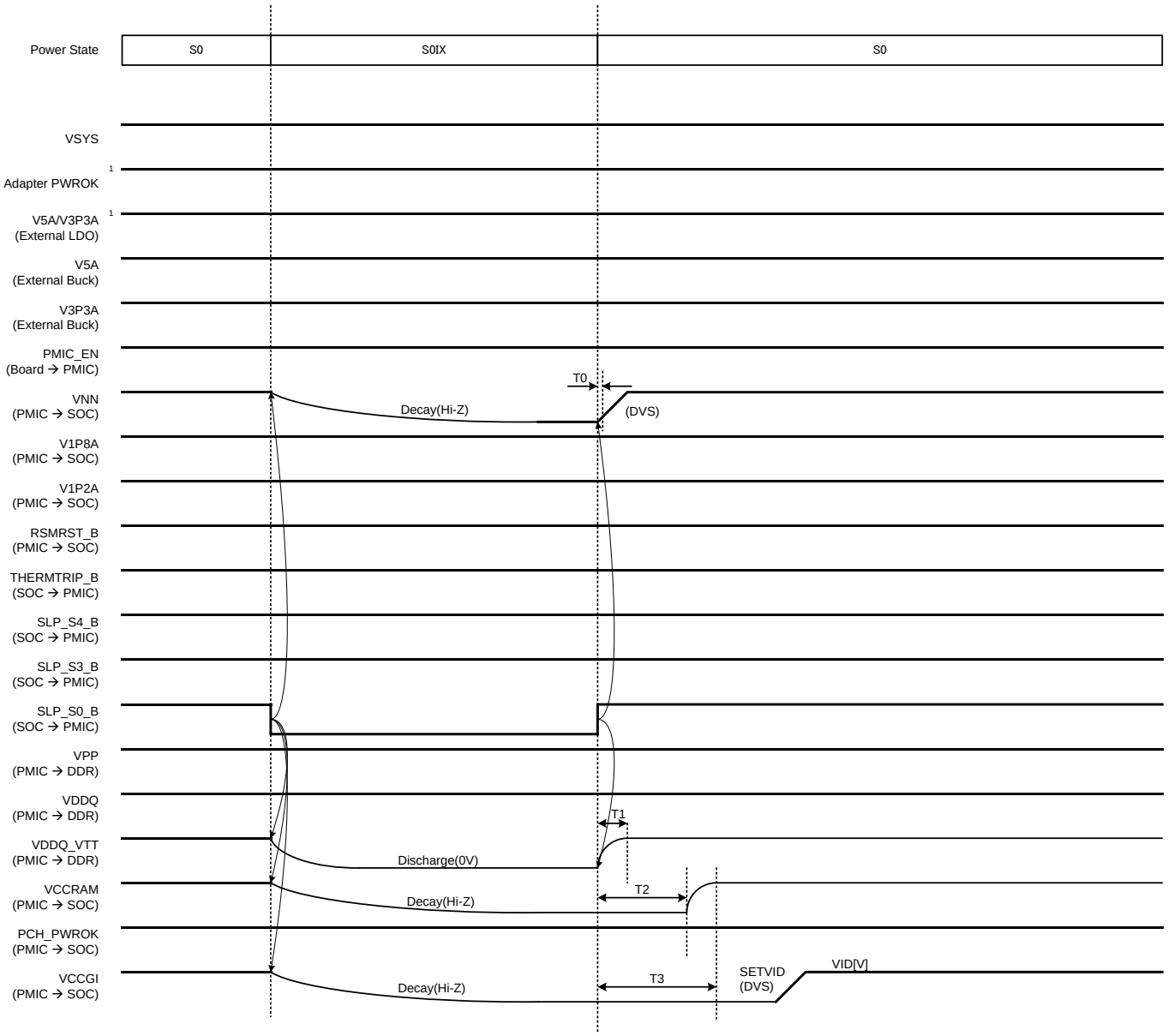


Figure 5-5 S0IX Entry and Exit Power Sequence

Table 5-14 S0IX Entry and Exit Power Sequence Timing Specification

Parameter	Description	Min	Typ	Max	Unit
T0	SLP_S0_B de-assert to VNN turn on (20%) delay	-	70	100	µs
T1	SLP_S0_B de-assert to VDDQ_VTT valid (90%) delay	-	-	100	µs
T2	SLP_S0_B de-assert to VCCRAM turn on (10%) delay	3.1	3.5	3.9	ms
T3	SLP_S0_B de-assert to VCCRAM valid (90%) delay	2.8	-	5	ms

5-9 S3 Entry and Exit Power Sequence

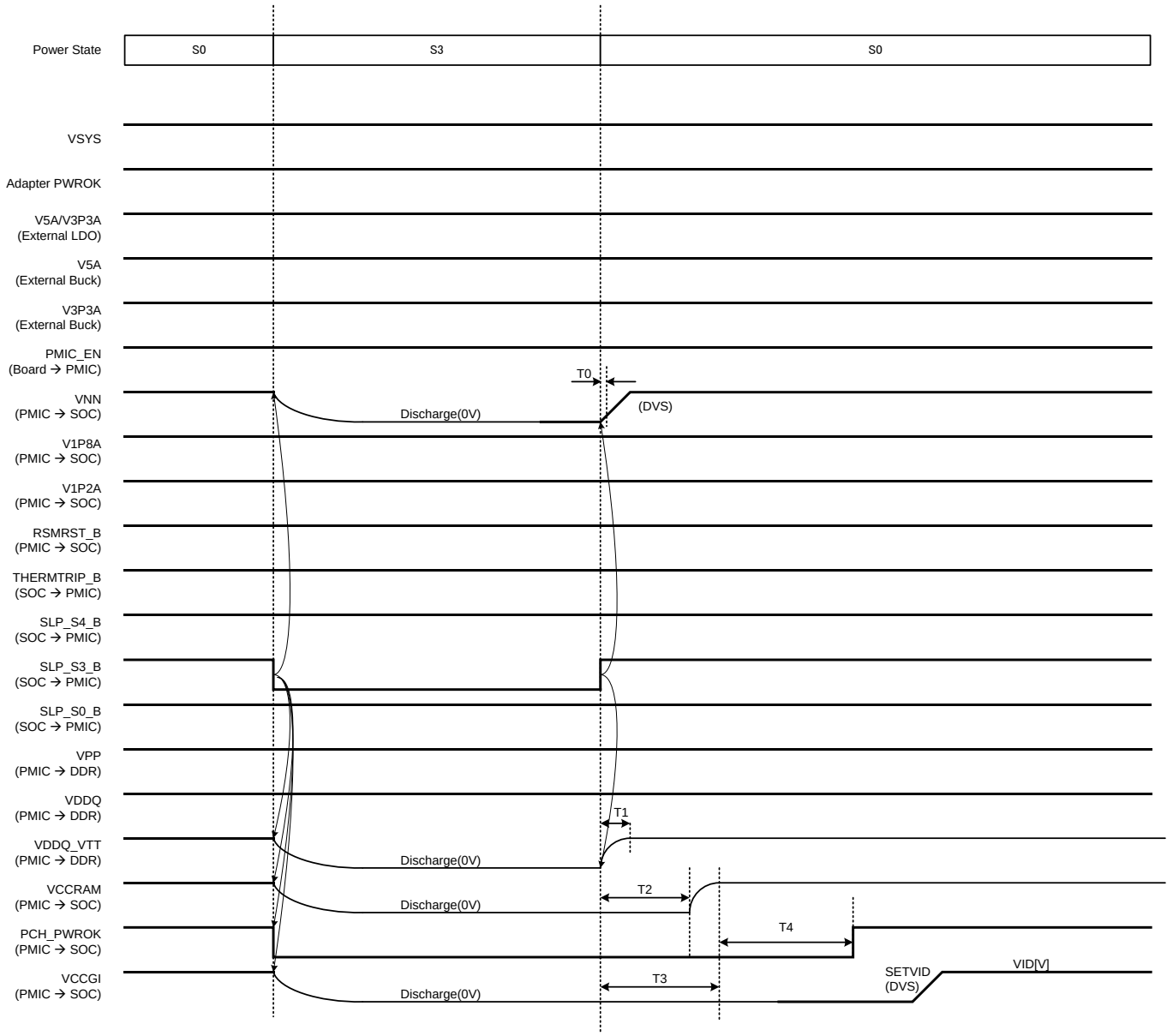


Figure 5-6 S3 Entry and Exit Power Sequence

Table 5-15 S3 Entry and Exit Power Sequence Timing Specification

Parameter	Description	Min	Typ	Max	Unit
T0	SLP_S3_B de-assert to VNN turn on (20%) delay	-	70	100	µs
T1	SLP_S3_B de-assert to VDDQ_VTT valid (90%) delay	-	-	100	µs
T2	SLP_S3_B de-assert to VCCRAM turn on (10%) delay	3.1	3.5	3.9	ms
T3	SLP_S3_B de-assert to VCCRAM valid (90%) delay	-	-	5	ms
T4	VCCRAM valid (90%) to PCH_PWROK assert	Typ x 90%	PWROK DELAY	Typ x 110%	ms

5-10 S4/S5 to S0 Entry and Exit Power Sequence

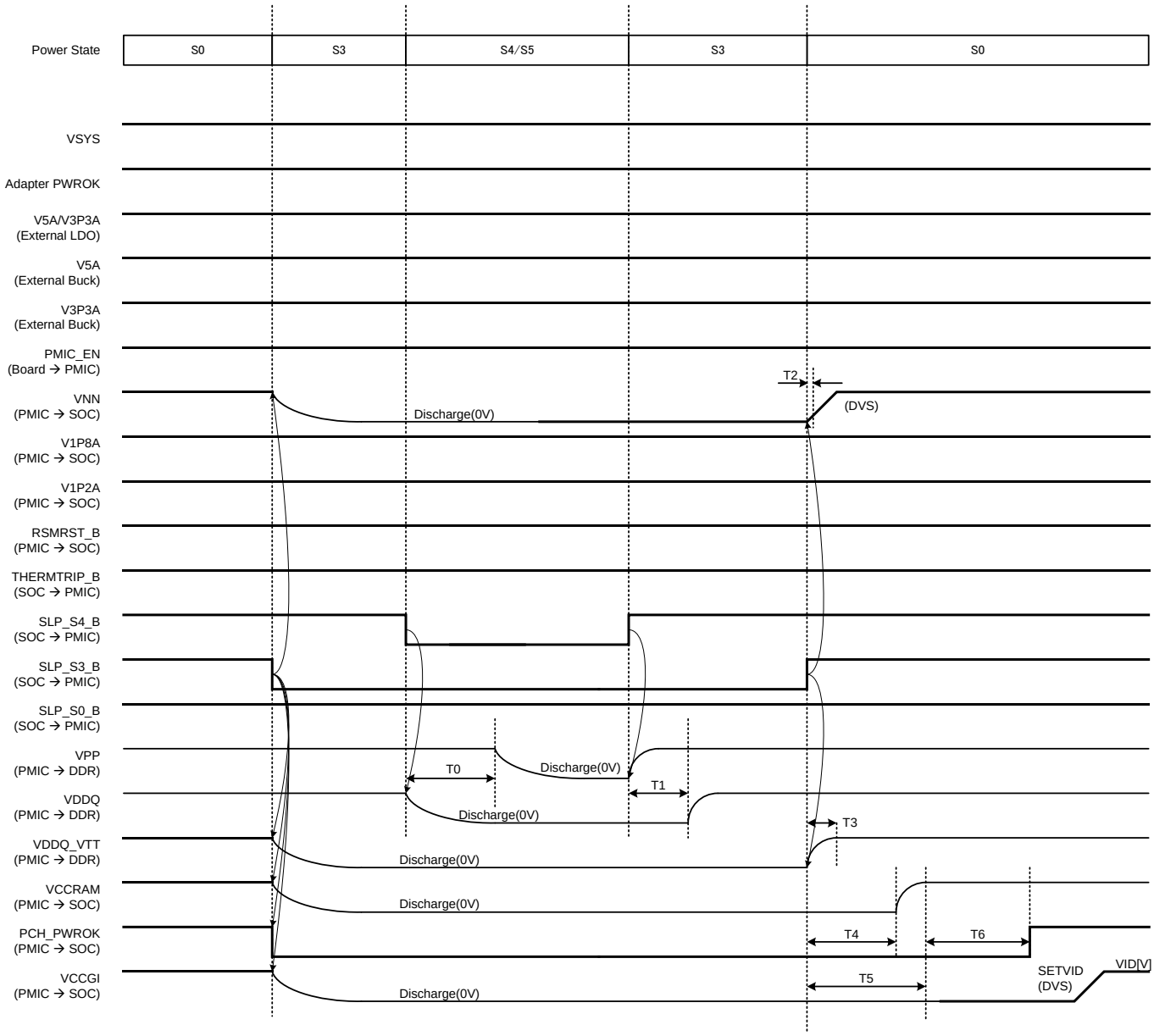


Figure 5-7 S4/S5 to S0 Entry and Exit Power Sequence

Table 5-16 S4/S5 to S0 Entry and Exit Power Sequence Timing Specification

Parameter	Description	Min	Typ	Max	Unit
T0	SLP_S4_B assert to LDO_VPP decay start point delay	40	45	50	ms
T1	SLP_S4_B de-assert to VDDQ turn on (10%) delay	2.7	3	3.3	ms
T2	SLP_S3_B de-assert to VNN turn on (20%) delay	-	70	100	µs
T3	SLP_S3_B de-assert to VDDQ_VTT valid (90%) delay	-	-	100	µs
T4	SLP_S3_B de-assert to VCCRAM turn on (10%) delay	3.1	3.5	3.9	ms
T5	SLP_S3_B de-assert to VCCRAM valid (90%) delay	-	-	5	ms
T6	VCCRAM valid(90%) to PCH_PWROK assert	Typ x 90%	PWROK DELAY	Typ x 110%	ms

5-11 S4/S5 to S0 Entry and Exit Power Sequence (SLP_S3_B=SLP_S4_B)

BD2671MWV is designed to support simultaneous input control of the SLP_S4_B, SLP_S3_B, SLP_S0_B signals. Described in Section “5-2 Power States”, it is capable of jumping directly from S4/S5 state to S0 state or S0 state to S4/S5 state by controlling SLP_S3_B and SLP_S4_B at the same time, or just by SLP_S4_B. Figure 5-8 is a sequence example of SLP_S3_B and SLP_S4_B signals controlled at the same timing, but it follows the same sequence by just controlling SLP_S4_B and keeping SLP_S3_B logic H.
When this sequence is applied, while VDDQ_VTT is normally controlled to turn on at the same time as Exit S3 or Exit S0IX, VDDQ_VTT is controlled to wait for the VDDQ to boot up and become stable. This is to assure that VDDQ_VTT would not violate the system specification.

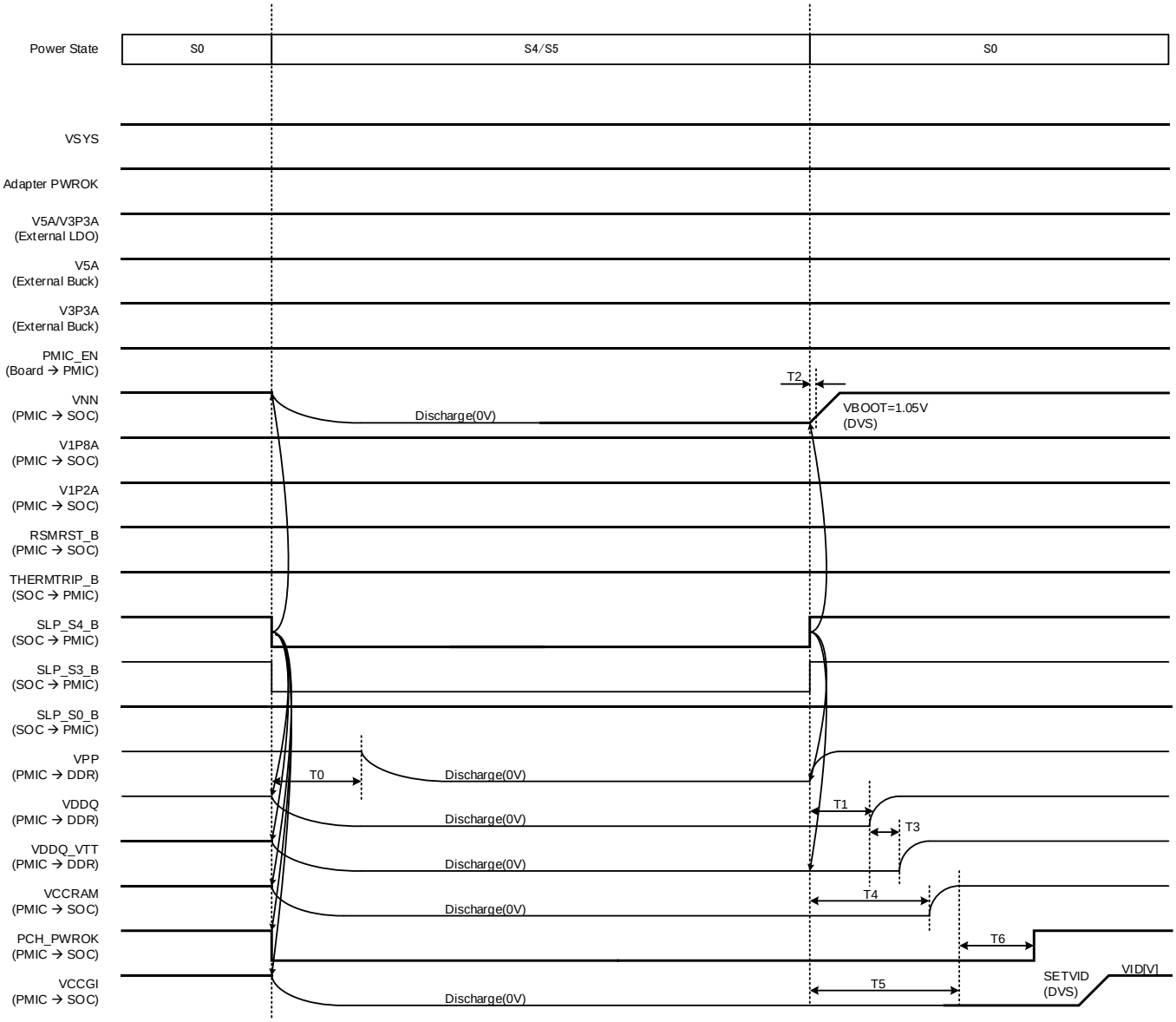


Figure 5-8 S4/S5 to S0 Entry and Exit Power Sequence (SLP_S3_B=SLP_S4_B)

Table 5-17 S4/S5 to S0 Entry and Exit Power Sequence Timing Specification

Parameter	Description	Min	Typ	Max	Unit
T0	SLP_S4_B assert to LDO_VPP decay start point delay	40	45	50	ms
T1	SLP_S4_B de-assert to VDDQ turn on (10%) delay	2.7	3	3.3	ms
T2	SLP_S3_B de-assert to VNN turn on (20%) delay	-	70	100	µs

Parameter	Description	Min	Typ	Max	Unit
T3 *1	VDDQ turn on(10%) to VDDQ_VTT turn on (10%) delay	180	200	-	µs
T4	SLP_S3_B de-assert to VCCRAM turn on (10%) delay	3.1	3.5	3.9	ms
T5	SLP_S3_B de-assert to VCCRAM valid (90%) delay	-	-	5	ms
T6	VCCRAM valid(90%) to PCH_PWROK assert	Typ x 90%	PWROK DELAY	Typ x 110%	ms

Note 1: VDDQ_VTT always boots up after VDDQ is valid.

5-12 S0 to PMIC G3 Power Sequence

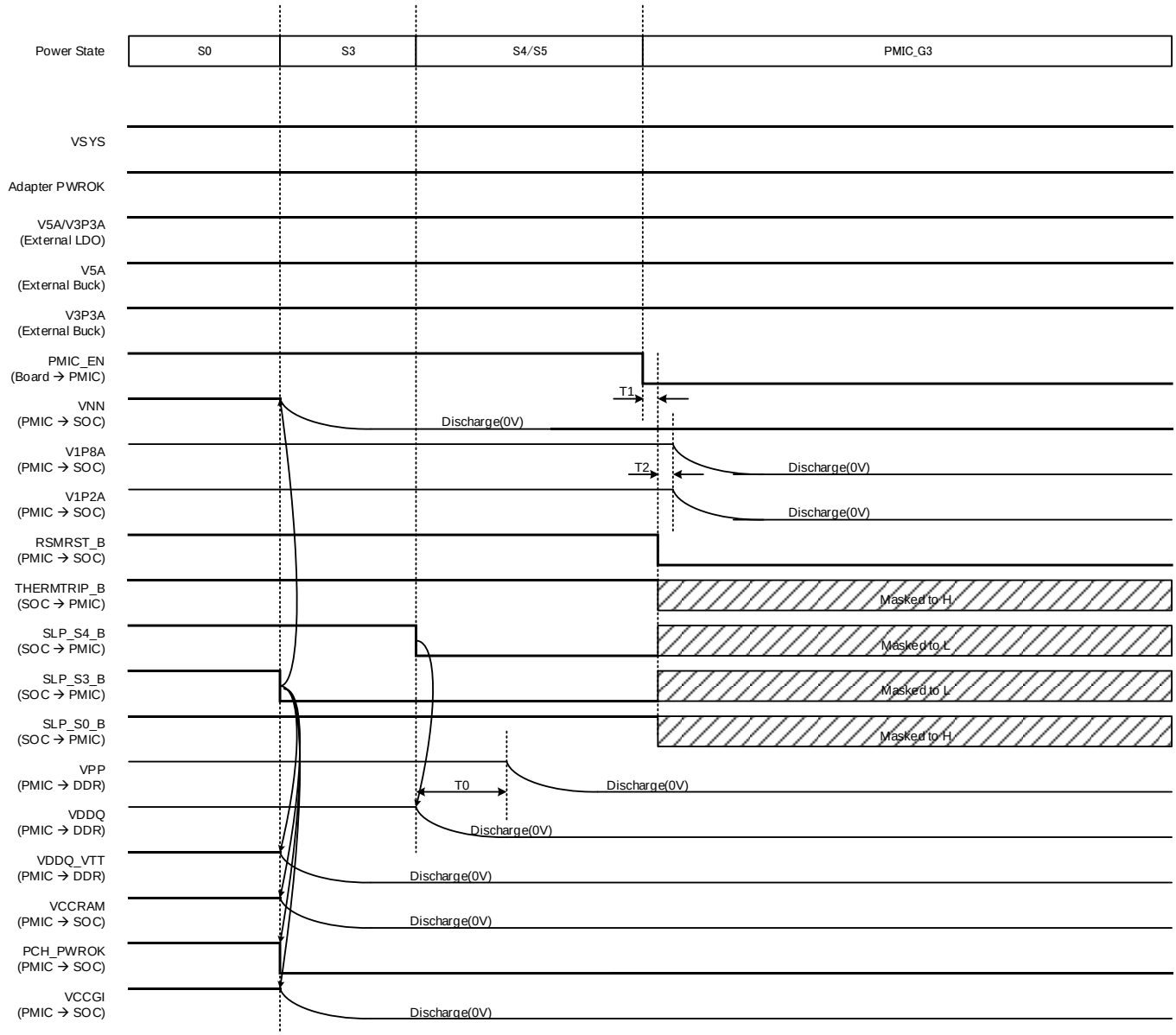


Figure 5-9 S0 to PMIC G3 Power Sequence

Table 5-18 S0 to PMIC G3 Power Sequence Timing Specification

Parameter	Description	Min	Typ	Max	Unit
T0	SLP_S4_B assert to LDO_VPP decay start point delay	40	45	50	ms
T1	PMIC_EN de-assert to RSMRST_B assert delay	-	0.5	1	µs
T2	RSMRST_B assert to VR turn off point	0.5	1	-	µs

5-13 VSYS UVLO Emergency Shutdown Sequence

BD2671MWV supports an emergency shutdown sequence when operating in a system with a 2S or 3S battery configuration, as shown in Figure 5-10. For droop or loss on VSYS, the emergency shutdown trigger threshold is 5.4V. The VSYS droop or loss detection debounce time is 5µs typical. On VSYS ramp up the emergency shutdown release threshold voltage is 5.6V with a debounce time of 100µs typical.
Once the shutdown sequence is initiated, PMIC_EN boot is masked for a time of 100ms typical to prevent a new boot sequence to occur right after the shutdown. This is to assure enough time for all the rails to discharge and reboot as a clean start.
While the PMIC_EN boot is masked, PMIC_EN is always honored and the L to H edge is detectable even during the mask period.
When the PMIC_EN L to H edge is detected during the mask period and if PMIC_EN maintains H at the end of the mask period, the PMIC will reboot right after the mask is disabled.

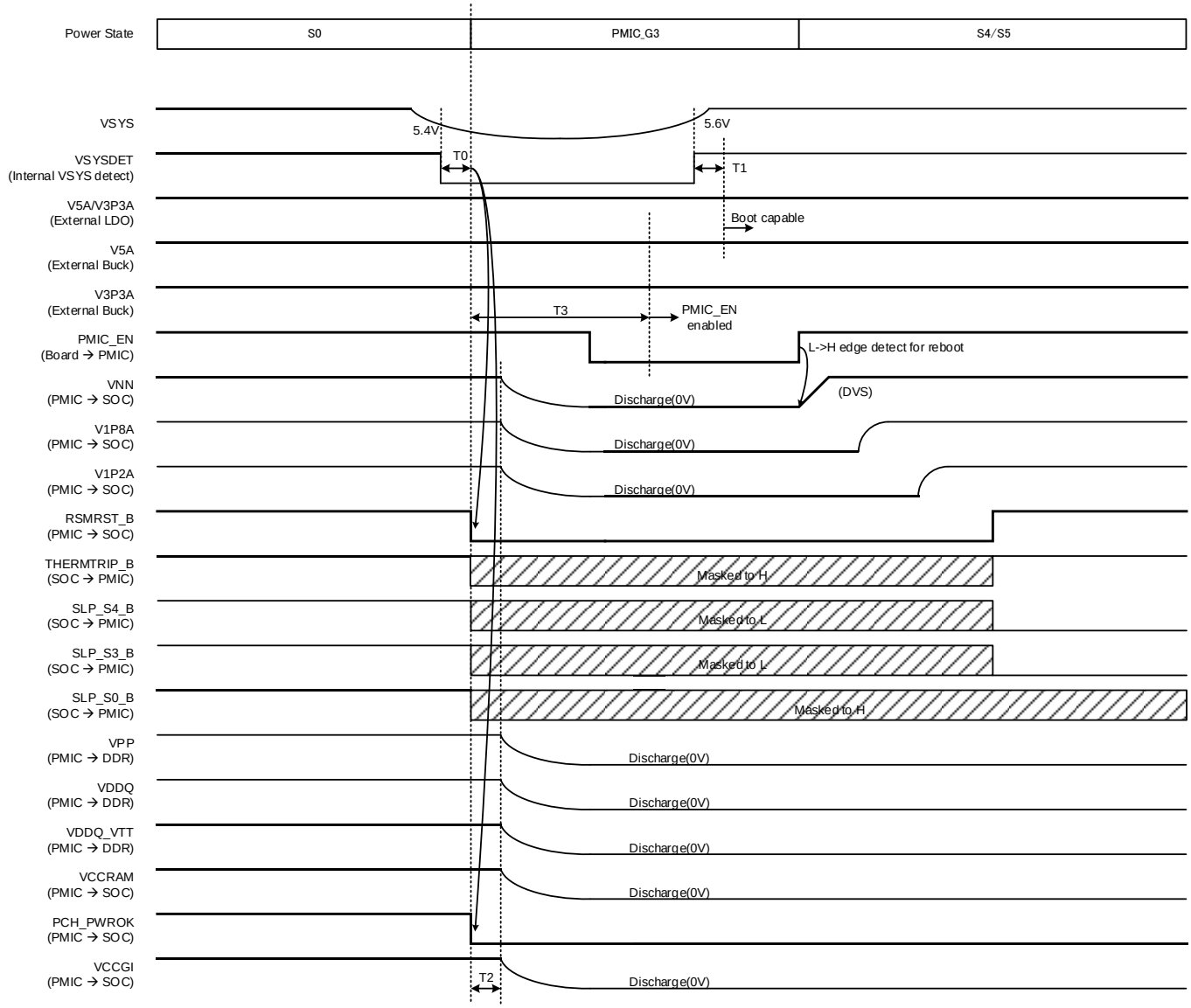


Figure 5-10 VSYS UVLO Emergency Shutdown Sequence

Table 5-19 VSYS UVLO Emergency Shutdown Sequence Timing Specification

Parameter	Description	Min	Typ	Max	Unit
T0	VSYS UVLO Detect debounce time (VSYS ≤ 5.4V)	3	5	7	µs
T1	VSYS UVLO Release debounce time (VSYS > 5.60V)	90	100	110	µs
T2	RSMRST_B assert or PCH_PWROK de-assert to VR turn off point	0.5	1	-	µs
T3	Emergency Shutdown to PMIC_EN reboot mask disabled	90	100	110	ms

The VR enable timing after the reboot is exactly the same as the cold boot sequence described in Section “5-5 G3 to S5/S4 & S5/S4 to S0 Power Sequence”.

5-14 THERMTRIP_B Emergency Shutdown Sequence

BD2671MWV supports an emergency shutdown sequence at the assertion of the THERMTRIP_B (H to L) signal from the SOC.
It follows the same sequence as the other shutdown sequences with the same timing applied.

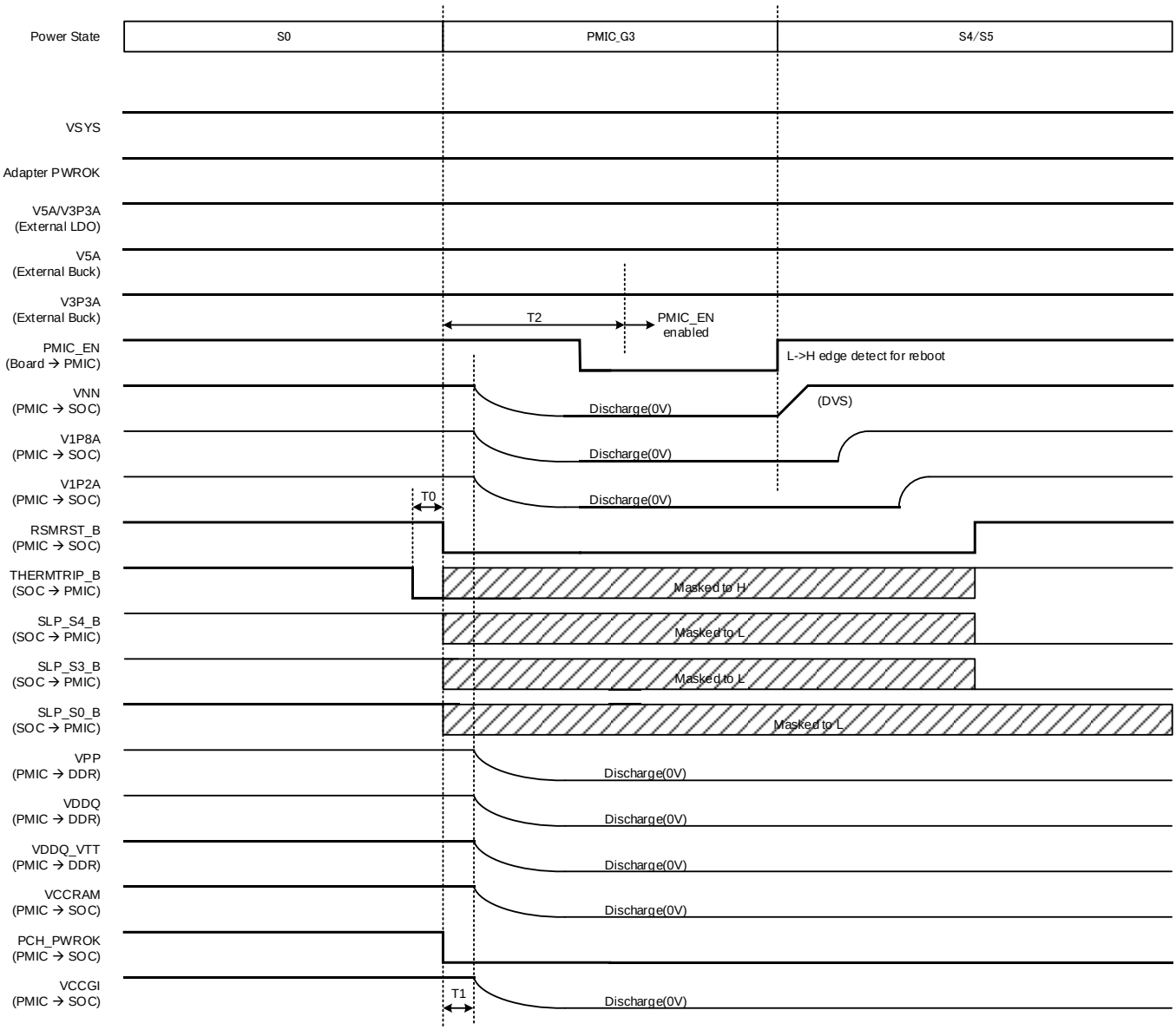


Figure 5-11 THERMTRIP_B Emergency Shutdown Sequence

Table 5-20 THERMTRIP_B Emergency Shutdown Sequence Timing Specification

Parameter	Description	Min	Typ	Max	Unit
T0	THERMTRIP_B assert to RSMRST_B assert and PCH_PWROK de-assert delay	-	0.5	1	µs
T1	RSMRST_B assert or PCH_PWROK de-assert to VR turn off point	0.5	1	-	µs
T2	Emergency Shutdown to PMIC_EN reboot mask disabled	90	100	110	ms

The VR enable timing after the reboot is exactly the same as the cold boot sequence described in Section “5-5 G3 to S5/S4 & S5/S4 to S0 Power Sequence”.

5-15 PMIC_EN Emergency Shutdown Sequence and quick reboot by PMIC_EN

BD2671MWV supports an emergency shutdown sequence by the de-assertion of the PMIC_EN signal from the SOC.
It follows the same sequence as the other shutdown sequences with the same timing applied.

The Figure 5-12 is the PMIC_EN emergency shutdown behavior. In this case, the PMIC_EN L to H reboot edge is inputted during the PMIC reboot mask period.
The sequence shows that PMIC_EN is honored at all times and it reboots as soon as the reboot mask is disabled.

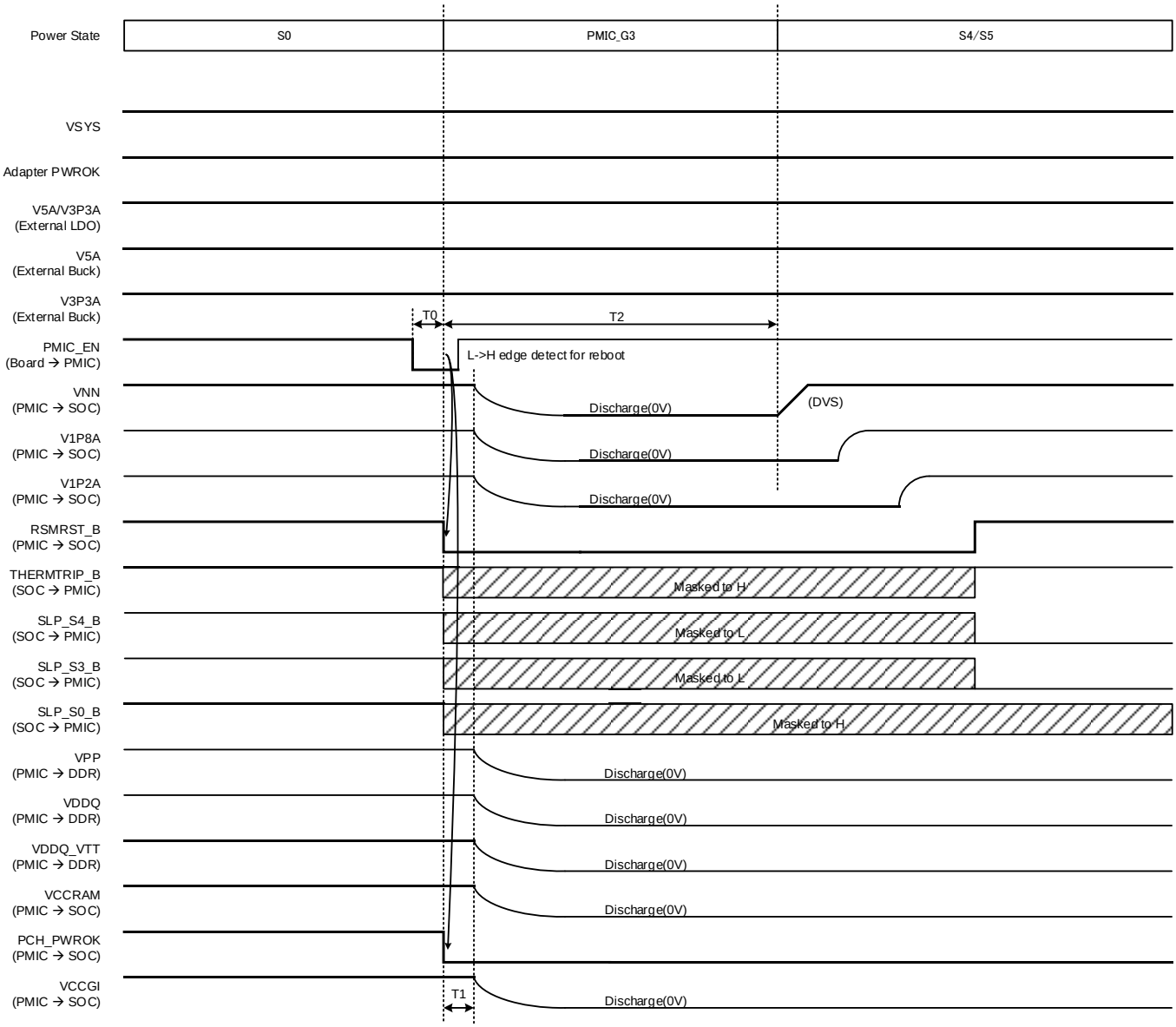


Figure 5-12 PMIC_EN Emergency Shutdown Sequence

Table 5-21 PMIC_EN Emergency Shutdown Sequence Timing Specification

Parameter	Description	Min	Typ	Max	Unit
T0	PMIC_EN de-assert to RSMRST_B assert and PCH_PWROK de-assert delay	-	0.5	1	µs
T1	RSMRST_B assert or PCH_PWROK de-assert to VR turn off point	0.5	1	-	µs
T2	Emergency Shutdown to PMIC_EN reboot mask disabled	90	100	110	ms

The VR enable timing after the reboot is exactly the same as the cold boot sequence described in Section “5-5 G3 to S5/S4 & S5/S4 to S0 Power Sequence”.

5-16 Emergency Shutdown Events

When BD2671MWV detects any kind of fault which is listed below in Table 5-22, it will all lead to an Emergency Shutdown. This sequence will be applied to any Power State (S4/S5, S3, S0IX, and S0). The Sequence timing is common among all the shutdown events.

Table 5-22 Emergency Shutdown Factors

Event	Condition	Note
Die Temp	BD2671MWV detects a PMIC Die critical temperature condition (T>150ºC) on its internal die sensor.	BD2671MWV asserts RSMRST_B and de-asserts PCH_PWROK immediately. After 1µs, all VR's will shut down. It will assert DIETEMP 1st level interrupt register to 1.
VSYS UVLO	BD2671MWV detects VSYS under voltage (VSYS < 5.4V) by VSYS under voltage comparator.	BD2671MWV asserts RSMRST_B and de-asserts PCH_PWROK immediately. After 1µs, all VR's will shut down. It will assert ONOFFSRC 1st level interrupt register and UVLO 2nd level interrupt register to 1.
PMIC_EN	BD2671MWV detects a PMIC_EN de-assertion by the SOC.	BD2671MWV asserts RSMRST_B and de-asserts PCH_PWROK immediately. After 1µs, all VR's will shut down. It will assert ONOFFSRC 1st level interrupt register and COLDOFF 2nd level interrupt register to 1.
VR OCP	BD2671MWV detects an OCP failure in any of the rails. (VNN, VCCGI, VCCRAM, V1P8A, V1P2A, VDDQ)	BD2671MWV asserts RSMRST_B and de-asserts PCH_PWROK immediately. After 1µs, all VR's will shut down. It will assert ONOFFSRC 1st level interrupt register and OCP 2nd level interrupt register to 1.
VR Voltage	BD2671MWV detects a Voltage failure in any of the rails. (VNN, VCCGI, VCCRAM, V1P8A, V1P2A, VDDQ)	BD2671MWV asserts RSMRST_B and de-asserts PCH_PWROK immediately. After 1µs, all VR's will shut down. It will assert VR_FAULT 1st level register and **_FAULT 2nd level interrupt register to 1.

Note: **_FAULT: Any bit of the 2nd level interrupt register VRFAULT_INT.

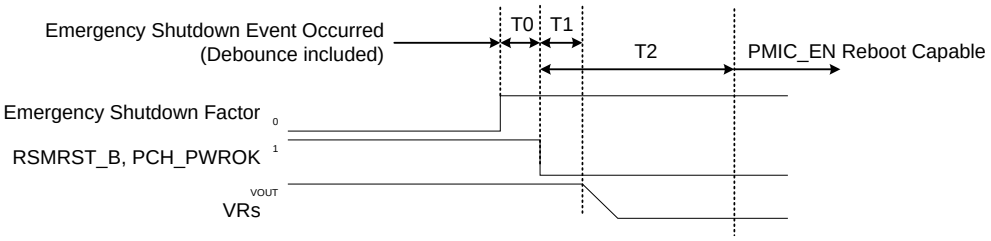


Figure 5-13 Emergency Shutdown Sequence

Table 5-23 Emergency Shutdown Sequence Timing Specification

Parameter	Description	Min	Typ	Max	Unit
T0	Emergency Shutdown Factor to RSMRST_B assert and PCH_PWROK de-assert delay	-	0.5	1	µs
T1	RSMRST_B assert or PCH_PWROK de-assert to VR turn off point	0.5	1	-	µs
T2	Emergency Shutdown to PMIC_EN reboot mask disabled	90	100	110	ms

6 Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition. However, pins that drive inductive loads (e.g. motor driver outputs, DC-DC converter outputs) may inevitably go below ground due to back EMF or electromotive force. In such cases, the user should make sure that such voltages going below ground will not cause the IC and the system to malfunction by examining carefully all relevant factors and conditions such as motor characteristics, supply voltage, operating frequency and PCB wiring to name a few.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

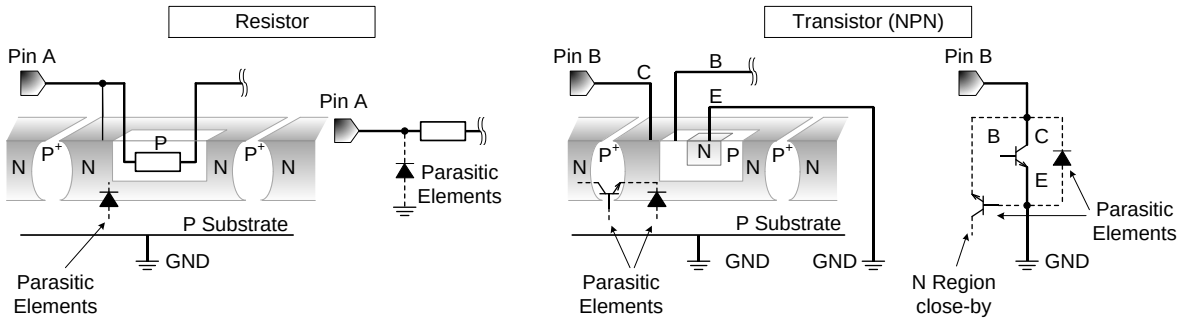
Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



12. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Thermal Consideration

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. The IC should be powered down and turned ON again to resume normal operation because the TSD circuit keeps the outputs at the OFF state even if the Tj falls below the TSD threshold.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

14. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Notice

Precaution on using ROHM Products

1. Our Products are designed and manufactured for application in ordinary electronic equipment (such as AV equipment, OA equipment, telecommunication equipment, home electronic appliances, amusement equipment, etc.). If you intend to use our Products in devices requiring extremely high reliability (such as medical equipment (Note 1), transport equipment, traffic equipment, aircraft/spacecraft, nuclear power controllers, fuel controllers, car equipment including car accessories, safety devices, etc.) and whose malfunction or failure may cause loss of human life, bodily injury or serious damage to property ("Specific Applications"), please consult with the ROHM sales representative in advance. Unless otherwise agreed in writing by ROHM in advance, ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of any ROHM's Products for Specific Applications.

(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
   [a] Installation of protection circuits or other protective devices to improve system safety
   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are designed and manufactured for use under standard conditions and not under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

Precaution for Product Label

A two-dimensional barcode printed on ROHM Products label is for ROHM's internal use only.

Precaution for Disposition

When disposing Products please dispose them properly using an authorized industry waste company.

Precaution for Foreign Exchange and Foreign Trade act

Since concerned goods might be fallen under listed items of export control prescribed by Foreign exchange and Foreign trade act, please consult with ROHM in case of export.

Precaution Regarding Intellectual Property Rights

1. All information and data including but not limited to application example contained in this document is for reference only. ROHM does not warrant that foregoing information or data will not infringe any intellectual property rights or any other rights of any third party regarding such information or data.

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