Multiple Input Switch Monitor LSI for Automotive

BD3381EKV-C

General Description

BD3381EKV-C is a 33-channel Multiple Input Switch Monitor IC that detects the opening and closing of mechanical switches. Once it senses a change in the status of a switch, it sends an interrupt signal to the MCU via a serial peripheral interface (SPI).

The 33 switch inputs have two types of power supply, VPUB and VPUA. The VPUB and the VPUA power supplies can either be from a battery or from another power supply system. VPUB is the supply for the INB inputs while VPUA is for the INZ and INA inputs.

BD3381EKV-C has two modes of operation, Normal and Sleep. In both modes, the internal registers can be set to make the device perform either intermittent or continuous monitoring of the switches.

In intermittent monitoring, the switch status is monitored at regular time intervals, allowing the IC to operate with low power consumption. Also, operation with reduced noise can be achieved by enabling uniform sequential monitoring of all switches or sequential monitoring by power supply system.

Features

- AEC-Q100 Qualified *(Note 1)*
- Uses 3.3 V/5.0 V SPI Protocol in Communicating with the MCU
- Serial Communication Error Checking through 8-bit CRC
- Thermal Shutdown Protection (TSD)
- Power on Reset (POR)
- Selectable Source/Sink Current Levels through Register Settings
- Wetting Current Timer Capability
- 12 Source or Sink Input Pins (VPUA)
- 21 Source Input Pins
- Separable Power Supply
  VPUA: 22-channel (INA&INZ), VPUB: 11-channel (INB)
- Interrupt Notification upon Switch Status Change
- 1 Time to 10 Times Matched LPF that Eliminates Input Pin Noise
- Low Current Consumption (Intermittent Monitoring)
- Status Display of Selected Pin at DOUT Pin

(Note 1) Grade 1

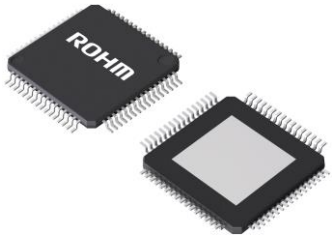
Application

- Engine Control Module

Package

HTQFP64BV
(64 pin QFP)

W(Typ) x D(Typ) x H(Max)
12.00 mm x 12.00 mm x 1.00 mm



Key Specifications

- Low-voltage Operating Range: 3.9 V to 6.0 V
- Fully Operational Voltage Range: 6 V to 28 V
- Input Voltage on Switch Pin: -14 V to +40 V
- Selectable Wetting Current (Min):
  1 mA, 3 mA, 5 mA, 10 mA, 15 mA

Typical Application Circuit

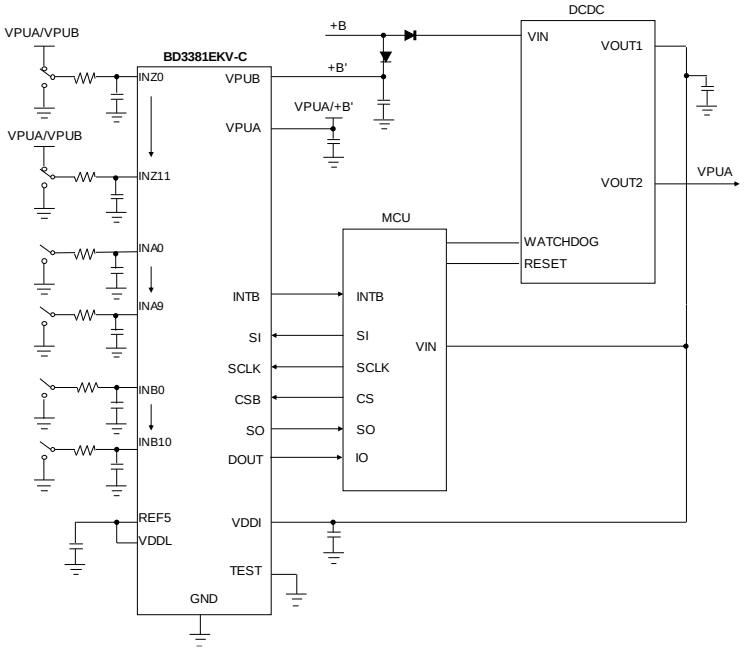


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration

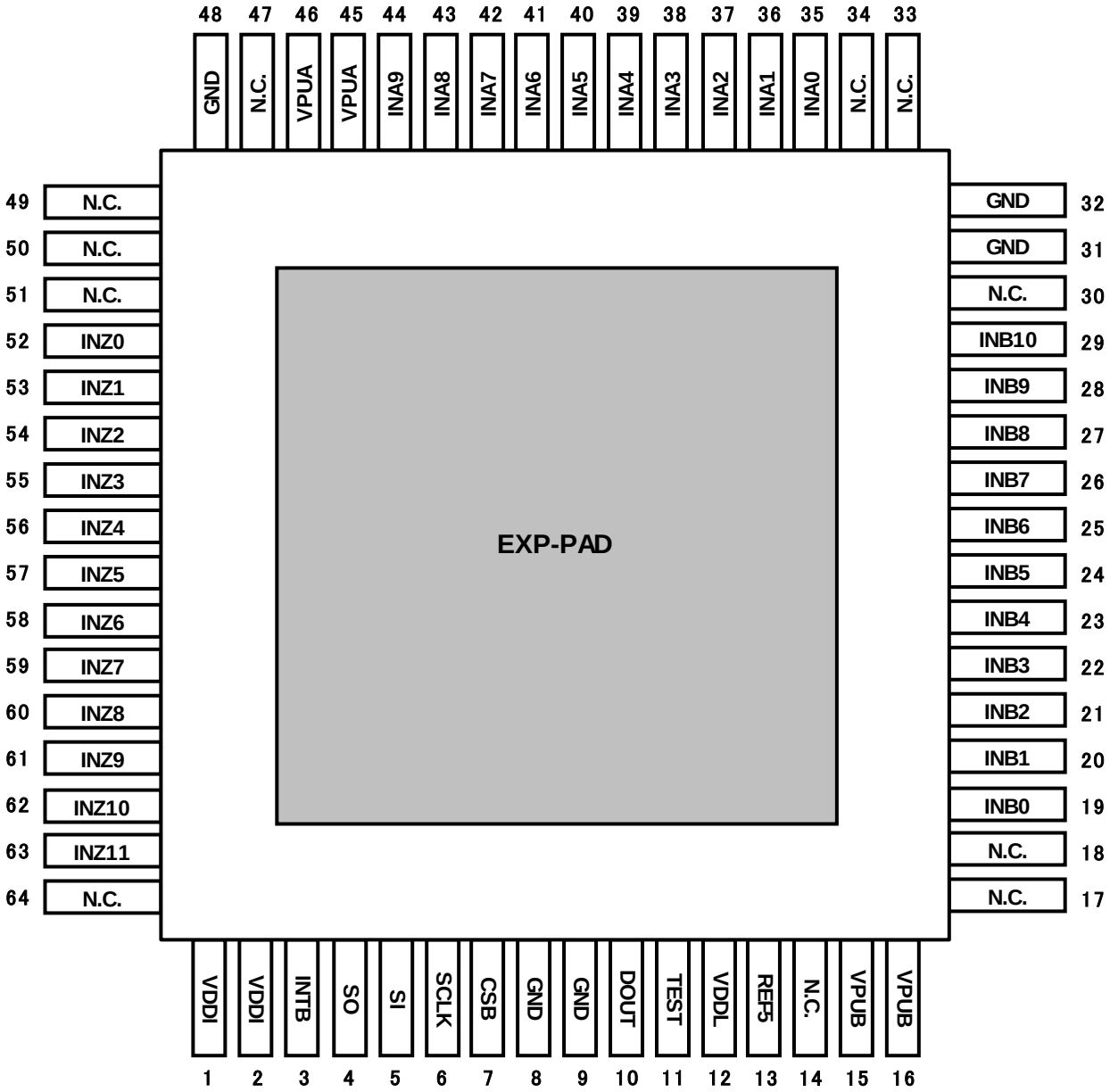


Figure 2. Pin Configuration (Top View)

Pin Description

Table 1. Pin Description (1/2)

Pin No.	Pin Name	Function	Description	I/O Equivalence Circuit Diagram *(Note 2)*
1	VDDI	Input	Power supply pin for CSB, SI, SCLK, SO, INTB and DOUT	--
2	VDDI	Input	Power supply pin for CSB, SI, SCLK, SO, INTB and DOUT	--
3	INTB	Output	Open-drain interrupt output pin to the MCU (with an internal pull-down resistor)	C
4	SO	Output	SPI data output pin to the MCU	G
5	SI	Input	SPI control data input pin from the MCU (with an internal pull-down resistor)	A
6	SCLK	Input	SPI control clock input pin from the MCU (with an internal pull-down resistor)	A
7	CSB	Input	SPI control chip select input pin from the MCU (with internal pull-up current source)	B
8	GND	Ground	Ground pin	--
9	GND	Ground	Ground pin	--
10	DOUT	Output	General purpose output for digital functions	F
11	TEST	Input	Test mode control pin*(Note 3)* (with an internal pull-down resistor)	I
12	VDDL	Input	Power supply input pin for the analog and logic block*(Note 4)*	--
13	REF5	Output	5 V power supply output pin for internal use*(Note 4)*	H
14	N.C.	-	No Connection*(Note 5)*	--
15	VPUB	Input	Power supply input pin for the main system and INB switches	--
16	VPUB	Input	Power supply input pin for the main system and INB switches	--
17	N.C.	-	No Connection*(Note 5)*	--
18	N.C.	-	No Connection*(Note 5)*	--
19	INB0	Input	Switch input pin 0 under VPUB power supply system (with an internal pull-up current source)	E
20	INB1	Input	Switch input pin 1 under VPUB power supply system (with an internal pull-up current source)	E
21	INB2	Input	Switch input pin 2 under VPUB power supply system (with an internal pull-up current source)	E
22	INB3	Input	Switch input pin 3 under VPUB power supply system (with an internal pull-up current source)	E
23	INB4	Input	Switch input pin 4 under VPUB power supply system (with an internal pull-up current source)	E
24	INB5	Input	Switch input pin 5 under VPUB power supply system (with an internal pull-up current source)	E
25	INB6	Input	Switch input pin 6 under VPUB power supply system (with an internal pull-up current source)	E
26	INB7	Input	Switch input pin 7 under VPUB power supply system (with an internal pull-up current source)	E
27	INB8	Input	Switch input pin 8 under VPUB power supply system (with an internal pull-up current source)	E
28	INB9	Input	Switch input pin 9 under VPUB power supply system (with an internal pull-up current source)	E
29	INB10	Input	Switch input pin 10 under VPUB power supply system (with an internal pull-up current source)	E
30	N.C.	-	No Connection*(Note 5)*	--
31	GND	Ground	Ground pin	--
32	GND	Ground	Ground pin	--

(Note 2) Ref. Page 72 and Page 73 I/O Equivalence Circuit.
(Note 3) Short TEST pin to ground when mounted.
(Note 4) Short REF5 pin to VDDL pin, and connect a 4.7 µF (Min) capacitor between it and ground. Do not use it as voltage source to another IC.
(Note 5) Keep N.C. pins electrically opened.

Pin Description - continued

Table 2. Pin Description (2/2)

Pin No.	Pin Name	Function	Description	I/O Equivalence Circuit Diagram *(Note 2)*
33	N.C.	-	No Connection*(Note 5)*	--
34	N.C.	-	No Connection*(Note 5)*	--
35	INA0	Input	Switch input pin 0 under VPUA power supply system (with an internal pull-up current source)	E
36	INA1	Input	Switch input pin 1 under VPUA power supply system (with an internal pull-up current source)	E
37	INA2	Input	Switch input pin 2 under VPUA power supply system (with an internal pull-up current source)	E
38	INA3	Input	Switch input pin 3 under VPUA power supply system (with an internal pull-up current source)	E
39	INA4	Input	Switch input pin 4 under VPUA power supply system (with an internal pull-up current source)	E
40	INA5	Input	Switch input pin 5 under VPUA power supply system (with an internal pull-up current source)	E
41	INA6	Input	Switch input pin 6 under VPUA power supply system (with an internal pull-up current source)	E
42	INA7	Input	Switch input pin 7 under VPUA power supply system (with an internal pull-up current source)	E
43	INA8	Input	Switch input pin 8 under VPUA power supply system (with an internal pull-up current source)	E
44	INA9	Input	Switch input pin 9 under VPUA power supply system (with an internal pull-up current source)	E
45	VPUA	Input	Power supply input pin for INA and INZ switches	--
46	VPUA	Input	Power supply input pin for INA and INZ switches	--
47	N.C.	-	No Connection*(Note 5)*	--
48	GND	Ground	Ground pin	--
49	N.C.	-	No Connection*(Note 5)*	--
50	N.C.	-	No Connection*(Note 5)*	--
51	N.C.	-	No Connection*(Note 5)*	--
52	INZ0	Input	Switch input pin 0 under VPUA power supply system (with an internal pull-up/down current source)	D
53	INZ1	Input	Switch input pin 1 under VPUA power supply system (with an internal pull-up/down current source)	D
54	INZ2	Input	Switch input pin 2under VPUA power supply system (with an internal pull-up/down current source)	D
55	INZ3	Input	Switch input pin 3 under VPUA power supply system (with an internal pull-up/down current source)	D
56	INZ4	Input	Switch input pin 4 under VPUA power supply system (with an internal pull-up/down current source)	D
57	INZ5	Input	Switch input pin 5 under VPUA power supply system (with an internal pull-up/down current source)	D
58	INZ6	Input	Switch input pin 6 under VPUA power supply system (with an internal pull-up/down current source)	D
59	INZ7	Input	Switch input pin 7 under VPUA power supply system (with an internal pull-up/down current source)	D
60	INZ8	Input	Switch input pin 8 under VPUA power supply system (with an internal pull-up/down current source)	D
61	INZ9	Input	Switch input pin 9 under VPUA power supply system (with an internal pull-up/down current source)	D
62	INZ10	Input	Switch input pin 10 under VPUA power supply system (with an internal pull-up/down current source)	D
63	INZ11	Input	Switch input pin 11 under VPUA power supply system (with an internal pull-up/down current source)	D
64	N.C.	-	No Connection*(Note 5)*	--
-	EXP-PAD	Exposed PAD	Short EXP-PAD on the product to ground.	--

(Note 2) Ref. Page 72 and Page 73 I/O Equivalence Circuit.
(Note 5) Keep N.C. pins electrically opened.

Block Diagram

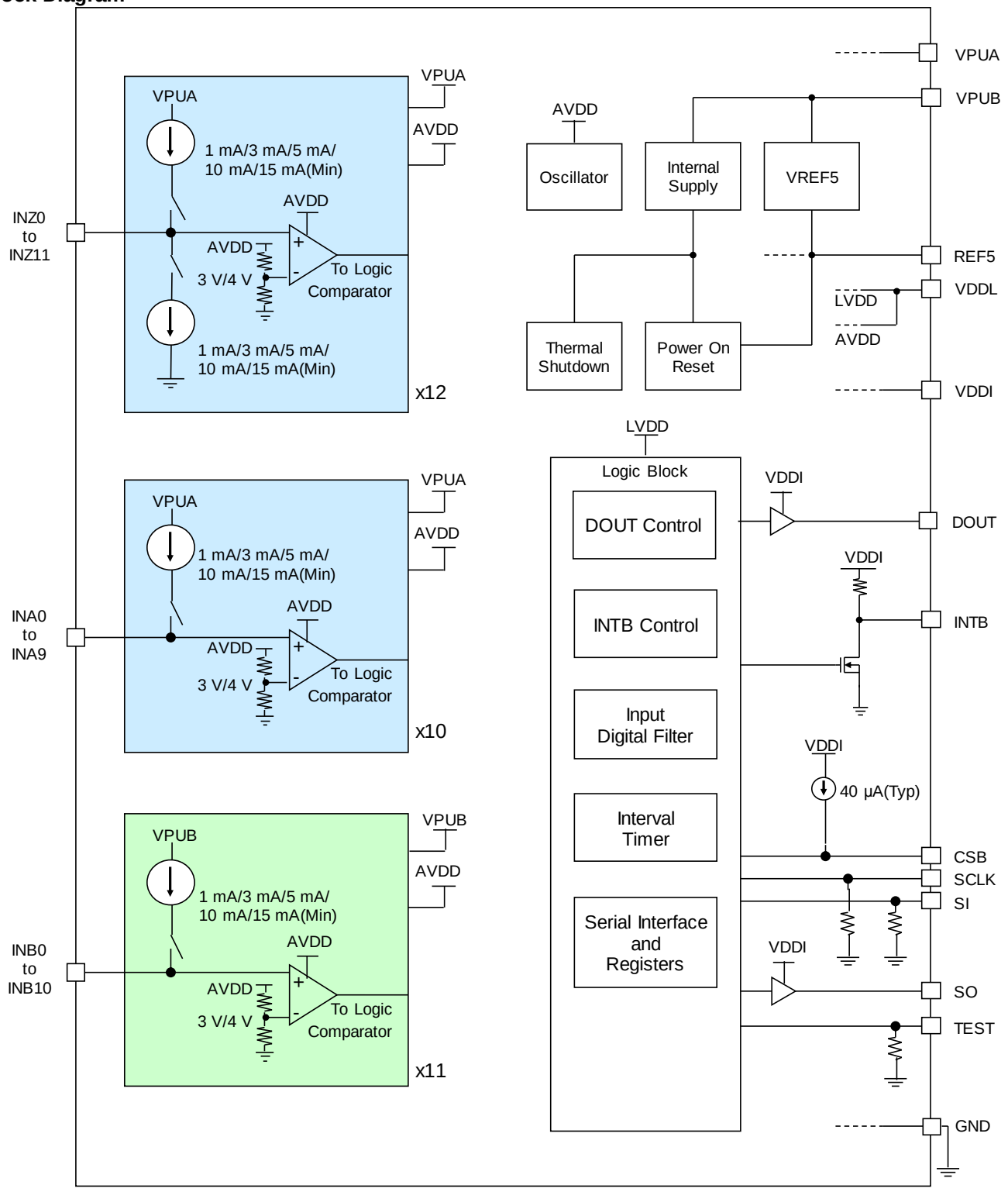


Figure 3. Block Diagram

Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply Voltage	V_{VPUA}, V_{VPUB}	-0.3 to +40.0	V
	V_{VDDI}, V_{VDDL}	-0.3 to +7.0	
Input Voltage	V_{INX} *(Note 6)*	-14 to +40	V
	V_{CSB}, V_{SCLK}, V_{SI}, V_{TEST}	-0.3 to +7.0	
Output Voltage	V_{DOUT}, V_{INTB}, V_{REF5}, V_{SO}	-0.3 to +7.0	V
Maximum Junction Temperature	Tjmax	150	°C
Storage Temperature	Tstg	-55 to +150	°C

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 6) INx = INB0 to INB10, INA0 to INA9, INZ0 to INZ11

Thermal Resistance(Note 7)

Table 4. Thermal Resistance

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 9)	2s2p(Note 10)	
HTQFP64BV				
Junction to Ambient	θ_{JA}	64.5	16.1	°C/W
Junction to Top Characterization Parameter (Note 8)	Ψ_{JT}	3	2	°C/W

(Note 7) Based on JESD51-2A(Still-Air)
(Note 8) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 9) Using a PCB board based on JESD51-3 (Table 5).
(Note 10) Using a PCB board based on JESD51-5, 7 (Table 6).

Table 5. 1s

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 µm

Table 6. 2s2p

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 11)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 µm	74.2 mm x 74.2 mm	35 µm	74.2 mm x 74.2 mm	70 µm

(Note 11) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

Table 7. Recommended Operating Conditions

Parameter	Symbol	Ratings		Unit
		Min	Max	
Operating Temperature	Topr	-40	+125	°C
VPUA/VPUB Supply Voltage	V_{VPUX}	6.0	28.0	V
VDDI Supply Voltage	V_{VDDI}	3.1	5.25	V
Capacitance for REF5(Note 12)	C_{REF}	4.7	-	µF

(Note 12) Recommend a ceramic capacitance. Consider variation, temperature characteristics, DC bias characteristics and change over time of capacitance in order not to become lower than minimum rating.

Electrical Characteristics

Spec conditions: 6.0 V≤VPUA/VPUB≤28 V, 3.1 V≤VDDI≤5.25 V, -40 °C≤Topr≤+125 °C
VPUA/VPUB/INZ/INA/INB pin: resistors and capacitors are not connected
REF5 pin: 4.7 µF
Unless otherwise specified, the typical condition is VPUA/VPUB=13 V, VDDI=5.00 V, Topr=25 °C.

Table 8. Electrical Characteristics

Parameter	Symbol	Min	Typ	Max	Unit
VPUA/VPUB Supply Voltage Low-voltage Operating Range*(Note 13)* Fully Operational Voltage Range High-voltage Operating Range*(Note 14)*	 $V_{VPUX(QFL)}$ $V_{VPUX(FO)}$ $V_{VPUX(QFH)}$	 3.9 6.0 28.0	 - - -	 6.0 28.0 40.0	V
POR(Power on Reset) Activation Voltage*(Note 15)*	$V_{POR(LOW)}$	3.9	4.2	4.5	V
POR(Power on Reset) Deactivation Voltage*(Note 15)*	$V_{POR(HIGH)}$	4.0	4.3	4.6	V
VPUA/VPUB Operating Current Continuous Monitoring Current source is disabled, “Hi-Z” Status	$I_{VPUX(OFF)}$	-	-	720	µA
VPUA/VPUB Average Operating Current Intermittent Monitoring Monitoring Period=50 ms, Strobe Time=125 µs Source/Sink Current Setting=1 mA	$I_{VPUX(SS)}$	-	80	110	µA
VDDI Operating Current INTB=“H”, CSB=“H”	I_{VDDI}	-	5	10	µA
REF5 Output Voltage	V_{REF5}	4.75	5.00	5.25	V

(Note 13) Electrical characteristics are not guaranteed though functions are operating. POR is active between 3.9 V and 4.5 V.
(Note 14) Electrical characteristics are not guaranteed though functions are operating.
(Note 15) The POR circuit monitors the REF5 voltage.

Electrical Characteristics - continued

Table 9. Electrical Characteristics (Switch Input)

Parameter	Symbol	Min	Typ	Max	Unit
Source Current 1 (internal pull-up current source) 0 V external supply, VPUA/VPUB system (1 mA setting)	$I_{SOURCE1}$	1.0	1.4	1.8	mA
Sink Current 1 (internal pull-down current source) 8 V external supply, VPUA system (1 mA setting)	I_{SINK1}	1.0	1.4	1.8	mA
Source Current 2 (internal pull-up current source) 0 V external supply, VPUA/VPUB system (3 mA setting)	$I_{SOURCE3}$	3.0	4.2	5.4	mA
Sink Current 2 (internal pull-down current source) 8 V external supply, VPUA system (3 mA setting)	I_{SINK3}	3.0	4.2	5.4	mA
Source Current 3 (internal pull-up current source) 0 V external supply, VPUA/VPUB system (5 mA setting)	$I_{SOURCE5}$	5.0	7.0	9.0	mA
Sink Current 3 (internal pull-down current source) 8 V external supply, VPUA system (5 mA setting)	I_{SINK5}	5.0	7.0	9.0	mA
Source Current 4 (internal pull-up current source) 0 V external supply, VPUA/VPUB system (10 mA setting) VPUA/VPUB=6.0 V to 8.0 V VPUA/VPUB=8.0 V to 28.0 V	$I_{SOURCE10}$	 5.0 10.0	 14.0 14.0	 18.0 18.0	mA
Sink Current 4 (internal pull-down current source) 8 V external supply, VPUA system (10 mA setting)	I_{SINK10}	10.0	14.0	18.0	mA
Source Current 5 (internal pull-up current source) 0 V external supply, VPUA/VPUB system (15 mA setting) VPUA/VPUB=6.0 V to 8.0 V VPUA/VPUB=8.0 V to 28.0 V	$I_{SOURCE15}$	 5.0 15.0	 21.0 21.0	 27.0 27.0	mA
Sink Current 5 (internal pull-down current source) 8 V external supply, VPUA system (15 mA setting)	I_{SINK15}	15.0	21.0	27.0	mA
Low to High Switch Detection Threshold Voltage (3.0 V setting)	$V_{TH3(HIGH)}$	2.7	3.0	3.3	V
High to Low Switch Detection Threshold Voltage (3.0 V setting)	$V_{TH3(LOW)}$	2.6	2.9	3.2	V
Low to High Switch Detection Threshold Voltage (4.0 V setting) VPUA/VPUB= 7.0 V to 28.0 V*(Note 16)*	$V_{TH4(HIGH)}$	3.7	4.0	4.3	V
High to Low Switch Detection Threshold Voltage (4.0 V setting) VPUA/VPUB=7.0 V to 28.0 V*(Note 16)*	$V_{TH4(LOW)}$	3.6	3.9	4.2	V

(Note 16) Electrical characteristics are not guaranteed between 6.0 V≤V_{VPUX}<7.0 V.

Electrical Characteristics - continued

Table 10. Electrical Characteristics (Static Electrical Characteristics)

Parameter	Symbol	Min	Typ	Max	Unit
Serial Interface Threshold Voltage*(Note 17)*	$V_{INLOGIC}$	0.8	-	2.2	V
CSB Input Current CSB=VDDI	$I_{CSB(HIGH)}$	-10	-	+10	µA
CSB Pull-up Current CSB=0 V	$I_{CSB(LOW)}$	30	40	85	µA
SI, SCLK Pull-down Resistor	R_{SI},R_{SCLK}	50	100	150	kΩ
SI, SCLK Input Current SI, SCLK=0 V	$I_{SI(LOW)}$,$I_{SCLK(LOW)}$	-10	-	+10	µA
SO “H” Level Output Voltage I_{SOURCE}=200 µA	$V_{SO(HIGH)}$	V_{VDDI}-0.8	-	V_{VDDI}	V
SO “L” Level Output Voltage I_{SINK}=1.6 mA	$V_{SO(LOW)}$	-	-	0.4	V
SO (Set to “Hi-Z”) Input Current 0 V to VDDI	$I_{SO(TRI)}$	-10	-	+10	µA
DOUT “H” Level Output Voltage I_{SOURCE}=200 µA	$V_{DOUT(HIGH)}$	V_{VDDI}-0.8	-	V_{VDDI}	V
DOUT “L” Level Output Voltage I_{SINK}=1.6 mA	$V_{DOUT(LOW)}$	-	-	0.4	V
INTB Internal Pull-up Current	$I_{INTB(PU)}$	15	53	85	µA
INTB “H” Level Output Voltage INTB=OPEN	$V_{INTB(HIGH)}$	V_{VDDI}-0.5	-	V_{VDDI}	V
INTB “L” Level Output Voltage I_{SINK}=1.0 mA	$V_{INTB(LOW)}$	-	0.2	0.4	V

(Note 17) Applicable to SCLK, SI, CSB.

Electrical Characteristics - continued

Table 11. Electrical Characteristics (Dynamic Electrical Characteristics)

Parameter	Symbol	Min	Typ	Max	Unit
Wetting Current Timer Counting starts after n-times detection of matched LPF	t_{WCT}	13	-	22	ms
Interrupt Delay Time 1 Time from switch status change to INTB output change in continuous monitoring	t_{INTB_DLY1}	-	-	1	ms
Interrupt Delay Time 2 Time from switch status change to INTB output change in intermittent monitoring n: Setting time of LPF matched n times	t_{INTB_DLY2}	-	-	[Monitor cycle] x n+1	ms
Interrupt Clear Time Time from CSB rising edge to INTB output change	t_{INTB_CLR}	-	-	150	µs
Command Set Time Time from CSB rising edge to setting of register	t_{REG_EN}	-	-	150	µs
Transition Time to Normal mode Time from CSB rising edge to bit-30 of SO output	t_{MODE_DLY1}	-	-	1	ms
Transition Time to Sleep mode Time from CSB rising edge to bit-30 of SO output	t_{MODE_DLY2}	-	-	1	ms
Switch Strobe Time (93.75 µs setting)*(Note 18)*	t_{SCAN_94}	84.375	93.750	103.125	µs
Switch Strobe Time (125 µs setting)*(Note 18)*	t_{SCAN_125}	112.5	125.0	137.5	µs
Switch Strobe Time (187.5 µs setting)*(Note 18)*	t_{SCAN_188}	168.75	187.50	206.25	µs
Switch Strobe Time (250 µs setting)*(Note 18)*	t_{SCAN_250}	225	250	275	µs
Source/Sink Current Rise Time FSQ="0", FSQZ/A/B="0", 10 mA setting Load resistance 100 Ω	t_{SR_R}	-	20*(Note 19)*	-	µs
Source/Sink Current Fall Time FSQ="0", FSQZ/A/B="0", 10 mA setting Load resistance 100 Ω	t_{SR_F}	-	15*(Note 19)*	-	µs
Internal Clock Accuracy	t_{TIMER}	-10	-	+10	%

(Note 18) "H" width of internal signal which decides the timing of switch strobe. (Ref. Page 13 Figure 6).
(Note 19) Reference value.

Electrical Characteristics - continued

Table 12. Electrical Characteristics (Digital Interface Characteristics)

Parameter	Symbol	Min	Typ	Max	Unit
SCLK Frequency	f_{SCLK}	-	-	4.4	MHz
Setup Time from CSB Fall to SCLK Rise	t_{LEAD}	100	-	1000	ns
Setup Time from SCLK Fall to CSB Rise	t_{LAG}	50	-	500	ns
Setup Time from SI to SCLK Fall	$t_{SI(SU)}$	16	-	-	ns
Hold Time from SCLK Fall to SI	$t_{SI(HOLD)}$	20	-	-	ns
SI, CSB, SCLK Rise Time	$t_{R(SI)}$	-	5.0*(Note 20)*	-	ns
SI, CSB, SCLK Fall Time	$t_{F(SI)}$	-	5.0*(Note 20)*	-	ns
Time from CSB Fall to SO Output Low Impedance	$t_{SO(EN)}$	-	-	55	ns
Time from CSB Rise to SO Output High Impedance	$t_{SO(DIS)}$	-	-	55	ns
SCLK “H” Level Width	t_{SCLKH}	75	-	-	ns
SCLK “L” Level Width	t_{SCLKL}	75	-	-	ns
Time from SCLK Rise to Stable SO Data Output SO C_L=20 pF	t_{VALID}	-	25	55	ns
CSB “H” Level Time	t_{CSBH}	150	-	-	µs

(Note 20) Reference value.

Timing Chart

·Serial Access Timing

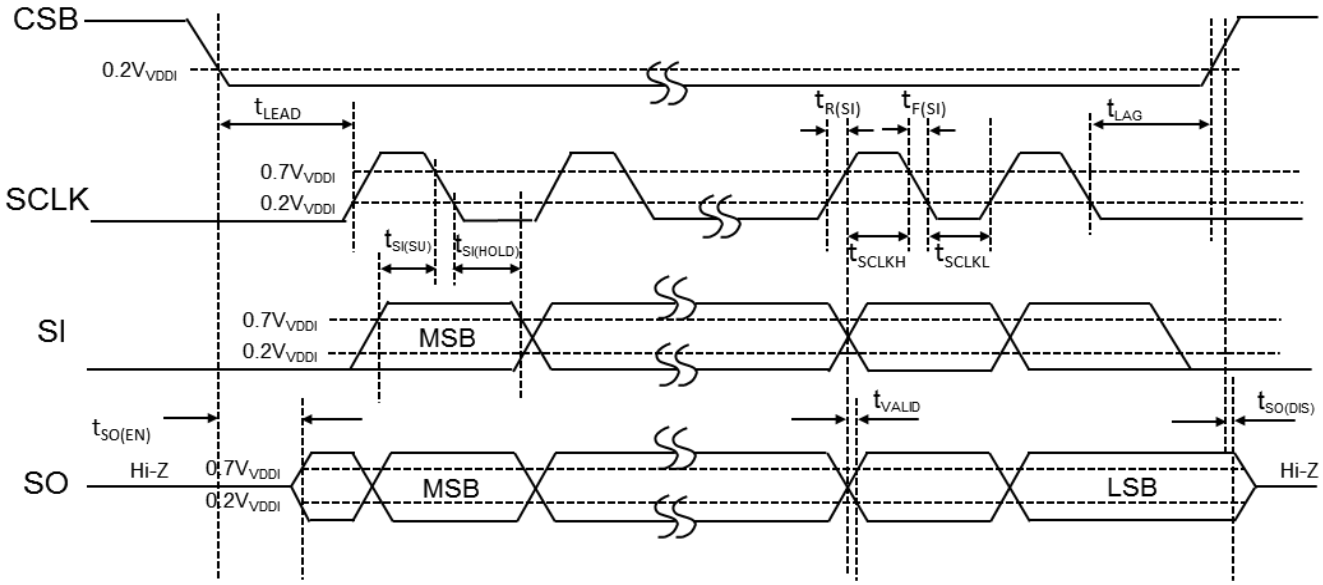


Figure 4. Serial Access Timing

Timing Chart - continued

·Power Supply Rising/Falling Sequence

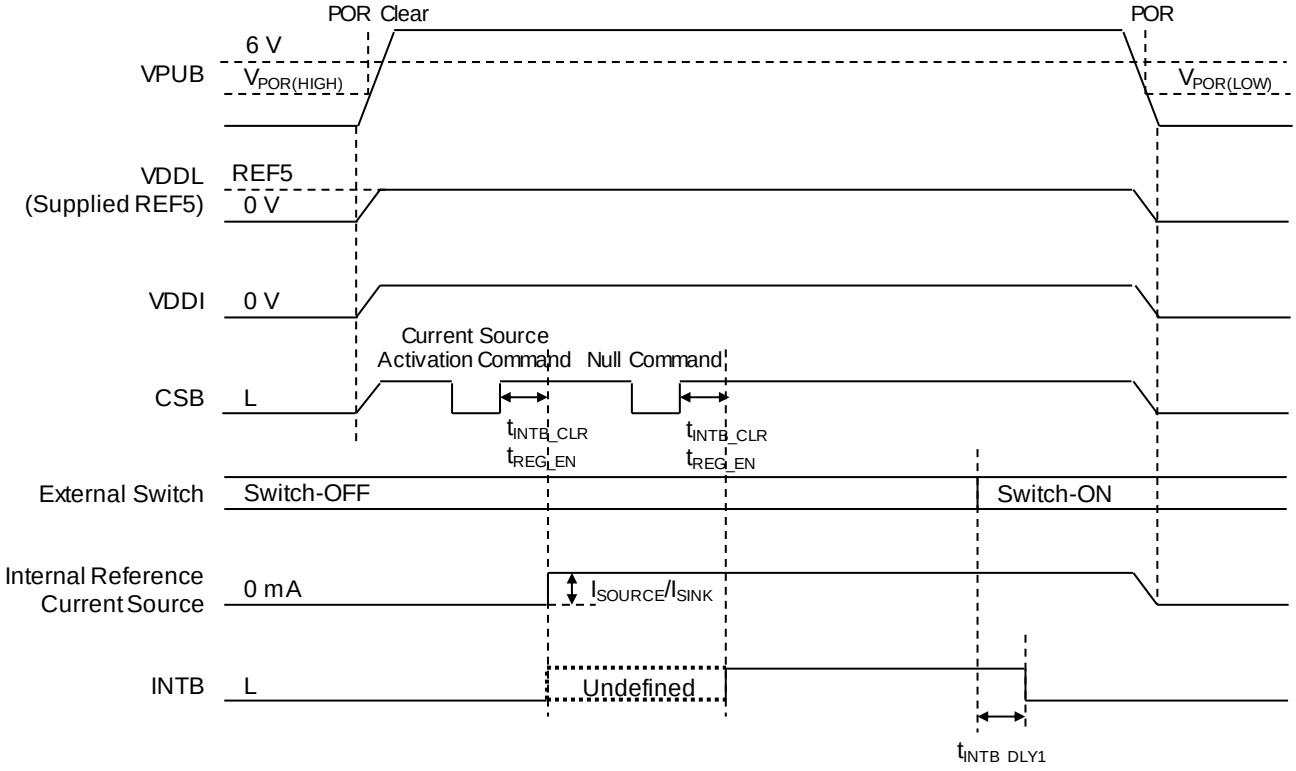


Figure 5. Power Supply Rising/Falling Sequence

·Source/Sink Current Rise and Fall Time

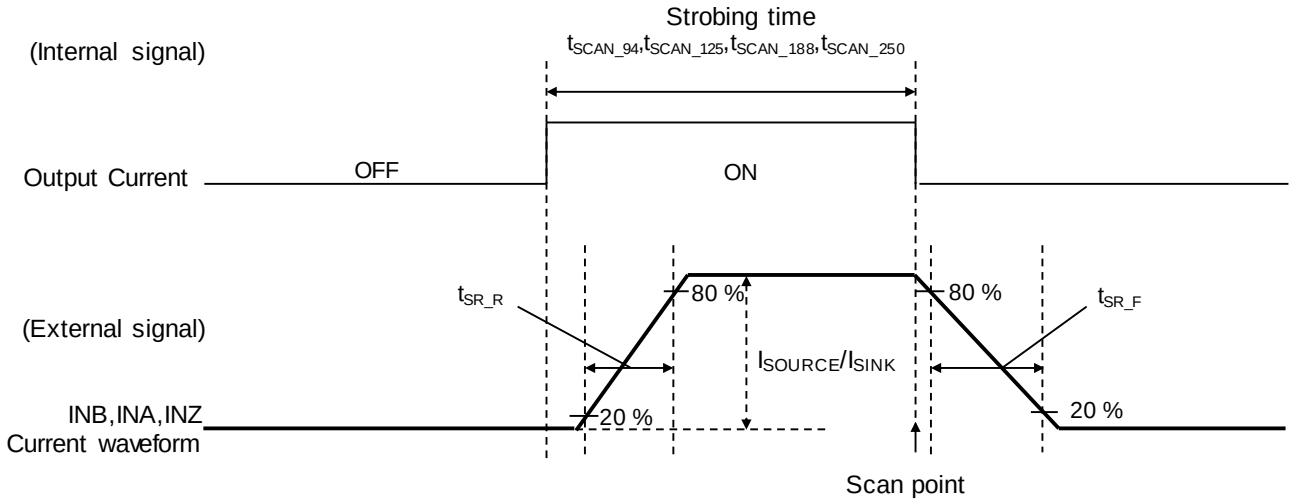


Figure 6. Intermittent Monitoring Enabled (FSQ=0, FSQZ/A/B=0), Source/Sink Current Rise and Fall Time

Basic Operation

[Basic Operation 1] Detection of Switch Status Change (Continuous Monitoring)

Upon detection of a change in switch status, interrupt (INTB="H"→"L") occurs and the IC requests serial communication with the MCU.

< Example of Recommended Operation Sequence >

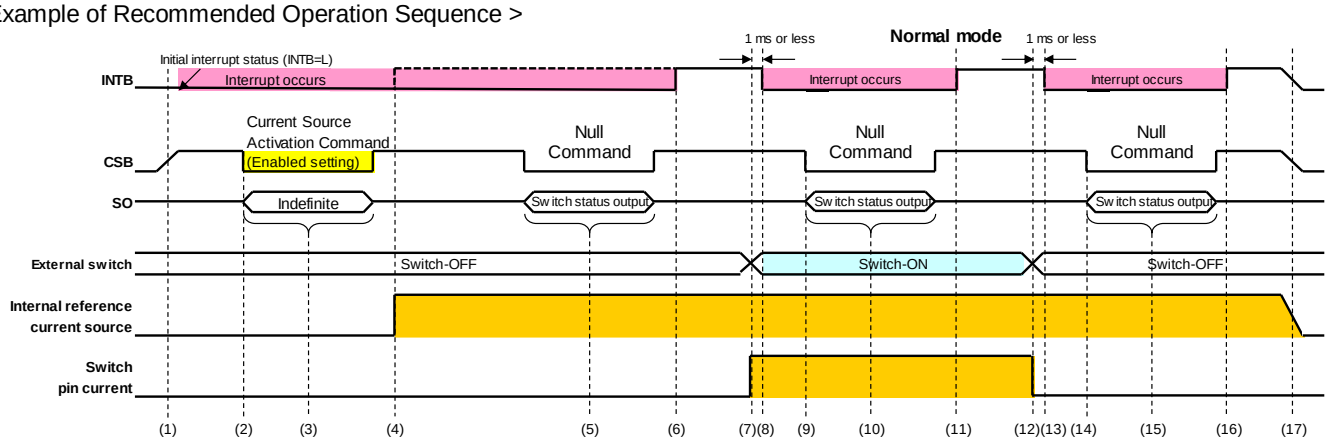


Figure 7. Basic Operation 1

(1) After power is turned on, interrupt (INTB="L") occurs.
(2) By serial communication, the switch status is obtained by the MCU at CSB falling edge.
(3) Since the current source is OFF, the switch pin is "Hi-Z", and the output of SO is undefined.
(4) Internal reference current source is activated.
(5) Switch status is output by SO.
(6) Interrupt is cleared (INTB="L"→"H") by CSB rising edge and prepares for switch change.
(7) Switch change occurs (OFF→ON) and IC detects switch status change.
(8) Interrupt (INTB="H"→"L") is notified to MCU, and serial communication is requested.
(9) By serial communication, switch status is obtained by the MCU at CSB falling edge.
(10) Switch status is output by SO.
(11) Interrupt is cleared (INTB="L"→"H") by CSB rising edge and prepares for switch change.
(12) Switch change occurs (ON→OFF) and IC detects switch status change.
(13) Interrupt (INTB="H"→"L") is notified to MCU, and serial communication is requested.
(14) By serial communication, the switch status is obtained by the MCU at CSB falling edge.
(15) Switch status is output by SO.
(16) Interrupt is cleared (INTB="L"→"H") by CSB rising edge and prepares for switch change.
(17) Power is turned off

Basic Operation - continued

[Basic Operation 2] Detection of Switch Status Change (Intermittent Monitoring)

When Intermittent Monitoring is enabled, switch status is monitored by periodically turning the current source on and off. Intermittent monitoring allows low power consumption.

< Example of Recommended Operation Sequence >

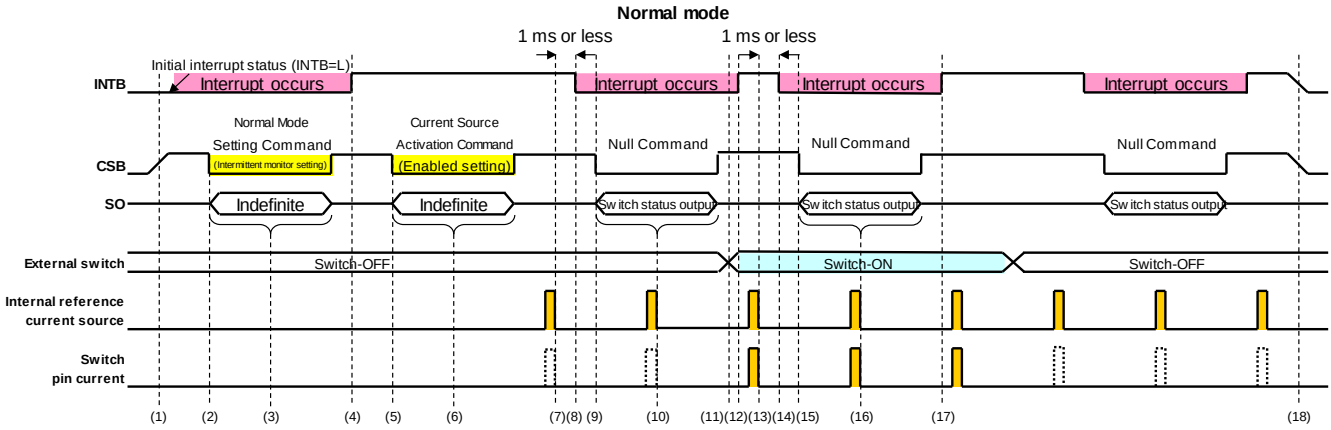


Figure 8. Basic Operation 2

(1) After power is turned on, interrupt (INTB="L") occurs.
(2) By serial communication, the switch status is obtained by the MCU at CSB falling edge.
(3) Since the current source is OFF, the switch pin is "Hi-Z", and the output of SO is undefined.
(4) Interrupt is cleared (INTB="L"→"H") by CSB rising edge and prepares for switch change.
(5) By serial communication, switch status is obtained by the MCU at CSB falling edge.
(6) Since the current source is OFF, the switch pin is "Hi-Z", and the output of SO is undefined.
(7) IC gets the switch status when the current source is ON.
(8) Interrupt (INTB="H"→"L") is notified to MCU, and serial communication is requested.
(9) By serial communication, switch status is obtained by the MCU at CSB falling edge.
(10) Switch status is output by SO.
(11) Switch change occurs (OFF→ON).
(12) Interrupt is cleared (INTB="L"→"H") by CSB rising edge and prepares for switch change.
(13) IC detects switch status change.
(14) Interrupt (INTB="H"→"L") is notified to MCU, and serial communication is requested.
(15) By serial communication, switch status is obtained by the MCU at CSB falling edge.
(16) Switch status is output by SO.
(17) Interrupt is cleared (INTB="L"→"H") by CSB rising edge and prepares for switch change.
(18) Power is turned off.

Basic Operation - continued

[Basic Operation 3] Sleep Mode Operation (Manual Transition)

When MDC register of Monitor Mode Transition Command is set to “1”, mode is changed to sleep.
When MDC register of Monitor Mode Transition Command is set to “0”, mode is changed to normal.

< Example of Recommended Operation Sequence >

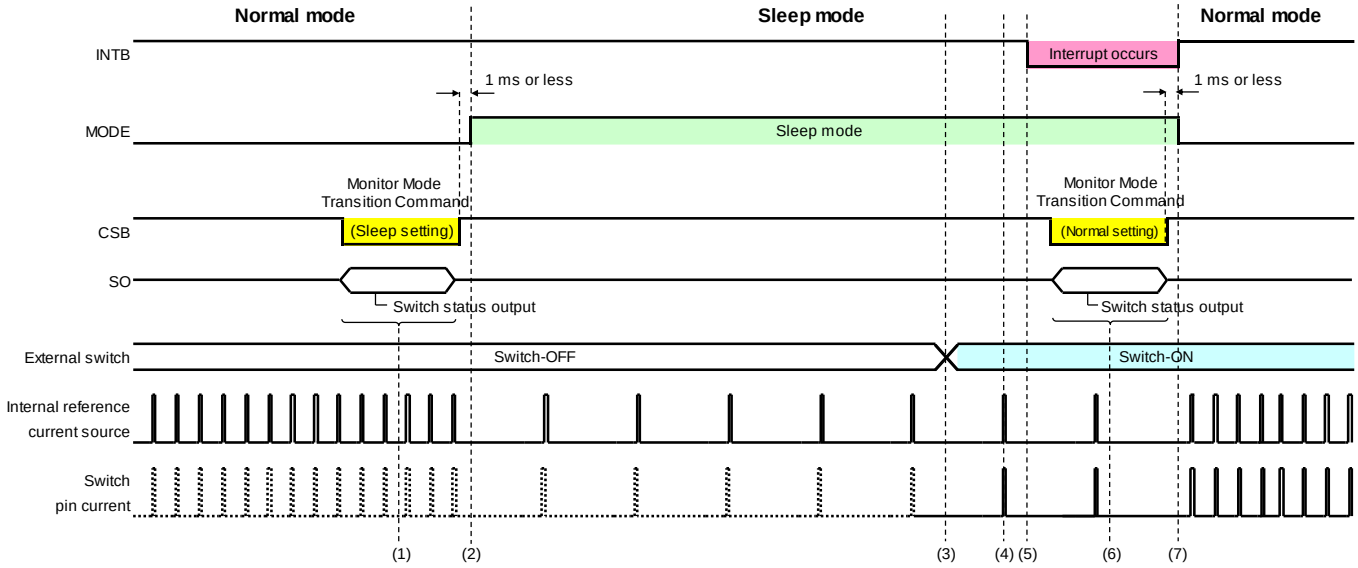


Figure 9. Basic Operation 3

(1) Monitor mode transition command (sleep mode setting) is received from MCU.
(2) Transition to sleep mode.
(3) Switch change occurs (OFF→ON).
(4) IC detects switch status change.
(5) IC informs MCU the interrupt (INTB=“H”→“L”) and serial communication is requested.
(6) Monitor mode transition command (normal mode setting) is received from MCU.
(7) Transition to normal mode.

Basic Operation - continued

[Basic Operation 4] Sleep Mode Operation (Automatic Transition to Normal Mode)

Automatic transition from sleep mode to normal mode when a switch status changes is possible when the automatic mode transition setting is enabled.

< Example of Recommended Operation Sequence >

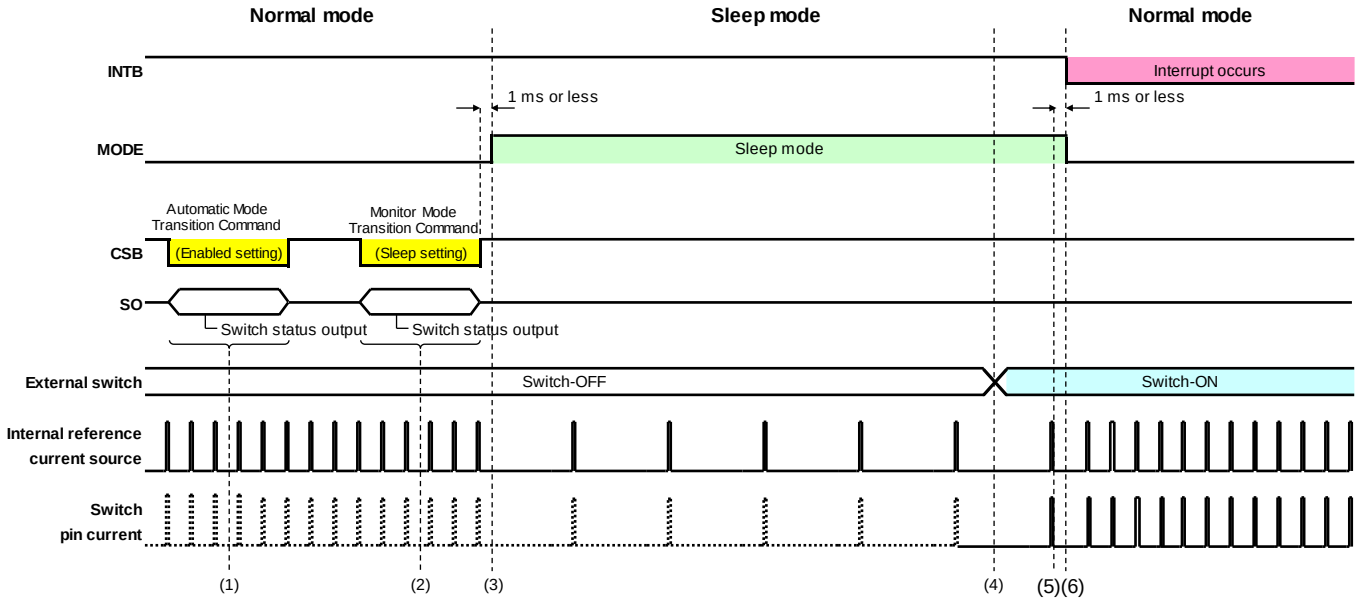


Figure 10. Basic Operation 4

(1) Automatic transition of mode is enable.
(2) Monitor mode transition command (sleep mode setting) is received from MCU.
(3) Transition to sleep mode.
(4) Switch change occurs (OFF→ON).
(5) IC detects switch status change.
(6) IC informs the interrupt to MCU with INTB(“H”→“L”) and changes to normal mode automatically.

Description of Functions

1. Power on Reset (POR)

Upon the application of an external voltage to VPUB, REF5 output is generated by the LDO(VREF5) inside the IC.
When REF5 ≤ 4.2 V(Typ), POR is activated.
When REF5 ≥ 4.3 V(Typ), POR is deactivated.

2. Serial Interface

Communication between IC and the MCU uses pins chip select bar input (CSB), serial clock input (SCLK), serial data input (SI), and serial data output (SO).
CSB is internally pulled-up to VDDI. When CSB status is “0”, SCLK and SI inputs are valid, and it is possible to read data from SO. When CSB status is “1”, SCLK and SI inputs are invalid, and SO status is “Hi-Z”.

·Communication Frame

The transmitted frame by the MCU is a bit-56 structure composed of the fixed transmission and reception discrimination “01” (bit-55 to bit-54), the address (bit-53 to bit-48), the setting data (bit-47 to bit-8), and the CRC (bit-7 to bit-0). The fixed transmission and reception discrimination ”01” (bit-55 to bit-54) is intended to differentiate between the transmitted and the received frame. The command (bit-53 to bit-8) sets various settings such as the “Interrupt Notification of Switch Change Setting Command”. The CRC (bit-7 to bit-0) outputs the result of a bit-55 to bit-8 CRC calculation. If a CRC error occurs, either when the structure of the frame is not bit-56 or when the transmission and reception discrimination bit is an error, communication error (the bit-49 of the SO frame is “H”) is output and data is not recognized. As for writing, SI data is latched by internal shift register at timing of SCLK falling.

Table 13. Serial Data Input (SI)

Communication frame	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
SI Input Bit	Register Address								Setting Data							
	0	1	Address													

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
Setting Data															

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
Setting Data																CRC

The received frame by the MCU has two types of bit alignment, “switch status output” and “register value output”.

The switch status output bit alignment is a bit-56 structure composed of fixed transmission and reception discrimination “10” (bit-52 to bit-48), fixed value “0” (bit-47), interrupt factor output (bit-52 to bit-48), fixed value “0” (bit-47), mode status output (bit-46), fixed value “0” (bit-45 to bit-41), switch status output (bit-40 to bit-8), and CRC (bit-7 to bit-0).
Fixed transmission and reception discrimination “10” (bit-52 to bit-48) is intended to discriminate transmit and receive frame. Interrupt factor (bit-52 to bit-48) is discussed on Page 20. When an interrupt factor occurs, the corresponding bit becomes “1”. Mode status (bit-46) is “0” when set to normal mode, and it is “1” when set to sleep mode. Switch status output (bit-40 to bit-8) is “1” when external switch is ON, and it is “0” when external switch is OFF. The CRC (bit-7 to bit-0) outputs the result of a bit-55 to bit-8 CRC calculation.
The switch status is latched to the timing of CSB falling edge. Then, in order of interrupt factor output, mode status and switch status output are output from SO by SCLK rising.

Table 14. Serial Data Output (SO-Switch Status Output)

Output frame	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
SO Output Bit	1	0	0	Interrupt Factor Output					0	Mode	0	0	0	0	0	Switch INB10 Status Output

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
Switch INB9 to INB0 Status Output										Switch INA9 to INA4 Status Output					

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
Switch INA3 to INA0 Status Output				Switch INZ11 to INZ0 Status Output												CRC

Description of Functions - continued

The register value output bit alignment is a bit-56 structure composed of fixed transmission and reception discrimination “10” (bit-55 to bit-54), fixed value “0” (bit-53), interrupt factor output (bit-52 to bit-48), register value output (bit-47 to bit-8), and CRC (bit-7 to bit-0).
The data is output by SO at SCLK's rising edge after the CSB falling edge of the command following the register value output command.
The bit alignment of the register value output is shown on Table 38. The sequence of register value output is shown in Figure 11 and Figure 12.

Table 15. Serial Data Output (SO-Register Value Output)

Output frame	55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
SO Output Bit (Register Value)	1	0	0	Interrupt Factor Output					Register Value Output							

39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
Register Value Output															

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
Register Value Output																CRC

The register value output command (Table 36 RIER to RMDR) is used to read-back the register value written by register write command (Table 36 IER to MDR).
Figure 11 describes the single read-back sequence. Figure 12 describes the continuous read-back sequence.

<Single Read-back Sequence – Recommended Sequence>

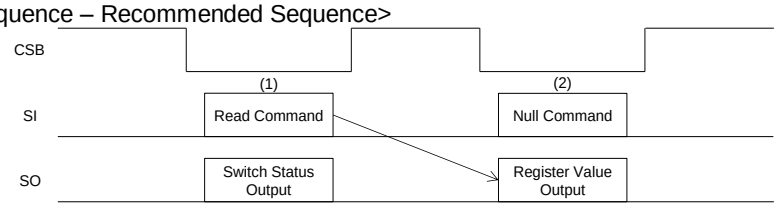


Figure 11. Single Read-back Sequence

(1) Send the register value output command.
The switch status is output by SO.
(2) Read the register value by sending the Null command.
The result of the register value output command (1) is output by SO.

<Continuous Sequential Read-back Sequence – Recommended Sequence>

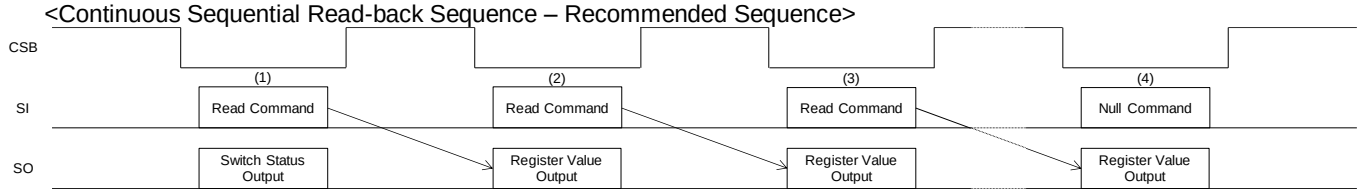


Figure 12. Continuous Read-back Sequence

(1) Send the register value output command.
The switch status is output by SO.
(2) Send the register value output command following (1). (The address of the register value output command does not need to be the next address.)
(3) Send the register value output command repeatedly as needed.
The SO output at each command is the result of the previous register value output command.
(4) Send the Null command in the end.
The register value of the previous register output command is output by SO.

3. Switch Status Output
Switch status can be sent through SO output.

Description of Functions - continued

4. Interrupt (INTB operation)

There are five interrupt factors that cause the INTB pin to output “L”. The type of interrupt factor that occurred can be checked in the SO output when CSB is “L”.
INTB output will return to “H” once the interrupt factor is cleared by the rising edge of CSB. The INTB pin is an open-drain output that is internally pulled-up to VDDI.

·Interrupt Factors

The interrupt factors are shown below:

Interrupt Factor	Interrupt flag (SO output)	Flag name
(1) Test Detection	SO output bit [52]:	“test_flg”
(2) Thermal Shutdown Detection	SO output bit [51]:	“them_flg”
(3) Reset Detection	SO output bit [50]:	“rst_flg”
(4) Communication Error Detection (CRC error, 56-bit frame error, or transmission and reception discrimination error)	SO output bit [49]:	“err_flg”
(5) Switch Status Change Detection	SO output bit [48]:	“sw_flg”

(1) Test Detection

The IC generates an interrupt after a transition to test mode. The TEST pin should always be connected to ground.

(2) Thermal Shutdown Detection

Interrupt occurs when the thermal shutdown circuit detects a temperature higher than the allowable junction temperature inside IC.

(3) Reset Detection

Interrupt occurs after the activation of Power on Reset (POR) or the transmission of the reset command. Upon POR activation, the SO output interrupt flag “rst_flg” is reflected instantly. With reset command transmission, “rst_flg” is reflected on the next command transmission.

(4) Communication Error Detection

Interrupt occurs due to either a CRC error, a 56-bit frame error, or a command transmission error. The interrupt flag “err_flg” is triggered by the following:

CRC error	:when there is a Cyclic Redundancy Check error
56-bit frame error	:when the command received is not 56-bit
Transmit and receive determination error	:when the first two bits of the command received is not [55:54]=“01”

(5) Switch Status Change Detection

Interrupt occurs when switch status changes (switch-ON→OFF or switch-OFF→ON).

·Clearing of INTB Output and Interrupt Factor

The INTB “L” output and the interrupt factor are both cleared by the CSB rising edge during command transmission. In case a new interrupt factor occurs during command transmission, the interrupt factor is not cleared. The new interrupt factor is reflected on the next command transmission.
The interrupt factor is not cleared by the register readout that follows the register value output command.

Description of Functions - continued

5. Operating Modes

IC has two types of operating mode, the normal and the sleep mode. Transition between the two modes can be done by sending the correct “Monitor Mode Transition Command”. The current mode of operation can be checked through the SO pin outputs.

Monitor Mode Transition register address (0x4F):Bit [47]: 0=Normal mode, 1=Sleep mode

·Normal Mode

Normal mode operation can be set to continuous monitoring, wherein the switch status is checked by a continuously ON current source, or to intermittent monitoring, wherein the switch status is checked by a regularly ON/OFF current source.
The period of intermittent monitoring(Note 21) can be set according to power supply system while strobe time(Note 22) is common for all switch pins.
At normal mode, the bit-46 of the SO output is “0”.

·Sleep Mode

Sleep mode operation, like in normal mode, can be set to continuous monitoring or intermittent monitoring.
The monitoring period(Note 21) of intermittent monitoring can be set according to power supply system.
The strobe time(Note 22) is common for all switch pins and both modes.

The difference with normal mode is that, from sleep mode, it is possible to change to normal mode automatically when interrupt occurs. (Automatic mode transition function)
At sleep mode, the bit-46 of SO output is “1” at sleep mode.

(Note 21) Ref. Monitor period (Figure 13).
(Note 22) Ref. Strobe time (Figure 13).

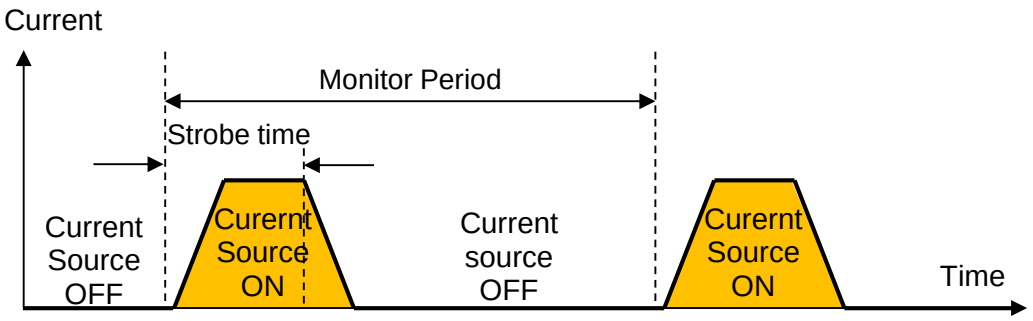


Figure 13. Intermittent Monitoring

6. Automatic Mode Transition Function

By sending the “Automatic Mode Transition Command” through setting the MIR register (0x4E) to “1”, automatic transition from sleep to normal mode is possible. The conditions for a change in mode from sleep to normal to occur for both enabled and disabled “Automatic Mode Transition Function” are shown below:

·Conditions for Sleep to Normal Mode Transition (“Automatic Mode Transition Function” is enabled):
1. Normal mode transition command is sent
2. POR occurs or reset command sent (Initialization)
3. A switch status changes (The “Switch Change Interrupt Setting” should be enabled)

·Conditions for Sleep to Normal Mode Transition (“Automatic Mode Transition Function” is disabled):
1. Normal mode transition command is sent
2. POR occurs or reset command sent (Initialization)

Description of Functions - continued

[Extension Function1: Intermittent Monitoring at the Same Time (with Current Slope)]

In intermittent monitoring, it is possible to detect the status of the all switches at the same time. When all inputs are set to detect the switch status by intermittent monitoring, the wetting current has a rising and falling slope.
(only when all comparators are enabled with “Comparator Operation Control Command”).

Normal Mode Setting Register (0x4B) : bit-47 to bit-44 is “0000” and intermittent monitoring setting
Sleep Mode Setting Register (0x4C) : bit-47 to bit-44 is “0000” and intermittent monitoring setting

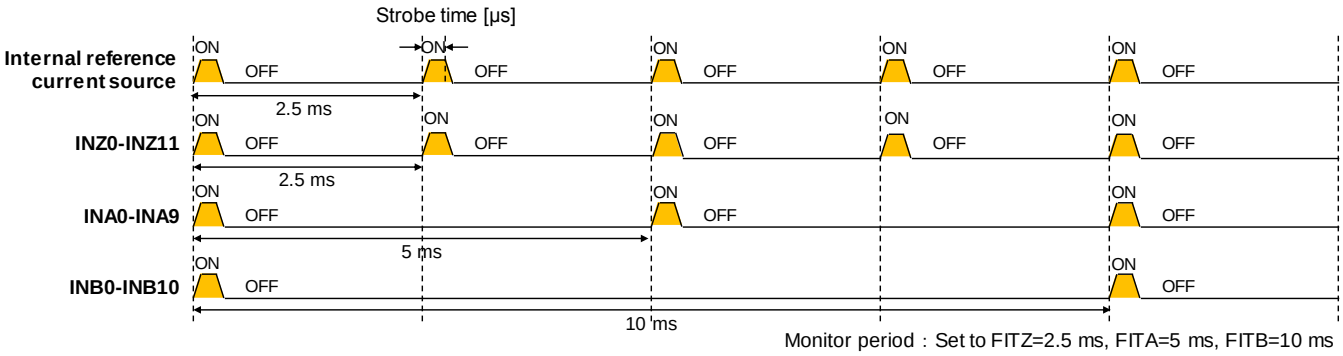


Figure 14. Intermittent Monitoring at the Same Time Example

[Extension Function 2: Sequential Monitoring by Power Supply System]

In this type of sequential monitoring, the status of the switches within a power supply system is monitored one at a time. This type has no slope. Since no two or more current sources in a power supply system are ON at the same time, radiation noise is reduced.

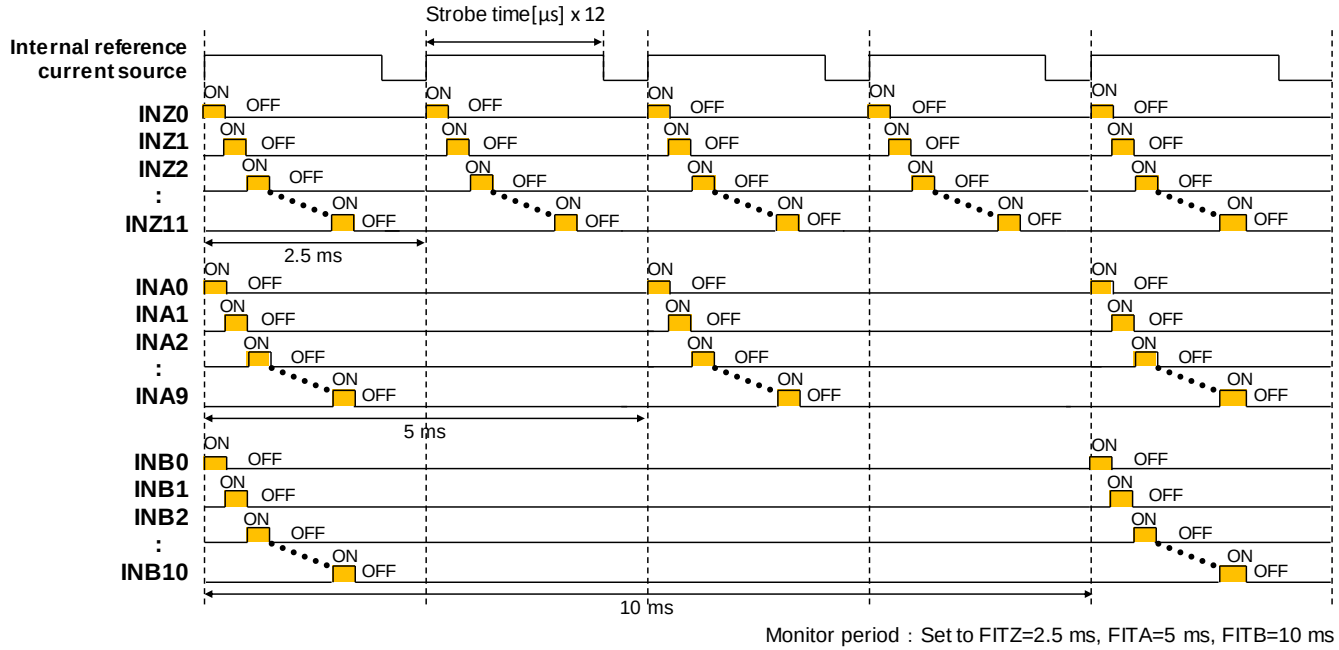


Figure 15. Sequential Monitoring by Power Supply System Example

Description of Functions - continued

[Extension Function 3: Sequential Monitoring of All Switch Pins]

In this type of sequential monitoring, the status of all switches is monitored one at a time.
Since no two or more current sources are ON at the same time, radiation noise is reduced. This type has no slope.

The monitoring period for all switches increases by four times the monitoring period set for the INZ channels as shown in Figure 16. Uniform sequential monitoring and sequential monitoring by power supply should not be enabled at the same time. In case the two sequential monitoring methods are activated simultaneously, the method which prevails is uniform sequential monitoring.

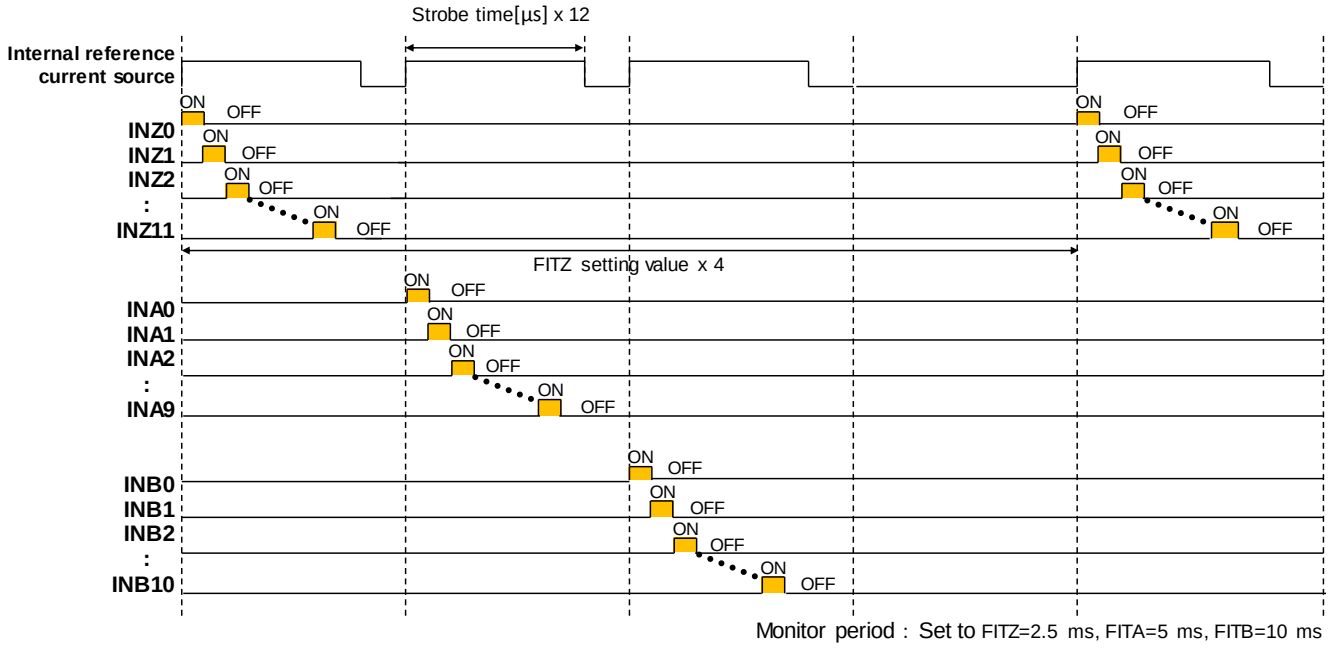


Figure 16. Sequential Monitoring of All Switches Pins Example

Description of Functions - continued

7. Source/Sink Current Source for Switch Pin

There are three types of switch pin inputs with internal current source: INZ, INA, and INB. The current level can be set for each switch pin.

·Current Source of INZ System (INZ0 to INZ11)

This current source is used to source or sink current to the external switch. The wetting current can be interchanged between pull-up and pull-down. VPUA is the power supply for the pull-up current source.

·Current Source of INA System (INA0 to INA9)

This current source is used to source current to the external switch. VPUA is the power supply.

·Current Source of INB System (INB0 to INB10)

This current source is used to source current to the external switch. VPUB is the power supply.

The current source settings can be fixed by INZ current source/sink selection command, the current source setting command, and the holding current/wetting current value setting command.

Description of Functions - continued

8. Wetting Current Timer

The wetting current timer is 13 ms to 22 ms. This function can be enabled individually for each switch pin. The timer starts after the switch has been detected as ON. After the 13 ms to 22 ms timer is finished, the wetting current (10 mA/15 mA) is switched to holding current (1 mA/3 mA/5 mA). The timer is reset after the switch is turned OFF.

[Function operation1] Wetting Current Timer (Continuous Operation)

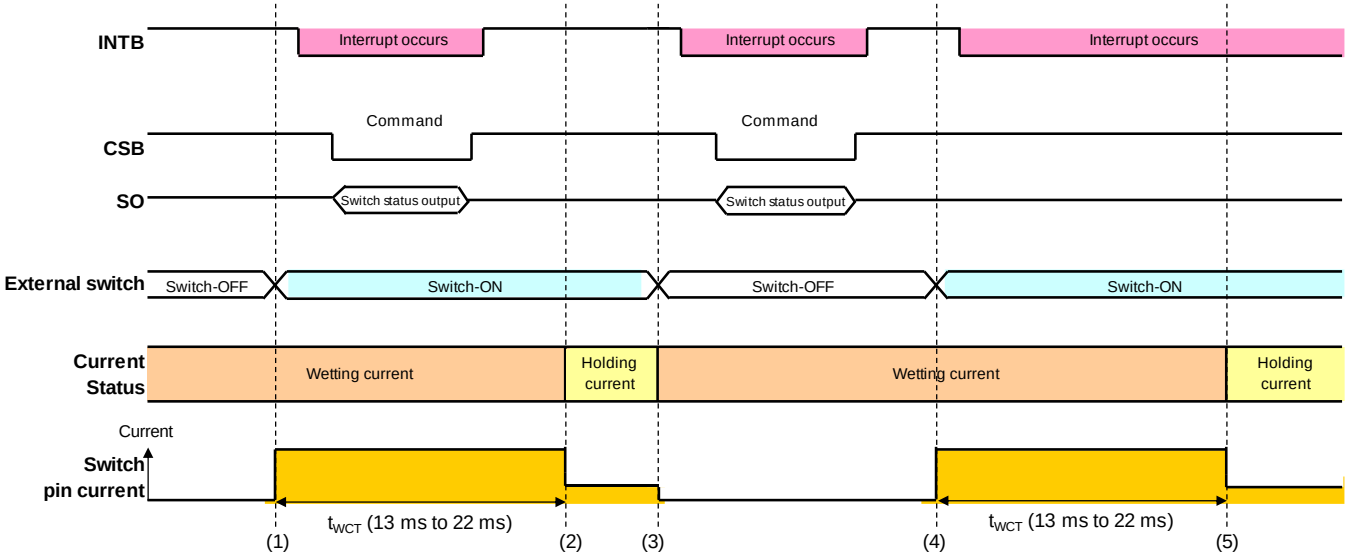


Figure 17. Wetting Current Timer (Continuous Operation)

(1) Switch change occurs (OFF→ON), IC detects switch status change.
(2) When ON state of the switch continues for more than 13 ms to 22 ms, the holding current is output.
(3) Switch change occurs (ON→OFF).
(4) Switch change occurs (OFF→ON), IC detects switch status change.
(5) When ON state of the switch continues for more than 13 ms to 22 ms, the holding current is output.

Description of Functions - continued

[Function operation2] Wetting Current Timer (Intermittent Monitoring)

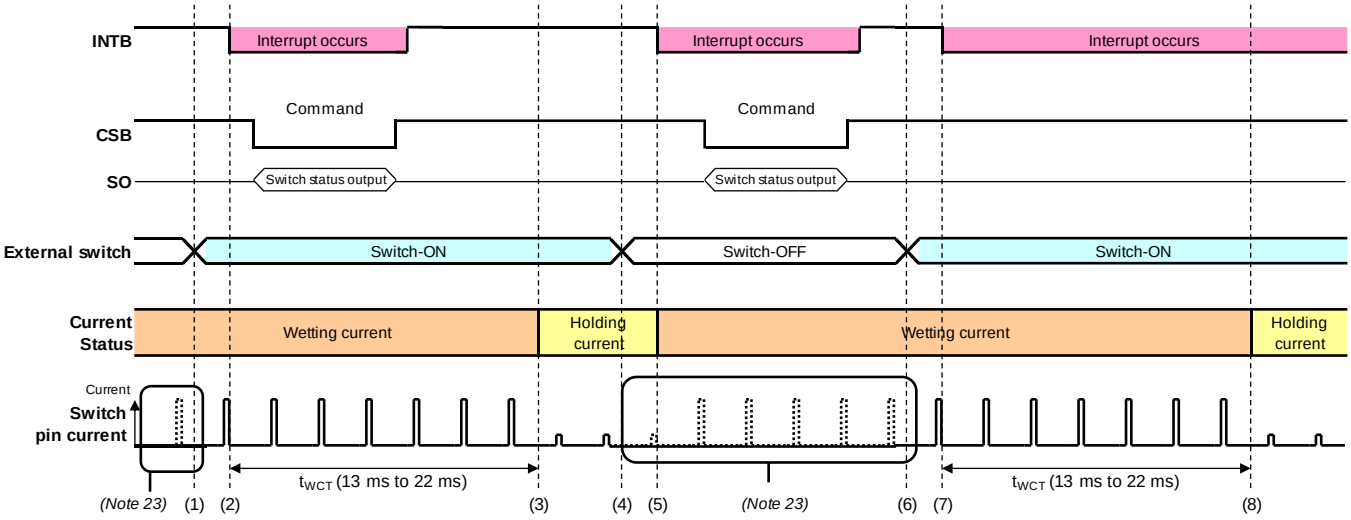


Figure 18. Wetting Current Timer (Intermittent Monitoring)

(1) Switch change occurs (OFF→ON).
(2) IC detects switch status change.
(3) When ON state of the switch continues for more than 13 ms to 22 ms, the holding current is output.
(4) Switch change occurs (ON→OFF).
(5) IC detects switch status change, switch current is switched from holding current to wetting current.
(6) Switch change occurs (OFF→ON).
(7) IC detects switch status change.
(8) When ON state of the switch continues for more than 13 ms to 22 ms, the holding current is output.

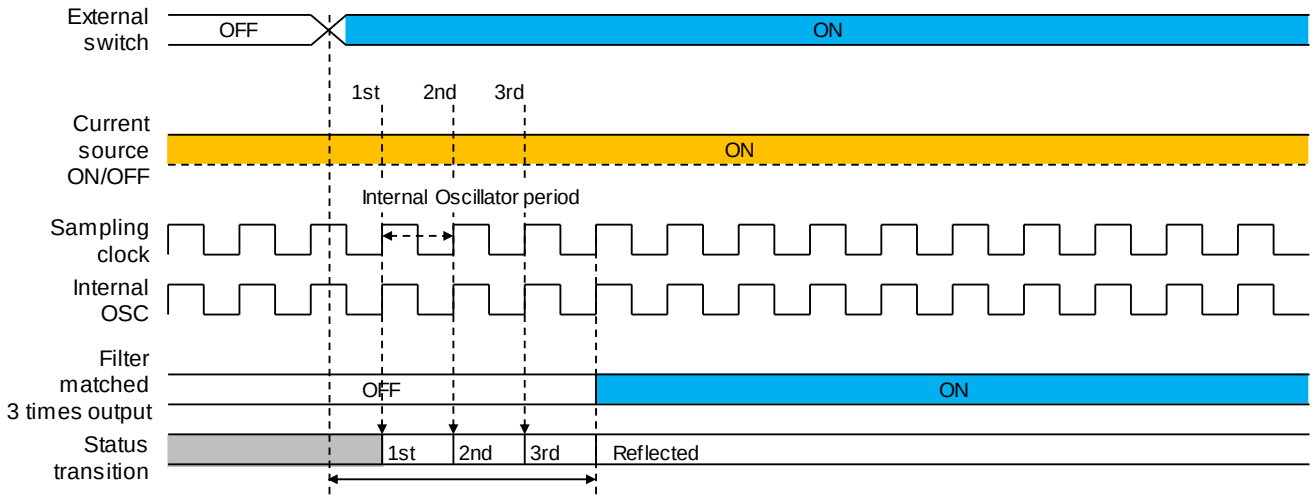
(Note 23) At switch-OFF situation. IC doesn't apply current.
This waveform indicates the timing of monitoring period.

Description of Functions - continued

9. n-Times Matched Filter

All switch inputs have built-in “1 time to 10 times matched filters”. This function can filter the ON/OFF switch status judgment made by the internal comparator. The filter function can be enabled for each power supply system. If the register has been updated during the counting of the filter, the counting is not reset.
If the monitoring method is continuous monitoring, the switch state is filtered n times (n: 1 to 10) multiplied by the period of the internal oscillator (32 kHz).
If the monitoring method is intermittent monitoring, the switch state is filtered n times (n: 1 to 10) multiplied by the monitoring period.

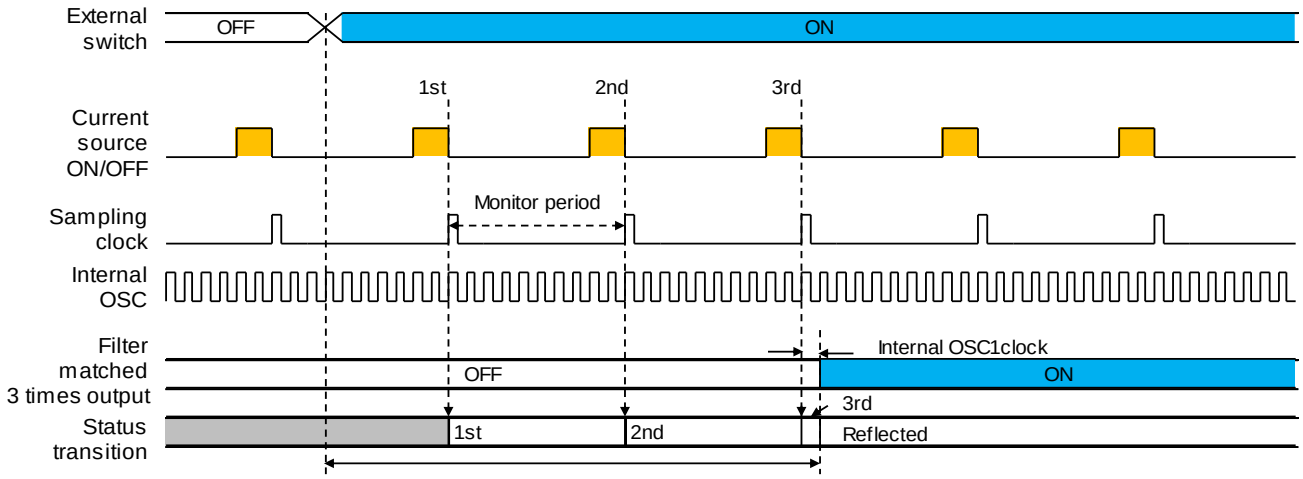
▪ **Set to full-time monitor :** Sampling period is internal oscillator period : 31.25 μs (Typ)



Time from Monitoring to End of Filtering:
{Monitoring Period x (Filter Number of Times -1) + Period of Internal Oscillator}
to {Monitoring Period x (Filter Number of Times) + Period of Internal Oscillator}

Figure 19. 3 Times Matched Filter Operation on Continuous Monitoring

▪ **Set to intermittent monitor :** Sampling monitor period is common with monitor period.



Time from Monitoring to End of Filtering:
{Monitoring Period x (Filter Number of Times -1) + Period of Internal Oscillator}
to {Monitoring Period x (Filter Number of Times) + Period of Internal Oscillator}

Figure 20. 3 Times Matched Filter Operation on Intermittent Monitoring

Description of Functions - continued

10. Digital Multiplexer Output

The status of the selected switch input is reflected by the DOUT pin. DOUT takes the output of the comparator on a timing determined by the monitoring method. When no switch is selected, the output of DOUT is “L”.
Only one switch pin at a time can be selected to be reflected by DOUT. The output signal can be inverted by setting.

11. Current Source Enable Signal Output

The Pull-up/Pull-down Current Source Enable Signal of the selected switch pin is output by the DOUT pin. It can be used to control external current source when the wetting current is generated by the external circuit. The polarity of this enable signal can be selected through command settings.

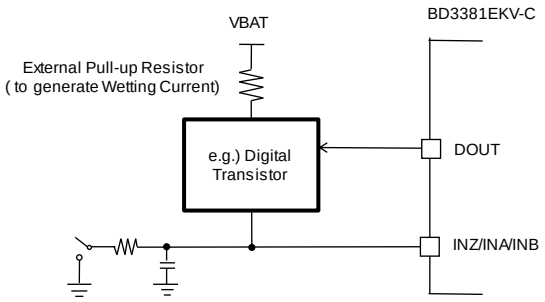


Figure 21. Example of Current Source Enable Signal Usage

12. Input Threshold Voltage of Switch Pin

The switch input threshold voltage is a fraction of the REF5 voltage. It can be set to 3.0 V or to 4.0 V.

·3.0 V Setting: $V_{TH3(HIGH)}$=VDDL*(Note 24)*x0.6 (6.0 V≤V_{VPUX}≤28.0 V)
·4.0 V Setting: $V_{TH4(HIGH)}$=VDDL*(Note 24)*x0.8 (7.0 V≤V_{VPUX}≤28.0 V)

Table 16. Relationship between the Switch Input Threshold Voltage and the SO Output

Input type	Source or Sink	Input Voltage	Comparator Output	SO Serial Interface Bit
INZ	Source	INZ<Threshold	0	H
	Source	INZ>Threshold	1	L
	Sink	INZ<Threshold	0	L
	Sink	INZ>Threshold	1	H
INA,INB	N/A	INA,INB<Threshold	0	H
	N/A	INA,INB>Threshold	1	L

(Note 24) As shown at Typical Application Circuit, short REF5 pin and VDDL pin externally. (Page 1, Figure 1)

13. Over-temperature Protection Circuit

When the junction temperature of the IC becomes higher than the thermal limit 160 °C (Typ), interrupt (INTB=“L”) occurs and the source/sink current through the switch pins is switched to 1 mA (Min). The MCU is notified by the SO over-temperature detection flag (them_flg) changing to “1” that an irregularity in temperature has occurred. When the junction temperature of the IC has fallen below 140 °C (Typ), interrupt is cleared on the next command transmission and the wetting current level returns to what was set on the registers.

Notice: The over-temperature detection value, 155 °C (Typ) to 175 °C (Typ), and the hysteresis temperature, 10 °C (Typ) to 30 °C (Typ), were not tested in shipment test. Also, the over-temperature protection circuit operates beyond the absolute maximum temperature ratings so the IC should not be used in a system where activation of the said protection function is expected.

14. Cyclic Redundancy Check (CRC)

The bit-7 to bit-0 of both the transmitted and received communication frame of the IC is the cyclic redundancy check (CRC), which is responsible for the detection of a data communication error.
If the IC received a CRC error, asserts interrupt (INTB=“L”) and error flag (“err_flg”) to SO output. SO output becomes “H” on the next communication to notify the MCU of the error. A command that has a CRC error is not a valid command.

The CRC generation polynomial is

$$X^8 + X^5 + X^4 + 1$$

Command Description

Each Command has two types of functions. One is to write a value to a register. The other is to read back the register value which was written by the write command. The function to be used is set by the bit-53 of each command. (The Null and Reset commands don't include the register value output command because they don't write in the registers.)
In the command descriptions below, the write command is for writing a value to a register and the read command is for reading back a register value.

1. Null Command

This command is a read only command that allows the user to monitor interrupt and switch status.

Table 17. Null Command (Read Only)

Command 0:"L", 1:"H", x: don't care		Register Address								Setting Data							
		55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
Null Command (Read Only)	IRC	0	1	0	0	0	0	0	0	x	x	x	x	x	x	x	x

Setting Data															
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Setting Data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

2. Interrupt Notification of Switch Change Setting Command

This command allows the user to configure interrupt sources for the INTB pin.
Specifically, this command allows the user to individually configure which switches trigger an interrupt on INTB by enabling or disabling the IEBn, IEAn, and IEZn setting bits shown below.
The SO output will return the switch status depending on the settings stored at the next CSB falling edge.

Table 18. Interrupt Notification of Switch Change Setting Command

Command 0:"L", 1:"H", x: don't care		Register Address								Setting Data							
		55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
Interrupt Notification of Switch Change Setting	IER	0	1	W/R	0	0	0	0	1	x	x	x	x	x	x	x	IEB10

Setting Data															
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
IEB9	IEB8	IEB7	IEB6	IEB5	IEB4	IEB3	IEB2	IEB1	IEB0	IEA9	IEA8	IEA7	IEA6	IEA5	IEA4

Setting Data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
IEA3	IEA2	IEA1	IEA0	IEZ11	IEZ10	IEZ9	IEZ8	IEZ7	IEZ6	IEZ5	IEZ4	IEZ3	IEZ2	IEZ1	IEZ0	CRC

IEB [10:0] [Default: 1] Interrupt Notification of Switch Status Change for INB System
0: Disabled 1: Enabled

IEA [9:0] [Default: 1] Interrupt Notification of Switch Status Change for INA System
0: Disabled 1: Enabled

IEZ [11:0] [Default: 1] Interrupt Notification of Switch Status Change for INZ System
0: Disabled 1: Enabled

W/R Register Write/Read Setting
0: Write 1: Read ("Setting data" is disabled)

Command Description - continued

3. Comparator Operation Control Command

This command allows the user to individually enable or disable the switch pin comparator for each switch input.
When a switch input's comparator is disabled through this register, both the corresponding settings available for that switch input within the "Interrupt Notification of Switch Change Setting Command" and the "Current Source Activation Command" are disabled.
When the comparator is active, the switch status output does not depend on whether the wetting current is set to source or sink. The switch status output is "1" when the switch is ON and "0" when the switch is OFF.
When the comparator is set to disabled, the switch status is undefined.

Table 19. Comparator Operation Control Command

Command 0:"L", 1:"H", x: don't care		Register Address								Setting Data							
		55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
Comparator Operation Control	CMR	0	1	W/R	0	0	0	1	0	x	x	x	x	x	x	x	CMB10

Setting Data															
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
CMB9	CMB8	CMB7	CMB6	CMB5	CMB4	CMB3	CMB2	CMB1	CMB0	CMA9	CMA8	CMA7	CMA6	CMA5	CMA4

Setting Data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
CMA3	CMA2	CMA1	CMA0	CMZ11	CMZ10	CMZ9	CMZ8	CMZ7	CMZ6	CMZ5	CMZ4	CMZ3	CMZ2	CMZ1	CMZ0	CRC

CMB [10:0] [Default: 1] Comparator Operation for INB System
0: Disabled 1: Enabled

CMA [9:0] [Default: 1] Comparator Operation for INA System
0: Disabled 1: Enabled

CMZ [11:0] [Default: 1] Comparator Operation for INZ System
0: Disabled 1: Enabled

W/R Register Write/Read Setting
0: Write 1: Read ("Setting data" is disabled)

4. Comparator Threshold Selection Command

This command allows the user to set the comparator threshold of the switch pins.
Switch detection threshold selection is available for each power supply system (See CTB, CTA, CTZ settings shown below).

Table 20. Comparator Threshold Selection Command

Command 0:"L", 1:"H", x: don't care		Register Address								Setting Data							
		55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
Comparator Threshold Selection	CTR	0	1	W/R	0	0	0	1	1	CTB	CTA	CTZ	x	x	x	x	x

Setting Data															
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Setting Data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

CTB [Default: 0] Comparator Threshold for INB System
0: 3.0 V 1: 4.0 V

CTA [Default: 0] Comparator Threshold for INA System
0: 3.0 V 1: 4.0 V

CTZ [Default: 0] Comparator Threshold for INZ System
0: 3.0 V 1: 4.0 V

W/R Register Write/Read Setting
0: Write 1: Read ("Setting data" is disabled)

Command Description - continued

5. INZ Current Source/Sink Selection Command

This command allows the user to select the current configuration, whether source (internal pull-up current source) or sink (internal pull-down current source), through the INZ input switch pins.

Table 21. INZ Current Source/Sink Selection Command

Command 0:"L", 1:"H", x: don't care		Register Address								Setting Data							
		55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
INZ Current Source/Sink Selection	PUDR	0	1	W/R	0	0	1	0	0	x	x	x	x	x	x	x	x

Setting Data															
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Setting Data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
x	x	x	x	PUD11	PUD10	PUD9	PUD8	PUD7	PUD6	PUD5	PUD4	PUD3	PUD2	PUD1	PUD0	CRC

PUD [11:0] [Default: 0] Source or Sink Selection for INZ System
0: Source (internal pull-up current source)
1: Sink (internal pull-down current source)

W/R Register Write/Read Setting
0: Write 1: Read ("Setting data" is disabled)

6. Current Source Activation Command

This command allows the user to enable or disable the wetting current sources at the switch input pins. The current sources can be set to ON or OFF per power supply system.
The output current level is determined by the "Holding Current / Wetting Current Value Setting Command" discussed in section 7 below.
If an external current source is used, the comparator should be enabled (see section 3 above) and the internal current source should be disabled using this register.

Table 22. Current Source Activation Command

Command 0:"L", 1:"H", x: don't care		Register Address								Setting Data							
		55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
Current Source Activation	CER	0	1	W/R	0	0	1	0	1	CEB	CEA	CEZ	x	x	x	x	x

Setting Data															
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Setting Data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

CEB [Default: 0] Current Sources of INB System
0: Disabled 1: Enabled

CEA [Default: 0] Current Sources of INA System
0: Disabled 1: Enabled

CEZ [Default: 0] Current Source of INZ System
0: Disabled 1: Enabled

W/R Register Write/Read Setting
0: Write 1: Read ("Setting data" is disabled)

Command Description - continued

7. Holding Current / Wetting Current Level Selection Command

This command allows the user to select the output level of each current source. This command also has arguments to set both the holding and the wetting current.
The holding current can be set to 1 mA, 3 mA, or 5 mA.
The wetting current can be set to OFF (“Hi-Z”), 1 mA, 3 mA, 5 mA (set to holding current), 10 mA, or 15 mA.
Unlike holding current, wetting current output levels can be set individually for each switch pin.

Table 23. Holding Current / Wetting Current Level Selection Command (LSB)

Command 0:“L”, 1:“H”, x: don't care		Register Address								Setting Data							
		55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
Holding Current / Wetting Current Level Selection (LSB)	LCR	0	1	W/R	0	0	1	1	0	CRH1	CRH0	x	x	x	x	x	LCB10

Setting Data															
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
LCB9	LCB8	LCB7	LCB6	LCB5	LCB4	LCB3	LCB2	LCB1	LCB0	LCA9	LCA8	LCA7	LCA6	LCA5	LCA4

Setting Data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
LCA3	LCA2	LCA1	LCA0	LCZ11	LCZ10	LCZ9	LCZ8	LCZ7	LCZ6	LCZ5	LCZ4	LCZ3	LCZ2	LCZ1	LCZ0	CRC

Table 24. Holding Current / Wetting Current Level Selection Command (MSB)

Command 0:“L”, 1:“H”, x: don't care		Register Address								Setting Data							
		55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
Holding Current / Wetting Current Level Selection (MSB)	MCR	0	1	W/R	0	0	1	1	1	x	x	x	x	x	x	x	MCB10

Setting Data															
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
MCB9	MCB8	MCB7	MCB6	MCB5	MCB4	MCB3	MCB2	MCB1	MCB0	MCA9	MCA8	MCA7	MCA6	MCA5	MCA4

Setting Data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
MCA3	MCA2	MCA1	MCA0	MCZ11	MCZ10	MCZ9	MCZ8	MCZ7	MCZ6	MCZ5	MCZ4	MCZ3	MCZ2	MCZ1	MCZ0	CRC

CRH [1:0] [Default: 00] — Holding Current Value
00: 1 mA 01: 3 mA
10: 5 mA 11: 1 mA

{MCB[10:0], LCB[10:0]} [Default: 01] — Wetting Current Value for INB System
00: Disabled(Hi-Z) 01: 1 mA/3 mA/5 mA(Holding Current Value)
10: 10 mA 11: 15 mA

{MCA[9:0], LCA[9:0]} [Default: 01] — Wetting Current Value for INA System
00: Disabled(Hi-Z) 01: 1m A/3 mA/5 mA(Holding Current Value)
10: 10 mA 11: 15 mA

{MCZ[11:0], LCZ[11:0]} [Default: 01] — Wetting Current Value for INZ System
00: Disabled(Hi-Z) 01: 1m A/3 mA/5 mA(Holding Current Value)
10: 10 mA 11: 15 mA

W/R — Register Write/Read Setting
0: Write 1: Read (“Setting data” is disabled)

Command Description - continued

8. Wetting Current Operation Control Command

This command allows the user to enable or disable the “wetting current timer”.
This “wetting current timer” counts 13 ms to 22 ms after the switch has been closed and the wetting current changes to holding current (1 mA/3 mA/5 mA). The timer is reset when the switch is turned off.
If the wetting current level is the same as the holding current level, the timer does not operate.
The wetting current timer can be enabled or disabled individually for each switch pin.

Table 25. Wetting Current Operation Control Command

Command 0:“L”, 1:“H”, x: don't care		Register Address								Setting Data							
		55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
Wetting Current Operation Control	WTR	0	1	W/R	0	1	0	0	0	x	x	x	x	x	x	x	WTB10

Setting Data															
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
WTB9	WTB8	WTB7	WTB6	WTB5	WTB4	WTB3	WTB2	WTB1	WTB0	WTA9	WTA8	WTA7	WTA6	WTA5	WTA4

Setting Data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
WTA3	WTA2	WTA1	WTA0	WTZ11	WTZ10	WTZ9	WTZ8	WTZ7	WTZ6	WTZ5	WTZ4	WTZ3	WTZ2	WTZ1	WTZ0	CRC

WTB [10:0] [Default: 0] Wetting Current Timer for INB System
0: Disabled 1: Enabled

WTA [9:0] [Default: 0] Wetting Current Timer for INA System
0: Disabled 1: Enabled

WTZ [11:0] [Default: 0] Wetting Current Timer for INZ System
0: Disabled 1: Enabled

W/R Register Write/Read Setting
0: Write 1: Read (“Setting data” is disabled)

Command Description - continued

9. n-Times Matched Filter Activation Control Command

This command allows the user to enable or disable the n-times matched LPF.
If this function is enabled, the switch output is updated only after the comparator output has been sampled “n” times (where n = 1 to 10) and if all sampled comparator outputs match.
This command allows for each switch pin groups to be enabled or disabled.

Table 26. n-Times Matched Filter Activation Control Command

Command 0:“L”, 1:“H”, x: don't care		Register Address								Setting Data							
		55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
n-Times Matched Filter Activation Control	DFR	0	1	W/R	0	1	0	0	1	DFB3	DFB2	DFB1	DFB0	DFA3	DFA2	DFA1	DFA0

Setting Data															
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
DFZ3	DFZ2	DFZ1	DFZ0	x	x	x	x	x	x	x	x	x	x	x	x

Setting Data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

DFB [3:0] [Default: 0000] n-Times Matched LPF Settings for INB System

0000	: Disabled (1 time)	0001	: 2 times
0010	: 3 times	0011	: 4 times
0100	: 5 times	0101	: 6 times
0110	: Disabled (1 time)	0111	: Disabled (1 time)
1000	: Disabled (1 time)	1001	: 7 times
1010	: 8 times	1011	: 9 times
1100	: 10 times	1101	: Disabled (1 time)
1110	: Disabled (1 time)	1111	: Disabled (1 time)

DFA [3:0] [Default: 0000] n-Times Matched LPF Settings for INA System

0000	: Disabled (1 time)	0001	: 2 times
0010	: 3 times	0011	: 4 times
0100	: 5 times	0101	: 6 times
0110	: Disabled (1 time)	0111	: Disabled (1 time)
1000	: Disabled (1 time)	1001	: 7 times
1010	: 8 times	1011	: 9 times
1100	: 10 times	1101	: Disabled (1 time)
1110	: Disabled (1 time)	1111	: Disabled (1 time)

DFZ [3:0] [Default: 0000] n-Times Matched LPF Settings for INZ System

0000	: Disabled (1 time)	0001	: 2 times
0010	: 3 times	0011	: 4 times
0100	: 5 times	0101	: 6 times
0110	: Disabled (1 time)	0111	: Disabled (1 time)
1000	: Disabled (1 time)	1001	: 7 times
1010	: 8 times	1011	: 9 times
1100	: 10 times	1101	: Disabled (1 time)
1110	: Disabled (1 time)	1111	: Disabled (1 time)

W/R Register Write/Read Setting
0: Write 1: Read (“Setting data” is disabled)

Command Description - continued

10. DOUT Setting Command

This command allows the user to configure how the DOUT pin will function. There are two available functions for the DOUT pin. One is to output the result of the digital multiplexer, and the other is to output the state of a current enable signal.

For the first function, the DOUT Setting Command can be used to enable or disable the digital multiplexer. If the digital multiplexer is enabled, the result of the selected switch pin's comparator is output to the DOUT pin at a timing that depends on the monitoring method used. The switch pin selection is made through the CSL0 to CSL5 bits of the command. Also, the output signal can be inverted through the POL bit.

For the second function, DOUT can be configured so that it will indicate whether the internal pull-up/pull-down current is enabled or disabled for the selected switch input. The POL bit can also be used to invert the output for this function. If the Positive Polarity Setting is chosen, "H" output means the signal is enabled, and "L" output means the signal is disabled. If the Negative Polarity Setting is chosen, the result is the opposite.

Table 27. DOUT Setting Command

Command 0:"L", 1:"H", x: don't care		Register Address								Setting Data							
		55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
DOUT Setting	DOT	0	1	W/R	0	1	0	1	0	CSL5	CSL4	CSL3	CSL2	CSL1	CSL0	x	x

Setting Data															
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
FSL	x	x	x	POL	x	x	x	x	x	x	x	x	x	x	x

Setting Data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

Table 28. DOUT Channel Selection

bit-47 to bit-42	Selected Channel
000000	Disabled (Output is "L")
000001	INZ0
000010	INZ1
000011	INZ2
000100	INZ3
000101	INZ4
000110	INZ5
000111	INZ6
001000	INZ7
001001	INZ8
001010	INZ9
001011	INZ10
001100	INZ11
001101	INA0
001110	INA1
001111	INA2
010000	INA3
010001	INA4

bit-47 to bit-42	Selected Channel
010010	INA5
010011	INA6
010100	INA7
010101	INA8
010110	INA9
010111	INB0
011000	INB1
011001	INB2
011010	INB3
011011	INB4
011100	INB5
011101	INB6
011110	INB7
011111	INB8
100000	INB9
100001	INB10
100010 to 111111	Disabled (Output is "L")

Command Description - continued

CSL [5:0] [Default:000000]	Switch Channel Selection Setting 000000 : Disable (DOUT is “L”) 000001 to 001100 : INZ Channel Selection 001101 to 010110 : INA Channel Selection 010111 to 100001 : INB Channel Selection 100010 to 111111 : Disable (DOUT is “L”)
FSL [Default:0]	DOUT Function Setting 0: Digital Multiplexer Signal Output 1: Current Source Enable Signal Output
POL [Default:0]	Polarity Setting 0: Positive 1: Negative
W/R	Register Write/Read Setting 0: Write 1: Read (“Setting data” is disabled)

Command Description - continued

11. Normal Mode Setting Command

This command allows the user to set the monitoring period, strobe time, and monitoring method of normal mode.
The normal mode is set after power on reset or by “Monitor Mode Transition Command”.
The monitoring period can be set individually per power supply system but the strobe time is common to all switch pins.
The monitoring method can be set continuous monitoring, intermittent monitoring at the same time, sequential monitoring by power supply system and sequential monitoring of all switch pins.

The monitoring period of the normal mode and strobe time setting have some restrictions as follows.
· 1 ms monitoring period with sequential monitoring by power supply system is prohibited.
· 1 ms monitoring period with sequential monitoring of all switch pins is prohibited.
· At 2.5 ms monitoring period setting with sequential monitoring by power supply system, only 93.75 µs and 125 µs strobe time are allowed. Other strobe time settings are prohibited.
· At 2.5 ms monitoring period setting and sequential monitoring of all switch pins, only 93.75 µs and 125 µs strobe time are allowed. Other strobe time settings are prohibited.

·Continuous Monitoring:
IC monitors switch status continuously.
Refer to the “[Basic Operation 1] Detection of switch status change (Continuous Monitoring)” section for additional details.
·Intermittent Monitoring at the Same Time:
IC monitors switch status per power supply system at the same time.
Refer to the “[Extension Function1: Intermittent Monitoring at the Same Time (with Current Slope)]” section for additional details.
·Sequential Monitoring by Power Supply System:
IC monitors switch status per switch by turns on power supply system.
Refer to the “[Extension Function 2: Sequential Monitoring by Power Supply System]” section for additional details.
·Sequential Monitoring of All Switch Pins:
IC monitors switch status per switch by turns.
Refer to the “[Extension Function 3: Sequential Monitoring of All Switch Pins]” section for additional details.

If both sequential and continuous monitoring are enabled at the same time, continuous monitoring will be the one implemented.
If both sequential monitoring by power supply system and sequential monitoring of all switch pins are enabled at the same time, sequential monitoring of all switch pins will be the one implemented.

Table 29. Normal Mode Setting Command

Command 0:“L”, 1:“H”, x: don't care		Register Address								Setting Data							
		55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
Normal Mode Setting	FMR	0	1	W/R	0	1	0	1	1	FSQ	FSQB	FSQA	FSQZ	FITB3	FITB2	FITB1	FITB0

Setting Data															
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
FITA3	FITA2	FITA1	FITA0	FITZ3	FITZ2	FITZ1	FITZ0	SVW1	SVW0	x	x	x	x	x	x

Setting Data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

FSQ [Default: 0] Sequential Monitoring of All Switch Terminals
0: Disabled 1: Enabled

FSQB [Default: 0] Sequential Monitoring by Power Supply System for INB System
0: Disabled 1: Enabled

FSQA [Default: 0] Sequential Monitoring by Power Supply System for INA System
0: Disabled 1: Enabled

FSQZ [Default: 0] Sequential Monitoring by Power Supply System for INZ System
0: Disabled 1: Enabled

FIT*[3:0] (*: B, A, Z) [Default: 0000] Monitoring Period for Normal Mode
0000: Continuous Monitoring 0001: 2.5 ms
0010: 5 ms 0011: 10 ms
0100: 20 ms 0101: 30 ms
0110: 40 ms 0111: 50 ms
1000:100 ms 1001: 1 ms
1010 to 1111: Setting prohibited

Command Description - continued

SVW [1:0] [Default: 01]	Strobe Time 00: 93.75 µs 01: 125 µs 10: 187.5 µs 11: 250 µs
W/R	Register Write/Read Setting 0: Write 1: Read (“Setting data” is disabled)

Command Description - continued

12. Sleep Mode Setting Command

This command allows the user to set the monitoring period and monitoring method of sleep mode.
The sleep mode is set by “Monitor Mode Transition Command”.
The strobe time of sleep mode is the same as the normal mode.
About the monitoring period and monitoring method, refer to the “Normal Mode Setting Command” discussed in section 11 below.

The monitoring period of the sleep mode and strobe time setting have some restrictions as follows.

- 1ms monitoring period with sequential monitoring by power supply system is prohibited.
- 1ms monitoring period with sequential monitoring of all switch pins is prohibited.
- At 2.5 ms monitoring period setting with sequential monitoring by power supply system, only 93.75 µs and 125 µs strobe time are allowed. Other strobe time settings are prohibited.
- At 2.5 ms monitoring period setting and sequential monitoring of all switch pins, only 93.75 µs and 125 µs strobe time are allowed. Other strobe time settings are prohibited.

Table 30. Sleep Mode Setting Command

Command 0:“L”, 1:“H”, x: don't care		Register Address								Setting Data							
		55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
Sleep Mode Setting	SMR	0	1	W/R	0	1	1	0	0	SSQ	SSQB	SSQA	SSQZ	SITB3	SITB2	SITB1	SITB0

Setting Data																	
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24		
SITA3	SITA2	SITA1	SITA0	SITZ3	SITZ2	SITZ1	SITZ0	x	x	x	x	x	x	x	x		

Setting Data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

SSQ [Default: 0] Sequential Monitoring of All Switch Terminals
0: Disabled 1: Enabled

SSQB [Default: 0] Sequential Monitoring by Power Supply System for INB System
0: Disabled 1: Enabled

SSQA [Default: 0] Sequential Monitoring by Power Supply System for INA System
0: Disabled 1: Enabled

SSQZ [Default: 0] Sequential Monitoring by Power Supply System for INZ System
0: Disabled 1: Enable

SIT*[3:0] (*: B, A, Z) [Default: 0111] Monitoring Period for Sleep Mode
0000: Continuous Monitoring 0001: 2.5 ms
0010: 5 ms 0011: 10 ms
0100: 20 ms 0101: 30 ms
0110: 40 ms 0111: 50 ms
1000:100 ms 1001: 1 ms
1010 to 1111: Setting prohibited

W/R Register Write/Read Setting
0: Write 1: Read (“Setting data” is disabled)

Command Description - continued

13. Detection Edge Selection Command

This command allows the user to configure interrupt trigger of switches for the INTB pin.
The interrupt trigger can be set to only the falling edge(Note 25) or both the rising and falling edges of the switch input voltage per power supply system.
If only the falling edge is selected, the INTB pin not changes by the rising edges of switch input voltage.

(Note 25) If the INZ current "Source Setting" is enabled, the falling edge of the switch input pin is seen when the external switch is turned on. If the INZ current "Sink Setting" is enabled, the falling edge is seen when the external switch is turned off.

Table 31. Detection Edge Selection Command

Command 0:"L", 1:"H", x: don't care		Register Address								Setting Data							
		55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
Detection Edge Selection	ISR	0	1	W/R	0	1	1	0	1	ISB	ISA	ISZ	x	x	x	x	x

Setting Data															
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Setting Data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

ISB [Default: 1] Switch Edge where Interrupt Occurs for INB System
0: Only Falling Edge 1: Both Edges

ISA [Default: 1] Switch Edge where Interrupt Occurs for INA System
0: Only Falling Edge 1: Both Edges

ISZ [Default: 1] Switch Edge where Interrupt Occurs for INZ System
0: Only Falling Edge 1: Both Edges

W/R Register Write/Read Setting
0: Write 1: Read ("Setting data" is disabled)

14. Automatic Mode Transition Command

This command allows the user to configure the mode to automatically change from sleep mode to normal mode by a change in switch status.
If the automatic transition is enabled, the monitoring period and monitoring method are changed to normal mode settings when it detects a change in switch status on sleep.
Refer to the "[Basic Operation 4] Sleep Mode Operation Automatic Transition to Normal Mode" section for additional details on how sleep mode operations works for this IC.

Table 32. Automatic Mode Transition Command

Command 0:"L", 1:"H", x: don't care		Register Address								Setting Data							
		55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
Automatic Mode Transition	MIR	0	1	W/R	0	1	1	1	0	MR_IER	x	x	x	x	x	x	x

Setting Data															
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Setting Data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

MR_IER [Default: 1] Automatic Mode Transition
0: Disabled 1: Enabled (Automatically mode transition, depend on the switch status changing)

W/R Register Write/Read Setting
0: Write 1: Read ("Setting data" is disabled)

Command Description - continued

15. Monitor Mode Transition Command

This command allows the user to change the mode of operation between normal and sleep.
Refer to the “[Basic Operation 3] Sleep Mode Operation (Manual Transition)” section for additional details on how sleep mode operations works for this IC.

Table 33. Monitor Mode Transition Command

Command 0:“L”, 1:“H”, x: don't care		Register Address								Setting Data							
		55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
Monitor Mode Transition	MDR	0	1	W/R	0	1	1	1	1	MDC	x	x	x	x	x	x	x

Setting Data															
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Setting Data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

MDC [Default: 0] Monitoring Mode
0: Normal Mode 1: Sleep Mode

W/R Register Write/Read Setting
0: Write 1: Read (“Setting data” is disabled)

Command Description - continued

16. Reset Command

This command allows the user to reset the registers to their initial settings. After the reset command has been sent, the physical interrupt pin goes to low (INTB="L").

Table 34. Reset Command

Command 0:"L", 1:"H", x: don't care		Register Address								Setting Data							
		55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
Reset	RST	0	1	0	1	1	1	1	1	x	x	x	x	x	x	x	x

Setting Data															
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Setting Data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

17. TEST Command

This command is used to enter test mode, which is only possible when the TEST pin is "H".
Short TEST pin to ground and don't enter to test mode.

Table 35. TEST Command

Command 0:"L", 1:"H", x: don't care		Register Address								Setting Data							
		55	54	53	52	51	50	49	48	47	46	45	44	43	42	41	40
TEST	TSR	0	1	1	1	1	0	0	1	TSS7	TSS6	TSS5	TSS4	TSS3	TSS2	TSS1	TSS0

Setting Data															
39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

Setting Data																CRC
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7 to 0
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	CRC

Command Description - continued

18. Register Map

Table 36. Register Map (1/2)

Register Name	Symbol	Register Address	Setting Data Name (def*: Default Setting)																																							CRC
		55:48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7:0
Null Command	IRC	0x40																																									CRC
Interrupt Notification of Switch Change Setting Command [Default: Enabled]	IER	0x41								IEB10 (def:1)	IEB9 (def:1)	IEB8 (def:1)	IEB7 (def:1)	IEB6 (def:1)	IEB5 (def:1)	IEB4 (def:1)	IEB3 (def:1)	IEB2 (def:1)	IEB1 (def:1)	IEB0 (def:1)	IEA9 (def:1)	IEA8 (def:1)	IEA7 (def:1)	IEA6 (def:1)	IEA5 (def:1)	IEA4 (def:1)	IEA3 (def:1)	IEA2 (def:1)	IEA1 (def:1)	IEA0 (def:1)	IEZ11 (def:1)	IEZ10 (def:1)	IEZ9 (def:1)	IEZ8 (def:1)	IEZ7 (def:1)	IEZ6 (def:1)	IEZ5 (def:1)	IEZ4 (def:1)	IEZ3 (def:1)	IEZ2 (def:1)	IEZ1 (def:1)	IEZ0 (def:1)	CRC
Comparator Operation Control Command [Default: Enabled]	CMR	0x42								CMB10 (def:1)	CMB9 (def:1)	CMB8 (def:1)	CMB7 (def:1)	CMB6 (def:1)	CMB5 (def:1)	CMB4 (def:1)	CMB3 (def:1)	CMB2 (def:1)	CMB1 (def:1)	CMB0 (def:1)	CMA9 (def:1)	CMA8 (def:1)	CMA7 (def:1)	CMA6 (def:1)	CMA5 (def:1)	CMA4 (def:1)	CMA3 (def:1)	CMA2 (def:1)	CMA1 (def:1)	CMA0 (def:1)	CMZ11 (def:1)	CMZ10 (def:1)	CMZ9 (def:1)	CMZ8 (def:1)	CMZ7 (def:1)	CMZ6 (def:1)	CMZ5 (def:1)	CMZ4 (def:1)	CMZ3 (def:1)	CMZ2 (def:1)	CMZ1 (def:1)	CMZ0 (def:1)	CRC
Comparator Threshold Selection Command [Default: 3.0 V]	CTR	0x43	CTB (def:0)	CTA (def:0)	CTZ (def:0)																																						CRC
INZ Current Source/Sink Selection Command [Default: Source]	PUDR	0x44																													PUD11 (def:0)	PUD10 (def:0)	PUD9 (def:0)	PUD8 (def:0)	PUD7 (def:0)	PUD6 (def:0)	PUD5 (def:0)	PUD4 (def:0)	PUD3 (def:0)	PUD2 (def:0)	PUD1 (def:0)	PUD0 (def:0)	CRC
Current Source Activation Command [Default: OFF (Disabled)]	CER	0x45	CEB (def:0)	CEA (def:0)	CEZ (def:0)																																						CRC
Holding Current / Wetting Current Level Selection Command (LSB) [Default: Wetting current=1 mA (Holding current)]	LCR	0x46	CRH1 (def:0)	CRH0 (def:0)						LCB10 (def:1)	LCB9 (def:1)	LCB8 (def:1)	LCB7 (def:1)	LCB6 (def:1)	LCB5 (def:1)	LCB4 (def:1)	LCB3 (def:1)	LCB2 (def:1)	LCB1 (def:1)	LCB0 (def:1)	LCA9 (def:1)	LCA8 (def:1)	LCA7 (def:1)	LCA6 (def:1)	LCA5 (def:1)	LCA4 (def:1)	LCA3 (def:1)	LCA2 (def:1)	LCA1 (def:1)	LCA0 (def:1)	LCZ11 (def:1)	LCZ10 (def:1)	LCZ9 (def:1)	LCZ8 (def:1)	LCZ7 (def:1)	LCZ6 (def:1)	LCZ5 (def:1)	LCZ4 (def:1)	LCZ3 (def:1)	LCZ2 (def:1)	LCZ1 (def:1)	LCZ0 (def:1)	CRC
Holding Current / Wetting Current Level Selection Command (MSB) [Default: Wetting current =1 mA (Holding current)]	MCR	0x47								MCB10 (def:0)	MCB9 (def:0)	MCB8 (def:0)	MCB7 (def:0)	MCB6 (def:0)	MCB5 (def:0)	MCB4 (def:0)	MCB3 (def:0)	MCB2 (def:0)	MCB1 (def:0)	MCB0 (def:0)	MCA9 (def:0)	MCA8 (def:0)	MCA7 (def:0)	MCA6 (def:0)	MCA5 (def:0)	MCA4 (def:0)	MCA3 (def:0)	MCA2 (def:0)	MCA1 (def:0)	MCA0 (def:0)	MCZ11 (def:0)	MCZ10 (def:0)	MCZ9 (def:0)	MCZ8 (def:0)	MCZ7 (def:0)	MCZ6 (def:0)	MCZ5 (def:0)	MCZ4 (def:0)	MCZ3 (def:0)	MCZ2 (def:0)	MCZ1 (def:0)	MCZ0 (def:0)	CRC
Wetting Current Operation Control Command [Default: Disabled]	WTR	0x48								WTB10 (def:0)	WTB9 (def:0)	WTB8 (def:0)	WTB7 (def:0)	WTB6 (def:0)	WTB5 (def:0)	WTB4 (def:0)	WTB3 (def:0)	WTB2 (def:0)	WTB1 (def:0)	WTB0 (def:0)	WTA9 (def:0)	WTA8 (def:0)	WTA7 (def:0)	WTA6 (def:0)	WTA5 (def:0)	WTA4 (def:0)	WTA3 (def:0)	WTA2 (def:0)	WTA1 (def:0)	WTA0 (def:0)	WTZ11 (def:0)	WTZ10 (def:0)	WTZ9 (def:0)	WTZ8 (def:0)	WTZ7 (def:0)	WTZ6 (def:0)	WTZ5 (def:0)	WTZ4 (def:0)	WTZ3 (def:0)	WTZ2 (def:0)	WTZ1 (def:0)	WTZ0 (def:0)	CRC
n-Times Matched Filter Activation Control Command [Default: Disabled]	DFR	0x49	DFB3 (def:0)	DFB2 (def:0)	DFB1 (def:0)	DFB0 (def:0)	DFA3 (def:0)	DFA2 (def:0)	DFA1 (def:0)	DFA0 (def:0)	DFZ3 (def:0)	DFZ2 (def:0)	DFZ1 (def:0)	DFZ0 (def:0)																													CRC
DOUT Setting Command [Default: Disabled]	DOT	0x4A	CSL5 (def:0)	CSL4 (def:0)	CSL3 (def:0)	CSL2 (def:0)	CSL1 (def:0)	CSL0 (def:0)			FSL (def:0)				POL (def:0)																												CRC
Normal Mode Setting Command [Default: Full-time monitor,Strobe time:125 us,Sequential monitor is disabled]	FMR	0x4B	FSQ (def:0)	FSQB (def:0)	FSQA (def:0)	FSQZ (def:0)	FITB3 (def:0)	FITB2 (def:0)	FITB1 (def:0)	FITB0 (def:0)	FITA3 (def:0)	FITA2 (def:0)	FITA1 (def:0)	FITA0 (def:0)	FITZ3 (def:0)	FITZ2 (def:0)	FITZ1 (def:0)	FITZ0 (def:0)	SVW1 (def:0)	SVW0 (def:1)																							CRC
Sleep Mode Setting Command [Default: Monitor period:50 ms,Sequential monitor is disabled]	SMR	0x4C	SSQ (def:0)	SSQB (def:0)	SSQA (def:0)	SSQZ (def:0)	SITB3 (def:0)	SITB2 (def:1)	SITB1 (def:1)	SITB0 (def:1)	SITA3 (def:0)	SITA2 (def:1)	SITA1 (def:1)	SITA0 (def:1)	SITZ3 (def:0)	SITZ2 (def:1)	SITZ1 (def:1)	SITZ0 (def:1)																									CRC
Detection Edge Selection Command [Default: Both edges]	ISR	0x4D	ISB (def:1)	ISA (def:1)	ISZ (def:1)																																						CRC
Automatic Mode Transition Command [Default: Automatic transition is enabled]	MIR	0x4E	MR_IER (def:1)																																								CRC
Monitor Mode Ttransition Command [Default: Normal mode]	MDR	0x4F	MDC (def:0)																																								CRC

Command Description - continued

Table 37. Register Map (2/2)

Register Name	Symbol	Register Address	Setting Data Name (def*: Default Setting)																																		CRC
		55:48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7:0
Reset Command	RST	0x5F																																									CRC
Interrupt Notification of Switch Change Setting Command Read	RIER	0x61																																									CRC
Comparator Operation Control Command Read	RCMR	0x62																																									CRC
Comparator Threshold Selection Command Read	RCTR	0x63																																									CRC
INZ Current Source/Sink Selection Command Read	RPUDR	0x64																																									CRC
Current Source Activation Command Read	RCER	0x65																																									CRC
Holding Current / Wetting Current Level Selection Command (LSB) Read	RLCR	0x66																																									CRC
Holding Current / Wetting Current Level Selection Command (MSB) Read	RMCR	0x67																																									CRC
Wetting Current Operation Control Command Read	RWTR	0x68																																									CRC
n-Times Matched Filter Activation Control Command Read	RDFR	0x69																																									CRC
DOUT Setting Command Read	RDOT	0x6A																																									CRC
Normal Mode Setting Command Read	RFMR	0x6B																																									CRC
Sleep Mode Setting Command Read	RSMR	0x6C																																										CRC
Detection Edge Selection Command Read	RISR	0x6D																																									CRC
Automatic Mode Transition Command Read	RMIR	0x6E																																										CRC
Monitor Mode Ttransition Command Read	RMDR	0x6F																																									CRC
TEST Command [Default: Disabled]	TSR	0x79	TSS7 (def:0)	TSS6 (def:0)	TSS5 (def:0)	TSS4 (def:0)	TSS3 (def:0)	TSS2 (def:0)	TSS1 (def:0)	TSS0 (def:0)																																CRC

Command Description - continued

Table 38. Register Map (SO Bit Alignment)

Register Name	Symbol	-	Read Data Name																																		CRC
		55:48	47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7:0
Interrupt Notification of Switch Change Setting Command Read	RIER	"100", Interrupt Factor	0	0	0	0	0	0	0	IEB10 (def:1)	IEB9 (def:1)	IEB8 (def:1)	IEB7 (def:1)	IEB6 (def:1)	IEB5 (def:1)	IEB4 (def:1)	IEB3 (def:1)	IEB2 (def:1)	IEB1 (def:1)	IEB0 (def:1)	IEA9 (def:1)	IEA8 (def:1)	IEA7 (def:1)	IEA6 (def:1)	IEA5 (def:1)	IEA4 (def:1)	IEA3 (def:1)	IEA2 (def:1)	IEA1 (def:1)	IEA0 (def:1)	IEZ11 (def:1)	IEZ10 (def:1)	IEZ9 (def:1)	IEZ8 (def:1)	IEZ7 (def:1)	IEZ6 (def:1)	IEZ5 (def:1)	IEZ4 (def:1)	IEZ3 (def:1)	IEZ2 (def:1)	IEZ1 (def:1)	IEZ0 (def:1)	CRC
Comparator Operation Control Command Read	RCMR	"100", Interrupt Factor	0	0	0	0	0	0	0	CMB10 (def:1)	CMB9 (def:1)	CMB8 (def:1)	CMB7 (def:1)	CMB6 (def:1)	CMB5 (def:1)	CMB4 (def:1)	CMB3 (def:1)	CMB2 (def:1)	CMB1 (def:1)	CMB0 (def:1)	CMA9 (def:1)	CMA8 (def:1)	CMA7 (def:1)	CMA6 (def:1)	CMA5 (def:1)	CMA4 (def:1)	CMA3 (def:1)	CMA2 (def:1)	CMA1 (def:1)	CMA0 (def:1)	CMZ11 (def:1)	CMZ10 (def:1)	CMZ9 (def:1)	CMZ8 (def:1)	CMZ7 (def:1)	CMZ6 (def:1)	CMZ5 (def:1)	CMZ4 (def:1)	CMZ3 (def:1)	CMZ2 (def:1)	CMZ1 (def:1)	CMZ0 (def:1)	CRC
Comparator Threshold Selection Command Read	RCTR	"100", Interrupt Factor	CTB (def:0)	CTA (def:0)	CTZ (def:0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC
INZ Current Source/Sink Selection Command Read	RPUDR	"100", Interrupt Factor	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	PUD11 (def:0)	PUD10 (def:0)	PUD9 (def:0)	PUD8 (def:0)	PUD7 (def:0)	PUD6 (def:0)	PUD5 (def:0)	PUD4 (def:0)	PUD3 (def:0)	PUD2 (def:0)	PUD1 (def:0)	PUD0 (def:0)	CRC
Wetting Current Operation Control Command Read	RCER	"100", Interrupt Factor	CEB (def:0)	CEA (def:0)	CEZ (def:0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC
Holding Current / Wetting Current Level Selection Command (LSB) Read	RLCR	"100", Interrupt Factor	CRH1 (def:0)	CRH0 (def:0)	0	0	0	0	0	LCB10 (def:1)	LCB9 (def:1)	LCB8 (def:1)	LCB7 (def:1)	LCB6 (def:1)	LCB5 (def:1)	LCB4 (def:1)	LCB3 (def:1)	LCB2 (def:1)	LCB1 (def:1)	LCB0 (def:1)	LCA9 (def:1)	LCA8 (def:1)	LCA7 (def:1)	LCA6 (def:1)	LCA5 (def:1)	LCA4 (def:1)	LCA3 (def:1)	LCA2 (def:1)	LCA1 (def:1)	LCA0 (def:1)	LCZ11 (def:1)	LCZ10 (def:1)	LCZ9 (def:1)	LCZ8 (def:1)	LCZ7 (def:1)	LCZ6 (def:1)	LCZ5 (def:1)	LCZ4 (def:1)	LCZ3 (def:1)	LCZ2 (def:1)	LCZ1 (def:1)	LCZ0 (def:1)	CRC
Holding Current / Wetting Current Level Selection Command (MSB) Read	RMCR	"100", Interrupt Factor	0	0	0	0	0	0	0	MCB10 (def:0)	MCB9 (def:0)	MCB8 (def:0)	MCB7 (def:0)	MCB6 (def:0)	MCB5 (def:0)	MCB4 (def:0)	MCB3 (def:0)	MCB2 (def:0)	MCB1 (def:0)	MCB0 (def:0)	MCA9 (def:0)	MCA8 (def:0)	MCA7 (def:0)	MCA6 (def:0)	MCA5 (def:0)	MCA4 (def:0)	MCA3 (def:0)	MCA2 (def:0)	MCA1 (def:0)	MCA0 (def:0)	MCZ11 (def:0)	MCZ10 (def:0)	MCZ9 (def:0)	MCZ8 (def:0)	MCZ7 (def:0)	MCZ6 (def:0)	MCZ5 (def:0)	MCZ4 (def:0)	MCZ3 (def:0)	MCZ2 (def:0)	MCZ1 (def:0)	MCZ0 (def:0)	CRC
Wetting Current Operation Control Command Read	RWTR	"100", Interrupt Factor	0	0	0	0	0	0	0	WTB10 (def:0)	WTB9 (def:0)	WTB8 (def:0)	WTB7 (def:0)	WTB6 (def:0)	WTB5 (def:0)	WTB4 (def:0)	WTB3 (def:0)	WTB2 (def:0)	WTB1 (def:0)	WTB0 (def:0)	WTA9 (def:0)	WTA8 (def:0)	WTA7 (def:0)	WTA6 (def:0)	WTA5 (def:0)	WTA4 (def:0)	WTA3 (def:0)	WTA2 (def:0)	WTA1 (def:0)	WTA0 (def:0)	WTZ11 (def:0)	WTZ10 (def:0)	WTZ9 (def:0)	WTZ8 (def:0)	WTZ7 (def:0)	WTZ6 (def:0)	WTZ5 (def:0)	WTZ4 (def:0)	WTZ3 (def:0)	WTZ2 (def:0)	WTZ1 (def:0)	WTZ0 (def:0)	CRC
n-Times Matched Filter Activation Control Command Read	RDFR	"100", Interrupt Factor	DFB3 (def:0)	DFB2 (def:0)	DFB1 (def:0)	DFB0 (def:0)	DFA3 (def:0)	DFA2 (def:0)	DFA1 (def:0)	DFA0 (def:0)	DFZ3 (def:0)	DFZ2 (def:0)	DFZ1 (def:0)	DFZ0 (def:0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC
DOUT Setting Command Read	RDOT	"100", Interrupt Factor	CSL5 (def:0)	CSL4 (def:0)	CSL3 (def:0)	CSL2 (def:0)	CSL1 (def:0)	CSL0 (def:0)	0	0	FSL (def:0)	0	0	0	POL (def:0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC
Normal Mode Setting Command Read	RFMR	"100", Interrupt Factor	FSQ (def:0)	FSQB (def:0)	FSQA (def:0)	FSQZ (def:0)	FITB3 (def:0)	FITB2 (def:1)	FITB1 (def:1)	FITB0 (def:1)	FITA3 (def:0)	FITA2 (def:0)	FITA1 (def:1)	FITA0 (def:1)	FITZ3 (def:0)	FITZ2 (def:0)	FITZ1 (def:1)	FITZ0 (def:1)	SVW1 (def:0)	SVW0 (def:1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC
Sleep Mode Setting Command Read	RSMR	"100", Interrupt Factor	SSQ (def:0)	SSQB (def:0)	SSQA (def:0)	SSQZ (def:0)	SITB3 (def:0)	SITB2 (def:1)	SITB1 (def:1)	SITB0 (def:1)	SITA3 (def:0)	SITA2 (def:1)	SITA1 (def:1)	SITA0 (def:1)	SITZ3 (def:0)	SITZ2 (def:1)	SITZ1 (def:1)	SITZ0 (def:1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC
Detection Edge Selection Command Read	RISR	"100", Interrupt Factor	ISB (def:1)	ISA (def:1)	ISZ (def:1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC
Automatic Mode Transition Command Read	RMIR	"100", Interrupt Factor	MR_IER (def:1)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC
Monitor Mode Ttransition Command Read	RMDR	"100", Interrupt Factor	MDC (def:0)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	CRC

Typical Performance Curves

Unless otherwise specified, VPUA=VPUB=13 V, VDDI=5 V, VDDL=REF5.
Series products (BD3380MUV-M/BD3381EKV-C) use the same data.

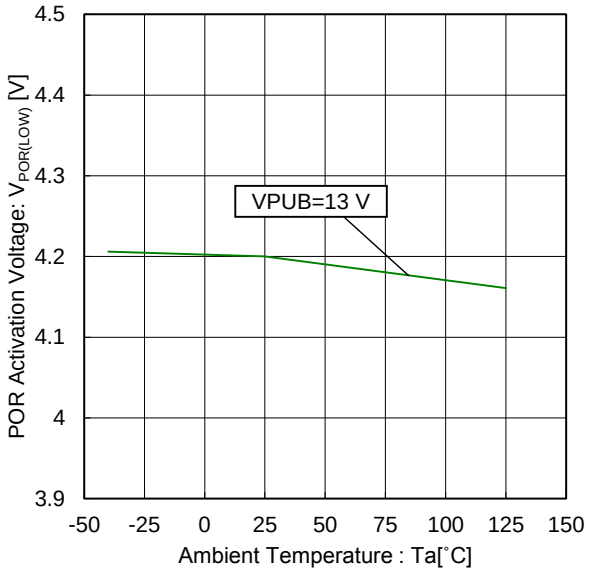


Figure 22. POR (Power on Reset) Activation Voltage vs Ambient Temperature

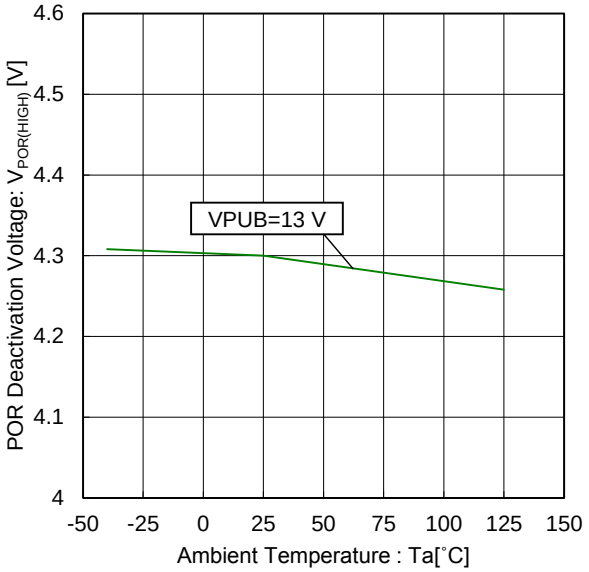


Figure 23. POR (Power on Reset) Deactivation Voltage vs Ambient Temperature

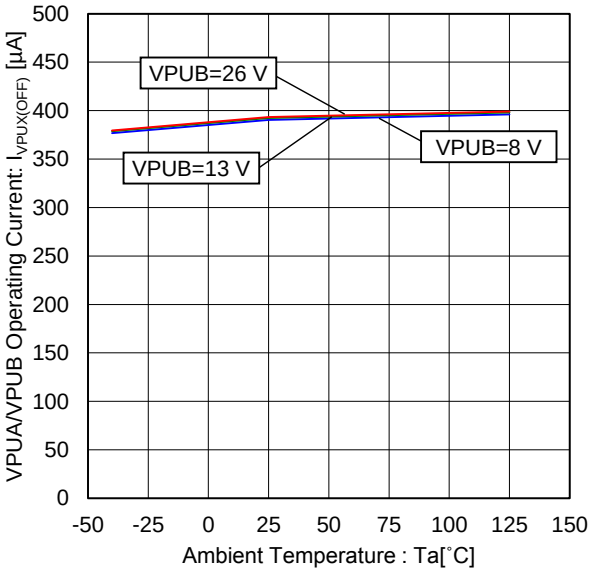


Figure 24. VPUA/VPUB Operating Current vs Ambient Temperature
(Continuous monitor setting, Current source is disabled, “Hi-Z” Status)

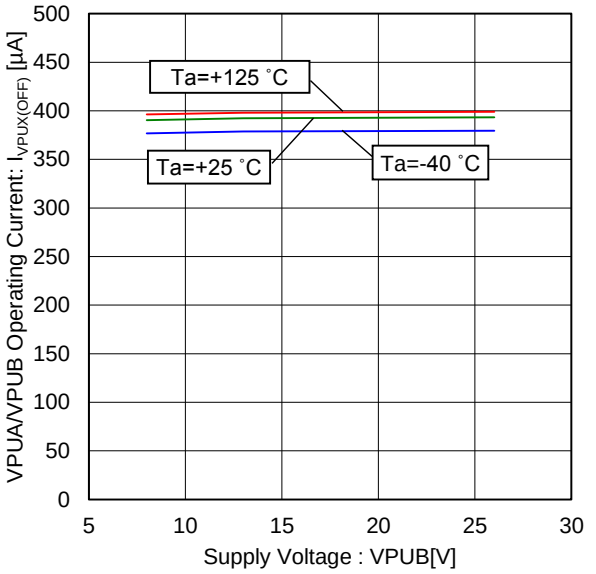


Figure 25. VPUA/VPUB Operating Current vs Supply Voltage
(Continuous monitor setting, Current source is disabled, “Hi-Z” Status)

Typical Performance Curves - continued

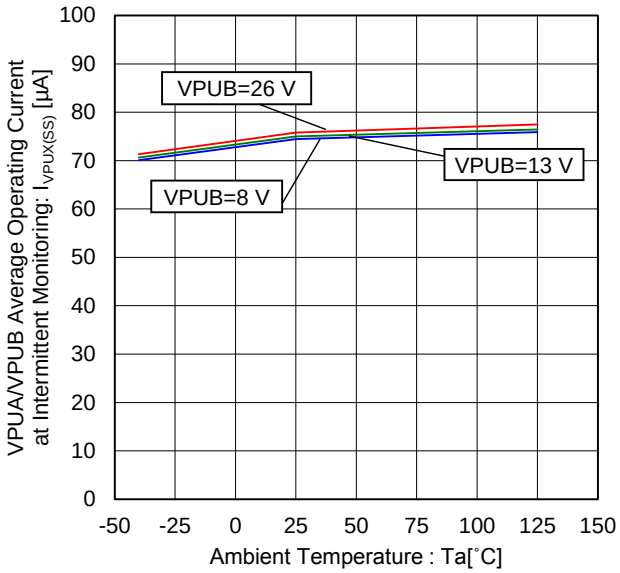


Figure 26. VPUA/VPUB Average Operating Current at Intermittent Monitoring vs Ambient Temperature (Monitoring Period: 50 ms, Strobe Time: 125 µs, Source/Sink Current Setting: 1 mA)

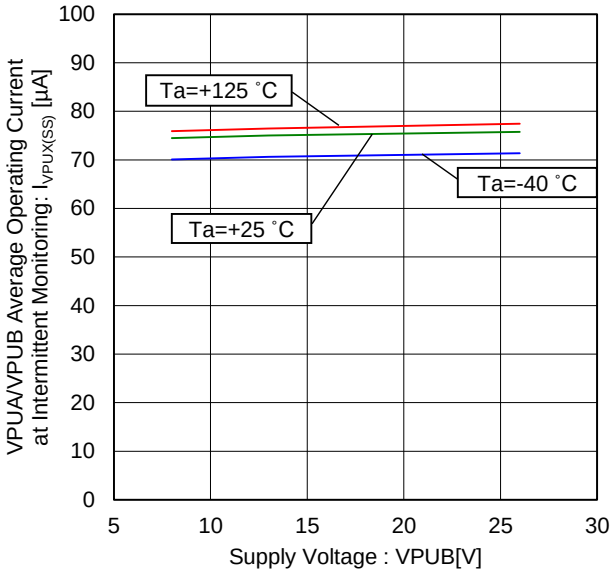


Figure 27. VPUA/VPUB Average Operating Current at Intermittent Monitoring vs Supply Voltage (Monitoring Period: 50 ms, Strobe Time: 125 µs, Source/Sink Current Setting: 1 mA)

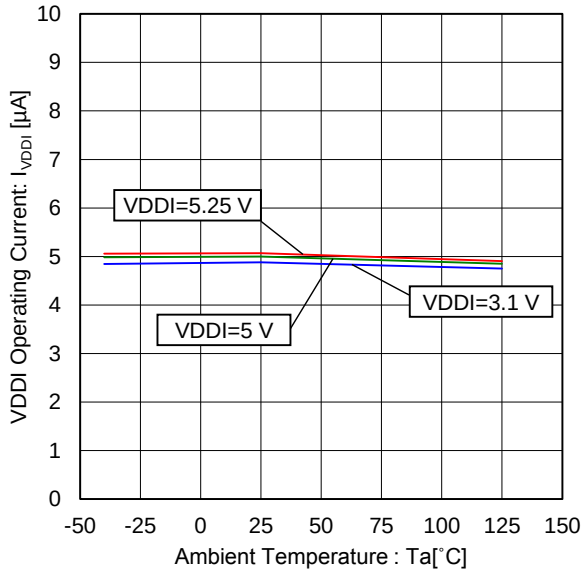


Figure 28. VDDI Operating Current vs Ambient Temperature (INTB="H", CSB="H")

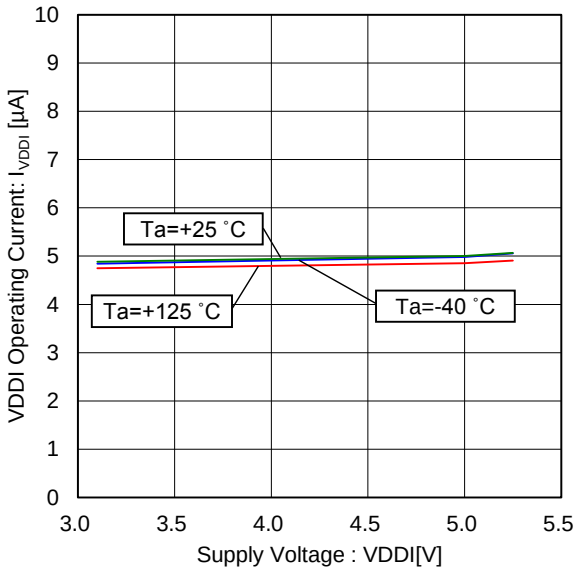


Figure 29. VDDI Operating Current vs Supply Voltage (INTB="H", CSB="H")

Typical Performance Curves - continued

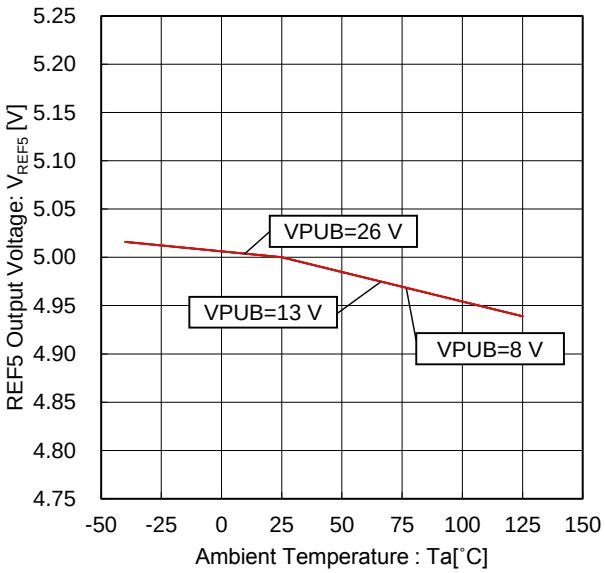


Figure 30. REF5 Output Voltage vs Ambient Temperature

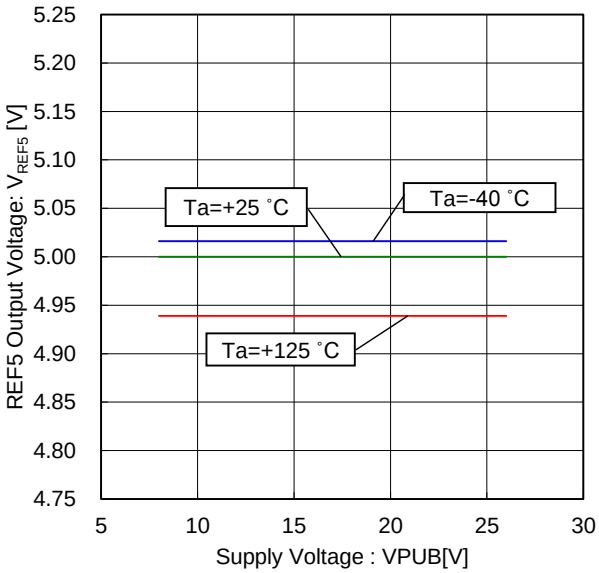


Figure 31. REF5 Output Voltage vs Supply Voltage

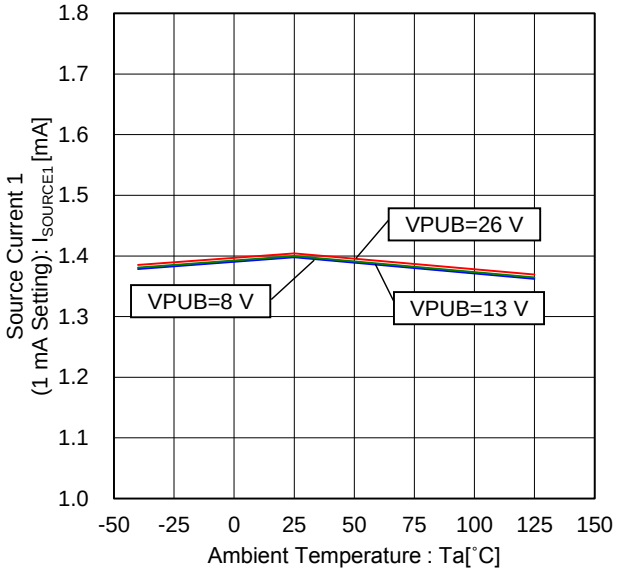


Figure 32. Source Current 1 vs Ambient Temperature
(1 mA Setting, 0 V external supply)

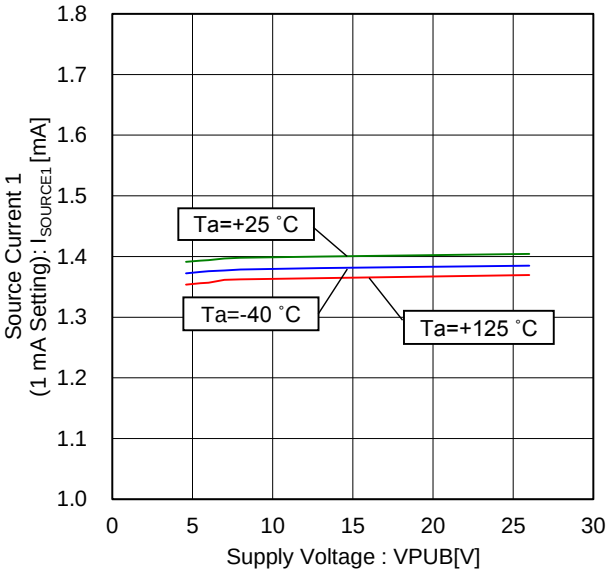


Figure 33. Source Current 1 vs Supply Voltage
(1 mA Setting, 0 V external supply)

Typical Performance Curves - continued

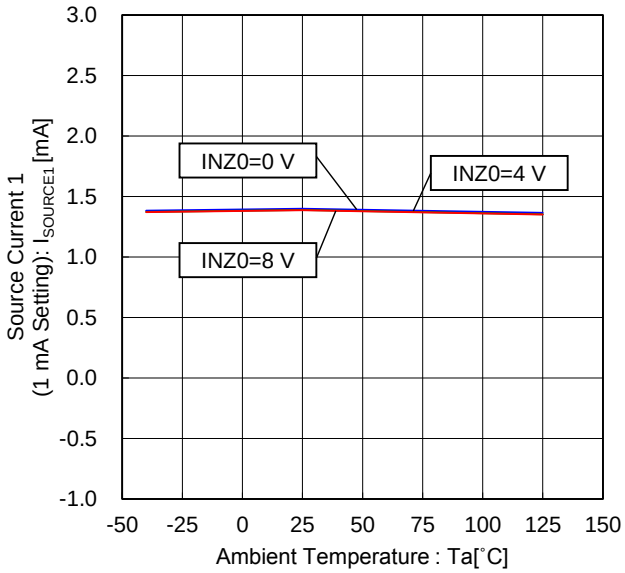


Figure 34. Source Current 1 vs Ambient Temperature
(1 mA Setting)

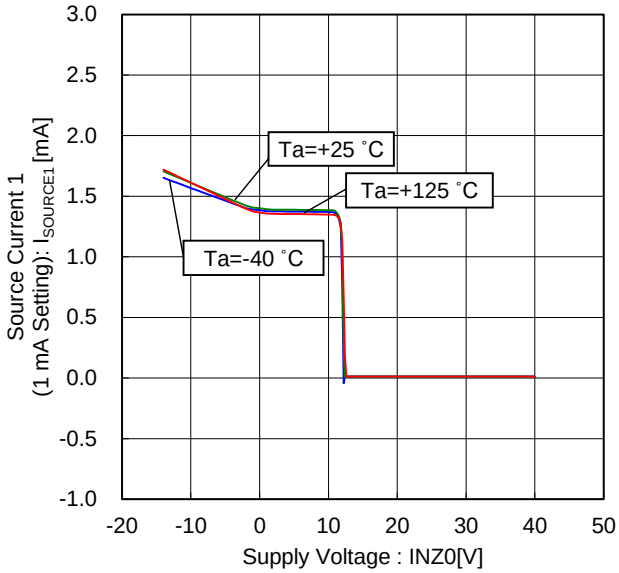


Figure 35. Source Current 1 vs Supply Voltage
(1 mA Setting)

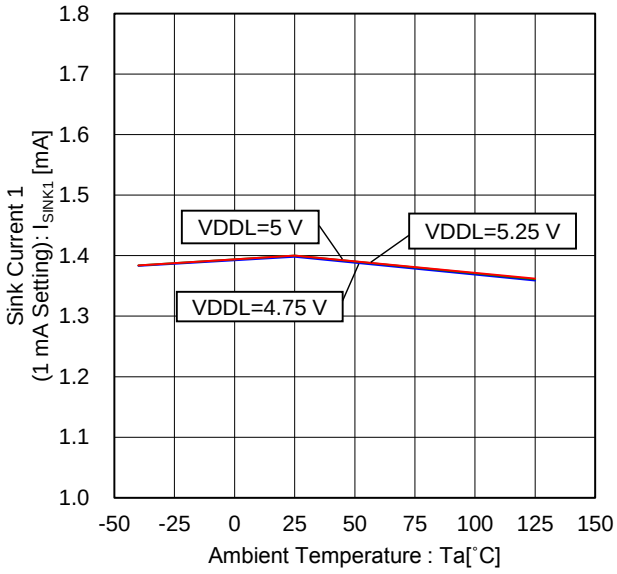


Figure 36. Sink Current 1 vs Ambient Temperature
(1 mA Setting, 8 V external supply)

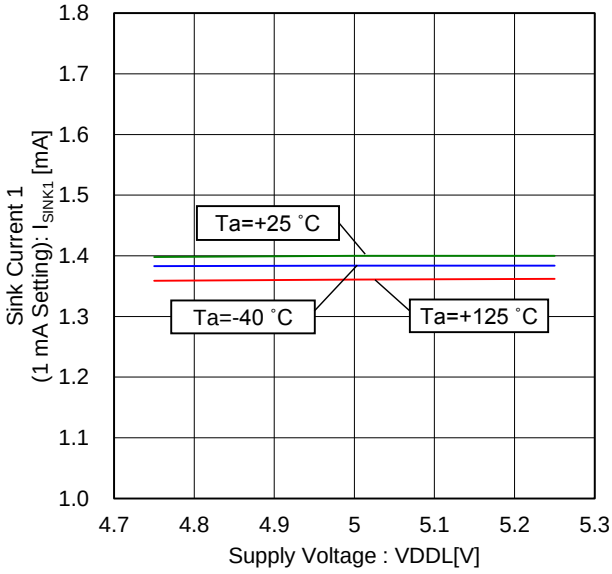


Figure 37. Sink Current 1 vs Supply Voltage
(1 mA Setting, 8 V external supply)

Typical Performance Curves - continued

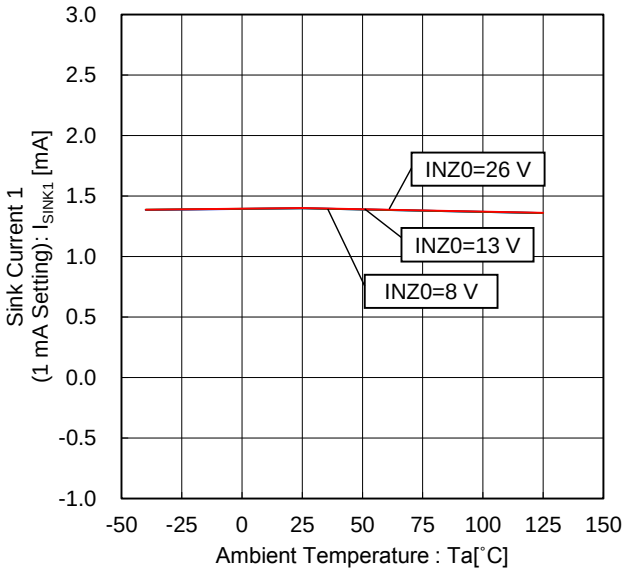


Figure 38. Sink Current 1 vs Ambient Temperature
(1 mA Setting)

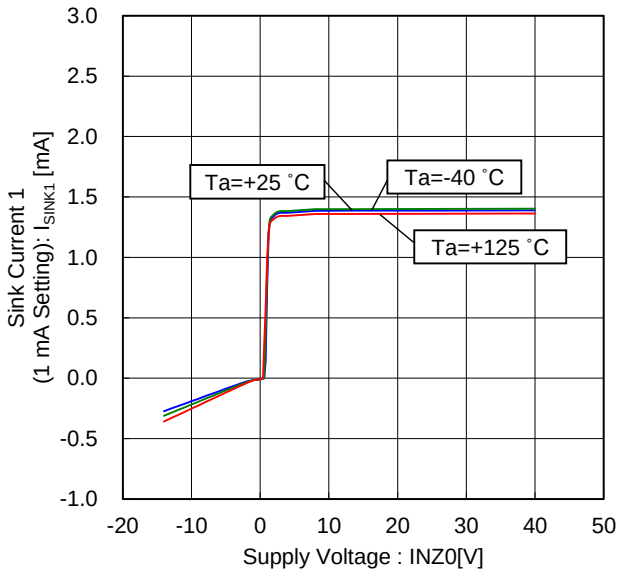


Figure 39. Sink Current 1 vs Supply Voltage
(1 mA Setting)

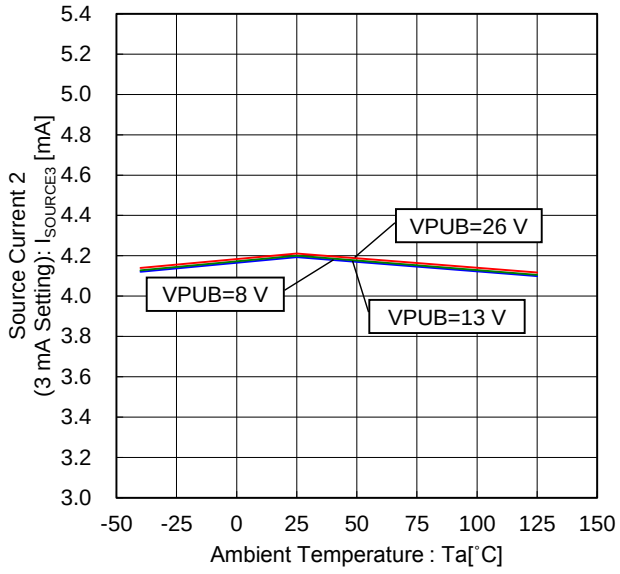


Figure 40. Source Current 2 vs Ambient Temperature
(3 mA Setting, 0 V external supply)

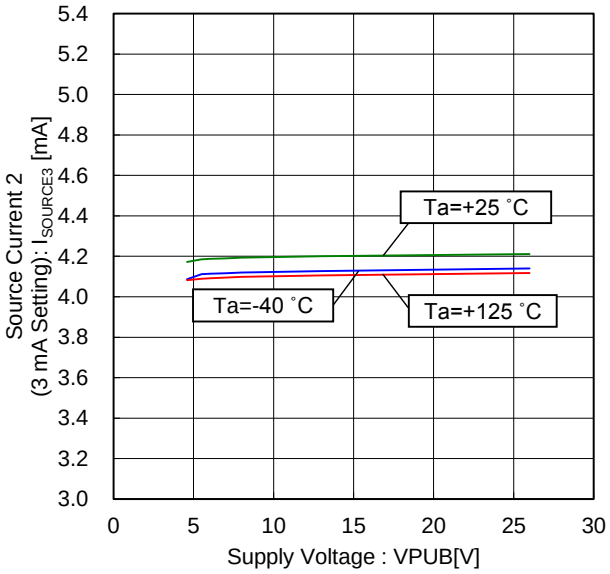


Figure 41. Source Current 2 vs Supply Voltage
(3 mA Setting, 0 V external supply)

Typical Performance Curves - continued

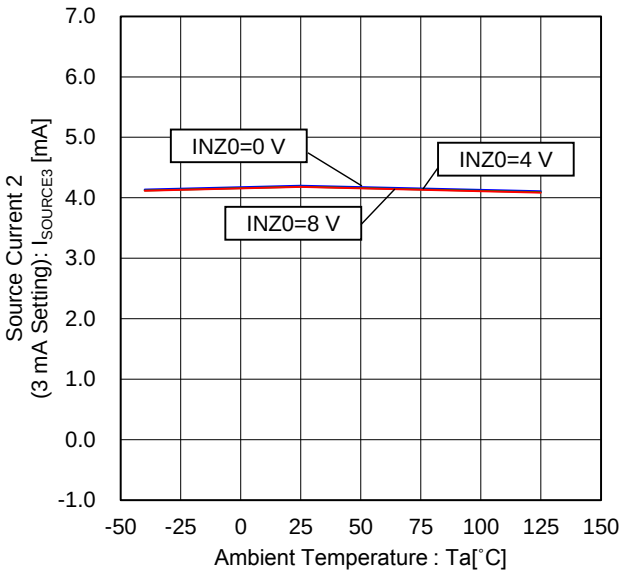


Figure 42. Source Current 2 vs Ambient Temperature
(3 mA Setting)

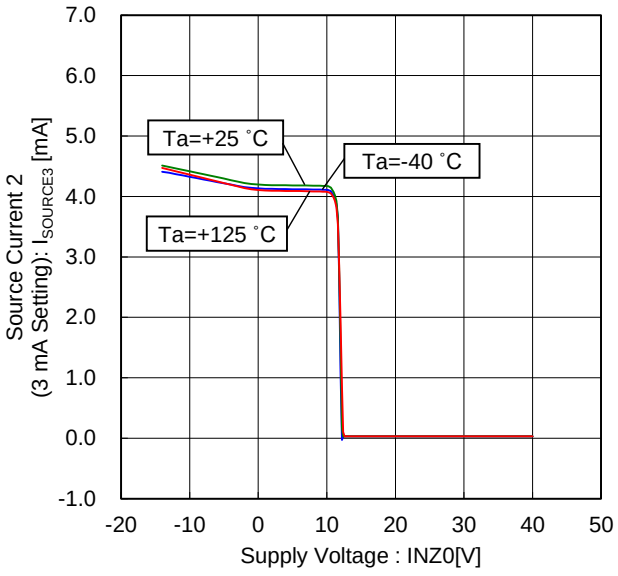


Figure 43. Source Current 2 vs Supply Voltage
(3 mA Setting)

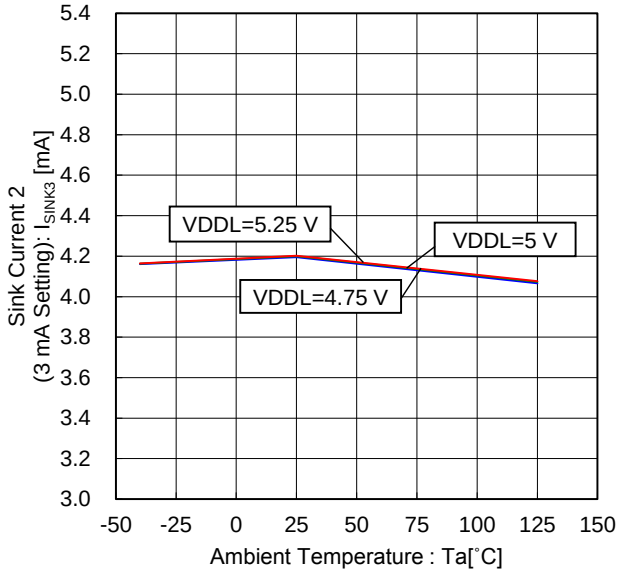


Figure 44. Sink Current 2 vs Ambient Temperature
(3 mA Setting, 8 V external supply)

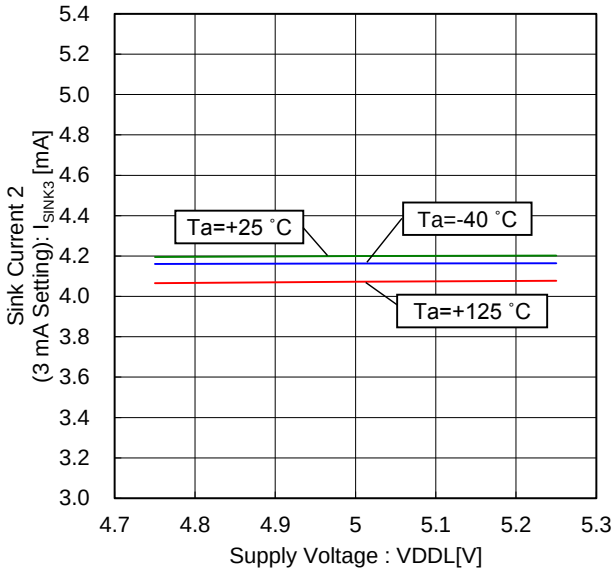


Figure 45. Sink Current 2 vs Supply Voltage
(3 mA Setting, 8 V external supply)

Typical Performance Curves - continued

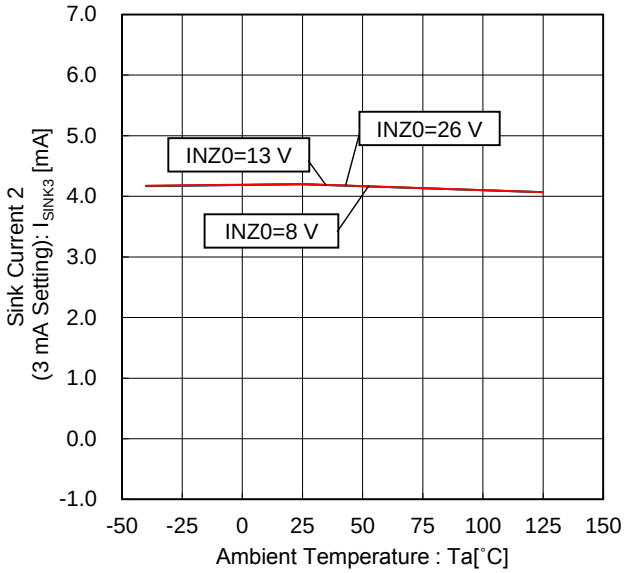


Figure 46. Sink Current 2 vs Ambient Temperature
(3 mA Setting)

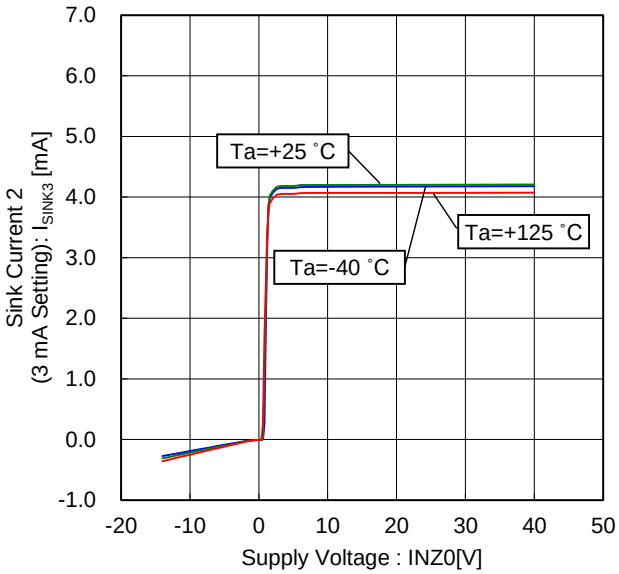


Figure 47. Sink Current 2 vs Supply Voltage
(3 mA Setting)

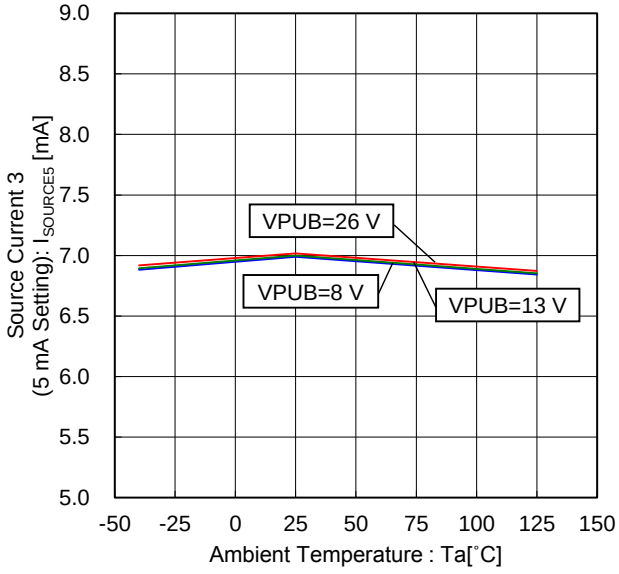


Figure 48. Source Current 3 vs Ambient Temperature
(5 mA Setting, 0 V external supply)

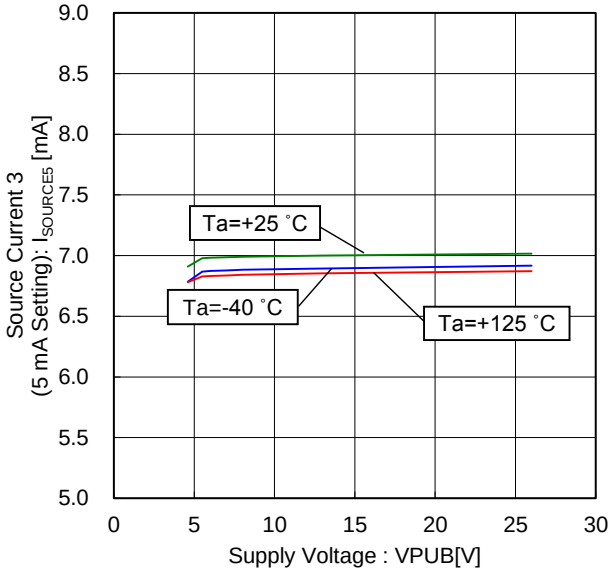


Figure 49. Source Current 3 vs Supply Voltage
(5 mA Setting, 0 V external supply)

Typical Performance Curves - continued

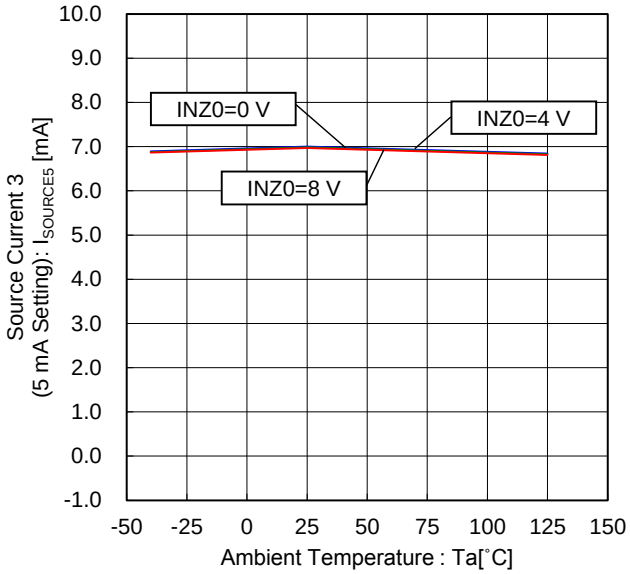


Figure 50. Source Current 3 vs Ambient Temperature
(5 mA Setting)

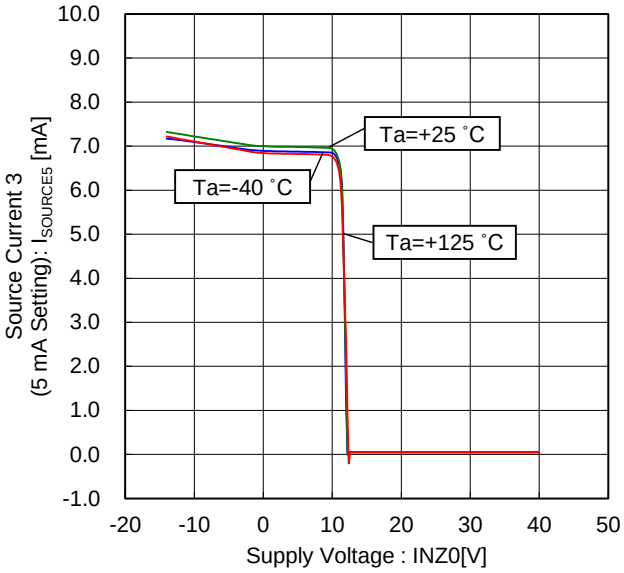


Figure 51. Source Current 3 vs Supply Voltage
(5 mA Setting)

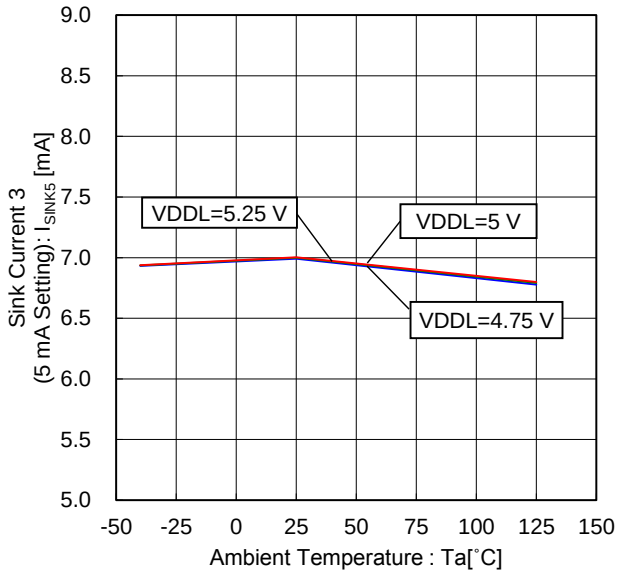


Figure 52. Sink Current 3 vs Ambient Temperature
(5 mA Setting, 8 V external supply)

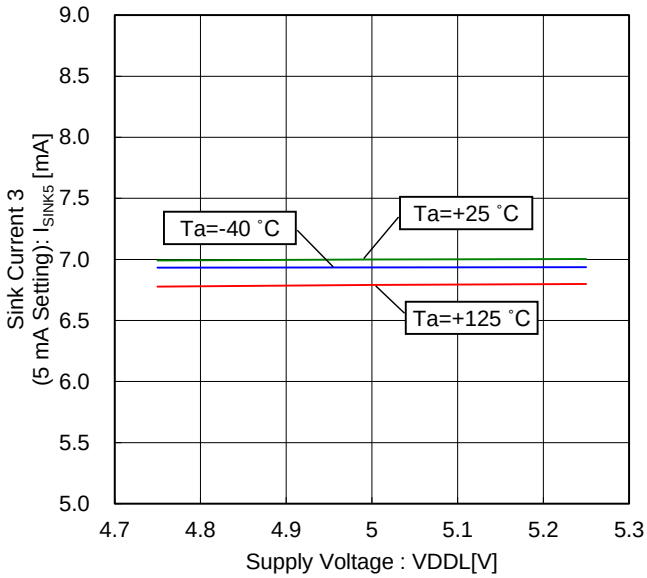


Figure 53. Sink Current 3 vs Supply Voltage
(5 mA Setting, 8 V external supply)

Typical Performance Curves - continued

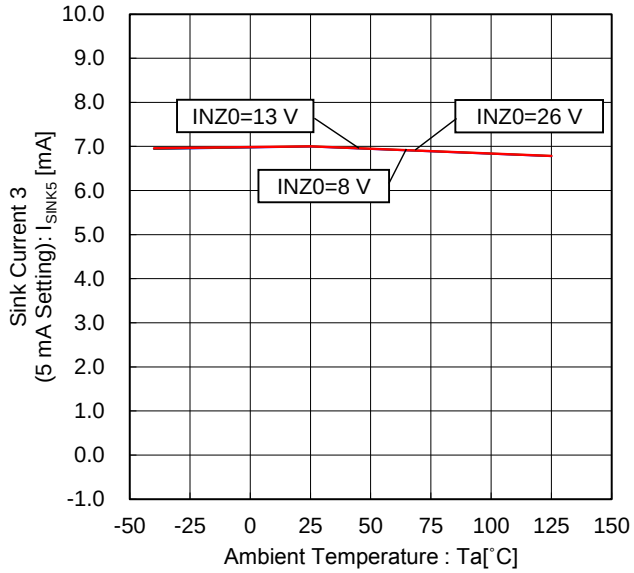


Figure 54. Sink Current 3 vs Ambient Temperature
(5 mA Setting)

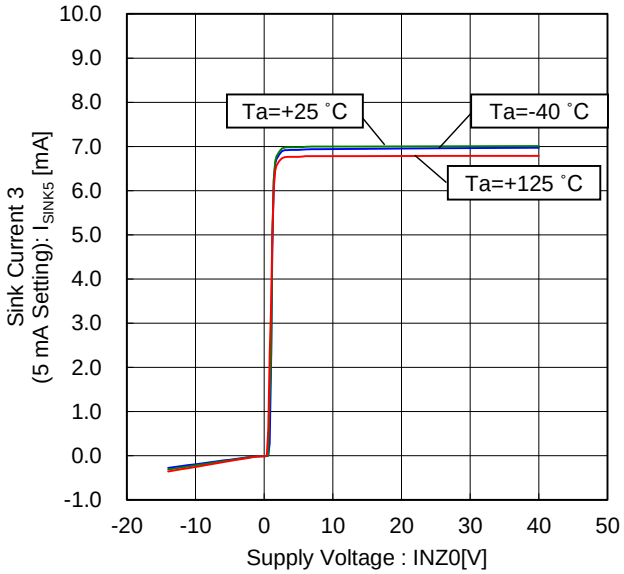


Figure 55. Sink Current 3 vs Supply Voltage
(5 mA Setting)

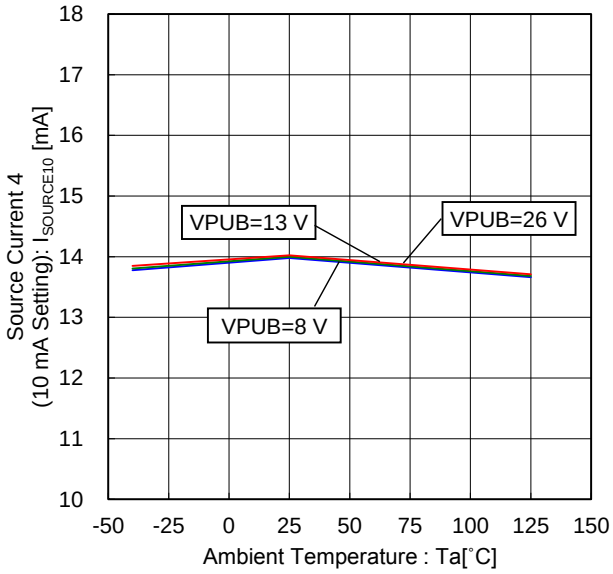


Figure 56. Source Current 4 vs Ambient Temperature
(10 mA Setting, 0 V external supply)

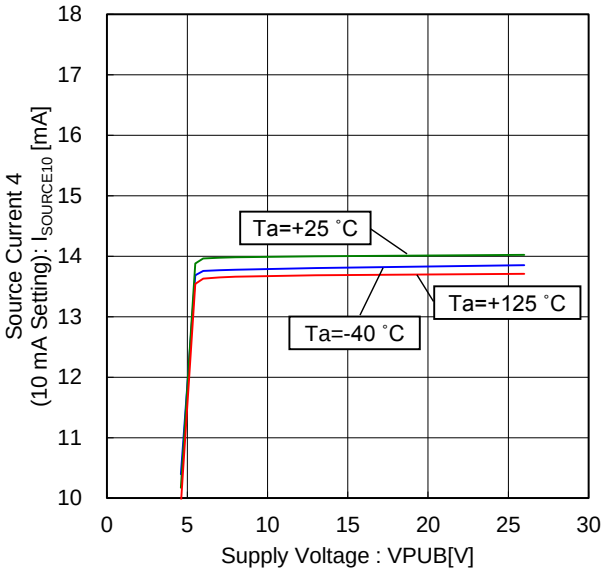


Figure 57. Source Current 4 vs Supply Voltage
(10 mA Setting, 0 V external supply)

Typical Performance Curves - continued

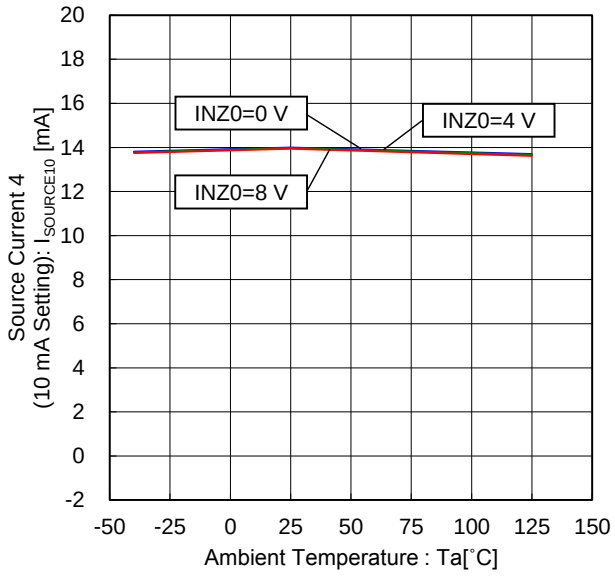


Figure 58. Source Current 4 vs Ambient Temperature (10 mA Setting)

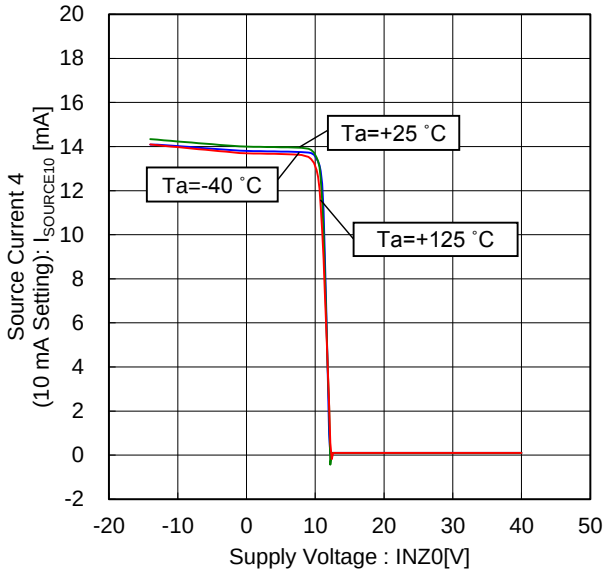


Figure 59. Source Current 4 vs Supply Voltage (10 mA Setting)

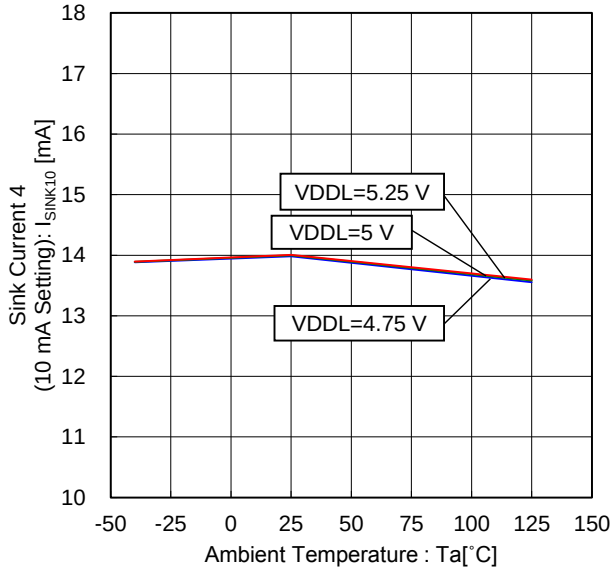


Figure 60. Sink Current 4 vs Ambient Temperature (10 mA Setting, 8 V external supply)

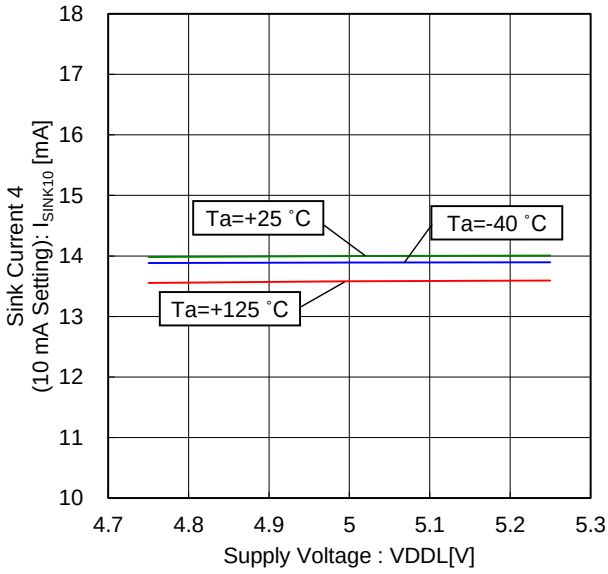


Figure 61. Sink Current 4 vs Supply Voltage (10 mA Setting, 8 V external supply)

Typical Performance Curves - continued

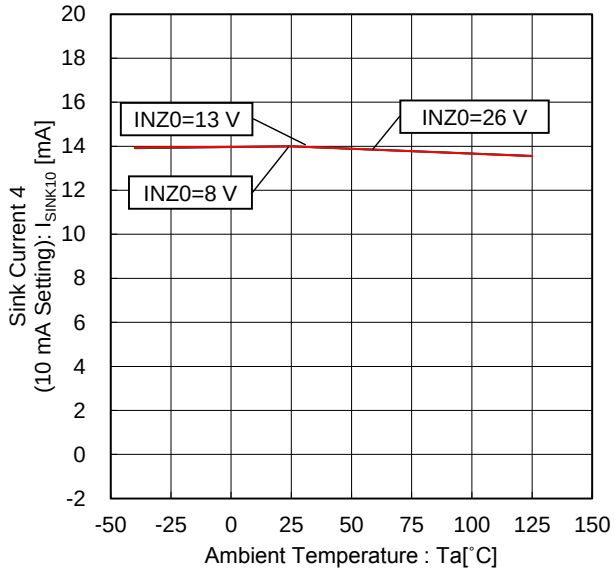


Figure 62. Sink Current 4 vs Ambient Temperature
(10 mA Setting)

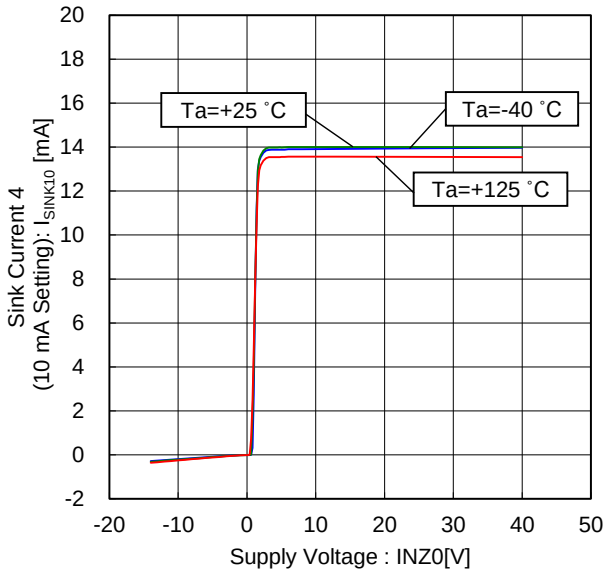


Figure 63. Sink Current 4 vs Supply Voltage
(10 mA Setting)

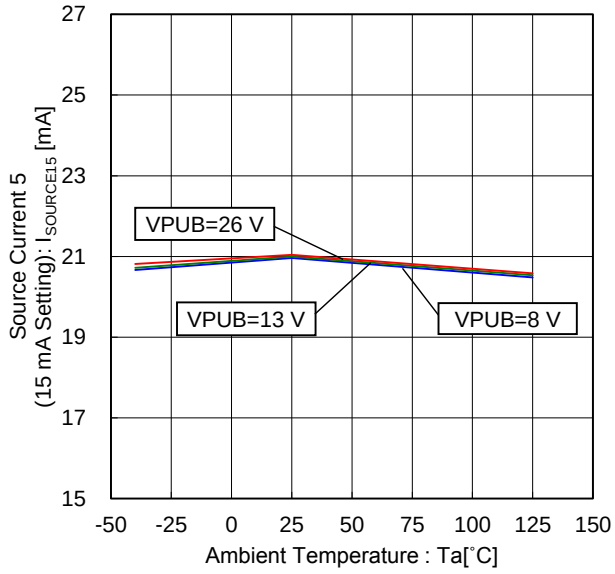


Figure 64. Source Current 5 vs Ambient Temperature
(15 mA Setting, 0 V external supply)

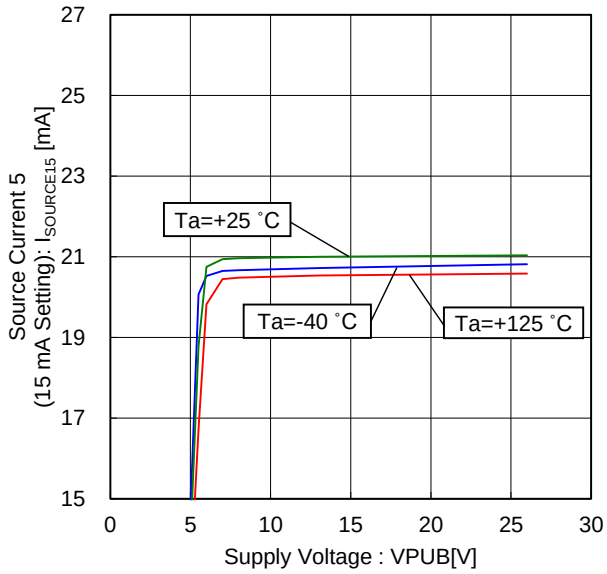


Figure 65. Source Current 5 vs Supply Voltage
(15 mA Setting, 0 V external supply)

Typical Performance Curves - continued

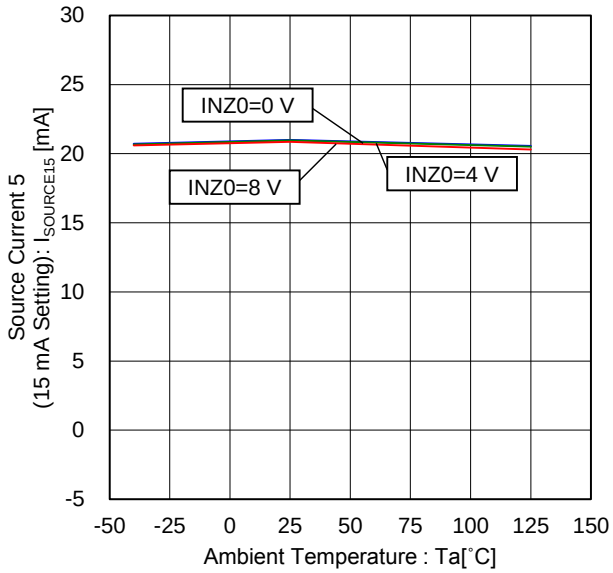


Figure 66. Source Current 5 vs Ambient Temperature
(15 mA Setting)

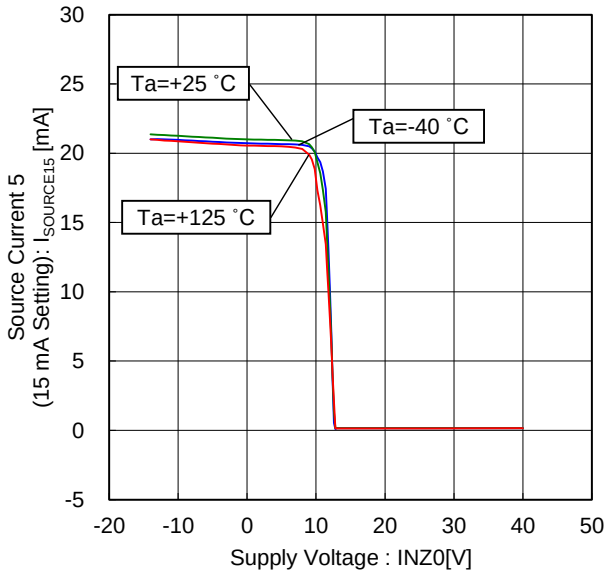


Figure 67. Source Current 5 vs Supply Voltage
(15 mA Setting)

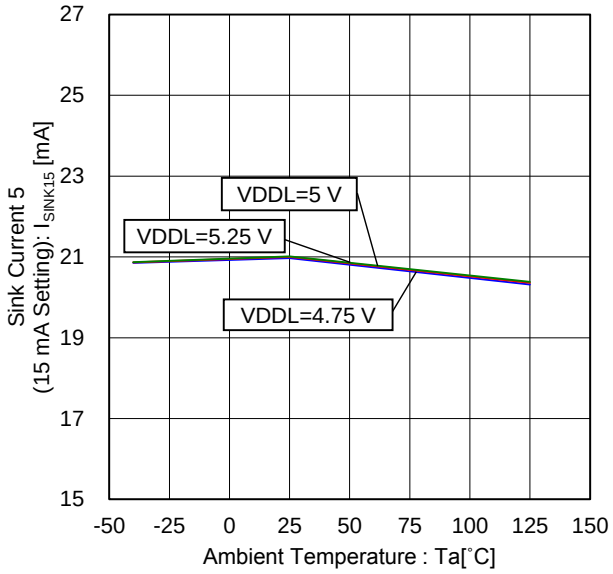


Figure 68. Sink Current 5 vs Ambient Temperature
(15 mA Setting, 8 V external supply)

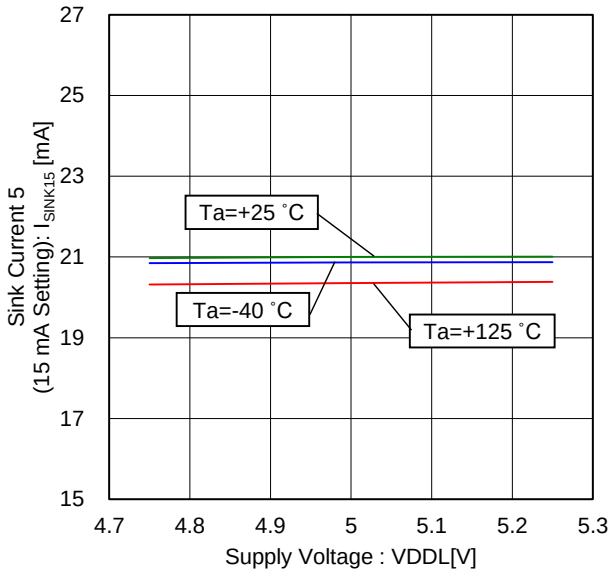


Figure 69. Sink Current 5 vs Supply Voltage
(15 mA Setting, 8 V external supply)

Typical Performance Curves - continued

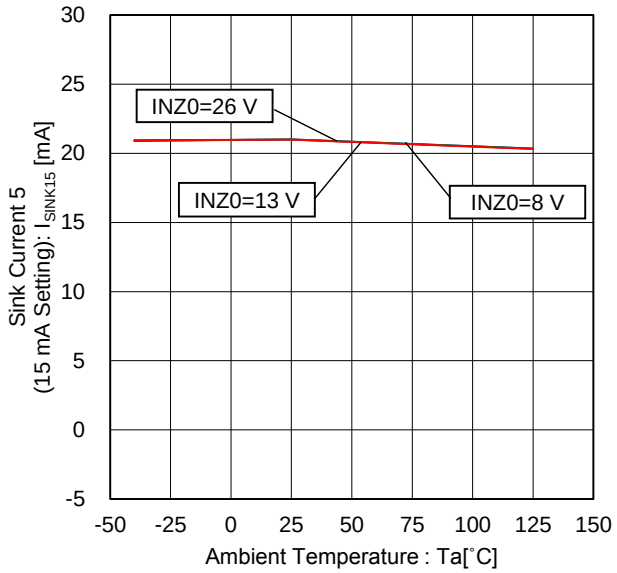


Figure 70. Sink Current 5 vs Ambient Temperature (15 mA Setting)

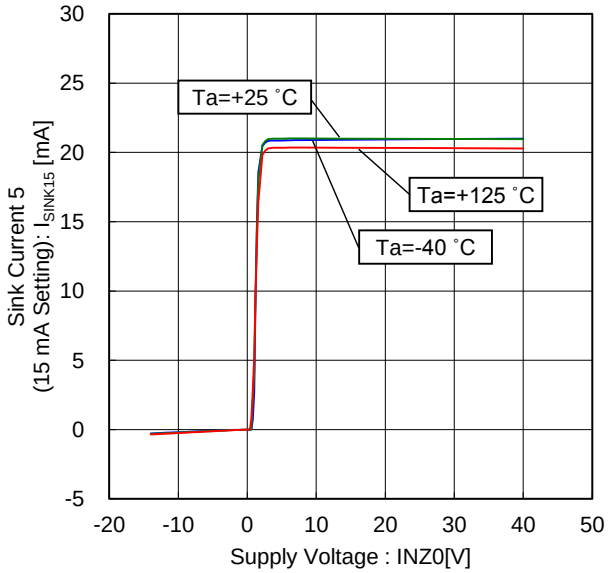


Figure 71. Sink Current 5 vs Supply Voltage (15 mA Setting)

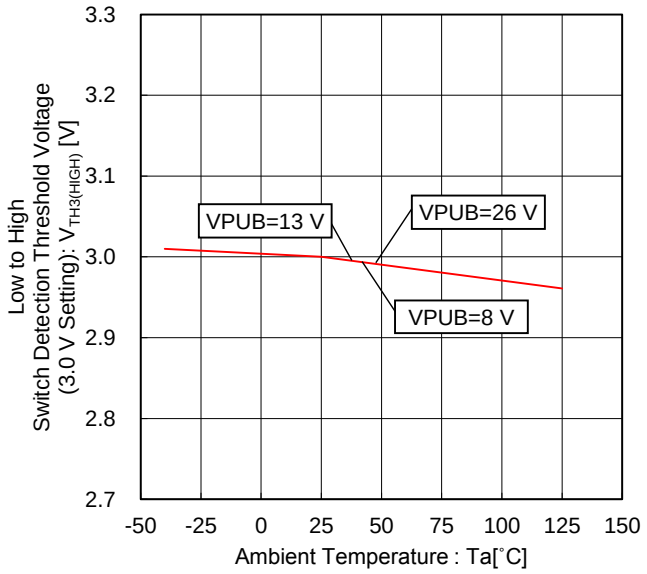


Figure 72. Low to High Switch Detection Threshold Voltage vs Ambient Temperature (3.0 V Setting)

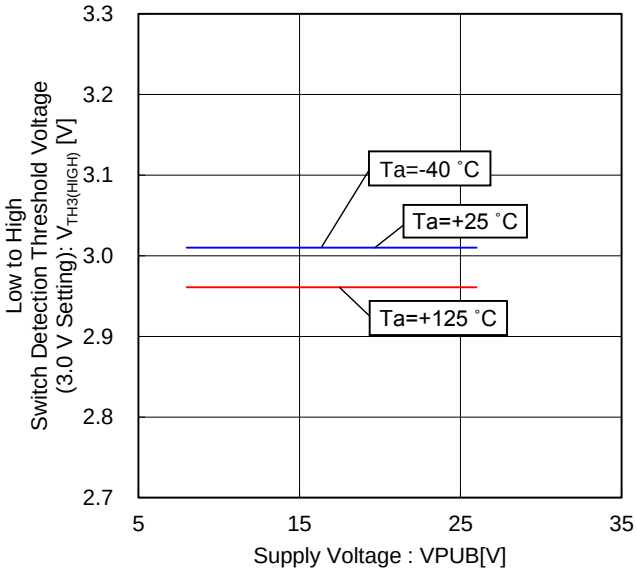


Figure 73. Low to High Switch Detection Threshold Voltage vs Supply Voltage (3.0 V Setting)

Typical Performance Curves - continued

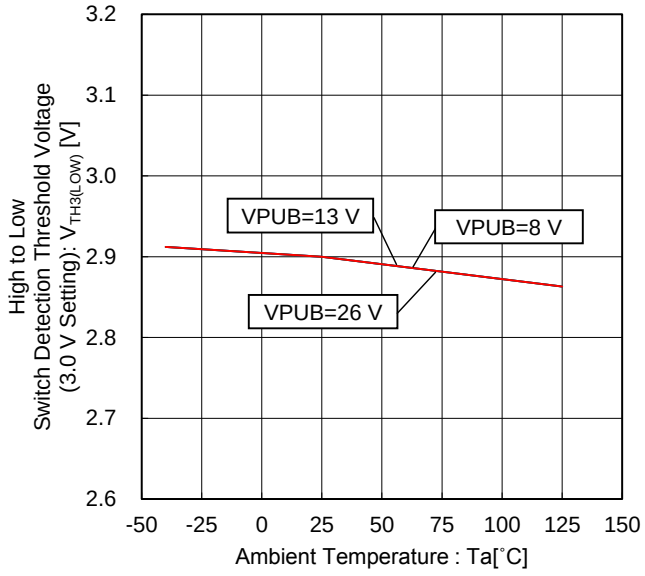


Figure 74. High to Low Switch Detection Threshold Voltage vs Ambient Temperature (3.0 V Setting)

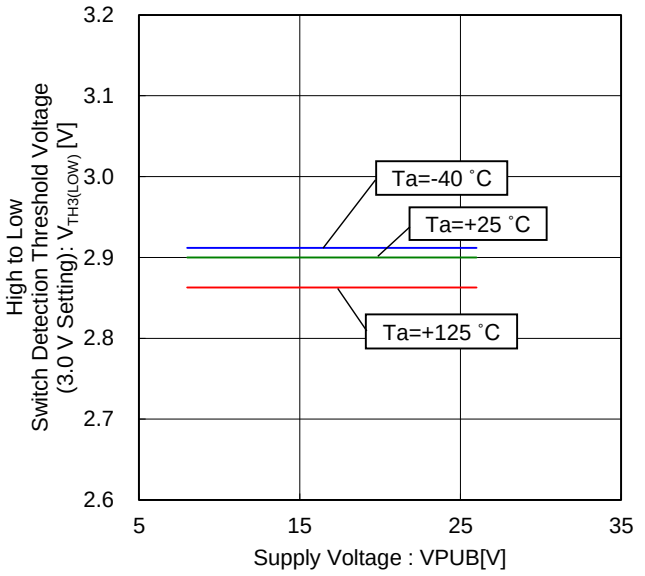


Figure 75. High to Low Switch Detection Threshold Voltage vs Supply Voltage (3.0 V Setting)

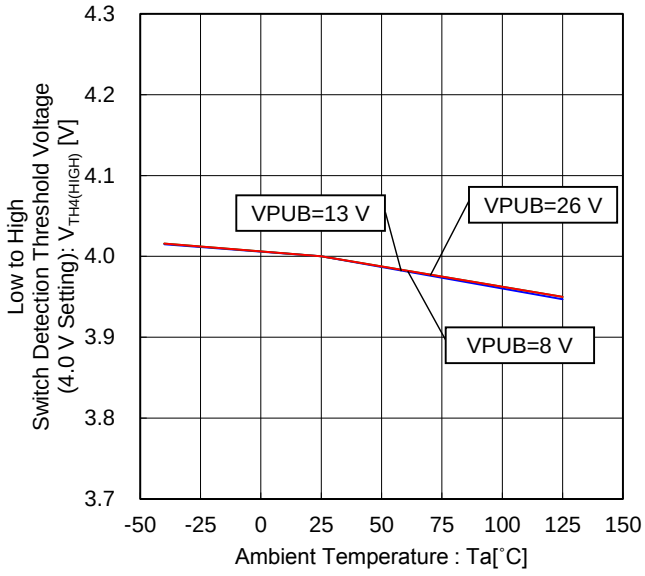


Figure 76. Low to High Switch Detection Threshold Voltage vs Ambient Temperature (4.0 V Setting)

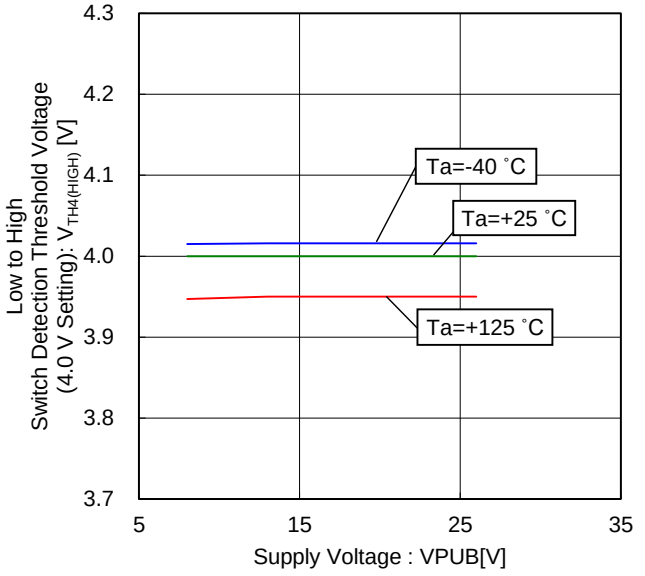


Figure 77. Low to High Switch Detection Threshold Voltage vs Supply Voltage (4.0 V Setting)

Typical Performance Curves - continued

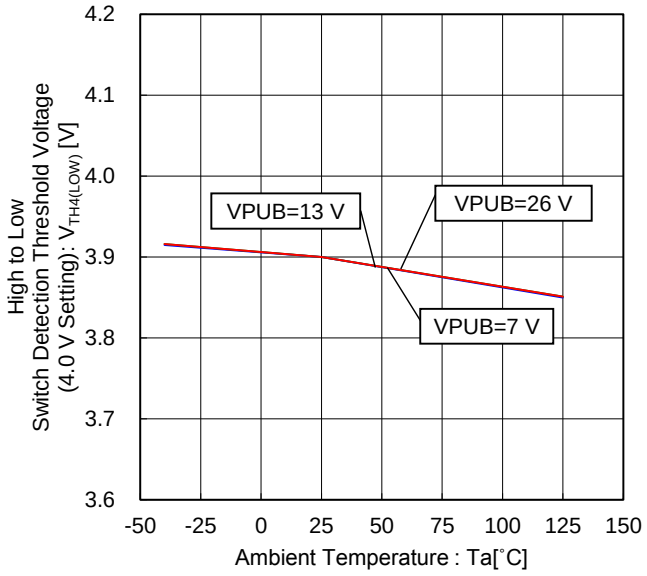


Figure 78. High to Low Switch Detection Threshold Voltage vs Ambient Temperature (4.0 V Setting)

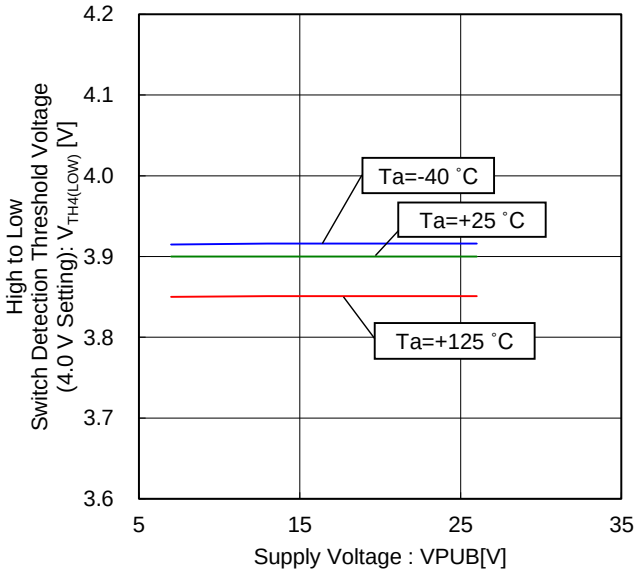


Figure 79. High to Low Switch Detection Threshold Voltage vs Supply Voltage (4.0 V Setting)

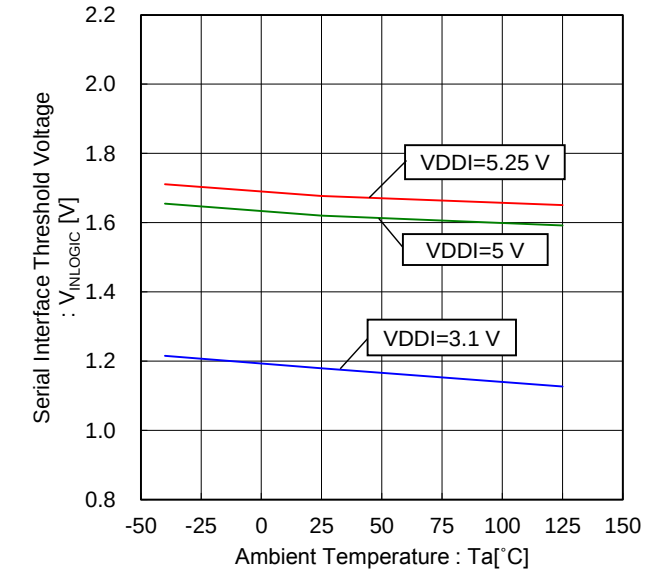


Figure 80. Serial Interface Threshold Voltage vs Ambient Temperature

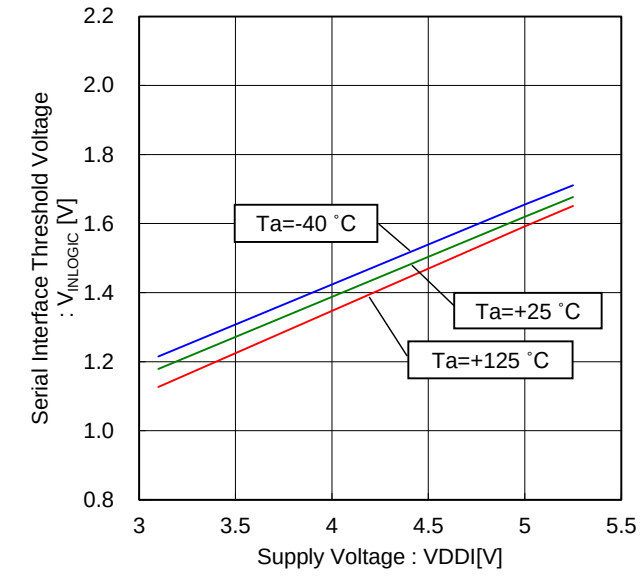


Figure 81. Serial Interface Threshold Voltage vs Supply Voltage

Typical Performance Curves - continued

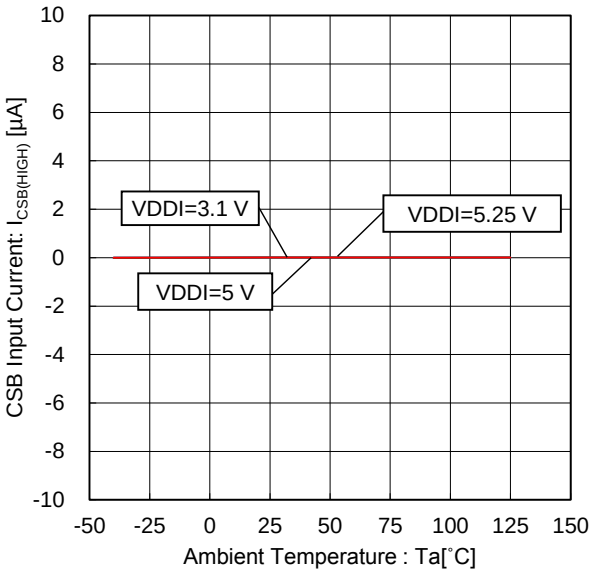


Figure 82. CSB Input Current vs Ambient Temperature (CSB=VDDI)

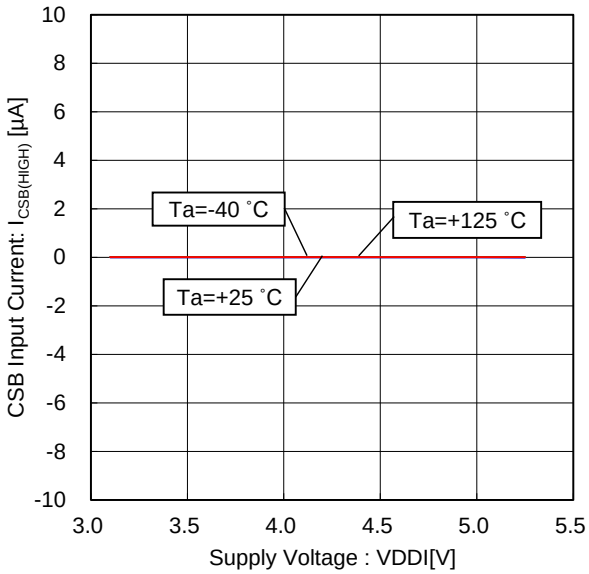


Figure 83. CSB Input Current vs Supply Voltage (CSB=VDDI)

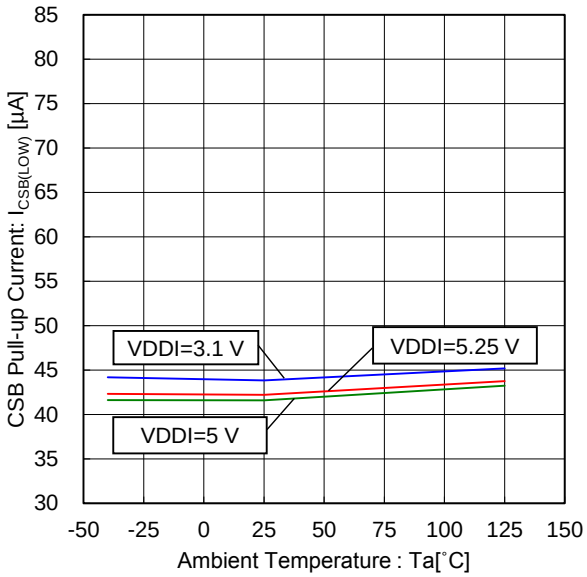


Figure 84. CSB Pull-up Current vs Ambient Temperature (CSB=0 V)

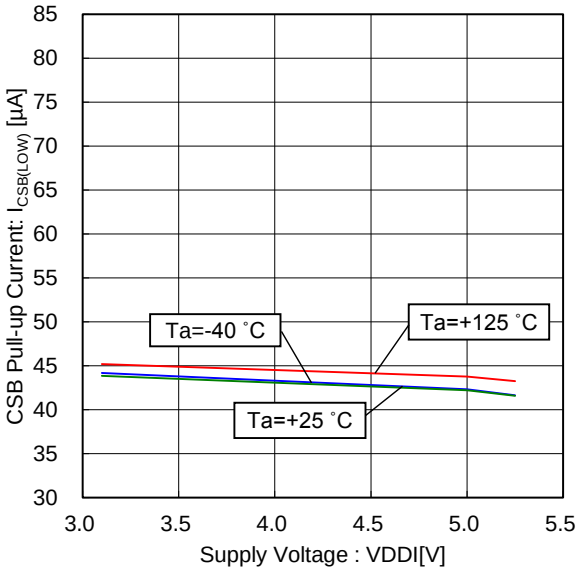


Figure 85. CSB Pull-up Current vs Supply Voltage (CSB=0 V)

Typical Performance Curves - continued

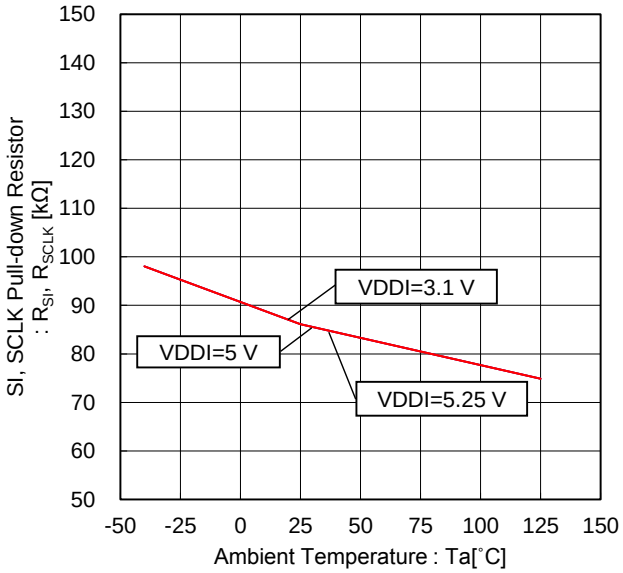


Figure 86. SI, SCLK Pull-down Resistor vs Ambient Temperature

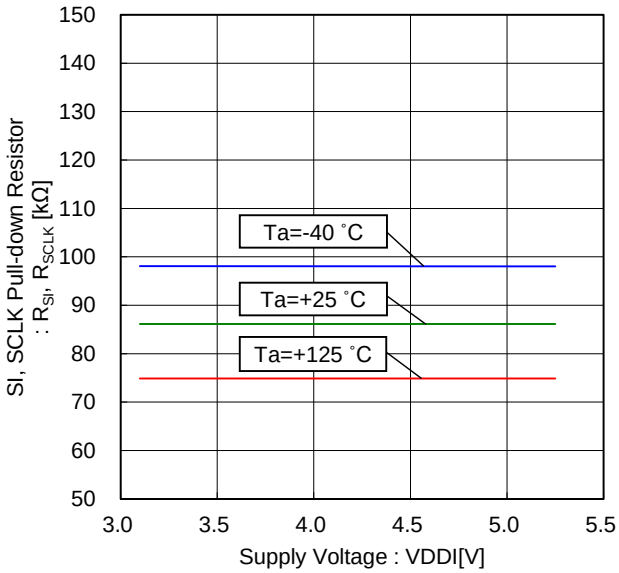


Figure 87. SI, SCLK Pull-down Resistor vs Supply Voltage

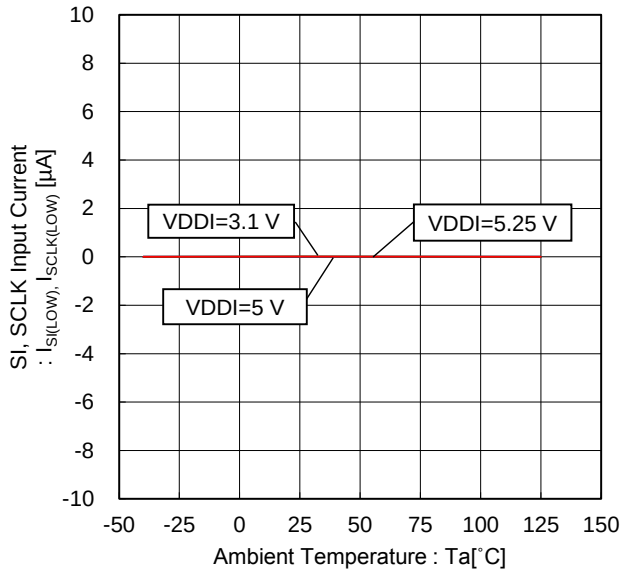


Figure 88. SI, SCLK Input Current vs Ambient Temperature (SI, SCLK=0 V)

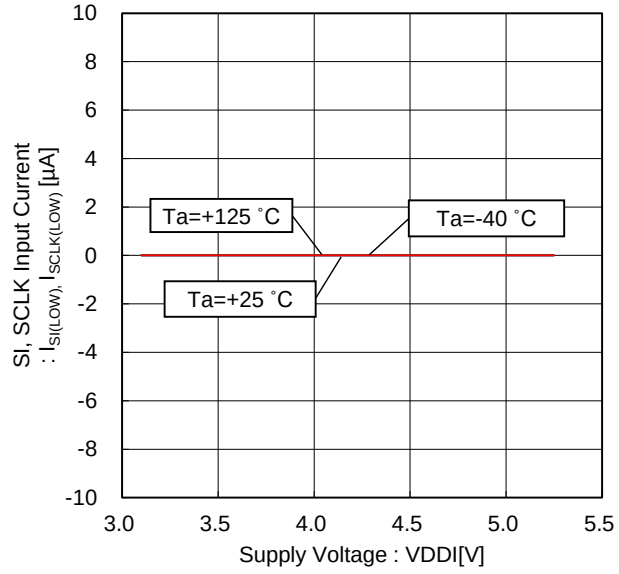


Figure 89. SI, SCLK Input Current vs Supply Voltage (SI, SCLK=0 V)

Typical Performance Curves - continued

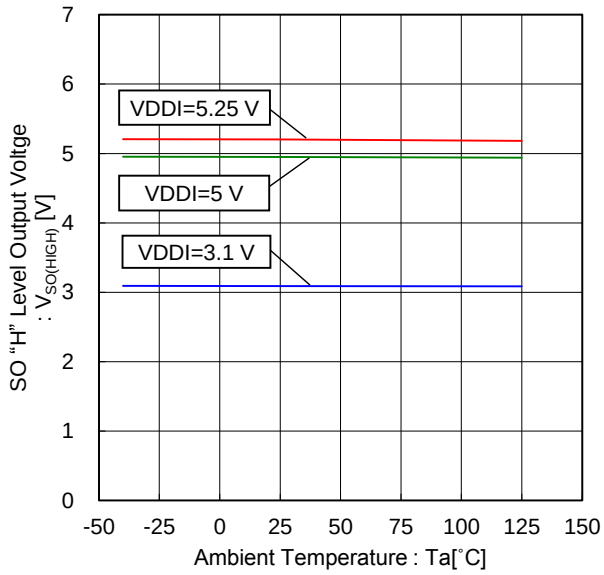


Figure 90. SO “H” Level Output Voltage vs Ambient Temperature (I_{SOURCE}=200 µA)

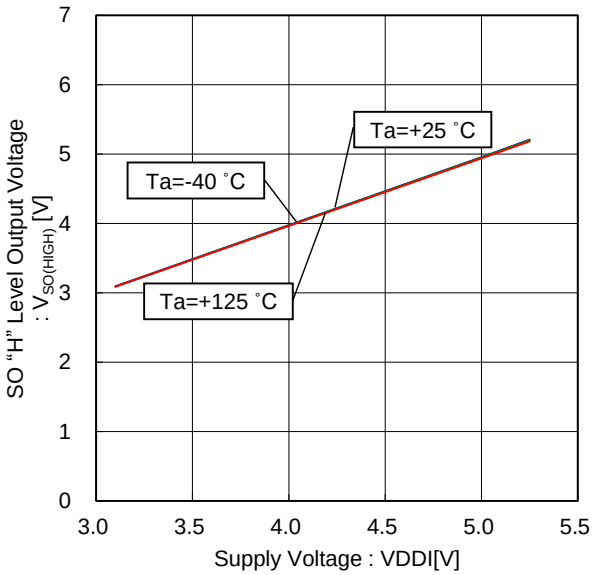


Figure 91. SO “H” Level Output Voltage vs Supply Voltage (I_{SOURCE}=200 µA)

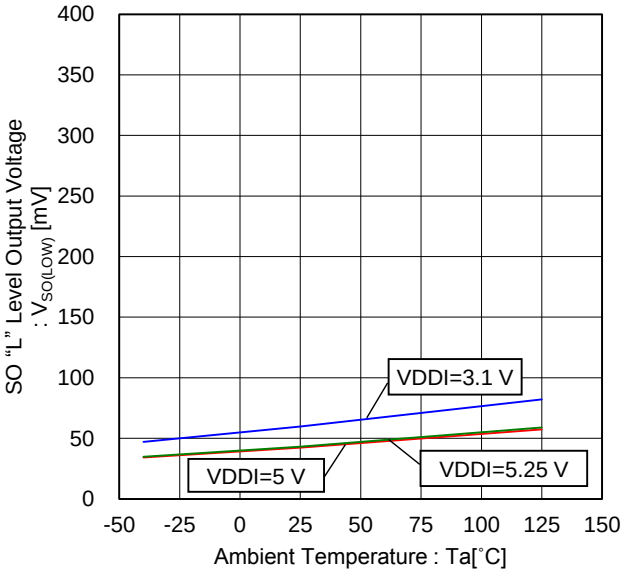


Figure 92. SO “L” Level Output Voltage vs Ambient Temperature (I_{SINK}=1.6 mA)

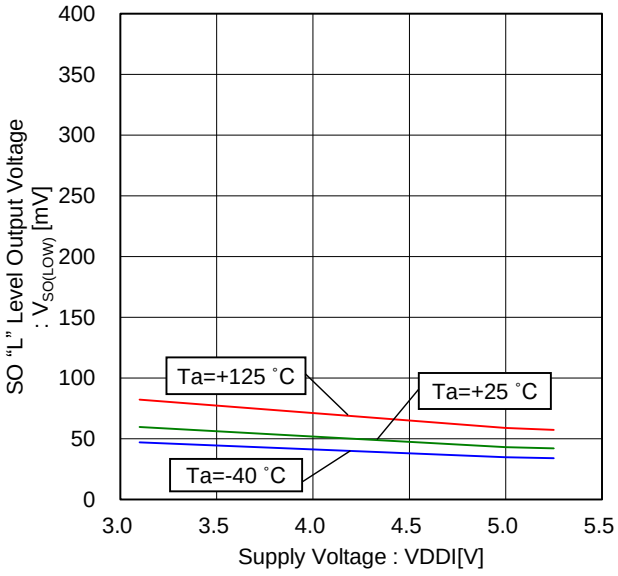


Figure 93. SO “L” Level Output Voltage vs Supply Voltage (I_{SINK} =1.6 mA)

Typical Performance Curves - continued

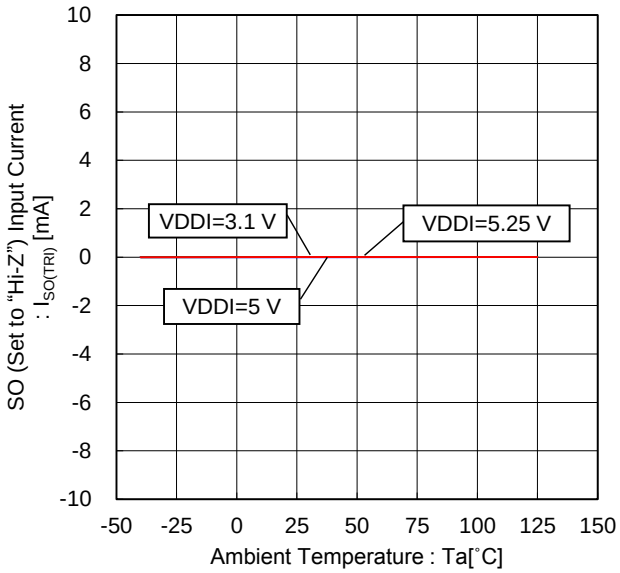


Figure 94. SO (Set to “Hi-Z”) Input Current vs Ambient Temperature

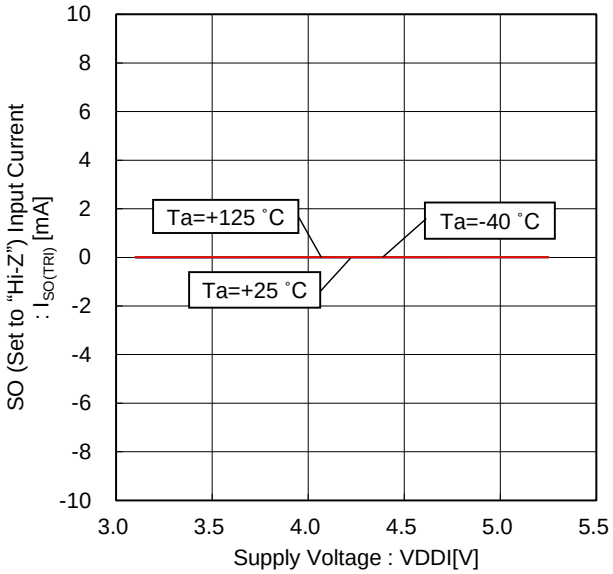


Figure 95. SO (Set to “Hi-Z”) Input Current vs Supply Voltage

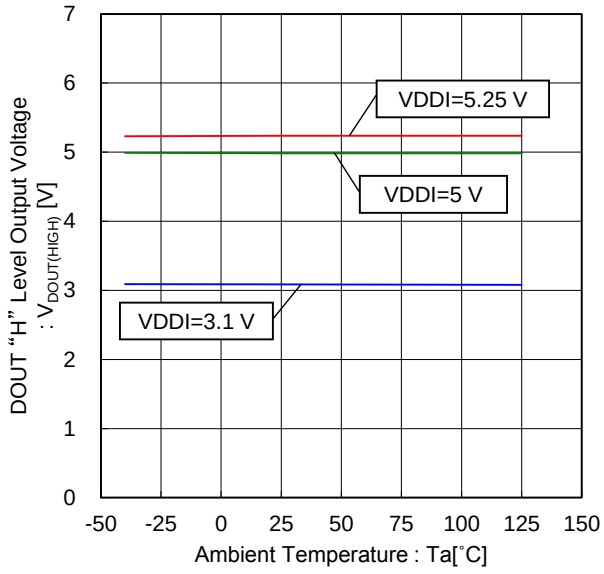


Figure 96. DOUT “H” Level Output Voltage vs Ambient Temperature (I_{SOURCE}=200 µA)

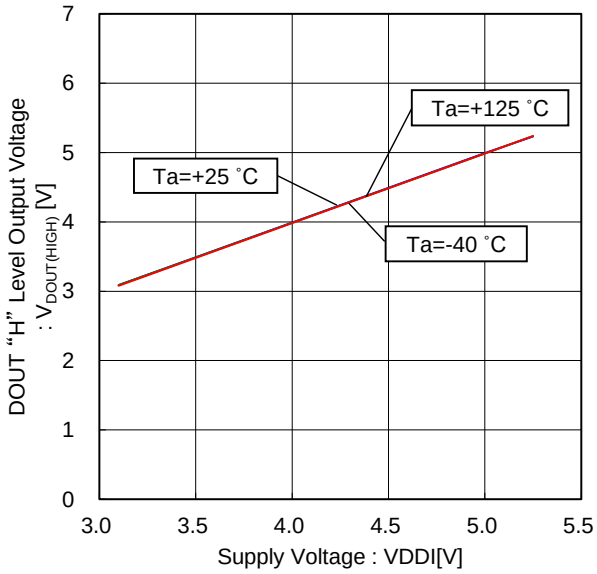


Figure 97. DOUT “H” Level Output Voltage vs Supply Voltage (I_{SOURCE}=200 µA)

Typical Performance Curves - continued

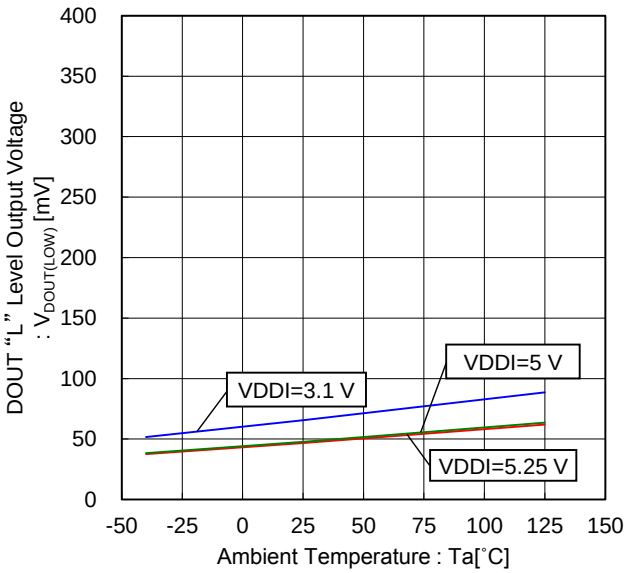


Figure 98. DOUT “L” Level Output Voltage vs Ambient Temperature (I_{SINK}=1.6 mA)

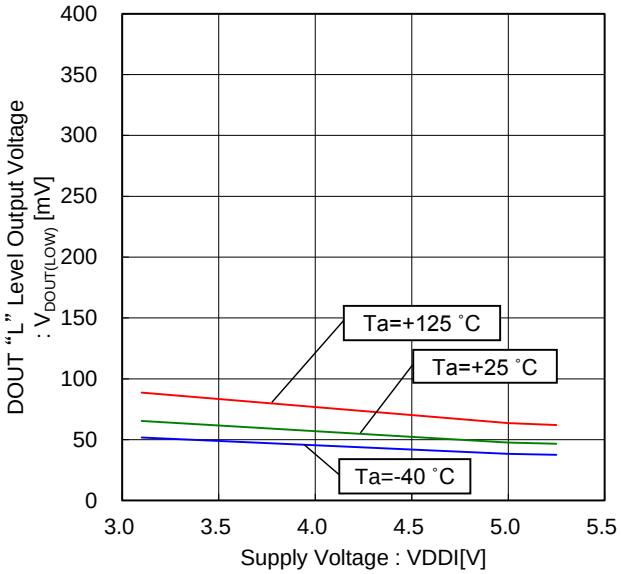


Figure 99. DOUT “L” Level Output Voltage vs Supply Voltage (I_{SINK}=1.6 mA)

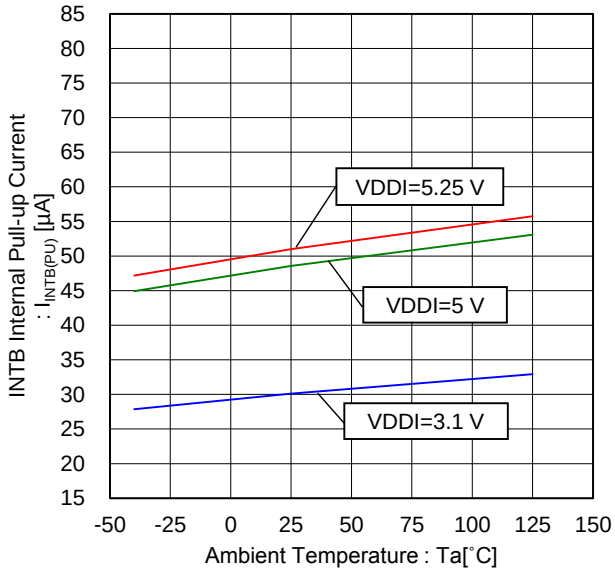


Figure 100. INTB Internal Pull-up Current vs Ambient Temperature

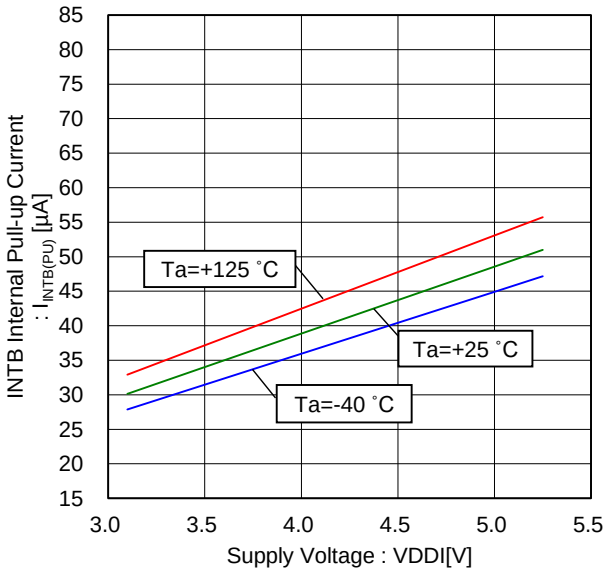


Figure 101. INTB Internal Pull-up Current vs Supply Voltage

Typical Performance Curves - continued

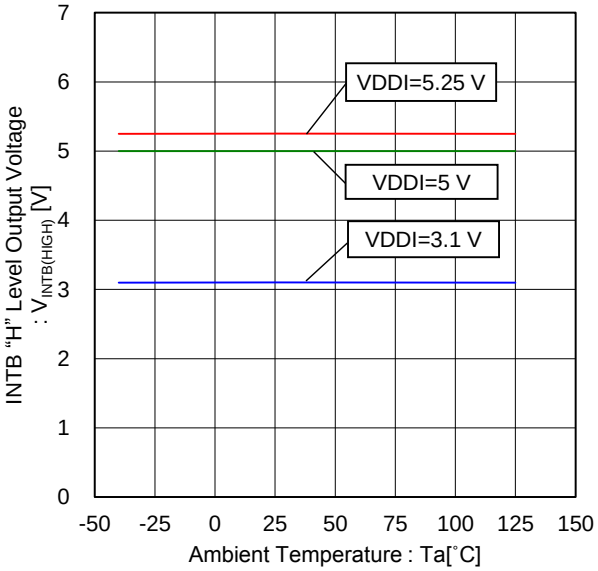


Figure 102. INTB "H" Level Output Voltage vs Ambient Temperature Characteristic (INTB=OPEN)

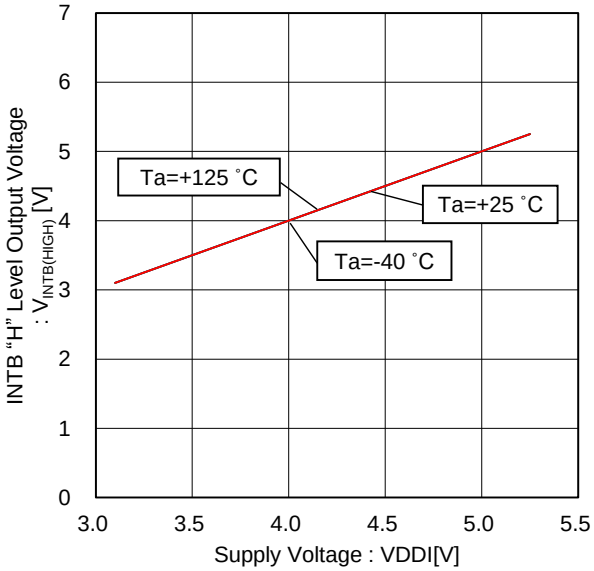


Figure 103. INTB "H" Level Output Voltage vs Supply Voltage (INTB=OPEN)

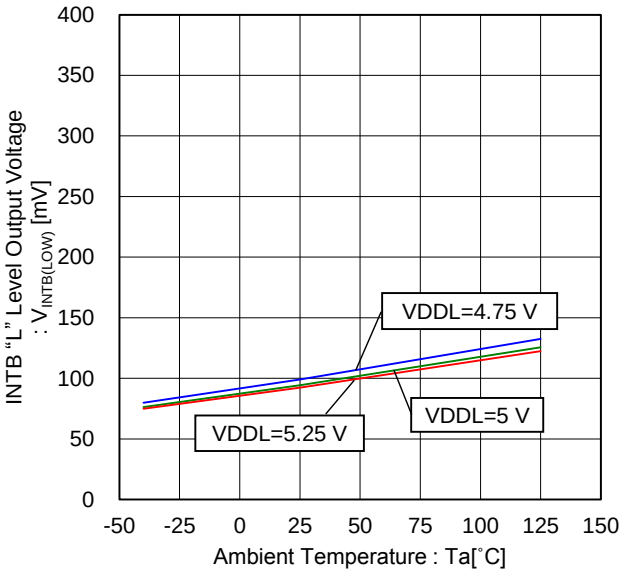


Figure 104. INTB "L" Level Output Voltage vs Ambient Temperature (I_{SINK}=1.0 mA)

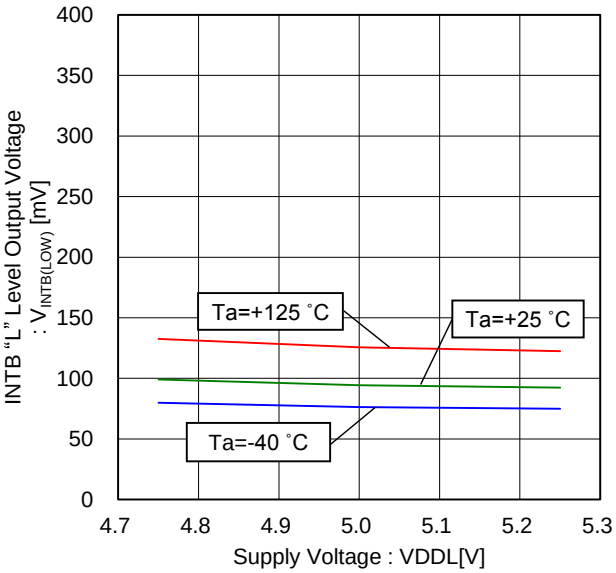


Figure 105. INTB "L" Level Output Voltage vs Supply Voltage (I_{SINK}=1.0 mA)

Typical Performance Curves - continued

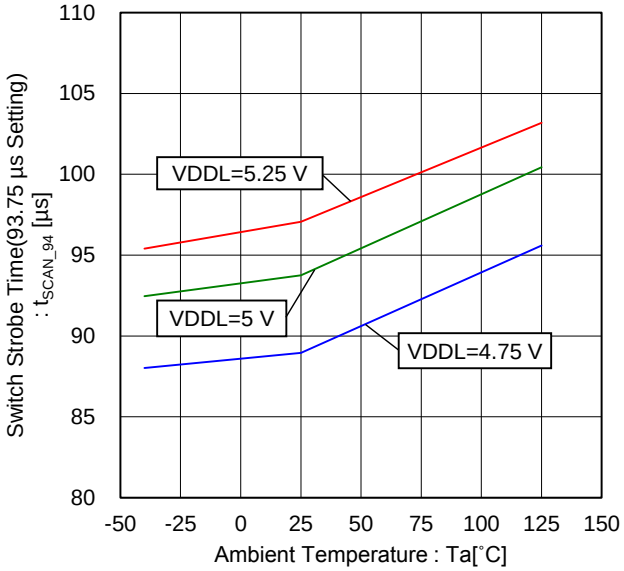


Figure 106. Switch Strobe Time vs Ambient Temperature (93.75 µs Setting)

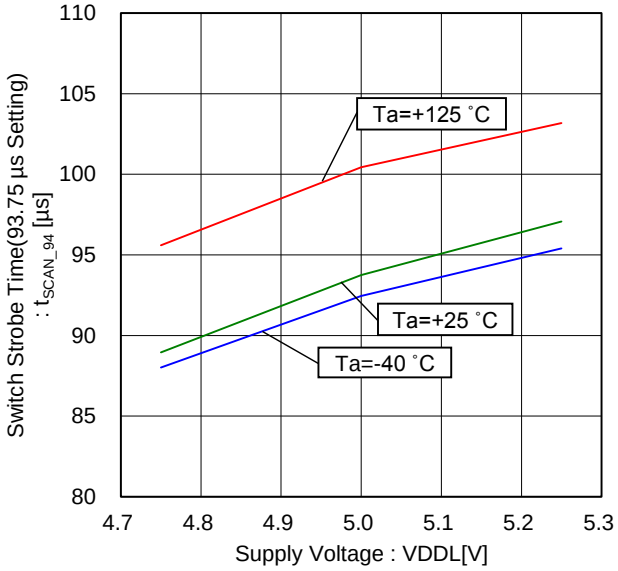


Figure 107. Switch Strobe Time vs Supply Voltage (93.75 µs Setting)

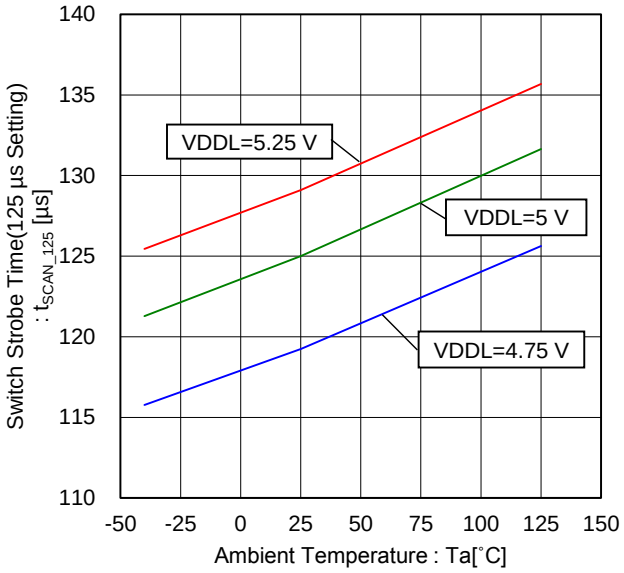


Figure 108. Switch Strobe Time vs Ambient Temperature (125 µs Setting)

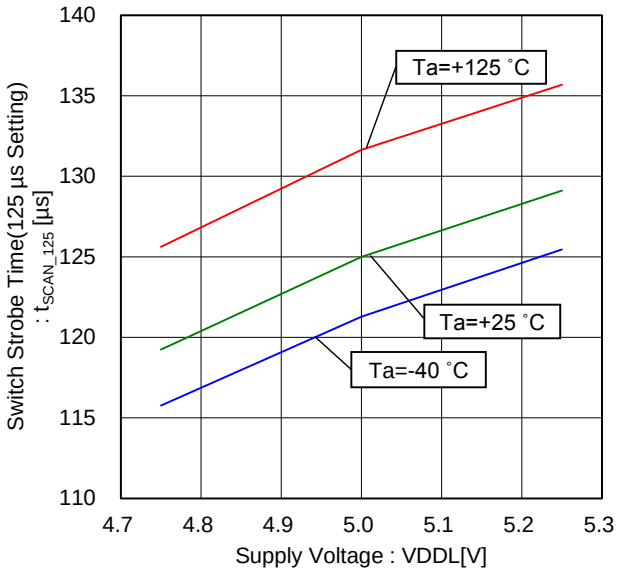


Figure 109. Switch Strobe Time vs Supply Voltage (125 µs Setting)

Typical Performance Curves - continued

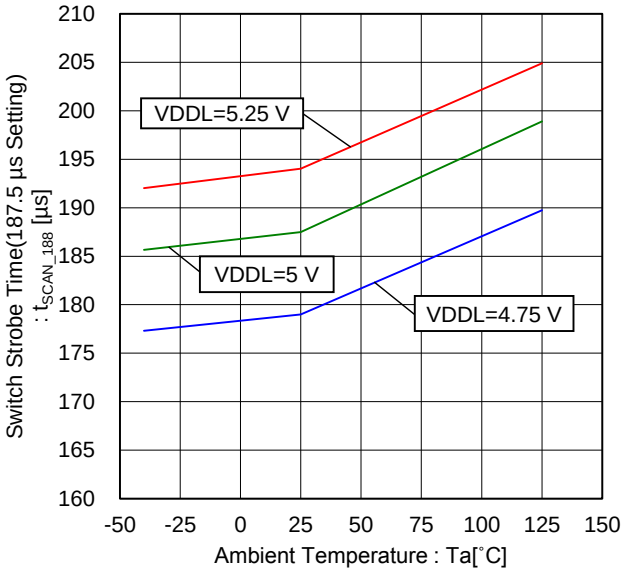


Figure 110. Switch Strobe Time vs Ambient Temperature (187.5 µs Setting)

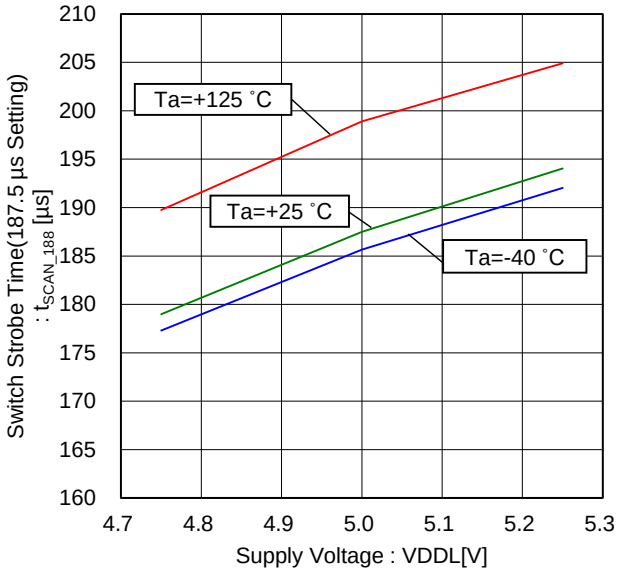


Figure 111. Switch Strobe Time vs Supply Voltage (187.5 µs Setting)

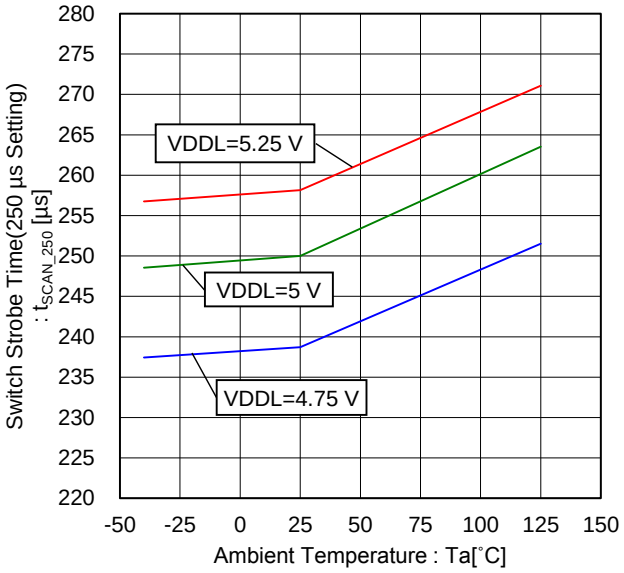


Figure 112. Switch Strobe Time vs Ambient Temperature (250 µs Setting)

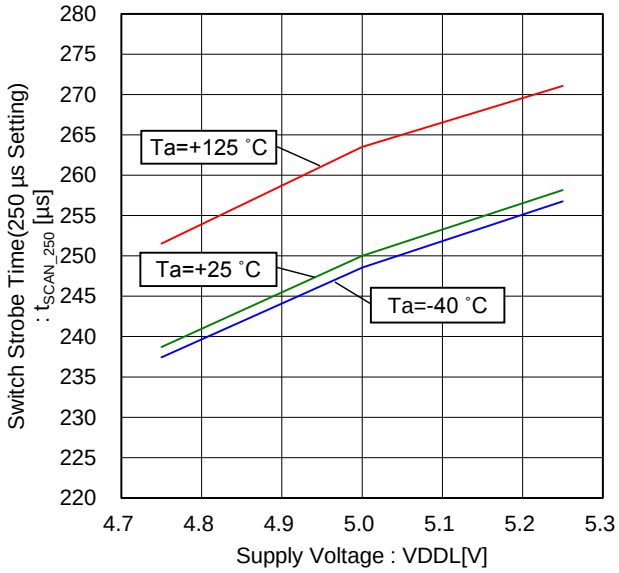


Figure 113. Switch Strobe Time vs Supply Voltage (250 µs Setting)

Typical Performance Curves - continued

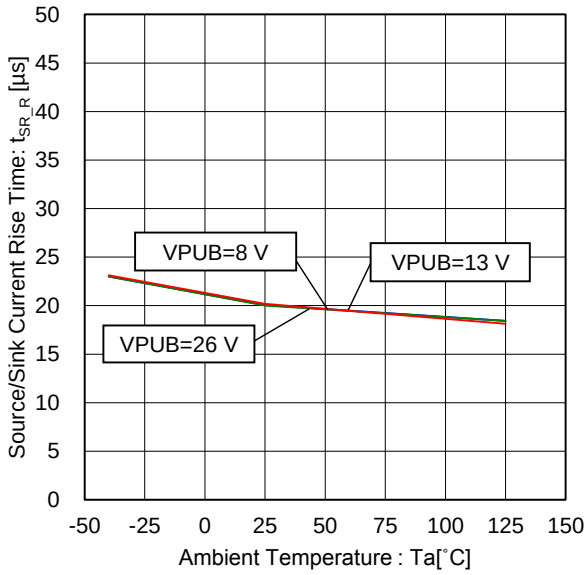


Figure 114. Source/Sink Current Rise Time vs Ambient Temperature (FSQ="0", FSQZ/A/B="0", 10 mA Setting, Load Resistance=100 Ω)

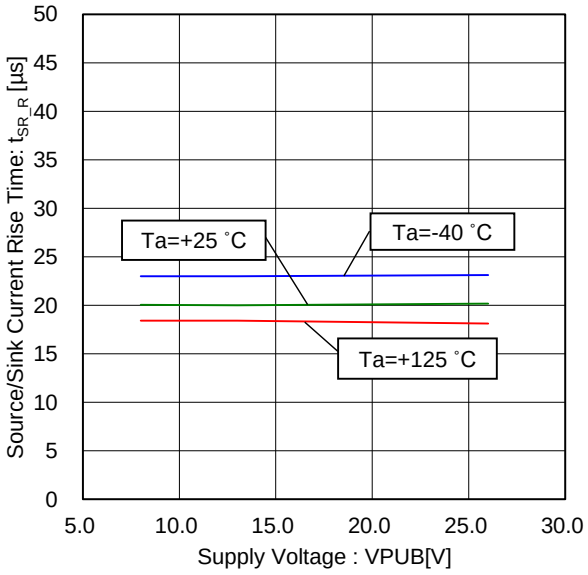


Figure 115. Source/Sink Current Rise Time vs Supply Voltage (FSQ="0", FSQZ/A/B="0", 10 mA Setting, Load Resistance=100 Ω)

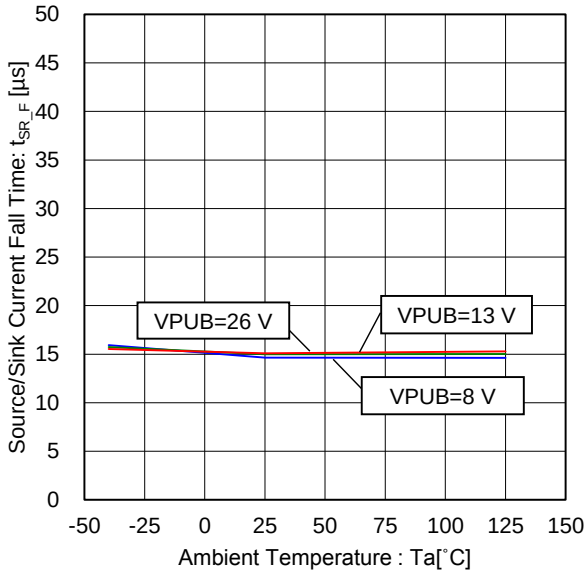


Figure 116. Source/Sink Current Fall Time vs Ambient Temperature (FSQ="0", FSQZ/A/B="0", 10 mA Setting, Load Resistance=100 Ω)

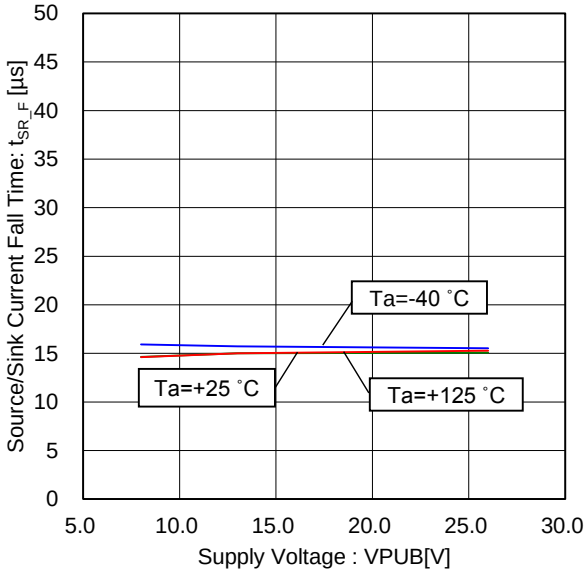


Figure 117. Source/Sink Current Fall Time vs Supply Voltage (FSQ="0", FSQZ/A/B="0", 10 mA Setting, Load Resistance=100 Ω)

Application Examples

1. Example of Application Circuit and its External Components

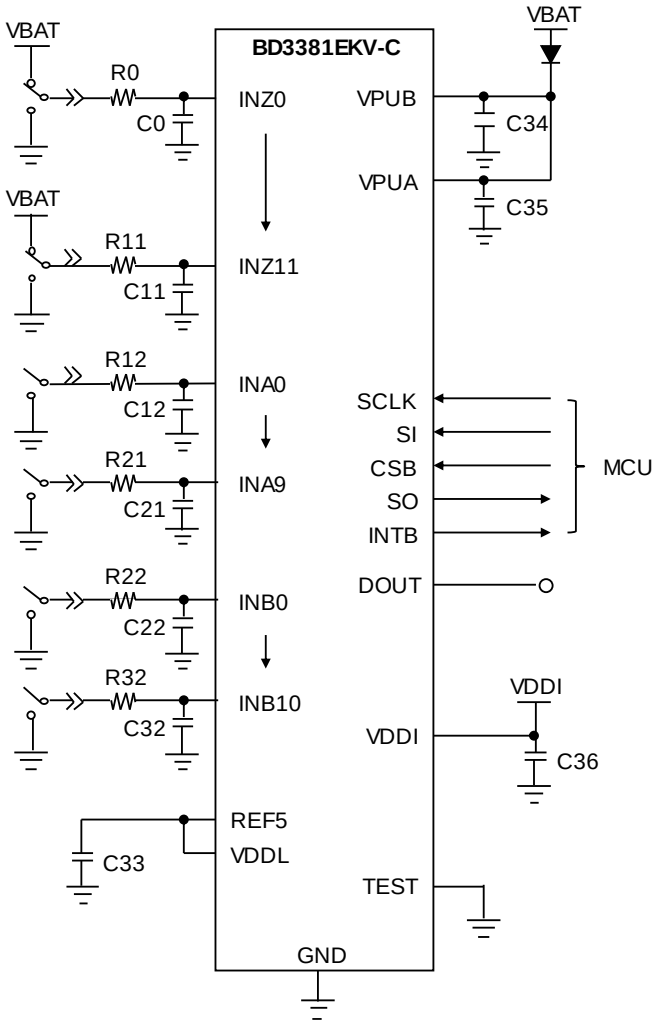


Figure 118. Example of Application Circuit and its External Components

·Capacitor (C34, C35, C36) at Power Supply Pins (VPUA, VPUB, VDDI)
Insert a 0.1 µF capacitor between each power supply pin (VPUA, VPUB, and VDDI) and ground. Make sure to design the external components with sufficient margin for the intended application. It is recommended to use capacitors with excellent voltage and temperature characteristics.

·Capacitor (C33) at REF5
In order to prevent oscillation, a capacitor needs to be placed between the REF5 output pin and ground. It is recommended to use a capacitor (electrolytic, tantalum, or ceramic of at least 4.7 µF). Make sure that capacitance of 4.7 µF or higher is maintained at the intended operating supply voltage and temperature range. Temperature change can cause fluctuation in capacitance, which may lead to oscillation. If a ceramic capacitor is chosen, it is recommended to use X5R, X7R, or any others with better temperature and DC biasing characteristics and higher voltage tolerance.

·Capacitor (C0 to C32) at Switch Pin (INZ, INA, INB)
It is recommended to use at least 0.1 µF capacitors as protection against ESD. Make sure to design the external circuit with sufficient margin for the intended application. Use capacitors with application specific voltage and temperature characteristics.

·Resistor (R0 to R32) at Switch Pin (INZ, INA, INB)
Choose the appropriate resistor to reduce EMI noise. Design the circuit so the pin voltage does not fall below the threshold voltage defined by ground float of [Load Resistance] x [Wetting Current] (when wetting current is set to source) or voltage drop (when wetting current is set to sink) may occur.

Application Examples - continued

2. Example of Parallel Connection Circuit

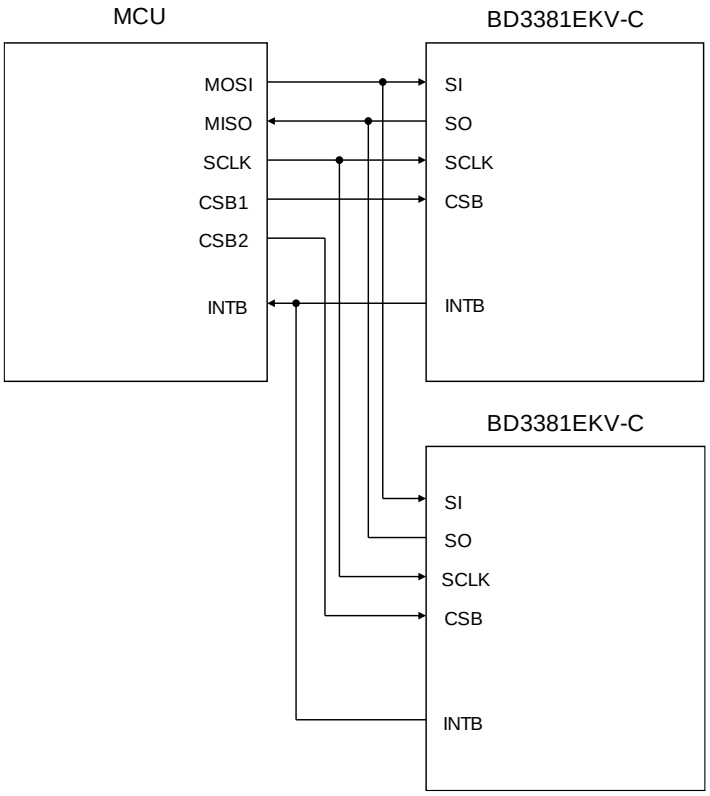
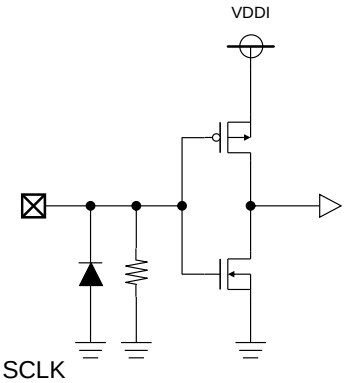
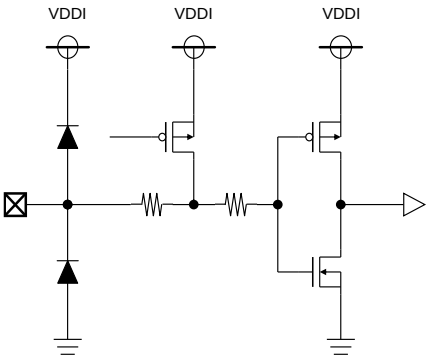
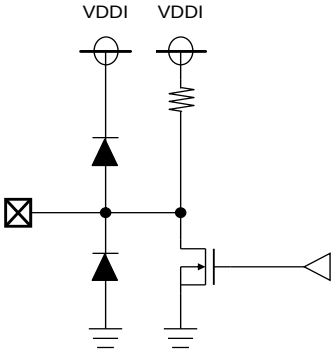
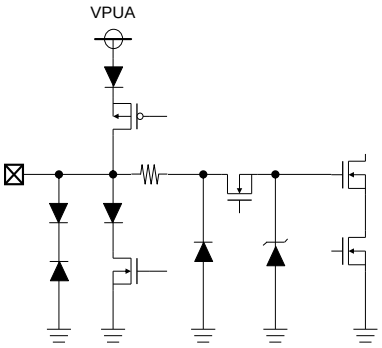
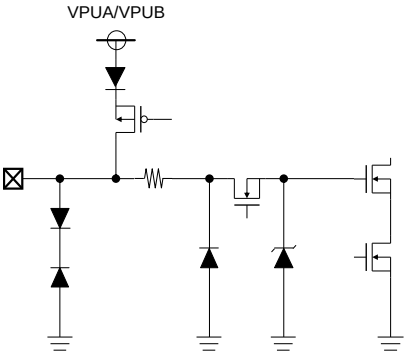
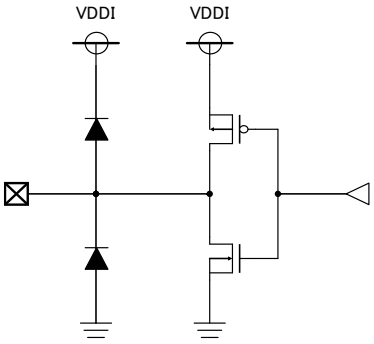
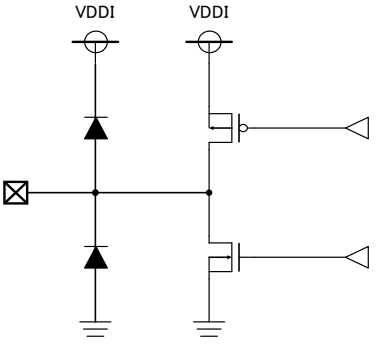
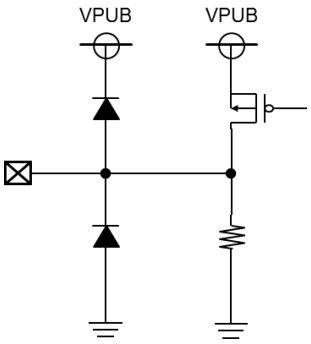


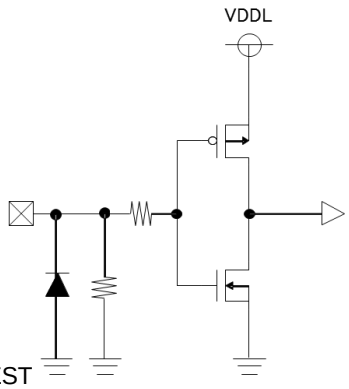
Figure 119. Example of Parallel Connection Circuit

·Parallel Connection
Prepare CSB pins respectively.

I / O Equivalence Circuit

Type	Equivalence circuit	Type	Equivalence circuit
A	 Input: SI, SCLK (with an internal pull-down resistor)	B	 Input: CSB (with an internal pull-up current source)
C	 Open-drain Interrupt Output: INTB (with an internal pull-up resistor)	D	 Switch Input: INZ0 to INZ11 (with an internal pull-up/pull-down current source)
E	 Switch Input: INA0 to INA9, INB0 to INB10 (with an internal pull-up current source)	F	 Output: DOUT
G	 Output: SO	H	 Output: REF5

I / O Equivalence Circuit - continued

Type	Equivalence circuit
I	 Input: TEST (with an internal pull-down resistor)

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes - continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

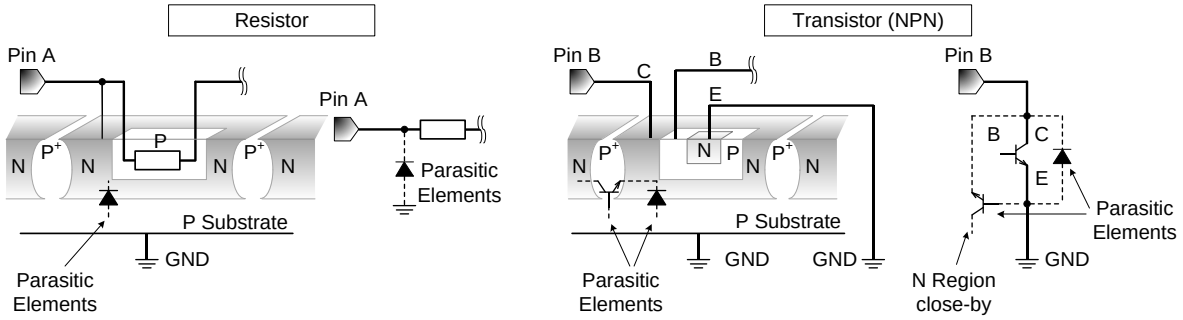


Figure 120. Example of monolithic IC structure

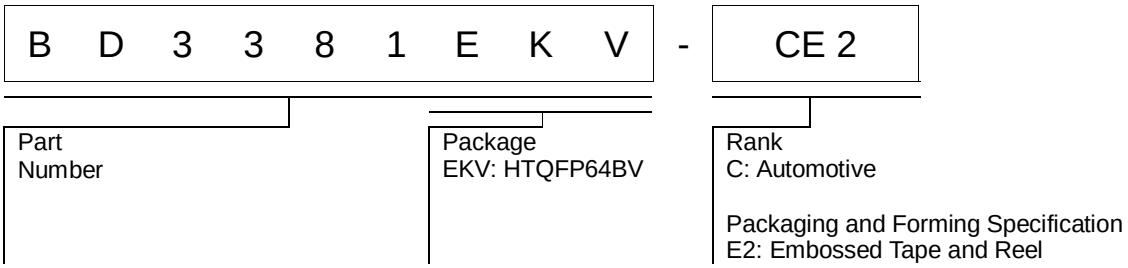
12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

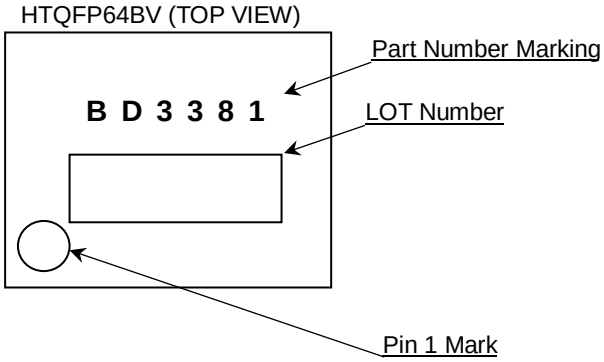
13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

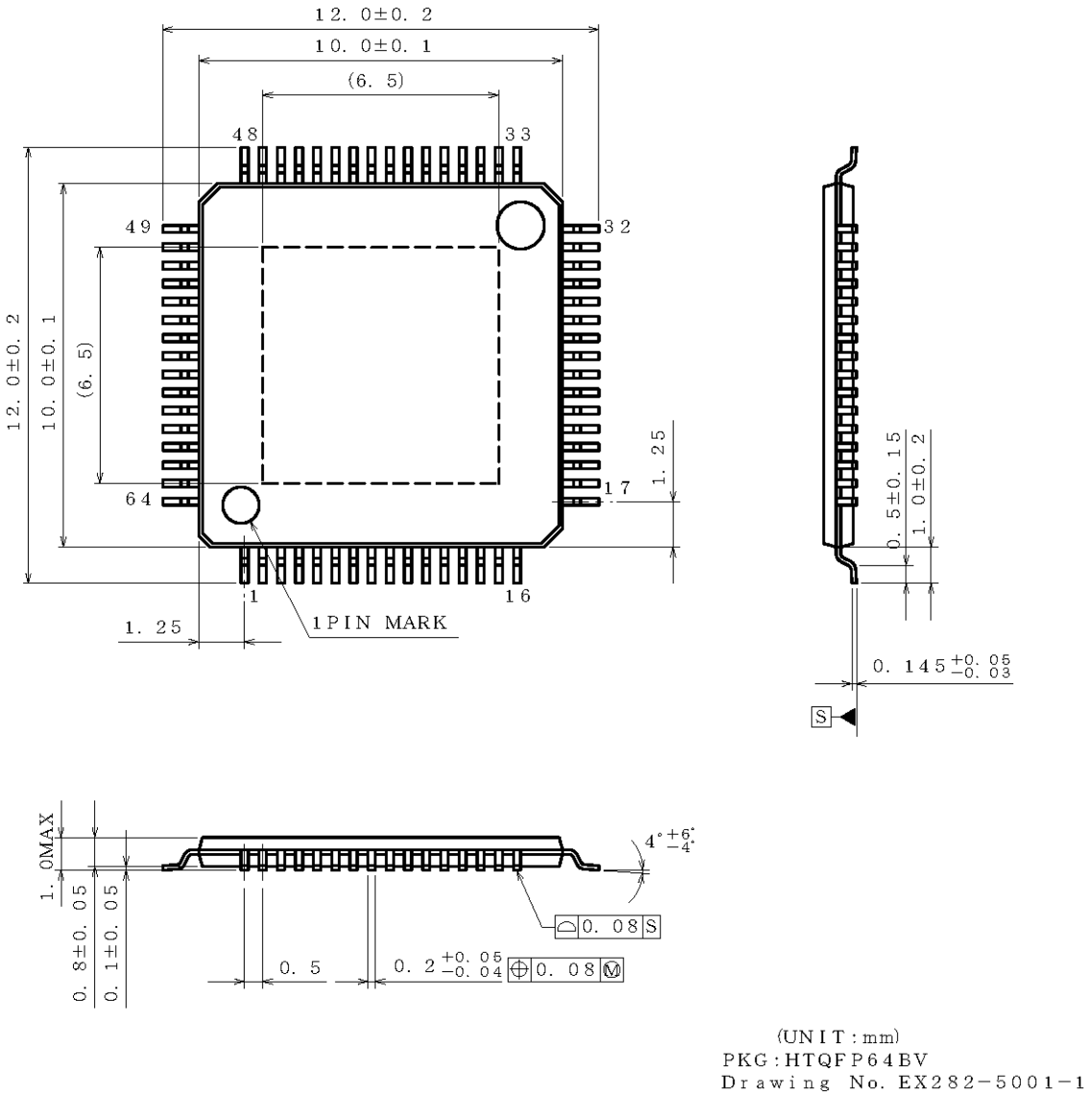


Marking Diagrams



Physical Dimension, Tape and Reel information

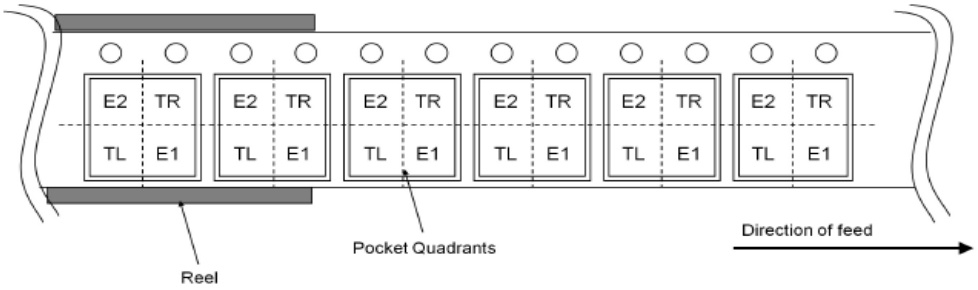
Package Name	HTQFP64BV



(UNIT:mm)
PKG:HTQFP64BV
Drawing No. EX282-5001-1

<Tape and Reel information>

Tape	**Embossed carrier tape (with dry pack)**
Quantity	**1000pcs**
Direction of feed	**E2** **(The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)**



Revision History

Date	Revision	Changes
09.Aug.2018	001	New release.

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JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
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   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

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7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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