Datasheet

Automotive 1.0 A LDO Regulator

BD33IC0MEFJ-C

General Description

BD33IC0MEFJ-C is a LDO regulator with output current 1.0 A. The output accuracy is ±3% between Ta = -40 °C to +125 °C. It has package type: HTSOP-J8 which is small and good heat resistance. Over current protection (for protecting the IC from destruction by output short circuit), circuit current ON/OFF switch (for setting the circuit 0 μA at shutdown mode), and thermal shutdown circuit (for protecting IC from heat destruction by over load condition) are all built in. It is usable for ceramic capacitor and enables to improve smaller set and long-life.

Key Specifications

- Input Power Supply Voltage Range: 2.4 V to 5.5 V
- Output Voltage: 3.3 V
- Output Current: 1.0 A (Max)
- Shutdown Current: 0 μA (Typ)
- Ambient Temperature Range Ta: -40 °C to +125 °C

Package

Package	W (Typ) x D (Typ) x H (Max)
HTSOP-J8	4.90 mm x 6.00 mm x 1.00 mm

Features

- AEC-Q100 Qualified(Note 1)
- High Accuracy Reference Voltage Circuit
- Built-in Over Current Protection Circuit (OCP)
- Built-in Thermal Shutdown Circuit (TSD)
- With Shutdown Switch

(Note 1) Grade1

Application

- Power Train
- Body
- Other Automotive Products

Typical Application Circuit

- Components Externally Connected
  Input Capacitor: 1.0 μF ≤ C_{IN} (Min)
  Output Capacitor: 1.0 μF ≤ C_O (Min)(Note 2)

(Note 2) Electrolytic, tantalum and ceramic capacitors can be used.

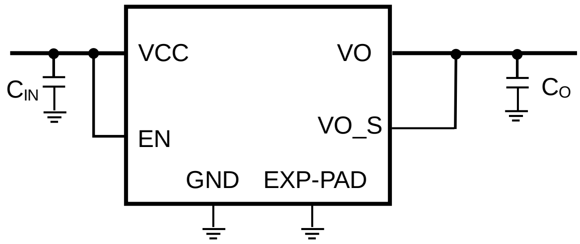


Figure 1

〇Product structure : Silicon integrated circuit 〇This product has no designed protection against radioactive rays

Contents

Pin Configuration

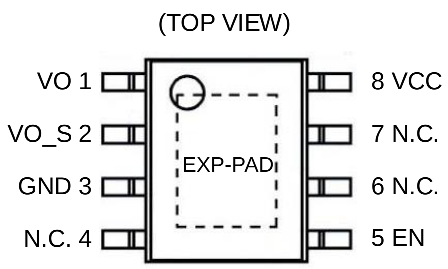


Figure 2

Pin Description

Pin No.	Pin Name	Function	Descriptions
1	VO	Output pin	This pin generate 3.3 V output. It is necessary to use a capacitor with a capacitance of 1.0 μF (Min) or higher between the VO pin and GND. The detail of a selection is described in page 17.
2	VO_S	Output sense pin	This pin monitors output voltage. VO_S should be connected to VO.
3	GND	GND pin	Ground
4	N.C.	Non Connection	N.C. pin can be opened or connected to GND, because it isn't connected it inside of IC.
5	EN	Enable pin	Enable the device with high input over the threshold. Disable the device with low input under the threshold.
6	N.C.	Non Connection	N.C. pin can be opened or connected to GND, because it isn't connected it inside of IC.
7	N.C.	Non Connection	N.C. pin can be opened or connected to GND, because it isn't connected it inside of IC.
8	VCC	Input pin	Input power supply voltage It is necessary to use a capacitor with a capacitance of 1.0 μF (Min) or higher between the VCC pin and GND. The detail of a selection is described in page 17. If the inductance of power supply line is high, please adjust input capacitor value.
Reverse	EXP-PAD	GND	Ground and Heat Sink This pin should be connected to Analog ground/Power ground.

Block Diagram

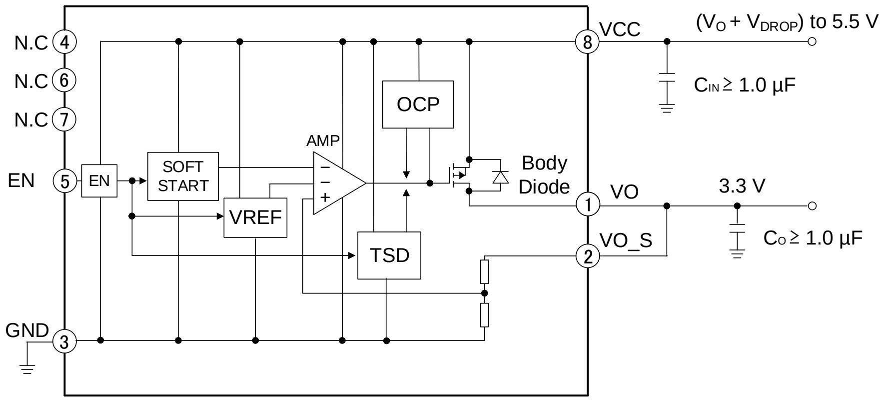


Figure 3

Description of Blocks

Block Name	Function	Description of Blocks
EN	Control Output Voltage ON / OFF	A logical "HIGH" (V_{EN} ≥ 2.4 V) at the EN enables the device and "LOW" (V_{EN} ≤ 0.8 V) at the EN disables the device.
TSD	Thermal Shutdown Protection	To protect the device from overheating. If the chip temperature (Tj) reaches 177 °C (Typ), the output is turned off.
VREF	Reference Voltage	Generate the Reference Voltage
AMP	Error Amplifier	The Error Amplifier amplifies the difference between the output voltage and the reference voltage and drive the Output MOSFET (Power Tr.)
SOFT START	Soft Start	Output voltage rises slowly to reduce overshoot and rash current. Output rise time is 800 µs (Typ).
OCP	Over Current Protection	To protect the device from damage caused by over current such as output short. If the output current reaches 2.3 A (Typ), the output current is limited.

Absolute Maximum Ratings

Parameter	Symbol	Limits	Unit
Power Supply Voltage(Note 1)	V_{CC}	-0.3 to +7.0	V
EN Voltage(Note 2)	V_{EN}	-0.3 to +7.0	V
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	+150	°C
ESD Withstand Voltage (HBM)(Note 3)	V_{ESD_HBM}	±2000	V
ESD Withstand Voltage (CDM)(Note 4)	V_{ESD_CDM}	±750	V

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance and power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

(Note 1) Not to exceed Tjmax
(Note 2) The start-up orders of power supply (V_{CC}) and the V_{EN} do not influence if the voltage is within the operation power supply voltage range.
(Note 3) ESD susceptibility Human Body Model "HBM"; base on ANSI/ESDA/JEDEC JS001 (1.5 kΩ, 100 pF).
(Note 4) ESD susceptibility Charged Device Model "CDM"; base on JEDEC JESD22-C101.

Operating Ratings

Parameter	Symbol	Min	Max	Unit	Conditions
Start-up Power Supply Voltage	V_{CC}	2.4	-	V	-
Input Power Supply Voltage	V_{CC}	4.1	5.5	V	I_O = 1 A
Operating Temperature	Ta	-40	+125	°C	-
EN Voltage	V_{EN}	0.0	5.5	V	-
Output Current	I_O	0.0	1.0	A	-
Input Capacitor(Note 5)	C_{IN}	1.0	-	µF	Ceramic Capacitor
Output Capacitor(Note 5)	C_O	1.0	-	µF	Ceramic Capacitor
Equivalent Series Resistance	ESR(C_O)	-	7	Ω	Output Capacitor

(Note 5) Set the value of the capacitor so that it does not fall below the minimum value.
Take into consideration the temperature characteristics, DC device characteristics and degradation with time.

Electrical Characteristics (Unless otherwise noted, Ta = -40 °C to +125 °C, V_{EN} = 3 V, V_{CC} = 5.0 V)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
Shutdown Current	I_{SD}	-	0	5	µA	V_{EN} = 0 V, OFF mode
Bias Current	I_{CC}	-	400	700	µA	-
Line Regulation	Reg.I	-	25	50	mV	V_{CC} = (V_O + 0.6 V) to 5.5 V
Load Regulation	Reg.I_O	-	25	75	mV	I_O = 0 A to 1 A
Dropout Voltage	V_{DROP}	-	0.40	0.90	V	V_{CC} = 3.3 V, I_O = 1 A
Output Voltage	V_O	3.201	3.300	3.399	V	I_O = 0 mA
EN Low Voltage	V_{EN}(Low)	0	-	0.8	V	-
EN High Voltage	V_{EN}(High)	2.4	-	5.5	V	-
EN Bias Current	I_{EN}	-	3	9	µA	-

Thermal Resistance(Note 1)

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 3)	2s2p(Note 4)	
HTSOP-J8				
Junction to Ambient	θ_{JA}	206.4	45.2	°C/W
Junction to Top Characterization Parameter(Note 2)	Ψ_{JT}	21	13	°C/W

(Note 1) Based on JESD51-2A(Still-Air).
(Note 2) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 3) Using a PCB board based on JESD51-3.
(Note 4) Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3 mm x 76.2 mm x 1.57 mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70 μm

Layer Number of Measurement Board	Material	Board Size	Thermal Via(Note 5)	
			Pitch	Diameter
4 Layers	FR-4	114.3 mm x 76.2 mm x 1.6 mmt	1.20 mm	Φ0.30 mm

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μm	74.2 mm x 74.2 mm	35 μm	74.2 mm x 74.2 mm	70 μm

(Note 5) This thermal via connects with the copper pattern of all layers.

Typical Performance Curves

(Unless otherwise noted, V_{EN} = 3 V, V_{CC} = 5.0 V, C_{IN} = C_O = 1 µF)

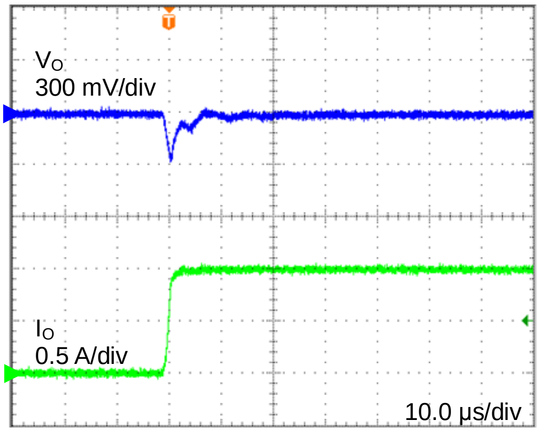


Figure 4. Transient Response
(1 mA→1000 mA, Ta = -40 °C)

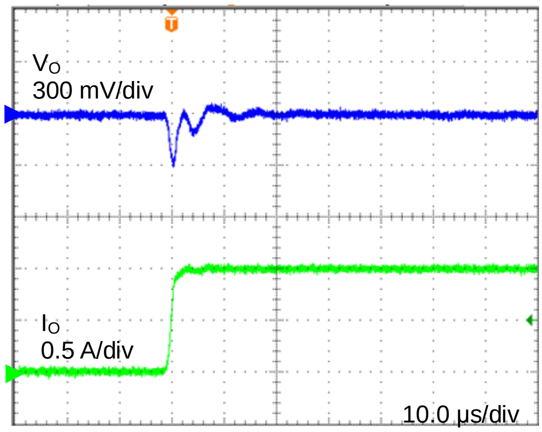


Figure 5. Transient Response
(1 mA→1000 mA, Ta = +25 °C)

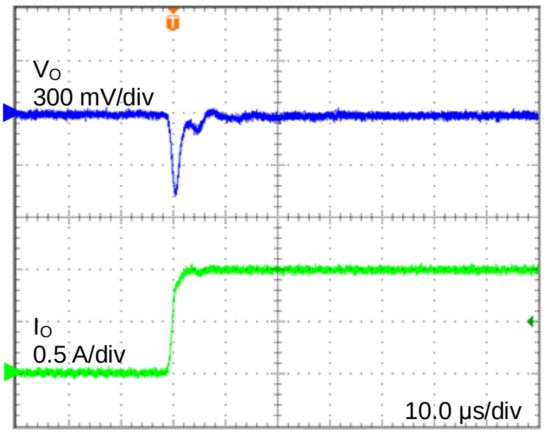


Figure 6. Transient Response
(1 mA→1000 mA, Ta = +125 °C)

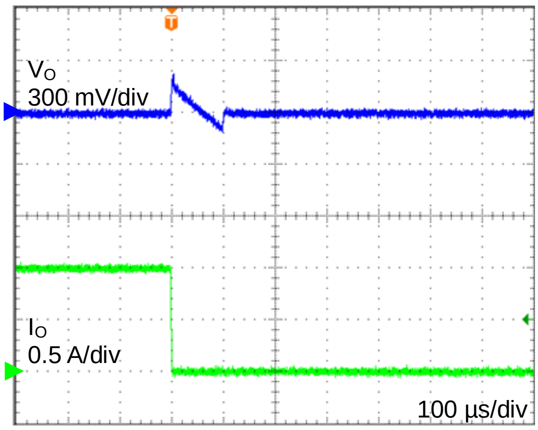


Figure 7. Transient Response
(1000 mA→1 mA, Ta = -40 °C)

Typical Performance Curves - continued

(Unless otherwise noted, V_{EN} = 3 V, V_{CC} = 5.0 V, C_{IN} = C_O = 1 µF)

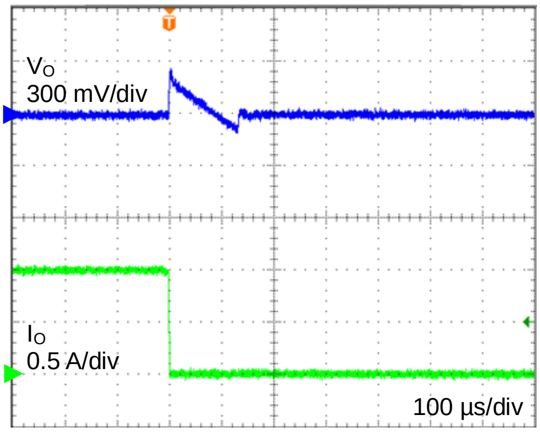


Figure 8. Transient Response
(1000 mA→1 mA, Ta = +25 °C)

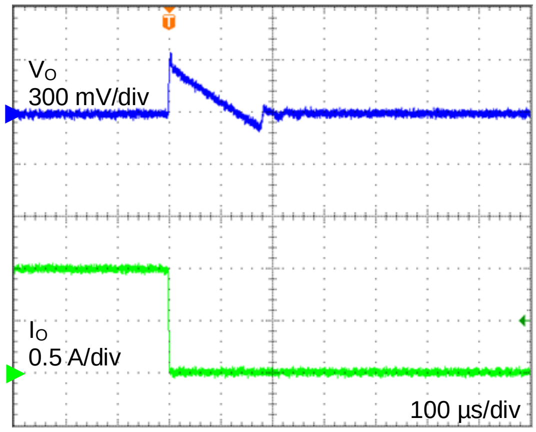


Figure 9. Transient Response
(1000 mA→1 mA, Ta = +125 °C)

Typical Performance Curves - continued

(Unless otherwise noted, V_{EN} = 3 V, V_{CC} = 5.0 V, C_{IN} = C_O = 1 µF)

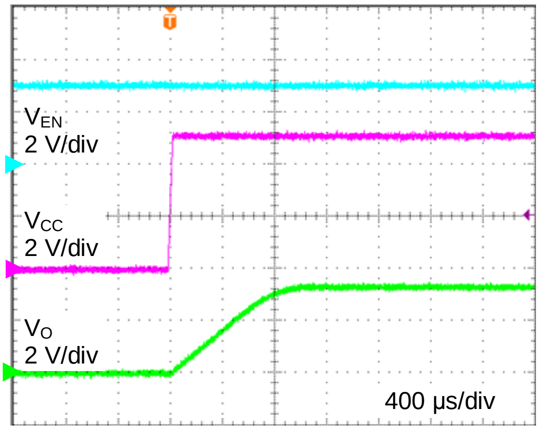


Figure 10. VCC Rise Response
(Ta = -40 °C)

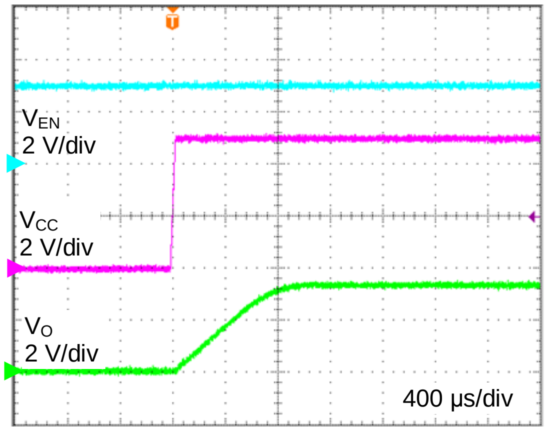


Figure 11. VCC Rise Response
(Ta = +25 °C)

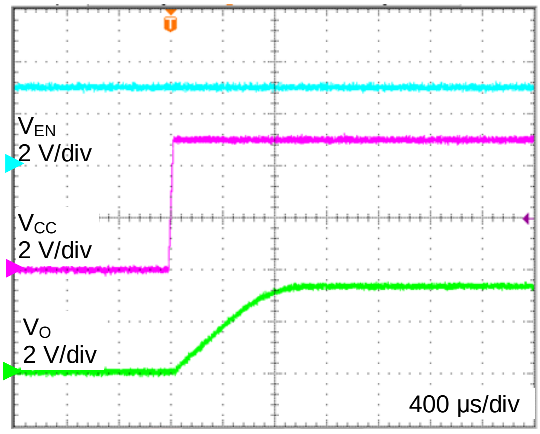


Figure 12. VCC Rise Response
(Ta = +125 °C)

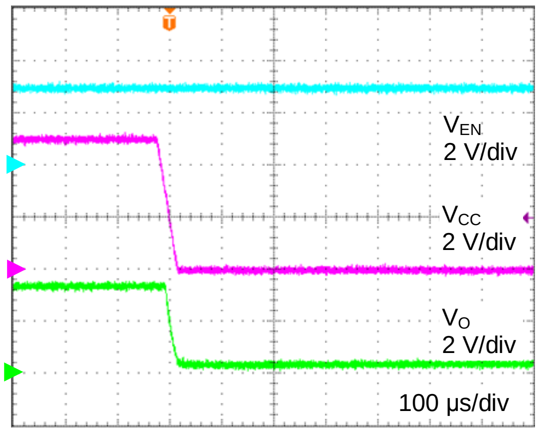


Figure 13. VCC Fall Response
(Ta = -40 °C)

Typical Performance Curves - continued

(Unless otherwise noted, V_{EN} = 3 V, V_{CC} = 5.0 V, C_{IN} = C_O = 1 µF)

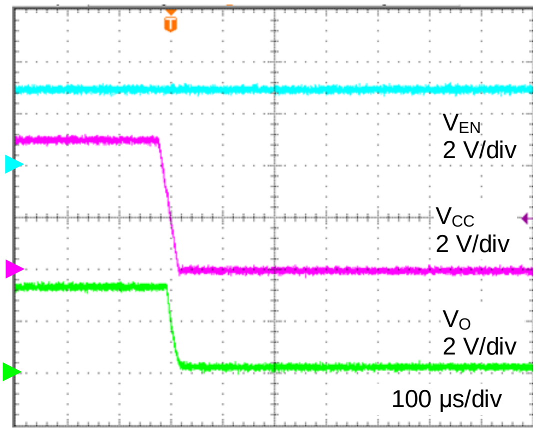


Figure 14. VCC Fall Response
(Ta = +25 °C)

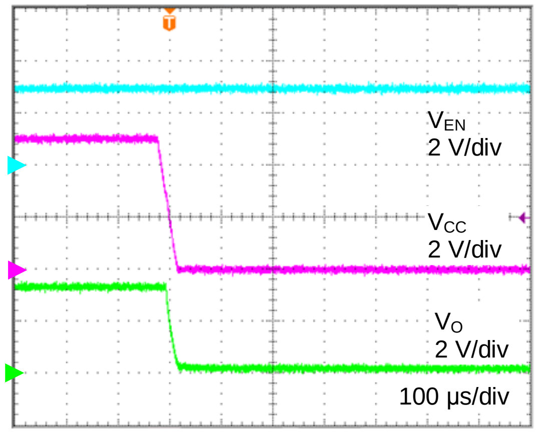


Figure 15. VCC Fall Response
(Ta = +125 °C)

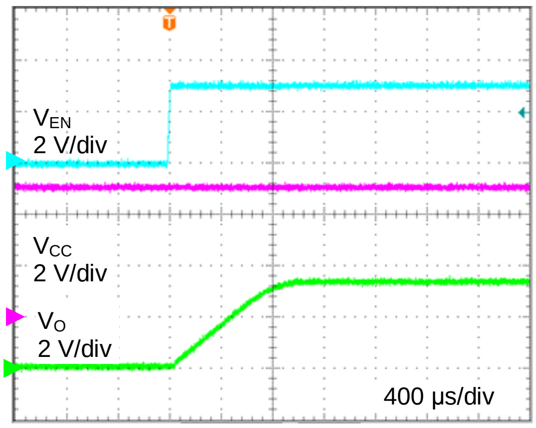


Figure 16. EN Rise Response
(Ta = -40 °C)

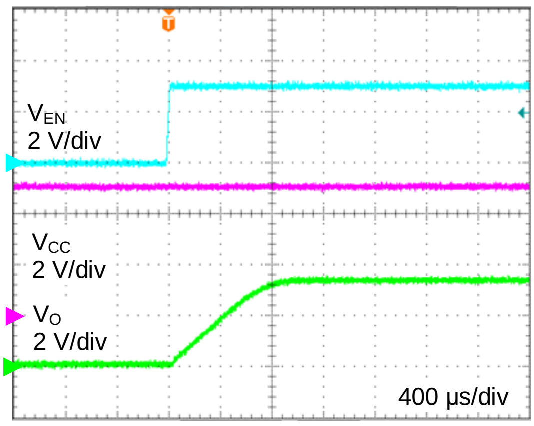


Figure 17. EN Rise Response
(Ta = +25 °C)

Typical Performance Curves - continued

(Unless otherwise noted, V_{EN} = 3 V, V_{CC} = 5.0 V, C_{IN} = C_O = 1 µF)

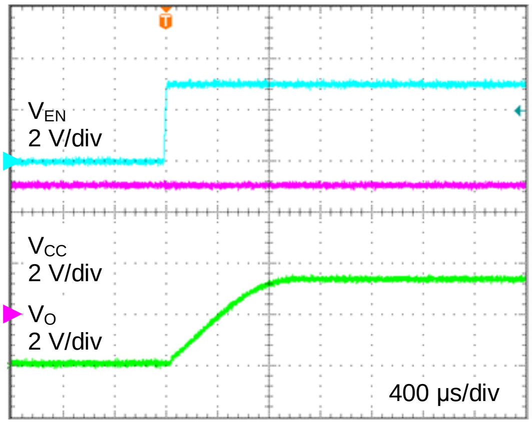


Figure 18. EN Rise Response
(Ta = +125 °C)

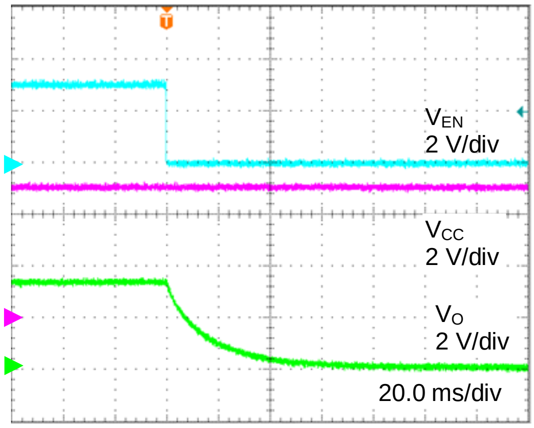


Figure 19. EN Fall Response
(Ta = -40 °C)

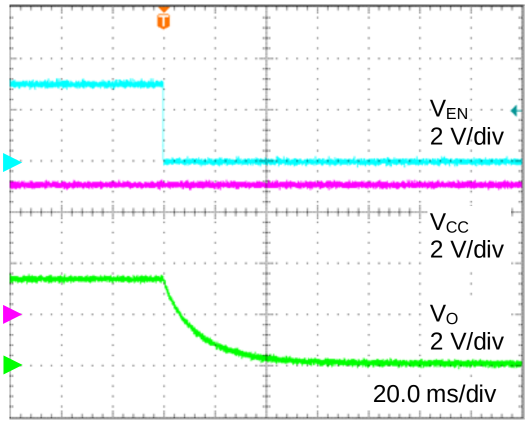


Figure 20. EN Fall Response
(Ta = +25 °C)

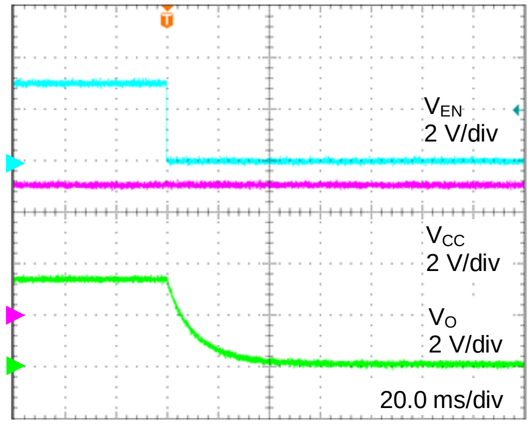


Figure 21. EN Fall Response
(Ta = +125 °C)

Typical Performance Curves - continued
(Unless otherwise noted, V_{EN} = 3 V, V_{CC} = 5.0 V, C_{IN} = C_O = 1 µF)

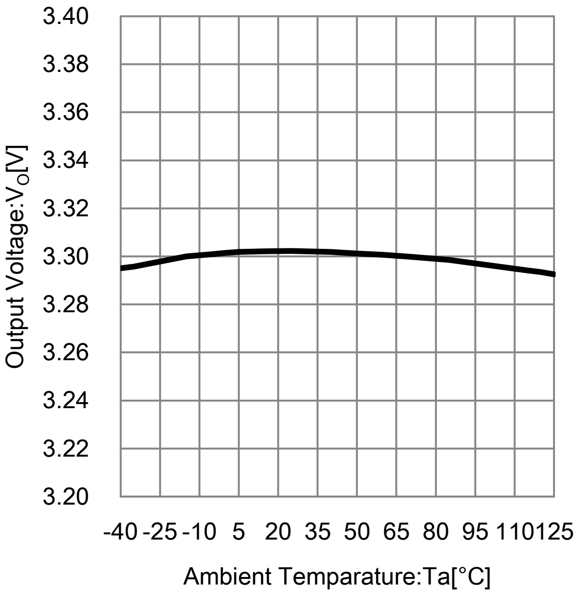


Figure 22. Output Voltage vs Ambient Temparature
(I_O = 0 mA)

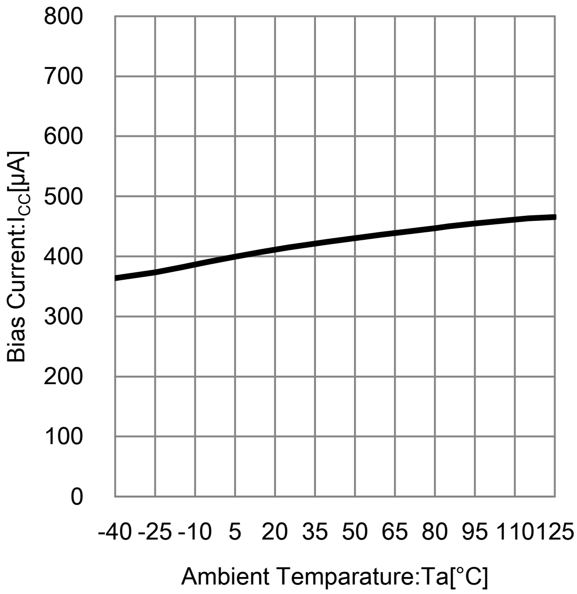


Figure 23. Bias Current vs Ambient Temparature

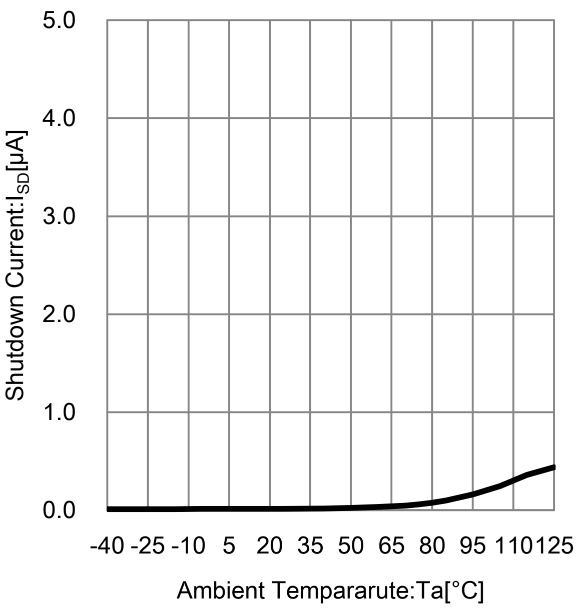


Figure 24. Shutdown Current vs Ambient Temparature

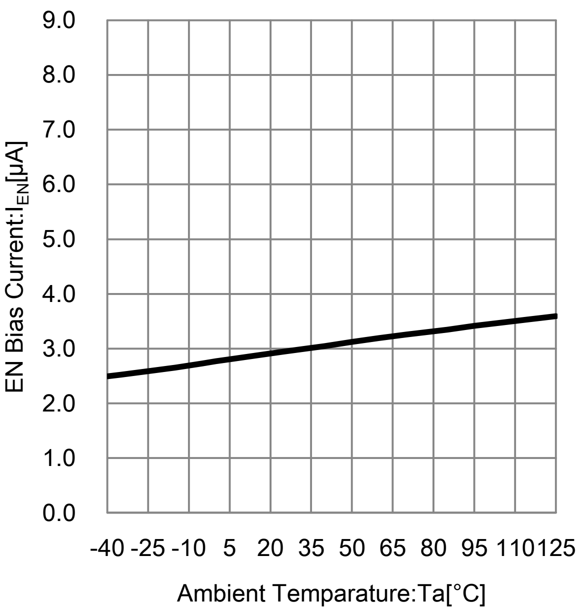


Figure 25. EN Bias Current vs Ambient Temparature

Typical Performance Curves - continued

(Unless otherwise noted, V_{EN} = 3 V, V_{CC} = 5.0 V, C_{IN} = C_O = 1 µF)

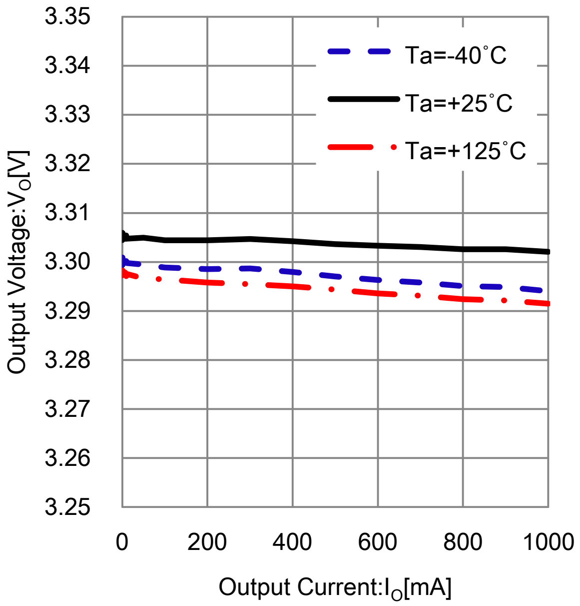


Figure 26. Output Voltage vs Output Current

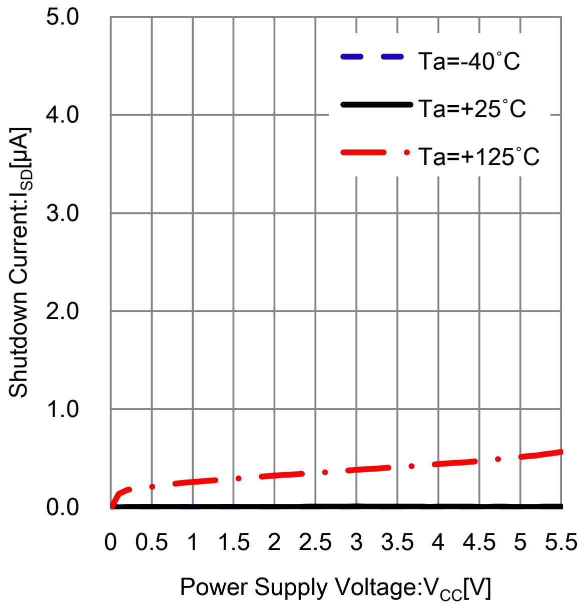


Figure 27. Shutdown Current vs Power Supply Voltage

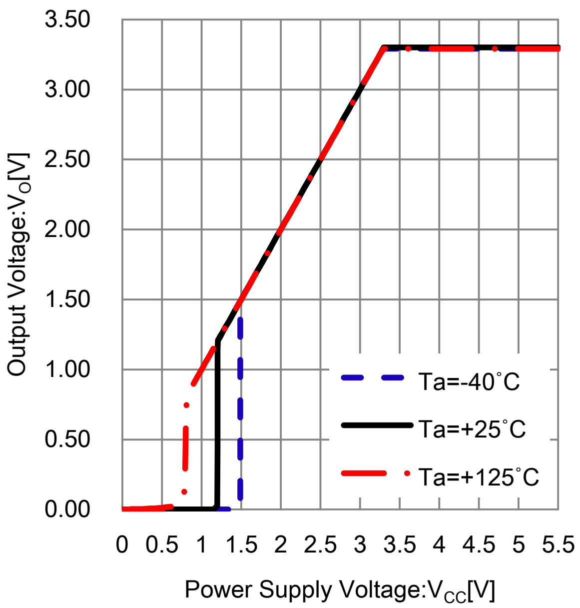


Figure 28. Output Voltage vs Power Supply Voltage

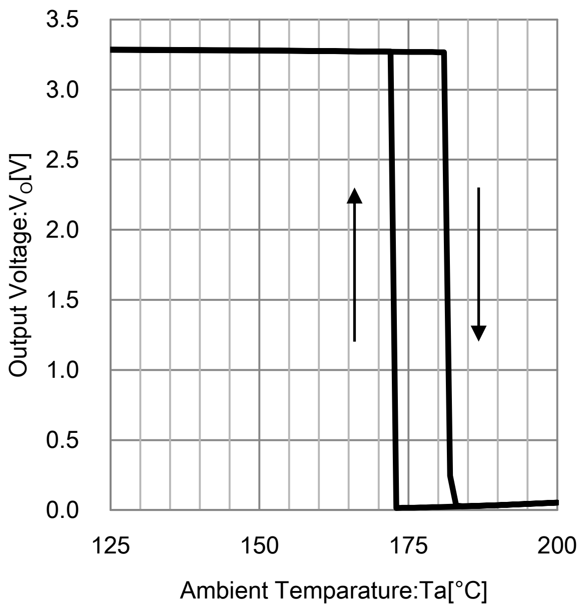


Figure 29. Output Voltage vs Ambient Temperature

Typical Performance Curves - continued

(Unless otherwise noted, V_{EN} = 3 V, V_{CC} = 5.0 V, C_{IN} = C_O = 1 µF)

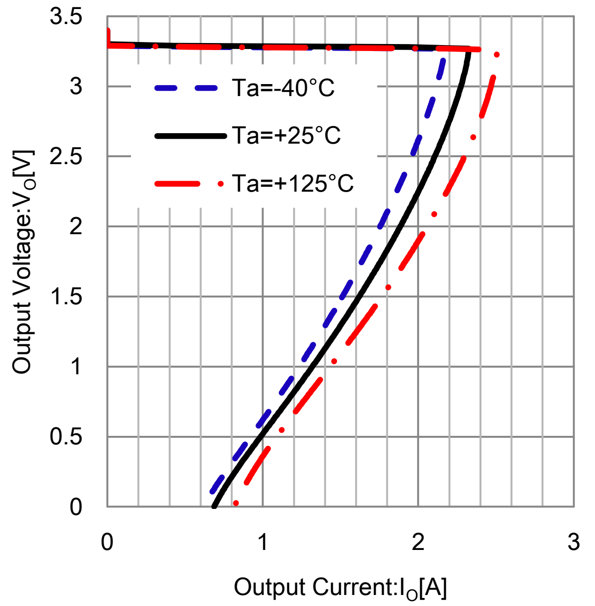


Figure 30. Output Voltage vs Output Current

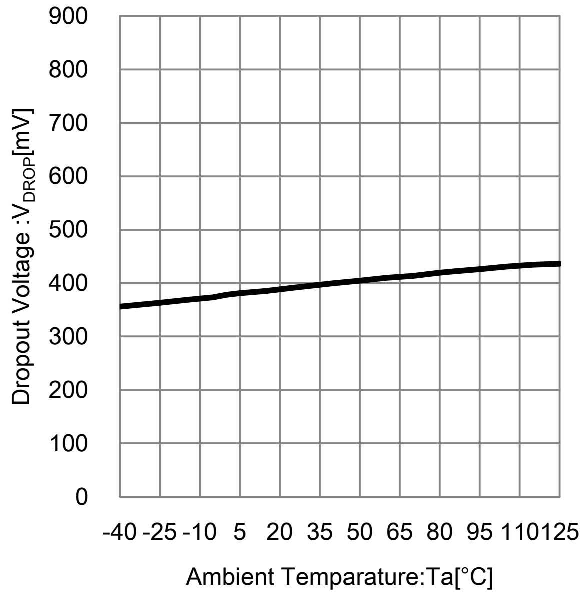


Figure 31. Dropout Voltage vs Ambient Temperature
(V_{CC} = 5 V, V_{O_S} = 0 V, I_O = 1 A)

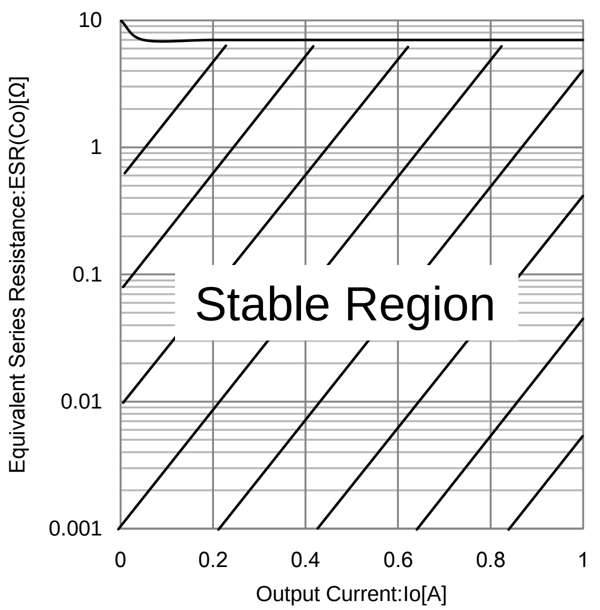


Figure 32. Equivalent Series Resistance vs Output Current
[-40 °C ≤ Ta ≤ +125 °C, (V_O + V_{DROP}) ≤ V_{CC} ≤ 5.5 V]

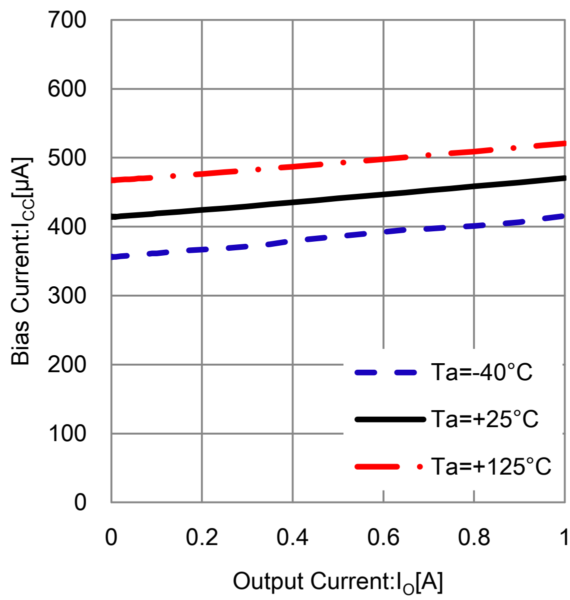


Figure 33. Bias Current vs Output Current

Typical Performance Curves - continued

(Unless otherwise noted, V_{EN} = 3 V, V_{CC} = 5.0 V, C_{IN} = C_O = 1 µF)

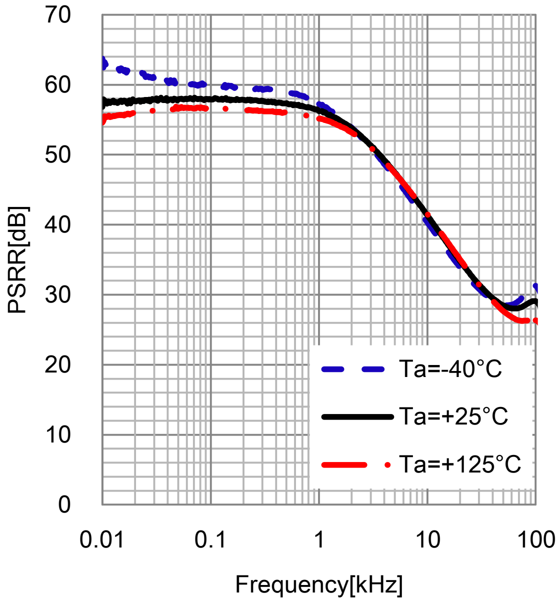


Figure 34. PSRR vs Frequency
(ein = 50 mVpp, Io = 100 mA, Co = 1 µF)

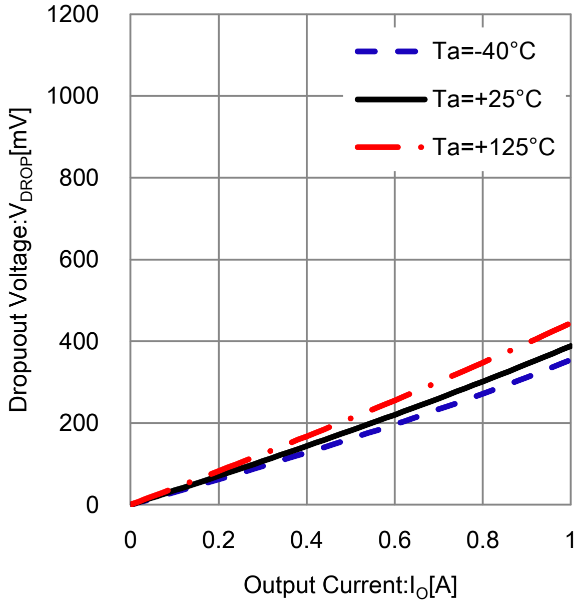


Figure 35. Dropout Voltage vs Output Current
(V_{CC} = 3.3 V, V_{O_S} = 0 V)

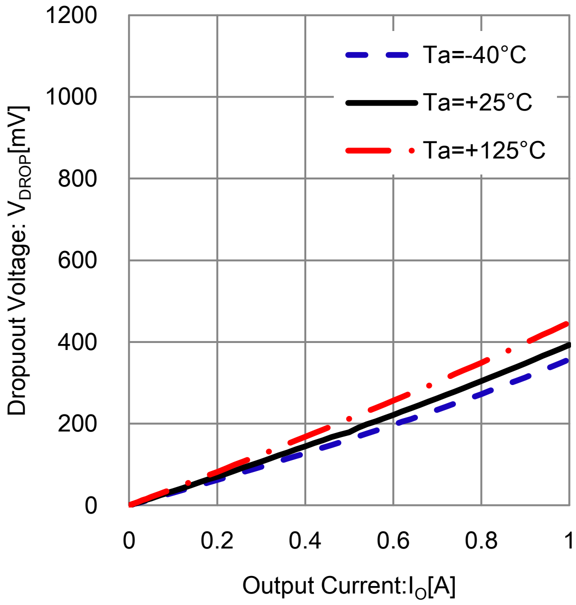


Figure 36. Dropout Voltage vs Output Current
(V_{CC} = 4.0 V, V_{O_S} = 0 V)

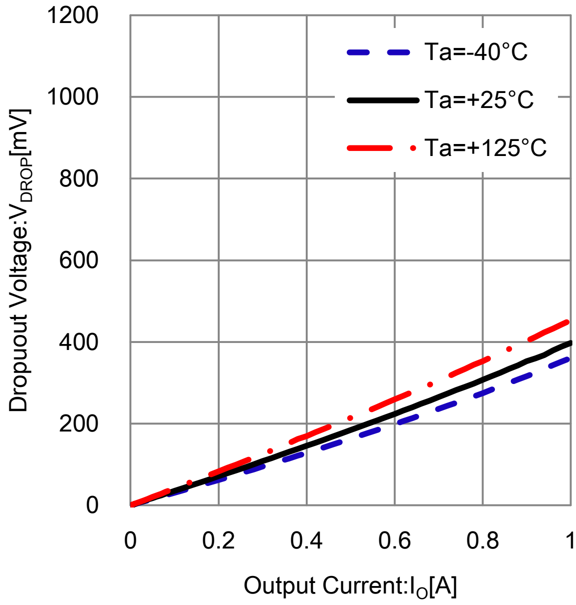


Figure 37. Dropout Voltage vs Output Current
(V_{CC} = 5.5 V, V_{O_S} = 0 V)

Power Dissipation

■HTSOP-J8

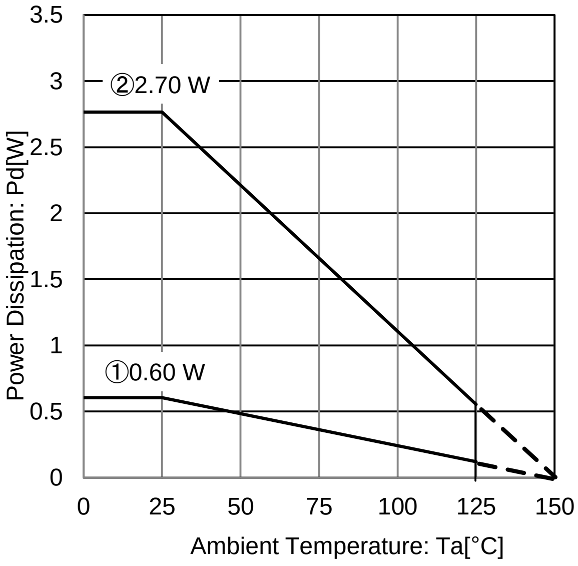


Figure 38. HTSOP-J8 Power Dissipation Graph
(Reference Data)

IC mounted on ROHM standard board based on JEDEC.
1: 1-layer PCB
(Copper foil area on the reverse side of PCB: 0 mm × 0 mm)
Board material: FR4
Board size: 114.3 mm × 76.2 mm × 1.57 mmt
Top copper foil: ROHM recommended footprint
+ wiring to measure, 2 oz. copper.

2: 4-layer PCB
(Copper foil area on the reverse side of PCB: 74.2 mm × 74.2 mm)
Board material: FR4
Board size: 114.3 mm × 76.2 mm × 1.60 mmt
Top copper foil: ROHM recommended footprint
+ wiring to measure, 2 oz. copper.
2 inner layers copper foil area of PCB:
74.2 mm × 74.2 mm, 1 oz. copper.
Copper foil area on the reverse side of PCB:
74.2 mm × 74.2 mm, 2 oz. copper.

Condition 1: θ_{JA} = 206.4 °C/W, Ψ_{JT} (top center) = 21 °C/W
Condition 2: θ_{JA} = 45.2 °C/W, Ψ_{JT} (top center) = 13 °C/W

Application and Implementation

Notice: The following information is provided only as reference for application and implementation, and does not guarantee its operation on specific function, accuracy or the external components in the application. On application, after a thorough confirmation such as characteristics of the capacitor, conduct the appropriate verification necessary in the actual application and design with sufficient margin.

Selection of External Components

Input Pin Capacitor

When battery is distant or when input-side impedance is high, a high capacitance capacitor is required to prevent line voltage drop. Select an input pin capacitor depending on the line impedance between power supply smoothing circuit and the input pin. In this case, although the capacitance value setting will vary according to application, in general a capacitor with capacitance value of 1.0 µF (Min) is recommended.

In addition, to prevent influence to the regulator characteristic from the external capacitor character variation, all input pin capacitor mentioned above is recommended to have good DC bias characteristics and temperature characteristics (approximately ±15%) with superior EIA standard high voltage breakdown. Mounting layout is recommended to be near the input pin as much as possible and capacitor shall be on identical mounting side.

Output Pin Capacitor

In order to stabilize the operation of the regulator, capacitor with capacitance value ≥ 1.0 µF (Min) and ESR up to 7 Ω (Max) must be inserted between output pin and GND pin for oscillation prevention.
Select an appropriate output pin capacitance value and ESR to improve the transient response of the regulator and the stability of control loop. The correlation of output capacitance value and ESR is as shown in the graph on the Figure 32 (ESR stability region). As described in the graph, this product is designed to achieve a stable regulator operation with capacitance value from 1.0 µF and with ESR value approximately within 7 Ω. (frequency bandwidth within approximately 10 kHz to 100 kHz range).

Provided however, the stable domain of this graph is based on the measurement result from single IC on our board with resistive load. In the actual environment, stability is affected by wire impedance on the board, input power supply impedance and load impedance, therefore we strongly recommend thorough verification in the actual usage environment.

For input voltage fluctuation or load fluctuation in frequency domain which is beyond regulator control loop responsiveness, responsiveness in this case generally depends on capacitance value of the output pin capacitor. Therefore, capacitance value of 1.0 µF (Min) or more for output pin capacitor is recommended. By insertion of bigger capacitance value, further improvement of responsiveness in a high frequency domain is expected. Various types of capacitors can be used for this high capacity output pin capacitor which includes electrolytic capacitor, electro-conductive polymer capacitor and tantalum capacitor. Provided however, depending on the type of capacitor, ESR (≤ 7 Ω) absolute value range, increase of ESR value and decrease of capacitance value in lower temperature needs to be taken into consideration.

As with the input pin capacitor, in order to avoid the influence on the regulator characteristics due to variations in the components of the external capacitor, DC bias characteristics and temperature characteristics are good for all of the above output pin capacitors and mounting layout position (about ± 15% , X7R, X8R), it is recommended to select a capacitor of an excellent EIA standard high withstanding voltage, place it as close to the output pin as possible so as not to be affected by mounting impedance etc, and lay it on the same mounting surface.

Thermal Design

Within this product, the power consumption is decided by the dropout voltage condition, the load current and the circuit current. Refer to Package Data illustrated in Figure 38 when using the IC in an environment of Ta ≥ 25 °C. Even if the ambient temperature Ta is at 25 °C, depending on the input voltage and the load current, chip junction temperature can be very high. Consider the design to be Tj ≤ Tjmax = 150 °C in all possible operating temperature range. On the reverse side of the package (HTSOP-J8) there is exposed heat pad for improving the heat dissipation.
Should by any condition the maximum junction temperature Tjmax = 150 °C rating be exceeded by the temperature increase of the chip, it may result in deterioration of the properties of the chip. The thermal impedance in this specification is based on recommended PCB and measurement condition by JEDEC standard. Verify the application and allow sufficient margins in the thermal design by the following method is used to calculate the junction temperature Tj.
Tj can be calculated by either of the two following methods.

1. The following method is used to calculate the Tj: Junction Temperature from Ta: Ambient Temperature.

$$Tj = Ta + P_C \times \theta_{JA} \quad [°C]$$

Where:

Tj	: Junction Temperature
Ta	: Ambient Temperature
P_C	: Power Consumption
θ_{JA}	: Thermal Impedance (Junction to Ambient)

2. The following method is also used to calculate the Tj: Junction Temperature from T_T: top Center of Case's (mold) Temperature.

$$Tj = T_T + P_C \times \Psi_{JT} \quad [°C]$$

Where:

Tj	: Junction Temperature
T_T	: Top Center of Case's (mold) Temperature
P_C	: Power Consumption
Ψ_{JT}	: Thermal Characteristic Parameter (Junction to Top Center of Case)

The following method is used to calculate the power consumption Pc (W) from input and output voltage, output current and circuit current.

$$Pc = (V_{CC} - V_O) \times I_O + V_{CC} \times I_{CC} \quad [W]$$

Where:

P_C	: Power Consumption
V_{CC}	: Input Voltage
V_O	: Output Voltage
I_O	: Output Current
I_{CC}	: Circuit Current

Thermal Design – continued

If V_{CC} = 5.0 V, V_O = 3.3 V, I_O = 0.1 A, I_{CC} = 400 μA, the power consumption Pc can be calculated as follows:

$$P_C = (V_{CC} - V_O) \times I_O + V_{CC} \times I_{CC}$$
$$= (5.0\ V - 3.3\ V) \times 0.1\ A + 5.0\ V \times 400\ \mu A$$
$$= 0.172\ W$$

At the ambient temperature Tamax = 125 °C, the thermal Impedance (Junction to Ambient) θ_{JA} = 45.2 °C/W (4-layer PCB),

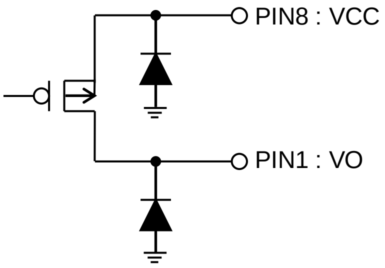
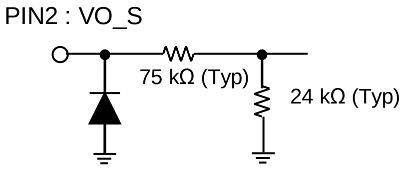
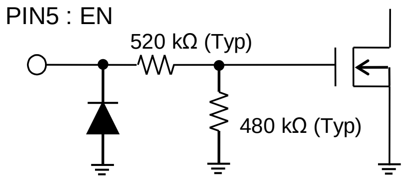
$$Tj = Tamax + P_C \times \theta_{JA}$$
$$= 125\ ℃ + 0.172\ W \times 45.2\ ℃/W$$
$$= 132.8\ ℃$$

When operating the IC, the top center of case's (mold) temperature T_T = 100 °C, Ψ_{JT} = 13 °C/W (4-layer PCB),

$$Tj = T_T + P_C \times \Psi_{JT}$$
$$= 100\ ℃ + 0.172\ W \times 13\ ℃/W$$
$$= 102.2\ ℃$$

For optimum thermal performance, it is recommended to expand the copper foil area of the board, increasing the layer and thermal via between thermal land pad.

I/O Equivalence Circuits

<table>
<tr><th>PIN8 : VCC
PIN1 : VO</th><th>PIN2 : VO_S</th><th>PIN5 : EN</th></tr>
<tr><td>
</td><td>
</td><td>
</td></tr>
</table>

Linear Regulators Surge Voltage Protection

In the following, it explains the protection method for ICs when surge exceed absolute maximum ratings is applied to the input.

Applying Positive Surge to the Input

If the positive surge that exceeds absolute maximum ratings 7 V is applied to the input, a Zener Diode should be placed to protect the device in between the IN and the GND as shown in the figure 39.

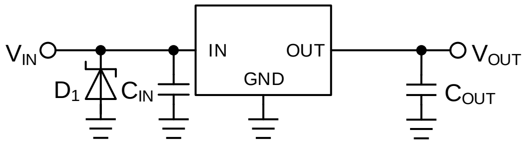


Figure 39. Surges Higher than 7 V is Applied to the Input

Applying Negative Surge to the input

If the negative surge that exceeds absolute maximum ratings -0.3 V is applied to the input, a Schottky Diode should be place to protect the device in between the IN and the GND as shown in the figure 40.

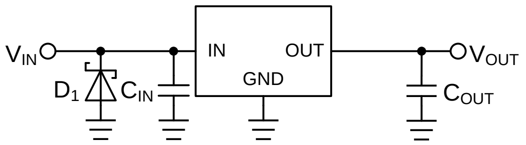


Figure 40. Surges Lower than -0.3 V is Applied to the Input

Linear Regulators Reverse Voltage Protection

A linear regulator integrated circuit (IC) requires that the input voltage is always higher than the output voltage. Output voltage, however, may become higher than the input voltage under specific situations or circuit configurations, and that reverse voltage and current may cause damage to the IC. A reverse polarity connection or certain inductor components can also cause a polarity reversal between the input and output pins. In the following, it explains the protection method for ICs when a condition of voltage reverses.

Reverse Input /Output Voltage

In a MOS linear regulator, a body diode exists as a parasitic element in the drain-source junction portion of its power MOSFET. Reverse input/output voltage triggers the current flow from the output to the input through the body diode. The inverted current may damage or destroy the semiconductor elements of the regulator since the effect of the parasitic body diode is not guaranteed the operation (Figure 41).

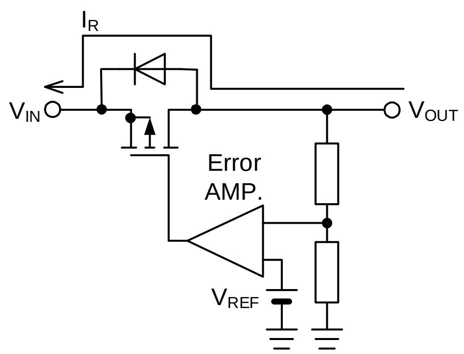


Figure 41. Reverse Current Path in a MOS Linear Regulator

Reverse Input /Output Voltage - continued

An effective solution to this is to connect an external bypass diode connected in-between the input and output to prevent the reverse current from flowing inside the IC (see Figure 42). Note that the bypass diode must be turned on before the internal circuit of the IC. Bypass diodes in the internal circuits of MOS linear regulators must have low forward voltage V_F. When the reverse current from this bypass diode is large, leakage current of the diode flows a lot from the input to the output even if it turns off the output with IC the shutdown function; therefore, it is necessary to choose one that has a small reverse current. Specifically, select a diode with a rated reverse voltage greater than the input to output voltage differential and rated forward current greater than the reverse current.

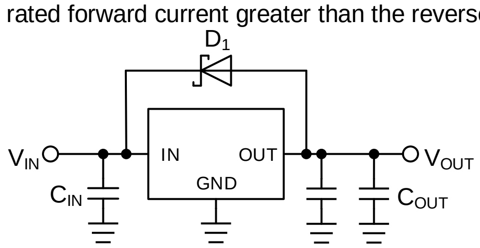


Figure 42. Bypass Diode for Reverse Current Diversion

The lower forward voltage (V_F) of Schottky barrier diodes cater to requirements of MOS linear regulators, however the main drawback is that their reverse current (I_R), which is relatively high. So, one with a low reverse current is recommended when choosing a Schottky diode. The I_R characteristics versus temperatures show increases at higher temperatures. It is recommended that confirming the datasheet for Schottky barrier diodes.

If V_{IN} is open in a circuit as shown in the following Figure 43 with its input/output voltage being reversed, the only current that flows in the reverse current path is the bias current of the IC. Because the amperage is too low to damage or destroy the parasitic element, a reverse current bypass diode is not required for this type of circuit.

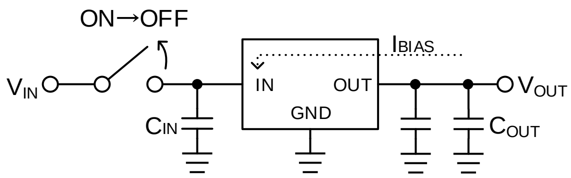


Figure 43. Open V_{IN}

Protection against Input Reverse Voltage

When connecting the power supply to the input, if plus and minus are inadvertently connected in reverse, or when there is a possibility that the input may become lower than the GND pin, it is necessary to prevent the electrostatic breakdown prevention diode between the IC input pin and the GND pin A large current may flow, so the IC may be destroyed (see Figure 44).

A Schottky barrier diode or rectifier diode connected in series with the power supply as shown in Figure 45 is the simplest solution to prevent this. There is a power loss calculated as V_F x $I_{OUT,}$ as the forward voltage V_F of the diode drops in a correct connection. The V_F of a Schottky barrier diode is lower than that of a rectifier diode gives a slightly smaller power loss. Because diodes generate heat, select a diode that has enough allowance in power dissipation. A reverse connection allows a negligible reverse current to flow in the diode.

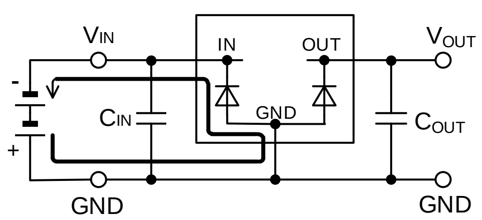


Figure 44. Current Path in Reverse Input Connection

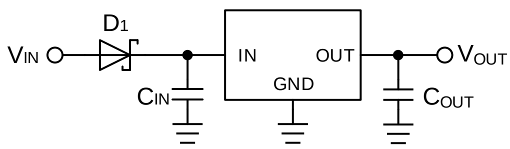


Figure 45. Protection against Reverse Polarity 1

Protection against Input Reverse Voltage - continued

Figure 46 shows a circuit in which a P-channel MOSFET is connected in series with the power. The diode located in the drain-source junction portion of the MOSFET is a body diode (parasitic element). Pch MOSFET turns on in a correct connection. The voltage drop is calculated by multiplying the ON resistance and the output current IOUT. Therefore, it is smaller than the voltage drop by the diode (see Figure 46) and results in less of a power loss. No current flows in a reverse connection where the MOSFET remains off.

If the voltage taking account of derating is greater than the voltage rating of MOSFET gate-source junction, lower the gate-source junction voltage by connecting voltage dividing resistors as shown in Figure 47.

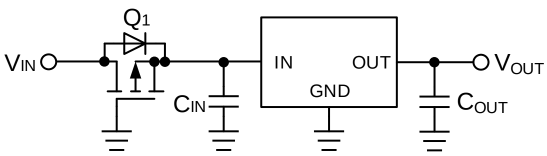


Figure 46. Protection against Reverse Polarity 2

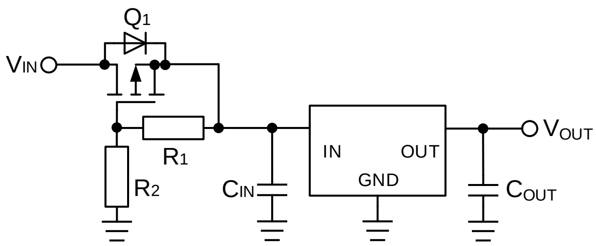


Figure 47. Protection against Reverse Polarity 3

Protection against Output Reverse Voltage when Output Connect to an Inductor
If the output load is inductive, electrical energy accumulated in the inductive load is released to the ground upon the output voltage turning off. There is a diode between the IC output pin and ground pin for preventing electrostatic breakdown, in which a large current flows that could destroy the IC. To prevent this, connect a Schottky barrier diode in parallel with the diode (see Figure 48).

Further, if a long wire is in use for the connection between the output pin of the IC and the load, observe the waveform on an oscilloscope, since it is possible that the load becomes inductive. An additional diode is needed for a motor load because a similar electric current flows by its counter electromotive force.

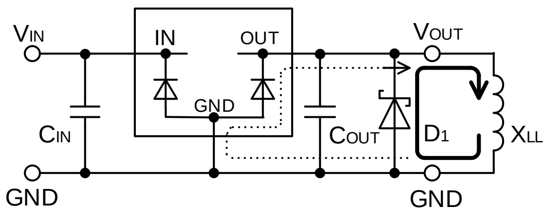


Figure 48. Current Path in Inductive Load (Output: Off)

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Operating Ratings**
   The function and operation of the IC are guaranteed within the range specified by the operating ratings. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. **Unused Input Pins**
   Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

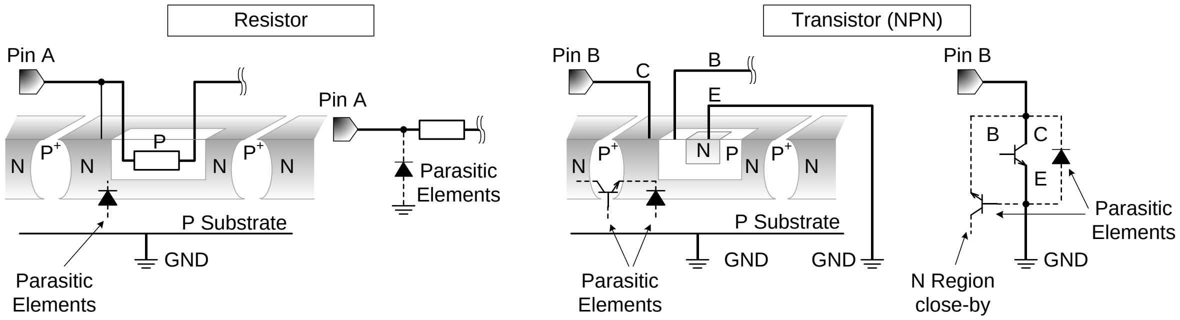


Figure 49. Example of monolithic IC structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC’s maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

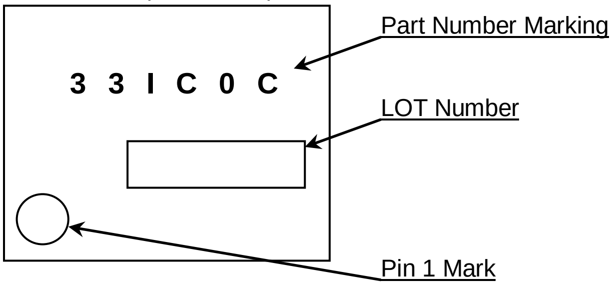
Ordering Information

B D 3 3 I C 0 M E F J - C E 2

Part Number	Output voltage	Voltage resistance	Output current	Characteristic	Package	Packaging and forming specification
BD	33: 3.3 V	I:7 V	C0:1.0 A	M:Automotive	EFJ:HTSOP-J8	C: Automotive Grade E2: Emboss tape reel

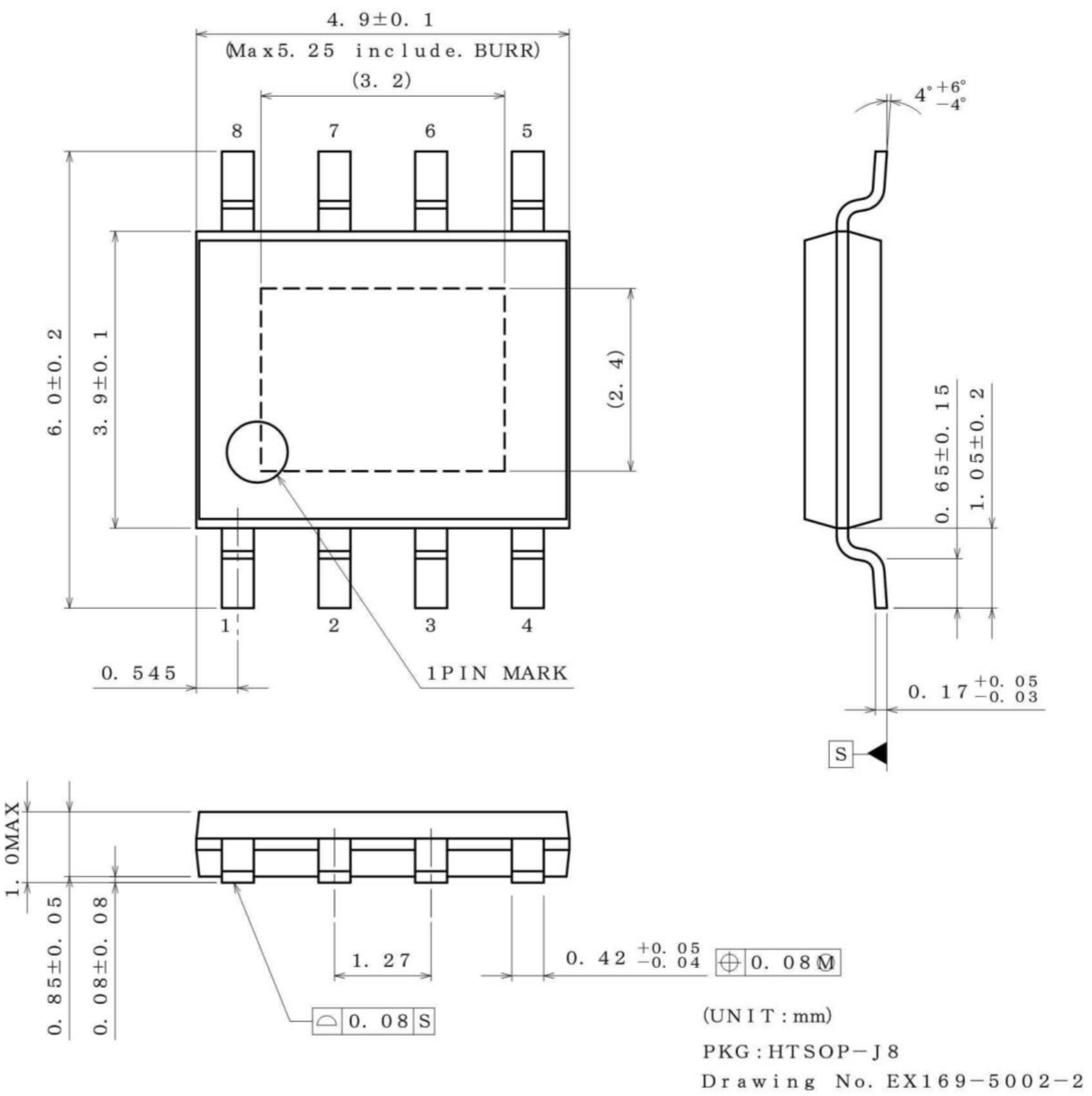
Marking Diagram

HTSOP-J8 (TOP VIEW)



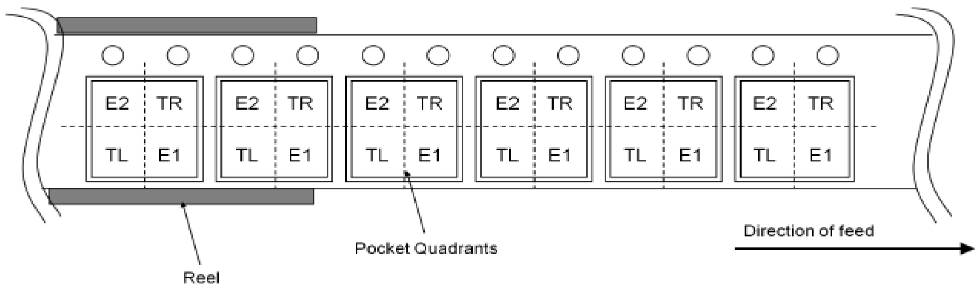
Physical Dimension and Packing Information

Package Name	HTSOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



Revision History

Date	Revision	Changes
26.Sep.2018	001	New release

Notice

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

2. ROHM designs and manufactures its Products subject to strict quality control system. However, semiconductor products can fail or malfunction at a certain rate. Please be sure to implement, at your own responsibilities, adequate safety measures including but not limited to fail-safe design against the physical injury, damage to any property, which a failure or malfunction of our Products may cause. The following are examples of safety measures:
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   [b] Installation of redundant circuits to reduce the impact of single or multiple circuit failure

3. Our Products are not designed under any special or extraordinary environments or conditions, as exemplified below. Accordingly, ROHM shall not be in any way responsible or liable for any damages, expenses or losses arising from the use of any ROHM's Products under any special or extraordinary environments or conditions. If you intend to use our Products under any special or extraordinary environments or conditions (as exemplified below), your independent verification and confirmation of product performance, reliability, etc, prior to use, must be necessary:
   [a] Use of our Products in any types of liquid, including water, oils, chemicals, and organic solvents
   [b] Use of our Products outdoors or in places where the Products are exposed to direct sunlight or dust
   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
   [d] Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
   [e] Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
   [f] Sealing or coating our Products with resin or other coating materials
   [g] Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

Precautions Regarding Application Examples and External Circuits

1. If change is made to the constant of an external circuit, please allow a sufficient margin considering variations of the characteristics of the Products and external components, including transient characteristics, as well as static characteristics.

2. You agree that application notes, reference designs, and associated data and information contained in this document are presented only as guidance for Products use. Therefore, in case you use such information, you are solely responsible for it and you must exercise your own independent verification and judgment in the use of such information contained in this document. ROHM shall not be in any way responsible or liable for any damages, expenses or losses incurred by you or third parties arising from the use of such information.

Precaution for Electrostatic

This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

Precaution for Storage / Transportation

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
   - [a] the Products are exposed to sea winds or corrosive gases, including Cl2, H2S, NH3, SO2, and NO2
   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.

4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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