# General-Purpose 6ch Electronic Volume with Built-in Advanced Switch 

## BD3461FS

## General Description

BD3461FS is a 6ch electronic volume which has the best audio efficiency in the industry. It has an external sound mixing function (with volume) in the favorite channel for mixing of portable audio and car navigation's guide sound. Also, BD3461FS has a volume switching shock sound prevention technique called "Advanced Switch," supporting the construction of high quality car audio space by simple control.

## Features

- Reduce switching noise of volume by using Advanced Switch circuit.
- Mixing for external sound monaural 3ch. It is possible that is mixed to front/Rear/Sub output Lch/Rch independently.
- Built-in 3ch ATT for external sound mixing that can be controlled independently.
- Built-in buffered ground isolation amplifier inputs, ideal for external input.
■ Energy-saving design resulting in low-current consumption by utilizing the Bi -CMOS process. It has the advantage in quality over scaling down the power heat control of internal regulators.
- Arranges all I/O terminals together for easier PCB layout and smaller PCB area.
- $I^{2} \mathrm{C}$ BUS can be controlled by $3.3 \mathrm{~V} / 5 \mathrm{~V}$.


## Key Specifications

- Power Supply Voltage Range:
7.0V to 9.5 V
- Circuit Current (no signal):
- Total Harmonic Distortion:
- Maximum Input Voltage:
- Cross-talk between Selectors:
- Volume Control Range:
- Output Noise Voltage:
- Residual Output Noise Voltage:
- Operating Temperature Range:

25 mA (Typ) 0.0004\% (Typ)
2.35 Vrms (Typ)
-105dB (Typ) +23 dB to -79 dB
$1.9 \mu \mathrm{Vrms}(\mathrm{Typ})$
$1.6 \mu \mathrm{Vrms}$ (Typ)
$-40^{\circ} \mathrm{C}$ to $+85^{\circ} \mathrm{C}$

Package
W(Typ) $\times \mathrm{D}($ Typ $) \times \mathrm{H}($ Max $)$


SSOP-A24
$10.00 \mathrm{~mm} \times 7.80 \mathrm{~mm} \times 2.10 \mathrm{~mm}$

## Applications

It is optimal for car audio. It can also be used for car navigation, audio equipment of mini Compo, micro Compo, DVD, TV, etc.

## Typical Application Circuit



Unit
$\mathrm{R}:[\Omega]$
C: [F]

## Pin Configuration



Pin Descriptions

| Pin No. | Pin Name | Description | Pin No. | Pin Name | Description |
| :---: | :---: | :--- | :---: | :---: | :--- |
| 1 | INF1 | 1ch Front input terminal | 13 | OUTS2 | 2ch Subwoofer output terminal |
| 2 | INF2 | 2ch Front input terminal | 14 | OUTS1 | 1ch Subwoofer output terminal |
| 3 | INR1 | 1ch Rear input terminal | 15 | OUTR2 | 2ch Rear output terminal |
| 4 | INR2 | 2ch Rear input terminal | 16 | OUTR1 | 1ch Rear output terminal |
| 5 | INS1 | 1ch Subwoofer input terminal | 17 | OUTF2 | 2ch Front output terminal |
| 6 | INS2 | 2ch Subwoofer input terminal | 18 | OUTF1 | 1ch Front output terminal |
| 7 | EXT1 | 1ch External input terminal | 19 | VCC | Power supply terminal |
| 8 | EXT2 | 2ch External input terminal | 20 | CS | Chip select terminal |
| 9 | EXT3 | 3ch External input terminal | 21 | SCL | I $^{2} C$ Communication clock terminal |
| 10 | DIFOUT | DIFF amp output terminal | 22 | SDA | I $^{2} C$ Communication data terminal |
| 11 | NIN | DIFF amp negative input terminal | 23 | GND | GND terminal |
| 12 | PIN | DIFF amp positive input terminal | 24 | FIL | VCC/2 terminal |

## Block Diagram



## Absolute Maximum Ratings $\left(\mathrm{Ta}=25^{\circ} \mathrm{C}\right.$ )

| Parameter | Symbol | Rating | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply Voltage | $\mathrm{V}_{\text {cc }}$ | 10.0 V | V |
| Input Voltage | V IN | $\mathrm{V}_{\mathrm{cc}}+0.3$ to GND-0.3 | V |
| Power Dissipation | Pd | $1^{(\text {Note } 1)}$ | W |
| Storage Temperature | Tstg | -55 to +150 | ${ }^{\circ} \mathrm{C}$ |

(Note 1) This value decreases $8 \mathrm{~mW} /{ }^{\circ} \mathrm{C}$ for $\mathrm{Ta}=25^{\circ} \mathrm{C}$ or more.
ROHM standard board shall be mounted. Thermal resistance $\theta \mathrm{ja}=125\left({ }^{\circ} \mathrm{C} / \mathrm{W}\right)$
ROHM standard board Size : $70 \times 70 \times 1.6\left(\mathrm{~mm}^{3}\right)$
Material : FR4 grass epoxy board ( $3 \%$ or less of copper foil area)
Caution: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Recommended Operating Conditions

| Parameter | Symbol | Rating | Unit |
| :--- | :---: | :---: | :---: |
| Power Supply Voltage | V cc | 7.0 to 9.5 | V |
| Temperature | Topr | -40 to +85 | ${ }^{\circ} \mathrm{C}$ |

Electrical Characteristics
(Unless specified, $\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{V} \mathrm{Vc}=8.5 \mathrm{~V}, \mathrm{f}=1 \mathrm{kHz}, \mathrm{V}_{\mathrm{IN}}=1 \mathrm{Vrms}, \mathrm{Rg}=600 \Omega$, $\mathrm{R}=10 \mathrm{k} \Omega$, INF1 input, Volume 0 dB )

| Parameter | Symbol | Limit |  |  | Conditions |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |

## Electrical Characteristics - continued

(Unless specified, $\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{V}_{\mathrm{CC}}=8.5 \mathrm{~V}, \mathrm{f}=1 \mathrm{kHz}, \mathrm{V}_{\mathrm{IN}}=1 \mathrm{Vrms}, \mathrm{Rg}=600 \Omega$, $\mathrm{R}_{\mathrm{L}}=10 \mathrm{k} \Omega$, INF 1 input, Volume 0 dB )

| $\begin{aligned} & \text { प্ঠ } \\ & \text { O } \\ & \text { © } \end{aligned}$ | Parameter | Symbol | Limit |  |  | Unit | Conditions |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Typ | Max |  |  |
| $\begin{aligned} & \sum_{\beth}^{\omega} \\ & \stackrel{\rightharpoonup}{0} \end{aligned}$ | Input Impedance | Rin_v | 70 | 100 | 130 | $\mathrm{k} \Omega$ |  |
|  | Maximum Input Voltage | Vıм | 2 | 2.35 | - | Vrms | $\begin{aligned} & \mathrm{V}_{\text {Iм }} \text { at } \mathrm{THD}+\mathrm{N}\left(\mathrm{~V}_{\text {out }}\right)=1 \% \\ & \mathrm{BW}=400 \mathrm{~Hz}-30 \mathrm{kHz} \end{aligned}$ |
|  | Maximum Gain | Gv_bSt | 21 | 23 | 25 | dB | $\begin{aligned} & \text { Gain }=23 \mathrm{~dB} \\ & \mathrm{~V}_{\text {IN }}=100 \mathrm{mVrms} \\ & \mathrm{Gv}=20 \log \left(\mathrm{~V}_{\text {out }} / \mathrm{V}_{\text {IN }}\right) \end{aligned}$ |
|  | Maximum Attenuation * | Gv_min | - | -109 | -90 | dB | $\begin{aligned} & \text { Volume }=-\infty \mathrm{dB} \\ & \mathrm{Gv}=20 \log (\text { Vout } / \mathrm{VIN}) \\ & \mathrm{BW}=\mathrm{IHF}-\mathrm{A} \end{aligned}$ |
|  | Step Resolution | Gv_step | - | 1 | - | dB | GAIN\&ATT $=+23 \mathrm{~dB}$ to $-79 \mathrm{~dB}$ |
|  | Gain Set Error | Gv_ERR | -2 | 0 | +2 | dB | Gain $=+1 \mathrm{~dB}$ to +23 dB |
|  | Attenuation Set Error 1 | Gv_ERR1 | -2 | 0 | +2 | dB | ATT $=-1 \mathrm{~dB}$ to -15 dB |
|  | Attenuation Set Error 2 | Gv_ERR2 | -3 | 0 | +3 | dB | ATT $=-16 \mathrm{~dB}$ to -47 dB |
|  | Attenuation Set Error 3 | Gv_ERR3 | -4 | 0 | +4 | dB | ATT $=-48 \mathrm{~dB}$ to -79 dB |
|  | Output Impedance | Rout | - | - | 50 | $\Omega$ | VIN $=100 \mathrm{mVms}$ |
|  | Maximum Output Voltage | Vом | 2 | 2.35 | - | Vrms | $\begin{aligned} & \text { THD+N=1\% } \\ & \text { BW }=400 \mathrm{~Hz}-30 \mathrm{kHz} \end{aligned}$ |
|  | Input Impedance | Rin_m | 70 | 100 | 130 | k $\Omega$ |  |
|  | Maximum Attenuation * | Gm_min | - | -90 | - | dB | $\begin{aligned} & \mathrm{G}_{\mathrm{M}}=20 \log \left(\mathrm{~V} \text { out } / \mathrm{V}_{\mathrm{IN}}\right) \\ & \mathrm{BW}=\text { IHF-A, ATT }=-\infty \mathrm{dB} \end{aligned}$ |
|  | Step Resolution 1 | GM_STEP1 | - | 8 | - | dB | ATT $=0 \mathrm{~dB}$ to -32 dB |
|  | Step Resolution 2 | GM_STEP2 | - | 16 | - | dB | ATT $=-32 \mathrm{~dB}$ to -64 dB |

VP-9690A (Average value detection, effective value display) filter by Matsushita Communication is used for * measurement.
Phase between input / output is same.

## Typical Performance Curves



Figure 1. Quiescent Current vs Supply Voltage


Figure 3. Voltage Gain vs Frequency


Figure 2. Total Harmonic Distortion vs Output Voltage


Figure 4. Volume Gain vs Frequency $(0 \mathrm{~dB}$ to $+23 \mathrm{~dB})$

## Typical Performance Curves - continued



Figure 5. Volume Gain vs Frequency 1
( +0 dB to -40 dB )


Figure 7. Cross-Talk Between Channels vs Frequency


Figure 6. Volume Gain vs Frequency 2
(-41dB to -79dB)


Figure 8. Ripple Rejection Ratio vs Frequency

## Typical Performance Curves - continued



Figure 9. Output Noise vs Volume Attenuation


Figure 11. Total Harmonic Distortion vs Frequency


Figure 10. Volume Gain of Large Output Level vs Frequency


Figure 12. Common Mode Rejection Ratio vs Frequency

## Typical Performance Curves - continued



Figure 13. Maximum Output Voltage vs Load Resistance

Figure 15. Advanced Switch 1


Figure 14. Mixing Attenuation vs Frequency


Figure 16. Advanced Switch 2

## Timing Chart

## CONTROL SIGNAL SPECIFICATIONS

(1) Electrical Specifications and Timing for Bus Lines and I/O Stages


Table 1 Characteristics of the SDA and SCL bus lines for $I^{2} \mathrm{C}$-bus devices
(Unless specified, $\mathrm{Ta}=25^{\circ} \mathrm{C}, \mathrm{V} \mathrm{Cc}=8.5 \mathrm{~V}$ )

| Parameter |  | Symbol | Fast-mode ${ }^{2} \mathrm{C}$-bus |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max |  |
| 1 | SCL clock frequency |  | fscl | 0 | 400 | kHz |
| 2 | Bus free time between a STOP and START condition | tbuF | 1.3 | - | $\mu \mathrm{S}$ |
| 3 | Hold time (repeated) START condition. After this period, the first clock pulse is generated | thd;sTA | 0.6 | - | $\mu \mathrm{S}$ |
| 4 | LOW period of the SCL clock | tıow | 1.3 | - | $\mu \mathrm{S}$ |
| 5 | HIGH period of the SCL clock | thigh | 0.6 | - | $\mu \mathrm{S}$ |
| 6 | Set-up time for a repeated START condition | tsu;STA | 0.6 | - | $\mu \mathrm{S}$ |
| 7 | Data hold time | thi; dat $^{\text {a }}$ | 0 (Note) | - | $\mu \mathrm{S}$ |
| 8 | Data set-up time | tsu;DAT | 100 | - | ns |
| 9 | Set-up time for STOP condition | tsu;STo | 0.6 | - | $\mu \mathrm{S}$ |

All values referred to VIH Min and VIL Max Levels (see Table 2).
(Note) To avoid sending right after the fall-edge of SCL (VIH min of the SCL signal), the transmitter sets a holding time of 300 ns or more for the SDA signal.
About 7 ( $\mathrm{t}_{H \mathrm{D} ; \mathrm{DAT}}$ ), $8\left(\mathrm{t}_{\mathrm{SU} ; \mathrm{DAT}}\right)$, make it the setup which a margin is fully in.
Table 2 Characteristics of the SDA and SCL I/O stages for $\mathrm{I}^{2} \mathrm{C}$-bus devices

| Parameter |  | Symbol | Fast-mode devices |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max |  |
| 10 | LOW level input voltage |  | VIL | -0.5 | +1 | V |
| 11 | HIGH level input voltage | $\mathrm{V}_{\mathrm{IH}}$ | 2.3 | - | V |
| 12 | Pulse width of spikes which must be suppressed by the input filter. | tsp | 0 | 50 | ns |
| 13 | LOW level output voltage (open drain or open collector) at 3mA sink current | Vol1 | 0 | 0.4 | V |
| 14 | Input current of each I/O pin with an input voltage between 0.4 V and 4.5 V | 1 | -10 | +10 | $\mu \mathrm{A}$ |



SCL clock frequency : 250 kHz
Figure 18. $\mathrm{I}^{2} \mathrm{C}$ Command Data Transmission Timing Diagram
(2) $\underline{\underline{1^{2} \mathrm{C}} \text { BUS FORMAT }}$

| MSB LSB |  | MSB |  | MSB |  | LSB |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| S | Slave Address | A | Select Address | A | Data | A | P |
| 1bit | 8bit | 1bit 8bit 1bit <br> $=$ Start condition (Recognition of start bit)  |  |  |  | 1bit 1bit |  |
|  | S |  |  |  |  |  |  |
|  | Slave Address | = Recognition of slave address. The first 7 bits correspond to the slave address. The least significant bit is " L " which corresponds to write mode. |  |  |  |  |  |
|  | A | = ACKNOWLEDGE bit (Recognition of acknowledgement) |  |  |  |  |  |
|  | Select Address | = Select address corresponding to volume, bass or treble. |  |  |  |  |  |
|  | Data | = Data on every volume and tone. |  |  |  |  |  |
|  | P | = Stop condition (Recognition of stop bit) |  |  |  |  |  |

(3) ${ }^{12} \mathrm{C}$ BUS Interface Protocol
(a) Basic Format

| S | Slave Address | A | Select Address | A | Data | A | P |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MSB |  | LSB | MSB | LSB | MSB | LSB |  |

(b) Automatic Increment (Select Address increases (+1) according to the number of data.)

| S | Slave Address | A | Select Address | A | Data1 | A | Data2 | A | $\cdots$ | DataN | A | P |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| MSB | LSB | MSB | LSB | MSB | LSB | MSB | LSB |  | MSB | LSB |  |  |

(Example) (1) Data1 shall be set as data of address specified by Select Address.
(2) Data2 shall be set as data of address specified by Select Address +1 .
(3) DataN shall be set as data of address specified by Select Address $+\mathrm{N}-1$.
(c) Configuration Unavailable for Transmission (In this case, only Select Address1 is set.)

| (c) |  |  |  |  |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| S | Slave Address | A | Select Address1 | A | Data | A | Select Address 2 | A | Data | A | P |
| MSB | LSB | MSB | LSB | MSB | LSB | MSB | LSB | MSB | LSB |  |  |

(Note) If any data is transmitted as Select Address 2 next to data, it is recognized as data, not as Select Address 2.
(4) Slave Address

Because the slave address can be changed by the setting of CS, it is possible to use two chips at the same time on identical BUS.

| MSB |  | ASB |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| SEL Voltage Condition | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W |
| GND to $0.2 \times$ Vcc | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| $0.8 \times$ Vcc to Vcc | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |

Establish the CS voltage to define the setting.
(5) Select Address \& Data

| Items to be set | Select Address (hex) | MSB | Data |  |  |  |  |  | LSB |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Initial Setup 1 | 01 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 |
| Volume 1ch Front | 28 | Volume Gain / Attenuation |  |  |  |  |  |  |  |
| Volume 2ch Front | 29 | Volume Gain / Attenuation |  |  |  |  |  |  |  |
| Volume 1ch Rear | 2A | Volume Gain / Attenuation |  |  |  |  |  |  |  |
| Volume 2ch Rear | 2B | Volume Gain / Attenuation |  |  |  |  |  |  |  |
| Volume 1ch Sub | 2 C | Volume Gain / Attenuation |  |  |  |  |  |  |  |
| Volume 2ch Sub | 2D | Volume Gain / Attenuation |  |  |  |  |  |  |  |
| EXT 1 ON/OFF | 30 | $\begin{gathered} \mathrm{EXT} 1 \\ \mathrm{~S} 2 \\ \hline \end{gathered}$ | $\begin{gathered} \text { EXT1 } \\ \text { S1 } \\ \hline \end{gathered}$ | $\begin{gathered} \text { EXT1 } \\ \text { R2 } \\ \hline \end{gathered}$ | $\begin{gathered} \text { EXT1 } \\ \text { R1 } \\ \hline \end{gathered}$ | $\begin{gathered} \hline \text { EXT1 } \\ \text { F2 } \\ \hline \end{gathered}$ | $\begin{gathered} \text { EXT1 } \\ \text { F1 } \\ \hline \end{gathered}$ | 0 | 0 |
| EXT 2 ON/OFF | 31 | $\begin{gathered} \text { EXT2 } \\ \text { S2 } \\ \hline \end{gathered}$ | $\begin{gathered} \text { EXT2 } \\ \text { S1 } \\ \hline \end{gathered}$ | $\begin{gathered} \mathrm{EXT2} 2 \\ \mathrm{R} 2 \\ \hline \end{gathered}$ | $\begin{gathered} \text { EXT2 } \\ \text { R1 } \\ \hline \end{gathered}$ | $\begin{gathered} \text { EXT2 } \\ \text { F2 } \\ \hline \end{gathered}$ | $\begin{gathered} \text { EXT2 } \\ \text { F1 } \end{gathered}$ | 0 | 0 |
| EXT 3 ON/OFF | 32 | $\begin{gathered} \text { EXT3 } \\ \text { S2 } \end{gathered}$ | $\begin{gathered} \text { EXT3 } \\ \text { S1 } \\ \hline \end{gathered}$ | $\begin{gathered} \text { EXT3 } \\ \text { R2 } \\ \hline \end{gathered}$ | $\begin{gathered} \text { EXT3 } \\ \text { R1 } \\ \hline \end{gathered}$ | $\begin{gathered} \text { EXT3 } \\ \text { F2 } \\ \hline \end{gathered}$ | $\begin{gathered} \text { EXT3 } \\ \text { F1 } \end{gathered}$ | 0 | 0 |
| EXT 1 ATT | 33 | 0 | 0 | 0 | 0 | 0 | EXT1 Attenuation |  |  |
| EXT 2 ATT | 34 | 0 | 0 | 0 | 0 | 0 | EXT2 Attenuation |  |  |
| EXT 3 ATT | 35 | 0 | 0 | 0 | 0 | 0 | EXT3 Attenuation |  |  |
| Test Mode | F0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| System Reset | FE | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |

(Note)
Advanced Switch

1. The Advanced Switch works in the latch part while changing from one function to another.
2. Upon continuous data transfer, the Select Address rolls over because of the automatic increment function, as shown below.

3. Changing "EXT = ON/OFF" and "EXT Atteuation", does not correspond for advance switch. Therefore, please do the measure that applies mute on the side of a set.

Select address 28, 29, 2A, 2B, 2C, 2D(hex)

| Gain \& ATT | MSB | Volume Gain/Attenuation |  |  |  |  |  | LSB |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Prohibition ${ }^{(N o t e)}$ | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
|  | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 |
|  | : | : | : | : | : | : | : | : |
|  | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 |
| 23dB | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 |
| 22dB | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 |
| 21 dB | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 |
| : | : | : | : | : | : | : | : | : |
| -78dB | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| -78dB | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| -79dB | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| Prohibition ${ }^{(N o t e)}$ | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 |
|  | : | : | : | : | : | : | : | : |
|  | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| $-\infty \mathrm{dB}$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

(Note) Gain is set to "- -dB " when sending "Prohibition data".

Select address 30, 31, 32(hex)

| MODE | MSB | EXT1 F1 |  |  |  |  |  | LSB |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| OFF | $\begin{gathered} \text { EXT1 } \\ \text { S2 } \end{gathered}$ | $\begin{gathered} \text { EXT1 } \\ \text { S1 } \end{gathered}$ | $\begin{aligned} & \text { EXT1 } \\ & \text { R2 } \end{aligned}$ | $\begin{gathered} \text { EXT1 } \\ \text { R1 } \end{gathered}$ | $\begin{gathered} \text { EXT1 } \\ \text { F2 } \end{gathered}$ | 0 | 0 | 0 |
| ON |  |  |  |  |  | 1 |  |  |


| MODE | MSB | E×T1 F2 |  |  |  |  |  | LSB |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| OFF | $\begin{gathered} \text { EXT1 } \\ \text { S2 } \end{gathered}$ | $\begin{gathered} \text { EXT1 } \\ \mathrm{S} 1 \end{gathered}$ | $\begin{gathered} \text { EXT1 } \\ \text { R2 } \end{gathered}$ | $\begin{gathered} \text { EXT1 } \\ \text { R1 } \\ \hline \end{gathered}$ | 0 | $\begin{gathered} \hline \text { EXT1 } \\ \text { F1 } \\ \hline \end{gathered}$ | 0 | 0 |
| ON |  |  |  |  | 1 |  |  |  |


| MODE | MSB | E×T1 R1 |  |  |  |  |  | LSB |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| OFF | $\begin{gathered} \text { EXT1 } \\ \text { S2 } \end{gathered}$ | $\begin{gathered} \hline \text { EXT1 } \\ \text { S1 } \end{gathered}$ | $\begin{gathered} \text { EXT1 } \\ \text { R2 } \end{gathered}$ | 0 | $\begin{gathered} \text { EXT1 } \\ \text { F2 } \end{gathered}$ | $\begin{gathered} \text { EXT1 } \\ \text { F1 } \end{gathered}$ | 0 | 0 |
| ON |  |  |  | 1 |  |  |  |  |


| MODE | MSB | E×T1 R2 |  |  |  |  |  | LSB |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| OFF | $\begin{gathered} \text { EXT1 } \\ \text { S2 } \end{gathered}$ | $\begin{gathered} \text { EXT1 } \\ \text { S1 } \end{gathered}$ | 0 | $\begin{gathered} \text { EXT1 } \\ \text { R1 } \end{gathered}$ | $\begin{gathered} \text { EXT1 } \\ \text { F2 } \end{gathered}$ | $\begin{gathered} \text { EXT1 } \\ \text { F1 } \end{gathered}$ | 0 | 0 |
| ON |  |  | 1 |  |  |  |  |  |


| MODE | MSB | EXT1 S1 |  |  |  |  |  | LSB |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| OFF | $\begin{gathered} \text { EXT1 } \\ \text { S2 } \end{gathered}$ | 0 | $\begin{gathered} \hline \text { EXT1 } \\ \text { R2 } \end{gathered}$ | $\begin{gathered} \hline \text { EXT1 } \\ \text { R1 } \end{gathered}$ | $\begin{gathered} \text { EXT1 } \\ \text { F2 } \\ \hline \end{gathered}$ | $\begin{gathered} \text { EXT1 } \\ \text { F1 } \end{gathered}$ | 0 | 0 |
| ON |  | 1 |  |  |  |  |  |  |


| MODE | MSB | EXT1 |  |  |  |  |  | S2 | LSB |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |  |
| OFF | 0 | EXT1 | EXT1 | EXT1 | EXT1 | EXT1 | 0 | 0 |  |
| ON | 1 | S1 | R2 | R1 | F2 | F1 | 0 |  |  |

Select address 33, 34, 35(hex)

| Gain | MSB | $E \times$ Attenuation |  |  |  |  |  | LSB |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 0dB | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| -8dB |  |  |  |  |  | 0 | 0 | 1 |
| -16dB |  |  |  |  |  | 0 | 1 | 0 |
| -24dB |  |  |  |  |  | 0 | 1 | 1 |
| -32dB |  |  |  |  |  | 1 | 0 | 0 |
| -48dB |  |  |  |  |  | 1 | 0 | 1 |
| -64dB |  |  |  |  |  | 1 | 1 | 0 |
| $-\infty \mathrm{dB}$ |  |  |  |  |  | 1 | 1 | 1 |

(6) About Power ON Reset

Initialization inside IC is carried out at one of supply voltage circuits. Initial data is sent to all addresses at supply voltage on. Mute is ON until this initial data is sent.

| Parameter | Symbol | Limit |  |  | Unit | Conditions |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Typ | Max |  |  |  |
| Rise Time of VCC | tRISE | 20 | - | - | $\mu \mathrm{sec}$ | V Cc rise time from 0V to 3V |
| VCC Voltage of Release <br> Power ON Reset | VPOR | - | 4.1 | - | V |  |

## Application Information

1. Volume Gain/Attenuation of the details

| (dB) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (dB) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| +23 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | -29 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| +22 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | -30 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| +21 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | -31 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| +20 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | -32 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| +19 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | -33 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| +18 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | -34 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| +17 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | -35 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| +16 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | -36 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| +15 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | -37 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| +14 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | -38 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| +13 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | -39 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| +12 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | -40 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| +11 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | -41 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| +10 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | -42 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| +9 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | -43 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| +8 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | -44 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| +7 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | -45 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| +6 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | -46 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| +5 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | -47 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| +4 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | -48 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| +3 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | -49 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| +2 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | -50 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| +1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | -51 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | -52 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| -1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | -53 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| -2 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | -54 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| -3 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | -55 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| -4 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | -56 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| -5 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | -57 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| -6 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | -58 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| -7 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | -59 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| -8 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | -60 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| -9 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | -61 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| -10 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | -62 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| -11 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | -63 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| -12 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | -64 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| -13 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | -65 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| -14 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | -66 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| -15 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | -67 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| -16 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | -68 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| -17 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | -69 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| -18 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | -70 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| -19 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | -71 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| -20 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | -72 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| -21 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | -73 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| -22 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | -74 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| -23 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | -75 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| -24 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | -76 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| -25 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | -77 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| -26 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | -78 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| -27 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | -79 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| -28 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | $-\infty$ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

## 2. Application Circuit Diagram



Figure 19. Application Circuit Diagram

Unit
$R:[\Omega]$
C: [F]

## Power Dissipation

About the thermal design by the IC
Characteristics of an IC have a great deal to do with the temperature at which it is used, and exceeding absolute maximum ratings may degrade and destroy elements. Careful consideration must be given to the heat of the IC from the two standpoints of immediate damage and long-term reliability of operation.


Figure 20. Temperature Derating Curve (SSOP-A24)
(Note) Values are actual measurements and are not guaranteed. Power dissipation values vary according to the board on which the IC is mounted.

## I/O Equivalent Circuits

| Terminal No. | Terminal Voltage | Equivalent Circuit | Terminal Description |
| :---: | :---: | :---: | :---: |
| INF1 INF2 INR1 INR2 INS1 INS2 NIN PIN EXT1 EXT2 EXT3 | 4.25 |  | Signal input terminal. <br> The input impedance is $100 \mathrm{k} \Omega$ (typ). |
| DIFOUT <br> OUTS2 <br> OUTS1 <br> OUTR2 <br> OUTR1 <br> OUTF2 <br> OUTF1 | 4.25 |  | Fader output terminal. |
| CS | - |  | Slave address selection terminal. <br> "CS" is "High" to slave address " 84 H " <br> "CS" is "Low" to slave address " 80 H" |

The values in the input/output equivalent circuits are reference values only and are not guaranteed.

I/O Equivalent Circuits - continued

| Terminal Name | Terminal Voltage | Equivalent Circuit | Terminal Description |
| :---: | :---: | :---: | :---: |
| VCC | 8.5 |  | Power supply terminal. |
| SCL | - |  | A terminal for clock input of $I^{2} C$ BUS communication. |
| SDA | - |  | A terminal for data input of $I^{2} \mathrm{C}$ BUS communication. |
| GND | 0 |  | Ground terminal. |
| FIL | 4.25 |  | Voltage for reference bias of analog signal system. The simple precharge circuit and simple discharge circuit for an external capacitor are built in. |

The values in the input/output equivalent circuits are reference values only and are not guaranteed.

## Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

## 2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.
3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

## 4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

## 5. Thermal Consideration

Should by any chance the power dissipation rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.
6. Recommended Operating Conditions

These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.
7. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.
8. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.
9. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.
10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

## 11. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

## Operational Notes - continued

12. Regarding the Input Pin of the IC

This monolithic IC contains P + isolation and P substrate layers between adjacent elements in order to keep them isolated. $\mathrm{P}-\mathrm{N}$ junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):
When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.
Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the $P$ substrate) should be avoided.


Figure 21. Example of monolithic IC structure

## 13. About a Signal Input Part

## About Input Coupling Capacitor Constant Value

The constant value of input coupling capacitor $C(F)$ is decided with respect to the input impedance $\operatorname{Ris}(\Omega)$ at the input signal terminal of the IC. The first HPF characteristic of RC is composed.



$$
A(f)=\sqrt{\frac{\left(2 \pi \mathrm{fCR}_{\mathrm{IN}}\right)^{2}}{1+\left(2 \pi \mathrm{fCR}_{\mathrm{IN}}\right)^{2}}}
$$

## Operational Notes - continued

14. About Output Load Characteristics

The usages of output load are below (reference). Please use more than $10[\mathrm{k} \Omega](\mathrm{TYP}$ ) load.
Output pin on target

| Pin Name | Pin Name | Pin Name | Pin Name |
| :---: | :---: | :---: | :---: |
| OUTF1 | OUTR1 | OUTS1 | DIFOUT |
| OUTF2 | OUTR2 | OUTS2 |  |



Output Load Characteristic at $\mathrm{Vcc}=8.5 \mathrm{~V}$. (Reference)
15. Frequency Characteristic at Large Output Level

High slew-rate amplifiers are used for high quality sound. This IC corresponds to " 192 kHz sampling on DVD-Audio" which is highest quality. Output level is " $2 \mathrm{Vrms}, 192 \mathrm{kHz}$ flat(typ)".
(See the below graph (reference)).


## Operational Notes - continued

16. Oscillation Countermeasure for GND Isolation Amplifier Outputs

Using higher capacitor than 10 pF at GND isolation amplifier outputs (DIFOUT) may cause oscillation. As oscillation countermeasure, insert resistor in series to terminal directly as below.

| Capacitance | Resistor in series to terminal directly |
| :---: | :---: |
| $\mathrm{C}<10 \mathrm{pF}$ | Not necessary |
| $10<\mathrm{C}<100 \mathrm{pF}$ | $220 \Omega$ |

Resistor for oscillation countermeasure

17. Oscillation Countermeasure for Volume Outputs at Power Supply ON/OFF

If using higher capacitor than 22 pF at volume outputs, oscillation may occur for a moment when turning ON/OFF power supply (when $\mathrm{V}_{c c}$ is about 3 V to 4 V ). As oscillation countermeasure, insert resistor in series to terminal directly as shown below, and set volume output to mute outside this device when turning ON/OFF power supply.

| Capacitance | Resistor in series to terminal directly |
| :---: | :---: |
| $\mathrm{C}<22 \mathrm{pF}$ | Not necessary |
| $22<\mathrm{C}<220 \mathrm{pF}$ | $220 \Omega$ |



## 18. $I^{2} C$ BUS Transferring Data

Resistor for oscillation countermeasure

## [1] Types of Data Transfer

1.1 The data transfer without Advanced Switch (data transfer without data latching format) does not have regulations on transferring data.
1.2 The data transfer with Advanced Switch (data transfer with data latching format) does not have regulations on transferring data too. But Advanced Switch data transfer follows the order in [2].
[2] Advanced Switch Data Transfer
2-1. The timing chart of Advanced Switch data transfer is as follows.
■ Data Transfer Example 1


It is the same even if it transfers data in auto increment mode.

## Operational Notes - continued

There are no timing regulations in $I^{2} \mathrm{C}$ BUS transferring data. But the changing time starts after the end of the present change. In addition, the timing of Advanced Switch is not dependent on transferring data turn. Instead, it follows the following turn.


## Advanced Switch Start Turn

(Note) The block in the same group can start the Advanced Switch at the same time.

- Data Transfer Example 2

The data transfer turn differs from the actual change turn as shown below.


Please transfer data after the present Advanced Switch, if it wants to make a transferring data turn and Advanced Switch turn the same.

- Data Transfer Example 3

Priority is given to the data of the same select address when it is transferred to the timing which Advanced Switch has not ended. In addition, when two or more data are transferred to the same select address, the end transferred data is effective.


■ Data Transfer Example 4
Refresh data is the same as the present setup data, therefore Advanced Switch does not change.

The gain change data of other channels are transferred after refresh data as shown below.


## Operational Notes - continued

[3] Attention of Transferring Data
BD3461FS cannot set the data transfer from a microcomputer correctly on very rare occasions. In such cases, the following phenomenon may occur.

1. Volume gain does not change.
2. Volume gain changes to MUTE.

Therefore, the data transfer from a microcomputer should send data as shown in the following conditions.
(1) When the Volume change data send, please send the same data twice as below.


If Refresh data can't be sent like ©1timing, the output wave may be mute momentarily.

(2) If Volume change data can send over 94.08 msec interval transferring data, there is no need to send Refresh data.


## Ordering Information



## Marking Diagram

SSOP-A24 (TOP VIEW)


Physical Dimension, Tape and Reel Information
Package Name


## Revision History

| Date | Revision |  | Changes |
| :---: | :---: | :--- | :---: |
| 16. Dec.2015 | 001 | New Release |  |

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| :---: | :---: | :---: | :---: |
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|  |  | CLASSIII |  |

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[h] Use of the Products in places subject to dew condensation
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6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
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2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
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