

# 1.0V to 5.5V, 1A 1ch Termination Regulators for DDR-SDRAMs

**BD3539FVM BD3539NUX**

## General Description

BD3539 is a termination regulator that complies with JEDEC requirements for DDR1-SDRAM, DDR2-SDRAM, and DDR3-SDRAM. This linear power supply uses a built-in N-channel MOSFET and high-speed OP-AMPS specially designed to provide excellent transient response. It has a sink/source current capability of up to 1A and has a power supply bias requirement of 3.3 V (for DDR2 and DDR3) and 5.0 V (for DDR1, DDR2, and DDR3) for driving the N-channel MOSFET. By employing an independent reference voltage input (VDDQ) and a feedback pin (VTTS), this termination regulator provides excellent output voltage accuracy and load regulation as required by JEDEC standards. Additionally, BD3539 has a reference power supply output (VREF) for DDR-SDRAM or for memory controllers. Unlike the VTT output that goes to "Hi-Z" state, the VREF output is kept unchanged when EN input is changed to "Low", making this IC suitable for DDR-SDRAM under "Self Refresh" state.

## Features

- Incorporates a Push-Pull Power Supply for Termination (VTT)
- Incorporates a Reference Voltage Circuit (VREF)
- Incorporates an Enabler
- Incorporates an Under Voltage Lockout (UVLO)
- Incorporates a Thermal Shutdown Protector (TSD)
- Compatible with Dual Channel (DDR1, DDR2, DDR3)
- Usable Ceramic Capacitor at Output

## Applications

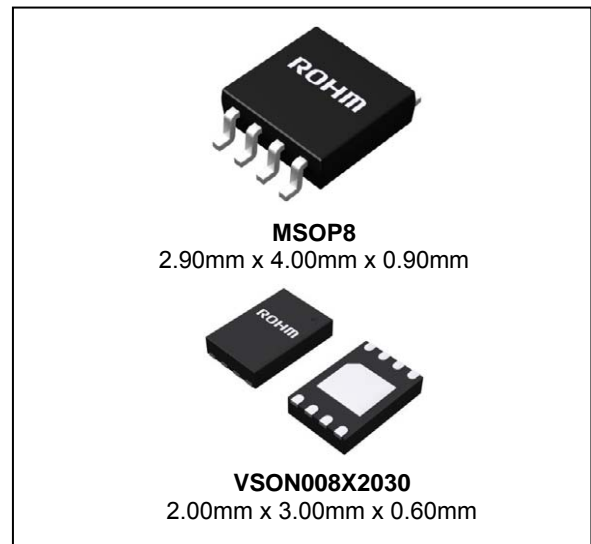
Power Supply for DDR 1/2/3 - SDRAM

## Key Specifications

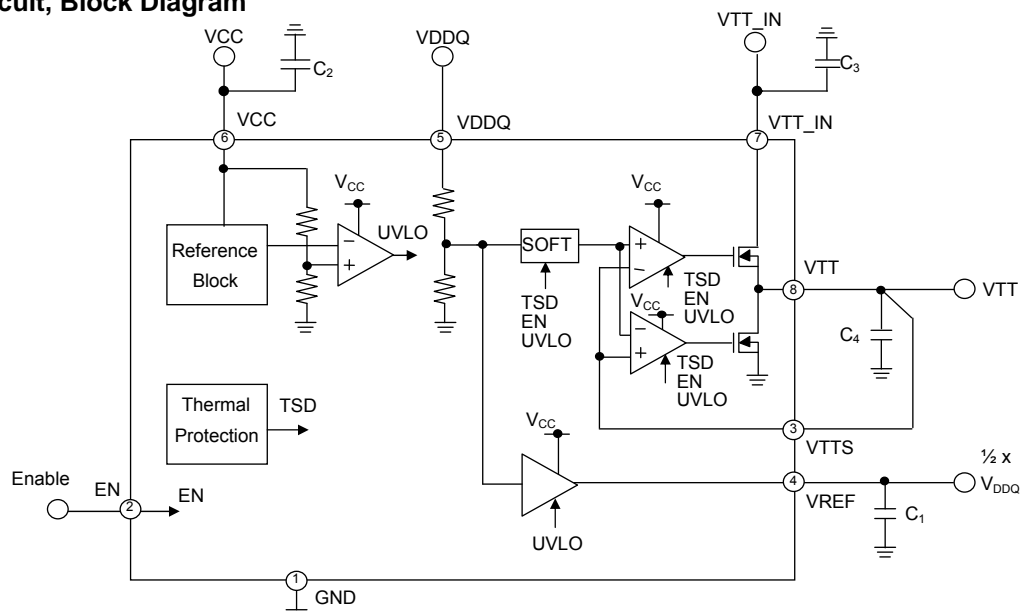
- Termination Input Voltage Range: 1.0V to 5.5V
- VCC Input Voltage Range: 2.7V to 5.5V
- VDDQ Reference Voltage Range: 1.0V to 2.75V
- Output Voltage:  $1/2 \times V_{DDQ}$  V(Typ)
- Output Current: 1.0A (Max)
- High side FET ON-Resistance: 0.35Ω(Typ)
- Low side FET ON-Resistance: 0.35Ω(Typ)
- Standby Current: 0.5mA (Typ)
- Operating Temperature Range: -30°C to +100°C

## Packages

W(Typ) x D(Typ) x H(Max)



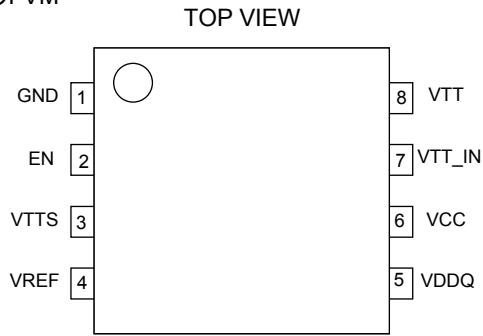
## Typical Application Circuit, Block Diagram



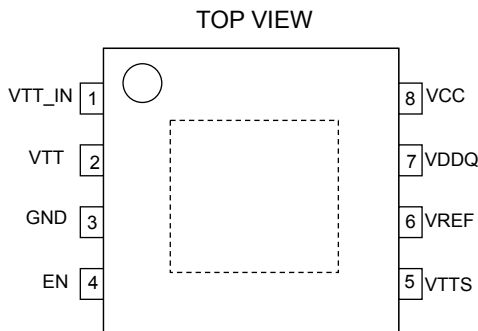
○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

## Pin Configurations

OFVM



ONUX



## Pin Descriptions

Pin No.	Pin Name	Pin Function
1	GND	Ground pin
2	EN	Enable input pin
3	VTTS	Detector pin for termination voltage
4	VREF	Reference voltage output pin
5	VDDQ	Reference voltage input pin
6	VCC	VCC pin
7	VTT_IN	Termination input pin
8	VTT	Termination output pin

Pin No.	Pin Name	Pin Function
1	VTT_IN	Termination input pin
2	VTT	Termination output pin
3	GND	Ground pin
4	EN	Enable input pin
5	VTTS	Detector pin for termination voltage
6	VREF	Reference voltage output pin
7	VDDQ	Reference voltage input pin
8	VCC	VCC pin
Bottom	FIN	Substrate (connected to GND)

## Description of Blocks

## 1. VCC

The VCC pin is for the independent power supply input that operates the internal circuit of the IC. It is the voltage at this pin that drives the IC's amplifier circuits. The VCC input ranges from 2.7V to 5.5V and maximum current consumption is 4mA. A bypass capacitor of 1 $\mu$ F or so should be connected to this pin when using the IC in an application circuit.

## 2. VDDQ

This is the power supply input pin for an internal voltage divider network. The voltage at VDDQ is halved by two 100k $\Omega$  internal voltage-divider resistors and the resulting voltage serves as reference for the VTT output. Since  $V_{REF}=V_{TT} = 1/2V_{DDQ}$ , the JEDEC requirement for DDR-SDRAM can be satisfied by supplying the correct voltage to VDDQ.

Noise input should be avoided at the VDDQ pin as it is also included by the voltage-divider at the output. An RC filter consisting of a resistor and a capacitor (220 $\Omega$  and 2.2 $\mu$ F, for instance,) may be used to reduce the noise input but make sure that it will not significantly affect the voltage-divider's output. the IC.

## 3. VTT\_IN

VTT\_IN is the power supply input pin for the VTT output. Input voltage may range from 1.0V to 5.5V, but consideration must be given to the current limit dictated by the ON-Resistance of the IC and to the change in allowable loss due to input/output voltage difference.

Generally, the following voltages are supplied:

- DDR3 VTT\_IN = 1.5V
- DDR2 VTT\_IN = 1.8V
- DDR1 VTT\_IN = 2.5V

Take note that a high-impedance voltage input at VTT\_IN may result in oscillation or degradation in ripple rejection, so connecting a 10 $\mu$ F capacitor with minimal change in capacitance to VTT\_IN terminal is recommended. However, this impedance may depend on the characteristics of the power supply input and the impedance of the PC board wiring, which must be carefully checked before use.

## Description of Blocks – continued

## 4. VREF

BD3539 provides a constant voltage, VREF, which is independent from the VTT output and can serve as reference input for memory controllers and DRAMs. The voltage level of VREF is kept constant even if the EN pin is at “Low” level, making the use of this IC compatible with the “Self Refresh” state of DRAMs.

In order to stabilize the output voltage, connecting the correct combination of capacitor and resistor to VREF is necessary. For this purpose, a 1.0 $\mu$ F to 2.2 $\mu$ F ceramic capacitor, characterized by minimal variation in capacitance, is recommended. The maximum current capability of the VREF pin is 25mA, but for an application which consumes a small amount of VREF current (1mA or less), using a capacitance of 0.1 $\mu$ F or less will do.

## 5. VTTS

VTTS is a sense pin for the load regulation of the VTT output voltage. In case the wire connecting VTT pin and the load is too long, connecting VTTS pin to the part of the wire nearer to the load may improve load regulation.

VTTS terminal is High impedance terminal. Therefore it is easy to be affected by the noise. The stable operation of the IC is possible by inserting RC filter (e.g.,: R=200 $\Omega$ , C=1000pF) near VTTS terminal.

## 6. VTT

This is the output pin for the DDR memory termination voltage and it has a sink/source current capability of  $\pm 1.0$ A. VTT voltage tracks the voltage at VDDQ pin divided in half. The output is turned OFF when EN pin is “Low” or when either the VCC UVLO or the thermal shutdown protection function is activated.

Always connect a capacitor to VTT pin for loop gain and phase compensation and for reduction in output voltage variation in the event of sudden load change. Be careful in choosing the capacitor as insufficient capacitance may cause oscillation and high ESR (Equivalent Series Resistance) may result in increased output voltage variation during a sudden change in load. A 10 $\mu$ F or so ceramic capacitor is recommended, though ambient temperature and other conditions should also be considered.

## 7. EN

A “High” input of 2.3V or higher to EN turns ON the VTT output. A “Low” input of 0.8V or less, on the other hand, turns VTT to a Hi-Z state. With a “Low” EN input, however, the VREF output remains ON, provided that sufficient VCC and VDDQ voltages have been established.

When EN terminal repeats ON/OFF, an inrush current may flow in VTT\_IN terminal. Please be careful about voltage Drop of the VTT\_IN line.

## Absolute Maximum Ratings

Parameter	Symbol	Limit		Unit
		BD3539FVM	BD3539NUX	
Input Voltage	V <sub>CC</sub>	7 (Note 1)		V
Enable Input Voltage	V <sub>EN</sub>	7 (Note 1)		V
Termination Input Voltage	V <sub>TT_IN</sub>	7 (Note 1)		V
VDDQ Reference Voltage	V <sub>DDQ</sub>	7 (Note 1)		V
Output Current	I <sub>TT</sub>	1		A
Power Dissipation1	Pd1	0.38 (Note 2)	0.24 (Note 4)	W
Power Dissipation2	Pd2	0.58 (Note 3)	0.51 (Note 5)	W
Power Dissipation3	Pd3	-	0.87 (Note 6)	W
Operating Temperature Range	Topr	-30 to +100		°C
Storage Temperature Range	Tstg	-55 to +150		°C
Maximum Junction Temperature	Tjmax	+150		°C

(Note 1) Should not exceed Pd. Instantaneous surge voltage, back electromotive force and voltage under less than 10% duty cycle.

(Note 2) For Ta $\geq$ 25°C (With no heat sink)  $\theta_{ja}$ =322.6°C/W

(Note 3) For Ta $\geq$ 25°C when mounting a 70mm x 70mm x 1.6mm glass-epoxy substrate, with no heat sink  $\theta_{ja}$ =212.8°C/W

(Note 4) For Ta $\geq$ 25°C (With no heat sink)  $\theta_{ja}$ =516.5°C/W

(Note 5) For Ta $\geq$ 25°C when mounting a 70mm x 70mm x 1.6mm glass-epoxy substrate 1-layer board,  $\theta_{ja}$ =242.7°C/W

(Note 6) For Ta $\geq$ 25°C when mounting a 70mm x 70mm x 1.6mm glass-epoxy substrate 4-layer board (copper foil density: 5505mm<sup>2</sup> (copper foil area in each layer)),  $\theta_{ja}$ =142.5°C/W

**Caution:** Operating the IC over the absolute maximum ratings may damage the IC. In addition, it is impossible to predict all destructive situations such as short-circuit modes, open circuit modes, etc. Therefore, it is important to consider circuit protection measures, like adding a fuse, in case the IC is operated in a special mode exceeding the absolute maximum ratings.

## Recommended Operating Ratings (Ta=25°C)

Parameter	Symbol	Limit		Unit
		Min	Max	
Input Voltage	V <sub>CC</sub>	2.7	5.5	V
Termination Input Voltage	V <sub>TT_IN</sub>	1.0	5.5	V
VDDQ Reference Voltage	V <sub>DDQ</sub>	1.0	2.75	V
Enable Input Voltage	V <sub>EN</sub>	-0.3	+5.5	V

## Electrical Characteristics

(Unless otherwise noted, Ta=25°C, V<sub>CC</sub>=3.3V, V<sub>EN</sub>=3V, V<sub>DDQ</sub>=1.5V, V<sub>TT\_IN</sub>=1.5V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Standby Current	I <sub>STBY</sub>	-	0.5	1.0	mA	V <sub>EN</sub> =0V
Circuit Current	I <sub>CC</sub>	-	2	4	mA	V <sub>EN</sub> =3V
[Enable]						
High Level Enable Input Voltage	V <sub>ENHIGH</sub>	2.3	-	5.5	V	
Low Level Enable Input Voltage	V <sub>ENLOW</sub>	-0.3	-	+0.8	V	
Enable Pin Input Current	I <sub>EN</sub>	-	7	10	μA	V <sub>EN</sub> =3V
[Termination]						
Termination Output Voltage (DDR3)	V <sub>TT3</sub>	1/2xV <sub>DDQ</sub> -15m	1/2xV <sub>DDQ</sub>	1/2xV <sub>DDQ</sub> +15m	V	I <sub>TT</sub> =-1.0A to +1.0A Ta=0°C to 100°C
Termination Output Voltage (DDR2)	V <sub>TT2</sub>	1/2xV <sub>DDQ</sub> -30m	1/2xV <sub>DDQ</sub>	1/2xV <sub>DDQ</sub> +30m	V	V <sub>CC</sub> = 3.3V, V <sub>DDQ</sub> = 1.8V V <sub>TT_IN</sub> = 1.8V I <sub>TT</sub> =-1.0A to +1.0A Ta=0°C to 100°C
Termination Output Voltage (DDR1)	V <sub>TT1</sub>	1/2xV <sub>DDQ</sub> -30m	1/2xV <sub>DDQ</sub>	1/2xV <sub>DDQ</sub> +30m	V	V <sub>CC</sub> = 5.0V, V <sub>DDQ</sub> = 2.5V V <sub>TT_IN</sub> = 2.5V I <sub>TT</sub> =-1.0A to +1.0A Ta=0°C to 100°C
Source Current	I <sub>TT+</sub>	1.0	-	-	A	
Sink Current	I <sub>TT-</sub>	-	-	-1.0	A	
Load Regulation	ΔV <sub>TT</sub>	-	-	30	mV	I <sub>TT</sub> =-1.0A to +1.0A
Upper Side ON-Resistance	R <sub>ON_H</sub>	-	0.35	0.65	Ω	
Lower Side ON-Resistance	R <sub>ON_L</sub>	-	0.35	0.65	Ω	
[VDDQ]						
Input Impedance	Z <sub>VDDQ</sub>	140	200	260	kΩ	
[VREF]						
Output Voltage	V <sub>REF</sub>	1/2xV <sub>DDQ</sub> -15m	1/2xV <sub>DDQ</sub>	1/2xV <sub>DDQ</sub> +15m	V	I <sub>REF</sub> =-25mA to +25mA Ta=0°C to 100°C
[UVLO]						
Threshold Voltage	V <sub>UVLO</sub>	2.30	2.45	2.60	V	V <sub>CC</sub> : sweep up
Hysteresis Voltage	ΔV <sub>UVLO</sub>	100	160	220	mV	V <sub>CC</sub> : sweep down

Typical Performance Curves

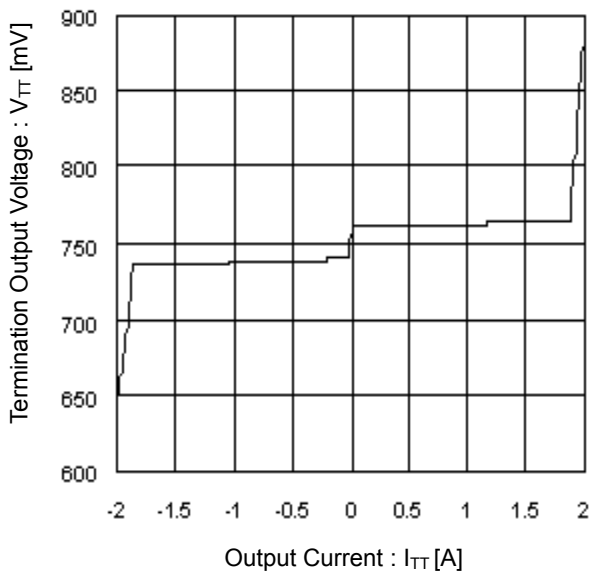


Figure 1. Termination Output Voltage vs Output Current (DDR3)

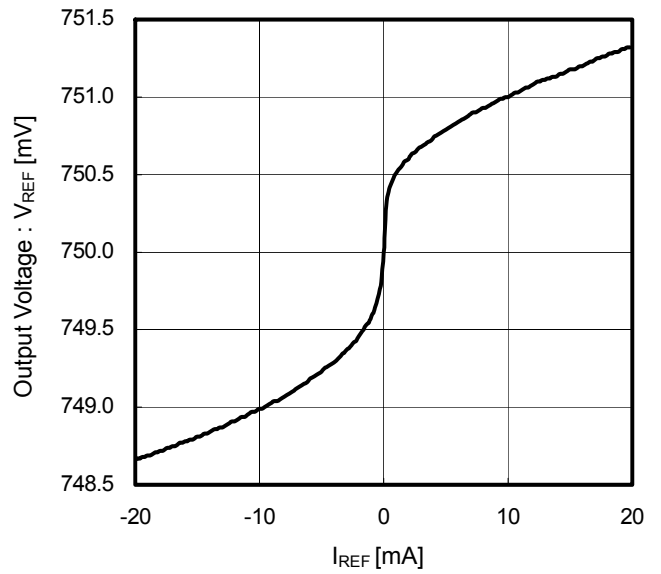


Figure 2. Output Voltage vs  $I_{REF}$  (DDR3)

Typical Waveforms

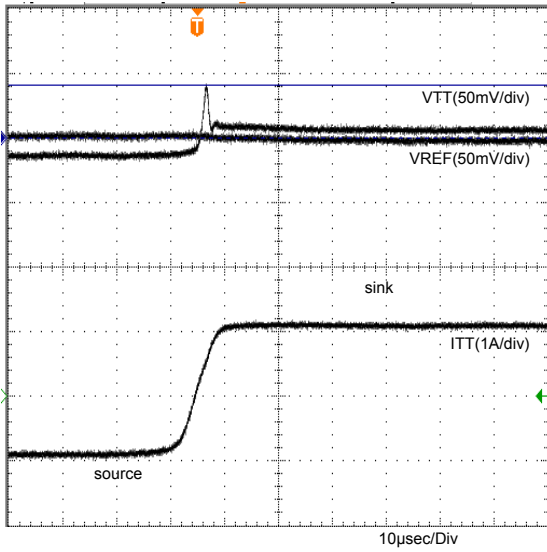


Figure 3. DDR3 (-1A to +1A)

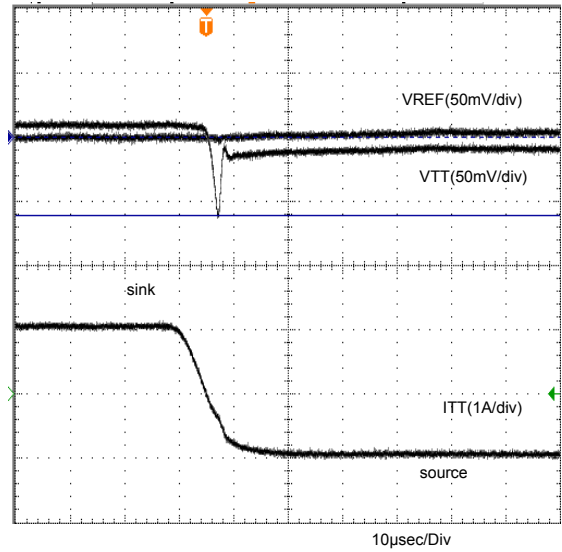


Figure 4. DDR3 (+1A to -1A)

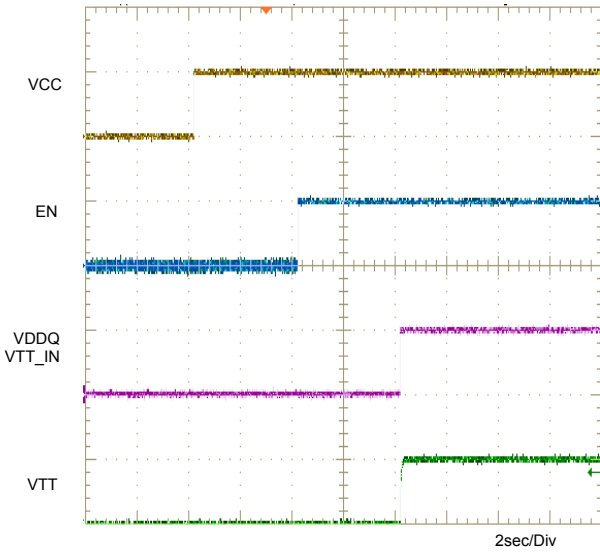


Figure 5. Input Sequence 1

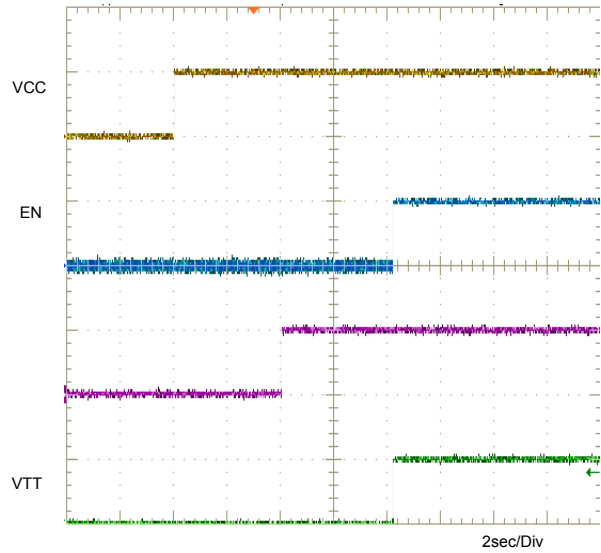


Figure 6. Input Sequence 2

Typical Waveforms – continued

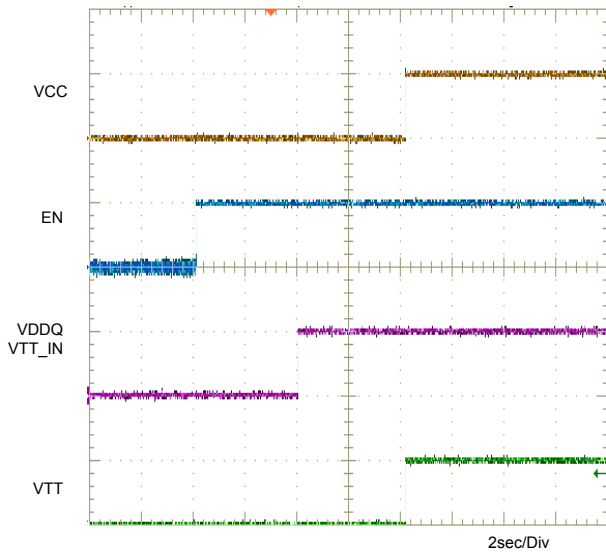


Figure 7. Input Sequence 3

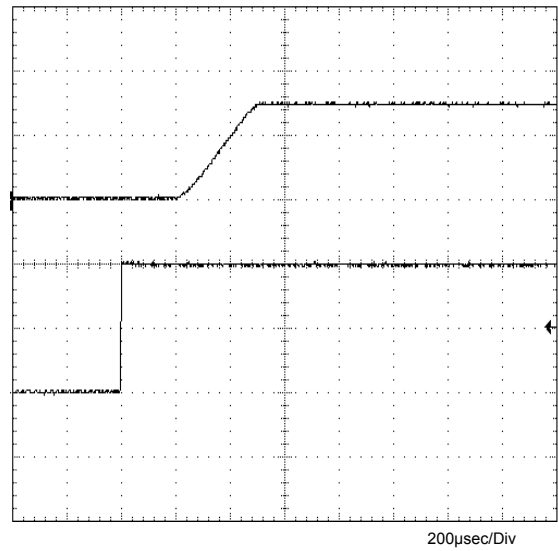


Figure 8. EN Soft Start

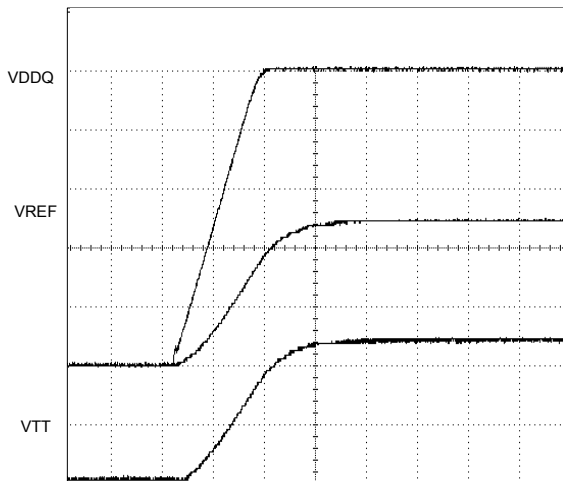
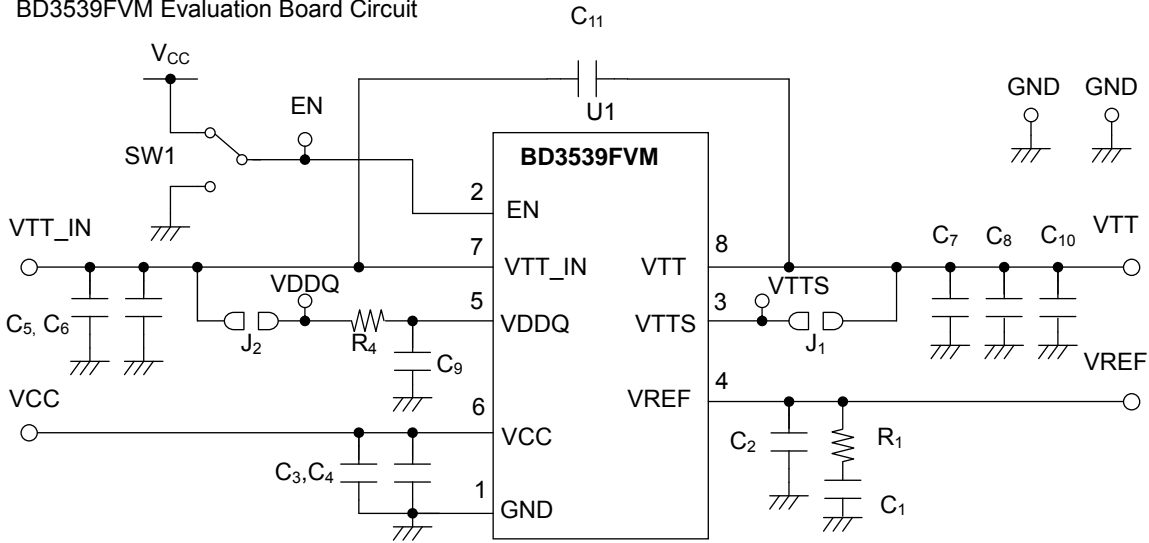


Figure 9. VDDQ Soft Start

Application Information

1. Evaluation Board

BD3539FVM Evaluation Board Circuit



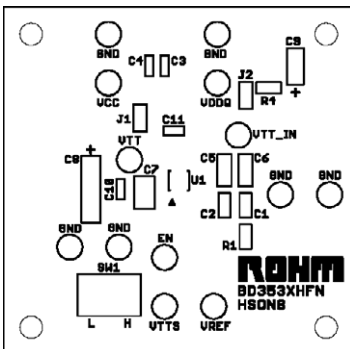
BD3539FVM Evaluation Board Application Components

Part No	Value	Company	Parts Name
U1	-	ROHM	BD3539FVM
R1	-	-	-
R4	220Ω	ROHM	MCR032200
J1	0Ω	-	-
J2	0Ω	-	-
C1	-	-	-
C2	1μF	KYOCERA	CM105B105K06A
C3	1μF	KYOCERA	CM105B105K06A

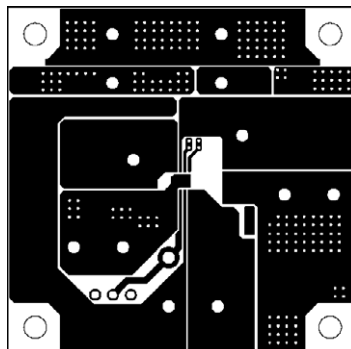
Part No	Value	Company	Parts Name
C4	-	-	-
C5	10μF	KYOCERA	CM21B106M06A
C6	-	-	-
C7	10μF	KYOCERA	CM21B106M06A
C8	-	-	-
C9	2.2μF	KYOCERA	CM105B225K06A
C10	-	-	-
C11	-	-	-

BD3539FVM Evaluation Board Layout

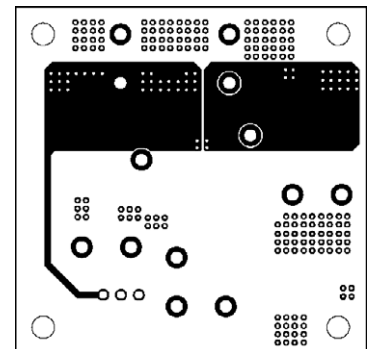
Silk Screen



Top Layer

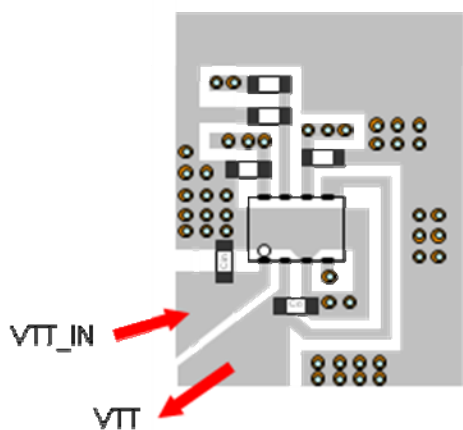


Bottom Layer

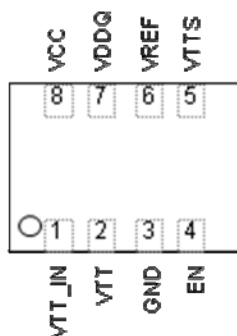




2. Example of Layout Pattern



[Example of Board Layout Pattern]



[Pin Configuration]

The input capacitor  $C_{in}$  of VTT\_IN should be placed as close as possible to VTT\_IN pin. Similarly, the VTT output capacitor should be placed as close as possible to the IC's pin. As for wiring pattern, make the pin wiring and the GND pattern as wide as possible. As for the metal trace connecting to the inner GND plane, please place many through holes.

Since VTTS pin has comparatively high impedance, floating capacitance should be as small as possible and design layout at upper layer pattern. Please be careful in drawing.

Please make the GND pattern space wide and design the layout with the ability to increase radiation efficiency.

### 3. Power Dissipation

In thermal design, consider the temperature range wherein the IC is guaranteed to operate and apply appropriate margins. The temperature conditions that need to be considered are listed below:

- (1) Ambient temperature  $T_a$ : 100°C or lower
- (2) Chip junction temperature  $T_j$ : 150°C or lower

The chip junction temperature  $T_j$  can be considered as follows:

- (a) Calculation based on IC surface temperature  $T_c$ , mounted on a board

$$T_j = T_c + \theta_j - c \times W$$

<Reference example>

$\theta_j$ -c:MSOP-8      46.0°C/W

PCB size: 70x70x1.6mm (Board copper foil area: 70x70mm<sup>2</sup>)

- (b) Calculation based on ambient temperature  $T_a$

$$T_j = T_a + \theta_j - a \times W$$

<Reference example>

$\theta_j$ -a:MSOP-8	212.8°C/W	With no heat sink
	322.6°C/W	1-layer board (copper foil area :70x70mm <sup>2</sup> )
$\theta_j$ -a:VSON008X2030	516.5°C/W	With no heat sink
	242.7°C/W	1-layer board(copper foil area:70x70mm <sup>2</sup> )
	142.5°C/W	4-layer board(copper foil area:70x70mm <sup>2</sup> )
	PCB size: 70x70x1.6mm <sup>3</sup> (with thermal via)	

Since the package has the FIN at the bottom of the IC, package power is considerably affected by the area of the copper foil where FIN is connected. In order to release heat, please make the board area large enough or add many through-holes to the inner layer pattern.

Most heat loss in BD3539 occurs at the output N-channel FET. The lost power is determined by multiplying the voltage between IN and OUT by the output current. Since this IC is packaged for high-power applications, its thermal derating characteristics significantly depend on the PC board. So when designing, the size of the PC board to be used should be carefully considered.

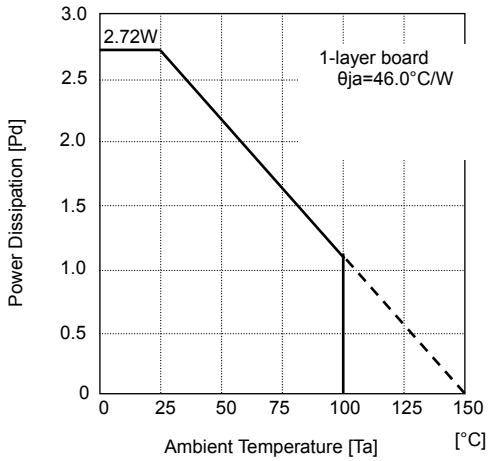
$$\text{Power consumption (W)} = \text{Input voltage (} V_{TT\_IN} \text{) - Output voltage (} V_{TT} \approx \frac{1}{2} V_{DDQ} \text{) } \times I_{OUT(Ave)}$$

Example) Where  $V_{TT\_IN} = 1.5V$ ,  $V_{DDQ} = 1.5V$ ,  $I_{OUT(Ave)} = 0.5A$

$$\begin{aligned} \text{Power consumption (W)} &= \{1.5(V) - 0.75(V)\} \times 0.5(A) \\ &= 0.375(W) \end{aligned}$$

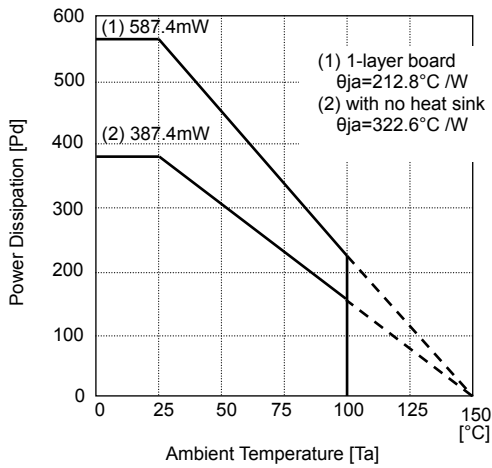
Heat Dissipation Characteristics [Tc]

MSOP8  
[W]

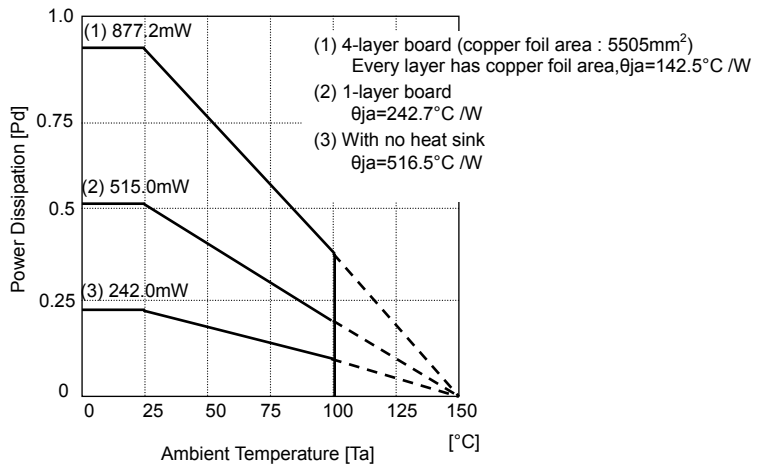


Heat Dissipation Characteristics [Ta]

MSOP8  
[mW]



VSON008X2030  
[W]



## Operational Notes

- 1. Reverse Connection of Power Supply**  
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply terminals.
- 2. Power Supply Lines**  
Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.
- 3. Ground Voltage**  
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.
- 4. Ground Wiring Pattern**  
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.
- 5. Thermal Consideration**  
Should by any chance the power dissipation rating be exceeded, the rise in temperature of the chip may result in deterioration of the properties of the chip. The absolute maximum rating of the Pd stated in this specification is when the IC is mounted on a 70mm x 70mm x 1.6mm glass epoxy board. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the Pd rating.
- 6. Recommended Operating Conditions**  
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.
- 7. Inrush Current**  
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.
- 8. Operation Under Strong Electromagnetic Field**  
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.
- 9. Testing on Application Boards**  
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned OFF completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.
- 10. Inter-pin Short and Mounting Errors**  
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.
- 11. Unused Input Terminals**  
Input terminals of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input terminals should be connected to the power supply or ground line.

## Operational Notes – continued

## 12. Regarding Input Pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When  $GND > Pin A$  and  $GND > Pin B$ , the P-N junction operates as a parasitic diode.  
When  $GND > Pin B$ , the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

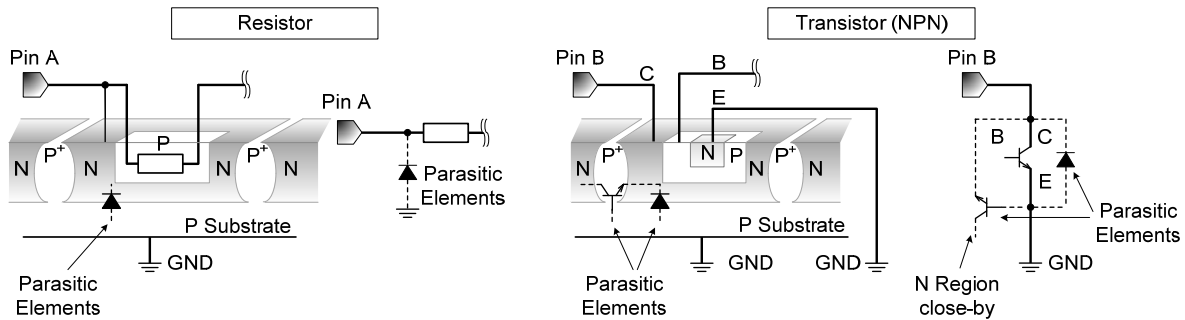


Figure 10. Example of Monolithic IC Structure

## 13. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's power dissipation rating. If however the rating is exceeded for a continued period, the junction temperature ( $T_j$ ) will rise which will activate the TSD circuit that will turn OFF all output pins. When the  $T_j$  falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

The present IC incorporates a thermal shutdown protection circuit (TSD circuit). The working temperature is  $175^\circ\text{C}$  (standard value) and has a  $-15^\circ\text{C}$  (standard value) hysteresis width.

## 14. Capacitor Across Output and GND

If a large capacitor is connected between the output pin and ground pin, current from the charged capacitor can flow into the output pin and may destroy the IC when the VCC or VTT\_IN pin is shorted to ground or pulled down to 0V. Use a capacitor smaller than  $1000\mu\text{F}$  between output and ground.

15. Output Capacitor, Resistor ( $C_1$ /Block Diagram)

Do not fail to connect a output capacitor to VREF output terminal for stabilization of output voltage. The capacitor connected to VREF output terminal works as a loop gain phase compensator. Insufficient capacitance may cause oscillation. It is recommended to use a low temperature coefficient  $1\text{-}10\mu\text{F}$  ceramic capacitor, though it depends on ambient temperature and load conditions. It is therefore requested to carefully check under the actual temperature and load conditions to be applied.

16. Output Capacitor ( $C_4$ )

Do not fail to connect a capacitor to VTT output pin for stabilization of output voltage. This output capacitor works as a loop gain phase compensator and an output voltage variation reducer in the event of sudden change in load. Insufficient capacitance may cause an oscillation. And if the equivalent series resistance (ESR) of this capacitor is high, the variation in output voltage increases in the event of sudden change in load. It is recommended to use a  $10\mu\text{F}$  or so ceramic capacitor, though it depends on ambient temperature and load conditions. It is therefore requested to carefully check under the actual temperature and load conditions to be applied.

## Operational Notes – continued

17. Input capacitors setting ( $C_2$  and  $C_3$ )

These input capacitors are used to reduce the output impedance of power supply to be connected to the input terminals (VCC and VTT\_IN). Increase in the power supply output impedance may result in oscillation or degradation in ripple rejecting characteristics. It is recommended to use a low temperature coefficient 1 $\mu$ F (for VCC) and 10 $\mu$ F (for VTT\_IN) capacitor, but it depends on the characteristics of the power supply input, and the capacitance and impedance of the pc board wiring pattern. It is therefore requested to carefully check under the actual temperature and load conditions to be applied.

## 18. Input Terminals (VCC, VDDQ, VTT\_IN and EN)

VCC, VDDQ, VTT\_IN and EN terminals of this IC are made up independent one another. To VCC terminal, the UVLO function is provided for malfunction protection. Irrespective of the input order of the inputs terminals, VTT output is activated to provide the output voltage when UVLO and EN voltages reach the threshold voltage while VREF output is activated when UVLO voltage reaches the threshold. If VDDQ and VTT\_IN terminals have equal potential and common impedance, any change in current at VTT\_IN terminal may result in variation of VTT\_IN voltage, which affects VDDQ terminal and may cause variation in the output voltage. It is therefore required to perform wiring in such manner that VDDQ and VTT\_IN terminals may not have common impedance. If impossible, take appropriate corrective measures including suitable CR filter to be inserted between VDDQ and VTT\_IN terminals.

## 19. VTTS terminal

This terminal is used to improve load regulation of VTT output. The connection with VTT terminal must be done so that it would not have a common impedance with high current line for better load regulation of VTT output.

## 20. Operating Range

Within the operating range, the operation and function of the circuits are generally guaranteed at an ambient temperature within the range specified. The values specified for electrical characteristics may not be guaranteed, but drastic change may not occur to such characteristics within the operating range.

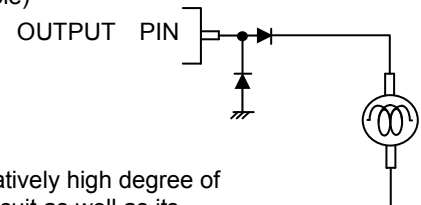
## 21. Allowable Loss Pd

For the allowable loss, the thermal derating characteristics are shown on page 12, which should be used as a guide. Any use that exceeds the allowable loss may result in degradation in the functions inherent to IC including a decrease in current capability due to chip temperature increase. Use within the allowable loss.

22. The use of the IC in the strong electromagnetic field may sometimes cause malfunction, to which care must be taken. In the event that a load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is recommended to insert a protection diode.

23. In the event that a load containing a large inductance component is connected to the output terminal, and generation of back-EMF at the start-up and when output is turned OFF is assumed, it is recommended to insert a protection diode.

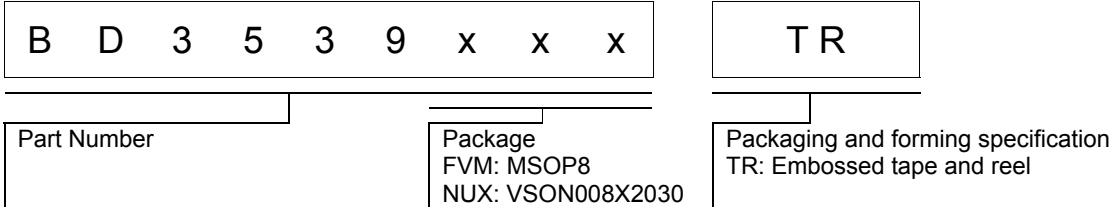
(Example)



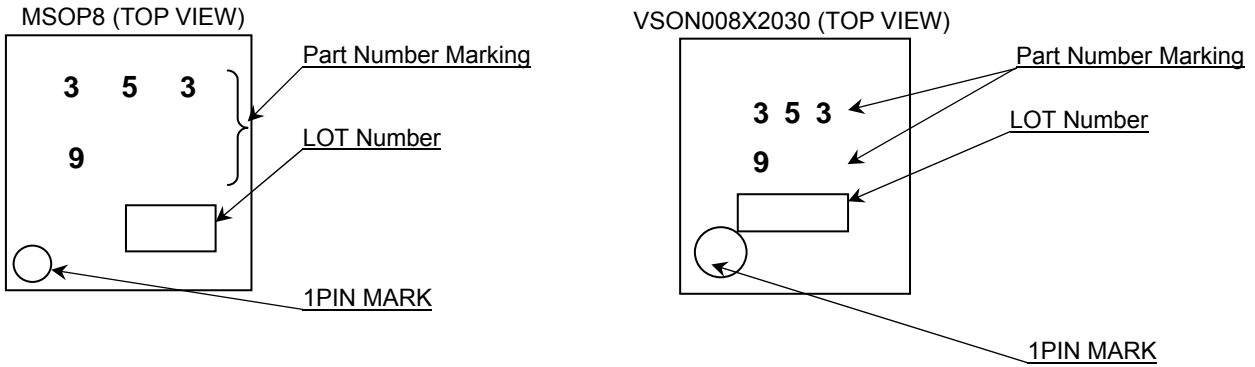
## 24. Application Circuit

Although we can recommend the application circuits contained herein with a relatively high degree of confidence, we ask that you verify all characteristics and specifications of the circuit as well as its performance under actual conditions. Please note that we cannot be held responsible for problems that may arise due to patent infringements or noncompliance with any and all applicable laws and regulations.

Ordering Information



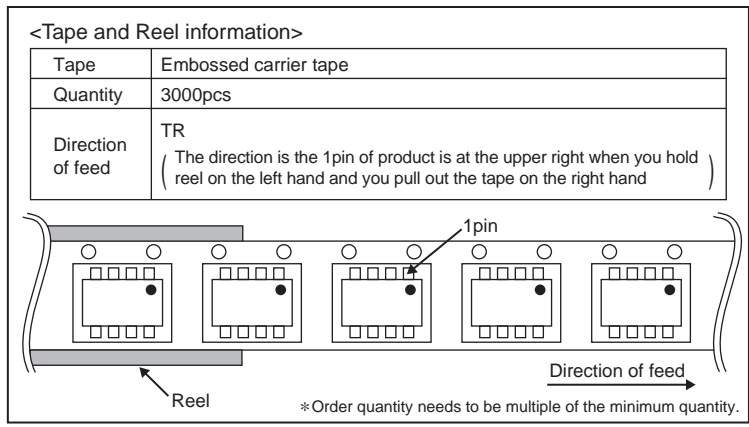
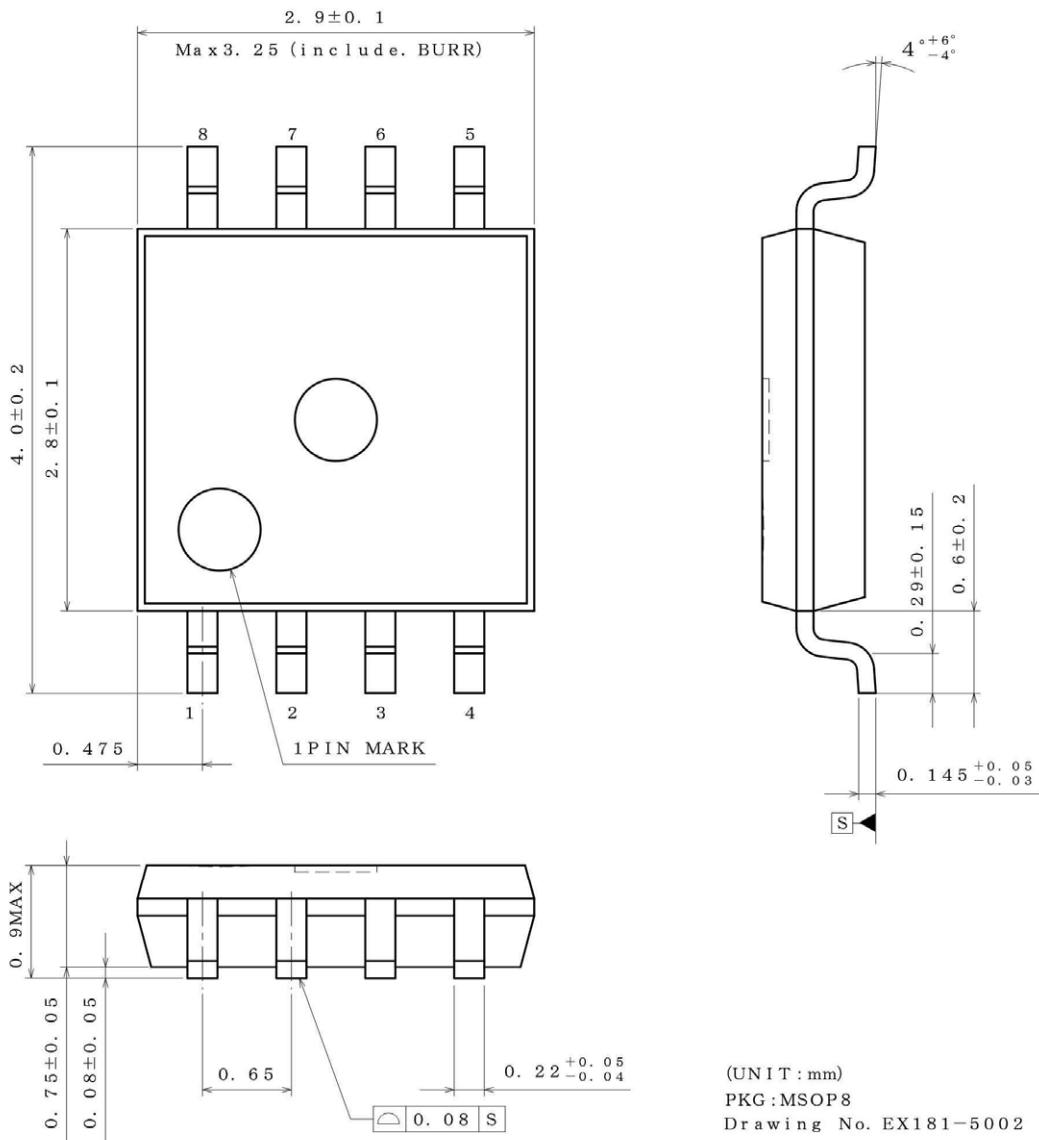
Marking Diagrams



Part Number Marking	Package	Orderable Part Number
3539	MSOP8	BD3539FVM-TR
3539	VSON008X2030	BD3539NUX-TR

Physical Dimension, Tape and Reel Information

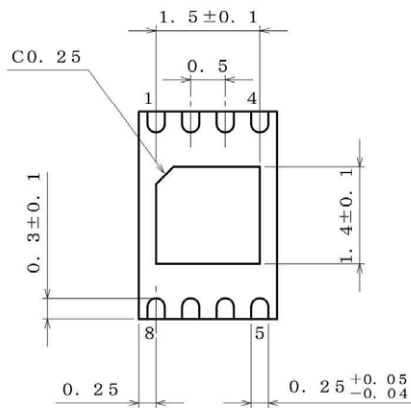
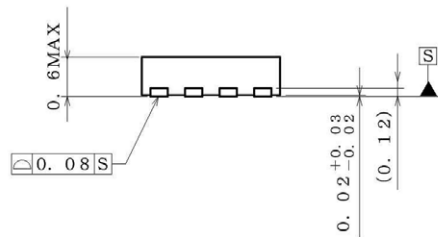
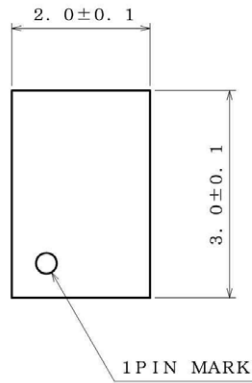
Package Name	MSOP8
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Physical Dimension, Tape and Reel Information – continued

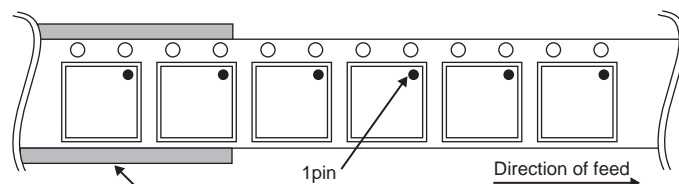
Package Name	VSON008X2030
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(UNIT : mm)  
 PKG : VSON008X2030  
 Drawing No. EX187-5001

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	4000pcs
Direction of feed	TR ( The direction is the 1pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand )



\*Order quantity needs to be multiple of the minimum quantity.

## Revision History

Date	Revision	Changes
07.Mar.2014	001	New Release
22.Jul.2015	002	Revised Applications

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
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CLASS IV		CLASS III	

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  - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
  - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
  - Sealing or coating our Products with resin or other coating materials
  - Use of our Products without cleaning residue of flux (even if you use no-clean type fluxes, cleaning residue of flux is recommended); or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
  - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation (Pd) depending on Ambient temperature (Ta). When used in sealed area, confirm the actual ambient temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

## Precaution for Mounting / Circuit board design

- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

**Precaution for Storage / Transportation**

1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
  - [a] the Products are exposed to sea winds or corrosive gases, including Cl<sub>2</sub>, H<sub>2</sub>S, NH<sub>3</sub>, SO<sub>2</sub>, and NO<sub>2</sub>
  - [b] the temperature or humidity exceeds those recommended by ROHM
  - [c] the Products are exposed to direct sunshine or condensation
  - [d] the Products are exposed to high Electrostatic
2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
3. Store / transport cartons in the correct direction, which is indicated on a carton with a symbol. Otherwise bent leads may occur due to excessive stress applied when dropping of a carton.
4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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