

Analog Sound Processors series

Sound Processor for car audio built-in 2nd order post filter

BD37067FV-M

General Description

It is built-in input selector of 6 stereo source and output to ADC after adjusting signal level. And built-in 2nd order post filter to reduce out of band noise and 6ch Volume circuit. Moreover, it is simple to design set by built-in TDMA noise reduction systems.

Features

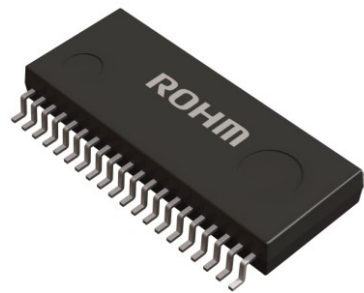
- AEC-Q100 (Grade3) Qualified
- Built-in differential input selector that can select single-ended / differential input
- Reduce the pop noise when switching gain due to built-in advanced switch circuit
- Less out-of-band noise of DAC by built-in 2nd order post filter.
- Built-in buffered ground isolation amplifier to realize high CMRR characteristics
- Built-in TDMA noise reduction circuit reduces the additional components for external filter.
- Package is SSOP-B40. Putting same direction input-terminals and output-terminals make PCB layout easier and PCB area smaller.
- Available to control by 3.3V / 5V for I²C-bus controller.

Key Specifications

- Total Harmonic Distortion : 0.003%(Typ)
- Maximum Input Voltage : 2.2V_{RMS}(Typ)
- Common Mode Rejection Ratio : 55dB(Min)
- Maximum Output Voltage : 2.1V_{RMS}(Typ)
- Output Noise Voltage : 8μV_{RMS}(Typ)
- Residual Output Noise Voltage : 2.5μV_{RMS}(Typ)
- Ripple Rejection: -70dB (Typ)
- Operating Temperature Range: -40 °C to +85°C

Package
SSOP-B40

W(Typ) x D(Typ) x H(Max)
13.60mm x 7.80mm x 2.00mm



SSOP-B40

Applications

It is the optimal for the car audio. Besides, it is possible to use for the audio equipment of mini Compo, micro Compo.

Typical Application Circuit

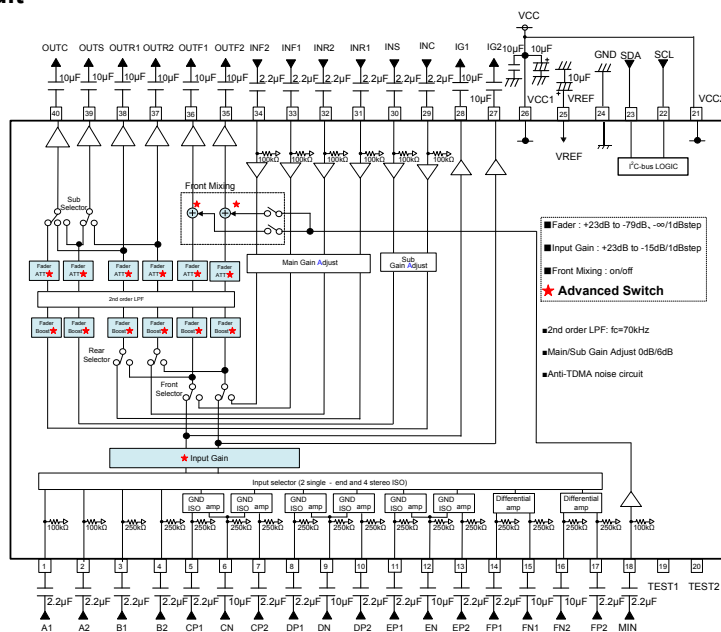


Figure 1. Typical Application Circuit

○Product structure : Silicon monolithic integrated circuit ○This product is not designed protection against radioactive rays.

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Contents

| | |
|--|----|
| General Description | 1 |
| Features | 1 |
| Applications | 1 |
| Key Specifications | 1 |
| Typical Application Circuit | 1 |
| Contents | 2 |
| Pin Configuration | 3 |
| Pin Descriptions | 3 |
| Block Diagram | 4 |
| Absolute Maximum Ratings (Ta=25°C) | 4 |
| Operating Range | 4 |
| Electrical Characteristic | 5 |
| Typical Performance Curve(s) | 7 |
| 1. Electrical specifications and timing for bus lines and I/O stages | 9 |
| 2. I ² C-bus Format | 10 |
| 3. I ² C-bus Interface Protocol | 10 |
| 4. Slave Address | 10 |
| 5. Select Address & Data | 11 |
| 6. About power on reset | 17 |
| 7. About start-up and power off sequence on IC | 17 |
| About Advanced Switch Circuit | 19 |
| Application Example | 25 |
| Thermal Derating Curve | 26 |
| I/O Equivalence Circuit | 27 |
| Application Information | 29 |
| 1. Absolute maximum rating voltage | 29 |
| 2. About a signal input part | 29 |
| 3. About output load characteristics | 29 |
| 4. About TEST1,2 terminal(19,20pin) | 30 |
| 5. About signal input terminals | 30 |
| 6. About changing gain of Input Gain and Fader Volume | 30 |
| Operational Notes | 31 |
| 1. Reverse Connection of Power Supply | 31 |
| 2. Power Supply Lines | 31 |
| 3. Ground Voltage | 31 |
| 4. Ground Wiring Pattern | 31 |
| 5. Thermal Consideration | 31 |
| 6. Recommended Operating Conditions | 31 |
| 7. Inrush Current | 31 |
| 8. Operation Under Strong Electromagnetic Field | 31 |
| 9. Testing on Application Boards | 31 |
| 10. Inter-pin Short and Mounting Errors | 32 |
| 11. Regarding the Input Pin of the IC | 32 |
| Ordering Name Selection | 33 |
| Physical Dimension Tape and Reel Information | 33 |
| Marking Diagram | 33 |
| Revision History | 34 |

Block Diagram

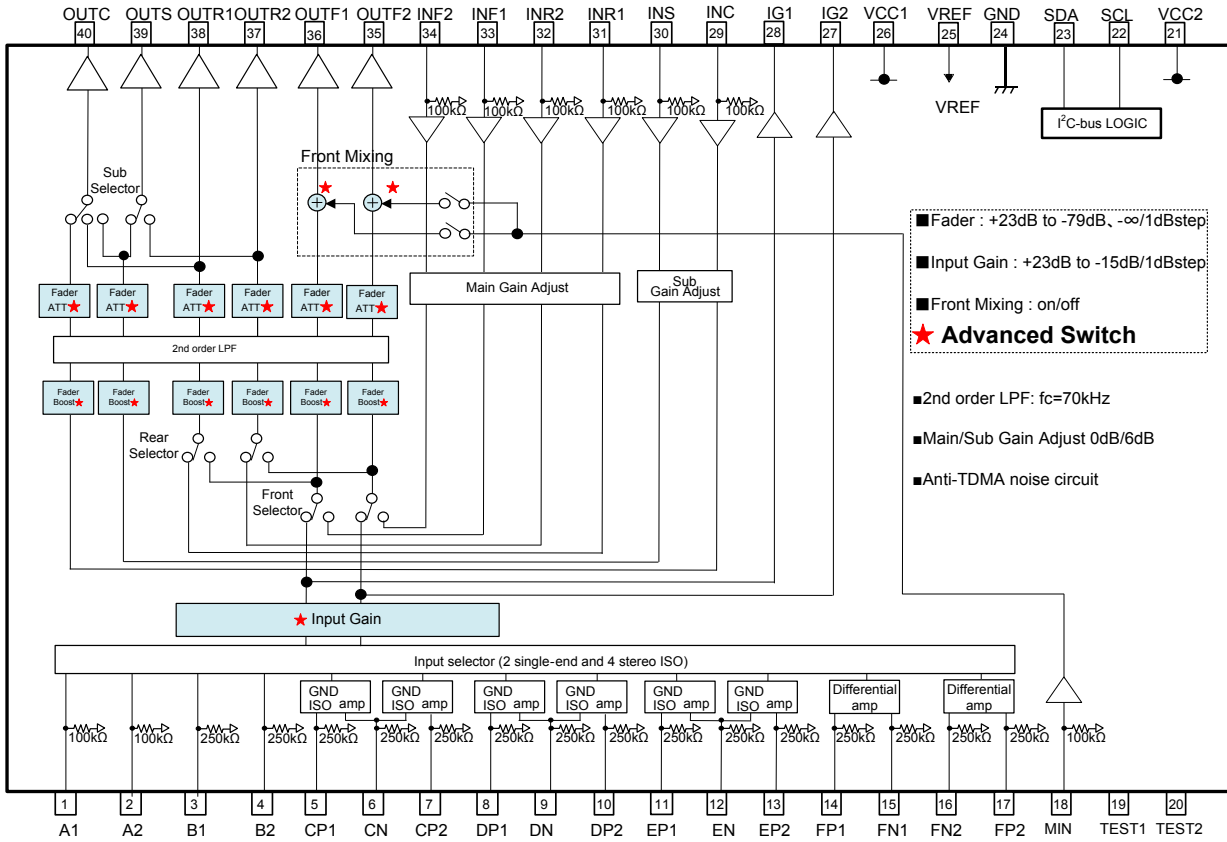


Figure 3. Block diagram and pin assign

Absolute Maximum Ratings (Ta=25°C)

| Parameter | Symbol | Rating | Unit |
|----------------------|------------------|--|------|
| Power Supply Voltage | VCC (VCC1,2) | 10 | V |
| Input Voltage | V _{IN} | VCC+0.3 to GND-0.3 Only SCL, SDA 7 to GND-0.3 | V |
| Power Dissipation | P _d | 1.12 ^(Note1) | W |
| Storage Temperature | T _{STG} | -55 to +150 | °C |

(Note1) This value decreases 9mW/°C for Ta=25°C or more.
 ROHM standard board shall be mounted. Thermal resistance $\theta_{ja} = 111.1(^{\circ}\text{C}/\text{W})$.
 ROHM Standard board size : 70x70x1.6(mm)
 material : A FR4 glass epoxy board(3% or less of copper foil area)

Operating Range

| Parameter | Symbol | Min | Typ | Max | Unit |
|----------------------|--------------|-----|-----|-----|------|
| Power Supply Voltage | VCC (VCC1,2) | 7.0 | 8.5 | 9.5 | V |
| Temperature | Topr | -40 | - | +85 | °C |

Electrical Characteristic

(Unless specified particularly, Ta=25°C, VCC1,2=8.5V, f=1kHz, VIN=1VRMS, RG=600Ω, RL=10kΩ,
A input, Input Gain 0dB, Gain Adjust +6dB, LPF ON, Fader 0dB, Input point=A1/A2, Monitor point=IG1/IG2)

| Block | Parameter | Symbol | Limit | | | Unit | Conditions |
|----------------|--|---------|-------|-------|------|-------|---|
| | | | Min | Typ | Max | | |
| General | Current upon no signal (IQ_VCC1+IQ_VCC2) | IQ_VCC | — | 35 | 53 | mA | No signal |
| Input Selector | Input Impedance (A) | RIN_S | 70 | 100 | 130 | kΩ | |
| | Input Impedance (B, C, D, E, F) | RIN_D | 175 | 250 | 325 | kΩ | |
| | Voltage Gain | GV | -1.5 | +0 | +1.5 | dB | GV=20log(VOUT/VIN) |
| | Channel Balance | CB | -1.5 | +0 | +1.5 | dB | CB = GV1-GV2 |
| | Total Harmonic Distortion | THD+N | — | 0.003 | 0.05 | % | VOUT =1VRMS BW=400-30kHz |
| | Output Noise Voltage ^(Note1) | VNO1 | — | 3.1 | 8.0 | μVRMS | RG = 0Ω BW = IHF-A |
| | Maximum Input Voltage | VIM | 2.0 | 2.2 | — | VRMS | VIM at THD+N(VOUT)=1% BW=400-30kHz |
| | Crosstalk Between Channels ^(Note1) | CTC | — | -100 | -90 | dB | RG = 0Ω CTC=20log(VOUT/VOUT') BW = IHF-A |
| | Crosstalk Between Selectors ^(Note1) | CTS | — | -100 | -90 | dB | RG = 0Ω CTS=20log(VOUT/VOUT') BW = IHF-A |
| | Common Mode Rejection Ratio (C, D, E, F) ^(Note1) | CMRR | 55 | 65 | — | dB | XP1 and XN input XP2 and XN input CMRR=20log(VIN/VOUT) BW = IHF-A, [X=C,D,E,F] |
| Input Gain | Minimum Input Gain | GIN_MIN | -17 | -15 | -13 | dB | Input gain -15dB GIN=20log(VOUT/VIN) |
| | Maximum Input Gain | GIN_MAX | 21 | 23 | 25 | dB | Input gain 23dB VIN =100mVRMS GIN=20log(VOUT/VIN) |
| | Gain Set Error | GIN_ERR | -2 | +0 | +2 | dB | GAIN=-15 to +23dB |
| | Output Impedance | ROUT | - | — | 50 | Ω | VIN =100mVRMS |
| | Maximum Output Voltage | VOM | 2.0 | 2.2 | — | VRMS | THD+N=1% BW=400-30kHz |

(Note1) VP-9690A (Average value detection, effective value display) filter by Panasonic is used for measurement. Input and output are in-phase.

(Unless specified particularly, Ta=25°C, VCC1,2=8.5V, f=1kHz, VIN=0.9VRMS, RG=600Ω, RL =10kΩ,
A input, Input Gain 0dB, Gain Adjust +6dB, LPF ON, Fader 0dB,
Input point=INF1/INF2/INR1/INR2/INC/INS, Monitor point=OUTF1/OUTF2/OUTR1/OUTR2/OUTC/OUTS)

| Block | Parameter | Symbol | Limit | | | Unit | Conditions |
|--------|------------------------|--------|-------|-----|-----|------|--------------------------|
| | | | Min | Typ | Max | | |
| Output | Output Impedance | ROUT | - | — | 50 | Ω | VIN =100mVRMS |
| | Maximum Output Voltage | VOM | 2.0 | 2.1 | — | VRMS | THD+N=1% BW=400-30kHz |

(Unless specified particularly, Ta=25°C, VCC1,2=8.5V, f=1kHz, V_{IN}=0.9V_{RMS}, R_G=600Ω, R_L=10kΩ,
A input, Input Gain 0dB, Gain Adjust +6dB, LPF ON, Fader 0dB,
Input point=INF1/INF2/INR1/INR2/INC/INS, Monitor point=OUTF1/OUTF2/OUTR1/OUTR2/OUTC/OUTS)

| Block | Parameter | Symbol | Limit | | | Unit | Conditions |
|------------------|--|---------------------|-------|-------|------|--|--|
| | | | Min | Typ | Max | | |
| Fader | Maximum Boost Gain | G _{F BST} | 21 | 23 | 25 | dB | Gain=23dB V _{IN} =100mV _{RMS} G _F =20log(V _{OUT} /V _{IN}) Gain Adjust=0dB |
| | Channel Balance | CB | -1.5 | +0 | +1.5 | dB | CB = G _{V1} -G _{V2} |
| | Total Harmonic Distortion | THD+N | — | 0.003 | 0.05 | % | BW=400-30KHz |
| | Output Noise Voltage ^(Note1) | V _{NO1} | — | 8 | 16 | μV _{RMS} | R _G = 0Ω BW = IHF-A |
| | Residual Output Noise Voltage ^(Note1) | V _{NOR} | — | 2.5 | 8.0 | μV _{RMS} | Fader = -∞dB R _G = 0Ω BW = IHF-A |
| | Maximum Input Voltage | V _{IM} | 2.0 | 2.1 | — | V _{RMS} | V _{IM} at THD+N(V _{OUT})=1% BW=400-30KHz Gain Adjust = 0dB |
| | Crosstalk Between Channels ^(Note1) | CTC | — | -100 | -90 | dB | R _G = 0Ω CTC=20log(V _{OUT} /V _{OUT'}) BW = IHF-A |
| | Maximum Attenuation ^(Note1) | G _{F MIN} | — | -100 | -90 | dB | Fader = -∞dB G _F =20log(V _{OUT} / V _{IN}) BW = IHF-A |
| | Gain Set Error | G _{F ERR} | -2 | +0 | +2 | dB | Gain=+1 to +23dB |
| | Attenuation Set Error 1 | G _{F ERR1} | -2 | +0 | +2 | dB | Attenuation=0 to -15dB |
| | Attenuation Set Error 2 | G _{F ERR2} | -3 | +0 | +3 | dB | Attenuation=-16 to -47dB |
| | Attenuation Set Error 3 | G _{F ERR3} | -4 | +0 | +4 | dB | Attenuation=-48 to -79dB |
| Ripple Rejection | PSRR | — | -70 | -40 | dB | f=1kHz V _{RR} =100mV _{RMS} RR _{VCC} =20log(V _{OUT} /VCC) | |
| Mixing | Input Impedance | R _{IN_M} | 70 | 100 | 130 | kΩ | |
| | Maximum Input voltage | V _{IM_M} | 2.0 | 2.2 | - | V _{RMS} | V _{IM} at THD+N(V _{OUT})=1% BW=400-30KHz MIN input |
| | Maximum Attenuation ^(Note1) | G _{MX MIN} | - | -100 | -85 | dB | Front Mixing=OFF G _{MX} =20log(V _{OUT} /V _{IN}) BW=IHF-A MIN input |
| | Mixing Gain | G _{MX} | -2 | +0 | +2 | dB | Front Mixing=ON G _{MX} =20log(V _{OUT} /V _{IN}) |
| Gain Adjust | Input Impedance | R _{IN_M} | 70 | 100 | 130 | kΩ | |
| | Boost Gain | G _{F BST} | 4 | 6 | 8 | dB | Gain=6dB V _{IN} =100mV _{RMS} G _F =20log(V _{OUT} /V _{IN}) |
| | Channel Balance | CB | -1.5 | +0 | +1.5 | dB | CB = G _{V1} -G _{V2} |

(Note1) VP-9690A (Average value detection, effective value display) filter by Panasonic is used for measurement. Input and output are in-phase.

Typical Performance Curve(s)

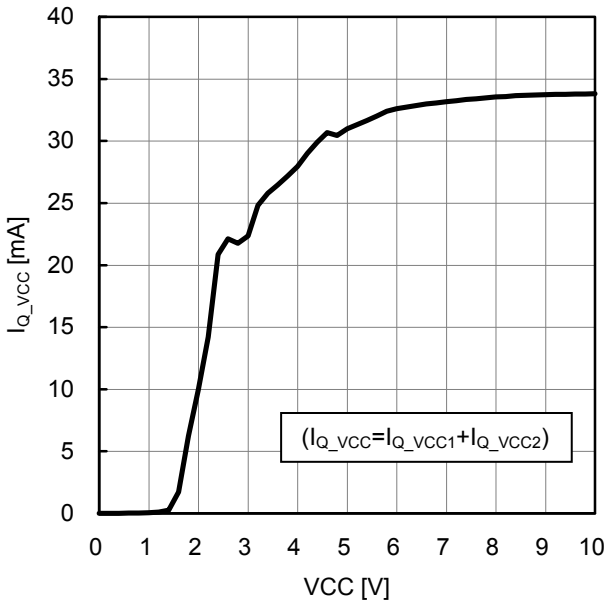


Figure 4. Iq_vcc vs. VCC

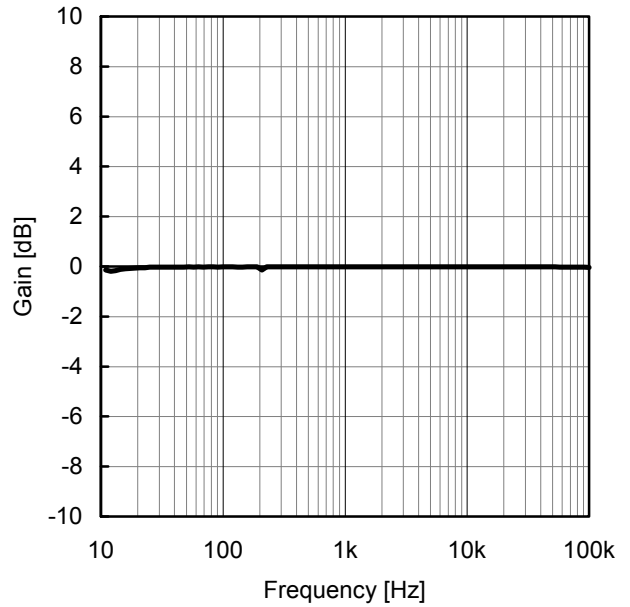


Figure 5. Gain vs. Frequency

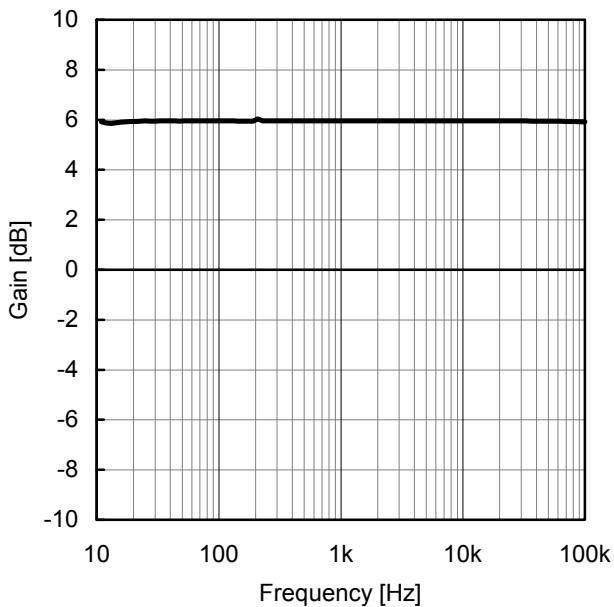


Figure 6. Gain vs. Frequency (Gain Adjust=+6dB)

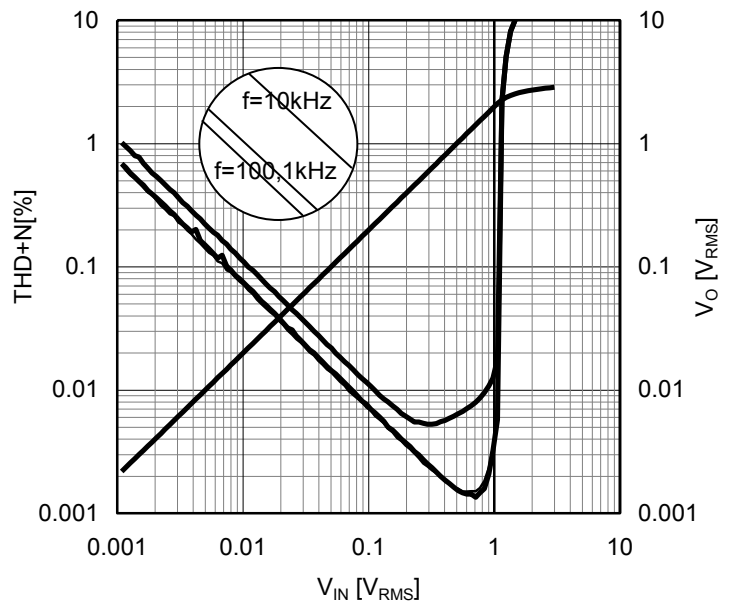


Figure 7. THD+N, VO vs VIN (Gain Adjust=+6dB)

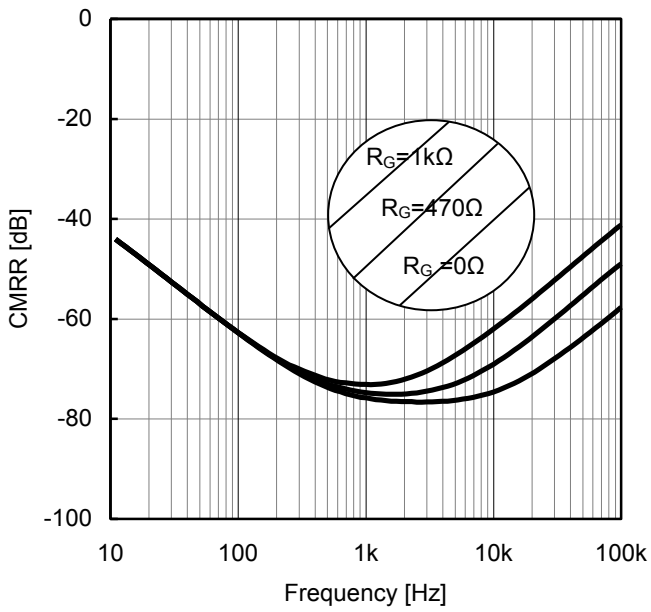


Figure 8. CMRR vs. Frequency

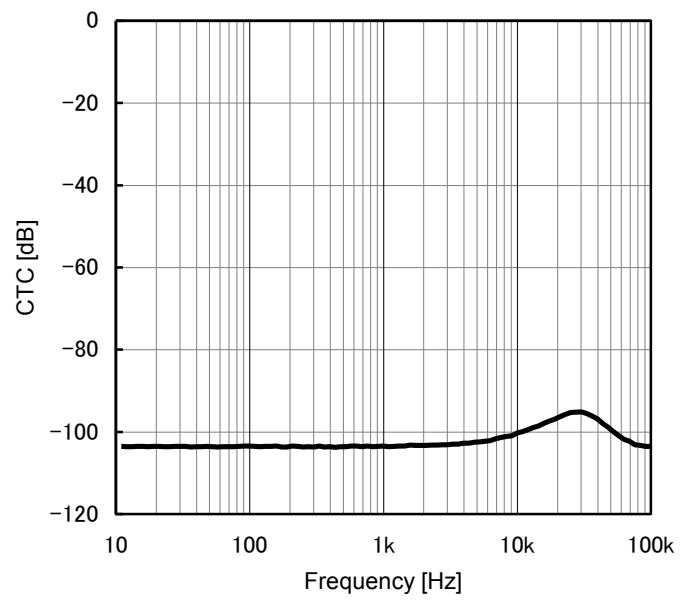


Figure 9. CTC vs. Frequency

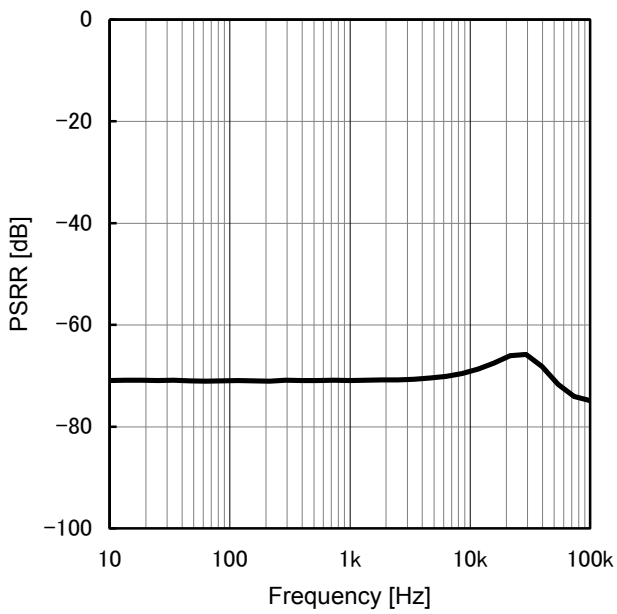


Figure 10. PSRR vs. Frequency

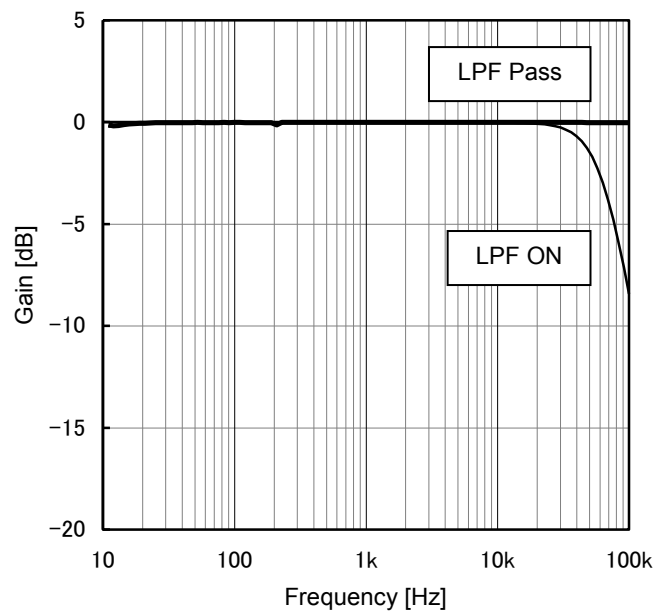


Figure 11. Gain vs. Frequency (LPF ON/Pass)

I²C-bus Control Signal Specification

1. Electrical specifications and timing for bus lines and I/O stages

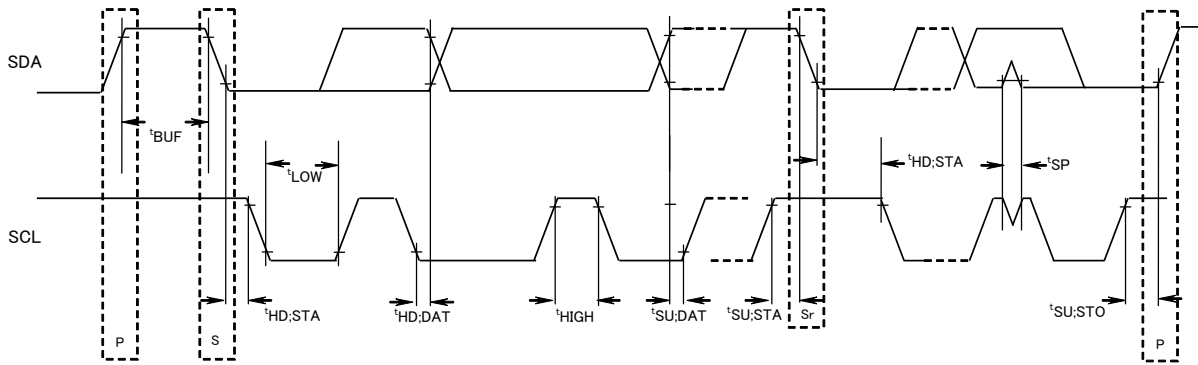


Figure 12. Definition of timing on the I²C-bus

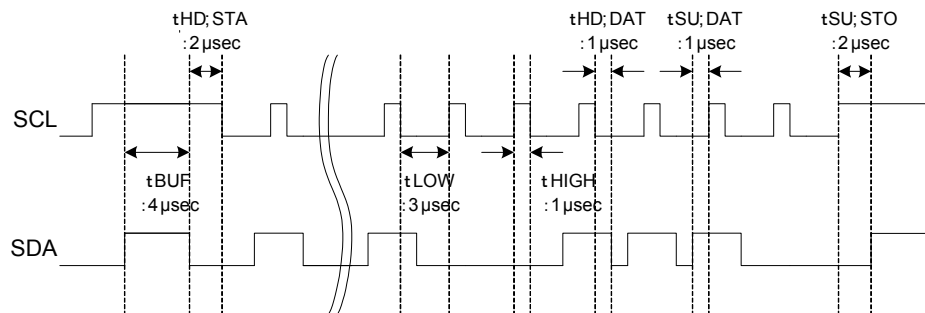
Table 1. Characteristics of the SDA and SCL bus lines for I²C-bus devices

| Parameter | Symbol | Fast-mode I ² C-bus | | Unit |
|---|---------|--------------------------------|-----|------|
| | | Min | Max | |
| 1 SCL Clock Frequency | fSCL | 0 | 400 | kHz |
| 2 Bus Free time between a STOP and START condition | tBUF | 1.3 | — | μsec |
| 3 Hold Time (repeated) START condition. After this period, the first clock pulse is generated | tHD;STA | 0.6 | — | μsec |
| 4 LOW Period of the SCL Clock | tLOW | 1.3 | — | μsec |
| 5 HIGH Period of the SCL Clock | tHIGH | 0.6 | — | μsec |
| 6 Set-up time for a Repeated START Condition | tSU;STA | 0.6 | — | μsec |
| 7 Data Hold Time | tHD;DAT | 0* | — | μsec |
| 8 Data set-up Time | tSU;DAT | 100 | — | μsec |
| 9 Set-up Time for STOP Condition | tSU;STO | 0.6 | — | μsec |

All values referred to VIH min. and VIL max. Levels (see Table 2.).

Table 2. Characteristics of the SDA and SCL I/O stages for I²C- bus devices

| Parameter | Symbol | Fast-mode I ² C-bus | | Unit |
|---|----------------|--------------------------------|-----|------|
| | | Min | Max | |
| 10 LOW level input voltage: Fixed input levels | VIL | -0.5 | +1 | V |
| 11 HIGH level input voltage: Fixed input levels | VIH | 2.3 | - | V |
| 12 Pulse width of spikes, which must be suppressed by the input filter. | tSP | 0 | 50 | nsec |
| 13 LOW level output voltage (open drain or open collector): At 3mA sink current | VOL1 | 0 | 0.4 | V |
| 14 Input current each I/O pin with an input voltage between 0.4V and 0.9 VDD max. | I _i | -10 | +10 | μA |



SCL clock frequency: 250kHz

Figure 13. I²C data transmission timing

2. I²C-bus Format

| | | | | | | | |
|------|---------------|------|----------------|------|------|------|------|
| MSB | LSB | MSB | LSB | MSB | LSB | | |
| S | Slave Address | A | Select Address | A | Data | A | P |
| 1bit | 8bit | 1bit | 8bit | 1bit | 8bit | 1bit | 1bit |

- S = Start condition (Recognition of start bit)
- Slave Address = Recognition of slave address. 7 bits in upper order are optional.
The last bit must be "L" for writing.
- A = Acknowledge bit (Recognition of acknowledgement)
- Select Address = Address for each function
- Data = Data of each function
- P = Stop condition (Recognition of stop bit)

3. I²C-bus Interface Protocol

1) Basic form

| | | | | | | | |
|-----|---------------|-----|----------------|-----|------|---|---|
| S | Slave Address | A | Select Address | A | Data | A | P |
| MSB | LSB | MSB | LSB | MSB | LSB | | |

2) Automatic increment(Select Address increases (+1) according to the number of data)

| | | | | | | | | | | | | |
|-----|---------------|-----|----------------|-----|-------|-----|-------|-----|-----|--------|-----|---|
| S | Slave Address | A | Select Address | A | Data1 | A | Data2 | A | ... | Data N | A | P |
| MSB | LSB | MSB | LSB | MSB | LSB | MSB | LSB | MSB | LSB | MSB | LSB | |

- (Example)①Data 1 shall be set as data of address specified by Select Address.
 ②Data 2 shall be set as data of address specified by Select Address +1.
 ③Data N shall be set as data of address specified by Select Address +(N-1).

3) Configuration unavailable for transmission (In this case, only Select Address 1 is set.)

| | | | | | | | | | | | |
|-----|---------------|-----|-----------------|-----|------|-----|------------------|-----|------|-----|-----|
| S | Slave Address | A | Select Address1 | A | Data | A | Select Address 2 | A | Data | A | P |
| MSB | LSB | MSB | LSB | MSB | LSB | MSB | LSB | MSB | LSB | MSB | LSB |

(Note)If any data is transmitted as Select Address 2 next to data, It is recognized as data, not as Select Address 2.

4. Slave Address

| | | | | | | | | | |
|-----|----|----|----|----|----|----|----|-----|-----|
| MSB | A6 | A5 | A4 | A3 | A2 | A1 | A0 | R/W | LSB |
| | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |

80(hex)

5. Select Address & Data

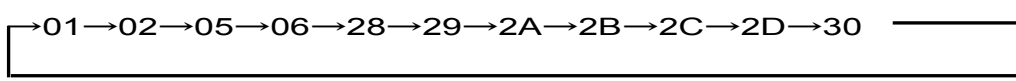
| Items | Select Address (hex) | MSB | | Data | | | | | | LSB | |
|------------------|----------------------|--------------------------|--------|--|----|----------------|----|-----------------|------------------|-----|--|
| | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | | |
| Initial Setup 1 | 01 | Advanced Switch ON/OFF | 0 | Advanced Switch time of Input Gain/Fader | | 0 | 0 | 0 | 0 | | |
| Initial Setup 2 | 02 | 0 | 0 | Sub Selector | | 0 | 0 | Rear Selector | Front Selector | | |
| Input Selector | 05 | 0 | 0 | 0 | 0 | Input Selector | | | | | |
| Input Gain | 06 | 0 | 0 | Input Gain | | | | | | | |
| Fader 1ch Front | 28 | Fader Gain / Attenuation | | | | | | | | | |
| Fader 2ch Front | 29 | Fader Gain / Attenuation | | | | | | | | | |
| Fader 1ch Rear | 2A | Fader Gain / Attenuation | | | | | | | | | |
| Fader 2ch Rear | 2B | Fader Gain / Attenuation | | | | | | | | | |
| Fader Center | 2C | Fader Gain / Attenuation | | | | | | | | | |
| Fader Subwoofer | 2D | Fader Gain / Attenuation | | | | | | | | | |
| LPF setup Mixing | 30 | Front Mixing ON/OFF | LPF fc | 0 | 0 | 0 | 0 | Sub Gain Adjust | Main Gain Adjust | | |
| System Reset | FE | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | | |

 Advanced switch

Note) Set up bit (It is written with "0" by the above table) which hasn't been used in "0".

Notes on data format

1. "Advanced switch" function is available for the hatched parts on the above table.
2. In case of transferring data continuously, Select Address(hex) flows by Automatic increment function, as shown below.



3. Input selector that is not corresponded for "Advanced switch" function, cannot reduce the noise caused when changing the input selector. Therefore, it is recommended to turn on mute when changing these settings.
4. In case of setting to infinite "-∞" by using Fader when input selector setting is changed, please consider "Advanced switch" time.

Select Address 01 (hex)

| Mode | Advanced Switch time of Input Gain/Fader | | | | | | | LSB |
|-----------|--|----|----|----|----|----|----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| 4.7 msec | Advanced Switch ON/OFF | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| 7.1 msec | | | 0 | 1 | | | | |
| 11.2 msec | | | 1 | 0 | | | | |
| 14.4 msec | | | 1 | 1 | | | | |

| Mode | Advanced Switch ON/OFF | | | | | | | LSB |
|------|------------------------|----|--|----|----|----|----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| OFF | 0 | 0 | Advanced Switch time of Input Gain/Fader | | 0 | 0 | 0 | 0 |
| ON | 1 | | 0 | 0 | 0 | 0 | 0 | |

Select Address 02 (hex)

| Mode | Front Selector | | | | | | LSB | |
|----------------|----------------|----|---------------|----|----|----|---------------|----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| FRONT | 0 | 0 | Sub Selector | | 0 | 0 | Rear Selector | 0 |
| INSIDE THROUGH | | | Rear Selector | 1 | | | | |

| Mode | Rear Selector | | | | | | LSB | |
|------------|---------------|----|--------------|----|----|----|-----|----------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| REAR | 0 | 0 | Sub Selector | | 0 | 0 | 0 | Front Selector |
| FRONT COPY | | | 1 | | | | | |

| Mode ^(Note1) | Sub Selector | | | | | | LSB | |
|--------------------------|--------------|----|----|----|----|----|---------------|----------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| OUTC(INS) OUTS(INS) | 0 | 0 | 0 | 0 | 0 | 0 | Rear Selector | Front Selector |
| OUTC(INR1) OUTS(INR2) | | | 0 | 1 | | | | |
| OUTC (INC) OUTS(INS) | | | 1 | 0 | | | | |
| Prohibition | | | 1 | 1 | | | | |

(Note1) xxx(INxx) : "xxx" means "Output terminal", "(INxx)" means "Output signal"

 : Initial condition

Select Address 05 (hex)

| Mode | MSB | | Input Selector | | | | LSB | |
|-------------|-----|----|----------------|----|----|----|-----|----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| A | | | | | 0 | 0 | 0 | 0 |
| B single | | | | | 0 | 0 | 0 | 1 |
| C single | | | | | 0 | 0 | 1 | 0 |
| D single | | | | | 0 | 0 | 1 | 1 |
| E single | | | | | 0 | 1 | 0 | 0 |
| F single | | | | | 0 | 1 | 0 | 1 |
| C diff | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 0 |
| D diff | | | | | 0 | 1 | 1 | 1 |
| E diff | | | | | 1 | 0 | 0 | 0 |
| F full-diff | | | | | 1 | 0 | 0 | 1 |
| Prohibition | | | | | 1 | 0 | 1 | 0 |
| | | | | | : | : | : | : |
| | | | | | 1 | 1 | 1 | 1 |

: Initial condition

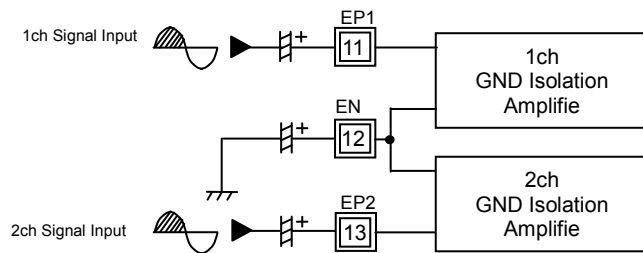
List of active input terminal when set input selector

| Mode | Lch positive input terminal | Lch negative input terminal | Rch positive input terminal | Rch negative input terminal |
|-------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| A | 1pin(A1) | - | 2pin(A2) | - |
| B | 3pin(B1) | - | 4pin(B2) | - |
| C single | 5pin(CP1) | - | 7pin(CP2) | - |
| D single | 8pin(DP1) | - | 10pin(DP2) | - |
| E single | 11pin(EP1) | - | 13pin(EP2) | - |
| F single | 14pin(FP1) | - | 17pin(FP2) | - |
| C diff | 5pin(CP1) | 6pin(CN) | 7pin(CP2) | 6pin(CN) |
| D diff | 8pin(DP1) | 9pin(DN) | 10pin(DP2) | 9pin(DN) |
| E diff | 11pin(EP1) | 12pin(EN) | 13pin(EP2) | 12pin(EN) |
| F full-diff | 14pin(FP1) | 15pin(FN1) | 17pin(FP2) | 16pin(FN2) |

[About Ground Isolation Amplifier]

Ground Isolation Amplifier : C diff to E diff

Please select this mode when you use them as a ground isolation amplifier.



Full Differential Amplifier : F full-diff

Please select this mode when you use it as a differential amplifier

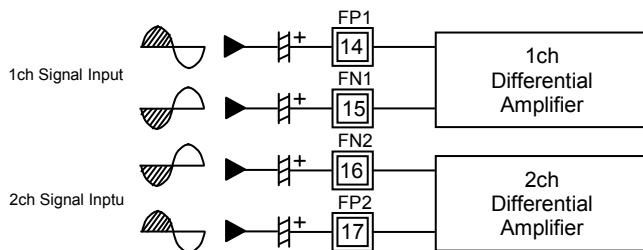


Figure 14. About Ground Isolation Amplifier

Select Address 06 (hex)

| Mode | MSB | | Input Gain | | | | | LSB |
|-------------|-----|----|------------|----|----|----|----|-----|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
| Prohibition | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| | | | : | : | : | : | : | : |
| 0 | | | 0 | 1 | 0 | 0 | 0 | |
| +23dB | | | 0 | 0 | 1 | 0 | 0 | 1 |
| +22dB | | | 0 | 0 | 1 | 0 | 1 | 0 |
| +21dB | | | 0 | 0 | 1 | 0 | 1 | 1 |
| +20dB | | | 0 | 0 | 1 | 1 | 0 | 0 |
| +19dB | | | 0 | 0 | 1 | 1 | 0 | 1 |
| +18dB | | | 0 | 0 | 1 | 1 | 1 | 0 |
| +17dB | | | 0 | 0 | 1 | 1 | 1 | 1 |
| +16dB | | | 0 | 1 | 0 | 0 | 0 | 0 |
| +15dB | | | 0 | 1 | 0 | 0 | 0 | 1 |
| +14dB | | | 0 | 1 | 0 | 0 | 1 | 0 |
| +13dB | | | 0 | 1 | 0 | 0 | 1 | 1 |
| +12dB | | | 0 | 1 | 0 | 1 | 0 | 0 |
| +11dB | | | 0 | 1 | 0 | 1 | 0 | 1 |
| +10dB | | | 0 | 1 | 0 | 1 | 1 | 0 |
| +9dB | | | 0 | 1 | 0 | 1 | 1 | 1 |
| +8dB | | | 0 | 1 | 1 | 0 | 0 | 0 |
| +7dB | | | 0 | 1 | 1 | 0 | 0 | 1 |
| +6dB | | | 0 | 1 | 1 | 0 | 1 | 0 |
| +5dB | | | 0 | 1 | 1 | 0 | 1 | 1 |
| +4dB | | | 0 | 1 | 1 | 1 | 0 | 0 |
| +3dB | | | 0 | 1 | 1 | 1 | 0 | 1 |
| +2dB | | | 0 | 1 | 1 | 1 | 1 | 0 |
| +1dB | | | 0 | 1 | 1 | 1 | 1 | 1 |
| 0dB | | | 1 | 0 | 0 | 0 | 0 | 0 |
| -1dB | | | 1 | 0 | 0 | 0 | 0 | 1 |
| -2dB | | | 1 | 0 | 0 | 0 | 1 | 0 |
| -3dB | | | 1 | 0 | 0 | 0 | 1 | 1 |
| -4dB | | | 1 | 0 | 0 | 1 | 0 | 0 |
| -5dB | | | 1 | 0 | 0 | 1 | 0 | 1 |
| -6dB | 1 | 0 | 0 | 1 | 1 | 0 | | |
| -7dB | 1 | 0 | 0 | 1 | 1 | 1 | | |
| -8dB | 1 | 0 | 1 | 0 | 0 | 0 | | |
| -9dB | 1 | 0 | 1 | 0 | 0 | 1 | | |
| -10dB | 1 | 0 | 1 | 0 | 1 | 0 | | |
| -11dB | 1 | 0 | 1 | 0 | 1 | 1 | | |
| -12dB | 1 | 0 | 1 | 1 | 0 | 0 | | |
| -13dB | 1 | 0 | 1 | 1 | 0 | 1 | | |
| -14dB | 1 | 0 | 1 | 1 | 1 | 0 | | |
| -15dB | 1 | 0 | 1 | 1 | 1 | 1 | | |
| Prohibition | 1 | 1 | 0 | 0 | 0 | 0 | | |
| | : | : | : | : | : | : | | |
| | 1 | 1 | 1 | 1 | 1 | 1 | | |

: Initial condition

Select Address 28, 29, 2A, 2B, 2C, 2D (hex)

| Gain & ATT | MSB | | Fader Gain / Attenuation | | | | | LSB | |
|-------------|-----|----|--------------------------|----|----|----|----|-----|--|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| Prohibition | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | |
| | : | : | : | : | : | : | : | : | |
| | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | |
| +23dB | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | |
| +22dB | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | |
| +21dB | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | |
| +10dB | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | |
| +9dB | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | |
| +8dB | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | |
| +7dB | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | |
| +6dB | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | |
| +5dB | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | |
| +4dB | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | |
| +3dB | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | |
| +2dB | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | |
| +1dB | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |
| 0dB | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | |
| -1dB | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | |
| -2dB | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | |
| -3dB | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | |
| ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | ⋮ | |
| -78dB | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | |
| -79dB | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | |
| Prohibition | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | |
| | : | : | : | : | : | : | : | : | |
| | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | |
| -∞dB | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | |

 : Initial condition


Select Address 30(hex)

| Mode | Main Gain Adjust | | | | | | | LSB | |
|------|------------------|--------|----|----|----|----|-----------------|-----|--|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0dB | Front Mixing | LPF fc | 0 | 0 | 0 | 0 | Sub Gain Adjust | 0 | |
| +6dB | | | | | | | | 1 | |

| Mode | Sub Gain Adjust | | | | | | | LSB | |
|------|-----------------|--------|----|----|----|----|----|-----|------------------|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 0dB | Front Mixing | LPF fc | 0 | 0 | 0 | 0 | 0 | | Main Gain Adjust |
| +6dB | | | | | | | 1 | | |

| Mode | LPF fc | | | | | | | LSB | |
|-------|--------------|----|----|----|----|----|-----------------|------------------|--|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| 70kHz | Front Mixing | 0 | 0 | 0 | 0 | 0 | Sub Gain Adjust | Main Gain Adjust | |
| PASS | | 1 | | | | | | | |

| Mode | Front Mixing ON/OFF | | | | | | | LSB | |
|------|---------------------|--------|----|----|----|----|-----------------|------------------|--|
| | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| OFF | 0 | LPF fc | 0 | 0 | 0 | 0 | Sub Gain Adjust | Main Gain Adjust | |
| ON | 1 | | | | | | | | |

 : Initial condition

6. About power on reset

It is possible for the reset circuit inside the IC to initialize when supply voltage is turned on. Please send data to all address as initial data when the supply is turned on, and turn on mute until all initial data are sent.

| Item | Symbol | Limit | | | Unit | Condition |
|--|------------|-------|-----|-----|-----------------|-----------------------------|
| | | Min | Typ | Max | | |
| Rise time of VCC1,2 | t_{RISE} | 33 | — | — | μsec | VCC rise time from 0V to 5V |
| VCC1,2 voltage of release power on reset | V_{POR} | — | 4.1 | — | V | |

7. About start-up and power off sequence on IC

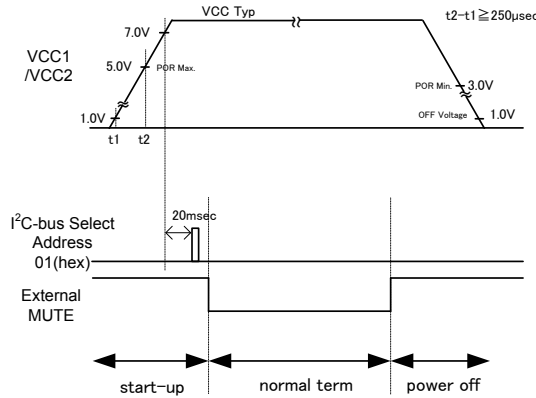


Figure 15. Power off and start-up sequence

This IC will become active-state by sending data of Select Address 01(hex) on I²C-bus after 20msec from that VCC1 and VCC2 reaches over 7.0V. Therefore, this command must always send in start-up sequence. In addition, External MUTE means recommended period that the muting outside IC.

About output terminal(27,28,35 to 40pin) vs. VCC

Bias voltage of output terminal (27,28,35 to 40pin) keep fixed voltage in operational range of VCC.

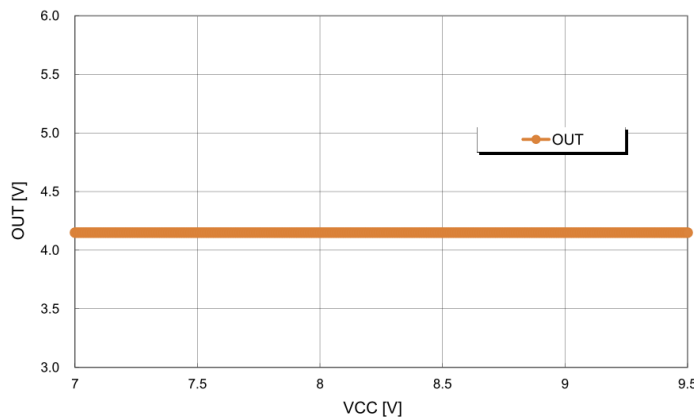


Figure 16. OUT(27,28,35 to 40pin)_DC-Bias = 4.15V fixed.

Fader Volume Attenuation of the Detail

| (dB) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | (dB) | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
|------|----|----|----|----|----|----|----|----|------|----|----|----|----|----|----|----|----|
| +23 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 1 | -29 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |
| +22 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 0 | -30 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 0 |
| +21 | 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | -31 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| +20 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | -32 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 |
| +19 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | -33 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 1 |
| +18 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | -34 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 |
| +17 | 0 | 1 | 1 | 0 | 1 | 1 | 1 | 1 | -35 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 1 |
| +16 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | -36 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| +15 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | -37 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| +14 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 0 | -38 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 0 |
| +13 | 0 | 1 | 1 | 1 | 0 | 0 | 1 | 1 | -39 | 1 | 0 | 1 | 0 | 0 | 1 | 1 | 1 |
| +12 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 0 | -40 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 |
| +11 | 0 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | -41 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 |
| +10 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | -42 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 |
| +9 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | -43 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 |
| +8 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | -44 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 |
| +7 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 1 | -45 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 1 |
| +6 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | -46 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 |
| +5 | 0 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | -47 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 |
| +4 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | -48 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| +3 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 1 |
| +2 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 0 |
| +1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | -51 | 1 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | -52 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 0 |
| -1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | -53 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| -2 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | -54 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 |
| -3 | 1 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | -55 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 1 |
| -4 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | -56 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 |
| -5 | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 1 | -57 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 1 |
| -6 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 0 | -58 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 0 |
| -7 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | -59 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 |
| -8 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | -60 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| -9 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 1 | -61 | 1 | 0 | 1 | 1 | 1 | 1 | 0 | 1 |
| -10 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 0 | -62 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 0 |
| -11 | 1 | 0 | 0 | 0 | 1 | 0 | 1 | 1 | -63 | 1 | 0 | 1 | 1 | 1 | 1 | 1 | 1 |
| -12 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | -64 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 |
| -13 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 1 | -65 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 1 |
| -14 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | -66 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 0 |
| -15 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | -67 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 |
| -16 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | -68 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 0 |
| -17 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 1 | -69 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | 1 |
| -18 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | -70 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 0 |
| -19 | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 1 | -71 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 |
| -20 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 0 | -72 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| -21 | 1 | 0 | 0 | 1 | 0 | 1 | 0 | 1 | -73 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| -22 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | -74 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| -23 | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 1 | -75 | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| -24 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 0 | -76 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 |
| -25 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | -77 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 1 |
| -26 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | -78 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 0 |
| -27 | 1 | 0 | 0 | 1 | 1 | 0 | 1 | 1 | -79 | 1 | 1 | 0 | 0 | 1 | 1 | 1 | 1 |
| -28 | 1 | 0 | 0 | 1 | 1 | 1 | 0 | 0 | -∞ | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |

 : Initial condition

About Advanced Switch Circuit

【1】 Advanced switch technology
1-1. Advanced switch effects

Advanced switch technology is ROHM original technology that can prevent from switching pop noise. If changing the gain setting (for example Fader) immediately, the audible signal will become discontinuously and pop noise will be occurred. This Advanced switch technology will prevent this discontinuous signal by completing the signal waveform and will significantly reduce the noise.

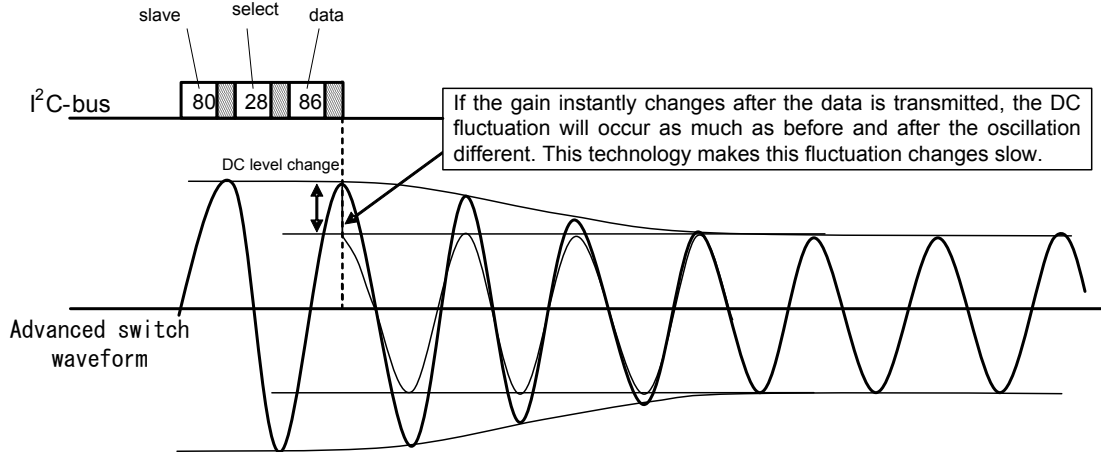


Figure 17. The explanation of advanced switch waveform

This Advanced switch circuit will start operating when the data is transmitted from microcontroller. Advanced switch waveform is shown as the figure above. For preventing switching noise, this IC will operate optimally by internal processing after the data is transmitted from microcontroller.

However, sometimes the switching waveform is not like the intended form depends on the transmission timing. Therefore, below is the example of the relationship between the transmission timing and actual switching time. Please consider this relationship for the setting.

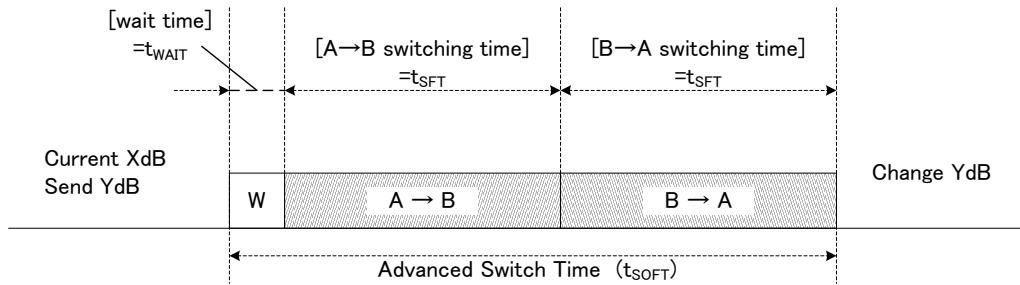
1-2. The kind of the Transferring Data

- Data setting that is not corresponded to Advanced switch
(Page11 Select Address & Data Data format without hatching)
There is no particular rule about transferring data.
- Data setting that is corresponded to Advanced switch
(Page11 Select Address & Data Data format with hatching)
There is no particular rule about transferring data, but Advanced switch must follow the switching sequence as mentioned in 【2】 as follows.

[2] Data transmission that is corresponded to Advanced switch

2-1. Switching time of Advanced switch

Switching time includes [t_{WAIT} (Wait time)], [t_{SFT} (A→B switching time)] and [t_{SFT} (B→A switching time)].
 25msec is needed per 1 switching. ($t_{SOFT} = t_{WAIT} + 2 * t_{SFT}$, $t_{WAIT} = 2.3msec$, $t_{SFT} = 11.2msec$)



In the figure above, Start/Stop state is expressed as “A” and temporary state is expressed as “B”.
 The switching sequence of Advanced switch consists of the cycle “A(start)→B(temporary)→A(stop)”. Therefore, switching sequence will not stop at B state.

For example, switching is performed from A(Initial gain)→B(set gain)→A(set gain) when switching from initial gain to set gain. And switching time (t_{SFT}) of A→B or B→A are equal.

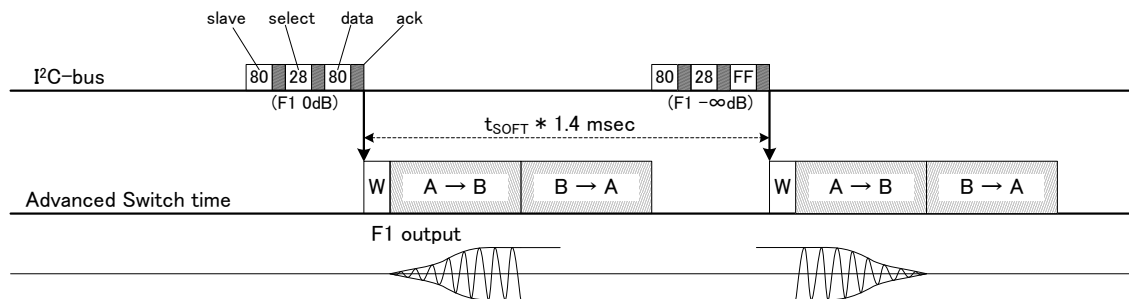
2-2. About the data transmission's timing in same block state and switching operation

■ Transmitting example 1

This is an example when transmitting data in same block with “enough interval for data transmission”.
 (enough interval for data transmission : $1.4 \times t_{SOFT}$ * “1.4” includes tolerance margin.)

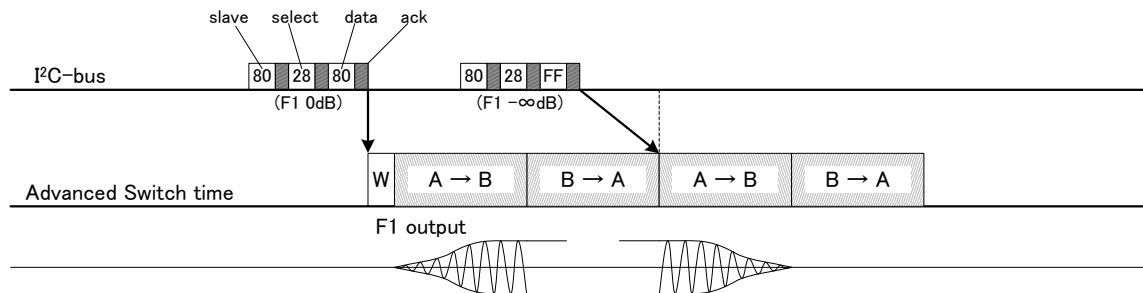
Definition of example expression :

F1=Fader 1ch Front, F2=Fader 2ch Front, R1=Fader 1ch Rear, R2=Fader 2ch Rear
 C=Fader Center, S=Fader Subwoofer, MIX=Front Mixing



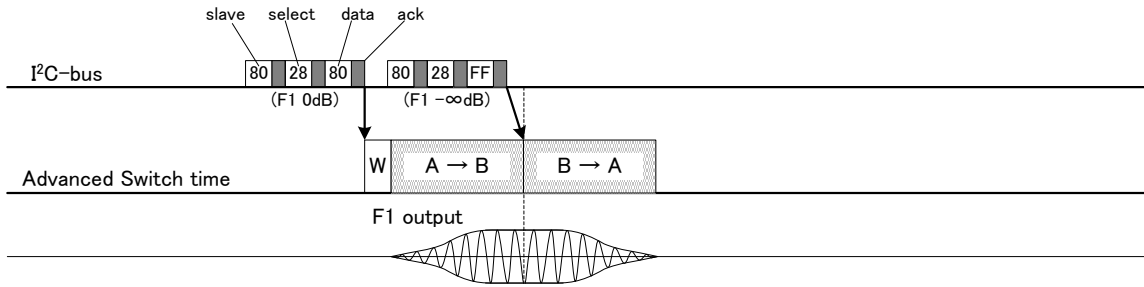
■ Transmitting example 2

This is an example when the transmission interval is not enough (smaller than “Transmission example 1”). When the data is transmitted during first switching operation, the second data will be reflected after the first switching operation. In this case, there is no wait time (t_{WAIT}) before the second switching operation.



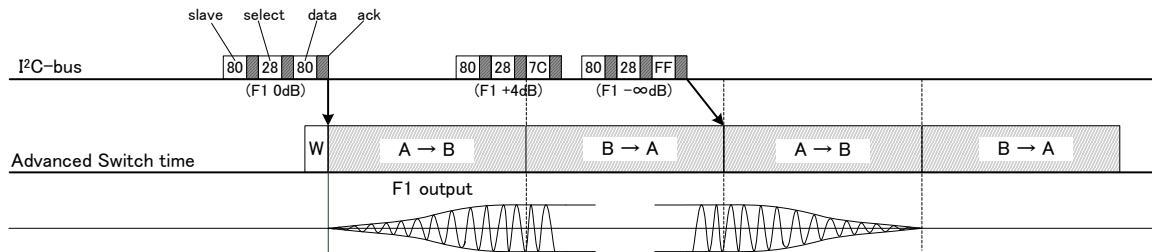
■ Transmitting example 3

This is an example of switching operation when transmission interval is smaller than “Transmission example 2”). When the data is transmitted during the first switching operation, and transmission timing is just during A→B switching operation, the second data will be reflected at B→A switching term.



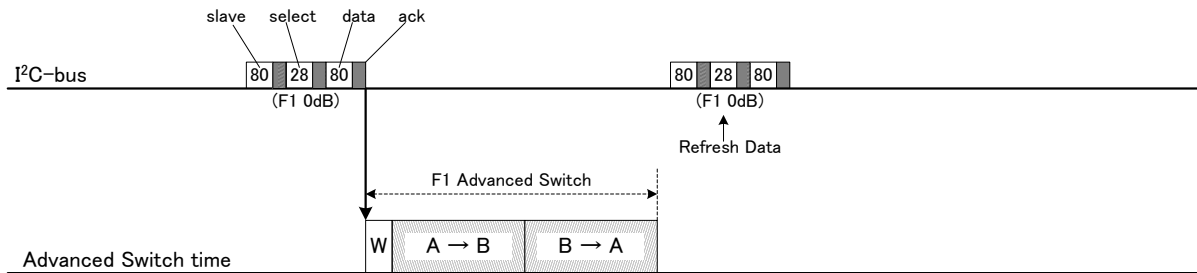
■ Transmitting example 4

The below figure shows an example of switching operation that the data are transmitted serially with smaller transmission interval than “Transmission example 3”. IC has internal data-storage buffer and buffer transmitted data as storage data constantly. However, only the latest data is kept so, in this example, +4dB data transmitted secondly is ignored.



■ Transmitting example 5

Transmitted data is firstly buffered and written to setting data which set gain. However, when there is no difference between transmitted data and setting data such as refresh data, advanced switch operation doesn't start.

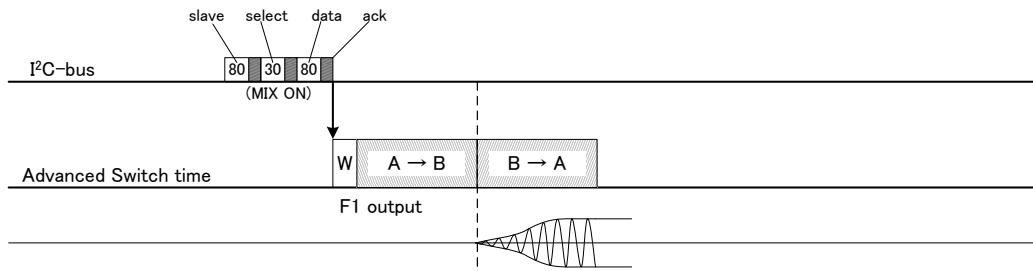


2-3. Mixing ON/OFF switching operation of Front Mixing

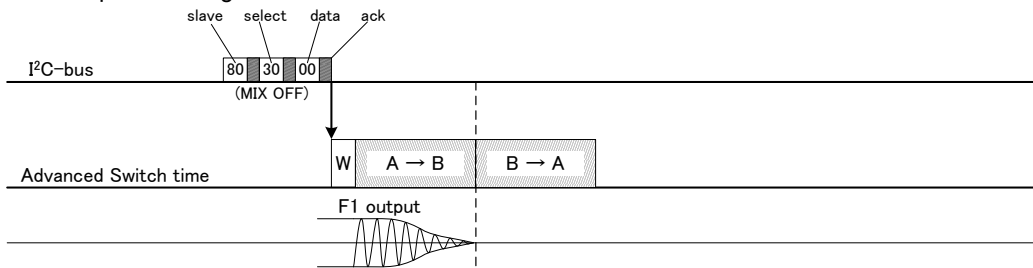
The action of the Mixing switching waveform is different in OFF to ON or ON to OFF.

■ Transmission example 1

This is an example of Mixing OFF to ON state.



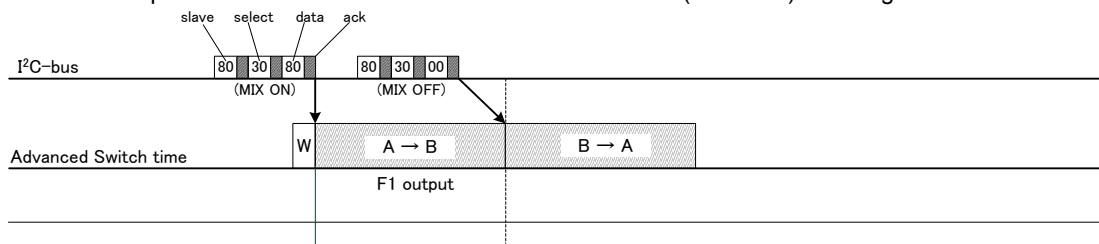
This is an example of Mixing ON to OFF state



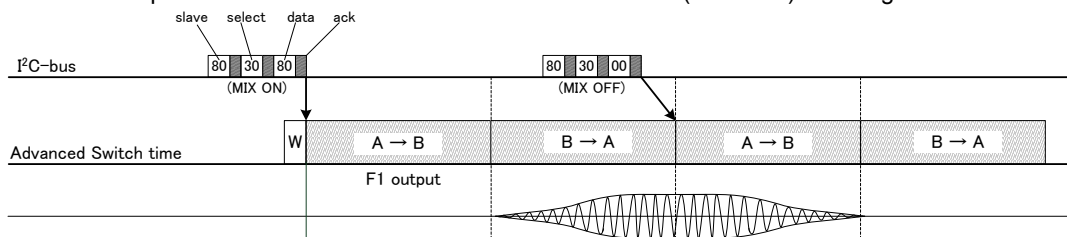
■ Transmission example 2

This is an example when transmission ON to OFF in short interval during to Mixing switching operation.

This is an example of in case of transmitted data of another status(MIX OFF) in during A→B transmission timing.



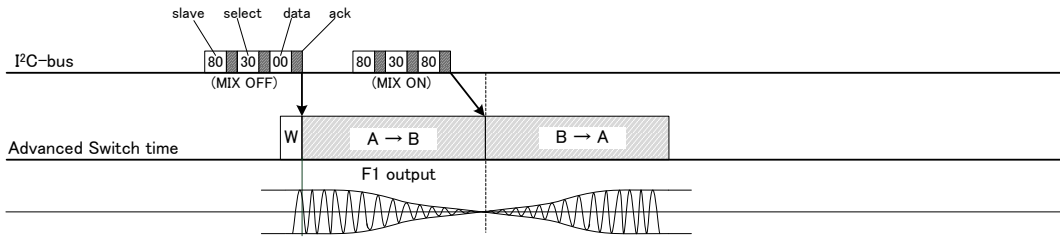
This is an example of in case of transmitted data of another status(MIX OFF) in during B→A transmission timing.



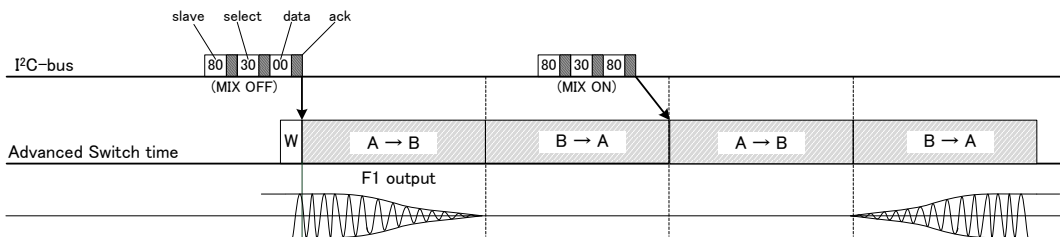
■ Transmission example 3

This is an example when transmission OFF to ON in short interval during to Mixing switching operation.

This is an example of in case of transmitted data of another status(MIX ON) in during A→B transmission timing.

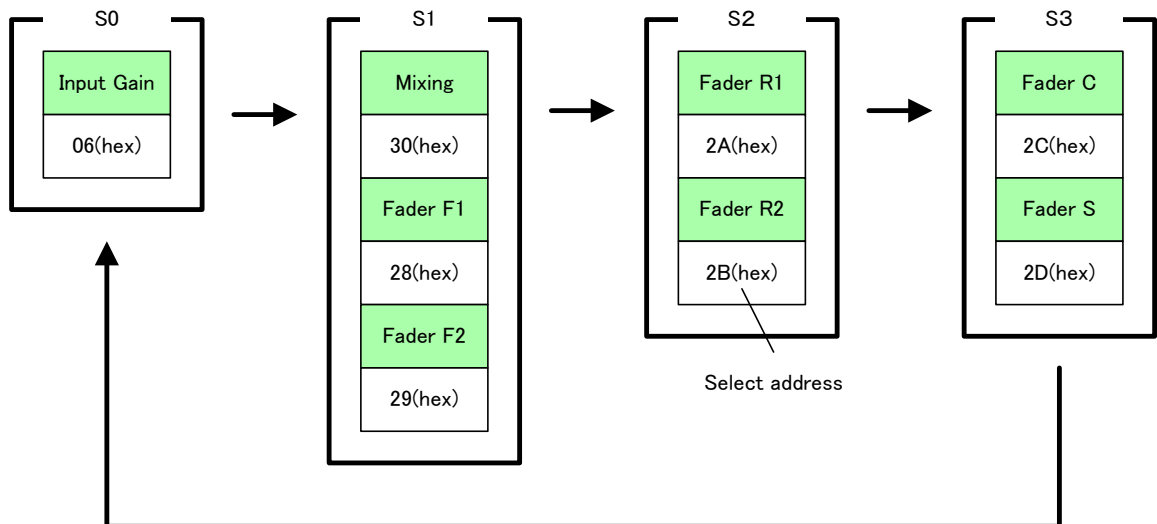


This is an example of in case of transmitted data of another status(MIX ON) in during B→A transmission timing.



2-3. About the data transmitting timing and the switching movement in several block state

When data are transmitted to several blocks, treatment in the BS (block state) unit is carried out inside the IC. The order of advanced switch movement start is decided in advance dependent on BS.



The order of advanced switch start

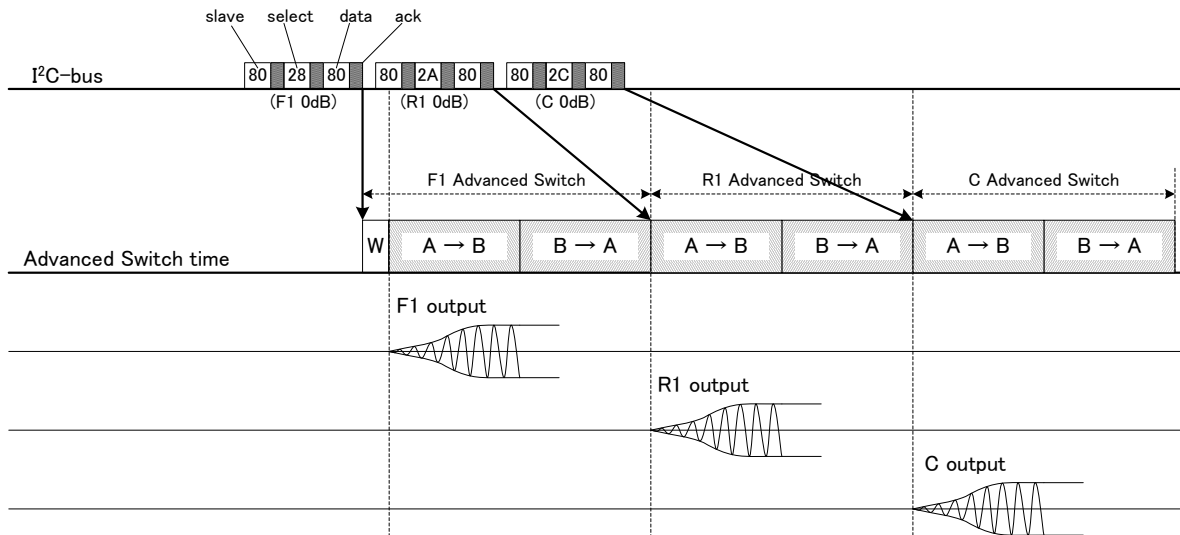
Note) It is possible that blocks in the same BS start switching at the same timing.

■ Transmitting example 1

About the transmission to several blocks also, as explained in the previous section, though there is no restriction of the I²C-bus data transmitting timing, the start timing of switching follows the figure of previous page, the order of advanced switch start.

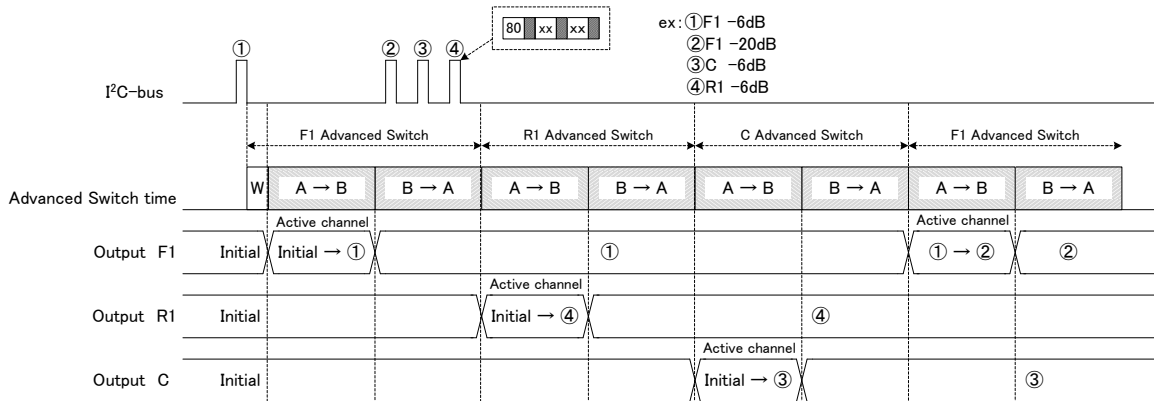
Therefore, it isn't based on the data transmitting order, and an actual switching order becomes as the figure of previous page, "The order of advanced switch start".

Each block data is being transmitted separately in the transmitting example 1, but it becomes the same result even if data are transmitted by automatic increment.



■ Transmitting example 2

In the case that data transmission order and actual switching order is different, or data is transmitted to the block in other BS before the advanced switch operation finished, switching of next BS starts after current switching.



Application Example

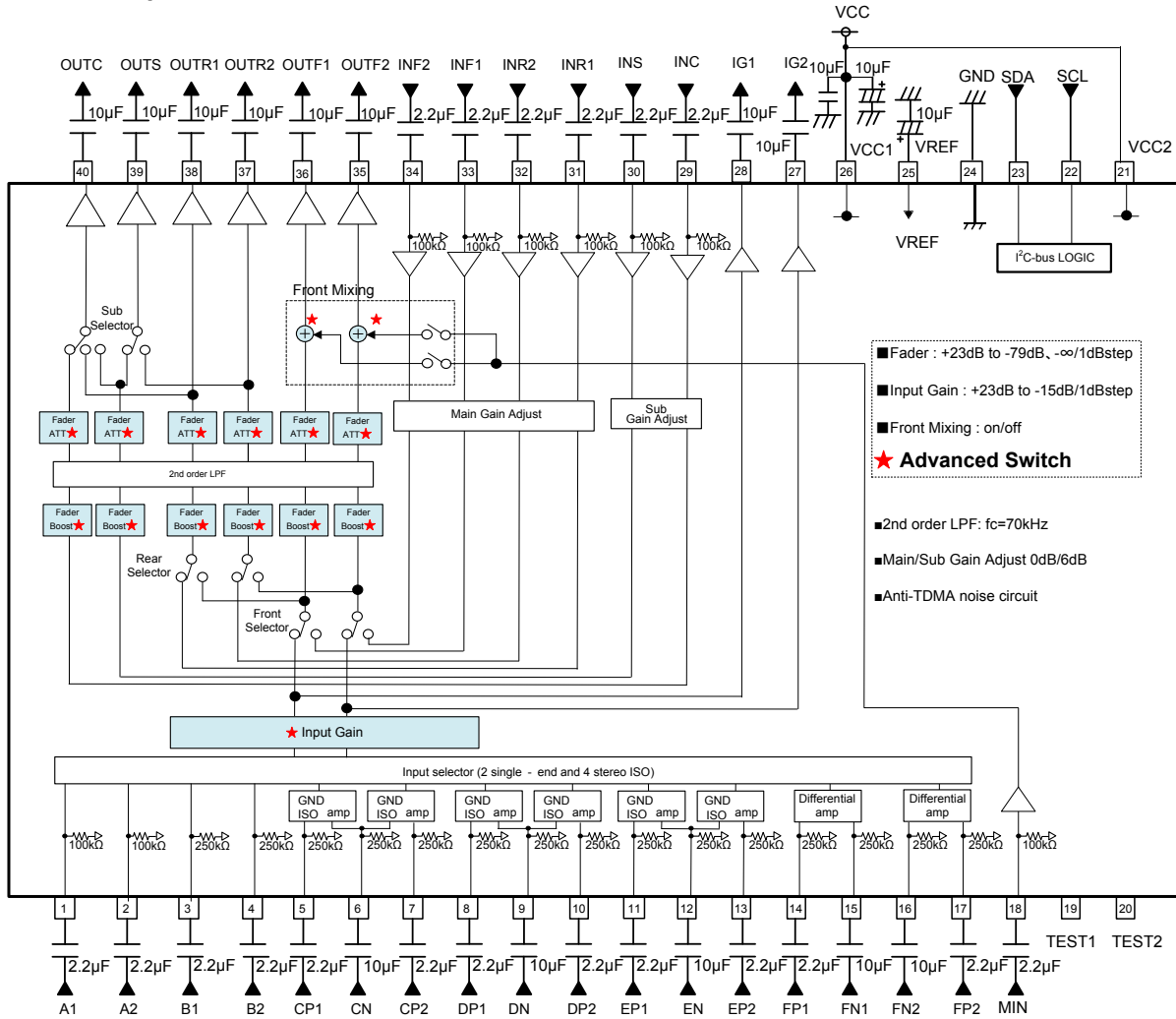


Figure 18. Application Example

- Notes on wiring**
- ① Please connect the decoupling capacitor of a power supply as close as possible to GND.
 - ② Lines of GND shall be one-point connected.
 - ③ Wiring pattern of Digital shall be away from that of analog unit and cross-talk shall not be acceptable.
 - ④ Lines of SCL and SDA of I²C-bus shall not be parallel if possible. The lines shall be shielded, if they are adjacent to each other.
 - ⑤ Lines of analog input shall not be parallel if possible. The lines shall be shielded, if they are adjacent to each other.
 - ⑥ About TEST1,2 terminal(19,20pin), please use with OPEN.

Thermal Derating Curve

About the thermal design by the IC

Characteristics of an IC have a great deal to do with the temperature at which it is used, and exceeding absolute maximum ratings may degrade and destroy elements. Careful consideration must be given to the heat of the IC from the two standpoints of immediate damage and long-term reliability of operation.

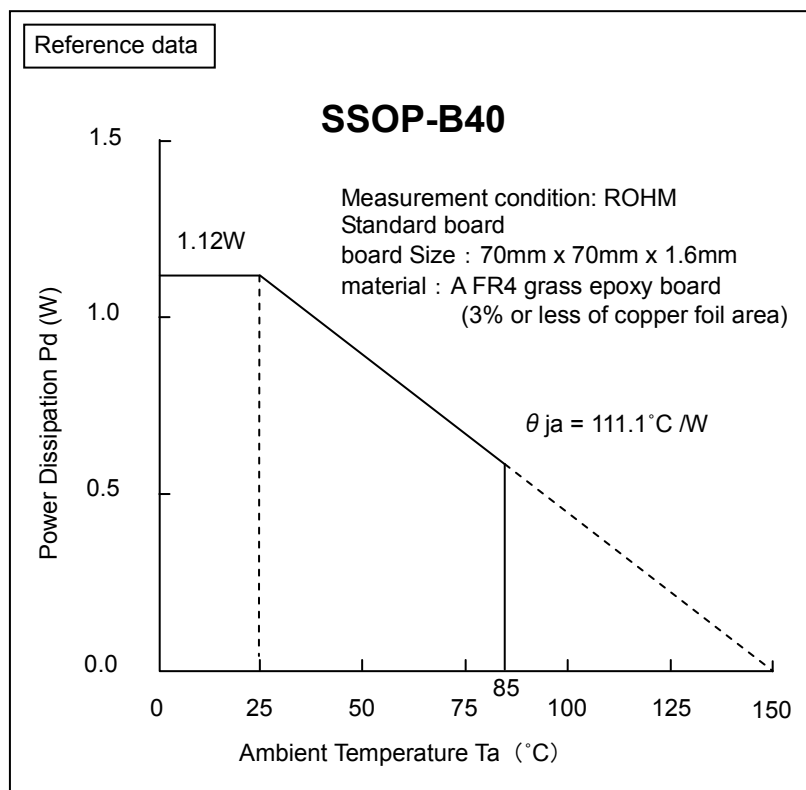


Figure 19. Temperature Derating Curve

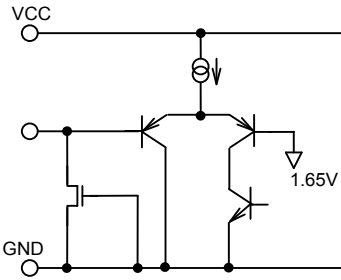
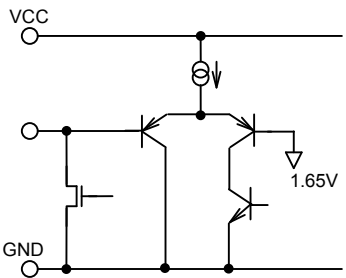
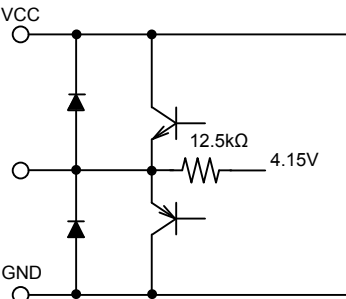
Note) Values are actual measurements and are not guaranteed.

Note) Power dissipation values vary according to the board on which the IC is mounted.

I/O Equivalence Circuit

| Terminal No | Terminal Name | Terminal Voltage | Equivalent Circuit | Terminal Description |
|---|--|------------------|--------------------|---|
| 1 2 29 30 31 32 33 34 18 | A1 A2 INC INS INR1 INR2 INF1 INF2 MIN | 4.15V | | Terminal for signal input The input impedance is 100kΩ(Typ). |
| 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 | B1 B2 CP1 CN CP2 DP1 DN DP2 EP1 EN EP2 FP1 FN1 FN2 FP2 | 4.15V | | Input terminal Single/Differential mode is selectable. The input impedance is 250kΩ(Typ). |
| 27 28 | IG2 IG1 | 4.15V | | Input Gain output terminal |
| 35 36 37 38 39 40 | OUTF2 OUTF1 OUTR2 OUTR1 OUTS OUTC | 4.15V | | Fader output terminal |

The figures in the pin explanation and input/output equivalent circuit is designed value, it doesn't guarantee the value.

| Terminal No | Terminal Name | Terminal Voltage | Equivalent Circuit | Terminal Description |
|-------------|-----------------|------------------|---|--|
| 21,26 | VCC (VCC1,2) | 8.5V | | Power supply terminal |
| 22 | SCL | — |  | Terminal for clock input of I ² C-bus communication (Note) When this pin is shorted to next pin(VCC), it may result in property degradation and destruction of the device. |
| 23 | SDA | — |  | Terminal for data input of I ² C-bus communication |
| 24 | GND | 0V | | Ground terminal |
| 25 | VREF | 4.15V |  | BIAS terminal Voltage for reference bias of analog signal system. The simple precharge circuit and simple discharge circuit for an external capacitor are built in. |

The figures in the pin explanation and input/output equivalent circuit is designed value, it doesn't guarantee the value.

Application Information

1. Absolute maximum rating voltage

When voltage is impressed to VCC exceeding absolute maximum rating voltage, circuit current increases rapidly and it may result in property degradation and destruction of a device.

When impressed by a VCC terminal (21,26pin) especially by surge examination etc., even if it includes an of operation voltage +surge pulse component, be careful not to impress voltage (about 14V VCC terminal) much higher than absolute maximum rating voltage.

2. About a signal input part

In the signal input terminal, the value of the input coupling capacitor C(F) should be sufficient to match the value of input impedance $R_{IN}(\Omega)$ inside the IC. The first HPF characteristic of CR is as shown below.

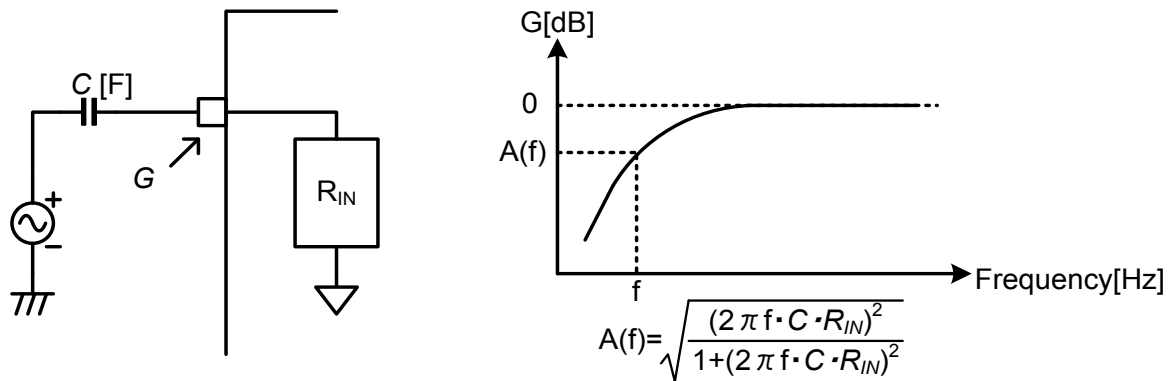


Figure 20. Input Equivalent Circuit

3. About output load characteristics

The usages of load for output are below (reference). Please use the load more than 10 k Ω (Typ).

Output terminal

| Terminal No. | Terminal Name | Terminal No. | Terminal Name | Terminal No. | Terminal Name | Terminal No. | Terminal Name |
|--------------|---------------|--------------|---------------|--------------|---------------|--------------|---------------|
| 28 | IG1 | 36 | OUTF1 | 38 | OUTR1 | 40 | OUTC |
| 27 | IG2 | 35 | OUTF2 | 37 | OUTR2 | 39 | OUTS |

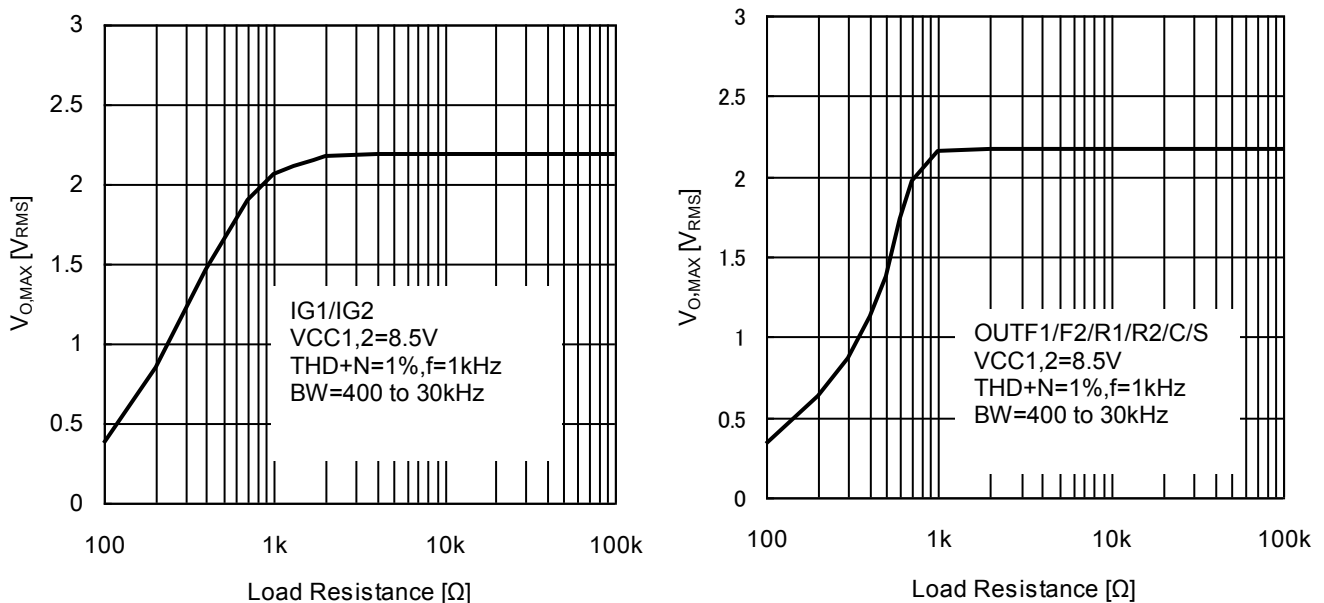


Figure 21. Output load characteristic at VCC1,2=8.5V (Reference)

Application Information – continued

4. About TEST1,2 terminal(19,20pin)
About TEST1,2 terminal(19,20pin), please use with OPEN.
5. About signal input terminals
Because the inner impedance of the terminal becomes 100 k Ω or 250 k Ω when the signal input terminal makes a terminal open, the plunge noise from outside sometimes becomes a problem. When there is an unused signal input terminal, design so it is shorted to ground.
6. About changing gain of Input Gain and Fader Volume
In case of the boost of the input gain and fader volume when changing to the high gain which exceeds 20 dB especially, the switching pop noise sometimes becomes big.
In this case, we recommend changing every 1 dB step without changing a gain at once.
Also, the pop noise sometimes can reduce by making advanced switch time long, too.

Operational Notes

- 1. Reverse Connection of Power Supply**
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.
- 2. Power Supply Lines**
Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.
- 3. Ground Voltage**
Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.
- 4. Ground Wiring Pattern**
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.
- 5. Thermal Consideration**
Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, increase the board size and copper area to prevent exceeding the maximum junction temperature rating.
- 6. Recommended Operating Conditions**
These conditions represent a range within which the expected characteristics of the IC can be approximately obtained. The electrical characteristics are guaranteed under the conditions of each parameter.
- 7. Inrush Current**
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.
- 8. Operation Under Strong Electromagnetic Field**
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.
- 9. Testing on Application Boards**
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

Operational Notes – continued

10. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

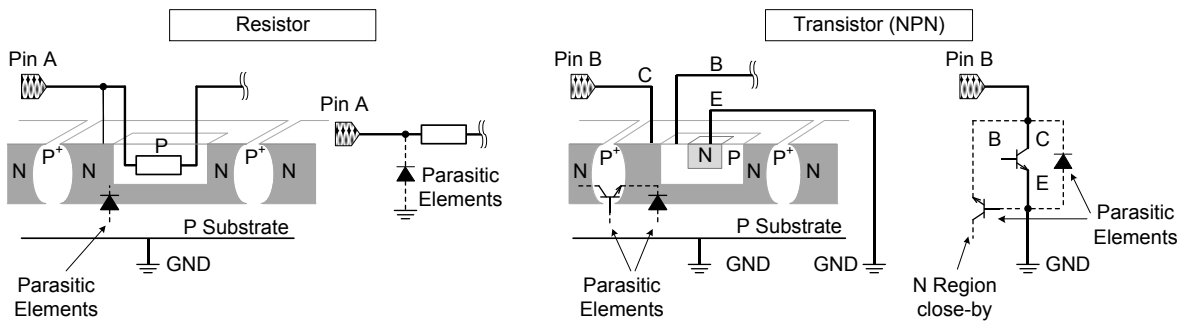
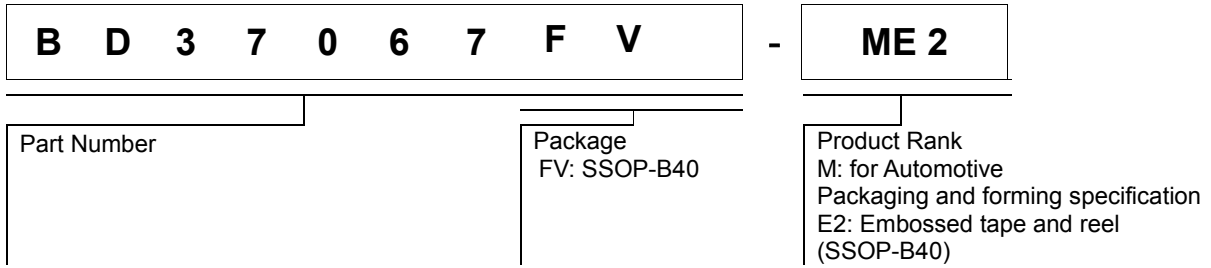


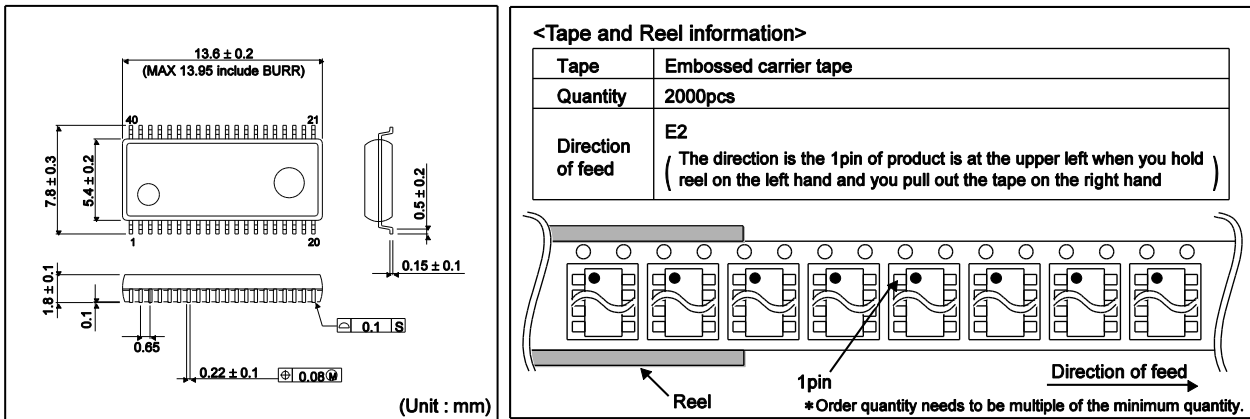
Figure 22. Example of monolithic IC structure

Ordering Name Selection

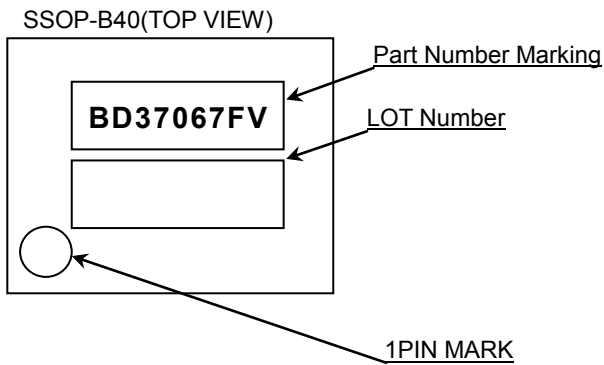


Physical Dimension Tape and Reel Information

SSOP-B40



Marking Diagram



Revision History

| Date | Revision | Changes |
|-------------|----------|---|
| 13.MAR.2014 | 001 | New Release |
| 14.NOV.2016 | 002 | <ul style="list-style-type: none">• Additional specification about advanced switch operation• Additional specification of power supply sequence• Change document style of specification |

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| CLASS IV | | CLASS III | |

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