

Power Supply IC for High Fidelity Audio

Linear Regulator for High Fidelity Audio

BD37201NUX

General Description

BD37201NUX is a linear regulator of low noise (3.3 μ Vrms) which is most suitable to high quality audio system. It operates at 2.7 V to 5.5 V and capable of supplying a maximum load of 500 mA.

In addition to the low noise, BD37201NUX has a high PSRR and good input transient fluctuation characteristic which makes it suitable for the stabilization of DC/DC converter output, and an ideal power supply to high precision analog circuits such as D/A converter (DAC) and Clock generator.

Furthermore, when BD37201NUX is placed in standby mode, the supply current can be as small as 0.02 μ A (Typ) which can greatly reduce power consumption.

Features

- Ultra Low Noise, High PSRR
- Standby Mode that is controlled by Enable pin
- Soft Start Function controlled by External Capacitor
- Under Voltage Lockout Protection, Over Current Protection, Thermal Shutdown Protection

Applications

- High Quality Audio Equipment
- Power Supply for D/A Converter and Clock Generator

Key Specifications

- Input Voltage Range: 2.7 V to 5.5 V
- Output Voltage Range: 1.0 V to 4.5 V
- Output Current: 500 mA(Max)
- Output Voltage Noise^(Note 1): 3.3 μ Vrms(10 Hz to 100 kHz, Typ)
- PSRR^(Note 2): 90 dB(1 kHz, Typ), 55 dB(1 MHz, Typ)
- Input Transient Response: 3 mV(1.0 V/ μ s, Typ)
- Standby Current: 0.02 μ A(Typ)
- Operating Temperature Range: -10 °C to +85 °C

(Note 1) C_{BC} =10 μ F, V_{OUT} =1 V, I_{OUT} =500 mA setting

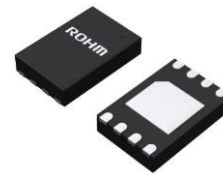
(Note 2) C_{OUT1} =47 μ F, C_{OUT2} =100 μ F, V_{OUT} =1 V, I_{OUT} =500 mA setting

Package

VSON008X2030

W(Typ) x D(Typ) x H(Max)

2.00 mm x 3.00 mm x 0.60 mm



VSON008X2030

Typical Application Circuit

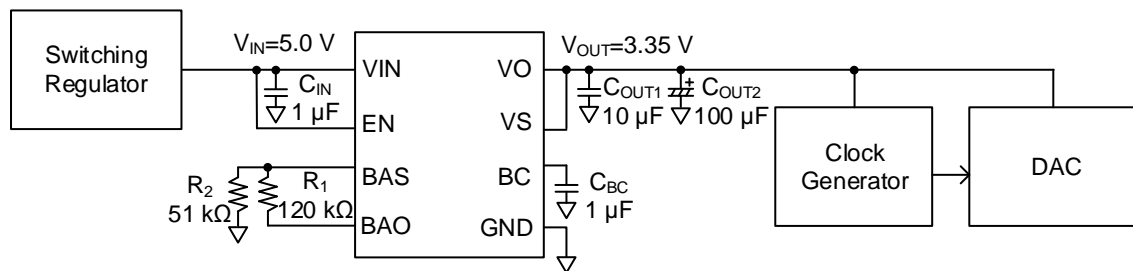


Figure 1. Basic Application Circuit Diagram (V_{OUT} =3.35 V)

Pin Configuration

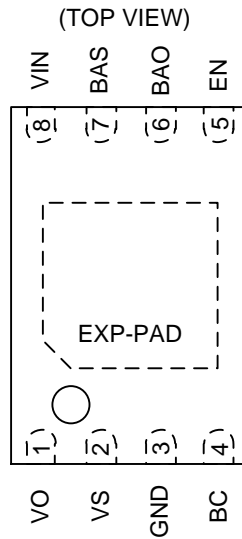


Figure 2. Pin Configuration

Pin Description

| Pin No. | Pin Name | Function |
|---------|----------|--|
| 1 | VO | Output voltage |
| 2 | VS | Output voltage feedback |
| 3 | GND | Ground |
| 4 | BC | Bypass capacitor pin connected to ground |
| 5 | EN | Enable |
| 6 | BAO | Programmed voltage output |
| 7 | BAS | Programmed voltage feedback |
| 8 | VIN | Input voltage |
| - | EXP-PAD | The exposed pad should be connected to GND pattern |

Block Diagram

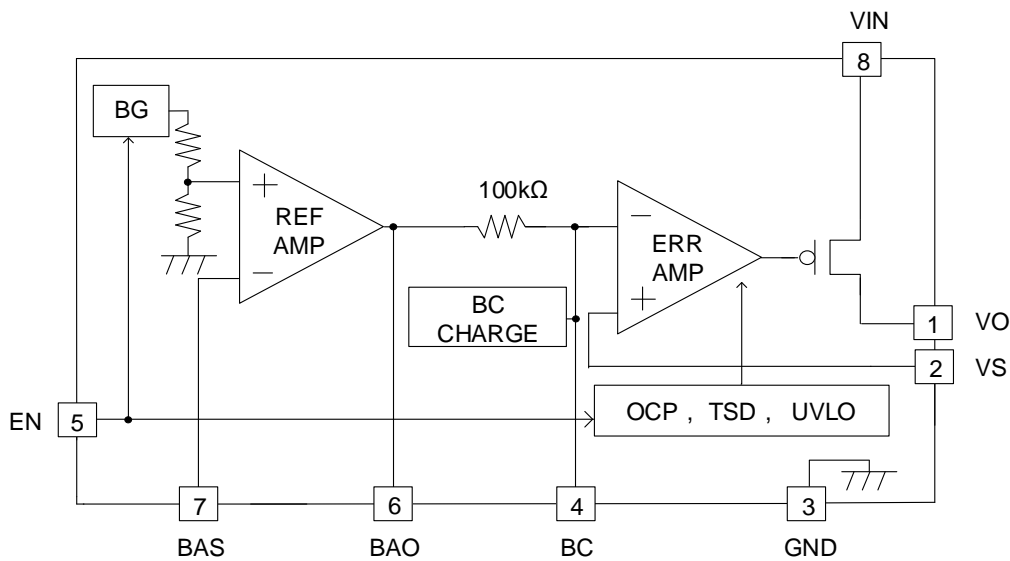


Figure 3. Block Diagram

Description of Block

1. Enable
Assuming EN is set to L, the IC can be set to standby state. In standby state, the output is OFF and since it will be in static state, the power consumption can be reduced.
2. Rising, Falling, and EN Controlled Timing

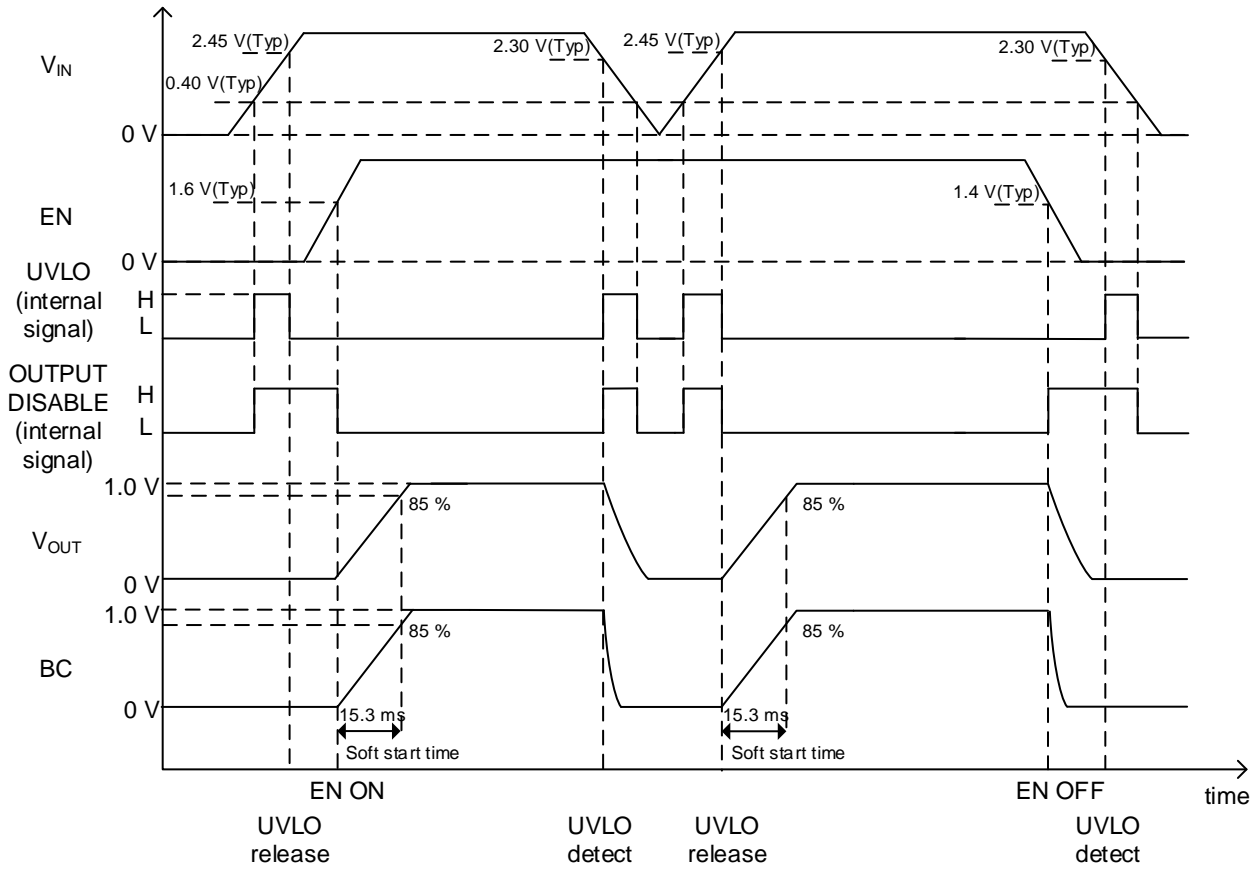


Figure 4. The Sequence Waveform During V_{IN}/EN Rising and Falling (When at BC Capacitor 1 μF and V_{OUT} 1.0 V Settings)

It will operate if EN is H and UVLO (Under Voltage Lockout) is released. In addition, when EN is L or UVLO is detected, the regulator operation stops. V_{IN} does not have the necessity to supply earlier than EN. The maximum slew rate of input voltage has to be set 1 V/μs or below.

3. Soft Start Function
In BD37201NUX, there exists a function that limits the rising speed of output when EN rises by the capacitor connected to the BC pin due to decrease of inrush current of output. The rising speed depends on the internal charging current 100 μA (Typ), the capacitance value connected to the BC pin and on the output programmed voltage. It is about 15.3 ms (Max) if capacitance of C_{BC} is 1 μF and output programmed voltage is 1.0 V, and almost 45.4 ms (Max) if output programmed voltage is set to 3.35 V. The above is an aim level, and soft start time may change depending on the case that the input voltage is less than the output voltage or the input and output voltage condition.

When EN ON / OFF repeating signal input during soft start time, soft start function doesn't work. After the EN ON operation, during the soft start time, EN ON / OFF operation that necessary to control not to perform.

4. REFAMP
REFAMP sets its output voltage. Refer [Selection of Components Externally Connected](#) about setting of output voltage.

Description of Block – continued

5. BC
Noise at the output voltage of REFAMP is reduced because of the internal resistor 100 k Ω and the external capacitor of the BC pin. In addition to it, the external capacitor of the BC pin also has a soft start function so the rising speed can be adjusted by this value.
The higher value of capacitor will decrease the noise but the soft start time will be longer.
6. ERRAMP
The ERRAMP outputs the voltage set in REFAMP at voltage follower. The VS pin must be connected to the VO pin by all means. In addition, the VS pin can decrease a voltage drop by the pattern resistance on the VO pin course by returning the voltage from the supply point.

Absolute Maximum Rating (Ta=25 °C)

| Parameter | Symbol | Rating | Unit |
|------------------------------------|-------------------|--------------|------|
| Power Supply Voltage (PIN 8) | V _{IN} | -0.3 to +7.0 | V |
| Pin Voltage (PIN 1, 2, 4, 5, 6, 7) | V _{PIN} | -0.3 to +7.0 | V |
| Storage Temperature Range | T _{stg} | -55 to +150 | °C |
| Junction Temperature | T _{jmax} | 150 | °C |

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance^(Note 3)

| Parameter | Symbol | Thermal Resistance (Typ) | | Unit |
|--|-----------------|--------------------------|--------------------------|------|
| | | 1s ^(Note 5) | 2s2p ^(Note 6) | |
| VSON008X2030 | | | | |
| Junction to Ambient | θ _{JA} | 308.3 | 69.6 | °C/W |
| Junction to Top Characterization Parameter ^(Note 4) | Ψ _{JT} | 43 | 10 | °C/W |

^(Note 3) Based on JEDEC51-2A(Still-Air).

^(Note 4) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

^(Note 5) Using a PCB board based on JEDEC51-3.

^(Note 6) Using a PCB board based on JEDEC51-5, 7.

| Layer Number of Measurement Board | Material | Board Size |
|-----------------------------------|----------|-------------------------------|
| Single | FR-4 | 114.3 mm x 76.2 mm x 1.57 mmt |

| Top | |
|-----------------------|-----------|
| Copper Pattern | Thickness |
| Footprints and Traces | 70 μm |

| Layer Number of Measurement Board | Material | Board Size | Thermal Via ^(Note 7) | |
|-----------------------------------|----------|------------------------------|---------------------------------|----------|
| | | | Pitch | Diameter |
| 4 Layers | FR-4 | 114.3 mm x 76.2 mm x 1.6 mmt | 1.20 mm | Φ0.30 mm |

| Top | | 2 Internal Layers | | Bottom | |
|-----------------------|-----------|-------------------|-----------|-------------------|-----------|
| Copper Pattern | Thickness | Copper Pattern | Thickness | Copper Pattern | Thickness |
| Footprints and Traces | 70 μm | 74.2 mm x 74.2 mm | 35 μm | 74.2 mm x 74.2 mm | 70 μm |

^(Note 7) This thermal via connects with the copper pattern of all layers.

Recommended Operating Conditions

| Parameter | Symbol | Min | Typ | Max | Unit |
|---|------------------|-----|-----|-----|------|
| Power Supply Voltage | V _{IN} | 2.7 | - | 5.5 | V |
| Output Voltage Setting is within a Possible Range | V _{OUT} | 1.0 | - | 4.5 | V |
| Output Current ^(Note 8) | I _{OUT} | - | - | 500 | mA |
| Operating Temperature | T _{opr} | -10 | +25 | +85 | °C |

^(Note 8) T_{jmax} should not be exceeded.

Operating Condition

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|---|-------------------|------|-----|-----|------|---|
| Input Capacitor ^(Note 9) | C _{IN} | 0.47 | 1 | - | μF | Film capacitors are recommended |
| Output Capacitor 1 ^{(Note 9)(Note 10)} | C _{OUT1} | 1 | 10 | - | μF | Film capacitors are recommended |
| Output Capacitor 2 ^{(Note 9)(Note 10)} | C _{OUT2} | 4.7 | 100 | - | μF | Electrolytic capacitors are recommended |
| BC Capacitor ^{(Note 9)(Note 10)} | C _{BC} | 0.01 | 1 | - | μF | Film capacitors are recommended |

^(Note 9) Set the capacity of the capacitor not to be less than the minimum in consideration of temperature or DC bias properties.

^(Note 10) Refer the Selection of Components Externally Connected written in [Page 16](#) and [Page 17](#), and decide the value of each capacitor.

Electrical Characteristics

(Unless otherwise specified, $V_{IN}=V_{OUT}+1.0$ V or 2.7 V whichever is greater $V_{OUT}=1.0$ V $T_a=25$ °C $C_{OUT1}=10$ μ F $C_{OUT2}=100$ μ F $C_{BC}=1$ μ F $I_{OUT}=5$ mA $V_{EN}=V_{IN}$)

| Parameter | Symbol | Min | Typ | Max | Unit | Conditions |
|--|---------------|------|------|----------|------------|--|
| Circuit Current | I_{CC} | - | 1.33 | 2.3 | mA | - |
| Standby Current | I_{STB} | - | 0.02 | 1.0 | μ A | $V_{IN}=5.5$ V, $V_{EN}=0$ V |
| Reference Voltage | V_{REF} | 0.99 | 1.00 | 1.01 | V | BAO Voltage |
| Line Regulation | D_{VI} | - | 1 | 20 | mV | $V_{IN}=2.7$ V to 5.5 V |
| Load Regulation | D_{VL} | - | 3 | 20 | mV | $I_{OUT}=0$ A to 500 mA |
| Dropout Voltage | V_{SAT} | - | 0.2 | 0.5 | V | $I_{OUT}=500$ mA, $V_{OUT}=3.35$ V |
| PSRR 1 kHz | $PSRR_{1kHz}$ | - | 90 | - | dB | $f=1$ kHz |
| PSRR 1 MHz | $PSRR_{1MHz}$ | - | 55 | - | dB | $f=1$ MHz, $C_{OUT1}=47$ μ F |
| Output Noise Voltage | V_{NOISE} | - | 3.3 | - | μ Vrms | BW=10 Hz to 100 kHz, $C_{BC}=10$ μ F, $I_{OUT}=500$ mA |
| Over Current Protection Detect Current | I_{OCP} | 500 | - | - | mA | - |
| UVLO Detect Voltage | V_{UVLOH} | 2.10 | 2.30 | 2.50 | V | - |
| UVLO Release Voltage | V_{UVLOL} | 2.25 | 2.45 | 2.65 | V | - |
| EN Input H Level | V_{THENH} | 2.20 | - | V_{IN} | V | - |
| EN Input L Level | V_{THENL} | 0.00 | - | 0.60 | V | - |
| EN Input Current | I_{EN} | - | 1.23 | 2.10 | μ A | $V_{EN}=3$ V |

Typical Performance Curves

(Unless otherwise specified, $V_{IN}=V_{OUT}+1.0$ V or 2.7 V whichever is greater $V_{OUT}=1.0$ V $T_a=25$ °C $C_{OUT1}=10$ μ F $C_{OUT2}=100$ μ F $C_{BC}=1$ μ F $I_{OUT}=5$ mA $V_{EN}=V_{IN}$)

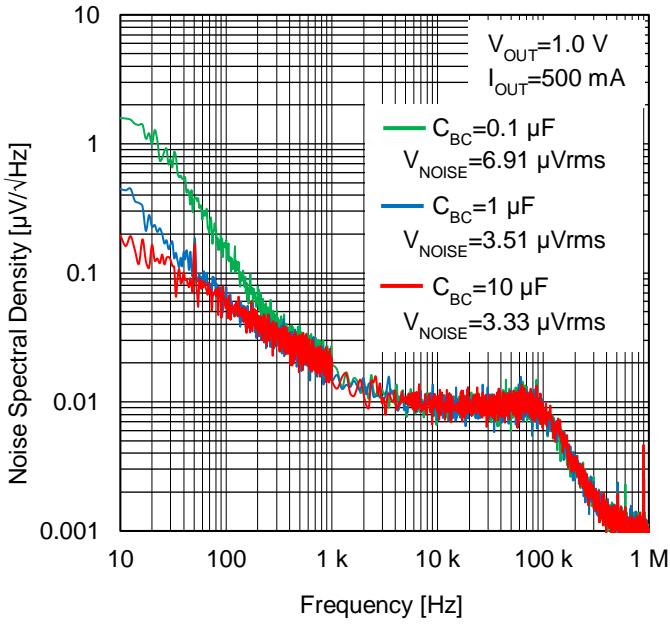


Figure 5. Noise Spectral Density vs Frequency ($V_{OUT}=1.0$ V)

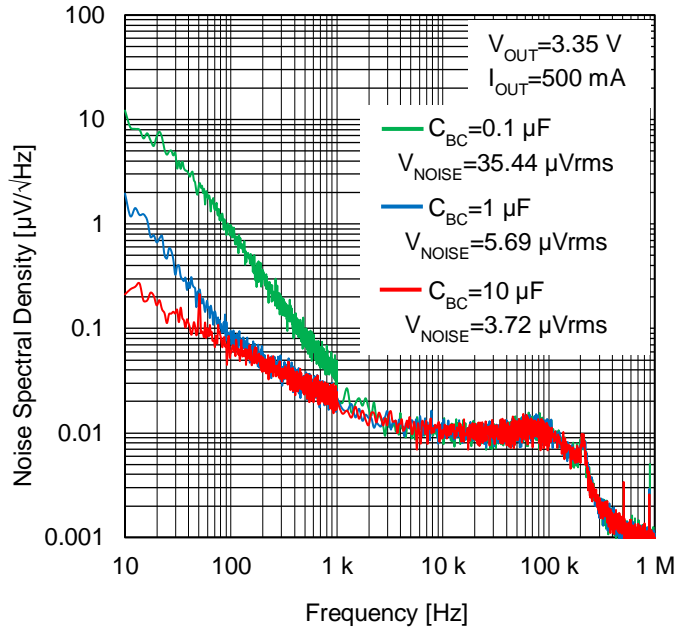


Figure 6. Noise Spectral Density vs Frequency ($V_{OUT}=3.35$ V)

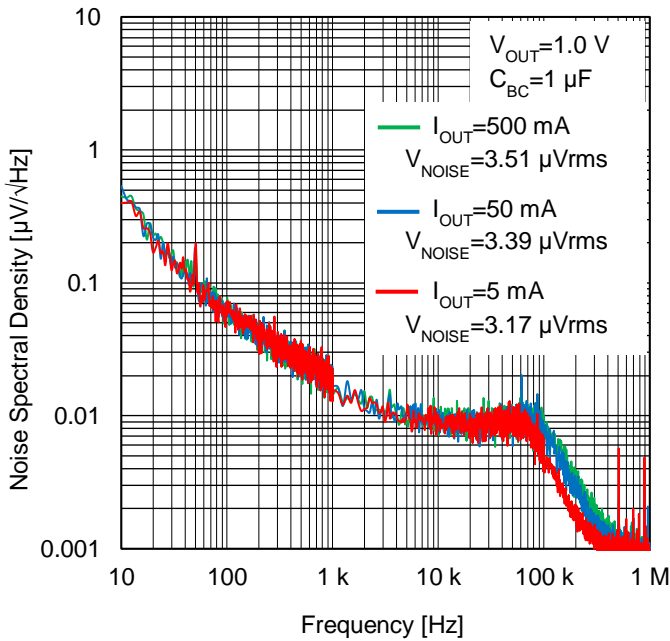


Figure 7. Noise Spectral Density vs Frequency ($V_{OUT}=1.0$ V)

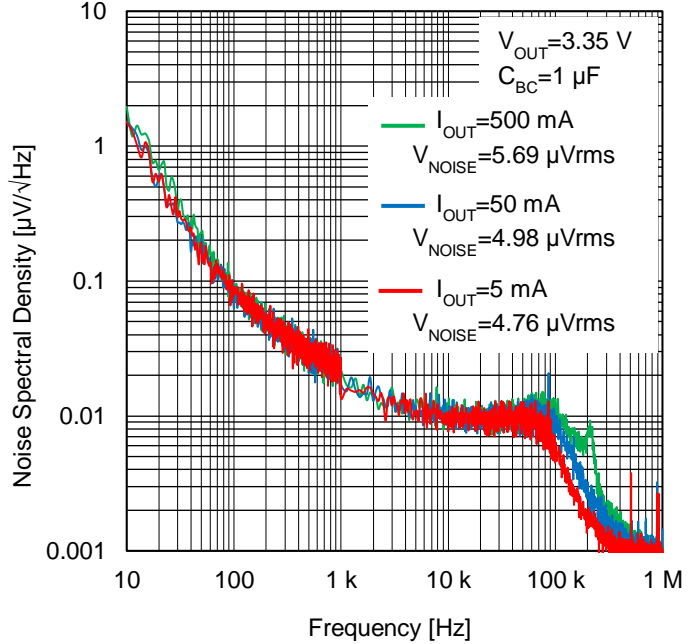


Figure 8. Noise Spectral Density vs Frequency ($V_{OUT}=3.35$ V)

Typical Performance Curves – continued

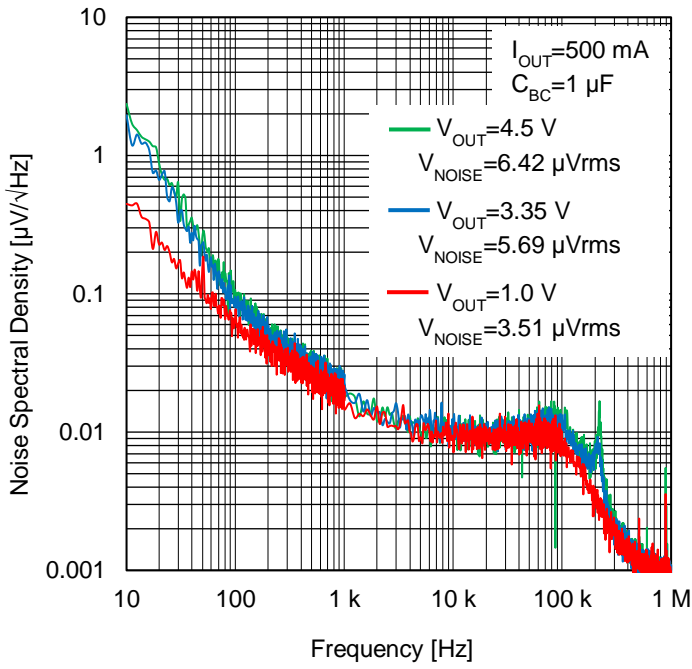


Figure 9. Noise Spectral Density vs Frequency

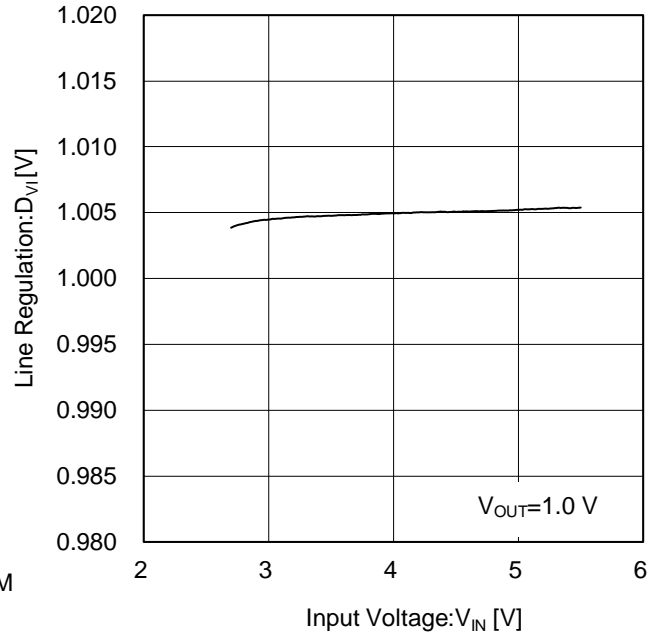


Figure 10. Line Regulation (D_{VI}) ($V_{OUT}=1.0\text{ V}$)

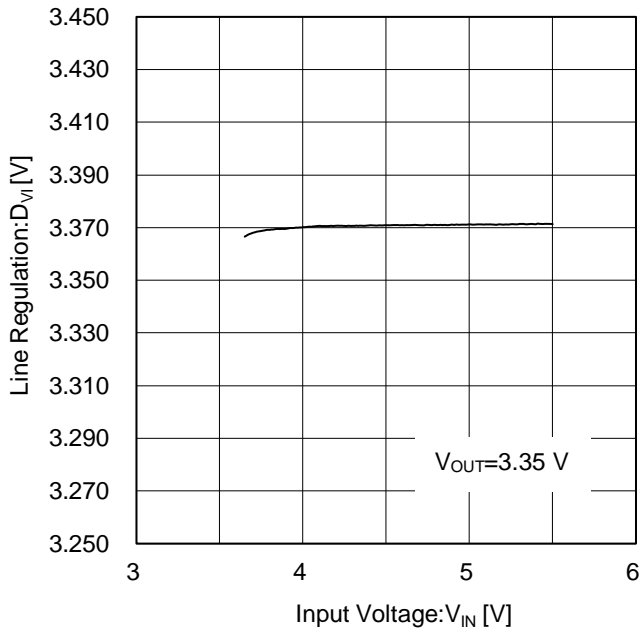


Figure 11. Line Regulation (D_{VI}) ($V_{OUT}=3.35\text{ V}$)

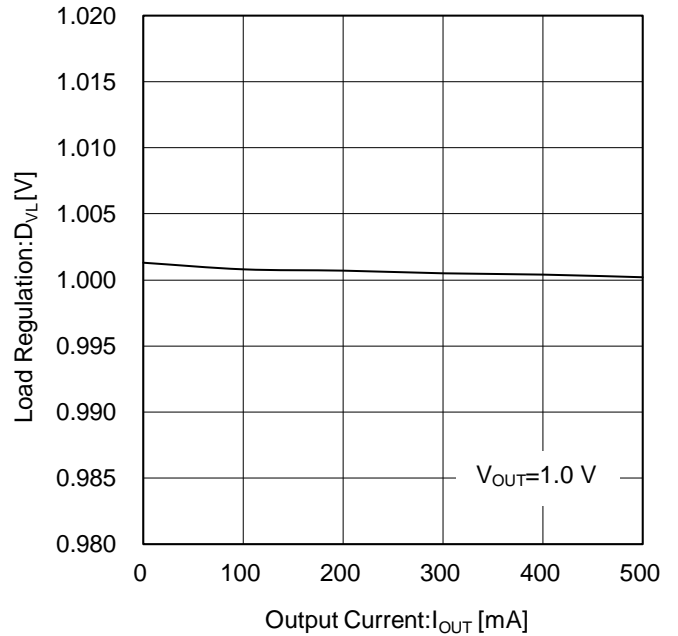


Figure 12. Load Regulation (D_{VL}) ($V_{OUT}=1.0\text{ V}$)

Typical Performance Curves – continued

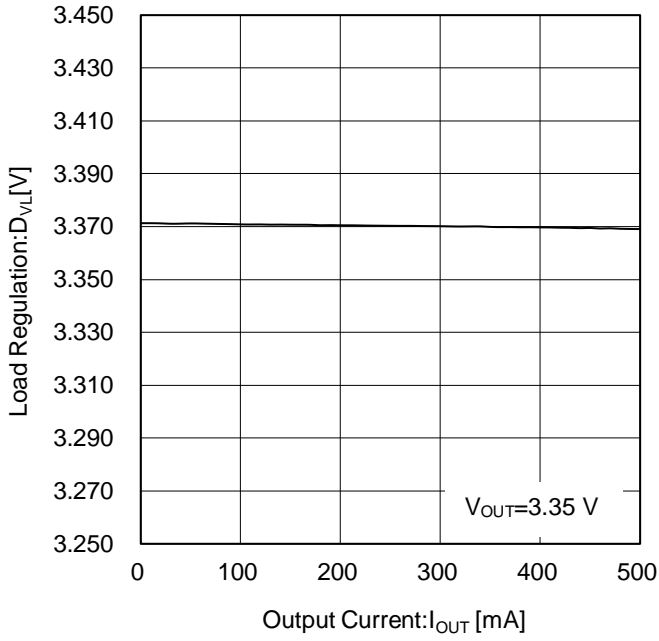


Figure 13. Load Regulation (D_{VL}) ($V_{OUT}=3.35$ V)

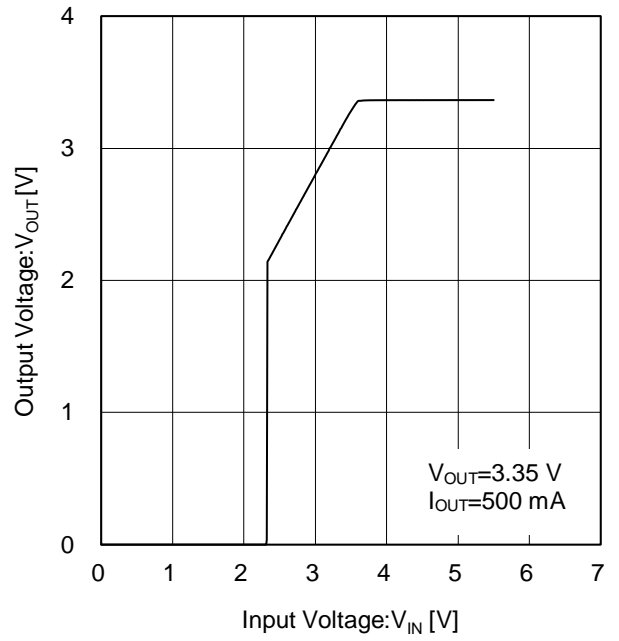


Figure 14. Output Voltage vs Input Voltage ($V_{OUT}=3.35$ V)

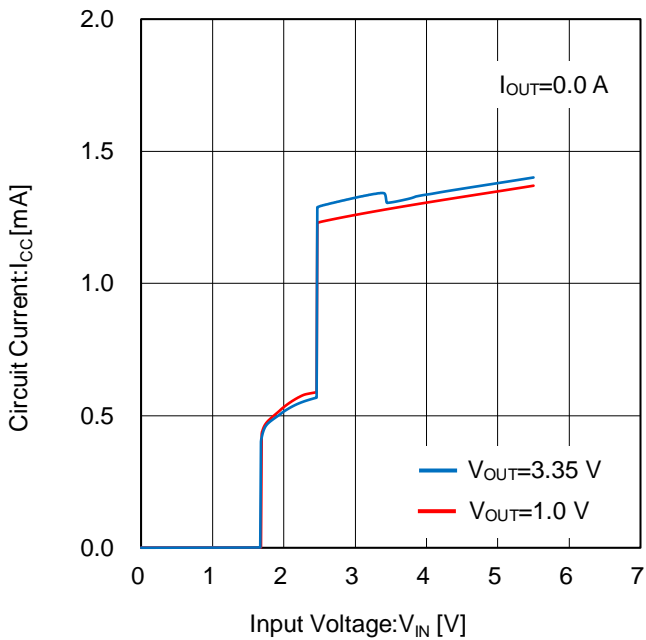


Figure 15. Circuit Current vs Input Voltage

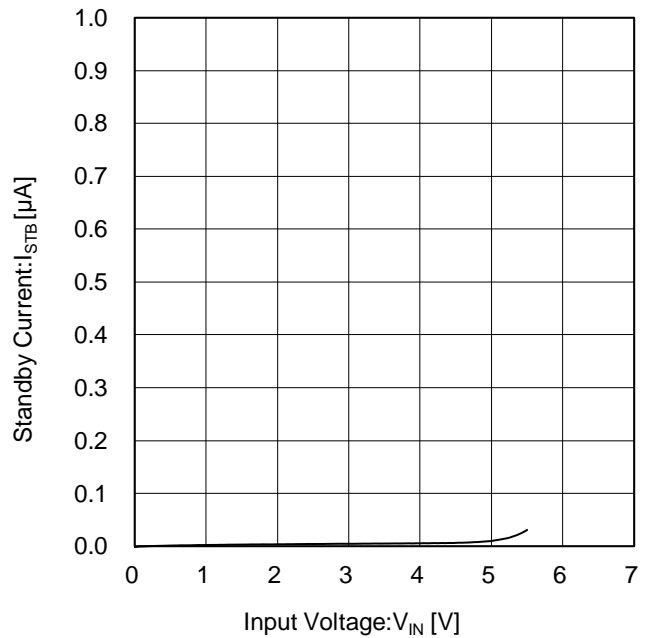


Figure 16. Standby Current vs Input Voltage

Typical Performance Curves – continued

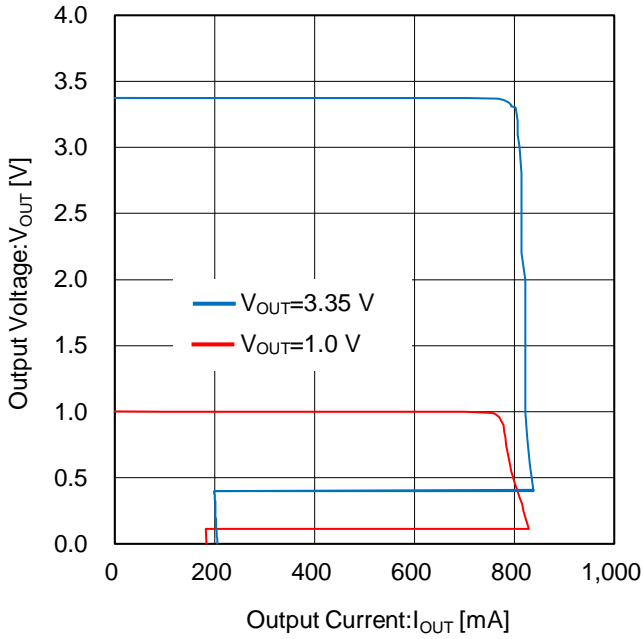


Figure 17. Output Voltage vs Output Current

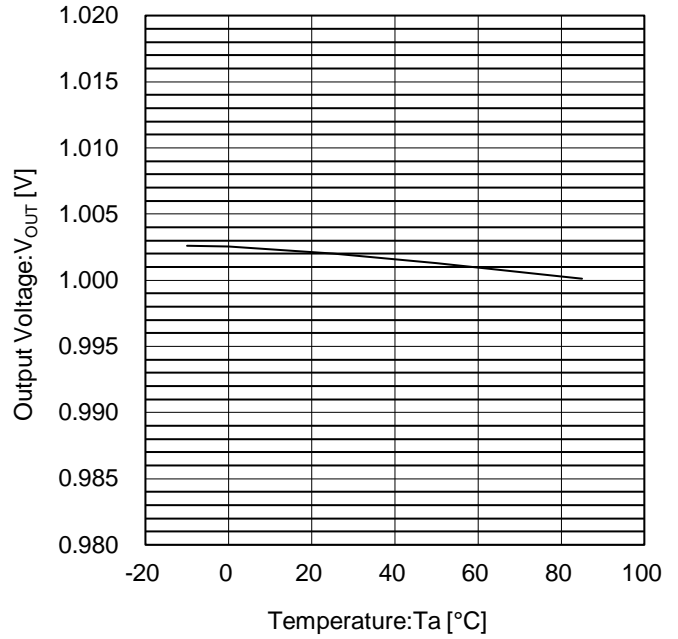


Figure 18. Output Voltage vs Temperature (V_{OUT}=1.0 V)

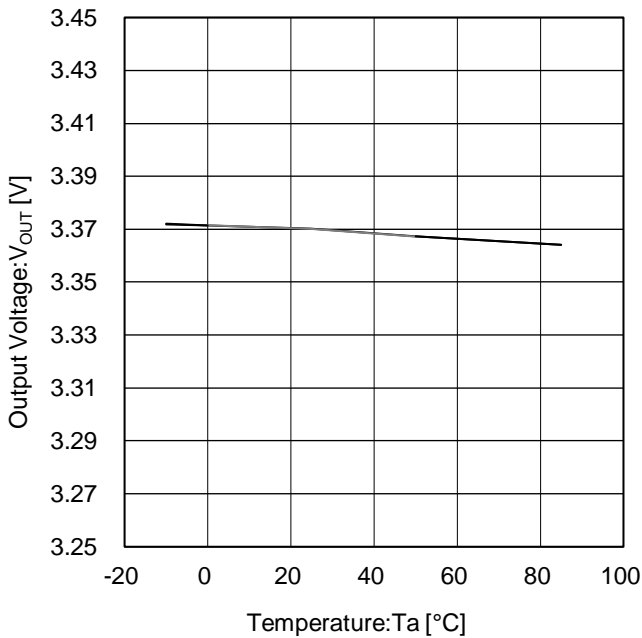


Figure 19. Output Voltage vs Temperature (V_{OUT}=3.35 V)

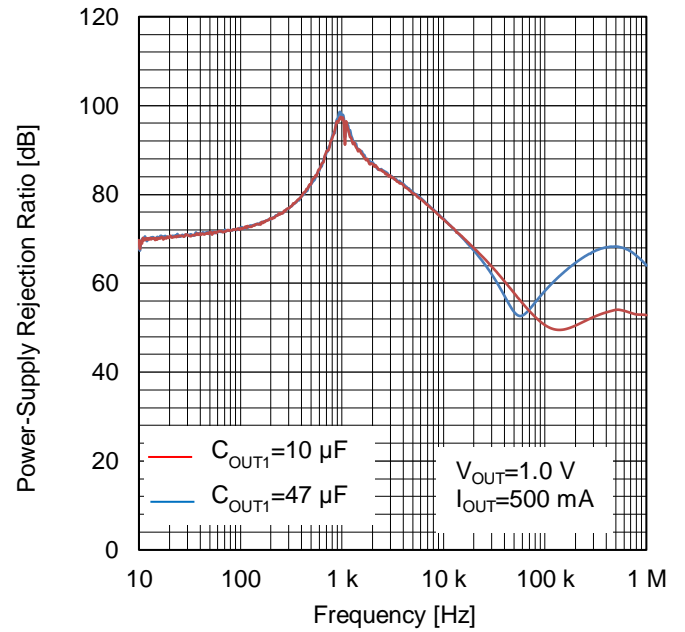


Figure 20. Power-Supply Rejection Ratio (V_{OUT}=1.0 V)

Typical Performance Curves – continued

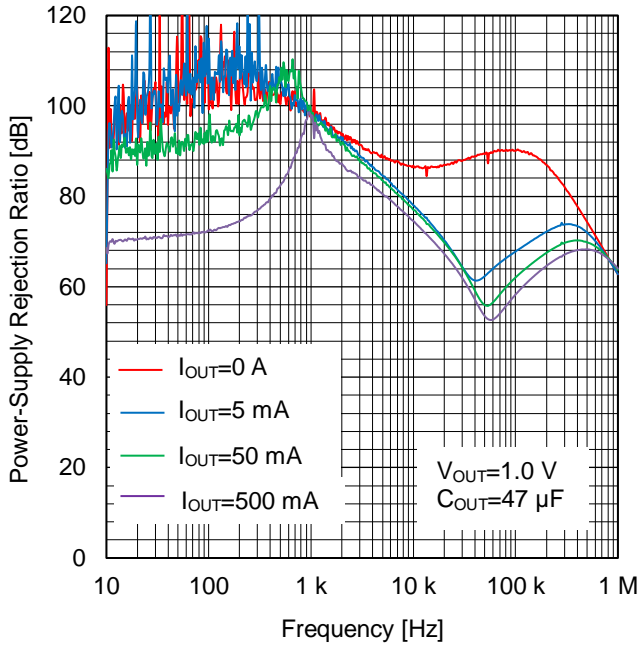


Figure 21. Power-Supply Rejection Ratio ($V_{OUT}=1.0\text{ V}$)

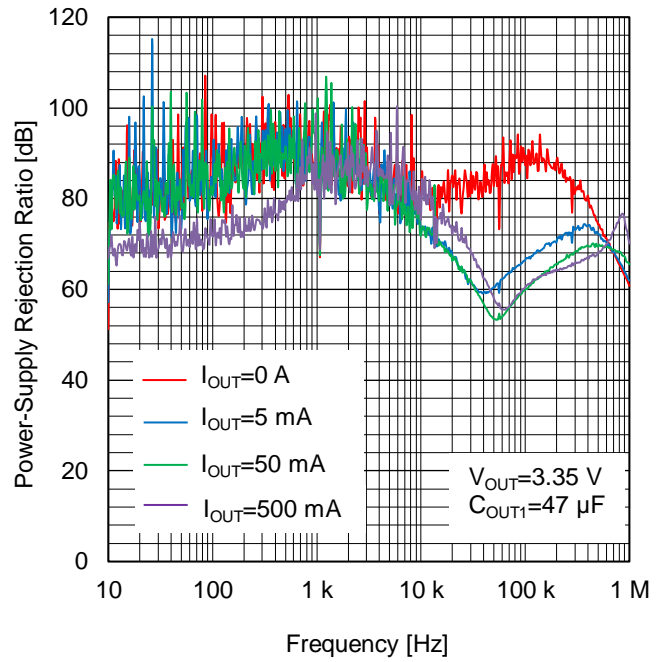


Figure 22. Power-Supply Rejection Ratio ($V_{OUT}=3.35\text{ V}$)

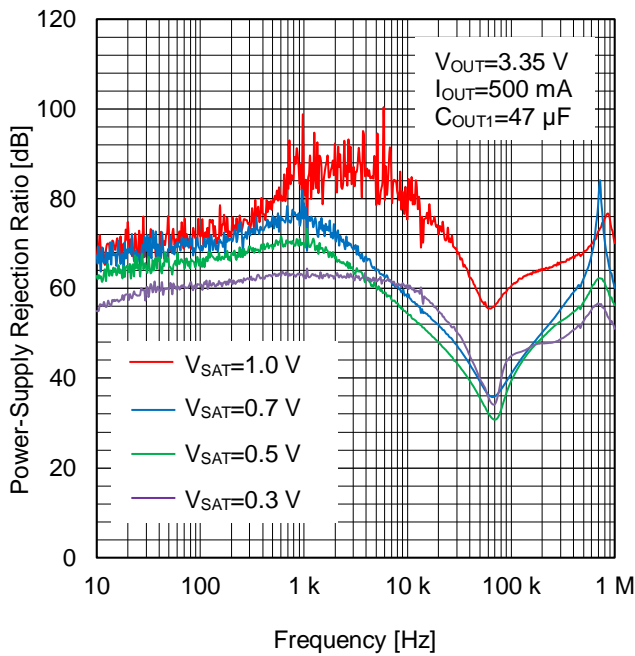


Figure 23. Power-Supply Rejection Ratio ($V_{OUT}=3.35\text{ V}$)

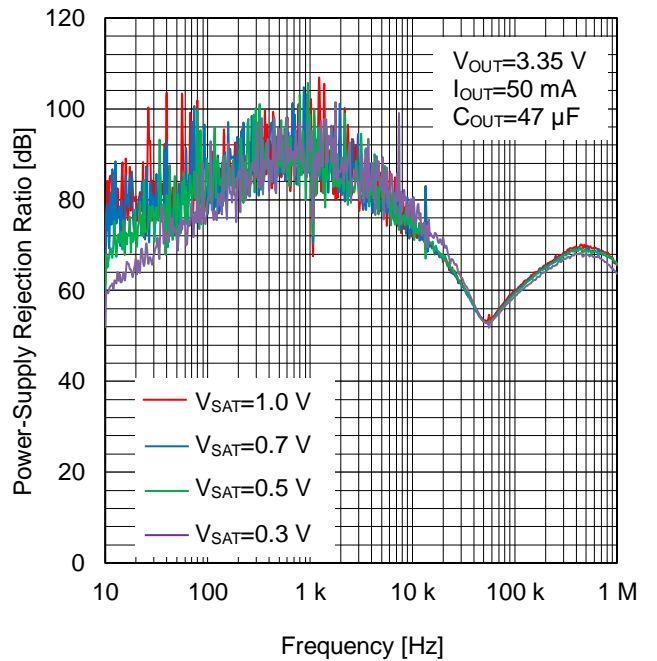


Figure 24. Power-Supply Rejection Ratio ($V_{OUT}=3.35\text{ V}$)

Typical Performance Curves – continued

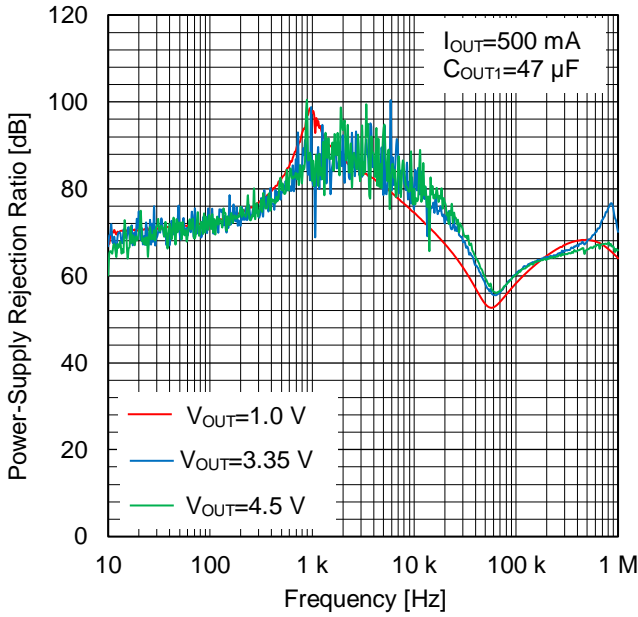


Figure 25. Power-Supply Rejection Ratio

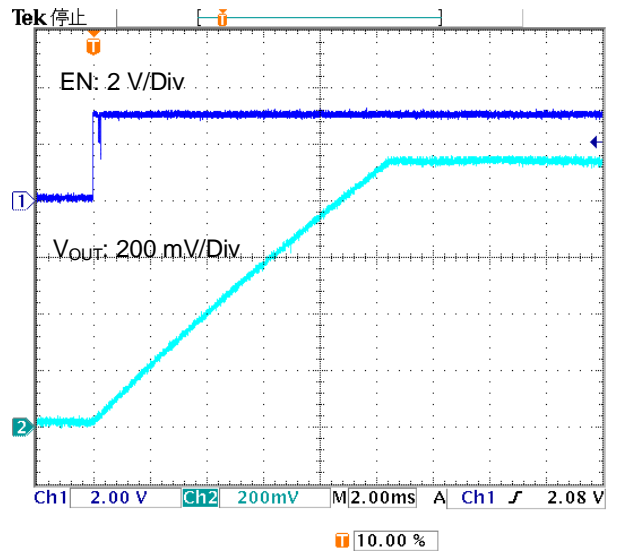


Figure 26. Soft Start ($V_{OUT}=1.0\text{ V}$)

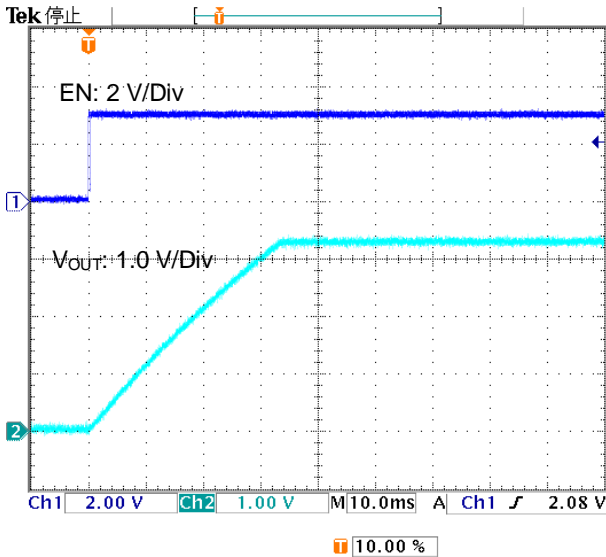


Figure 27. Soft Start ($V_{OUT}=3.35\text{ V}$)

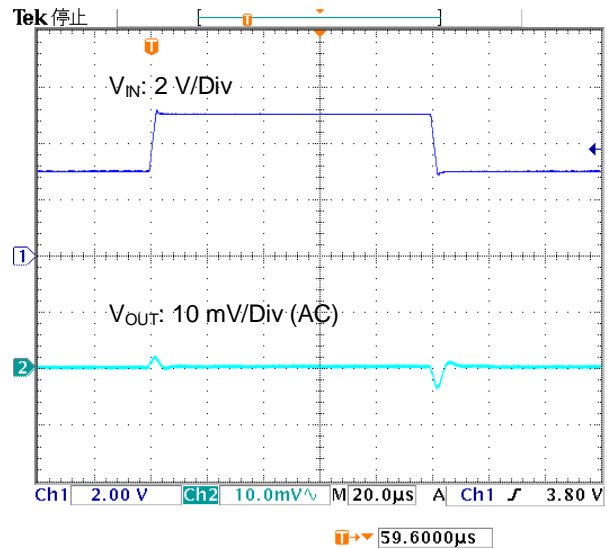


Figure 28. Line Transient ($I_{OUT}=500\text{ mA}$ Slew Rate= $1\text{ V}/\mu\text{s}$ $V_{OUT}=1.0\text{ V}$)

Typical Performance Curves – continued

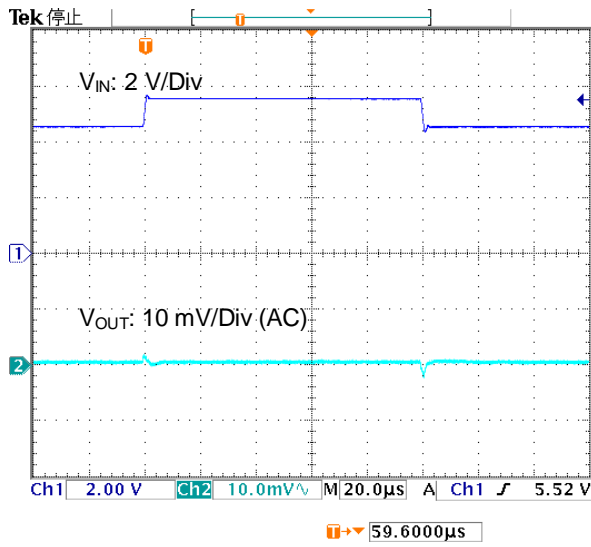


Figure 29. Line Transient
($I_{OUT}=500\text{ mA}$ Slew Rate= $1\text{ V}/\mu\text{s}$ $V_{OUT}=3.35\text{ V}$)

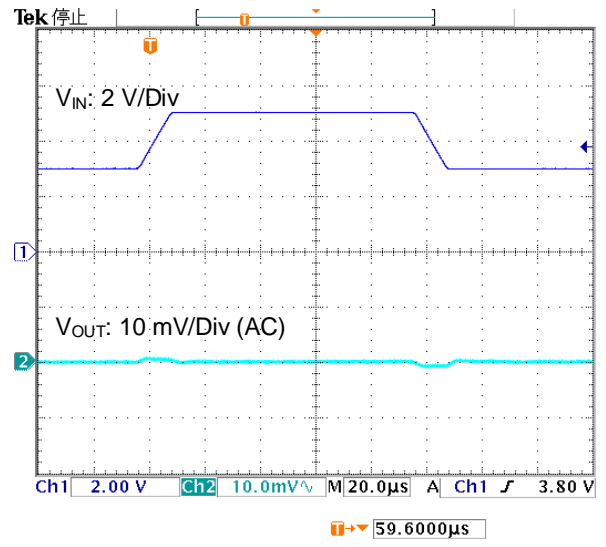


Figure 30. Line Transient
($I_{OUT}=500\text{ mA}$ Slew Rate= $0.2\text{ V}/\mu\text{s}$ $V_{OUT}=1.0\text{ V}$)

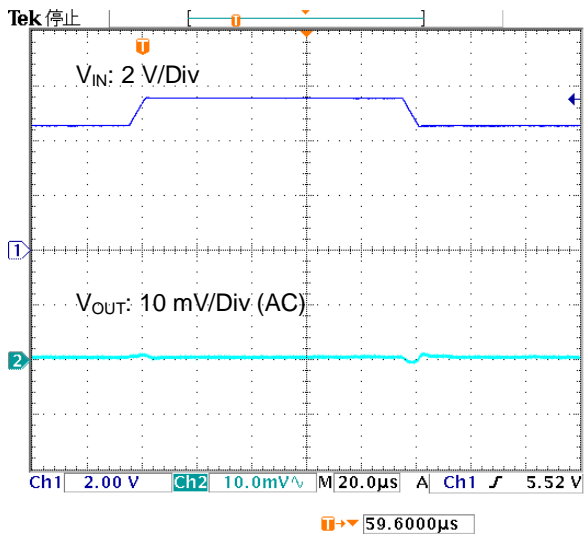


Figure 31. Line Transient
($I_{OUT}=500\text{ mA}$ Slew Rate= $0.2\text{ V}/\mu\text{s}$ $V_{OUT}=3.35\text{ V}$)

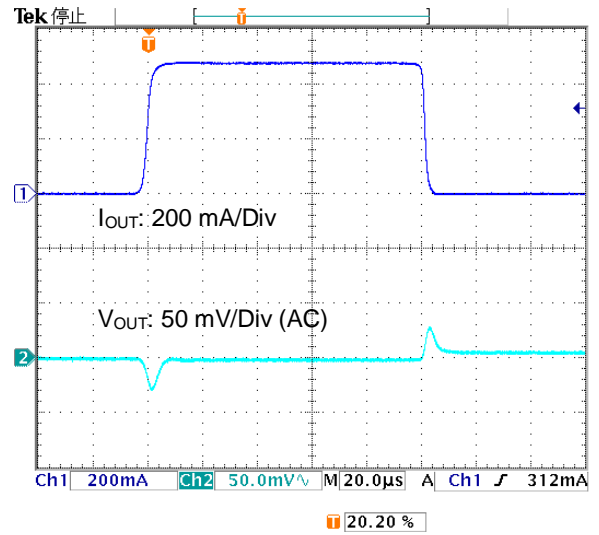


Figure 32. Load Transient
($I_{OUT}=0\text{ mA}$ to 500 mA $V_{OUT}=1.0\text{ V}$)

Typical Performance Curves – continued

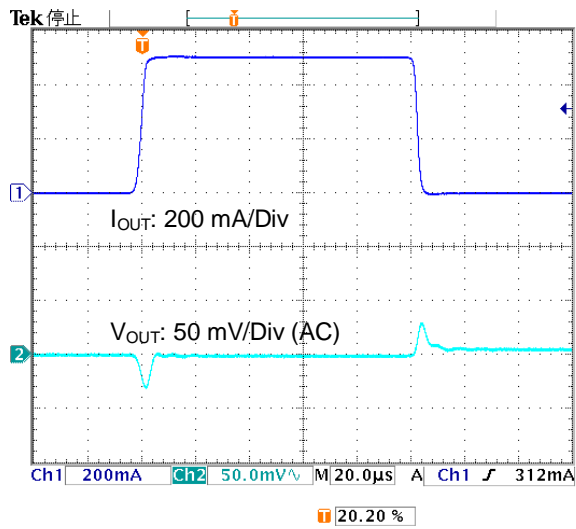
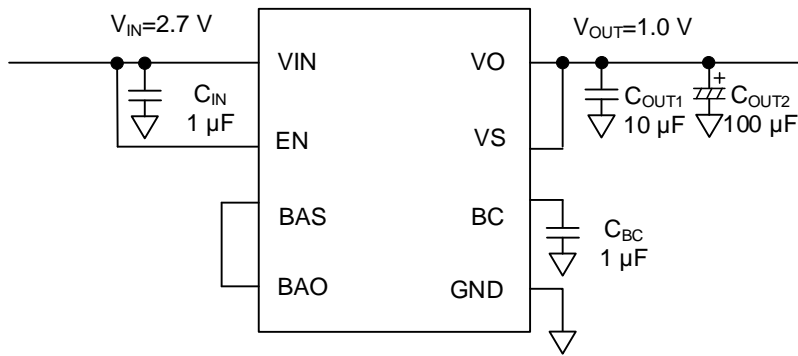


Figure 33. Load Transient
(I_{OUT}=0 mA to 500 mA V_{OUT}=3.35 V)

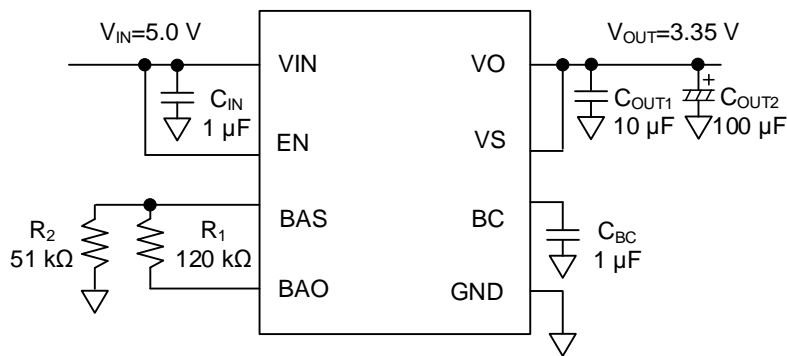
Application Examples



| Parts | Maker | Value | Parts |
|-------------------|--------------|--------|--------------|
| C _{IN} | Rubycon | 1 μF | 16MU105M3216 |
| C _{OUT1} | Rubycon | 10 μF | 16MU106M4532 |
| C _{OUT2} | Toshin Kogyo | 100 μF | 1CUTSJ101M0 |
| C _{BC} | Rubycon | 1 μF | 16MU105M3216 |

(Note) This application example is just one case. Actual setting will be decided after a thorough evaluation and verification in the set.
 (Note) Set the capacity of the capacitor not to be less than the minimum in consideration of temperature or DC bias properties.

Figure 34. Application Circuit 1 (V_{OUT}=1.0 V)



| Parts | Maker | Value | Part Number |
|-------------------|--------------|--------|---------------|
| R ₁ | ROHM | 120 kΩ | MCR03EZPD1203 |
| R ₂ | ROHM | 51 kΩ | MCR03EZPD5102 |
| C _{IN} | Rubycon | 1 μF | 16MU105M3216 |
| C _{OUT1} | Rubycon | 10 μF | 16MU106M4532 |
| C _{OUT2} | Toshin Kogyo | 100 μF | 1CUTSJ101M0 |
| C _{BC} | Rubycon | 1 μF | 16MU105M3216 |

(Note) This application example is just one case. Actual setting will be decided after a thorough evaluation and verification in the set.
 (Note) The value of R₁ and R₂ is set that R₁ + R₂ becomes 100 kΩ or above.
 The resistance for voltage setting is recommended the one that is 1 % accuracy or below.
 (Note) Set the capacity of the capacitor not to be less than the minimum in consideration of temperature or DC bias properties.

Figure 35. Application Circuit 2 (V_{OUT}=3.35 V)

Selection of Components Externally Connected

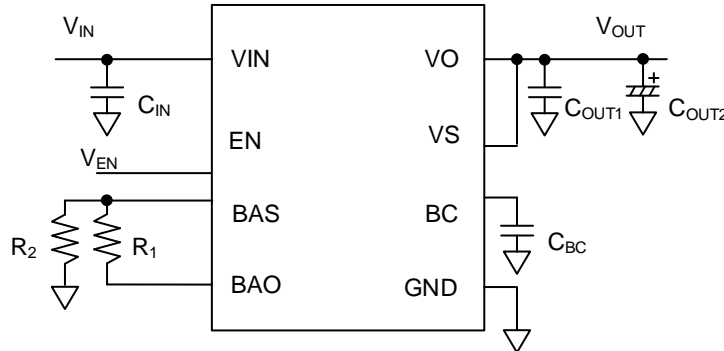


Figure 36. External Components Connection

1. Output Voltage Setting

To set output voltage, connect resistance of R₁ between the BAO pin and the BAS pin and connect resistance of R₂ in between the BAS pin and GND. The value of R₁ and R₂ is set that R₁ + R₂ becomes 100 kΩ or above. In addition, the resistance for voltage setting is recommended the one that is 1 % accuracy or below. In the case to use 1 V setting, short the BAS pin with the BAO pin.

$$V_{OUT} = V_{BAS} \times \frac{R_1 + R_2}{R_2} \quad [V]$$

$$V_{BAS} = 1.0 \quad [V] \text{ (Typ)}$$

2. Output Capacitor C_{OUT1}, C_{OUT2}

Output capacitor C_{OUT1} should be selected 1 μF or above considering about the voltage modulation, thermal characteristics, and distribution of the value. Also, Output capacitor C_{OUT2} should be selected 4.7 μF or above considering about the voltage modulation, thermal characteristics, and distribution of the value. Installation of output capacitor in the position near the pin in between VO and GND is recommended. In addition, the rated voltage of capacitor should be set with enough margins to output voltage.

The ESR of Output Capacitor C_{OUT1} effect the stability of IC operation. Refer the stable operation range for the selection of Output Capacitor which is given in the reference data of Figure 37. This reference data is measured in combination of the film capacitor of 10 μF and ESR in series to Output Capacitor C_{OUT1} and the electrolytic capacitor of 100 μF in parallel to Output Capacitor C_{OUT2}. The Stable operation range of this graph is given by only the IC and load resistance. For actual applications, the stable operating range is influenced by the wiring impedance of the PCB panel, input supply impedance and load impedance. Therefore, verification of the final operating environment is needed.

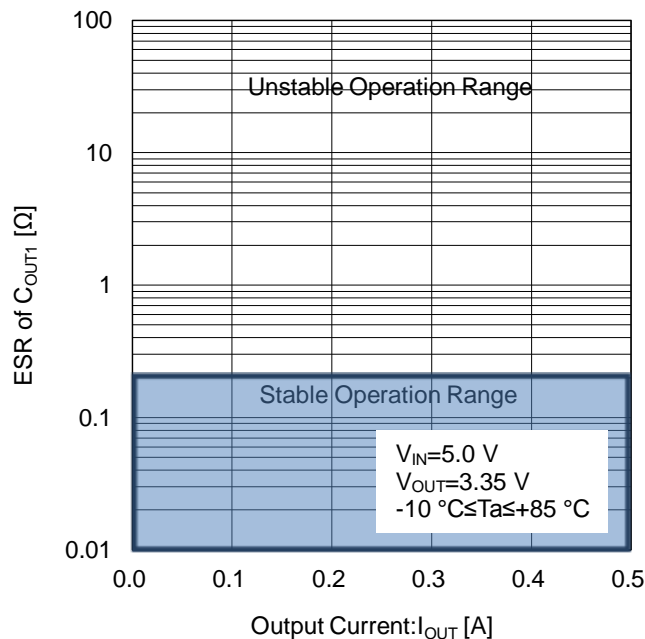


Figure 37. ESR of C_{OUT1} vs Output Current

Selection of Components Externally Connected – continued

3. Input Capacitor C_{IN}

Input capacitor should be selected 0.47 μ F or above considering about the voltage modulation, thermal characteristics, and distribution of the value. Installation of input capacitor in the position close to the pin in between VIN and GND is recommended also. In addition, the rated voltage of capacitor shall be set with enough margins with respect to input voltage.

4. Filter Capacitor C_{BC}

Filter capacitor C_{BC} and built-in resistance formed a low pass filter that reduces the noise that appears in output voltage. In addition, the filter capacitor C_{BC} also has a soft start function because it limits the rush current of output when it starts. The rising speed depends on the internal charging current 100 μ A (Typ), the capacitance value connected to the BC pin and on the output programmed voltage. The time of the soft start is about 15.3 ms (Max) if capacitance is 1 μ F and output programmed voltage is 1.0 V, and almost 45.4 ms (Max) if output programmed voltage is set to 3.35 V.

Because the higher value of capacitor will decrease the noise but the soft start time will be longer, it should be decided that the proper value of the capacitance.

Refer the following calculation for C_{BC} capacitance. Depending on the output capacitor, there is a possibility not to operate properly.

$$C_{BC} \geq \frac{C_{OUT1} + C_{OUT2}}{1000} \quad [F]$$

I/O Equivalence Circuits

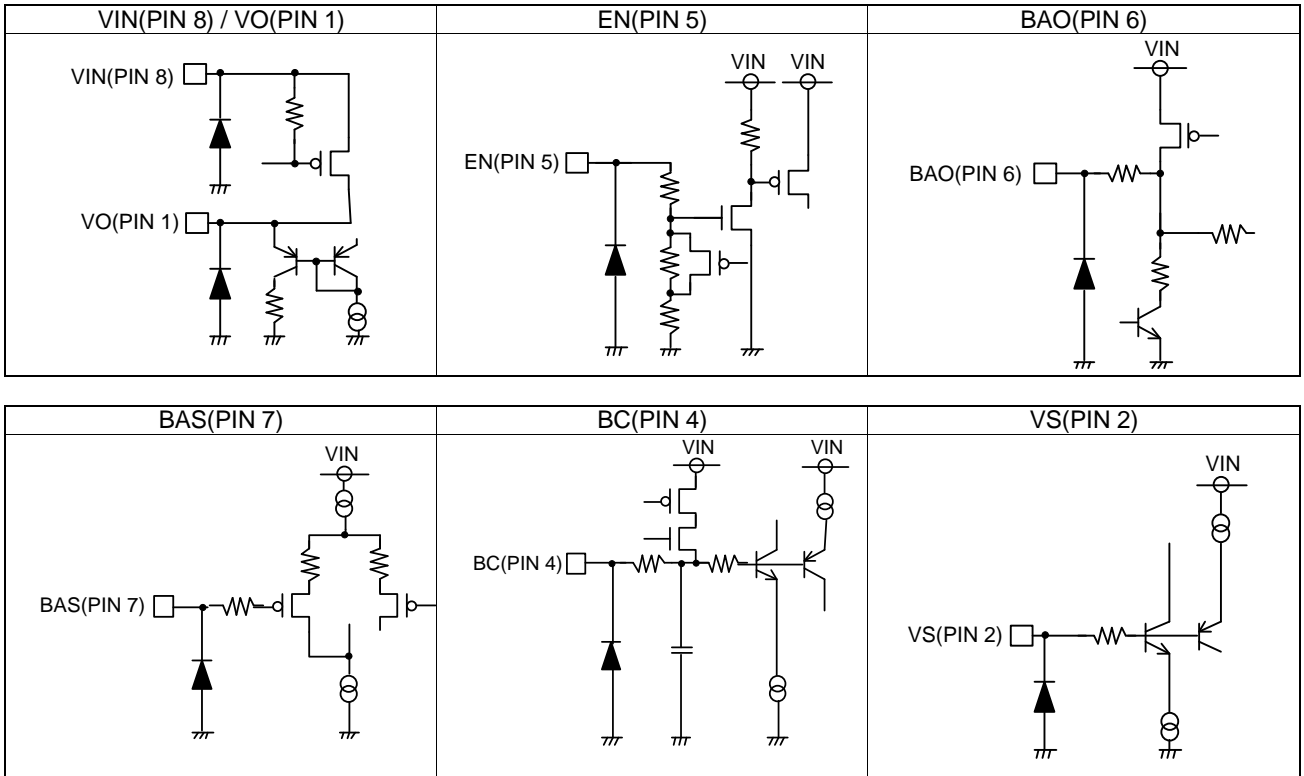
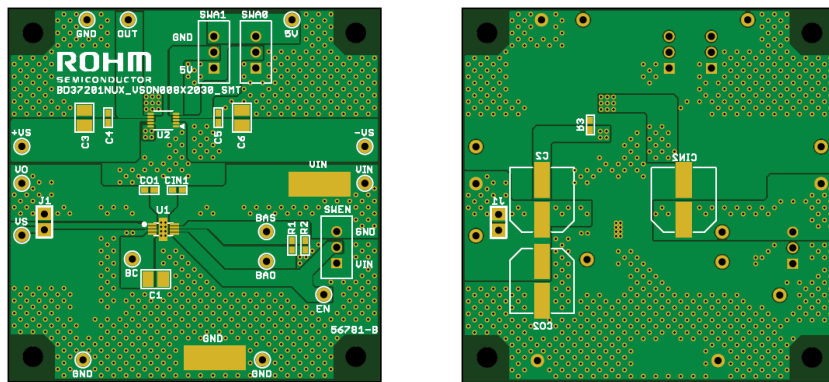


Figure 38. I/O Equivalence Circuits

PCB Layout Example



TOP
BOTTOM
(board size 60mm x 60mm, board thickness 1.6mm, material FR-4)

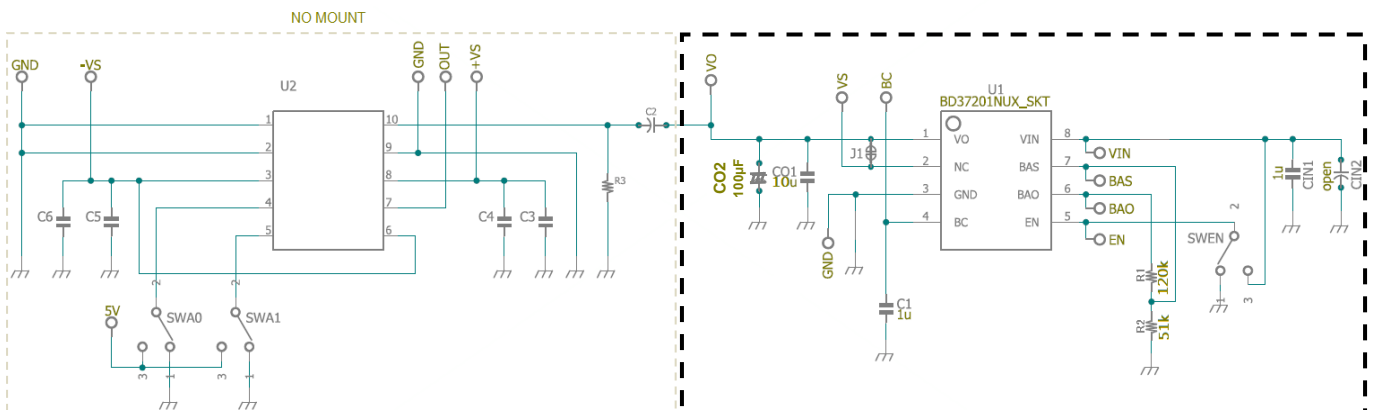


Figure 39. Circuit diagram of evaluation board

(Note) This PCB Layout example includes the test pattern also. This IC position is U1.

Operational Notes

1. Reverse Connection of Power Supply

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

9. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

10. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.

When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

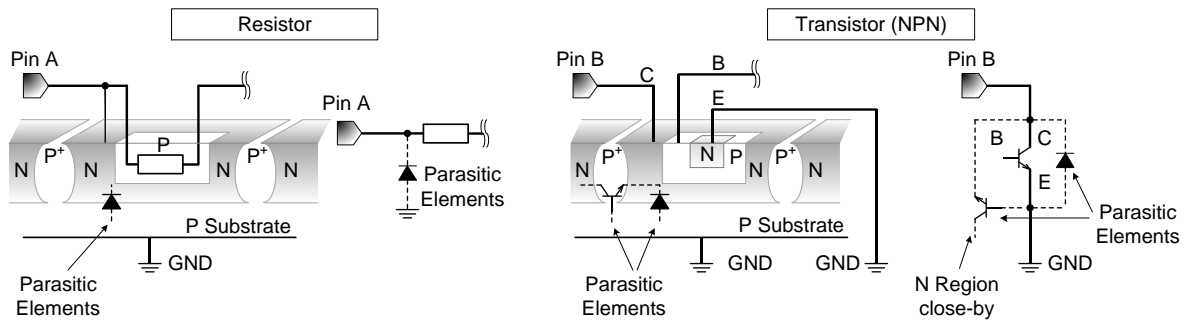


Figure 40. Example of monolithic IC structure

11. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

12. Thermal Shutdown Circuit (TSD)

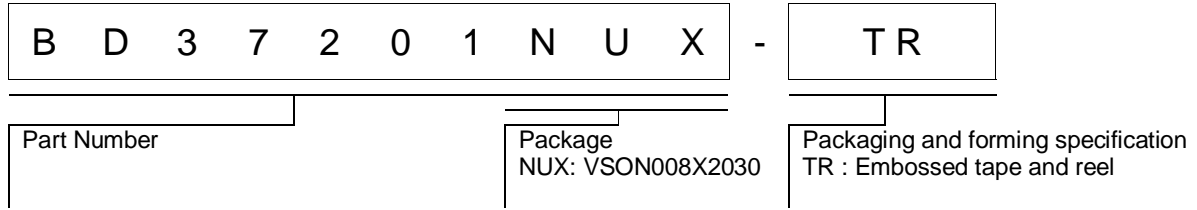
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF power output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

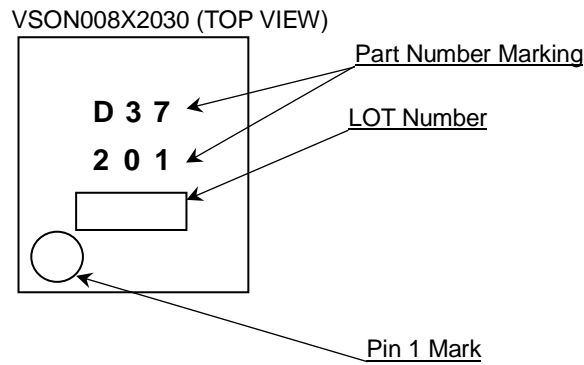
13. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

Ordering Information

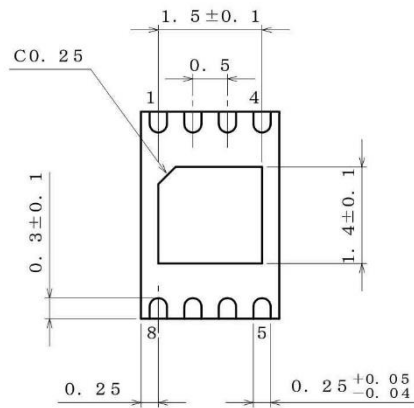
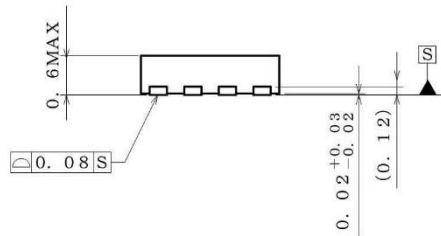
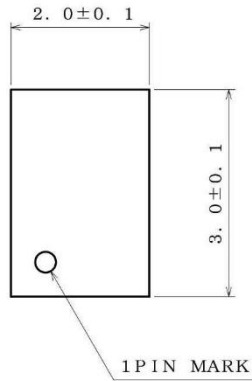


Marking Diagram



Physical Dimension and Packing Information

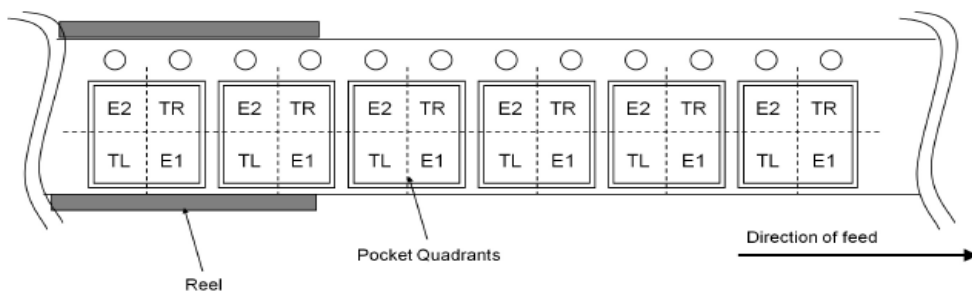
| | |
|--------------|--------------|
| Package Name | VSON008X2030 |
|--------------|--------------|



(UNIT : mm)
 PKG : VSON008X2030
 Drawing No. EX187-5001

<Tape and Reel information>

| | |
|-------------------|---|
| Tape | Embossed carrier tape |
| Quantity | 4000pcs |
| Direction of feed | TR (The direction is the 1 pin of product is at the upper right when you hold reel on the left hand and you pull out the tape on the right hand) |



Revision History

| Date | Revision | Changes |
|-------------|----------|---|
| 18.Apr.2016 | 001 | New Release |
| 19.Mar.2018 | 002 | Renewed the title Renewed Typical Performance Curves |
| 5.Oct.2018 | 003 | Change the Output Capacitor Renewed Typical Performance Curves |
| 7.Feb.2019 | 004 | Change the Operating Temperature Range |

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(Note1) Medical Equipment Classification of the Specific Applications

| JAPAN | USA | EU | CHINA |
|-----------|-----------|------------|-----------|
| CLASS III | CLASS III | CLASS II b | CLASS III |
| CLASS IV | | CLASS III | |

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 - Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl₂, H₂S, NH₃, SO₂, and NO₂
 - Use of our Products in places where the Products are exposed to static electricity or electromagnetic waves
 - Use of our Products in proximity to heat-producing components, plastic cords, or other flammable items
 - Sealing or coating our Products with resin or other coating materials
 - Use of our Products without cleaning residue of flux (Exclude cases where no-clean type fluxes is used. However, recommend sufficiently about the residue.) ; or Washing our Products by using water or water-soluble cleaning agents for cleaning residue after soldering
 - Use of the Products in places subject to dew condensation
- The Products are not subject to radiation-proof design.
- Please verify and confirm characteristics of the final or mounted products in using the Products.
- In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse, is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.
- De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.
- Confirm that operation temperature is within the specified range described in the product specification.
- ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

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- When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.
- In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

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2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.
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[TCR3DF27,LM\(CT](#) [TCR3DF19,LM\(CT](#) [TCR3DF125,LM\(CT](#) [TCR2EN18,LF\(S](#) [AP2112R5A-3.3TRG1](#) [AP7315-25W5-7](#)
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