CXPI Transceiver for Automotive

BD41001FJ-C

General Description

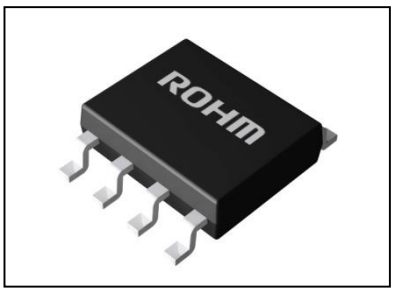
BD41001FJ-C can reduce EMI (Electromagnetic Emission) noise of AM frequency band in comparison with BD41000AFJ-C. BD41001FJ-C is a transceiver for the CXPI (Clock Extension Peripheral Interface) communication. Switching between Master/Slave Mode can be done using the external pin (the MS pin). Low power consumption during standby (non-communication) using Power Saving function. Arbitration function stops transmitter output upon the detection of BUS data collision. Also Fail-safe function stops transmitter output upon the detection of under voltage or temperature abnormality.

Key Specifications

- Power Supply Voltage: +7 V to +18 V
- Absolute Maximum Rating of BAT: -0.3 V to +40 V
- Absolute Maximum Rating of BUS: -27 V to +40 V
- Power OFF Mode Current: 3 µA (Typ)
- Operating Temperature Range: -40 °C to +125 °C

Package

Package	W(Typ) x D(Typ) x H(Max)
SOP-J8	4.90 mm x 6.00 mm x 1.65 mm



SOP-J8

Features

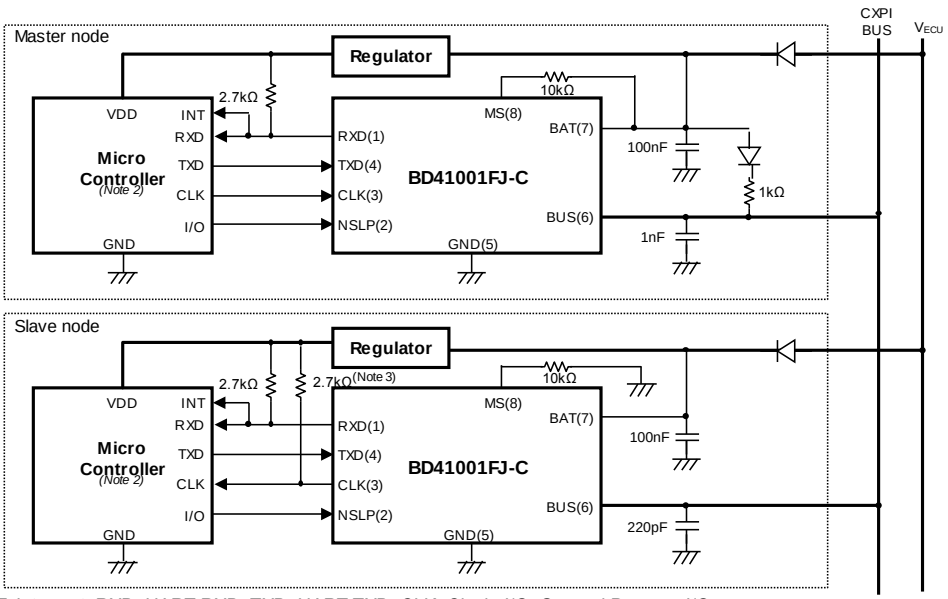
- AEC-Q100 Qualified(Note 1)
- CXPI Standards Qualified
- Transmission Speed Range from 18.8 kbps to 20 kbps
- Master/Slave Switching Function
- Microcontroller Interface Corresponds to 3.3 V/5.0 V
- Built-in Terminator (30 kΩ(Typ))
- Power Saving Function
- Data Arbitration Function
- Built-in Under Voltage Lockout (UVLO) Function
- Built-in Thermal Shutdown (TSD) Function
- Low Electro Magnetic Interference (EMI)
- High Electro Magnetic Susceptibility (EMS)
- High Electro Static Discharge (ESD) Robustness

(Note 1) Grade 1

Applications

- Automotive Networks

Typical Application Circuit



(Note 2) INT: Interrupt, RXD: UART RXD, TXD: UART TXD, CLK: Clock, I/O: General Purpose I/O
(Note 3) While using slave, it is no problem that the CLK pin is opened in the case of non-using the CLK output.

Figure 1. Typical Application Circuit

Consider the actual application design confirming the following linked document before applying this product.

- Application Note

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Pin Configuration

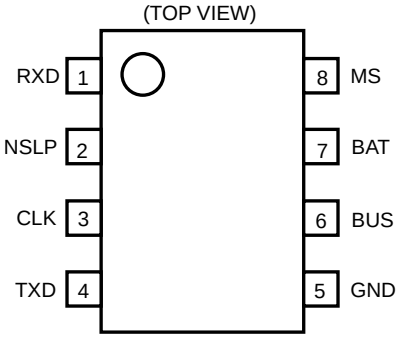


Figure 2. Pin Configuration

Pin Description

Table 1. Pin Description

Pin No.	Pin Name	Function
1	RXD	Received data output pin
2	NSLP	Power saving control input pin (“H”: Change to “Codec Mode”, “L”: Change to “Power OFF Mode”)
3	CLK	Clock signal input/output pin (Master setting: Input, Slave setting: Output)
4	TXD	Transmission data input pin
5	GND	Ground
6	BUS	CXPI BUS pin
7	BAT	Power supply pin
8	MS	Master/Slave switching pin (“H”: Master, “L”: Slave)

Block Diagram

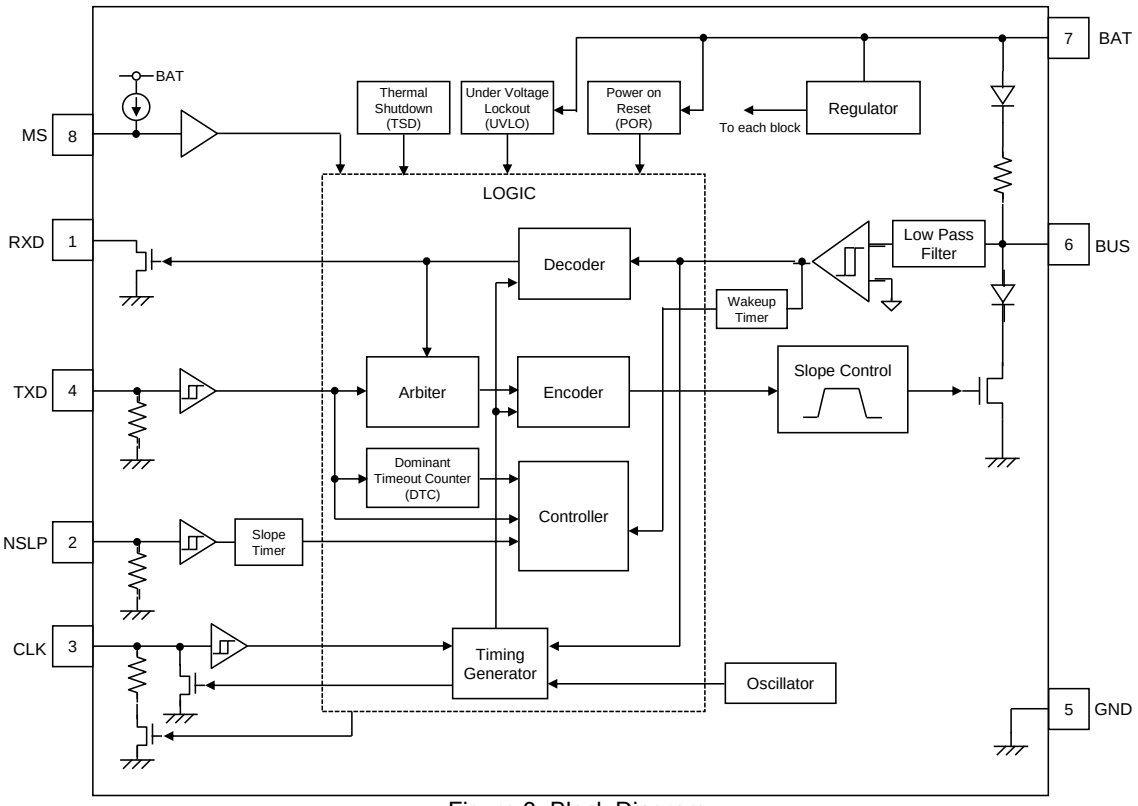
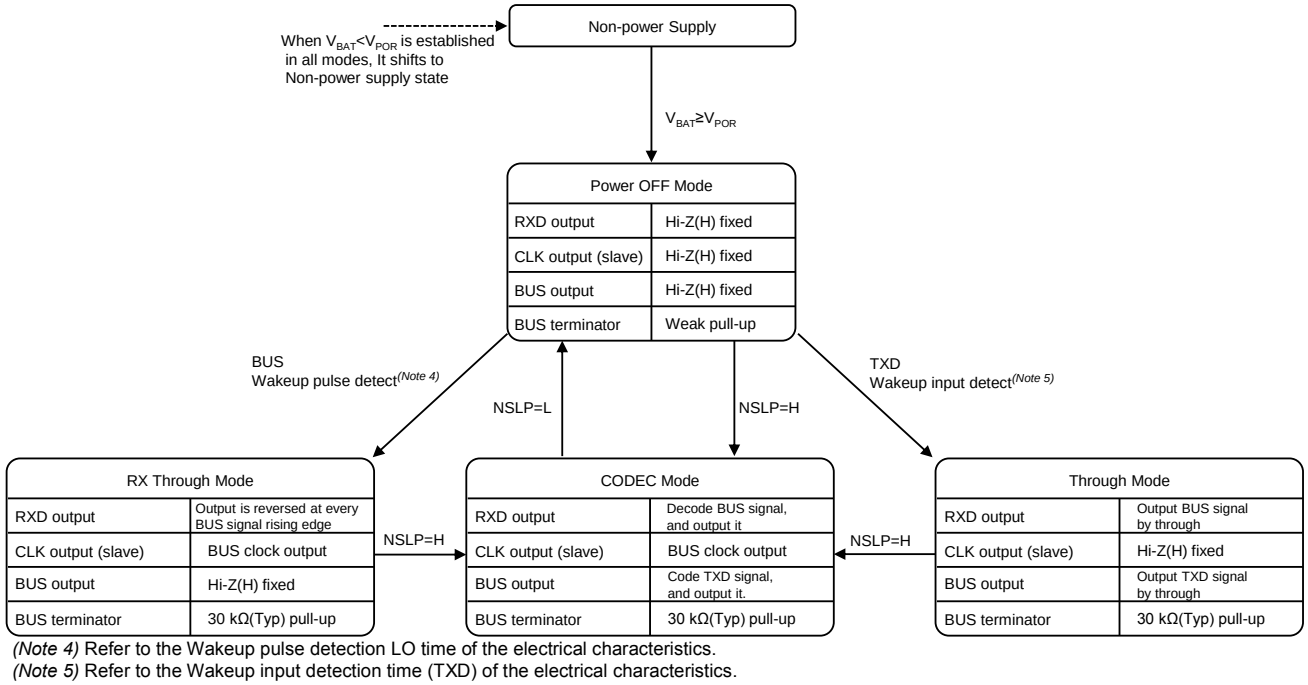


Figure 3. Block Diagram

Description of Blocks

State Transition Diagram

BD41001FJ-C has “Power OFF Mode”, “Through Mode”, “RX Through Mode” other than “CODEC Mode” for power saving control. Each mode is controlled by the NSLP, BUS, and TXD pins.



(Note 4) Refer to the Wakeup pulse detection LO time of the electrical characteristics.
(Note 5) Refer to the Wakeup input detection time (TXD) of the electrical characteristics.

Figure 4. State Transition Diagram

While using master, the CLK pin becomes input pin, and uses to input BUS clock in “CODEC Mode”.

Power OFF Mode

“Power OFF Mode” reduces power consumption by not supplying powers to any circuits other than necessary ones for “Wakeup pulse detection (the BUS pin)” and “Wakeup input detection (the TXD pin)”.
When the TXD pin is “H”, Wakeup input is detected, and then changes to “Through Mode”. If shift to “Power OFF Mode”, set the TXD pin to “L” and then set the NSLP pin to “L”.
“Through Mode” and “RX Through Mode” cannot change to “Power OFF Mode” directly. Change it via “CODEC Mode” by setting the NSLP pin to “H”.

Through Mode

“Through Mode” does not process Coding/Decoding. It only drives signals from the TXD pin to the BUS pin and from the BUS pin to the RXD pin directly.
When sending Wakeup pulse, change to “Through Mode” with the TXD pin as “H”.

RX Through Mode

“RX Through Mode” reverses the RXD pin output at each rising edge of the BUS pin.
When detecting Wakeup pulse in “Power OFF Mode”, monitor the change of the RXD pin

CODEC Mode

“CODEC Mode” is the mode of CXPI communication. NSLP should be “H” for the chip to enter “CODEC Mode”.
The RXD output changes synchronized with the falling edge of the CLK pin when in the Master setting, and with the falling edge of the BUS pin when in the Slave setting. The BUS output is delayed for 2.0±0.5 T_{bit} from the TXD input, and the RXD output is delayed for 1.0±0.5 T_{bit} from the BUS input.
For about the jitter of the clock signal supplying the CLK pin when in the Master setting, input the signal satisfies the CXPI standard (±1.0 %) considering the jitters occurs in the BD41001FJ-C (±0.2 %).

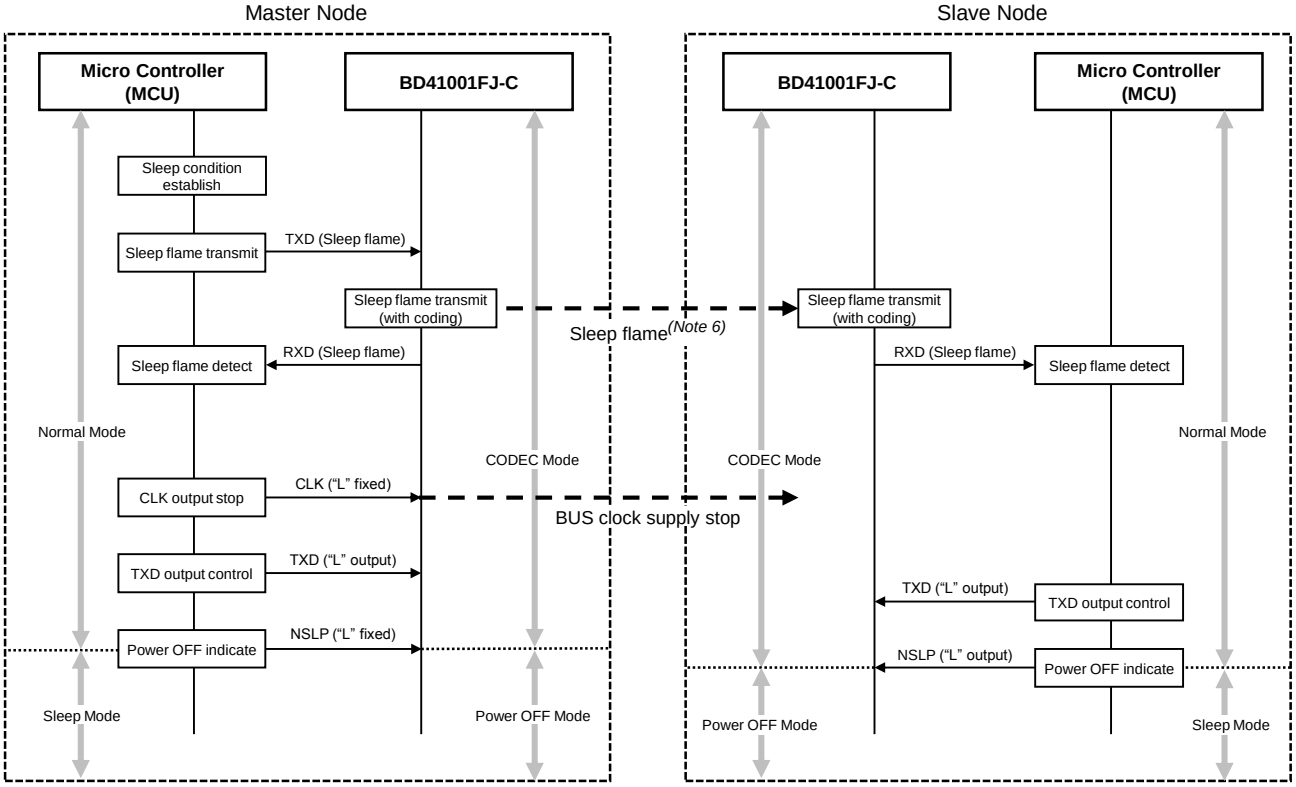
Description of Blocks – continued

Sequence Diagram

Show the examples of the BD41001FJ-C control sequence which corresponding to the mode management of CXPI standard, “Sleep Mode”, “Standby Mode” and “Normal Mode”.(Refer to the CXPI standard for specifications about the detail of mode management.)

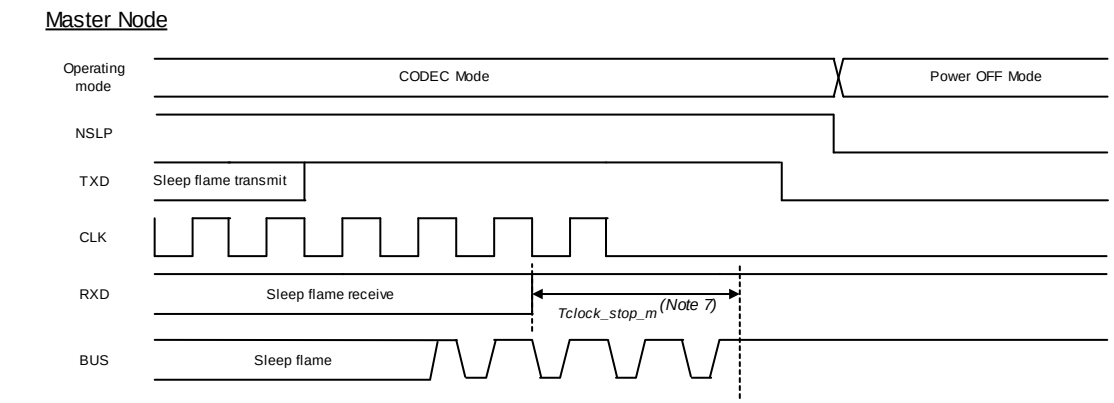
1. The Sequence from “Normal Mode” to “Sleep Mode”

When changing to “Sleep Mode”, the NSLP pin should be switched from “H” to “L”, and then turn the IC to “Power OFF Mode”. The TXD pin has built-in pull-down resistor in case of a fail-safe. Fix the TXD pin to “L” before BD41001FJ-C enters “Power OFF Mode” to prevent extra currents from MCU side while “Sleep Mode”.
Fix the CLK pin to “L” just like the TXD pin, because the pull-down resister of the CLK pin is active in the case of Master setting.



(Note 6) Refer to sleep flame shown in the JASO D015-3 standard.

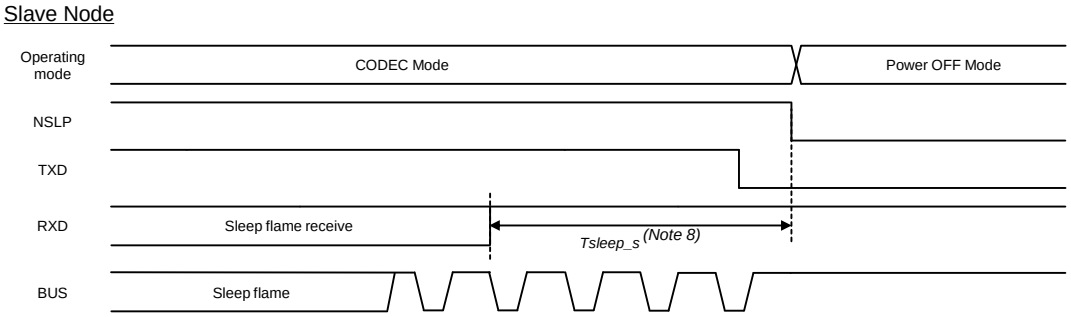
Figure 5. The Sequence from “Normal Mode” to “Sleep Mode”



(Note 7) Refer to *Tclock_stop_m* shown in the JASO D015-3 standard.

Figure 6. The Timing Chart from “Normal Mode” to “Sleep Mode” (Master)

1. The Sequence from "Normal Mode" to "Sleep Mode" – continued



(Note 8) Refer to *Tsleep_s* shown in the JASO D015-3 standard.

Figure 7. The Timing Chart from "Normal Mode" to "Sleep Mode" (Slave)

2. The Sequence from "Sleep Mode" to "Normal Mode" (Master Node Trigger)

To wakeup the node by an internal factor, switch the IC to "CODEC Mode" by setting the NSLP pin to "H". The TXD pin should be "H" within 30 µs before changing from "Power OFF Mode" to "CODEC Mode" in order to prevent abnormal the BUS output or the RXD output.

In the case of slave node, BD41001FJ-C reverses RXD output at every rising edge of the BUS signal after receiving the BUS clock. When start wakeup detecting at the RXD first falling edge, start micro controller initializing operation. To establish wakeup pulse, check if the RXD pin is "H" after initializing operation or detect RXD rising edge.

To change from "Standby Mode" to "Sleep Mode" because the slave node cannot receive the second rising pulse within the specified time, return to "Power OFF Mode" with the NSLP pin as "L" again after the change to "CODEC Mode" with the NSLP pin as "H".

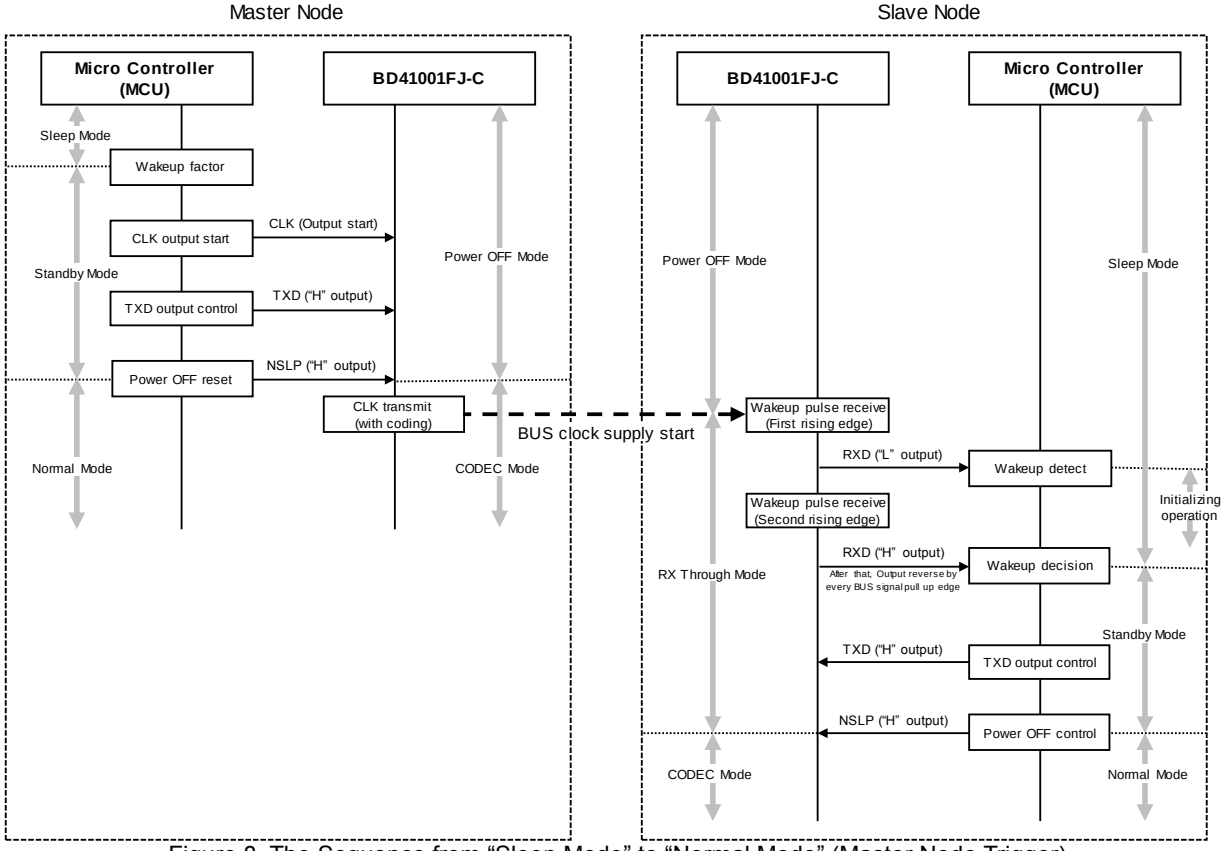


Figure 8. The Sequence from "Sleep Mode" to "Normal Mode" (Master Node Trigger)

2. The Sequence from “Sleep Mode” to “Normal Mode” (Master Node Trigger) – continued

Master Node

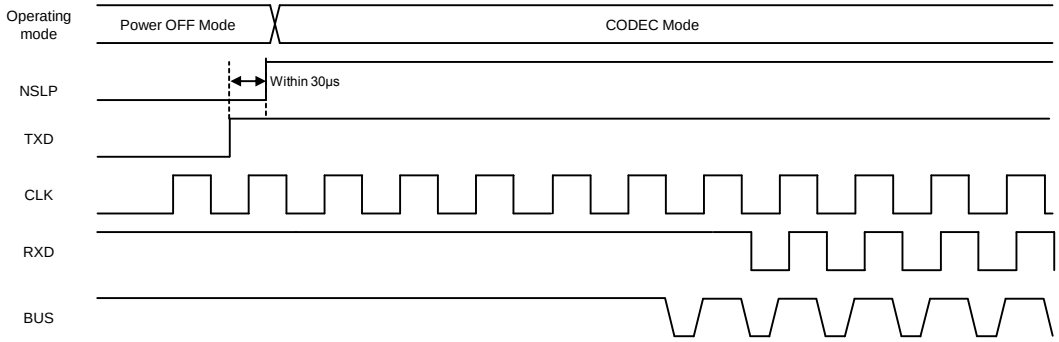


Figure 9. The Timing Chart from “Sleep Mode” to “Normal Mode” (Master Node Trigger, Master)

Slave Node

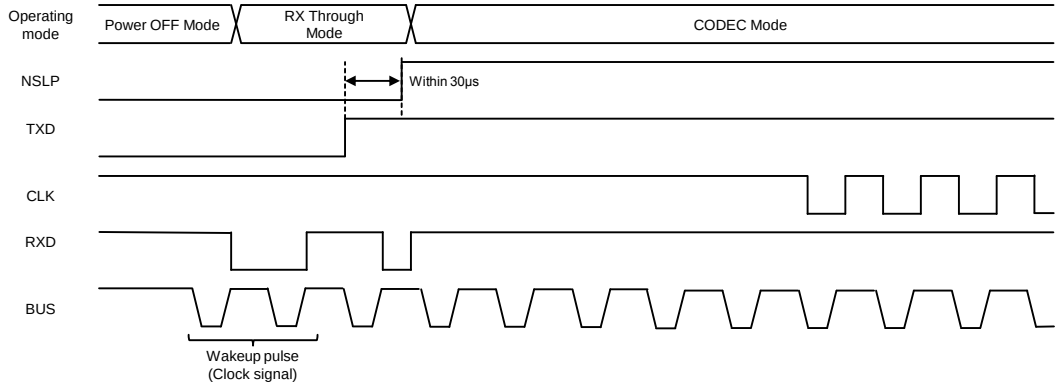


Figure 10. The Timing Chart from “Sleep Mode” to “Normal Mode” (Master Node Trigger, Slave)

Sequence Diagram – continued

3. The Sequence from "Sleep Mode" to "Normal Mode" (Slave Node Trigger)

When waking up the slave node by an internal factor, shift to "Through Mode" by setting the TXD pin to "H" and then send wakeup pulse.
After receiving the wakeup pulse in the Master Node, the RXD output reverses at every rising edge of the BUS signal. Master node should establish wakeup pulse at the RXD first falling edge.
To change from "Standby Mode" to "Sleep Mode", in case the master node cannot receive BUS clock within the specified time, return to "Power OFF Mode" with the NSLP pin as "L" again after the change to "CODEC Mode" with the NSLP pin as "H".

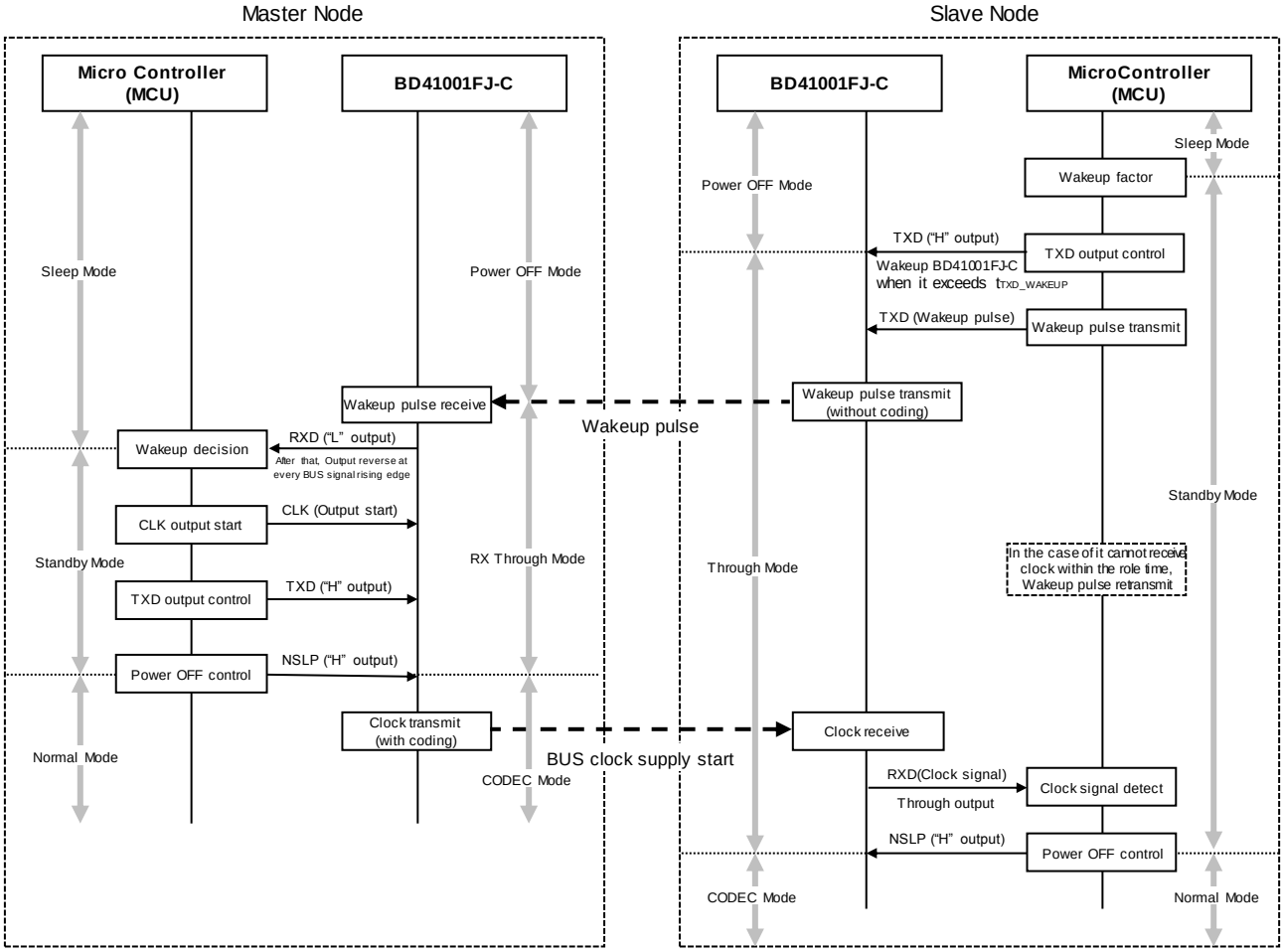
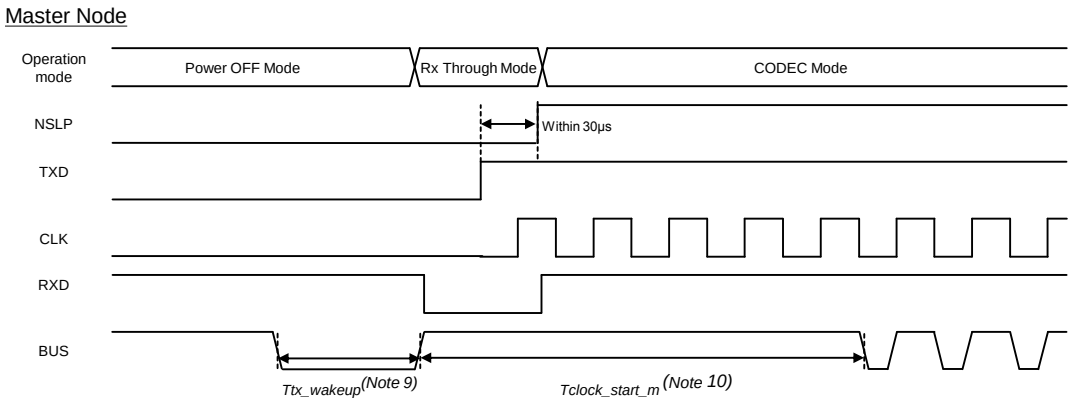


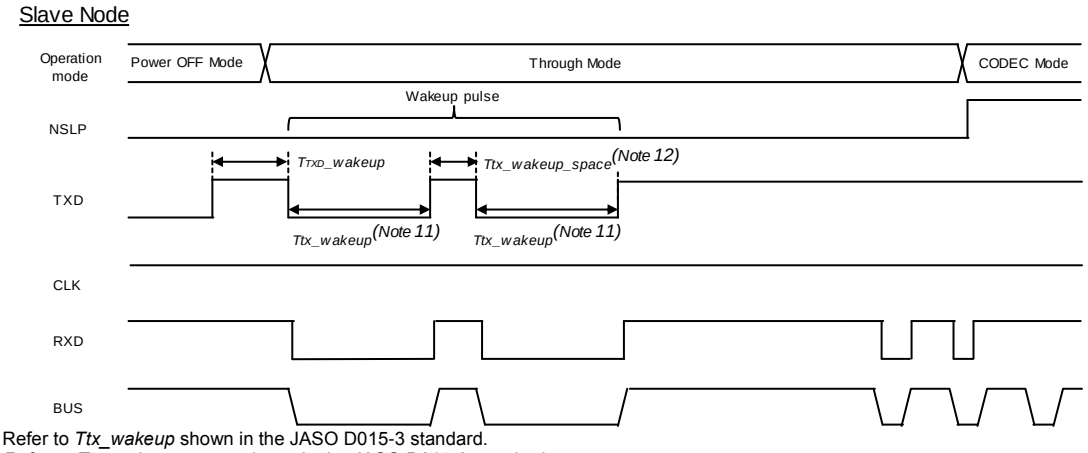
Figure 11. The Sequence from "Sleep Mode" to "Normal Mode" (Slave Node Trigger)



(Note 9) Refer to *Ttx_wakeup* shown in the JASO D015-3 standard.
(Note 10) Refer to *Tclock_start_m* shown in the JASO D015-3 standard.

Figure 12. The Timing Chart from "Sleep Mode" to "Normal Mode" (Slave Node Trigger, Master)

3. The Sequence from "Sleep Mode" to "Normal Mode" (Slave Node Trigger) – continued



(Note 11) Refer to *Ttx_wakeup* shown in the JASO D015-3 standard.
(Note 12) Refer to *Ttx_wakeup_space* shown in the JASO D015-3 standard.

Figure 13. The Timing Chart from "Sleep Mode" to "Normal Mode" (Slave Node Trigger, Slave)

Transmission and Reception Starting Effective Time after Shift to CODEC Mode

After changing to "CODEC Mode" by setting the NSLP pin to "H", BD41001FJ-C detect the clock period and then learn the LO width of logic value1. To secure the learning time of the LO width of logic value1, start to transmit and receive data after the time equal to 16 T_{bit} clocks at least. (After setting the NSLP pin to "H", 6 T_{bit} (maximum) clocks are necessary to output clock signal to the BUS signal input or the CLK signal input.)

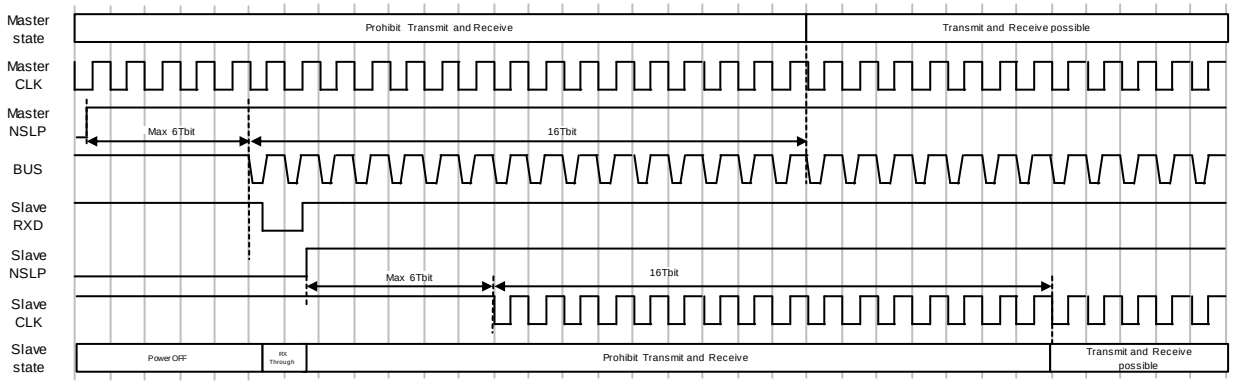


Figure 14. The Actual Time of Transmission and Reception after "CODEC Mode" Changing

Arbitration Function

To carry out collision resolution functions that defined by CXPI specification, both micro controller and BD41001FJ-C share functions. Basically, BD41001FJ-C arbitrates the bit data in the UART flame and micro controller arbitrates the byte data between the UART flames.

1. In case of collision is happened by transmitting from other node at the same time

In the case of collision (arbitration defeat) is happened by transmitting from other node at the same time, it stops the transmission of remaining UART flame data after the collision from micro controller side. It is necessary to have the interval of 1 T_{bit} or more (BUS baud rate period) to transmit again after arbitration defeat. Set the wait time in consideration of the frequency deviation of the baud rate clock in micro controller side and BUS side and the delay at UART circuit in micro controller side.

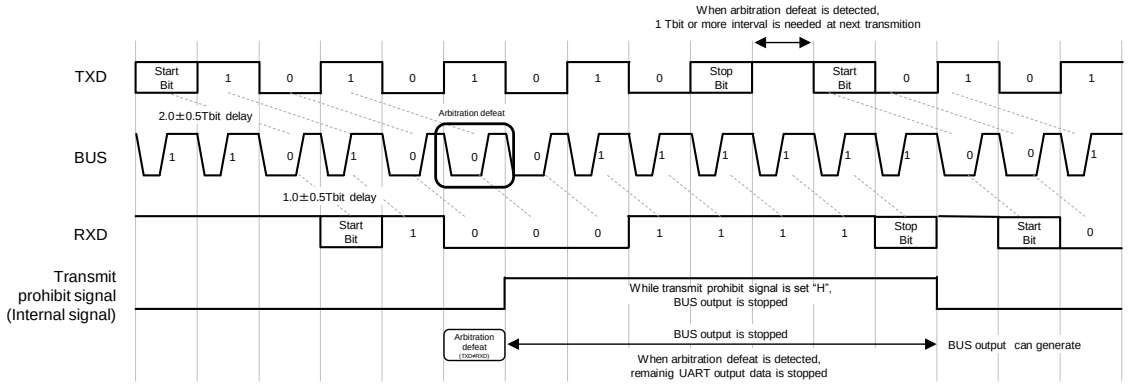


Figure 15. Arbitration Function (When the Collision is detected after Data Transmission)

2. In case of collision is detected by receiving from other node before transmission is started.

After BD41001FJ-C detects transmission of other node on BUS, BD41001FJ-C stops to transmit data for 10 T_{bit} period not to destroy other node transmission. If the TXD signal is inputted to BD41001FJ-C while stopping to transmit data, BD41001FJ-C stops to transmit data for further 10 T_{bit} period of the transmit data.

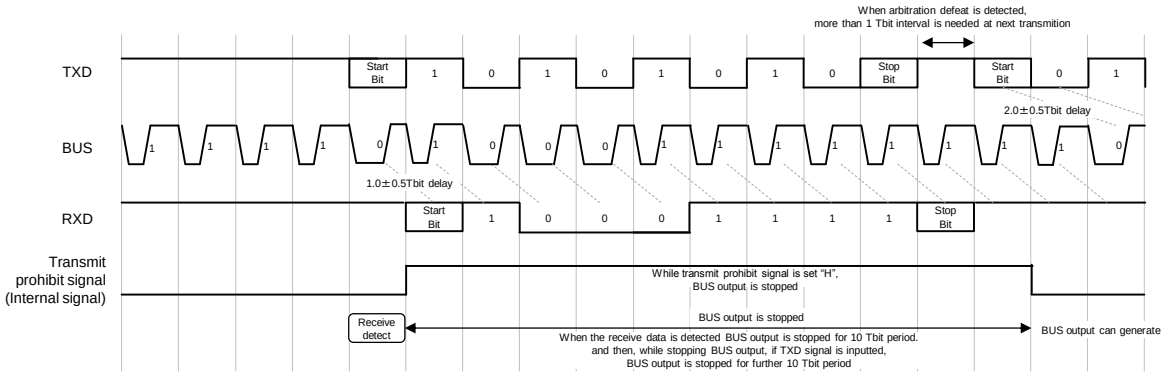


Figure 16. Arbitration Function (When receive data is detected before transmission)

Arbitration Function – continued

3. In case of arbitration function failure is happened because micro controller outputs transmission data to BD41001FJ-C at the out of range of BD41001FJ-C arbitration function.

The BUS output is delayed for 2.5 T_{bit}(Maximum) from the TXD input and the RXD output is delayed for 1.5 T_{bit}(Maximum) from BUS input. When micro controller outputs transmission data to BD41001FJ-C at the timing that shown in Figure 17, CXPI frame of other node is destroyed because BD41001FJ-C outputs PID just after receive PID.
Micro controller should stop transmission while receiving UART flame.
Figure 17 shows the example in case of 2.0 T_{bit} delay from the TXD input to the BUS output and 1.0 T_{bit} delay from the BUS input to the RXD output.

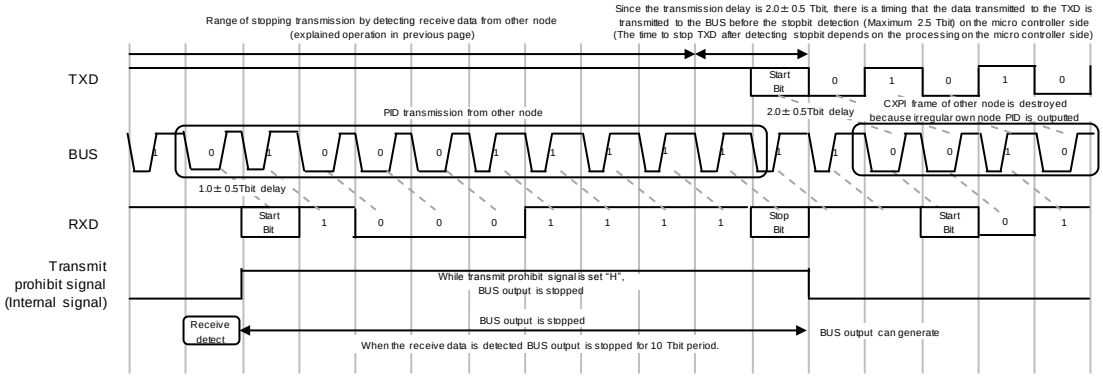


Figure 17. Arbitration Function (When micro controller detects receive data with stopbit)

In case of supporting event trigger method of CXPI standard, not to destroy CXPI flame, micro controller should detect startbit of UART receive flame before transmitting PID, and then stop transmission of PID.

Fail-safe Function

BD41001FJ-C has built in fail-safe mode such as DTC (TXD Dominant Abnormal Detection Circuit), TSD (Abnormal Thermal Detection Circuit) and UVLO/POR (Under Voltage Lockout Circuit/Power ON Reset Circuit).
The operations of each abnormal situation are as follows;

Table 2. Fail-safe Functions

Fail-safe Function	State Transition	BUS Output	RXD Output	CLK Output (While using slave)
DTC abnormality	No change	CODEC Mode: Logical value1 output*(Note 13)* Through Mode: Hi-Z(H) fixed	BUS signal output	Hi-Z(H) fixed
TSD abnormality	No change	Hi-Z(H) fixed	Hi-Z(H) fixed	Hi-Z(H) fixed
UVLO abnormality	No change	Hi-Z(H) fixed	Hi-Z(H) fixed	Hi-Z(H) fixed
POR abnormality	Power OFF Mode	Hi-Z(H) fixed	Hi-Z(H) fixed	Hi-Z(H) fixed

(Note 13) In the case of TXD fixed L, Logical value0 is outputted only in first 10bit. Logical value1 is outputted before DTC abnormality is detected.

When "L" time of the TXD pin is more than t_{DTC}, DTC (Dominant Timeout Counter) detects abnormality, and then it stops output. It can return to normal status with the TXD pin as "H"

When the junction temperature exceeds $T_{TSD,}$ TSD (Thermal Shutdown) circuit detects abnormality, and then it stops output. It can return to normal status when the temperature drops $T_{TSD\_HYS.}$

Operations of UVLO (Under Voltage Lockout) and POR (Power ON Reset) are as follows;
When supply voltage is V_{UVLO} or less, UVLO abnormality is detected, and then the BUS, the RXD and the CLK outputs (only slave) are fixed Hi-Z(H).

When power supply When power supply is V_{UVLO} or more, transceiver restarts output. When supply voltage drops below $V_{POR,}$ POR abnormality is detected, and then it changes to "Power OFF Mode", and reset status.

Fail-safe Function – continued

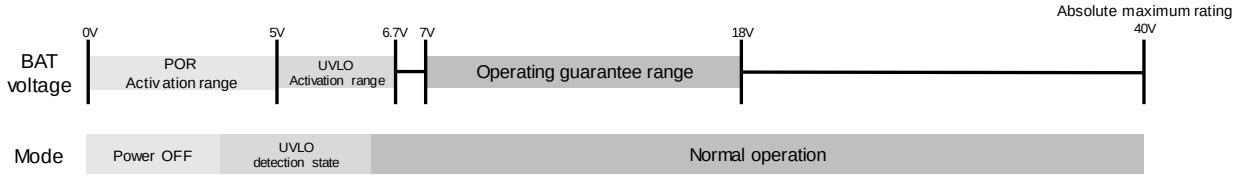


Figure 18. Internal Status and Mode by Supply Voltage

Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V_{BAT}	-0.3 to +40.0	V
Input Voltage	V_{MS}	-0.3 to +40.0	V
	V_{NSLP} ,V_{TXD}	-0.3 to +7.0	
Output Voltage	V_{RXD}	-0.3 to +7.0	V
Input/Output Voltage	V_{BUS}	-27.0 to +40.0	V
	V_{CLK}	-0.3 to +7.0	
Junction Max Temperature	Tjmax	+150	°C
Storage Temperature	Tstg	-55 to +150	°C
Electro Static Discharge (HBM)*(Note 14)*	V_{ESD}	4000	V

(Note 14) JEDEC qualified.

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Thermal Resistance(Note 15)

Table 4. Thermal Resistance

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s(Note 17)	2s2p(Note 18)	
SOP-J8				
Junction to Ambient	θ_{JA}	149.3	76.9	°C/W
Junction to Top Characterization Parameter(Note 16)	Ψ_{JT}	18	11	°C/W

(Note 15) Based on JESD51-2A(Still-Air)
(Note 16) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.
(Note 17) Using a PCB board based on JESD51-3(Table 5).
(Note 18) Using a PCB board based on JESD51-7(Table 6).

Table 5. 1 Layer Board

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt

Top	
Copper Pattern	Thickness
Footprints and Traces	70µm

Table 6. 4 Layers Board

Layer Number of Measurement Board	Material	Board Size
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt

Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70µm	74.2mm x 74.2mm	35µm	74.2mm x 74.2mm	70µm

Recommended Operating Conditions

Table 7. Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{BAT}	7.0	12.0	18.0	V
Operating Temperature	Topr	-40	+25	+125	°C

Electrical Characteristics (Unless Otherwise Specified Ta=-40°C to +125°C, V_{BAT}=7V to 18V)

Table 8. Electrical Characteristics (1)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
BAT						
Supply Current 1	I_{BAT_SLP}	-	3	10	μA	After NSLP shifts from H to L
Supply Current 2	I_{BAT_NOR}	-	3	10	mA	NSLP=H, MS=H, CLK=20kHz (Duty=50%) TXD=10kHz (Duty=50%)
TXD, NLSP, CLK (When Input)						
H Level Input Voltage	V_{IHMCU_IN}	2.0	-	-	V	
L Level Input Voltage	V_{ILMCU_IN}	-	-	0.8	V	
Input H Current	I_{IHMCU_IN}	6.0	14.0	40.0	μA	Input Voltage=5V
Input L Current	I_{ILMCU_IN}	-5.0	0.0	+5.0	μA	
Wakeup Input Detection Time (TXD)	t_{TXD_WAKEUP}	30	100	150	μs	H Width
Input Clock Duty (CLK)	$D_{DUTYCLK}$	48	50	95	%	Duty Rule of H Width
MS						
H Level Input Voltage	V_{IHMS_IN}	V_{BAT}-1.0	-	-	V	
L Level Input Voltage	V_{ILMS_IN}	-	-	V_{BAT}-3.0	V	
Input H Current	I_{IHMS_IN}	-5.0	-	+5.0	μA	Input Voltage= V_{BAT}=18V
Input L Current	I_{ILMS_IN}	-5.0	-	+5.0	μA	In Power OFF Mode
RXD, CLK (When Output)						
Output ON Current	I_{OLMCU_OUT}	1.3	3.5	-	mA	Output Pin=0.4V
Output OFF Current	I_{OHMCU_OUT}	-5.0	0.0	+5.0	μA	Output Pin=5V
BUS (DC Characteristics)						
Recessive Output Voltage *(Note 19)*	V_{BUS_RES}	V_{BAT} x 0.9	-	-	V	R_L=500Ω
Dominant Output Voltage 1 *(Note 19)*	$V_{BUS\_DOM\_1}$	-	-	1.2	V	V_{BAT}=7V, R_L=500Ω
Dominant Output Voltage 2 *(Note 19)*	$V_{BUS\_DOM\_2}$	0.6	-	-	V	V_{BAT}=7V, R_L=1kΩ
Dominant Output Voltage 3 *(Note 19)*	$V_{BUS\_DOM\_3}$	-	-	2.0	V	V_{BAT}=18V, R_L=500Ω
Dominant Output Voltage 4 *(Note 19)*	$V_{BUS\_DOM\_4}$	0.8	-	-	V	V_{BAT}=18V, R_L=1kΩ
H Level Leakage Current	I_{IHBUS}	-5.0	0.0	+5.0	μA	When Recessive Output V_{BAT}=V_{BUS}=18V
Pull-up Resister	R_{BUS}	20	30	50	kΩ	V_{BAT}=12V
Short-circuit Output Current *(Note 19)*	I_{OCPBUS}	40	-	200	mA	V_{BAT}=V_{BUS}=18V, R_L=0Ω
L Current at Receiver Operating	I_{OLBUS}	-1	-	-	mA	V_{BAT}=12V, V_{BUS}=0V
Input Leakage Current at Receiver Operating	I_{LBUS}	-	-	20	μA	V_{BAT}=8V, V_{BUS}=18V
Leakage Current when NO_GND	$I_{LBUS\_NO\_GND}$	-1	-	+1	mA	GND=V_{BAT}=12V, V_{BUS}=0V to 18V
Leakage Current when NO_BAT	$I_{LBUS\_NO\_BAT}$	-	-	100	μA	V_{BAT}=0V, V_{BUS}=0V to 18V
Input H Threshold Voltage	V_{IHBUS_REC}	V_{BAT} x 0.556	-	-	V	
Input L Threshold Voltage	V_{ILBUS_DOM}	-	-	V_{BAT} x 0.423	V	
Input Threshold Voltage (Typical)	V_{THCBUS}	V_{BAT} x 0.475	V_{BAT} x 0.5	V_{BAT} x 0.525	V	
Input Hysteresis Voltage	V_{HYSBUS}	-	-	V_{BAT} x 0.133	V	

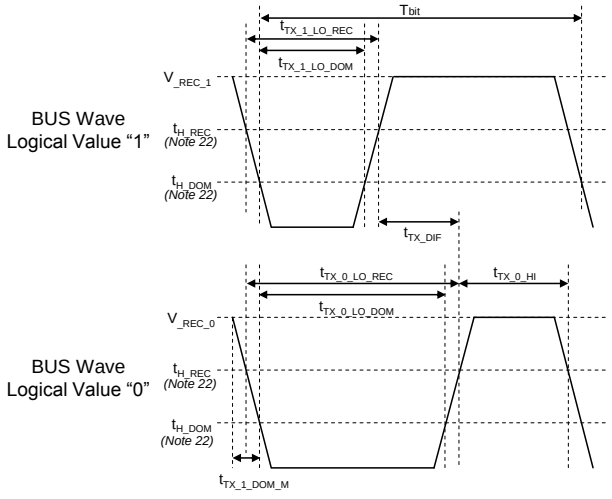
(Note 19) R_L is pull-up resistor that is connected between BAT and BUS terminal outside.

Electrical Characteristics – continued

Table 9. Electrical Characteristics (2)

Parameter	Symbol	Min	Typ	Max	Unit	Conditions
BUS (AC Characteristics)						
LO Level Time 1 of Logical Value “1”*(Note 20)*	$t_{TX\_1\_LO\_REC}$	-	-	$0.39T_{bit}$ +0.6τ	-	t_{H_REC}=70%
LO Level Time 2 of Logical Value “1”	$t_{TX\_1\_LO\_DOM}$	0.11	-	-	T_{bit}	t_{H_DOM}=30%
HI Detection Time of Receiving	$t_{TX\_0\_HI}$	0.06	-	-	T_{bit}	t_{H_REC}=55.6%
Difference of LO Level Time between Logical Value “1” and Logical Value “0”	t_{TX_DIF}	0.06	-	-	T_{bit}	t_{TX_DIF}= $t_{TX\_0\_LO}$ - $t_{TX\_1\_LO}$
Delay Time from the LO Level Detection to Logical Value “0” Output	$t_{TX\_0\_PD}$	-	-	0.11	T_{bit}	t_{H_DOM}=30%
LO Time 1 of Logical Value “0”	$t_{TX\_0\_LO\_REC}$	$t_{TX\_1\_LO\_REC}$ + 0.06	-	-	T_{bit}	t_{H_REC}=70%
LO Time 2 of Logical Value “0”	$t_{TX\_0\_LO\_DOM}$	$t_{TX\_1\_LO\_DOM}$ + 0.06	-	-	T_{bit}	t_{H_DOM}=30%
BUS Pull-down Time	$t_{TX\_1\_DOM\_M}$	-	-	0.16	T_{bit}	t_{H_DOM}=30%
Recessive Voltage of Logical Value “0”	$V_{\_REC\_0}$	93	-	-	%	Ratio for the Recessive Voltage ($V_{\_REC\_1}$) when logical value is 1
Wakeup Pulse Detection LO Time for Master Setting	$t_{RX\_WAKEUP\_MASTER}$	30	100	150	μs	t_{H_DOM}=42.3%
Wakeup Pulse Detection LO Time for Slave Setting	$t_{RX\_WAKEUP\_SLAVE}$	0.5	3	5	μs	t_{H_DOM}=42.3%
TSD						
TSD Detection Temperature *(Note 21)*	T_{TSD}	150	-	200	°C	
TSD Hysteresis Temperature *(Note 21)*	T_{TSD_HYS}	-	14	-	°C	
UVLO						
UVLO Detection Voltage	V_{UVLO}	5.0	-	6.7	V	
POR						
POR Detection Voltage	V_{POR}	-	-	5.0	V	
DTC						
Dominant Time-out Time	t_{DTC}	9	13	22	ms	

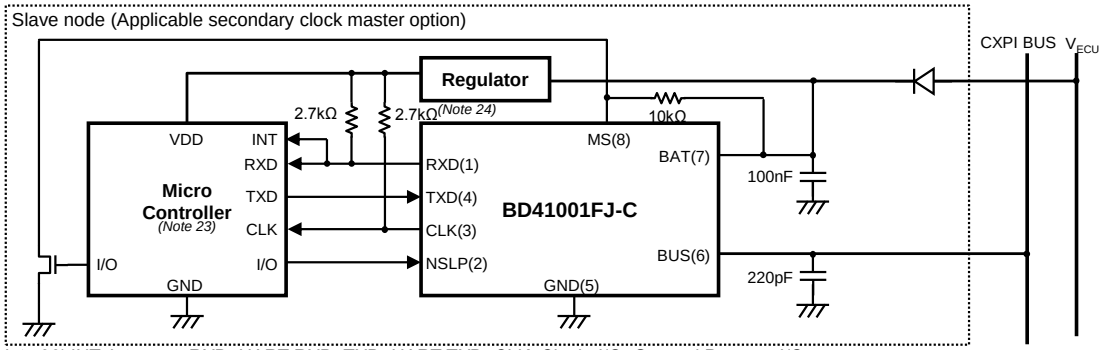
(Note 20) τ is a fixed number when BUS (1μs ≤ τ ≤ 5μs)
(Note 21) It is a design guarantee parameter, and is not production tested.



(Note 22) These parameters are shown as the ratio of V_{BAT}.

Figure 19. BUS Waves of Logical Value 1, 0

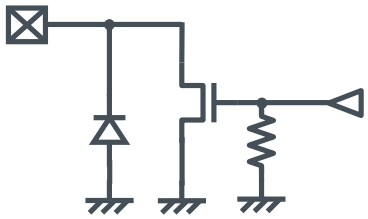
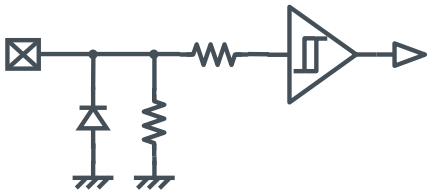
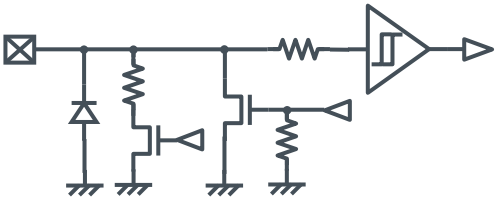
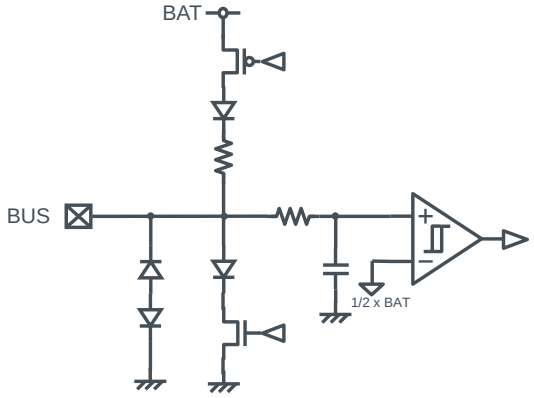
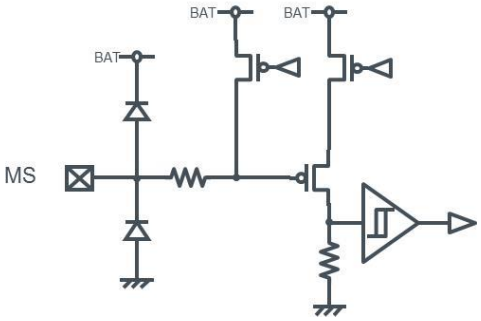
Application Example



(Note 23) INT: Interrupt, RXD: UART RXD, TXD: UART TXD, CLK: Clock, I/O: General Purpose I/O
(Note 24) While using slave, it is no problem that the CLK pin is opened in the case of non-using the CLK output.

Figure 20. Application Example of Secondary Clock Master Option

I/O Equivalence Circuits

Type	Equivalence Circuit	Type	Equivalence Circuit
A	 Output pin: RXD	B	 Input pin: NSLP, TXD
C	 Input/output pin: CLK	D	 CXPI BUS Input/output pin: BUS
E	 Input pin: MS		

Operational Notes

1. **Reverse Connection of Power Supply**
   Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. **Power Supply Lines**
   Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. **Ground Voltage**
   Ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. **Ground Wiring Pattern**
   When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. **Recommended Operating Conditions**
   The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. **Inrush Current**
   When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. **Operation Under Strong Electromagnetic Field**
   Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. **Testing on Application Boards**
   When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. **Inter-pin Short and Mounting Errors**
   Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. **Unused Input Pins**
    Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

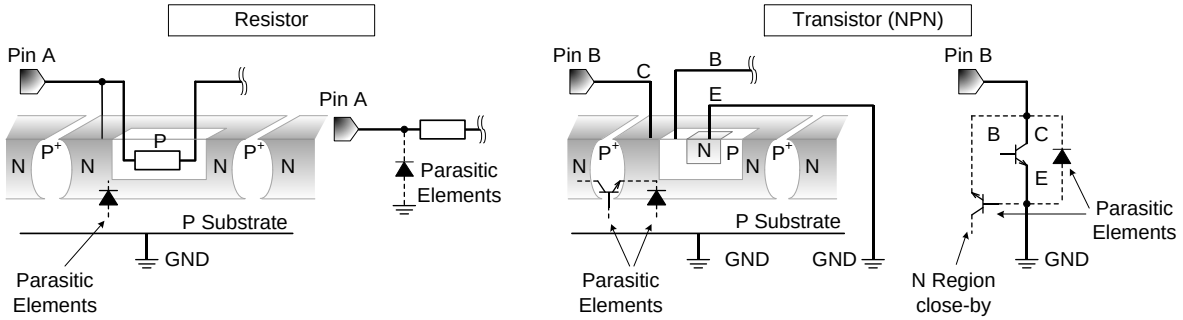


Figure 21. Example of Monolithic IC Structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

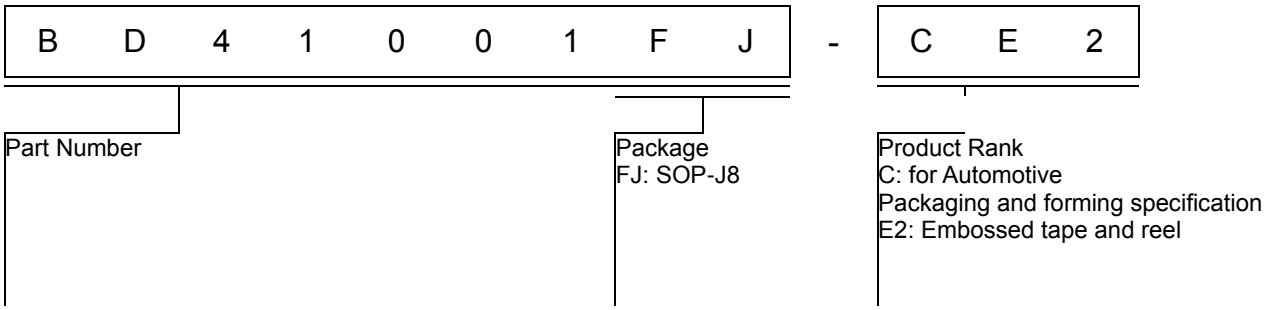
13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

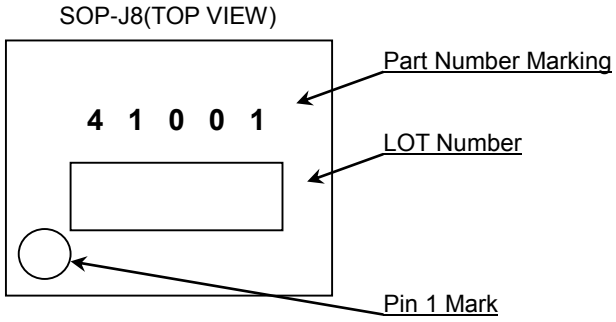
14. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF power output pins. When the Tj falls below the TSD threshold, the circuits are automatically restored to normal operation.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

Ordering Information

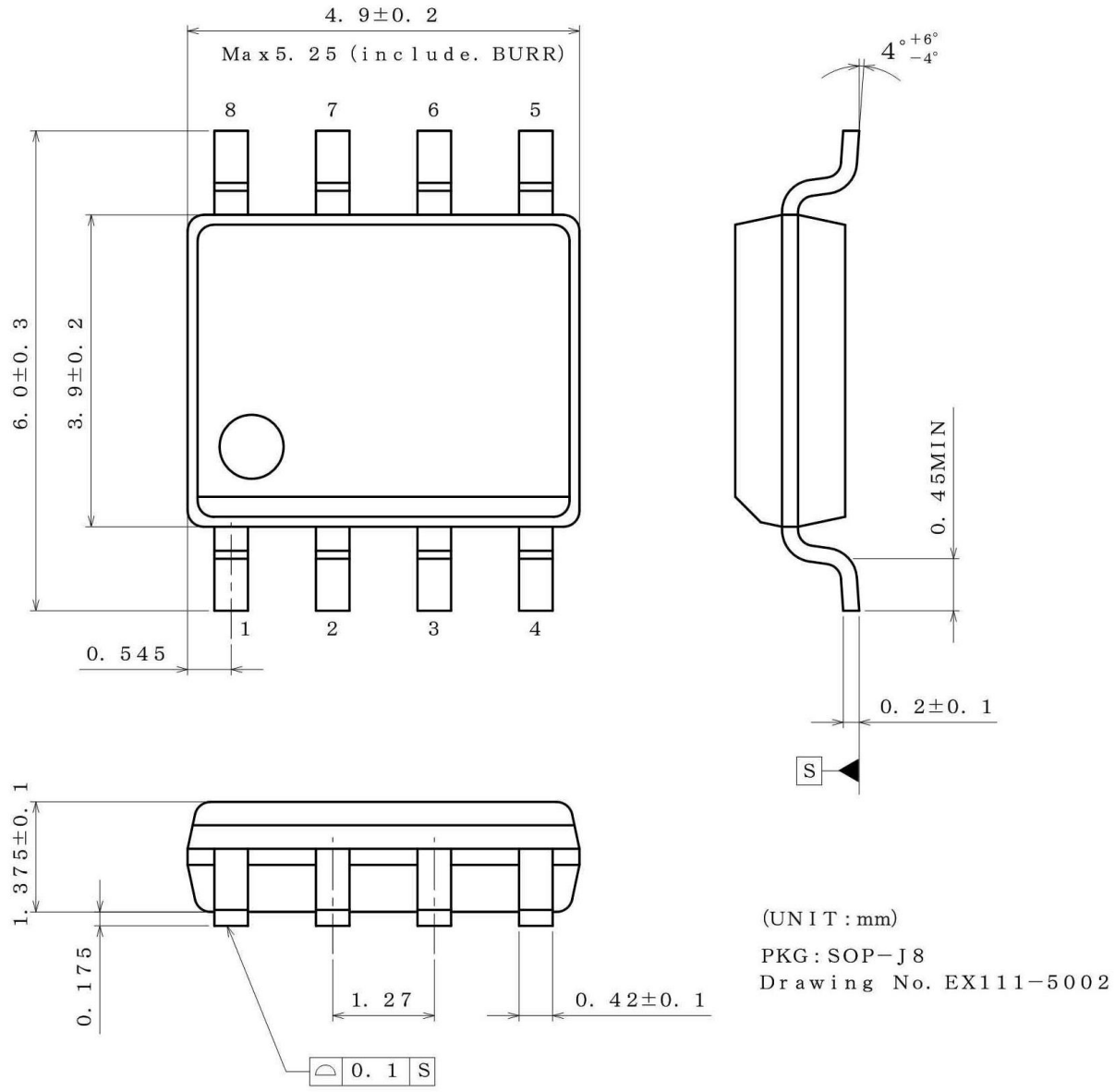


Marking Diagram



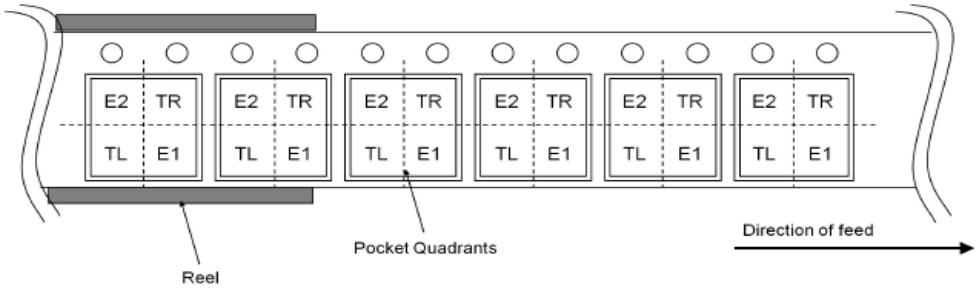
Physical Dimension and Packing Information

Package Name	SOP-J8



<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	2500pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand)



Revision History

Date	Revision	Changes
16.Mar.2018	001	New Release
26.Mar.2019	002	P1 Added the ApplicationNote information P9 1. In case of collision is happened by transmitting from other node at the same time Added a caution about the time to validate the transmit after an arbitration defeat occurred.

Notice

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CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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8. Confirm that operation temperature is within the specified range described in the product specification.

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   - [b] the temperature or humidity exceeds those recommended by ROHM
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2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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