

CAN FD Transceiver for Automotive

BD41044FJ-C

General Description

BD41044FJ-C is a transceiver LSI for CAN-FD communication (Fully ISO 11898-2:2016 compliant). It is equipped with circuitry that functions as transmitter and receiver, necessary for High-speed CAN-FD communication (up to 5Mbps)

Features

- AEC-Q100 Qualified^(Note 1)
 - Transmission Rate of 40kbps to 5Mbps
 - Power Saving Mode Correspondence
 - SPLIT Voltage Output for Stabilizing Recessive Bus Level
 - Under Voltage Detection Function
 - Thermal Shutdown (TSD) Function
 - TXD Dominant Time-out Function (Normal Mode)
 - CAN Bus Dominant Time-out Function (Standby Mode)
 - Bus Wake-up Capability
- (Note 1) Grade1*

Application

- CAN Communication for Automotive Networks

Key Specifications

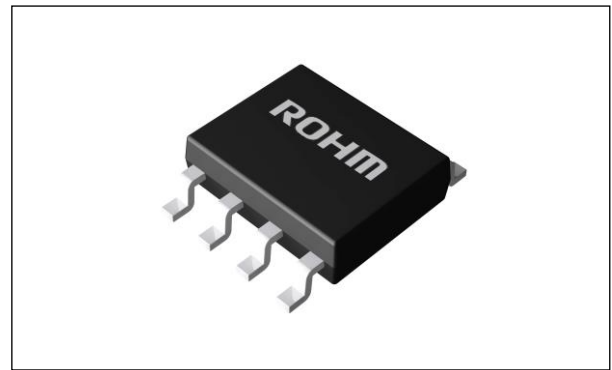
- Recommended Operating Voltage Range: 4.75V to 5.25V
- VCC, TXD, RXD, STB Absolute Maximum Rating: -0.3V to +7.0V
- CANH, CANL, SPLIT Absolute Maximum Rating: -27V to +40V

Package

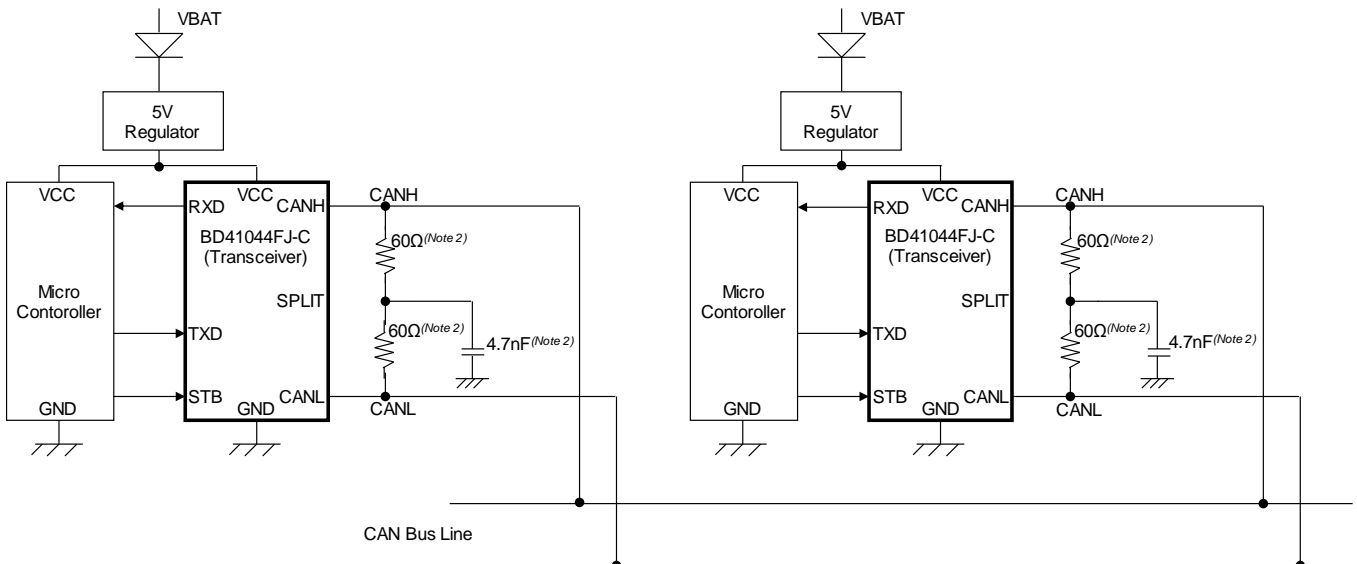
SOP-J8

W(Typ) x D(Typ) x H(Max)

4.90mm x 6.00mm x 1.65mm



Typical Application Circuit



(Note 2) Resistor value, capacitor value and connection about SPLIT should be selected by ECU specification. Capacitor value should be selected between 1nF to 100nF.

Figure 1. Typical Application Circuit

Pin Configuration

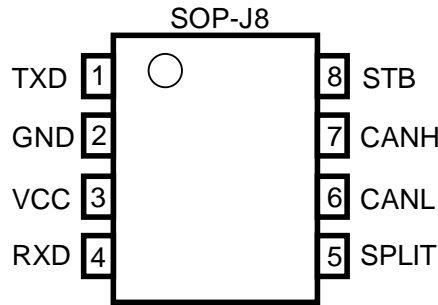


Figure 2. Pin Configuration(TOP VIEW)

Pin Descriptions

Table 1. Pin Description

Pin No.	Pin Name	Function
1	TXD	Transmission data input pin with pull-up resistance.
2	GND	Ground
3	VCC	Power supply
4	RXD	Receive data output
5	SPLIT	Common-mode stabilization output
6	CANL	LOW-level CAN bus line
7	CANH	HIGH-level CAN bus line
8	STB	Mode control input with pull-up resistance. HIGH : Standby mode LOW : Normal mode.

Block Diagram

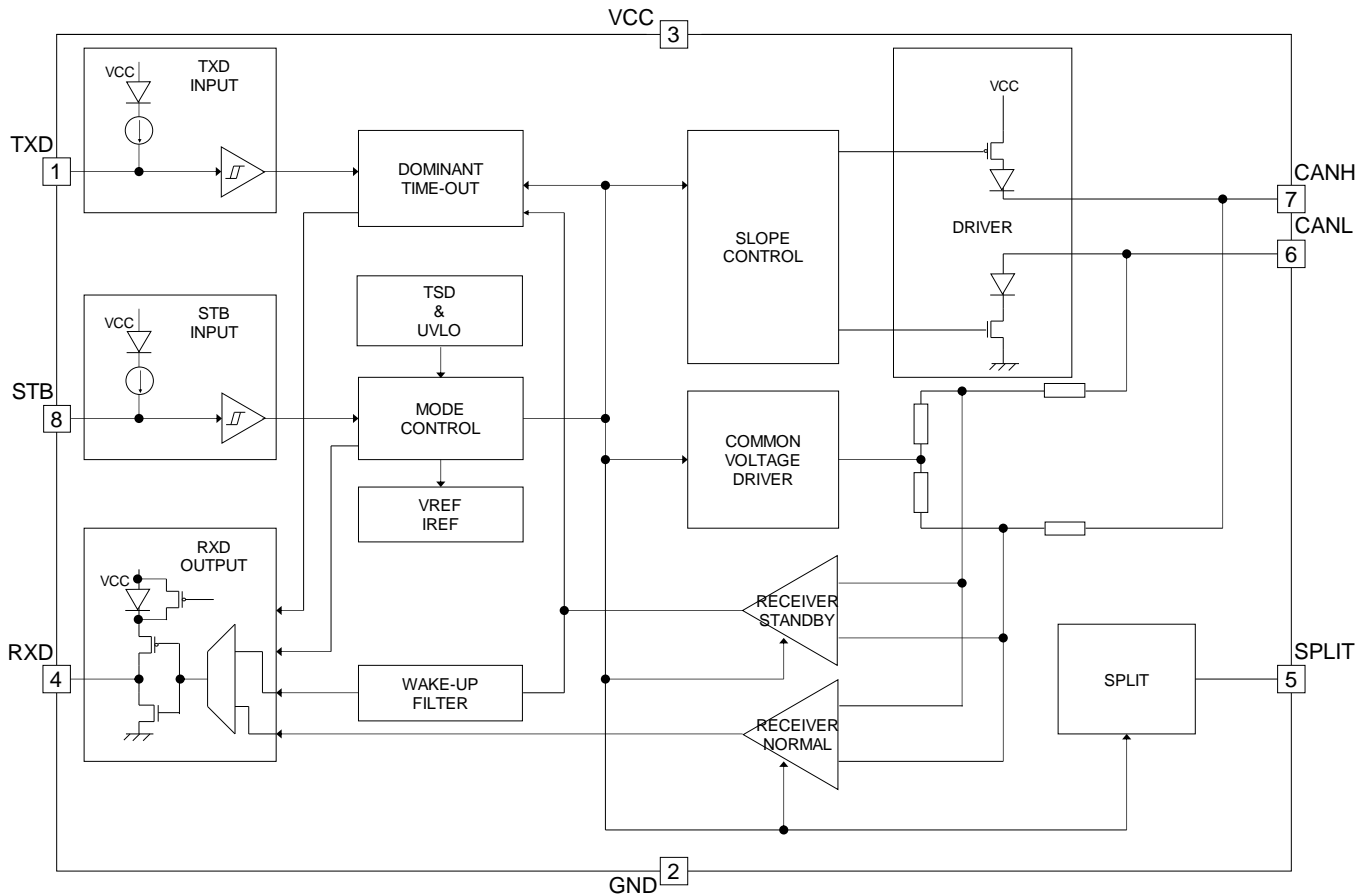


Figure 3. Block Diagram

Mode of Operation

BD41044FJ-C operates on Power-OFF mode, Standby mode or Normal mode depending on the logic state of STB pin and voltage of VCC (see Figure 4 for the state transition of each mode of operation)

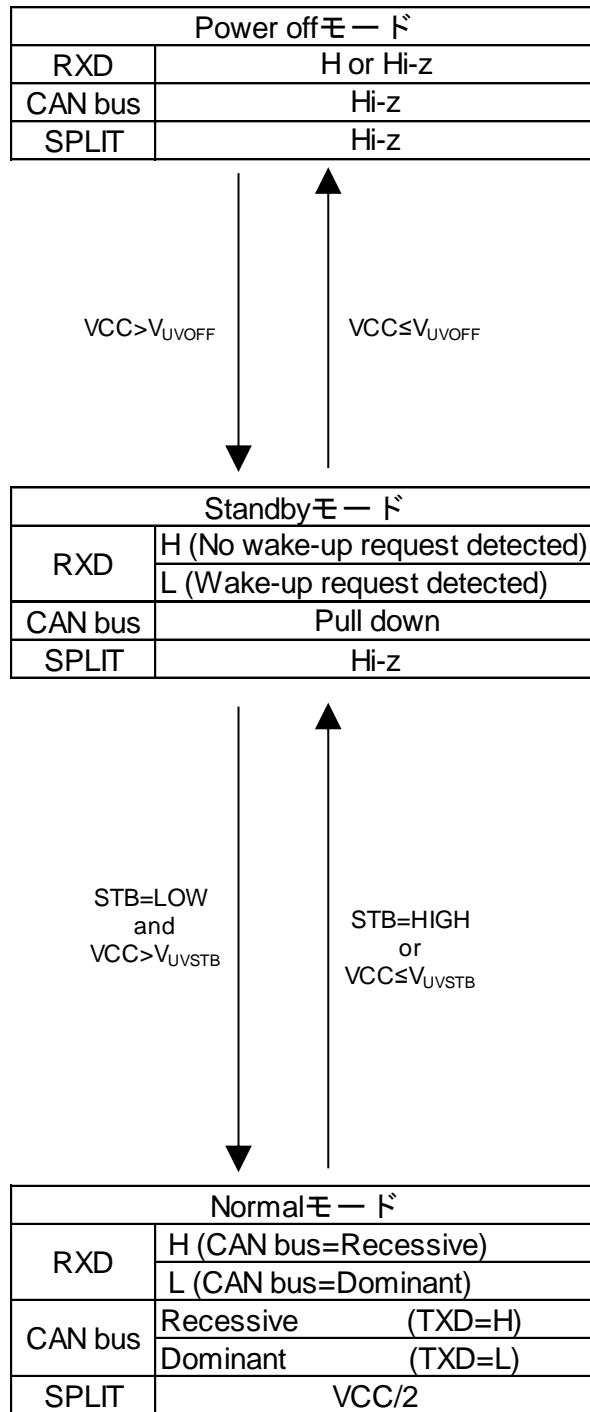


Figure 4. State Transition Chart

A diode is inserted on the RXD pin at the VCC side to prevent the reverse current to VCC. But a diode becomes invalid in Normal mode.

When it changed to Normal mode by STB=LOW while TXD=LOW, Dominant output to CAN bus is stopped. After TXD=HIGH once and then TXD=LOW again, Dominant output to CAN bus is started.

Mode of Operation – continued**1. Power-OFF Mode**

The Power OFF mode is the state in which the transceiver function is turned off due to an abnormal drop in VCC. In this mode, the IC cannot receive the Wake-up signal from CAN bus.

2. Standby Mode

The Standby Mode is the state in which electric power is saved by turning off all circuits except those with Receiver Standby, Wake up Filter and Dominate Time-out functions. RXD will output the wake up signal from CAN bus.

3. Normal Mode

The Normal mode is the state in which the transceiver is available for normal CAN communication. It transmits and receives data via the bus lines CANH and CANL. In this mode, TXD can transmit data to the CAN bus and RXD can receive data from the CAN bus. In addition, SPLIT outputs the voltage of $VCC/2$.

Absolute Maximum Ratings

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply Voltage	V _{CC}	-0.3 to +7.0	V
Input Voltage	V _{STB} , V _{TXD}	-0.3 to +7.0	V
Output Voltage	V _{RXD}	-0.3 to +7.0	V
Input/Output Voltage	V _{CANH} , V _{CANL} , V _{SPLIT}	-27 to +40	V
Differential Voltage between CANH and CANL	V _{DIFF}	-5.0 to +10.0	V
Junction Max Temperature	T _{jmax}	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C

Caution 1: Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.

Caution 2: Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with thermal resistance taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.

Thermal Resistance^(Note 3)

Table 3. Thermal Resistance

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 5)	2s2p ^(Note 6)	
SOP-J8				
Junction to Ambient	θ_{JA}	149.3	76.9	°C/W
Junction to Top Characterization Parameter ^(Note 4)	Ψ_{JT}	18	11	°C/W

(Note 3) Based on JESD51-2A(Still-Air)

(Note 4) The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 5) Using a PCB board based on JESD51-3(Table 4).

(Note 6) Using a PCB board based on JESD51-7(Table 5).

Table 4. 1 Layer Board

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt
Top		
Copper Pattern	Thickness	
Footprints and Traces	70μm	

Table 5. 4 Layers Board

Layer Number of Measurement Board	Material	Board Size			
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt			
Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70μm	74.2mm x 74.2mm	35μm	74.2mm x 74.2mm	70μm

Recommended Operating Conditions

Table 6. Recommended Operating Ranges

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Supply Voltage Range	V _{CC}	4.75	5.00	5.25	V	
Operating Temperature Range	Topr	-40	+25	+125	°C	
Capacitance of Pin SPLIT ^(Note 7)	C _{SPLIT}	1.0	4.7	100.0	nF	

(Note 7) Set the capacity of the condenser not to surpass a range of the value of standard in consideration of temperature characteristics and dc-bias properties.

Electrical Characteristics

The following specifications are $4.75V \leq V_{CC} \leq 5.25V$, conditions of $-40^{\circ}C \leq T_{opr} \leq 125^{\circ}C$
 The Typ level is $V_{CC}=5V$, $T_{opr}=25^{\circ}C$ unless otherwise specified.

Table 7. Electrical Characteristics (VCC)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Operating Current 1	I _{CCSTB}	-	10	15	μA	Standby mode; STB=HIGH
Operating Current 2	I _{CCREC}	-	5.0	7.5	mA	Normal mode, Recessive; STB=LOW TXD=HIGH R _{LOAD} =60Ω
Operating Current 3	I _{CCDOM}	-	45	65	mA	Normal mode, Dominant; STB=LOW TXD=LOW R _{LOAD} =60Ω
Under Voltage Detection Voltage 1	V _{UVSTB}	3.50	-	4.75	V	
Under Voltage Detection Voltage 2	V _{UVOFF}	1.30	-	2.95	V	

Table 8. Electrical Characteristics (STB)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
HIGH Level Input Voltage	V _{IH_STB}	0.7 x V _{CC}	-	V _{CC}	V	
LOW Level Input Voltage	V _{IL_STB}	0.0	-	+0.3 x V _{CC}	V	
HIGH Level Input Current	I _{IH_STB}	-1	-	+1	μA	V _{STB} =V _{CC}
LOW Level Input Current	I _{IL_STB}	-15	-	-1	μA	V _{STB} =0V

Table 9. Electrical Characteristics (TXD)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
HIGH Level Input Voltage	V _{IH_TXD}	0.7 x V _{CC}	-	V _{CC}	V	
LOW Level Input Voltage	V _{IL_TXD}	0.0	-	+0.3 x V _{CC}	V	
HIGH Level Input Current	I _{IH_TXD}	-5	-	+5	μA	V _{TXD} =V _{CC}
LOW Level Input Current	I _{IL_TXD}	-260	-150	-30	μA	V _{TXD} =0V

Table 10. Electrical Characteristics (RXD)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Normal Mode Time Output HIGH Current	I _{OH_RXD}	-8	-	-1	mA	V _{RXD} =V _{CC} -0.4V
Normal Mode Time Output LOW Current	I _{OL_RXD}	1	-	12	mA	V _{RXD} =0.4V

Electrical Characteristics – continued

Table 11. Electrical Characteristics (SPLIT)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Output Voltage 1	V _{ILN_SPLIT}	0.3 x V _{CC}	-	0.7 x V _{CC}	V	I _{LOAD} =-500μA
Output Voltage 2	V _{ILP_SPLIT}	0.3 x V _{CC}	-	0.7 x V _{CC}	V	I _{LOAD} =500μA
Output Voltage 3	V _{RL_SPLIT}	0.45 x V _{CC}	-	0.55 x V _{CC}	V	R _{LOAD} =1MΩ
Leakage Current 1	I _{IL_SPLIT}	-5	-	+5	μA	V _{SPLIT} =-27V
Leakage Current 2	I _{IH_SPLIT}	-5	-	+5	μA	V _{SPLIT} =40V

Electrical Characteristics – continued

Table 12. Electrical Characteristics (CANH, CANL)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Common Voltage Range	V_{CM_CAN}	-12.0	+2.5	+12.0	V	
CANH Dominant Output Voltage	V_{DOM_CANH}	2.75	3.50	4.50	V	$R_{LOAD} = 50\Omega$ to 65Ω
CANL Dominant Output Voltage	V_{DOM_CANL}	0.50	1.50	2.25	V	$R_{LOAD} = 50\Omega$ to 65Ω
CANH–CANL Dominant Output Voltage	V_{DOM_DIFF}	1.5	-	3.0	V	$R_{LOAD} = 50\Omega$ to 65Ω
CANH–CANL Dominant Output Voltage2	V_{DOM_DIFF2}	1.5	-	5.0	V	$R_{LOAD} = 2240\Omega$
CANH+CANL Output Waveform Symmetry	V_{AC_SYM}	$0.9 \times V_{CC}$	-	$1.1 \times V_{CC}$	V	$R_{LOAD} = 60\Omega$ $C_{SPLIT} = 4.7nF$ $f_{TXD} = 250kHz, 1.0MHz$
CANH+CANL–VCC Dominant Output Voltage	V_{DOM_SYM}	-400	-	+400	mV	$R_{LOAD}=60\Omega$
CANH Recessive Output Voltage	V_{REC_CANH}	2.0	$0.5 \times V_{CC}$	3.0	V	no Load
CANL Recessive Output Voltage	V_{REC_CANL}	2.0	$0.5 \times V_{CC}$	3.0	V	no Load
CANH–CANL Recessive Output Voltage 1	V_{REC_DIFF1}	-50	-	+50	mV	no Load
CANH–CANL Recessive Output Voltage 2	V_{REC_DIFF2}	-120	-	+12	mV	$R_{LOAD}=60\Omega$
CANH Dominant Output Current	I_{DOM_CANH}	-100	-	-	mA	$V_{CANH}=-3V$
CANL Dominant Output Current	I_{DOM_CANL}	-	-	100	mA	$V_{CANL}=18V$
CANH Recessive Output Current	I_{REC_CANH}	-5	-	+5	mA	$V_{CANH}=-27V$ to $+40V$
CANL Recessive Output Current	I_{REC_CANL}	-5	-	+5	mA	$V_{CANL}=-27V$ to $+40V$
CANH Standby Output Voltage	V_{STB_CANH}	-0.1	-	+0.1	V	no Load
CANL Standby Output Voltage	V_{STB_CANL}	-0.1	-	+0.1	V	no Load
CANH–CANL Stanby Differential Output Voltage	V_{DIFF_STB}	-0.2	-	+0.2	V	no load
CANH Leakage Current	I_{OFF_CANH}	-3	-	+3	μA	$V_{CC}=0V$ $V_{CANH}=5V$
CANL Leakage Current	I_{OFF_CANL}	-3	-	+3	μA	$V_{CC}=0V$ $V_{CANL}=5V$
CANH Input Impedance	R_{I_CANH}	6	15	28	k Ω	$-2.0V \leq V_{CANH} \leq +7.0V$
CANL Input Impedance	R_{I_CANL}	6	15	28	k Ω	$-2.0V \leq V_{CANL} \leq +7.0V$
CANH, CANL Input Impedance Offset	R_{I_OFFSET}	-3	-	+3	%	$V_{CANH}=+5.0V, V_{CANL}=+5.0V$
CANH, CANL Differential Input Impedance	R_{I_DIFF}	12	30	52	k Ω	$-2.0V \leq V_{CANH} \leq +7.0V$ $-2.0V \leq V_{CANL} \leq +7.0V$
Differential Input Voltage Range “Recessive” (Normal Mode)	$V_{RX_NRM_R}$	-3.0	-	+0.5	V	$-12.0V \leq V_{CANH} \leq +12.0V$ $-12.0V \leq V_{CANL} \leq +12.0V$
Differential Input Voltage Range “Dominant” (Normal Mode)	$V_{RX_NRM_D}$	0.9	-	8.0	V	$-12.0V \leq V_{CANH} \leq +12.0V$ $-12.0V \leq V_{CANL} \leq +12.0V$
Normal Mode Receiver Detection Voltage Hysteresis	$V_{RX_NRM_HYS}$	100	-	300	mV	$-12.0V \leq V_{CANH} \leq +12.0V$ $-12.0V \leq V_{CANL} \leq +12.0V$
Differential Input Voltage Range “Recessive” (Standby Mode)	$V_{RX_STB_R}$	-3.0	-	+0.4	V	$-12.0V \leq V_{CANH} \leq +12.0V$ $-12.0V \leq V_{CANL} \leq +12.0V$
Differential Input Voltage Range “Dominant” (Standby Mode)	$V_{RX_STB_D}$	1.15	-	8.00	V	$-12.0V \leq V_{CANH} \leq +12.0V$ $-12.0V \leq V_{CANL} \leq +12.0V$

Electrical Characteristics – continued

Table 13. Electrical Characteristics (Timing)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Delay Time from TXD to Bus Dominant	t _{TXD_DOM}	-	-	140	ns	R _{LOAD} =60Ω C _{LOAD} =100pF
Delay Time from TXD to Bus Recessive	t _{TXD_REC}	-	-	140	ns	R _{LOAD} =60Ω C _{LOAD} =100pF
Delay Time from Bus Dominant to RXD	t _{DOM_RXD}	-	-	140	ns	C _{RXD} =15pF
Delay Time from Bus Recessive to RXD	t _{REC_RXD}	-	-	140	ns	C _{RXD} =15pF
Propagation Delay from TXD to RXD Fall	t _{TXD_RXD_F}	60	-	220	ns	R _{LOAD} =60Ω C _{LOAD} =100pF
Propagation Delay from TXD to RXD Rise	t _{TXD_RXD_R}	60	-	220	ns	R _{LOAD} =60Ω C _{LOAD} =100pF
Transmitted Recessive Bit Width1	t _{bit_BUS2}	435	-	530	ns	f _{TXD} =1.0MHz R _{LOAD} =60Ω C _{LOAD} =100pF C _{RXD} =15pF
Transmitted Recessive Bit Width2	t _{bit_BUS5}	155	-	210	ns	f _{TXD} =2.5MHz R _{LOAD} =60Ω C _{LOAD} =100pF C _{RXD} =15pF
Bit Time on Pin RXD1	t _{bit_RXD2}	400	-	550	ns	f _{TXD} =1.0MHz R _{LOAD} =60Ω C _{LOAD} =100pF C _{RXD} =15pF
Bit Time on Pin RXD2	t _{bit_RXD5}	120	-	220	ns	f _{TXD} =2.5MHz R _{LOAD} =60Ω C _{LOAD} =100pF C _{RXD} =15pF
Receiver Timing Symmetry1	Δt _{rec2}	-65	-	+40	ns	f _{TXD} =1.0MHz R _{LOAD} =60Ω C _{LOAD} =100pF C _{RXD} =15pF
Receiver Timing Symmetry2	Δt _{rec5}	-45	-	+15	ns	f _{TXD} =2.5MHz R _{LOAD} =60Ω C _{LOAD} =100pF C _{RXD} =15pF
Bus Wake-up Time	t _{BUS_WK}	0.5	-	5.0	μs	V _{RX_STB_D} =1.15V to 5.00V
Standby to Normal Mode	t _{STB_NRM}	7	-	47	μs	
TXD Dominant Time-out	t _{DOM_TON}	0.8	-	10.0	ms	In Normal Mode
Bus Dominant Time-out	t _{DOM_TOS}	0.8	-	10.0	ms	In Standby Mode

Timing Chart

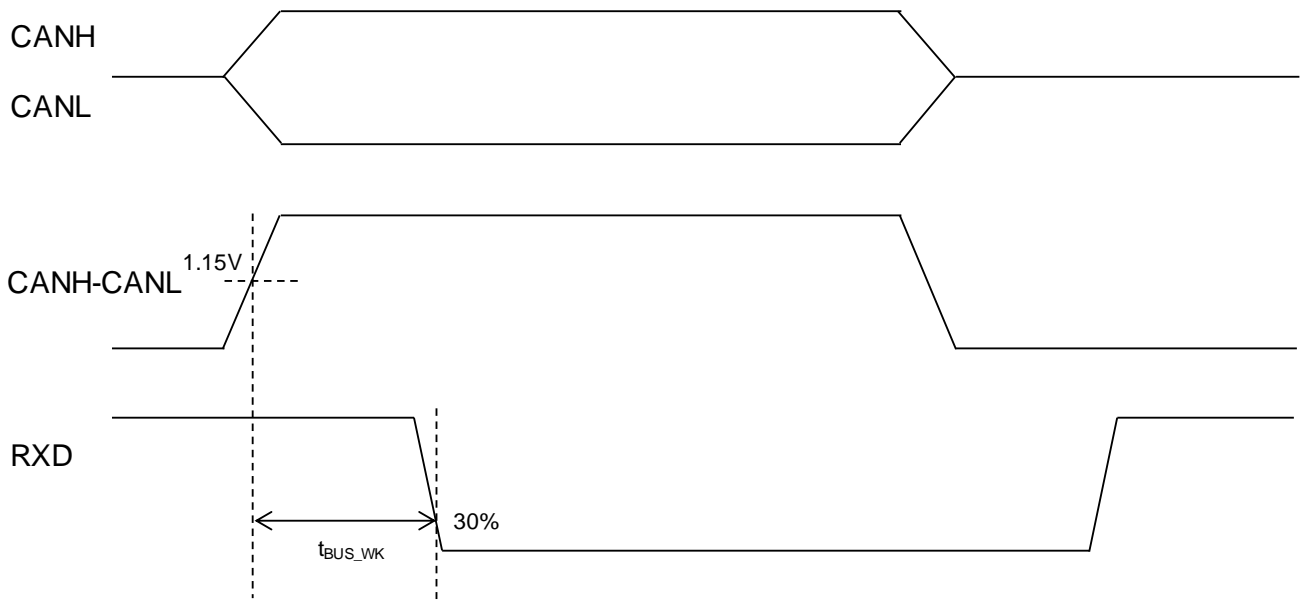


Figure 5. Standby Mode Function

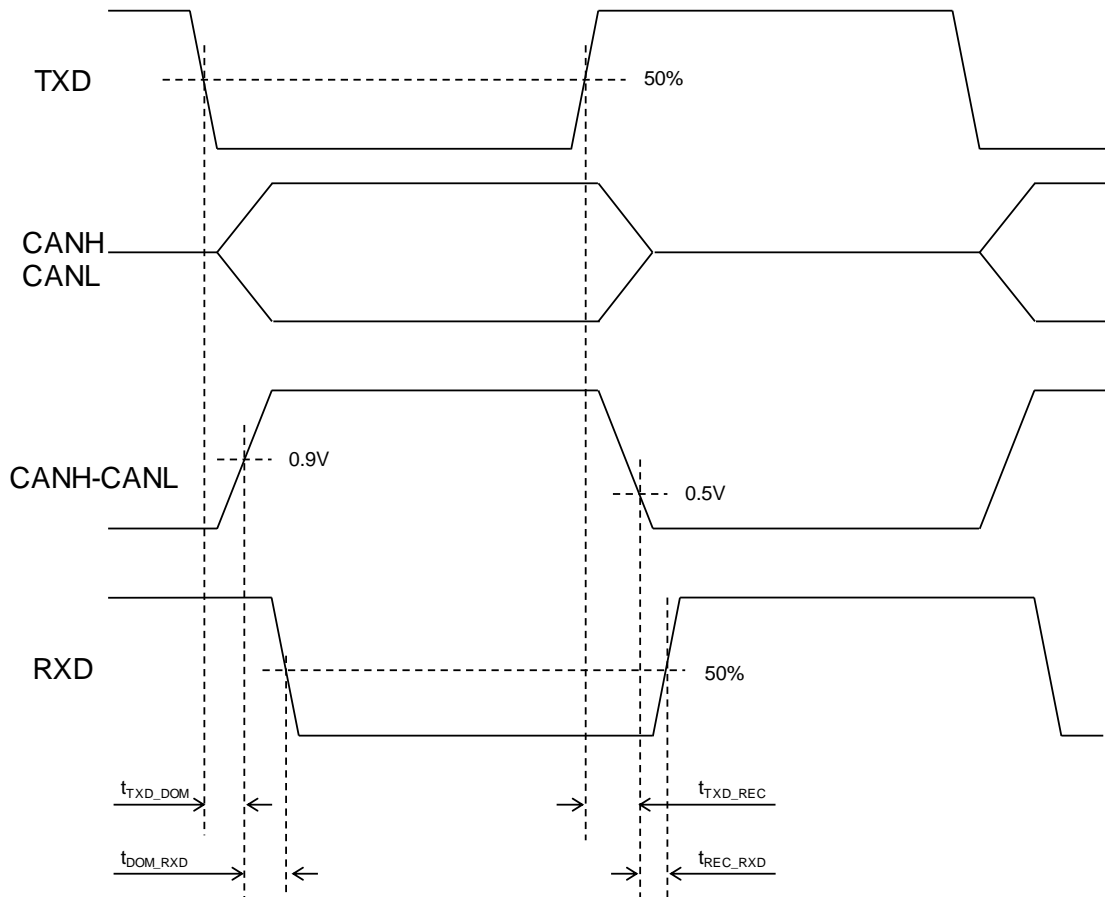


Figure 6. Normal Mode Function

Timing Chart – continued

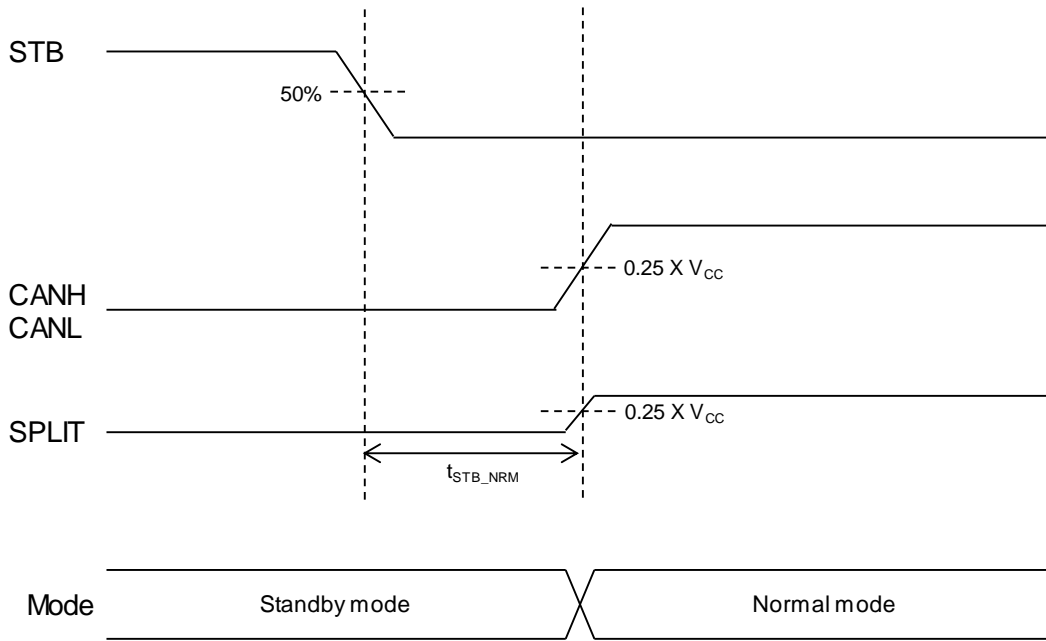
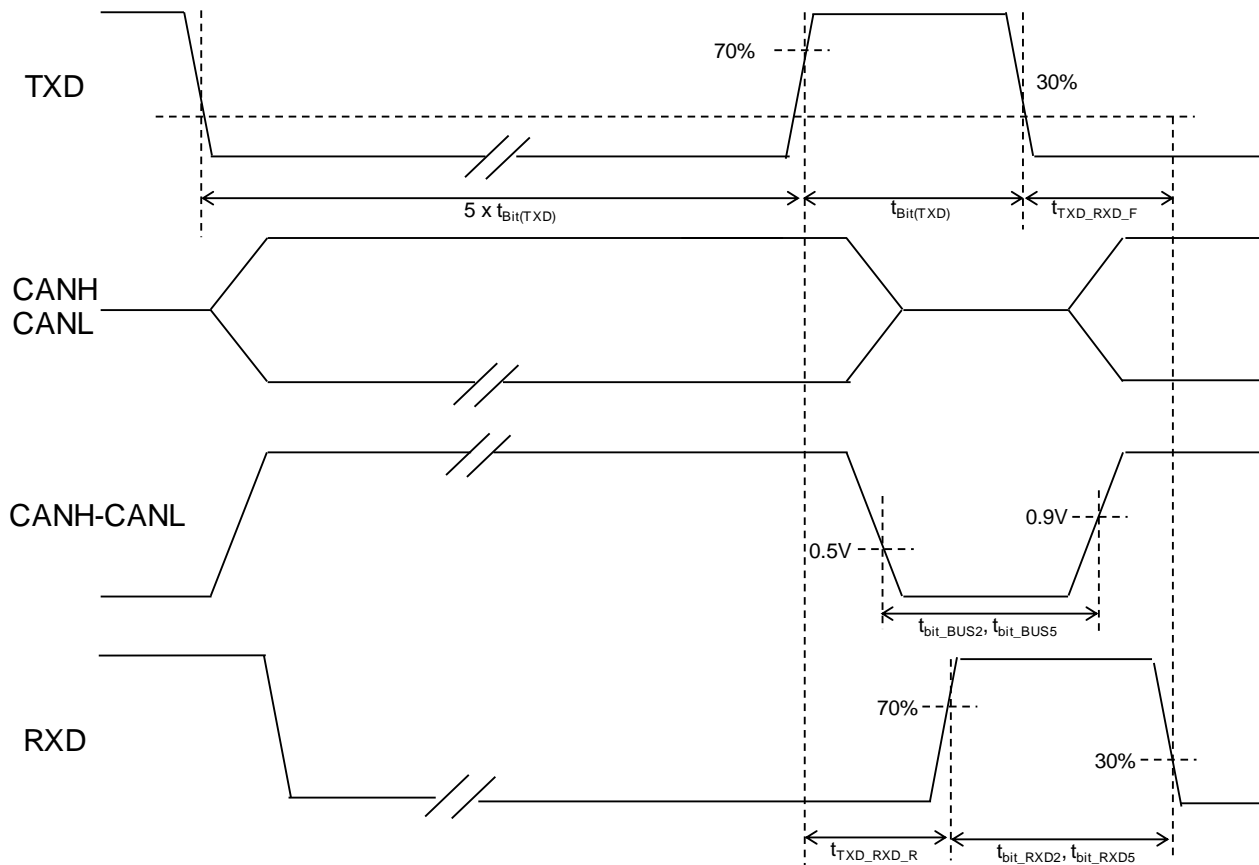


Figure 7. Transition from Standby Mode to Normal Mode



According to ISO11898-2:2016.

Figure 8. CAN FD Normal Mode Operating

Fail Safe Function

1. Thermal Shut Down

Thermal shut down is a function to automatically stop output to the CAN bus during an abnormal heat generation overrun. When the junction temperature of the IC becomes higher than a sensed temperature (Typ 170°C), CAN bus changes to the Recessive state. When the junction temperature of the IC is less than the detection release temperature(Typ 155°C), the thermal shut down function is cancelled by setting TXD HIGH.

Attention: The sensed temperature reaches 150°C to 190°C, and the hysteresis temperature is 5°C to 30 °C. The sensed temperature/hysteresis temperature is not inspected for shipped samples. In addition, please avoid system designs that operate near the absolute maximum ratings as the temperature protective circuits activate when the limits are exceeded.

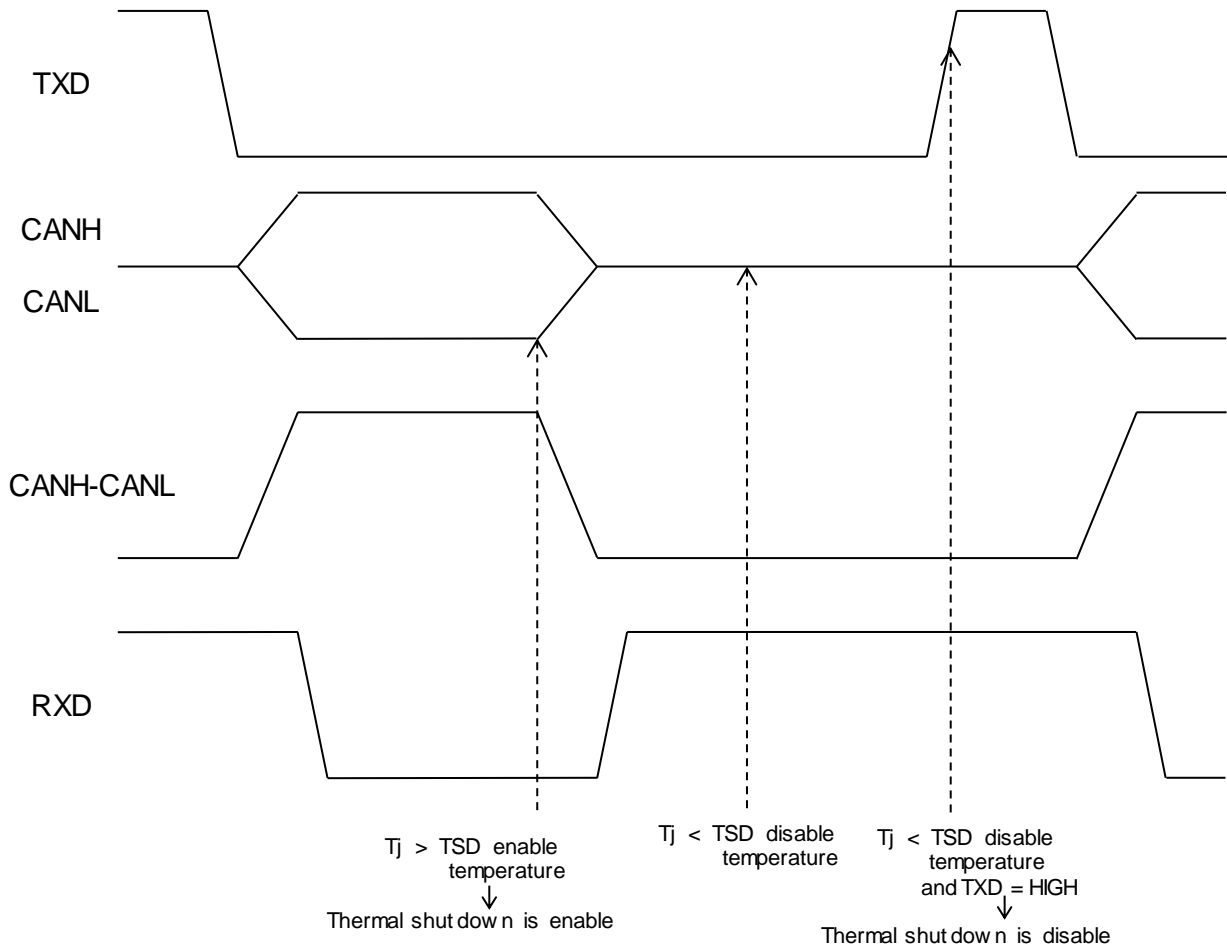


Figure 9. Thermal Shutdown Operating

Fail Safe Function – continued

2. TXD Dominant Time-out

TXD dominant time-out is a function to automatically stop the output to CAN bus when TXD is set LOW during Normal mode. If TXD dominant time-out is enabled, CAN bus changes to the Recessive state. The TXD dominant time-out is released by setting TXD to HIGH.

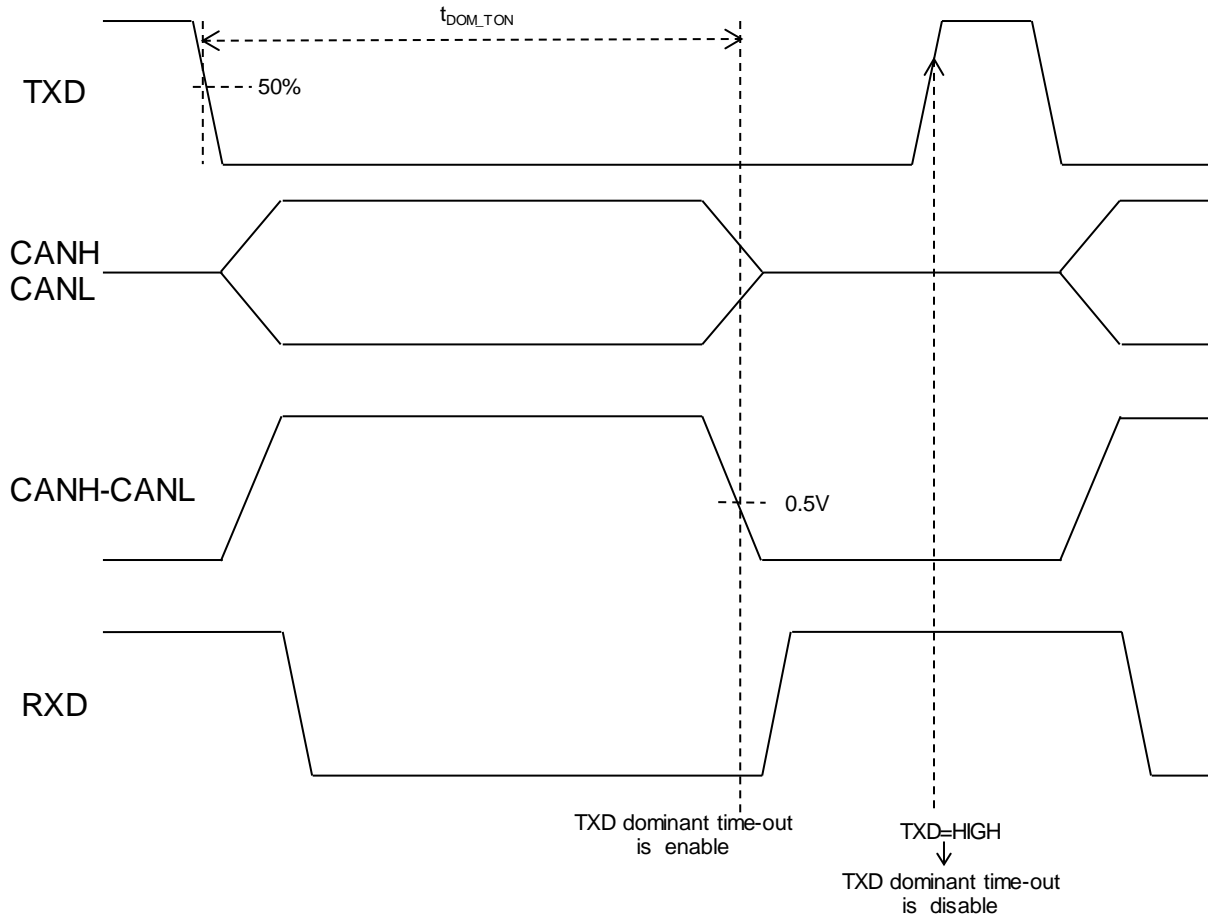


Figure 10. TXD Dominant Time-out Operating

Fail Safe Function – continued

3. CAN Bus Dominant Time-out

CAN Bus Dominant Time-out is a function to automatically stop the LOW output to RXD when CAN bus is set to Dominant during Standby Mode. If CAN bus dominant time-out is enabled, RXD becomes HIGH. The CAN bus dominant time-out is released by setting the CAN bus to Recessive.

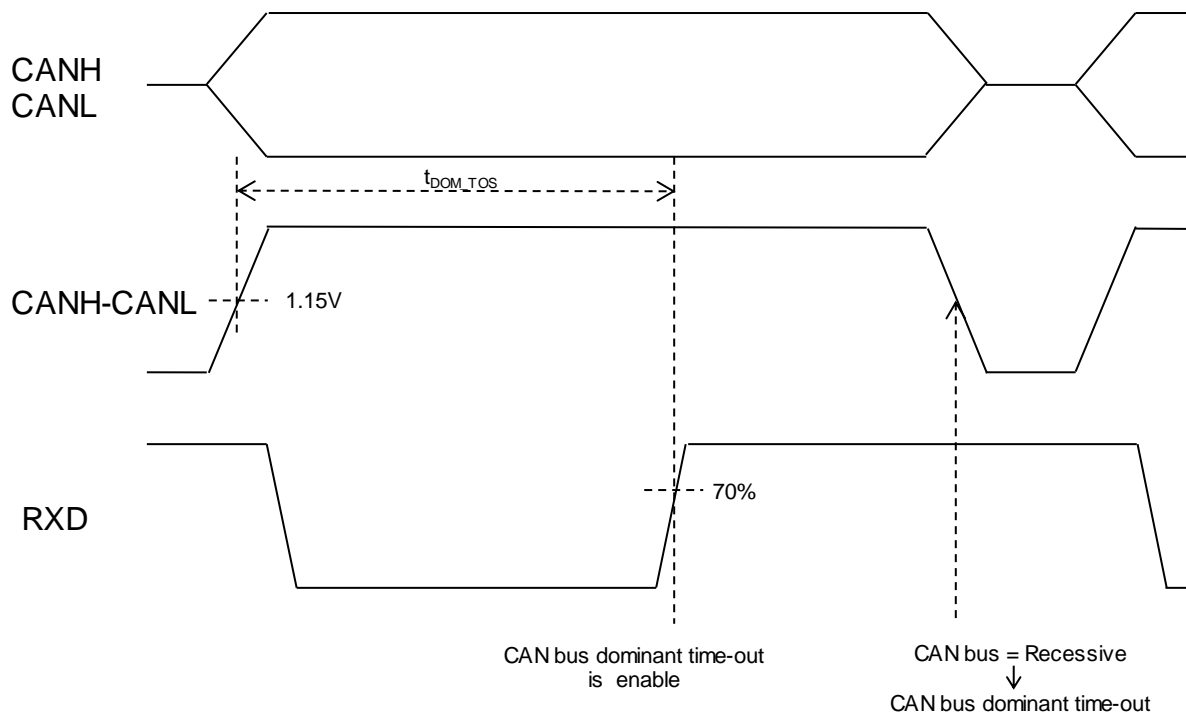
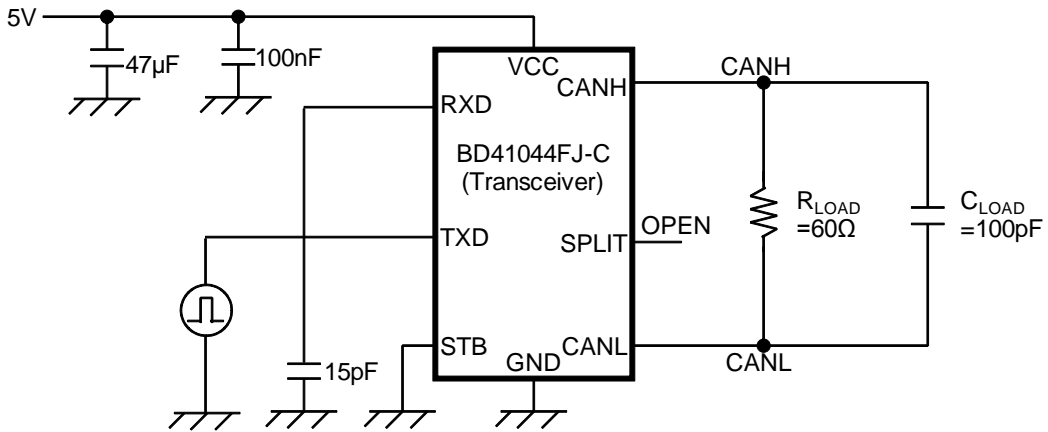


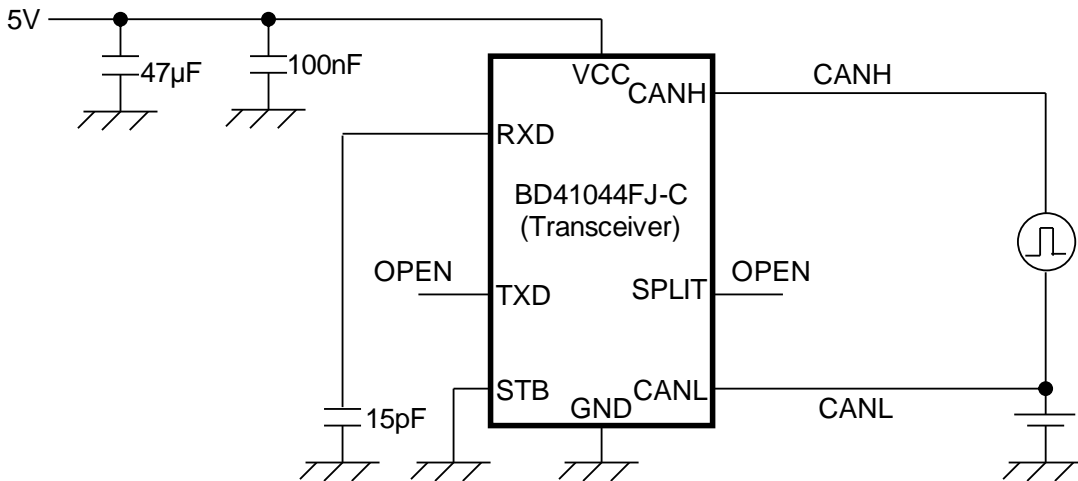
Figure 11. RXD Dominant Time-out Operating

Evaluation Circuit Diagram

1. t_{TXD_DOM} , t_{TXD_REC} , $t_{TXD_RXD_F}$, $t_{TXD_RXD_R}$, t_{bit_BUS2} , t_{bit_BUS5} , t_{bit_RXD2} , t_{bit_RXD5} , Δt_{rec2} , Δt_{rec5}



2. t_{DOM_RXD} , t_{REC_RXD}



3. V_{AC_SYM}

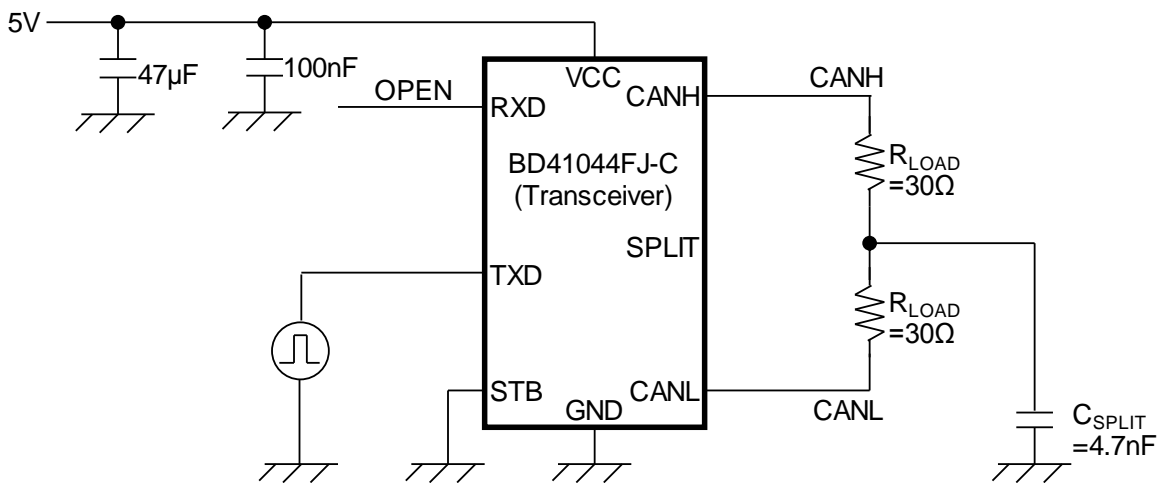


Figure 12. Evaluation Circuit Diagram

I/O Equivalent Circuits

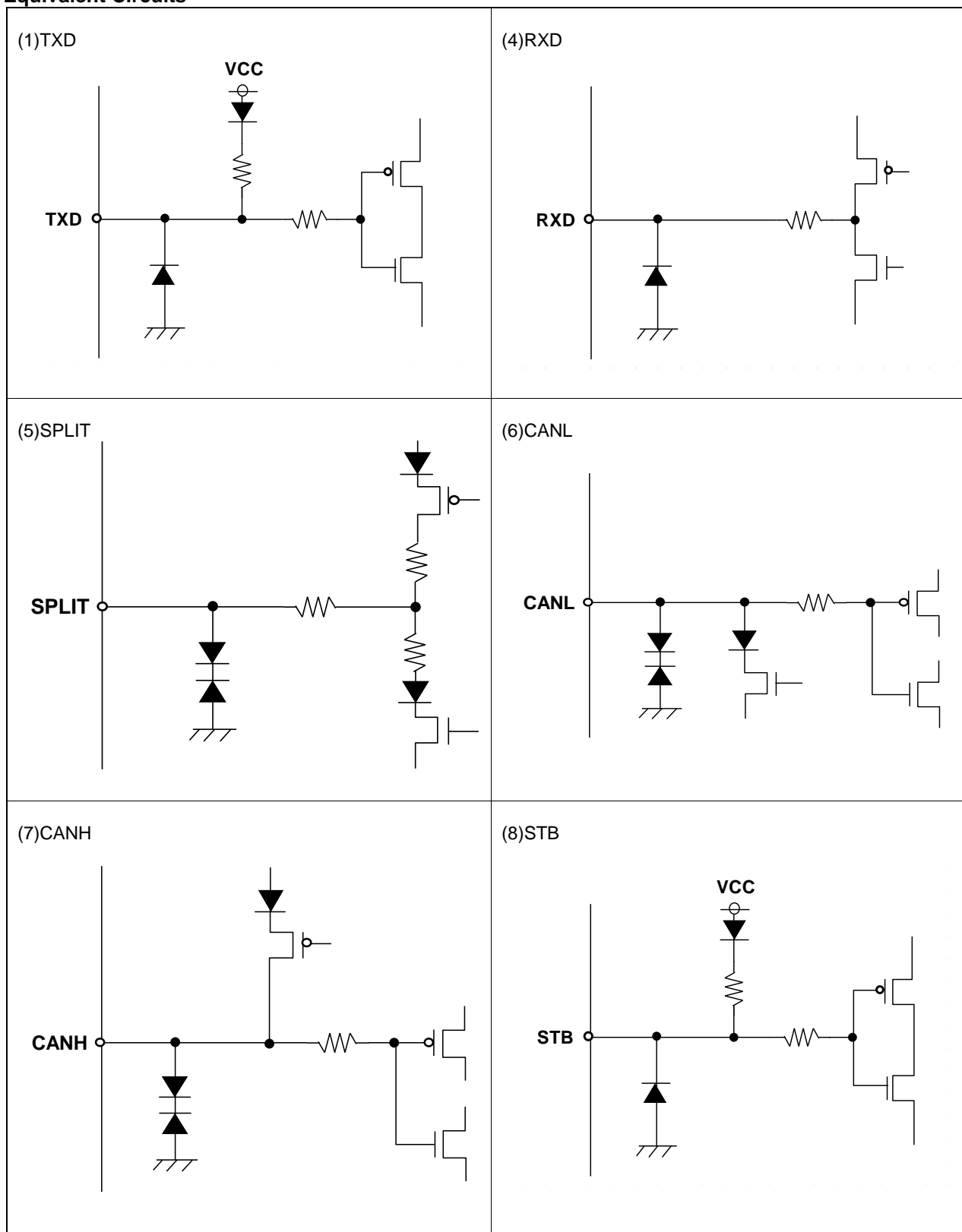


Figure 13. I/O Equivalent Circuits

Operational Notes**1. Reverse Connection of Power Supply**

Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines

Design the PCB layout pattern to provide low impedance supply lines. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage

Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern

When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions

The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current

When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Operation Under Strong Electromagnetic Field

Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. Testing on Application Boards

When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. Inter-pin Short and Mounting Errors

Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. Unused Input Pins

Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When $GND > Pin A$ and $GND > Pin B$, the P-N junction operates as a parasitic diode.
 When $GND > Pin B$, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

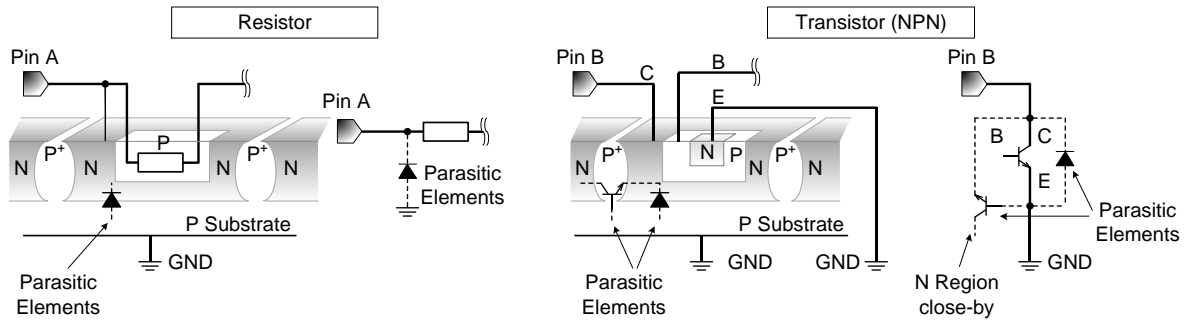


Figure 14. Example of monolithic IC structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine a capacitance value considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Area of Safe Operation (ASO)

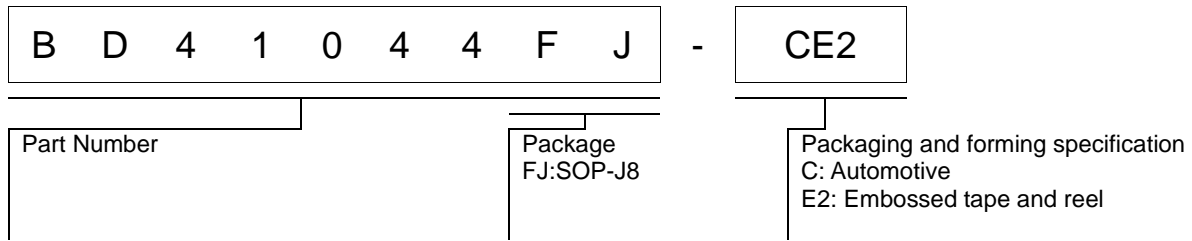
Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

14. Thermal Shutdown Circuit(TSD)

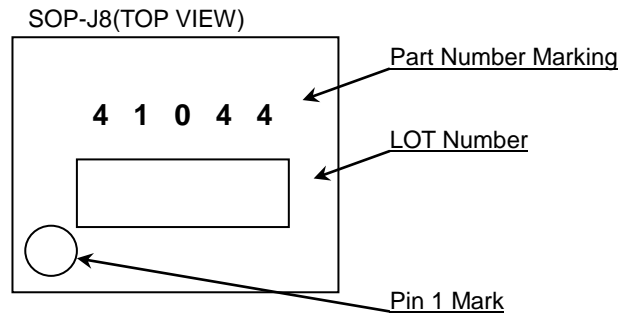
This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (T_j) will rise which will activate the TSD circuit that will turn OFF power output pins. When the T_j falls below the TSD threshold, the circuits are automatically restored to normal operation.

Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

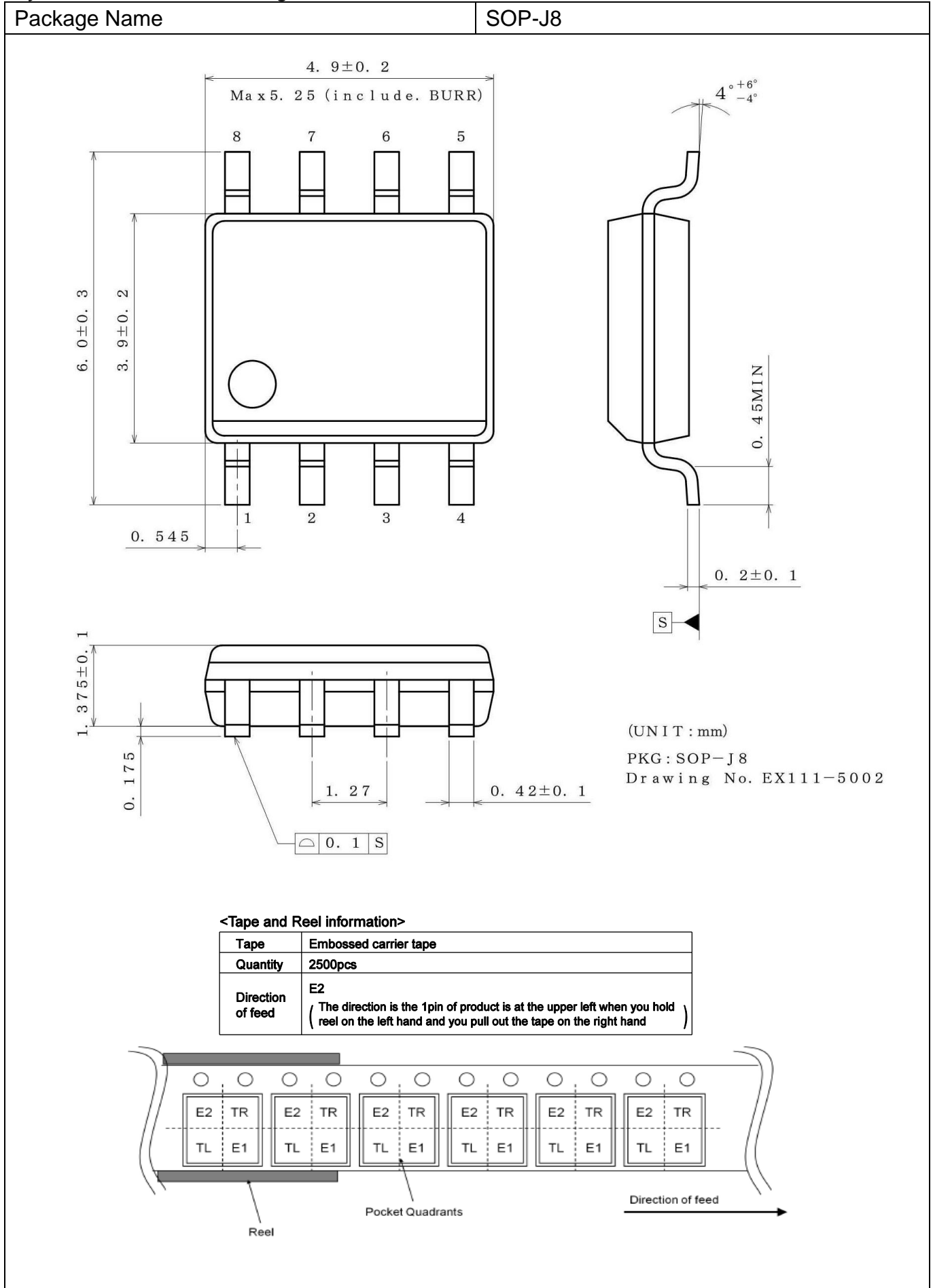
Ordering Information



Marking Diagram



Physical Dimension and Packing Information



Revision History

Date	Revision	Changes
15.Feb.2018	001	New Release
27.Dec.2018	002	<p>P1 Typical Application Circuit Added explanation of resistor valude, capacitor value, connection about SPLIT.</p> <p>P2 Block Diagram Deleated "STB" in RXD OUTPUT block.</p> <p>P3 Mode of Operation Modified to "H or Hi-Z" from "Hi-Z" at RXD in Power off mode. Modified to "STB=LOW and VCC>V_{UVSTB}" from "STB=LOW and TXD=HIGH and VCC>V_{UVSTB}" at the conditions to change to Normal mode from Standby mode. Added explanation of a diode at the RXD pin. Added explanation of the operation when it changed to the Normal mode by STB=LOW while TXD=LOW.</p> <p>P7 Table 8. Electrical Characteristics (STB) HIGH Level Input Voltage Modified the max value to "V_{CC}" from "V_{CC}+0.3". LOW Level Input Voltage Modified the min value to "0.0" from "-0.3".</p> <p>P7 Table 9. Electrical Characteristics (TXD) HIGH Level Input Voltage Modified the max value to "V_{CC}" from "V_{CC}+0.3". LOW Level Input Voltage Modified the min value to "0.0" from "-0.3".</p> <p>P11 Figure 6 Deleted "t_{TXD_RXD_F}" and "t_{TXD_RXD_R}". Modified the RXD threshold value to "50%".</p> <p>P12 Figure 7 Modified to "0.25 x V_{CC}" from "0.5 x V_{CC}".</p> <p>P12 Figure 8 Modified format.</p> <p>P16 Application Example Deleted</p>

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CLASS IV		CLASS III	

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