Wireless Power Consortium / Qi Compliant series

Wireless Power Receiver IC

BD57011AGWL

General Description

BD57011AGWL is stand-alone integrated IC for wireless power receiver. The device is composed fully synchronous rectifier circuit in low-impedance FETs, Qi compliant packet controller, Adjustable low-dropout, and open-drain output terminal to communicate the power transmitter by amplitude modulation.
BD57011AGWL applies to 5W-power mobile application based on WPC ver. 1.2.

Features

- Low Impedance FET in Rectifier
- High Efficiency Fully Synchronous Rectifier
- Maximum Input Voltage is 20V
- WPC / Qi ver1.2 BPP(Baseline Power Profile) Support
- Adjustable Voltage at Low-dropout(16steps)
- Open-Drain Output Terminal for Modulation
- TX-RX Coil Position Gap Alarm

Applications

WPC compliant Device

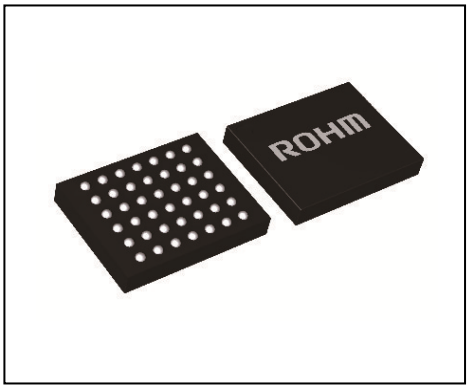
- Smart Phones
- Cell Phones
- Hand-held Mobile Devices

Key Specifications

- Variable Output Voltage: 4.3V to 5.3V(16steps)
- Maximum Input Voltage: 20V(Max)
- Maximum Input/Output Current: 1.1A(Max)
- AC Input Frequency: 100kHz to 210kHz
- Operating Temperature Range: -30°C to +85°C

Package

	W(Typ) x D(Typ) x H(Max)
UCSP50L3C (42Pin)	3.36mmx2.62mmx0.57mm (0.4mm pitch)



Typical Application Circuit

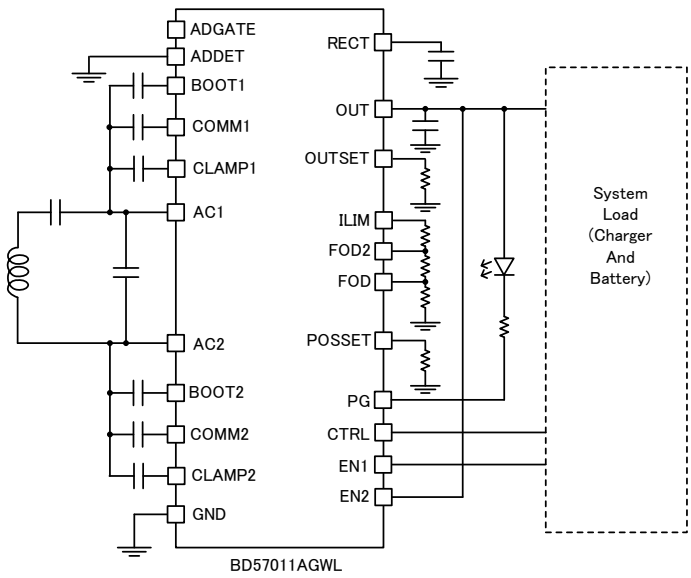


Figure 1. Typical application circuit

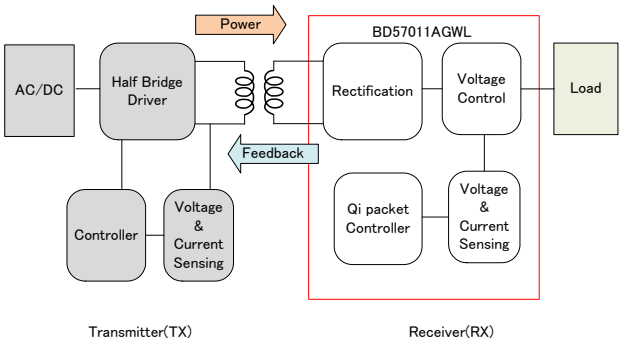


Figure 2. Product position in Wireless Power Supply System

○Product structure : Silicon monolithic integrated circuit ○This product has no designed protection against radioactive rays

Absolute Maximum Ratings (Ta=25°C)

Parameter	Symbol	Limit	Unit
RECT, AC1, AC2, COMM1, COMM2, CLAMP1, CLAMP2 Voltage	V_{INOUT_H}	-0.3 to +20	V
BOOT1, BOOT2 Voltage	V_{INOUT_H2}	-0.3 to +26	V
BOOT1 to AC1, BOOT2 to AC2 Voltage	V_{BOOT_AC}	-0.3 to +7	V
ADDET, ADGATE Voltage	V_{AD_MAX}	-0.3 to +28	V
OUT, OUTSET, POSSET, ILIM, CTRL, EN1, EN2, PG Voltage	V_{INOUT_L}	-0.3 to +7	V
FOD, FOD2 Voltage	V_{INOUT_L2}	-0.3 to +3.6	V
Input/Output Rating Current	I_{MAX}	1.5*(Note 1)*	A
PG pin Rating Current	I_{MAX_PG}	15	mA
Storage Temperature Range	Tstg	-55 to +150	°C
Power Dissipation	Pd	1.38*(Note 2)*	W

(Note 1) Applied to AC1, AC2, RECT and GND with the proviso that all multi-pin should connect to common pattern.
(Note 2) Derate by 11mW/°C when operating above Ta=25°C (when mounted in ROHM's standard board).

Caution 1: *Operating the IC over the absolute maximum ratings may damage the IC. The damage can either be a short circuit between pins or an open circuit between pins and the internal circuitry. Therefore, it is important to consider circuit protection measures, such as adding a fuse, in case the IC is operated over the absolute maximum ratings.*

Caution 2: *Should by any chance the maximum junction temperature rating be exceeded the rise in temperature of the chip may result in deterioration of the properties of the chip. In case of exceeding this absolute maximum rating, design a PCB boards with power dissipation taken into consideration by increasing board size and copper area so as not to exceed the maximum junction temperature rating.*

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Rectified Voltage Range	V_{RECT}	0	-	15	V
AC1, AC2 Input Peak Voltage Range	V_{AC1}, V_{AC2}	-	-	15	V
Capacitance between RECT and GND	C_{RECT}	20	-	-	µF
Operating Ambient Temperature Range	Topr	-30	-	+85	°C

Electrical Characteristics

(Unless otherwise specified, Ta=25°C, V_{RECT}=5.0V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Whole Chip						
Operating Circuit Current 1	I_{RECT1}	-	28	40	mA	V_{RECT}=5.0V, OUT off
Operating Circuit Current 2	I_{RECT2}	-	2.4	4.8	mA	V_{RECT}=5.5V, OUT on
Quiescent Current (wireless charging is disable)	I_{OUT}	-	20	40	µA	V_{OUT}=5.0V, V_{RECT}=0V
Protection Block						
RECT Under Voltage Lockout	V_{RECT_UVLO}	2.5	2.6	2.7	V	V_{RECT}:0V to 5V
Hysteresis on UVLO	$V_{RECT\_UVLO\ HYS}$	150	300	450	mV	V_{RECT}:5V to 0V
RECT Over Voltage Lockout	V_{RECT_OVLO}	14.5	15	15.5	V	V_{RECT}:10V to 18V
Hysteresis on OVLO	$V_{RECT\_OVLO\ HYS}$	60	130	260	mV	V_{RECT}:18V to 10V
OUTPUT Block						
Regulated Output Voltage	V_{OUT}	4.93	5.0	5.07	V	I_{LOAD}=100mA, R_{SET}=27kΩ
OUT Load Regulation	dV_{OUT}	-	100	200	mV	I_{LOAD}=0-500mA
PG Output Block						
Open Drain Ability on PG pin	V_{PG}	-	300	500	mV	I_{SINK}=5mA
PG pin Leak Current	I_{LEAK_PG}	-	-	2	µA	V_{PG}=7V
ILIM / FOD block						
ILIM Source Current	I_{ILIM}	9.7	10	10.3	µA	R_{ADJ}=100kΩ
Highest Value of Resistance for ILIM Setting	R_{ADJMAX}	-	-	150	kΩ	
Maximum Output Current Limit	$I_{LOADMAX}$	-	-	1.5	A	Maximum ILIM deliver within 1ms
FOD pin Leak Current	I_{LEAK_FOD}	-	-	2	µA	V_{FOD}=2V
FOD2 pin Leak Current	I_{LEAK_FOD2}	-	-	2	µA	V_{FOD2}=2V
COMM Block						
Comm1 and Comm2 ON Resistance	R_{ON_COMM}	-	2.8	4.2	Ω	
Driving Frequency on COMM Signal	f_{COMM}	1.92	2	2.08	kHz	
COMM pin Leak Current	I_{LEAK_COMM}	-	-	2	µA	V_{COMM}=20V

Electrical Characteristics – continued

(Unless otherwise specified, Ta=25°C, V_{RECT}=5.0V)

Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
CLAMP Block						
Clamp1 and Clamp2 ON Resistance	R_{ON_CLAMP}	-	3.8	5.7	Ω	
CLAMP pin Leak Current	I_{LEAK_CLAMP}	-	-	2	μA	V_{CLAMP}=20V
Adapter Detection Block						
Adapter Input Detection Threshold Voltage	V_{ADDET}	3.4	3.6	3.8	V	V_{ADDET}:0V to 5V
Adapter Input Detection Hysteresis Voltage	V_{HYS_AD}	200	400	600	mV	V_{ADDET}:5V to 0V
Adapter Input Overvoltage Detection Voltage	V_{ADDET_OV}	6.6	6.8	7.0	V	V_{ADDET}:5V to 7V
Adapter Input Overvoltage Detection Hysteresis Voltage	$V_{HYS\_AD\_OV}$	100	200	400	mV	V_{ADDET}:7V to 5V
ADDET pin Input Current	I_{ADGATE}	-	80	160	μA	V_{ADDET}=5V
EN1, EN2 and CTRL Input Block						
Input Low Threshold for EN1, EN2 and CTRL	V_{INL_EN}	-	-	0.4	V	
Input High Threshold for EN1, EN2 and CTRL	V_{INH_EN}	1.3	-	-	V	
EN1, EN2 and CTRL Pull Down Resistance	R_{EN}	100	200	400	kΩ	

Typical Performance Curves

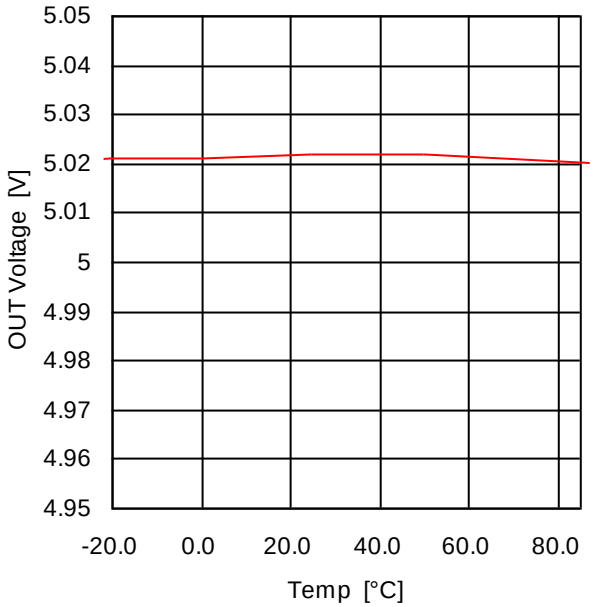


Figure 3. OUT Voltage [V] vs. Temp. [°C] (R_{SET}=27k Ω)

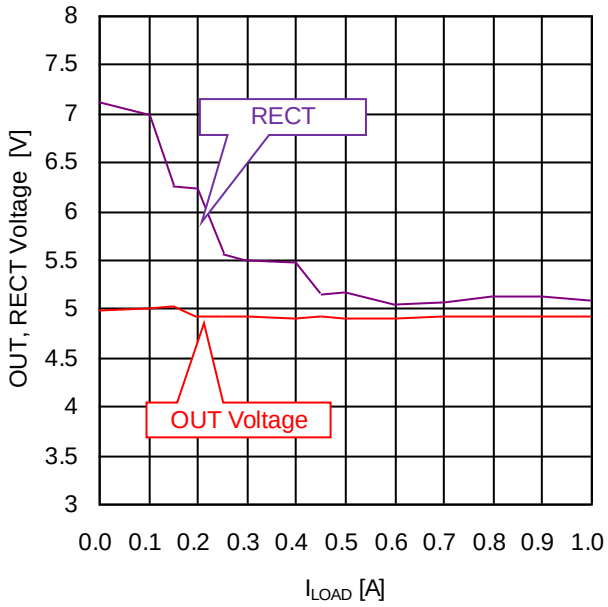


Figure 4. OUT Voltage [V] and RECT Voltage [V] vs. ILOAD [A] (R_{SET}=27k Ω)

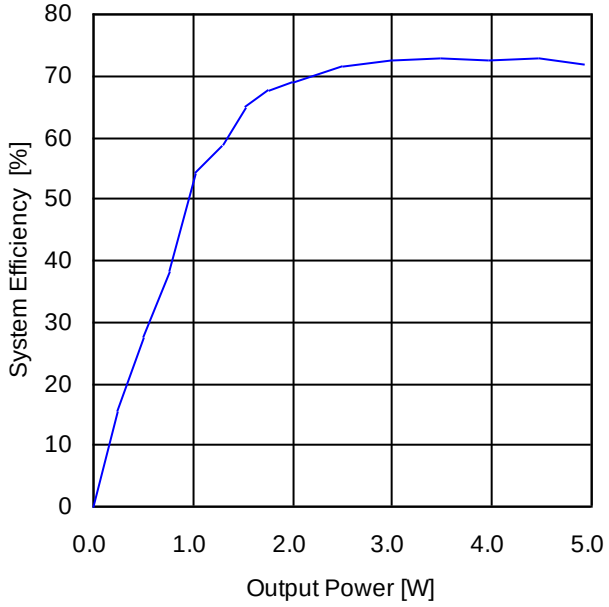


Figure 5. System Efficiency [%] vs. Output Power [W] (R_{SET}=27k Ω)

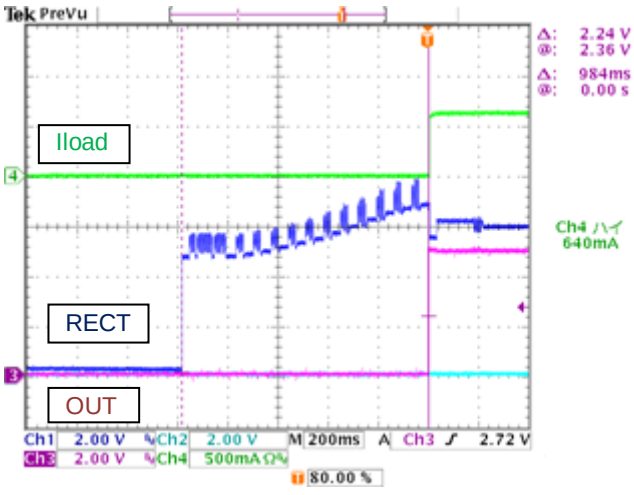


Figure 6. Startup Waveform (R_{SET}=27k Ω)

Pin Configuration

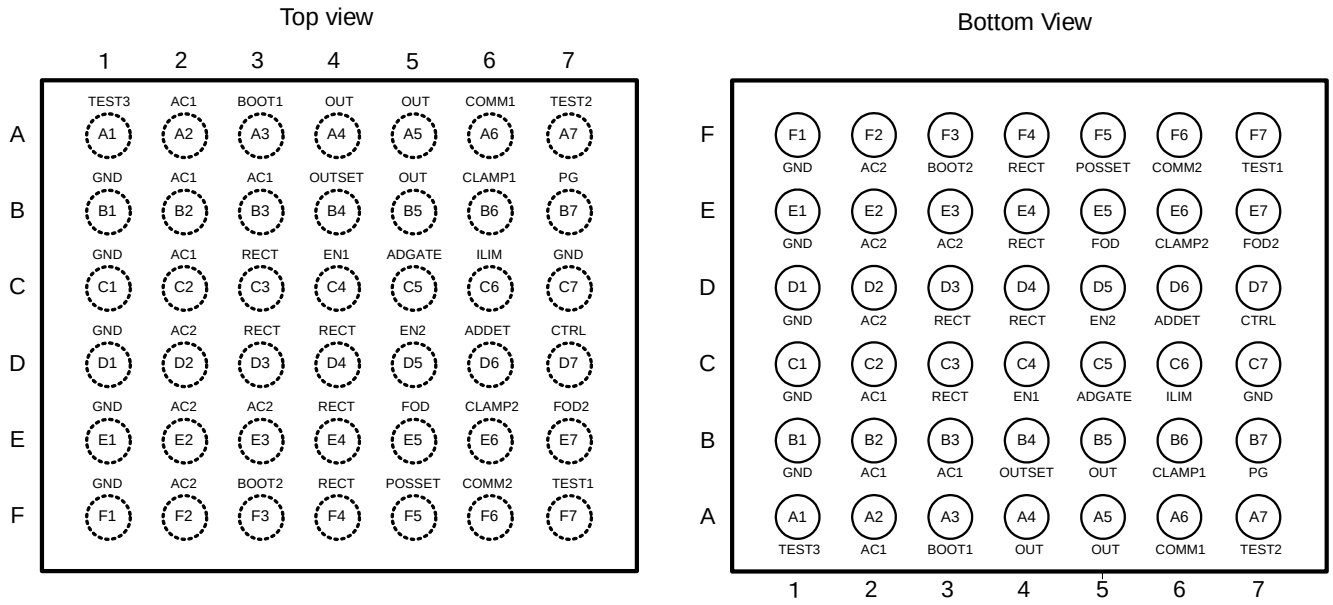


Figure 7. Pin configuration

Pin Description

Pin No.	Pin Name	I/O	Function
A1	TEST3	-	Test pin3 for shipment inspection / This pins deal with open
A2	AC1	In	AC input1
A3	BOOT1	In	Bootstrap capacitor1 connect for driving FET
A4	OUT	Out	Adjustable Output
A5	OUT	Out	Adjustable Output
A6	COMM1	Out	Modulation Control Output1
A7	TEST2	-	Test pin2 for shipment inspection / This pins deal with open
B1	GND	-	Rectifier and Analog Ground
B2	AC1	Out	AC input1
B3	AC1	Out	AC input1
B4	OUTSET	In/Out	Resistor connecting pin for output voltage setting
B5	OUT	Out	Adjustable Output
B6	CLAMP1	Out	AC1 Clamp Protection
B7	PG	Out	Open drain Output for inform the output is enabled
C1	GND	-	Rectifier and Analog Ground
C2	AC1	In	AC input1
C3	RECT	Out	Rectifier Output
C4	EN1	In	Input that decide to enable/disable wireless and wired charging
C5	ADGATE	Out	External Power Pass Gate Driver
C6	ILIM	In/Out	Connect current limit level setting resistor
C7	GND	-	Rectifier and Analog Ground
D1	GND	-	Rectifier and Analog Ground

Pin Description – continued

Pin No.	Pin Name	I/O	Function
D2	AC2	In	AC input2
D3	RECT	Out	Rectifier Output
D4	RECT	Out	Rectifier Output
D5	EN2	In	Input that decide to enable/disable wireless and wired charging
D6	ADDET	In	Adapter Voltage Detection
D7	CTRL	In	Input pin to send End Power Transfer packet/ abnormal temperature or termination signal.
E1	GND	-	Rectifier and Analog Ground
E2	AC2	In	AC input2
E3	AC2	In	AC input2
E4	RECT	Out	Rectifier Output
E5	FOD	In	Foreign Object Detecting adjust pin1
E6	CLAMP2	Out	AC2 Clamp Protection
E7	FOD2	In	Foreign Object Detecting adjust pin2
F1	GND	-	Rectifier and Analog Ground
F2	AC2	In	AC input2
F3	BOOT2	Out	Bootstrap capacitor2 connect for driving FET
F4	RECT	Out	Rectifier Output
F5	POSSET	In/Out	Resistor connecting pin for the Position Gap alarm.
F6	COMM2	Out	Modulation Control Output2
F7	TEST1	-	Test pin1 for shipment inspection / This pins deal with open

Block Diagram

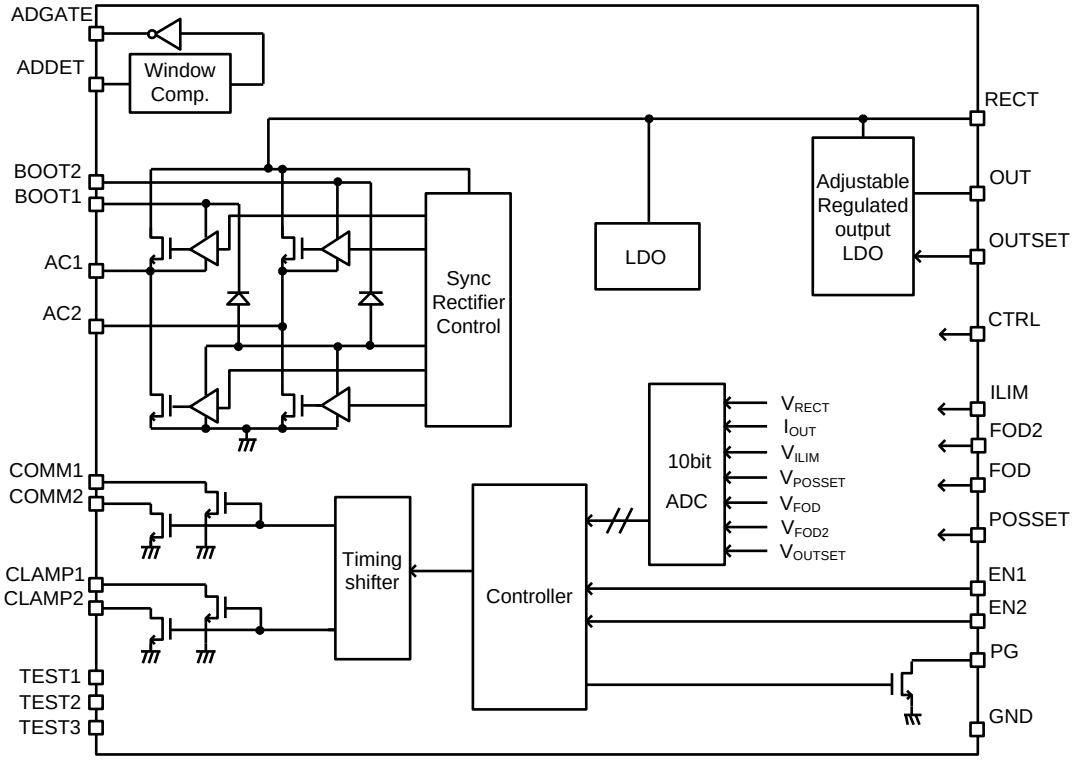


Figure 8. Block diagram

Description of Block

1. Rectifier block

According to electromagnetic induction phenomena, electromotive force occurs in a secondary side coil in inputting AC signal into the both ends of a primary side (TX) coil. Full-wave rectification by switching operation is realized by detecting output current from the coil generated from the above-mentioned operation, making on/off the built-in FET connected to the AC1 and the AC2 pin, outputting current to RECT, and charging the RECT pin external capacity.

The detecting a coil current is to compare the AC pin voltage (FET Ron x I_{COIL}) with GND level. The on/off signal of built-in FET is generated based on this detection signal. The on/off timing of L side FET and H side FET is monitored, and penetration current is prevented.

The bootstrap drive system which sets the H side and L side to Nch FET is adopted for high efficiency. Therefore, the capacitor for voltage maintenance is needed between the BOOT1 (BOOT2) pin and the AC1 (AC2) pin.

2. Low Drop Out (LDO) block

The OUT pin output voltage can be freely set up by external resistance. It assumes that system load (PMIC) including a charger is connected to the OUT pin. In order to suppress heating on the whole set, it recommends carrying out an OUT setup near the full charge voltage of the Li-ion battery.

An error signal is returned to the TX side so that the input-and-output difference of RECT and OUT may become the minimum.

An input-and-output difference is made small, so that load is large, and heating of IC simple substance is suppressed.

The relation between I_{OUT} and desired point (voltage which the RECT pin voltage converges) is as follows.

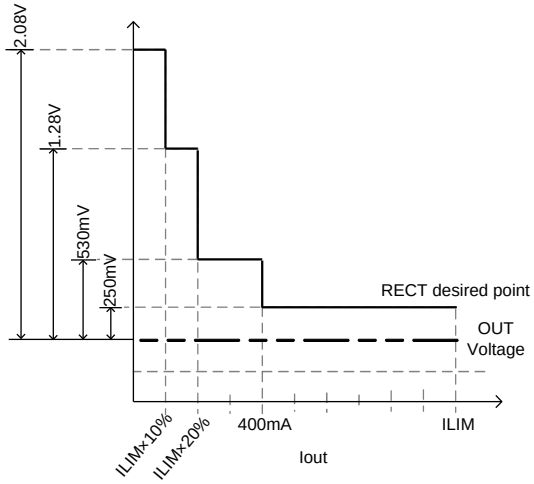


Figure 9. RECT desired point

Output voltage becomes settled uniquely in the resistance (E24 series) connected to the OUTSET pin.
It can choose from the 16 following steps.

Step	OUT setting[V]	RSET[kΩ] (E24)
0	4.30	180
1	4.35	120
2	4.40	91
3	4.45	75
4	4.50	62
5	4.55	56
6	4.60	47
7	4.65	43
8	4.70	39
9	4.75	36
10	4.80	33
11	4.90	30
12	5.00	27
13	5.10	24
14	5.20	22
15	5.30	20

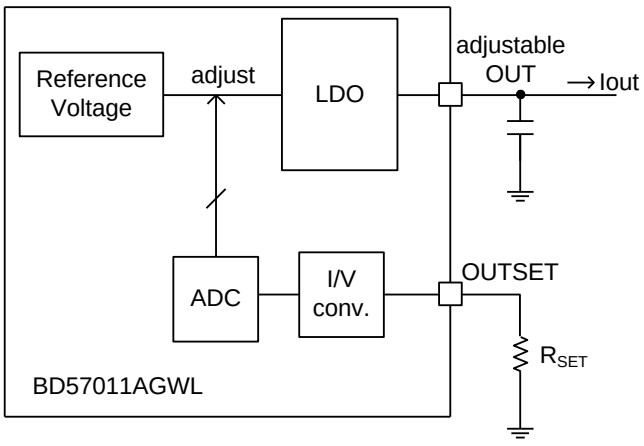


Figure 10. OUTSET circuit

An OUTSET terminal cannot be used by OPEN. Be sure to connect a resistor and use it.
Moreover, you can't change OUTSET setting during operation.
You need to apply a load after OUT output due to OCP limitation.

Description of Block – continued

3. A/D Converter block

The Analog to Digital translation of the various analog signals which serve as a candidate for operation in the case of packet generation is carried out. The A/D converter has adopted successive approximation register.
This converter is completed inside IC and cannot be controlled from the outside.

4. Controller block

The packet based on Qi standard (ver1.2) of WPC (Wireless Power Consortium) is controlled.
The packet to support becomes as follows about an End Power Transfer packet (EPT).

End Power transfer			
value	**reason**	**support**	**condition**
0x00	Unknown	Sent	Adapter Input detection
0x01	Charge Complete	Sent	Charge Complete
0x02	Internal Fault	Sent	Internal abnormal temperature, ILIM abnormal setting, OUTSET abnormal setting
0x03	Over Temperature	Sent	External abnormal temperature
0x04	Over Voltage	Not Sent	-
0x05	Over Current	Not Sent	-
0x06	Battery Failure	Not Sent	-
0x07	Reserved	Not Sent	-
0x08	No Response	Sent	No convergence to RECT desired point

5. Adapter detection block

BD57011AGWL includes the detective function of the cable power supply of the 5V system.
If it detects that the ADDET pin became 3.6V (Typ) or more, since priority is given to an adapter (cable charge), wireless power supply will be stopped (End Power Transfer output), and an OUT output will be stopped.
It checks that OUT voltage is 0.7V or less, and makes the PMOS opposite switch of an adapter line turn on (ADGATE:H to L).
The sequence of operation at the time of adapter detection is as follows.

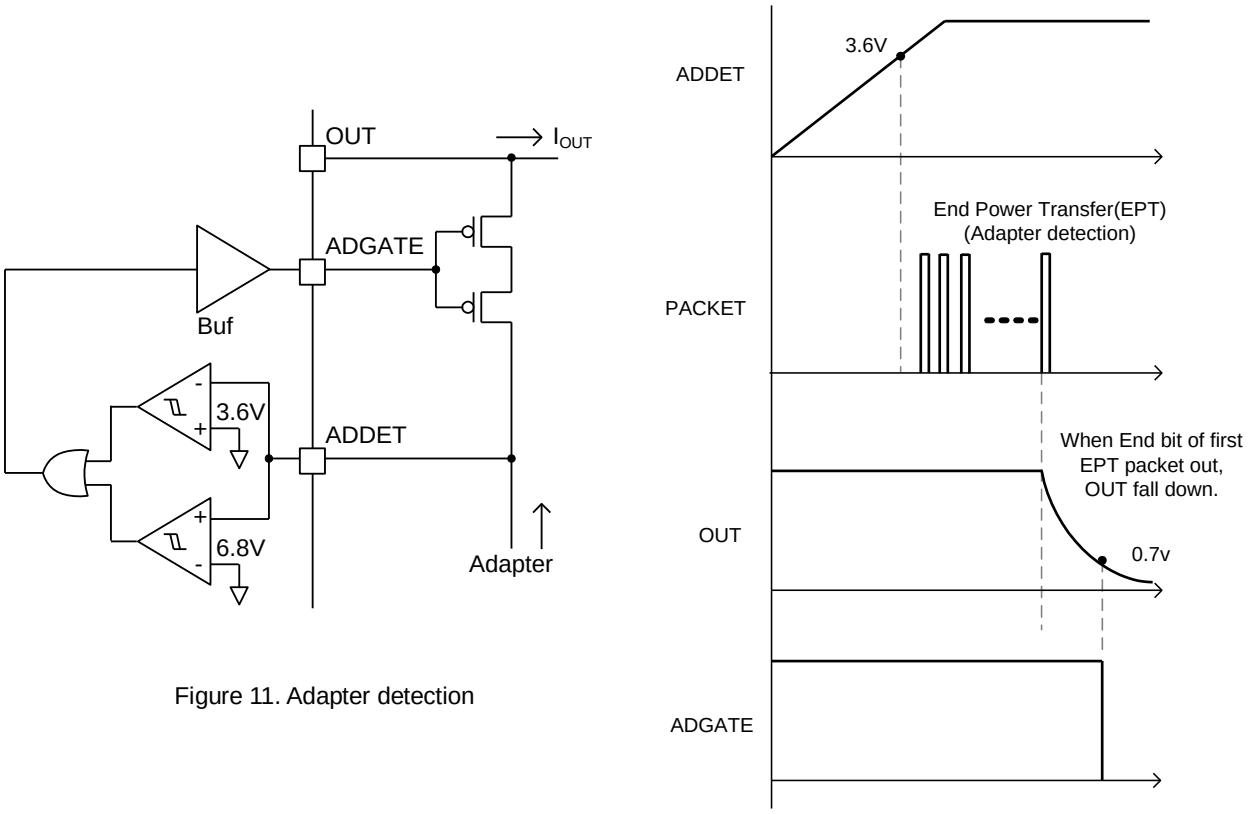


Figure 11. Adapter detection

If set to ADDET≥6.8V, it will be in an OVP detection state and will carry out the instant stop of the PMOS of a power path regardless of the existence of wireless power supply.

Description of Block – continued

6. External control input (EN1, EN2 and CTRL).

Active/non-active of wireless supply and wired (adapter) supply can be set up by EN1 and EN2.
It becomes the standard when (EN1=L, EN2=H) setting uses wireless charge, so both wireless power supply and adapter control are active. When both powers come, priority is given to adapter (wired power), wireless power is stopped according to the sequence explained in adapter detection block, and the electrical connection of the path from an adapter is carried out.
When EN1 turn to H, End Power Transfer (0x01:Charge Complete) packet outputs, so wireless power supply will be stopped.

It is as follows if these are summarized in a table.

EN1	EN2	Result
L	H	Both wireless power supply and adapter control are active. Priority is given to the supply from an adapter. That is, if an adapter input is carried out during wireless power supply, wireless power immediately stop and only an adapter carry out.
H	H	Both an adapter and wireless power supply are non-active. That is, in this mode, power is not supplied from OUT.

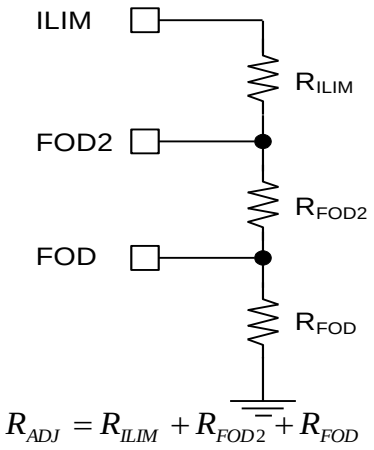
The CTRL pin becomes an external temperature abnormal signal input.
Please input H signal to suspend wireless power supply system compulsorily by unusual generation of heat of a set, etc.
End Power Transfer (0x03:Over Temperature) is outputted.

7. ILIM setup

The current limit value of the OUT pin can be set up by resistance connected to the ILIM pin.
The relation between setting resistance and limit current (ILIM) becomes as the following formula.

$$I_{ILIM} = R_{ADJ} \times 10^{-5} [A]$$

R_{ADJ} is total value of R_{LIM}, R_{FOD2} and R_{FOD}.
E.g. ILIM=1A setup at the time of R_{ADJ}=100kΩ.
If R_{ADJ} sets 150kΩ or over (ILIM setting 1.5A or over), IC outputs EPT packet (internal fault).



$$R_{ADJ} = R_{ILIM} + R_{FOD2} + R_{FOD}$$

Description of Block – continued

8. FOD adjust setting

In order to implement FOD (Foreign Object Detection) function that Qi compliant ver1.2 makes rules, it is necessary to compute received power strictly and to compare with the transmitted power from the TX side. The FOD and FOD2 pin is used for the received power fine tuning. These parameters adjust a lost (e.g. LC loss) which is not understood inside IC.
The relation between received power (P_{PR}) and FOD, FOD2 pin input voltage becomes as the following formula.

$$P_{PR} = \alpha \times f(RECT, I_{OUT}) + \beta [W]$$

$$\alpha = 1 + \frac{V_{FOD2}}{1.955mV} \times 0.004$$

$$\beta = \frac{V_{FOD}}{1.955mV} \times 0.004 - 0.25[W]$$

α is a parameter for slope adjust, proportional to FOD2 voltage. β is a parameter for offset adjust, proportional to FOD voltage.
A Function f (RECT, I_{OUT}) is a value calculating in IC, nearly proportional to output power.
Setting example presents. It necessary to coordinated with R_{FOD}, R_{FOD2} and ILIM setting resistor.
In the case of setting; ILIM=1A, α=1.2, β=-0.2W, Solving the following simultaneous equations, the value of FOD setting resistors is obtained.

$$R_{ADJ} = R_{ILIM} + R_{FOD2} + R_{FOD}$$

$$\frac{(\alpha - 1) \times 1.955mV}{0.004} = I_{ILIM} \times (R_{FOD2} + R_{FOD})$$

$$\frac{(\beta + 0.25) \times 1.955mV}{0.004} = I_{ILIM} \times R_{FOD}$$

In this case, R_{FOD}=2.4kΩ, R_{FOD2}=7.4kΩ, R_{ILIM}=90.2kΩ.
The configuration described above is a reference value. Must be adjusted by the considering external factors (the presence or absence of the metal for absorbing the magnetic flux, such as a battery) and the surrounding environment of the coil material, the coil shape, and the distance to the Tx coil.

9. POSSET setting

The height of the RECT voltage at a start-up is judged, and position gap of the XY direction between TX coil and RX coil is detected. The threshold (Vth, pos) of whether to take out alarm with the resistance connected to the POSSET pin can be decided. When RECT voltage is lower than Vth, pos, a pulse is outputted 5 times from the PG pin at the time of an OUT output.
The relation between setting resistance and detection threshold voltage (Vth, pos) becomes as the following formula.

$$Vth, pos = \frac{2.8 \times 10^5}{R_{POS}} [V]$$

R_{POS} is the POSSET pin connection resistance. E.g. Vth, pos=2.8V setup at the time of R_{POS}=100kΩ.
In the case of nullification for this function, set R_{POS}=120kΩ.

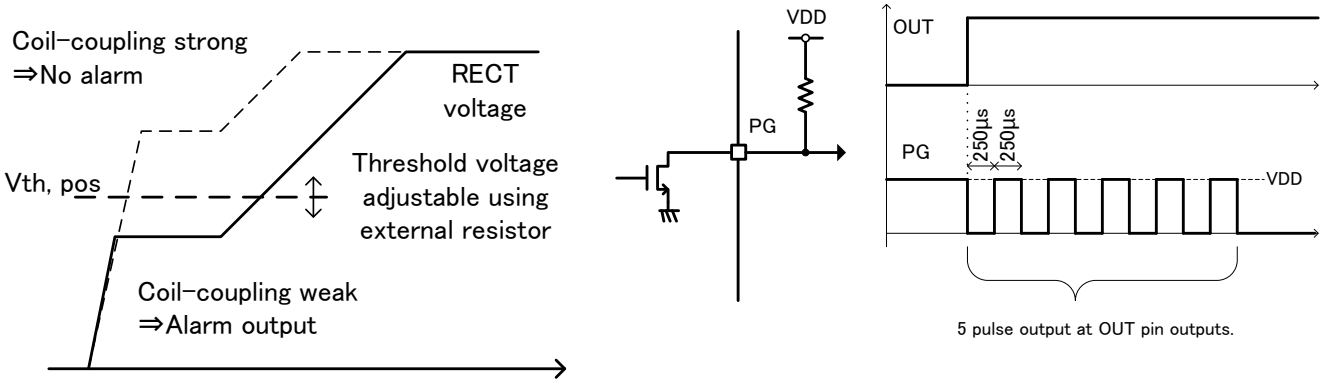


Figure 12. Position Gap alarm

Application Example

1. Recommended Diagram

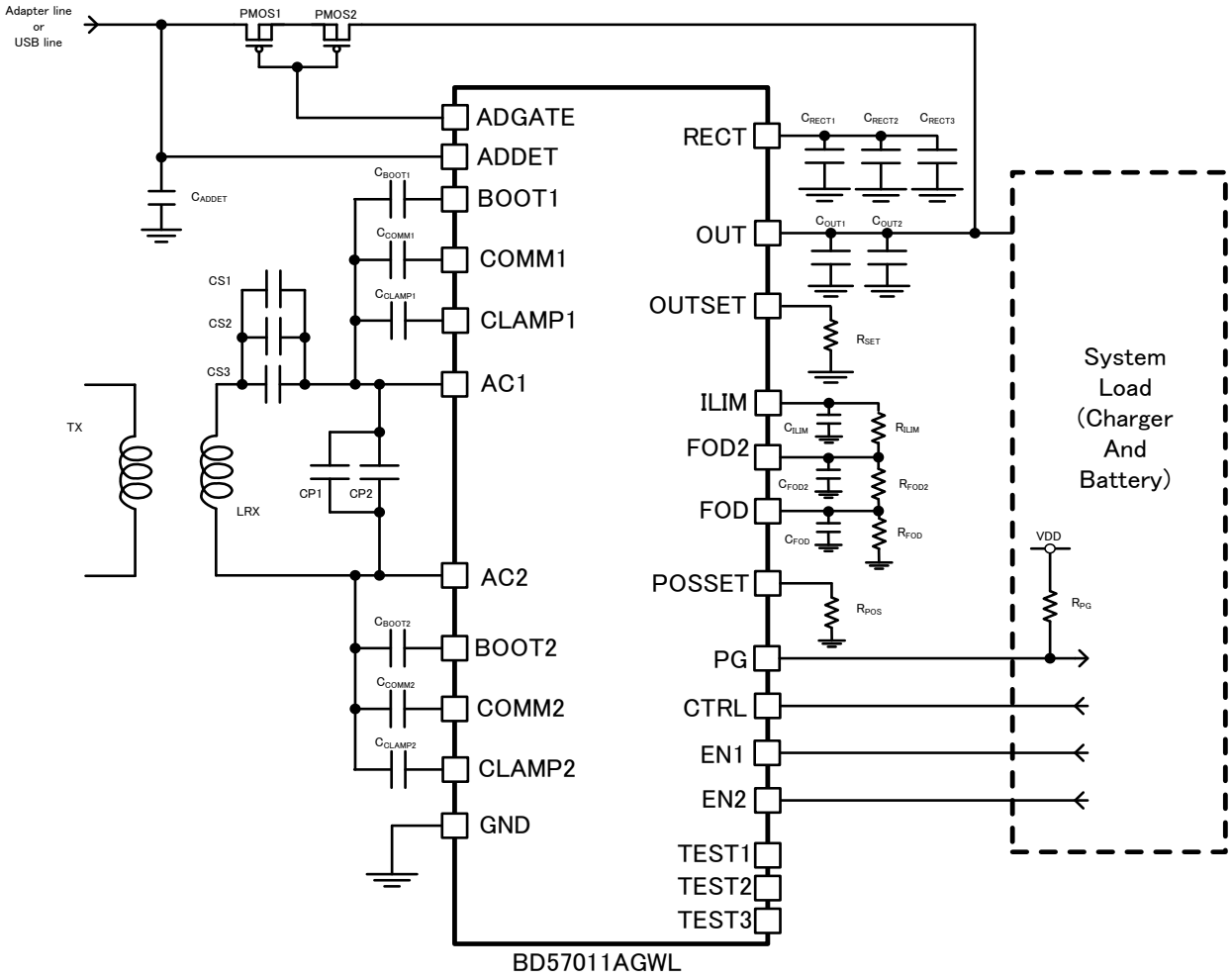


Figure 13. Typical application circuit

2. Parts list

Part Name	Recommended Value	Unit	Recommended Part	Maker
LRX	12	µH	WR-482350-15M2-G	TDK Co., Ltd.
CS1	0.068	µF	GRM188B11E683JA01#	MURATA Co., Ltd.
CS2	0.068	µF	GRM188B11E683JA01#	MURATA Co., Ltd.
CS3	0.068	µF	GRM188B11E683JA01#	MURATA Co., Ltd.
CP1	1500	pF	GRM155B11E152KA01#	MURATA Co., Ltd.
CP2	680	pF	GRM155B11E681KA01#	MURATA Co., Ltd.
C_{BOOT1}, C_{BOOT2}	0.01	µF	GRM155R61E103KA01#	MURATA Co., Ltd.
C_{COMM1}, C_{COMM2}	0.033	µF	GRM155B31E333KA87#	MURATA Co., Ltd.
C_{CLAMP1}, C_{CLAMP2}	0.47	µF	GRM155R61E474KE01#	MURATA Co., Ltd.
C_{RECT1}	0.1	µF	GRM155R61E104KA87#	MURATA Co., Ltd.
C_{RECT2}	10	µF	GRM188R61E106KA73#	MURATA Co., Ltd.
C_{RECT3}	10	µF	GRM188R61E106KA73#	MURATA Co., Ltd.
C_{OUT1}	0.1	µF	GRM155R61E104KA87#	MURATA Co., Ltd.
C_{OUT2}	2.2	µF	GRM155B31A225KE95#	MURATA Co., Ltd.
C_{ILIM}	No Mount (dummy)	-	-	-
C_{ADDET}	1.0	µF	GRM155R6YA105KE11#	MURATA Co., Ltd.
R_{SET}	27	kΩ	MCR006YLPD2702	ROHM Co., Ltd.
R_{ILIM}	100	kΩ	MCR006YLPD1003	ROHM Co., Ltd.
R_{FOD}	10	kΩ	MCR006YLPD1002	ROHM Co., Ltd.
R_{FOD2}	3.6	kΩ	MCR006YLPD3601	ROHM Co., Ltd.
R_{POS}	56	kΩ	MCR006YLPD5602	ROHM Co., Ltd.
R_{PG}	3	kΩ	MCR006YLPJ3001	ROHM Co., Ltd.
PMOS1, PMOS2	Ron < 100mΩ	-	TT8J2TR	ROHM Co., Ltd.

The above parts are those at the time of evaluation, and as for the coil, other coils made by TDK and wurth are also under consideration, so please contact us.

Timing Chart

Start up sequence

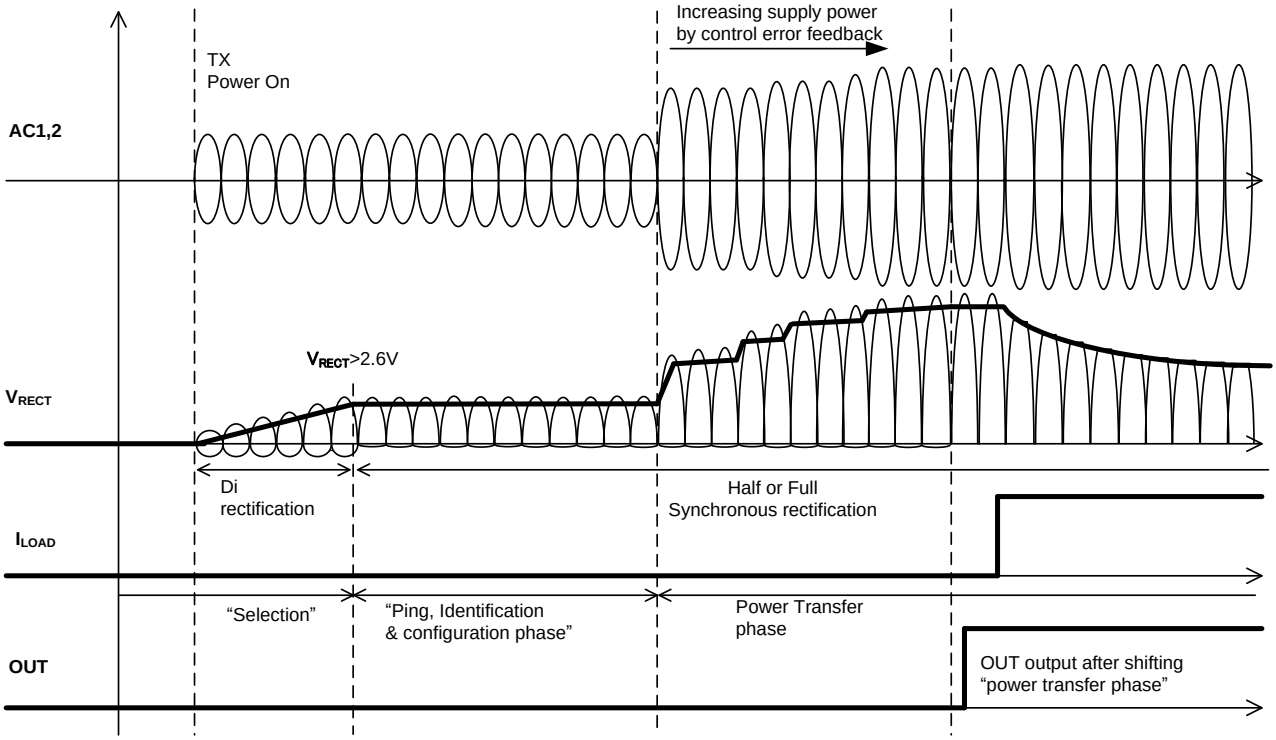
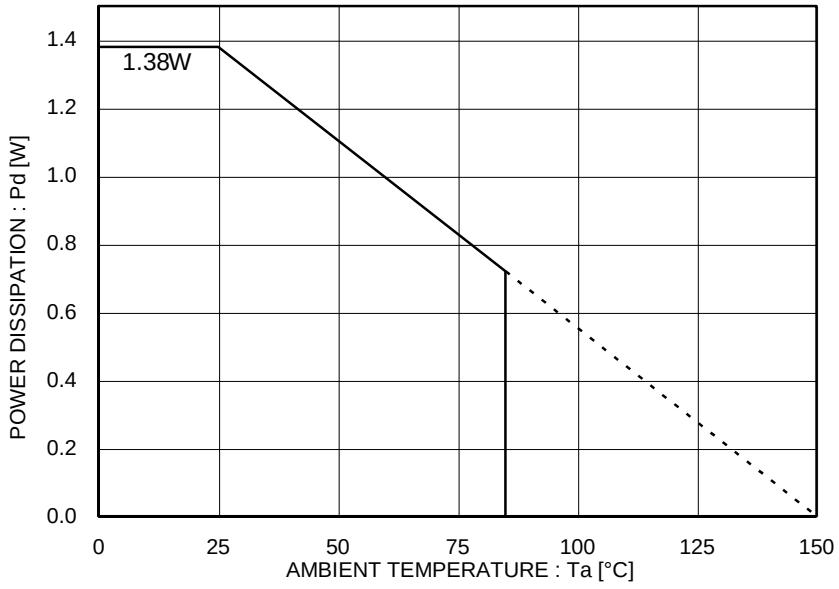


Figure 14. Start up sequence

Power Dissipation

(UCSP50L3C Package)

Use a thermal design that allows for a sufficient margin by taking into account the permissible power dissipation (Pd) in actual operating conditions.

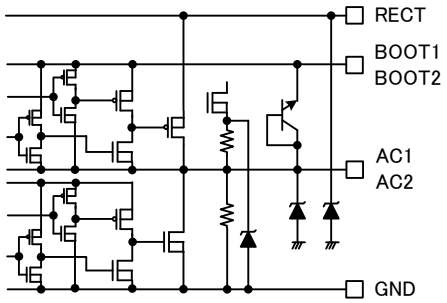


* 54mm x 62mm x 1.6mm Glass Epoxy Board

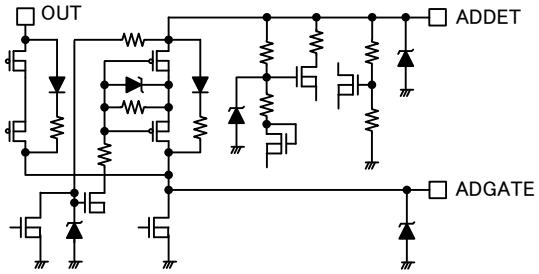
Figure 15. Power Dissipation Curve (Pd-Ta Curve)

I/O Equivalence Circuit

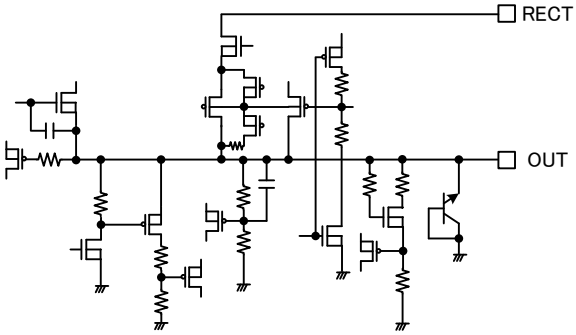
RECT, AC1, AC2, BOOT1, BOOT2, GND pin



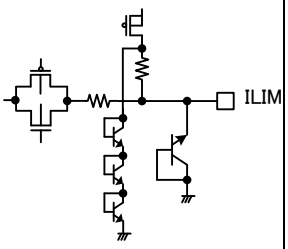
ADDET, ADGATE pin



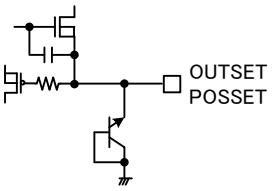
OUT pin



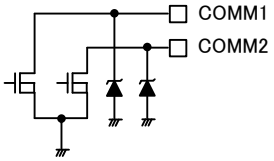
ILIM pin



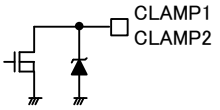
OUTSET, POSSET pin



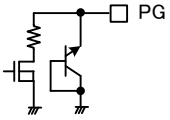
COMM1, COMM2 pin



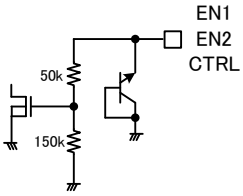
CLAMP1, CLAMP2 pin



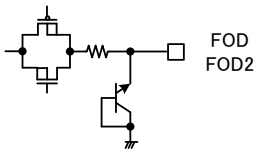
PG pin



EN1, EN2, CTRL pin



FOD, FOD2 pin



Operation Notes

1. Reverse Connection of Power Supply
Connecting the power supply in reverse polarity can damage the IC. Take precautions against reverse polarity when connecting the power supply, such as mounting an external diode between the power supply and the IC's power supply pins.

2. Power Supply Lines
Design the PCB layout pattern to provide low impedance supply lines. Separate the ground and supply lines of the digital and analog blocks to prevent noise in the ground and supply lines of the digital block from affecting the analog block. Furthermore, connect a capacitor to ground at all power supply pins. Consider the effect of temperature and aging on the capacitance value when using electrolytic capacitors.

3. Ground Voltage
Except for pins the output and the input of which were designed to go below ground, ensure that no pins are at a voltage below that of the ground pin at any time, even during transient condition.

4. Ground Wiring Pattern
When using both small-signal and large-current ground traces, the two ground traces should be routed separately but connected to a single ground at the reference point of the application board to avoid fluctuations in the small-signal ground caused by large currents. Also ensure that the ground traces of external components do not cause variations on the ground voltage. The ground lines must be as short and thick as possible to reduce line impedance.

5. Recommended Operating Conditions
The function and operation of the IC are guaranteed within the range specified by the recommended operating conditions. The characteristic values are guaranteed only under the conditions of each item specified by the electrical characteristics.

6. Inrush Current
When power is first supplied to the IC, it is possible that the internal logic may be unstable and inrush current may flow instantaneously due to the internal powering sequence and delays, especially if the IC has more than one power supply. Therefore, give special consideration to power coupling capacitance, power wiring, width of ground wiring, and routing of connections.

7. Operation Under Strong Electromagnetic Field
Operating the IC in the presence of a strong electromagnetic field may cause the IC to malfunction.

8. Testing on Application Boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance output pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from the test setup during the inspection process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

9. Inter-pin Short and Mounting Errors
Ensure that the direction and position are correct when mounting the IC on the PCB. Incorrect mounting may result in damaging the IC. Avoid nearby pins being shorted to each other especially to ground, power supply and output pin. Inter-pin shorts could be due to many reasons such as metal particles, water droplets (in very humid environment) and unintentional solder bridge deposited in between pins during assembly to name a few.

10. Unused Input Pins
Input pins of an IC are often connected to the gate of a MOS transistor. The gate has extremely high impedance and extremely low capacitance. If left unconnected, the electric field from the outside can easily charge it. The small charge acquired in this way is enough to produce a significant effect on the conduction through the transistor and cause unexpected operation of the IC. So unless otherwise specified, unused input pins should be connected to the power supply or ground line.

Operational Notes – continued

11. Regarding the Input Pin of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. P-N junctions are formed at the intersection of the P layers with the N layers of other elements, creating a parasitic diode or transistor. For example (refer to figure below):

When GND > Pin A and GND > Pin B, the P-N junction operates as a parasitic diode.
When GND > Pin B, the P-N junction operates as a parasitic transistor.

Parasitic diodes inevitably occur in the structure of the IC. The operation of parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Therefore, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

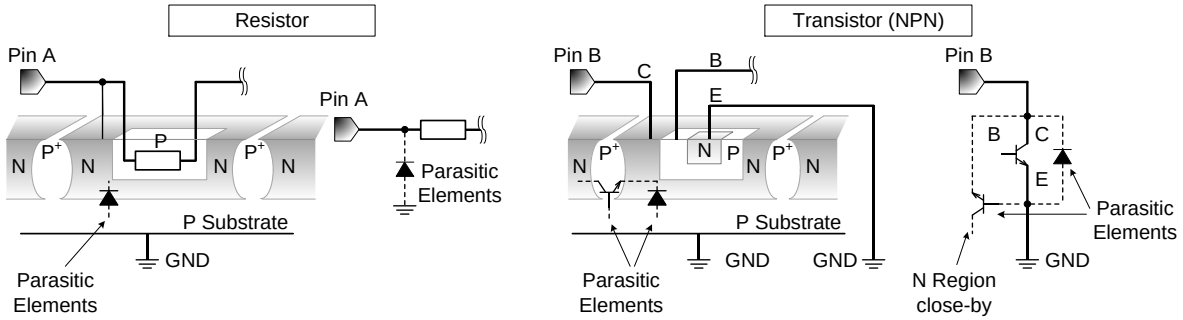


Figure 16. Example of monolithic IC structure

12. Ceramic Capacitor

When using a ceramic capacitor, determine the dielectric constant considering the change of capacitance with temperature and the decrease in nominal capacitance due to DC bias and others.

13. Area of Safe Operation (ASO)

Operate the IC such that the output voltage, output current, and the maximum junction temperature rating are all within the Area of Safe Operation (ASO).

14. Thermal Shutdown Circuit (TSD)

This IC has a built-in thermal shutdown circuit that prevents heat damage to the IC. Normal operation should always be within the IC's maximum junction temperature rating. If however the rating is exceeded for a continued period, the junction temperature (Tj) will rise which will activate the TSD circuit that will turn OFF all output pins. The IC should be powered down and turned ON again to resume normal operation because the TSD circuit keeps the outputs at the OFF state even if the TJ falls below the TSD threshold.
Note that the TSD circuit operates in a situation that exceeds the absolute maximum ratings and therefore, under no circumstances, should the TSD circuit be used in a set design or for any purpose other than protecting the IC from heat damage.

15. Over Current Protection Circuit (OCP)

This IC incorporates an integrated overcurrent protection circuit that is activated when the load is shorted. This protection circuit is effective in preventing damage due to sudden and unexpected incidents. However, the IC should not be used in applications characterized by continuous operation or transitioning of the protection circuit.

16. Disturbance Light

In a device where a portion of silicon is exposed to light such as in a WL-CSP and chip products, IC characteristics may be affected due to photoelectric effect. For this reason, it is recommended to come up with countermeasures that will prevent the chip from being exposed to light.

Ordering Information

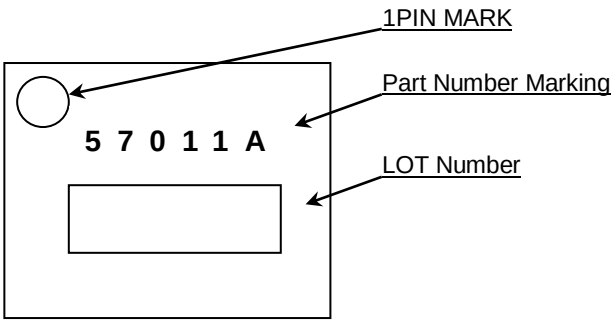
B D 5 7 0 1 1 A G W L	-	E 2

Part Number

Package
GWL: UCSP50L3C

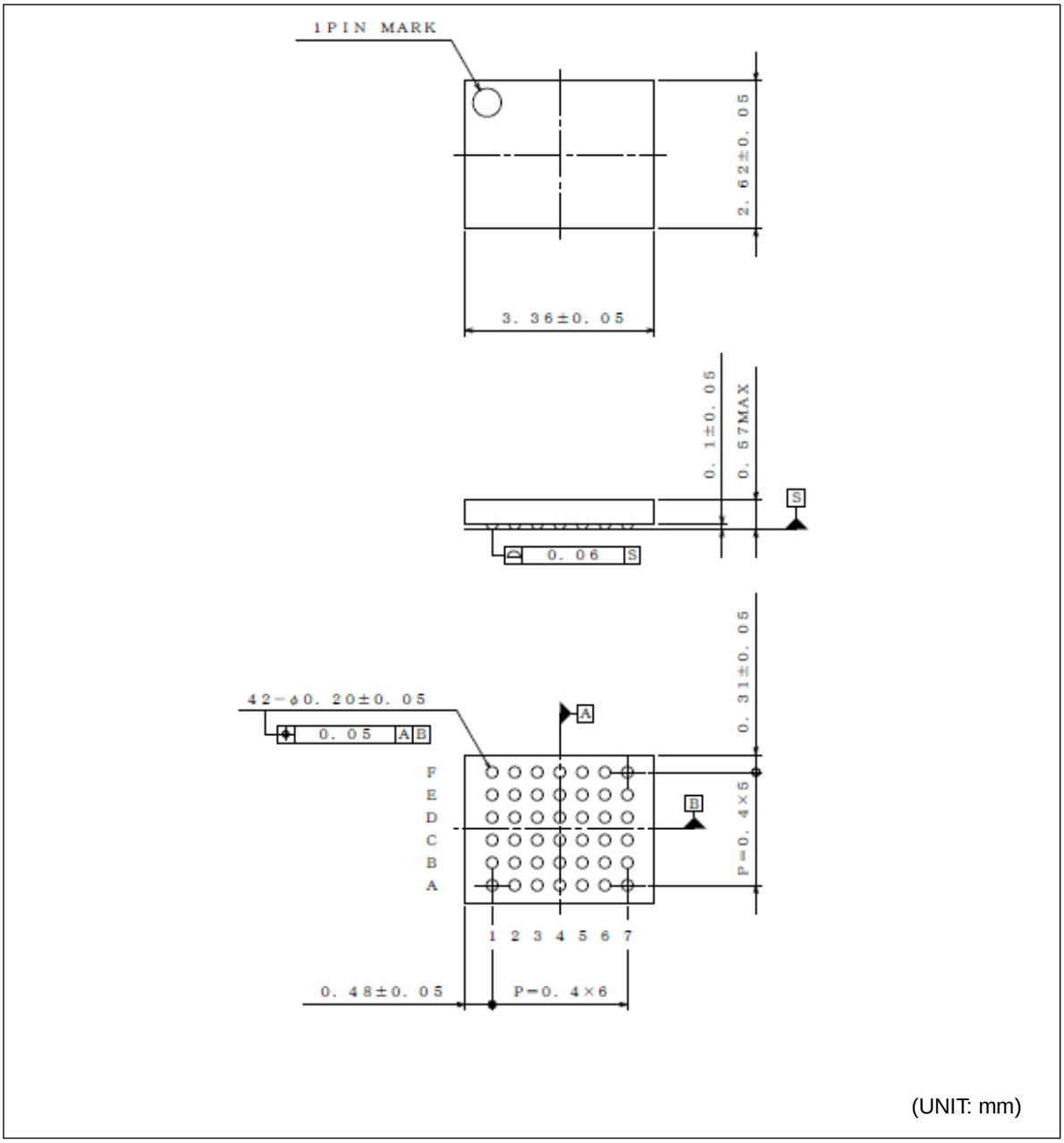
Packaging and forming specification
E2: Embossed tape and reel

Marking Diagram



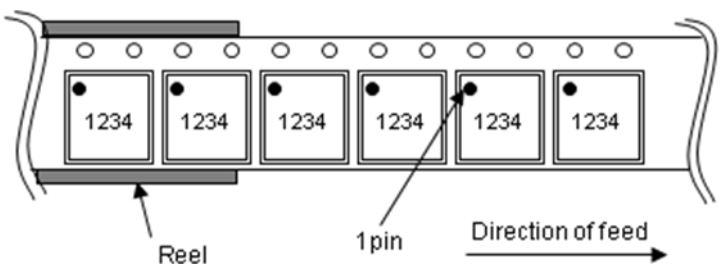
Physical Dimension Tape and Reel Information

Package Name	UCSP50L3C(BD57011AGWL)



< Tape and Reel Information >

Tape	Embossed carrier tape
Quantity	2,500pcs
Direction of feed	E2 The direction is the pin 1 of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand



Revision History

Date	Revision	Changes
01.Sep.2016	001	New Release
04.Oct.2017	002	Page.1 Correct written error (Operating Temperature Range) Modified terms based on latest specification Remove “Key Specifications” Addition of notation of number of pins Page.2 Correct written error (Operating Temperature Range) , Change of notation of recommended operating condition Page.6 Correct written error (CTRL pin function), Changing notation of terminal description Page.7 Changing notation of terminal description Page.8 Correct written error (Rectifier block) Page.9 Correct written error (Adapter detection block) Page.11 Correct written error (FOD adjust setting) Page.12 Annotation is added to the margin of the parts list Page.17 Add description of status of document
31.Jan.2018	003	Page.2 Addition of Caution 2 Page.3-4 Correction of notation (change from lower case to upper case), correct written error Page.5 Correct written error (R_{ILIM}) Page.6-7 Top View Added, Bottom View drawing correction, add explanation that the TEST pin is open and used for the pin description. Page.9-12 Correction of nation (change from lower case to upper case), Correct written error Page.13 Correct written error (part number), addition of part name Page.14-15 Correction of nation Page.16-17 Changing the description of the “Ground Voltage”, delete about the “Thermal Consideration”, modification of other notation
28.Jun.2018	004	Page.6 Top View and Bottom View drawing correction

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(Note1) Medical Equipment Classification of the Specific Applications

JAPAN	USA	EU	CHINA
CLASSⅢ	CLASSⅢ	CLASSⅡb	CLASSⅢ
CLASSⅣ		CLASSⅢ	

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   [c] Use of our Products in places where the Products are exposed to sea wind or corrosive gases, including Cl_2, H_2S, NH_3, SO_2, and NO_2
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   [h] Use of the Products in places subject to dew condensation

4. The Products are not subject to radiation-proof design.

5. Please verify and confirm characteristics of the final or mounted products in using the Products.

6. In particular, if a transient load (a large amount of load applied in a short period of time, such as pulse. is applied, confirmation of performance characteristics after on-board mounting is strongly recommended. Avoid applying power exceeding normal rated power; exceeding the power rating under steady-state loading condition may negatively affect product performance and reliability.

7. De-rate Power Dissipation depending on ambient temperature. When used in sealed area, confirm that it is the use in the range that does not exceed the maximum junction temperature.

8. Confirm that operation temperature is within the specified range described in the product specification.

9. ROHM shall not be in any way responsible or liable for failure induced under deviant condition from what is defined in this document.

Precaution for Mounting / Circuit board design

1. When a highly active halogenous (chlorine, bromine, etc.) flux is used, the residue of flux may negatively affect product performance and reliability.

2. In principle, the reflow soldering method must be used on a surface-mount products, the flow soldering method must be used on a through hole mount products. If the flow soldering method is preferred on a surface-mount products, please consult with the ROHM representative in advance.

For details, please refer to ROHM Mounting specification

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This Product is electrostatic sensitive product, which may be damaged due to electrostatic discharge. Please take proper caution in your manufacturing process and storage so that voltage exceeding the Products maximum rating will not be applied to Products. Please take special care under dry condition (e.g. Grounding of human body / equipment / solder iron, isolation from charged objects, setting of Ionizer, friction prevention and temperature / humidity control).

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1. Product performance and soldered connections may deteriorate if the Products are stored in the places where:
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   - [b] the temperature or humidity exceeds those recommended by ROHM
   - [c] the Products are exposed to direct sunshine or condensation
   - [d] the Products are exposed to high Electrostatic

2. Even under ROHM recommended storage condition, solderability of products out of recommended storage time period may be degraded. It is strongly recommended to confirm solderability before using Products of which storage time is exceeding the recommended storage time period.

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4. Use Products within the specified time after opening a humidity barrier bag. Baking is required before using Products of which storage time is exceeding the recommended storage time period.

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