Application Note

Charge Protection IC Series with Built-in FET

Standard Protection Type

BD6040GUL, BD6041GUL, BD6042GUL

No.09031EBY01

●Descriptions

The BD6040/41/42GUL charger protection IC developed for portable devices provides up to 28V of over voltage protection for charger Ics. Built-in circuits include overvoltage lockout, overcurrent limit, undervoltage protection, internal start up delay, and status flag.

●Features

1) 28V (max) overvoltage protection
2) Low quiescent current (45μA)
3) Low Ron (125mΩ) FET
4) Overvoltage lockout (OVLO) circuit
5) Undervoltage lockout (UVLO) circuit
6) Internal 2msec start up delay
7) Overcurrent protection circuit
8) Compact package: VCSP50L1(1.6mm x 1.6mm, t=0.55mm)

●Applications

Mobile phones, MP3 players, Digital Still Camera, PDA, IC recorder, Electronic Dictionary, Handheld Game, Game Controller, Camcorder, Bluetooth Headsets, etc

●Line Up

	Over Voltage Lockout (IN=Increasing)	Over Voltage Lockout (Hysteresis)	Package
BD6040GUL	6.40V	30mV	VCSP50L1
BD6041GUL	5.85V	100mV	VCSP50L1
BD6042GUL	6.20V	100mV	VCSP50L1

●ABSOLUTE MAXIMUM RATINGS (Ta = 25℃)

Contents	Symbol	Rating	Unit	Conditions
Input supply voltage 1	Vmax1	-0.3～30	V	IN1,IN2,IN3,IN4
Input supply voltage 2	Vmax2	-0.3～7	V	other
Power dissipation	Pd	725	mW	
Operating temperature range	Topr	-35～+85	℃	
Storage temperature range	Tstr	-55～+150	℃	

※1 When using more than at Ta=25℃, it is reduced 5.8 mW per 1℃.
ROHM specification board 50mm× 58mm mounting.

●RECOMMENDED OPERATING RANGE (Ta=-35～+85℃))

Parameter	Symbol	Range	Unit	Usage
Input voltage range	V_{in}	2.2～28	V	

※ This product is not especially designed to be protected from radioactivity.

●ELECTRICAL CHARACTERISTICS
(Unless otherwise noted, Ta = 25°C, IN=5V)

Parameter	Symbol	Device	Rating			Unit	Conditions
			Min.	Typ.	Max.		
●ELECTRICAL							
Input Voltage Range	VIN	ALL	-	-	28	V	
Supply Quiescent Current	ICC	ALL		45	90	μA	
Under Voltage Lockout	UVLO	ALL	2.53	2.65	2.77	V	IN= decreasing
Under Voltage Lockout Hysteresis	UVLOh	ALL	50	100	150	mV	IN= increasing
Over Voltage Lockout	OVLO	BD6040	6.2	6.4	6.6	V	IN= increasing
		BD6041	5.7	5.85	6.0	V	
		BD6042	6.0	6.2	6.4	V	IN= increasing
Over Voltage Lockout Hysteresis	OVLOh	BD6040	10	30	50	mV	IN= decreasing
		BD6041/42	50	100	150	mV	IN= decreasing
Current limit	ILM	ALL	1.2	-	-	A	
Vin vs. Vout Res.	RON	ALL	-	125	150	mΩ	
OK Output Low Voltage	OKVO	ALL	-	-	400	mV	SINK=1mA
OK Leakage Current	OKleak	ALL	-	-	1	μA	
EN input voltage (H)	ENH	ALL	1.45	-	-	V	
EN input voltage (L)	ENL	ALL	-	-	0.5	V	
EN input current	ENC	ALL	12	25	50	μA	EN=1.5V
●TIMINGS							
Start Up Delay	Ton	ALL	-	2	4	msec	
OK Going Up Delay	Tok	ALL	-	10	15	msec	
Output Turn Off Time	Toff	ALL	-	2	10	μsec	
Alert Delay	Tovp	ALL	-	1.5	10	μsec	

* This product is not especially designed to be protected from radioactivity.

●TYPICAL APPLICATION CIRCUIT

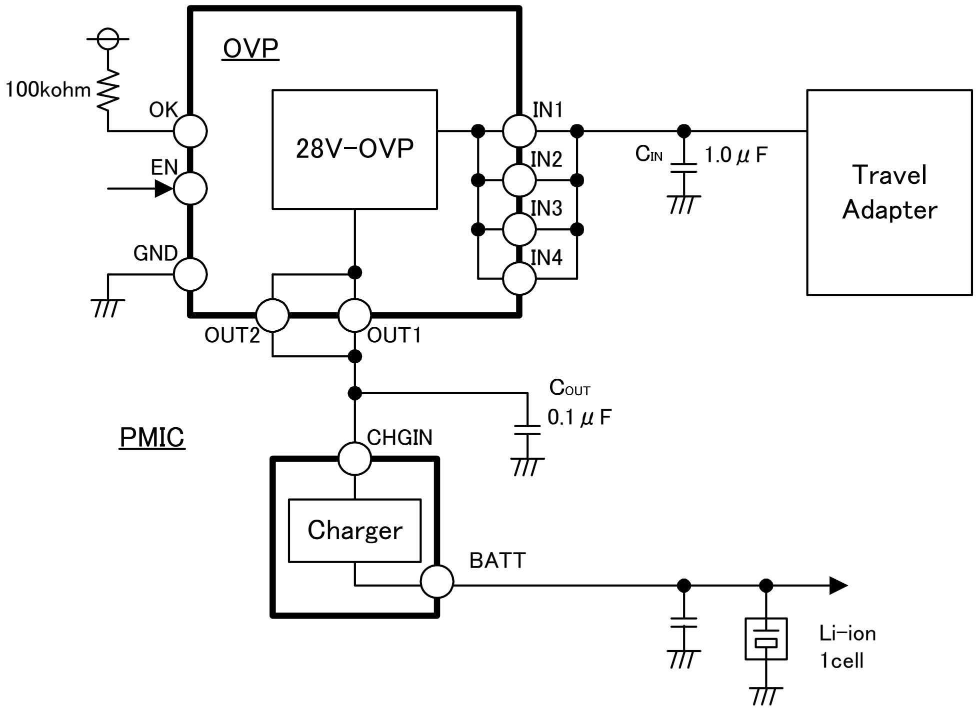


Figure1. Application Circuit

・Safety is high because it detects, and it protects it for an abnormal voltage up to 28V.
・It contributes to the miniaturization because all external is built into.

●BALL CONFIGURATION

Top View

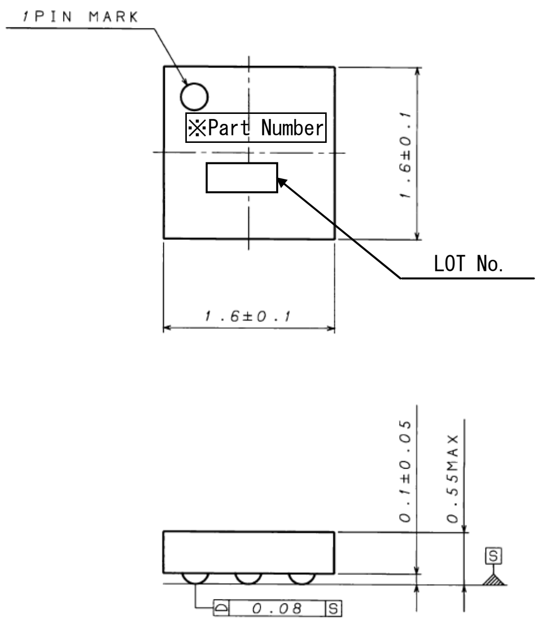
A	OUT	IN	IN
B	OUT	IN	IN
C	OK	EN	GND
	1	2	3

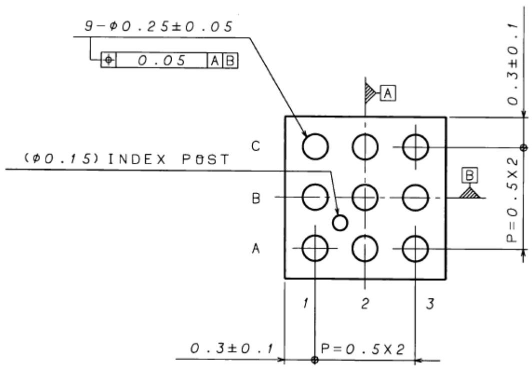
Bottom View

C	OK	EN	GND
B	OUT	IN	IN
A	OUT	IN	IN
	1	2	3

Figure2. BALL CONFIGURATION

●PACKAGE DIMENSIONS(VCSP50L1)





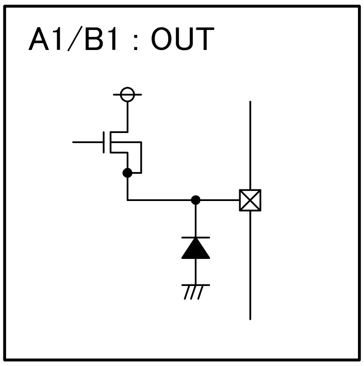
Bottom View

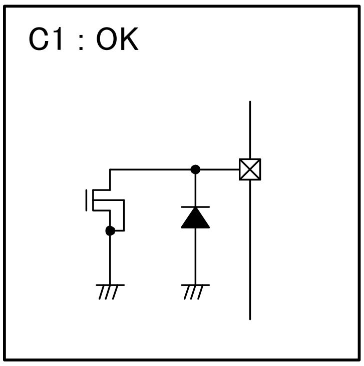
※BD6040GUL is “6040”, BD6041GUL is “6041” , BD6042GUL is “6042”.

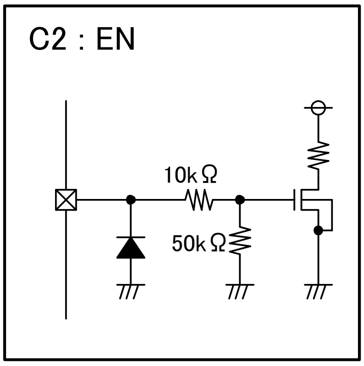
●PIN DESCRIPTIONS

No.	Pin	Name	I/O	ESD Diode		Function
				IN	GND	
1	A2	IN1	I	-	○	Bypass with 1uF Ceramic capacitor or larger to get full 15KV ESD protection (Air, IEC61000-4-2) at the input
2	A3	IN2	I	-	○	
3	B2	IN3	I	-	○	
4	B3	IN4	I	-	○	
5	A1	OUT1	O	-	○	Output Voltage Pin
6	B1	OUT2	O	-	○	
7	C3	GND	-	○	-	Ground Pin
8	C1	OK	O	-	○	Active-low open drain output to signal if the adapter voltage is correct
9	C2	EN	I	-	○	Enable input Drive EN high to turn off OUT (Hi-z output)

●EQUIVALENT CIRCUIT







●BLOCK DIAGRAM

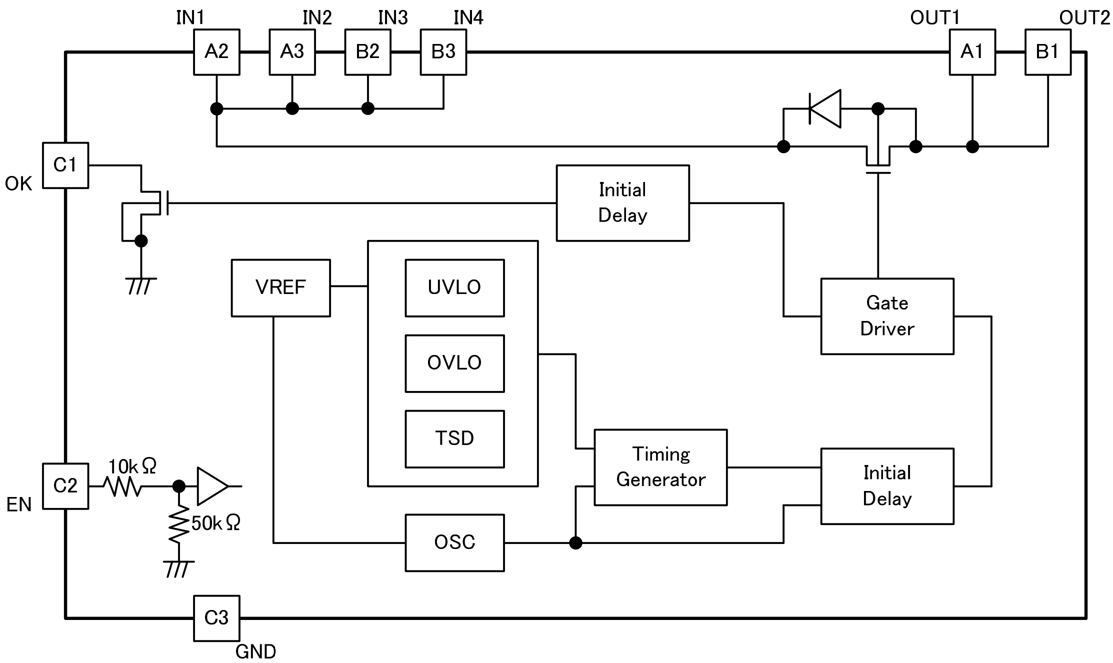


Figure 3. Block Diagram

●TIMING DIAGRAM

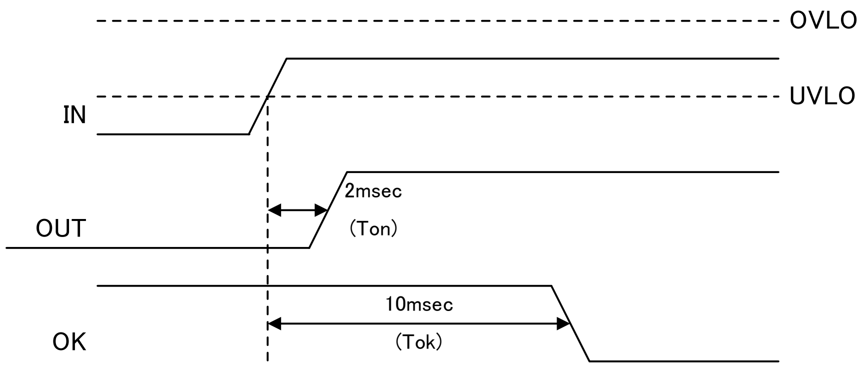


Figure 4. Start up sequence

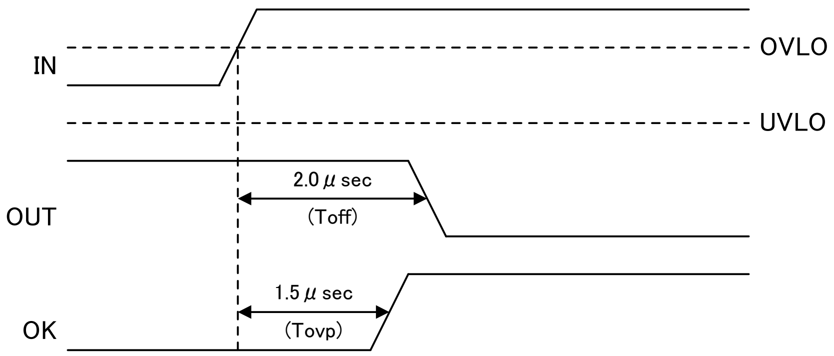


Figure 5. Shutdown by over voltage detection

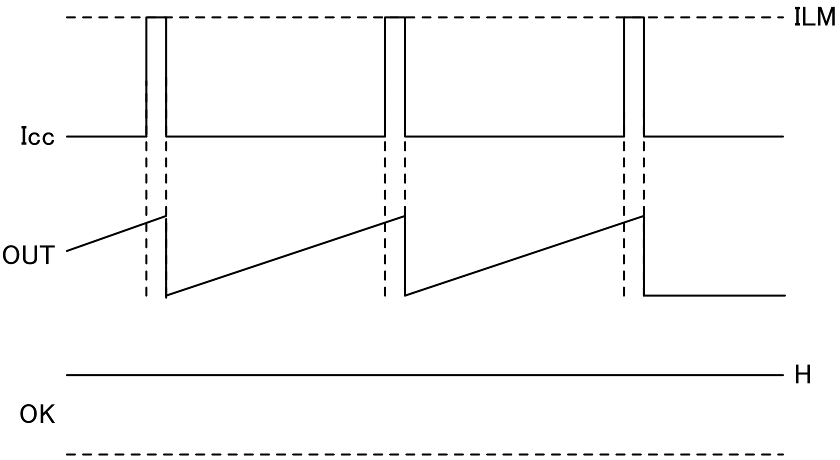


Figure 6. Operation by current limit detection

●TYPICAL OPERATING CHARACTERISTICS

※The test conditions for the Typical Operating Characteristics are IN=5V, CIN=1uF, COUT=0.1uF, Rok=100kΩ, Ta=25℃, Unless otherwise noted

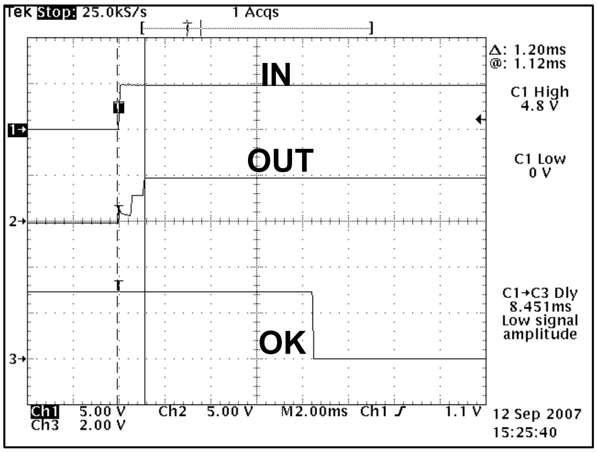


Figure 7. Start up（0→5V）

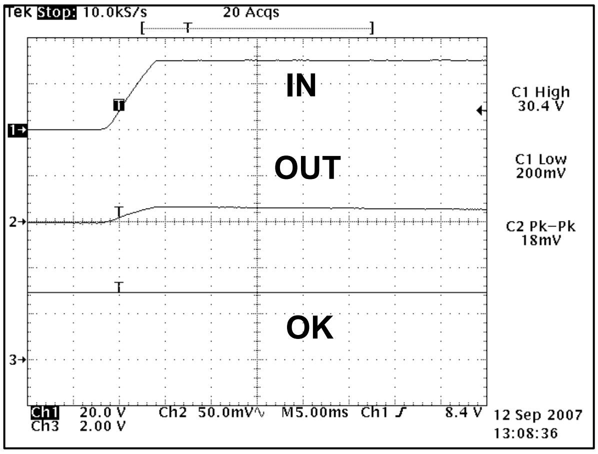


Figure 8. Input Steps（0→30V）

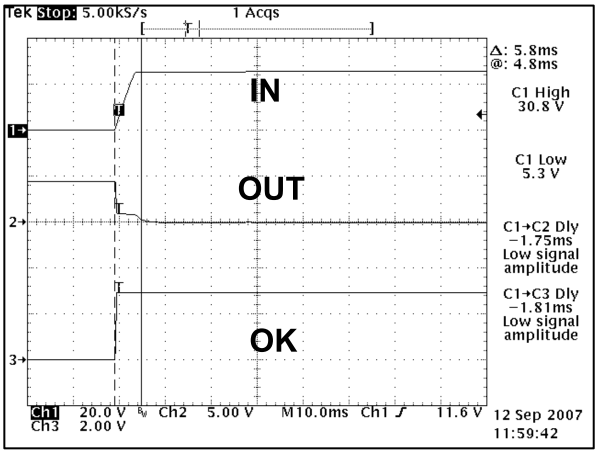


Figure9. Input Steps（5→30V）

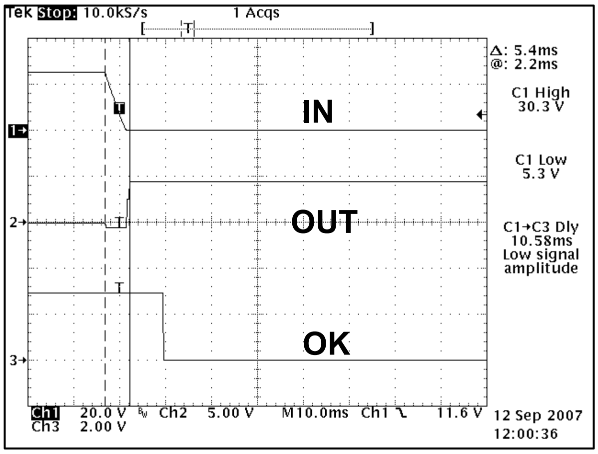


Figure 10. Input Steps（30→5V）

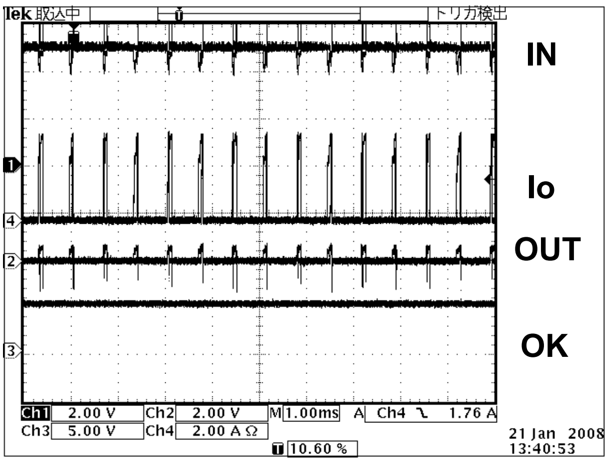


Figure 11. Output Short Circuit

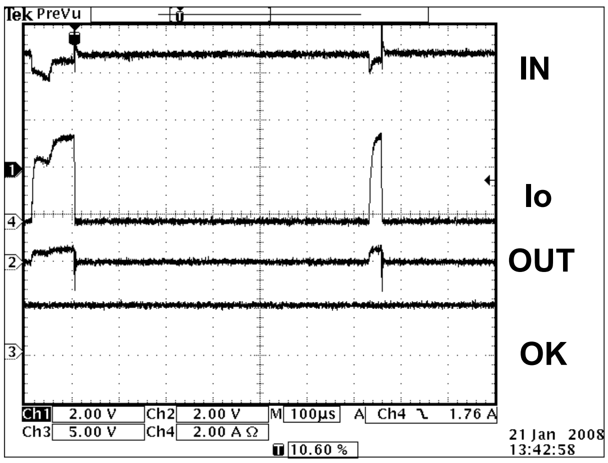


Figure 12. Output Short Circuit (Zoom)

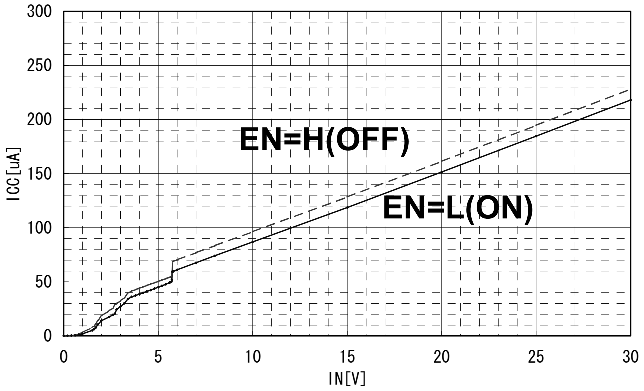


Figure 13. ICC vs. Input Voltage (0-30V)

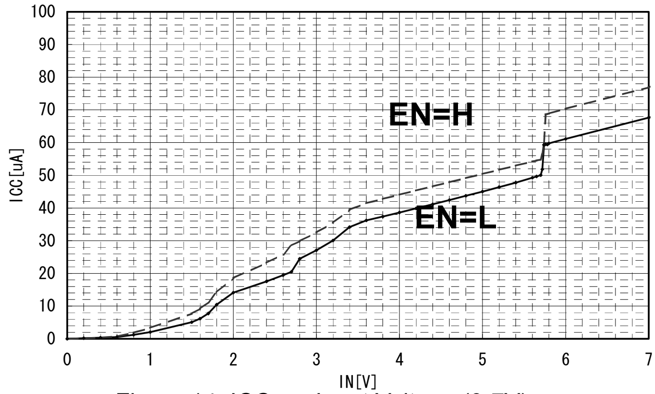


Figure 14. ICC vs. Input Voltage (0-7V)

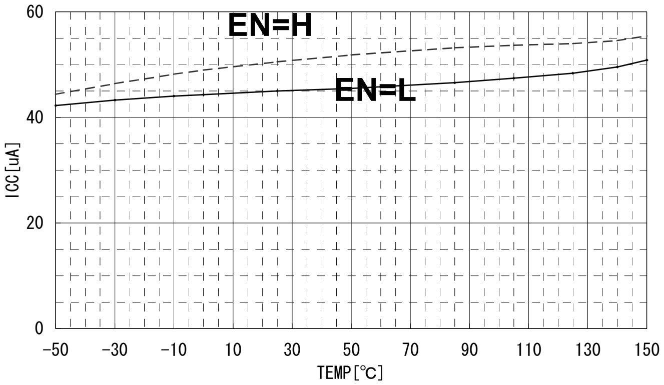


Figure 15. ICC vs. Temperature (IN=5V)

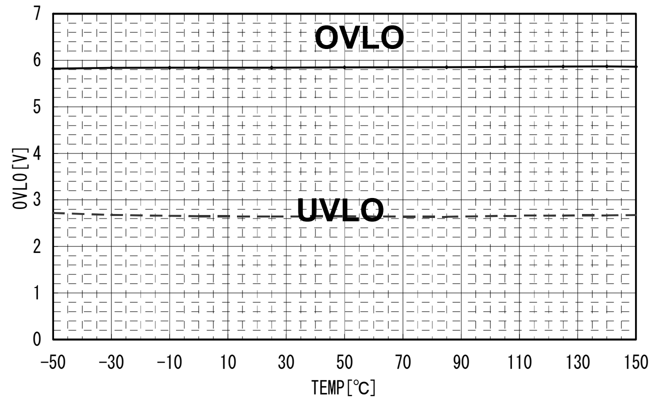


Figure 16. UVLO/OVLO vs. Temperature

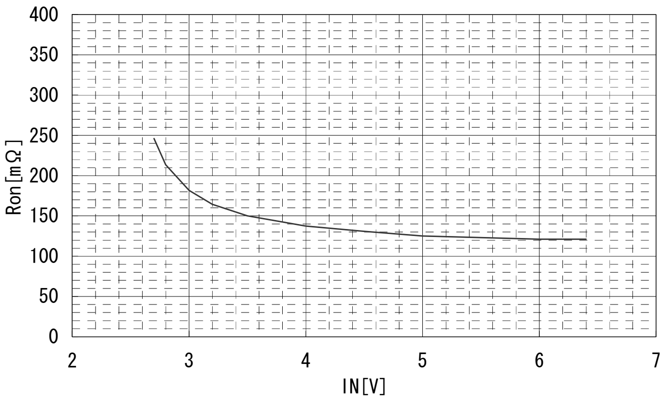


Figure 17. RON vs. Input Voltage

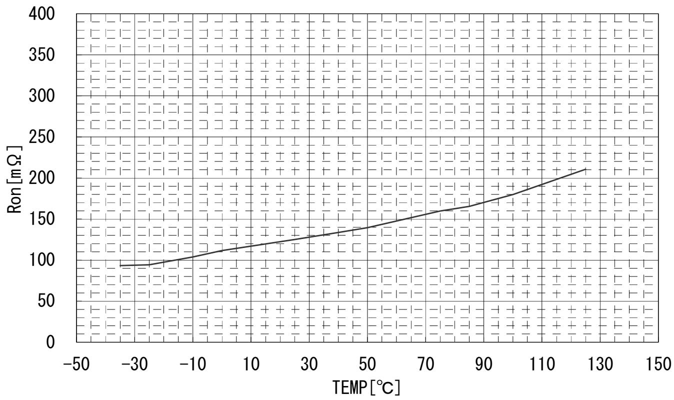
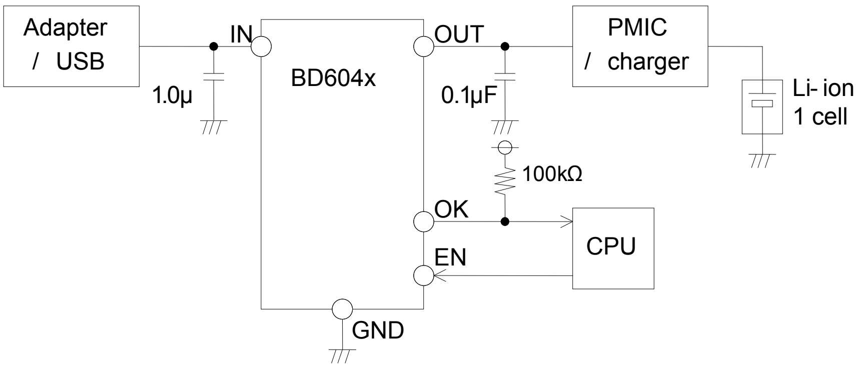
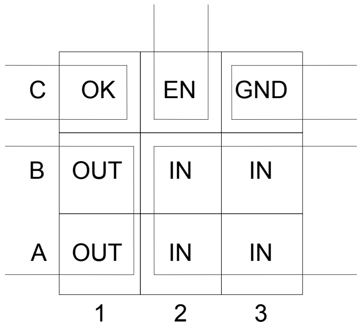


Figure 18. RON vs. Temperature (IN=5V)

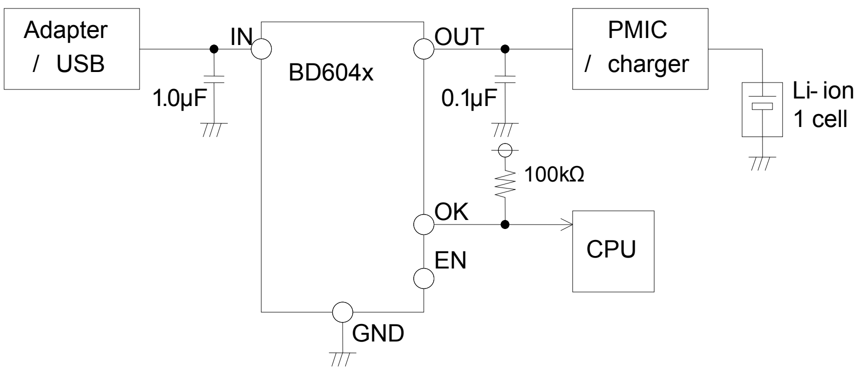
●EXAMPLES OF APPLICATION CIRCUIT (Ball Configuration is BOTTOM VIEW)

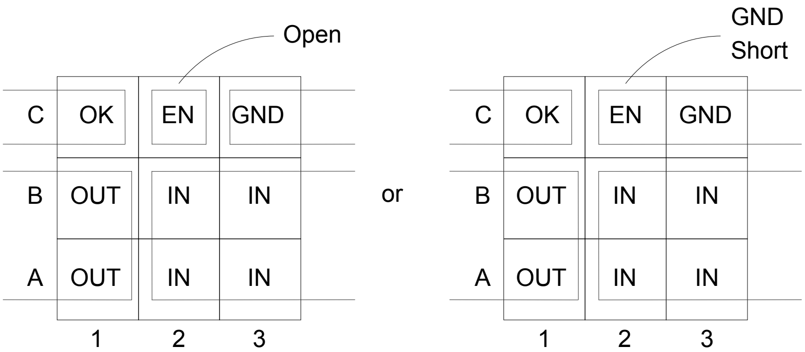
A: In case of both EN & OK pins are connected.



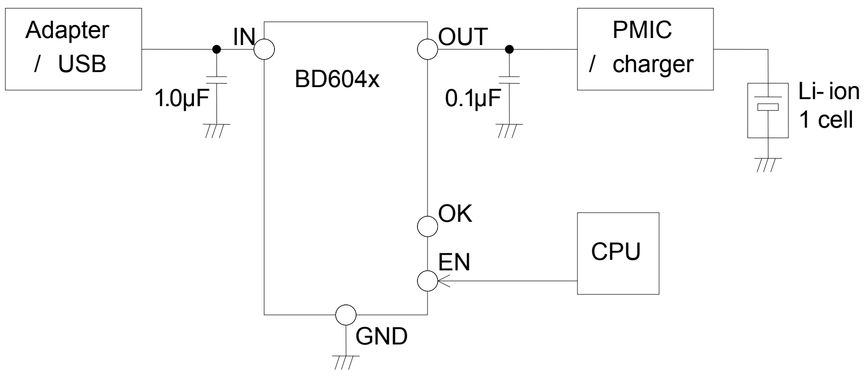


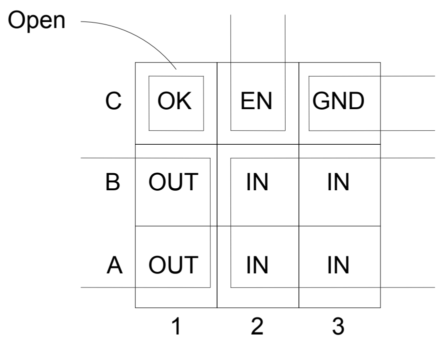
B: In case of OK pin is connected.



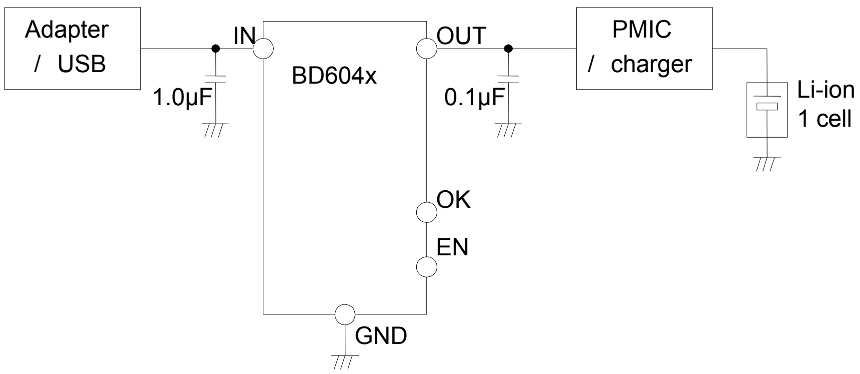


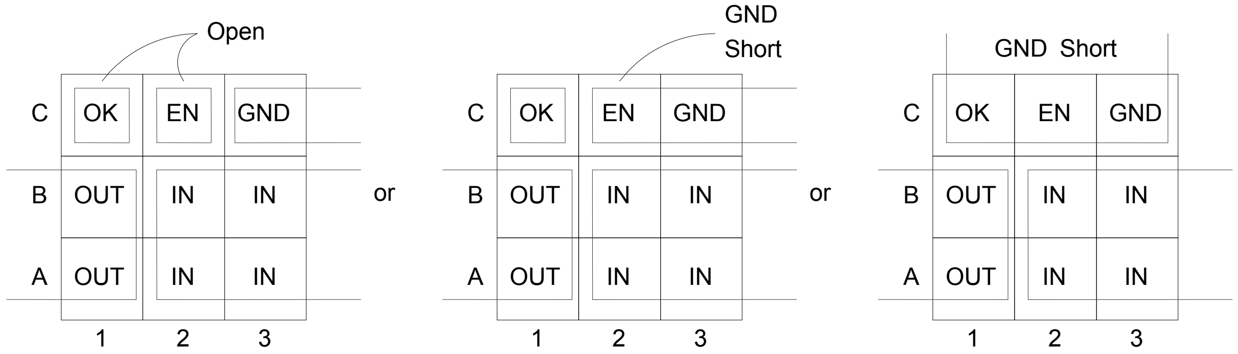
C: In case of EN pin is connected.





D: In case of both EN & OK pins are not connected.





●USE-RELATED CAUTIONS

(1) Absolute maximum ratings
If applied voltage (VDD, VIN), operating temperature range (Topr), or other absolute maximum ratings are exceeded, there is a risk of damage. Since it is not possible to identify short, open, or other damage modes, if special modes in which absolute maximum ratings are exceeded are assumed, consider applying fuses or other physical safety measures.

(2) Recommended operating range
This is the range within which it is possible to obtain roughly the expected characteristics. For electrical characteristics, it is those that are guaranteed under the conditions for each parameter. Even when these are within the recommended operating range, voltage and temperature characteristics are indicated.

(3) Reverse connection of power supply connector
There is a risk of damaging the LSI by reverse connection of the power supply connector. For protection from reverse connection, take measures such as externally placing a diode between the power supply and the power supply pin of the LSI.

(4) Power supply lines
In the design of the board pattern, make power supply and GND line wiring low impedance.

When doing so, although the digital power supply and analog power supply are the same potential, separate the digital power supply pattern and analog power supply pattern to deter digital noise from entering the analog power supply due to the common impedance of the wiring patterns. Similarly take pattern design into account for GND lines as well.

Furthermore, for all power supply pins of the LSI, in conjunction with inserting capacitors between power supply and GND pins, when using electrolytic capacitors, determine constants upon adequately confirming that capacitance loss occurring at low temperatures is not a problem for various characteristics of the capacitors used.

(5) GND voltage
Make the potential of a GND pin such that it will be the lowest potential even if operating below that. In addition, confirm that there are no pins for which the potential becomes less than a GND by actually including transition phenomena.

(6) Shorts between pins and misinstallation
When installing in the set board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is installed erroneously, there is a risk of LSI damage. There also is a risk of damage if it is shorted by a foreign substance getting between pins or between a pin and a power supply or GND.

(7) Operation in strong magnetic fields
Be careful when using the LSI in a strong magnetic field, since it may malfunction.

(8) Inspection in set board
When inspecting the LSI in the set board, since there is a risk of stress to the LSI when capacitors are connected to low impedance LSI pins, be sure to discharge for each process. Moreover, when getting it on and off of a jig in the inspection process, always connect it after turning off the power supply, perform the inspection, and remove it after turning off the power supply. Furthermore, as countermeasures against static electricity, use grounding in the assembly process and take appropriate care in transport and storage.

(9) Input pins
Parasitic elements inevitably are formed on an LSI structure due to potential relationships. Because parasitic elements operate, they give rise to interference with circuit operation and may be the cause of malfunctions as well as damage. Accordingly, take care not to apply a lower voltage than GND to an input pin or use the LSI in other ways such that parasitic elements operate. Moreover, do not apply a voltage to an input pin when the power supply voltage is not being applied to the LSI. Furthermore, when the power supply voltage is being applied, make each input pin a voltage less than the power supply voltage as well as within the guaranteed values of electrical characteristics.

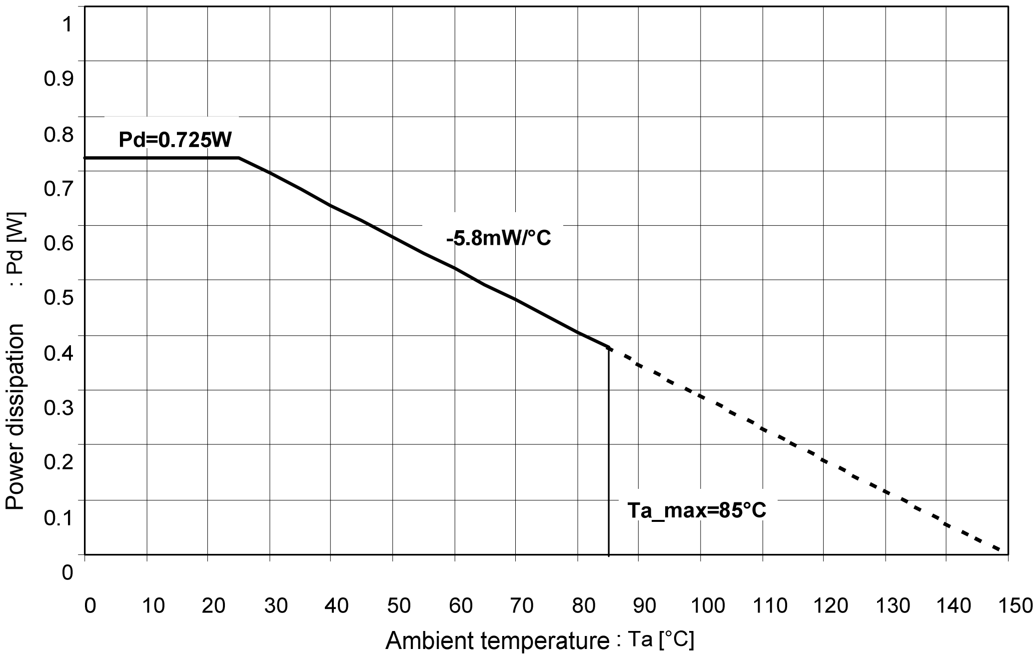
(10) Ground wiring pattern
When there is a small signal GND and a large current GND, it is recommended that you separate the large current GND pattern and small signal GND pattern and provide single point grounding at the reference point of the set so that voltage variation due to resistance components of the pattern wiring and large currents do not cause the small signal GND voltage to change. Take care that the GND wiring pattern of externally attached components also does not change.

(11) Externally attached capacitors
When using ceramic capacitors for externally attached capacitors, determine constants upon taking into account a lowering of the rated capacitance due to DC bias and capacitance change due to factors such as temperature.

(12) Thermal shutdown circuit (TSD)
When junction temperatures become 170°C (typ) or higher, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(13) Thermal design
Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

●POWER DISSIPATION



※ On the ROHM's specification Board

Figure19. Power dissipation vs. Ta

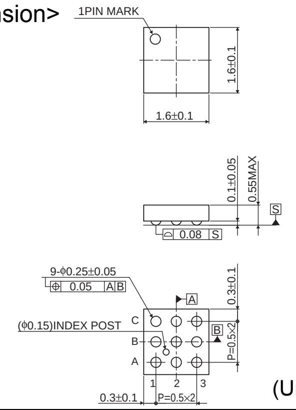
●Selection of order type

B	D		1	2	3	4		F	P	-	E	2

Part No.	Part No. BD6040 BD6041 BD6042	Package GUL : VCSP50L1	Packaging and forming specification E2: Embossed tape and reel

VCSP50L1 BD6040GUL, BD6041GUL, BD6042GUL

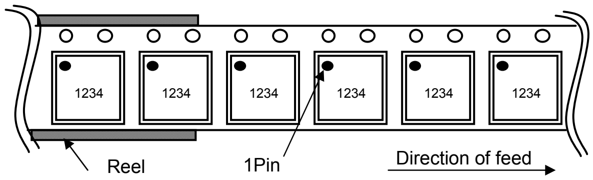
<Dimension>



(Unit:mm)

<Tape and Reel information>

Tape	Embossed carrier tape
Quantity	3000pcs
Direction of feed	E2 (The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand.)



※When you order , please order in times the amount of package quantity.

Notes

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