

Charge protection ICs with Built-in FET

Negative Voltage Protection type





BD6047AGUL

General Description

BD6047AGUL protects the devices from the abnormal input voltage at the USB port.

Addition to the conventinal charge protection IC, it prevents the negative voltage happened by

the USB reverse insertion without any additional compornents. ROHM's original charge protection IC series enables to protect the abnormal input voltage from -30V to +30V.

● Features

- Over Voltage Protection up to 30V
- Negative Voltage Protection down to -30V
- Over voltage Lockout (OVLO)
- Under voltage Lockout (UVLO)
- Over Current Protect
- Thermal Shut Down

Applications

Mobile phones, MP3 players, Digital Still Camera, PDA, IC recorder, Electronic Dictionary, Handheld Game, Game Controller, Camcorder, Bluetooth Headsets, etc

Key Specifications

Input voltage range:

Voltage Protection range:

Internal Low Ron:

Start Up Delay:

Operating temperature range:

2.2V to 28V

±30V

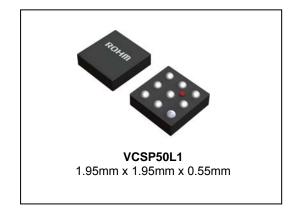
125mΩ(Typ.)

6.0msec(Typ.)

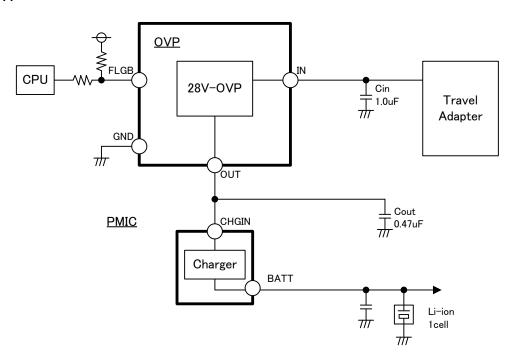
-40°C to +85°C

Package

W(Typ.) D(Typ.) H (Max.)

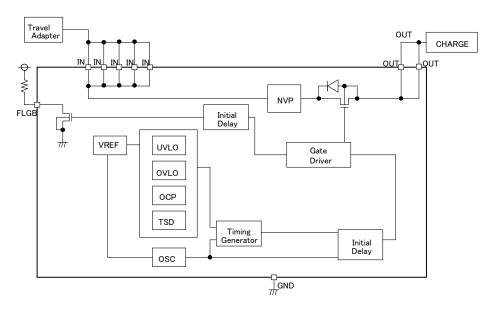


Typical Application Circuit

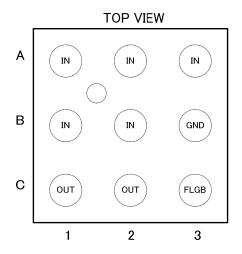


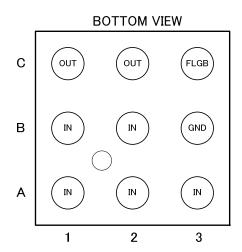
- Safety is high because it detects, and it protects it for an abnormal voltage up to ±30V.
- It contributes to the miniaturization because all external is built into.

Block Diagram



●Pin Configuration





●Pin Description

PIN	NAME	FUNCTION				
A1, A2, A3 B1, B2	IN	Input voltage Pin. A 1µF low ESR capacitor, or larger must be connected between this pin and GND				
C1, C2	OUT	Output Voltage Pin				
C3	FLGB	Open-drain output pin that turns low when any protection event occurs. (overvoltage protection, thermal shut down)				
В3	GND	Ground Pin				

● Absolute Maximum Ratings (Ta=25°C)

Contents	Symbol	Rating	Unit	Conditions
Input supply voltage 1	Vmax1	-30 to 30	٧	IN
Input supply voltage 2	Vmax2	-0.3 to 7	V	other
Power dissipation	Pd	900	mW	
Operating temperature range	Topr	-40 to +85	°C	
Storage temperature range	Tstr	-55 to +150	°C	

^{%1} When using more than at Ta=25°C, it is reduced 7.2mW per 1°C. ROHM specification board 50mm× 58mm mounting.

● Recommended Operating Ratings (Ta = -40°C to +85°C)

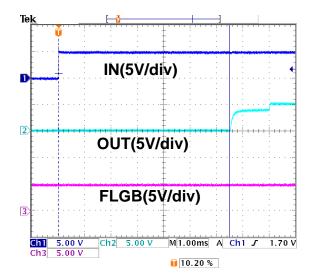
Parameter	Symbol	Range	Unit
Input voltage range	V _{in}	2.2 to 28	٧

● Electrical Characteristics

(Unless otherwise noted, Ta = 25°C, IN=5V)

Parameter	Symbol	Limit			Lloit	Conditions
Parameter		Min.	Тур.	Max.	Unit	Conditions
●ELECTRICAL						
Input Voltage Range	VIN	-	-	28	V	
Supply Quiescent Current	ICC	-	40	80	μA	
Under Voltage Lockout	UVLO	3.42	3.6	3.78	V	IN=decreasing
Under Voltage Lockout Hysteresis	UVLOh	50	100	150	mV	IN=increasing
Over Voltage Lockout	OVLO	5.7	5.85	6.0	V	IN=increasing
Over Voltage Lockout Hysteresis	OVLOh	50	100	150	mV	IN=decreasing
Current limit	ILM	1.7	-	-	Α	
Vin vs. Vout Res.	RON	-	125	150	mΩ	
FLGB Output Low Voltage	FLGBVO	-	-	400	mV	SINK=1mA
FLGB Leakage Current	FLGBleak	-	-	1	μA	
OUT pin input Current	OUTIIN	-	-	1	mA	IN=3V(UVLO), OUT=3V
●TIMINGS						
Start Up Delay	Ton	ı	6	10	msec	
Output Turn Off Time	Toff	-	2	10	µsec	
Alert Delay	Tovp	-	1.5	10	µsec	

●Typical Performance Curves



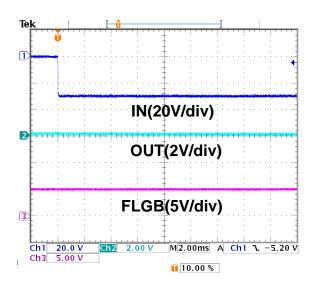
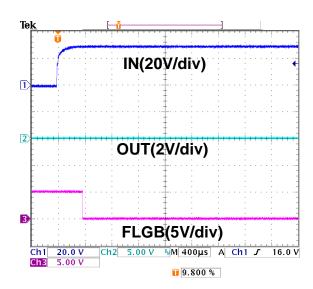


Figure 1. Start up (0→5V)

Figure 2. Input Steps (0→-30V)



IN(20V/div)

OUT(5V/div)

Ch1 20.0 V Ch2 S.00 V M2.00ms A Ch1 J 11.6 V 122.00 %

Figure 3. Input Steps (0→30V)

Figure 4. Input Steps (5→30V)

● Typical Performance Curves - continued

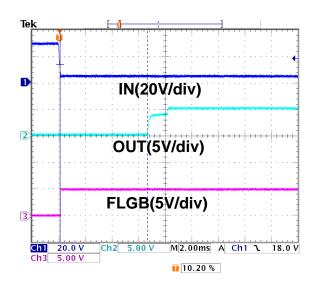


Figure 5. Input Steps (30→5V)

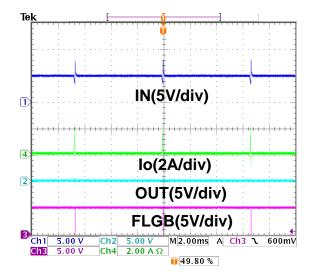


Figure 6. Output Short Circuit

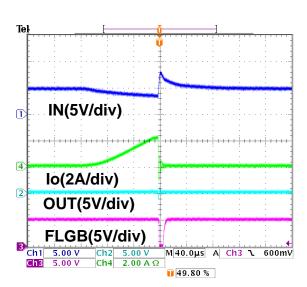
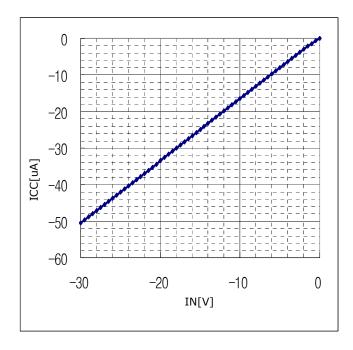


Figure 7. Output Short Circuit (Zoom)

● Typical Performance Curves - continued



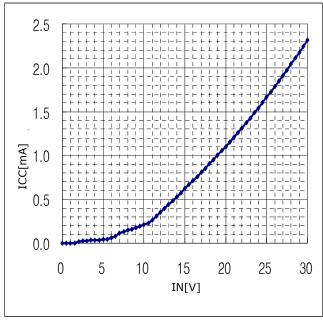
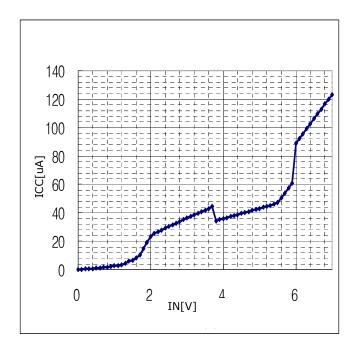


Figure 8. ICC vs Input Voltage (-30-0V)

Figure 9. ICC vs Input Voltage (0-30V)



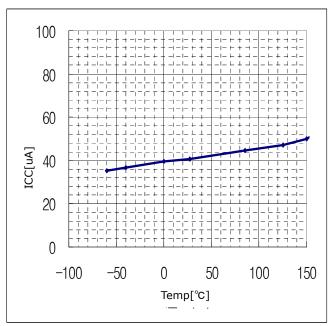
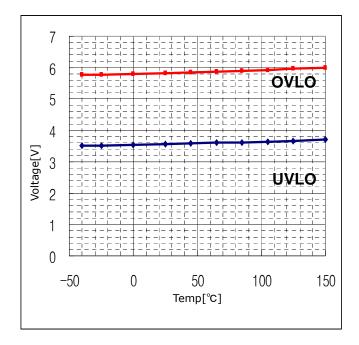


Figure 10. ICC vs Input Voltage (0-7V)

Figure 11. ICC vs Temperature (IN=5V)

● Typical Performance Curves - continued



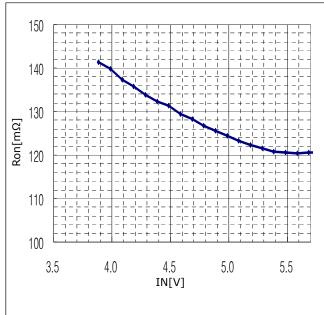


Figure 12. UVLO/OVLO vs Temperature

Figure 13. RON vs Input Voltage

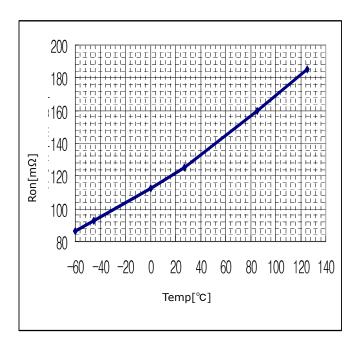


Figure 14. RON vs Temperature (IN=5V)

●Timing Diagram

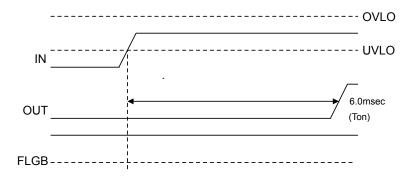


Figure 15. Start up sequence

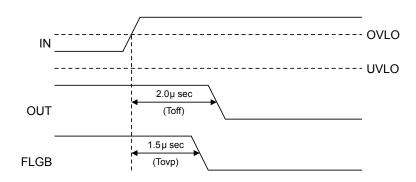


Figure 16. Shutdown by over voltage detection

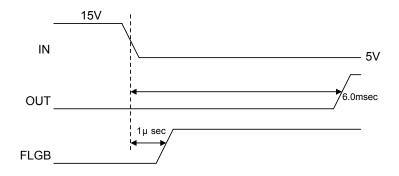
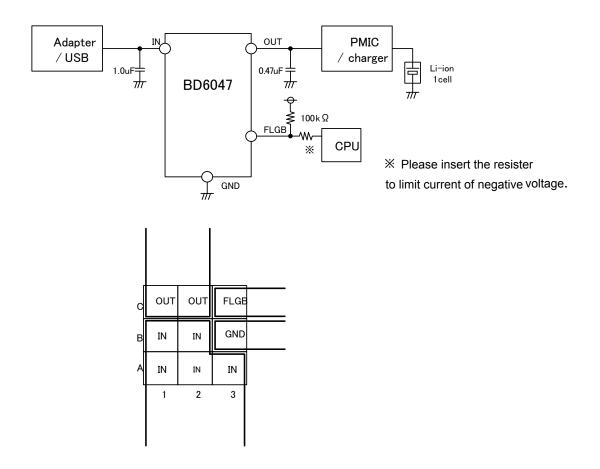


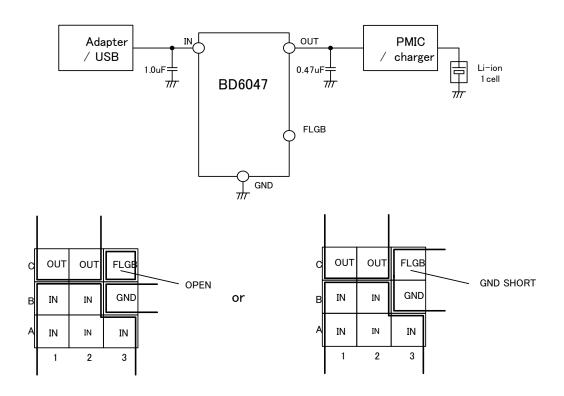
Figure 17. Recovery from overvoltage protection

● Examples of Application Circuit (Ball Configuration is Bottom View)

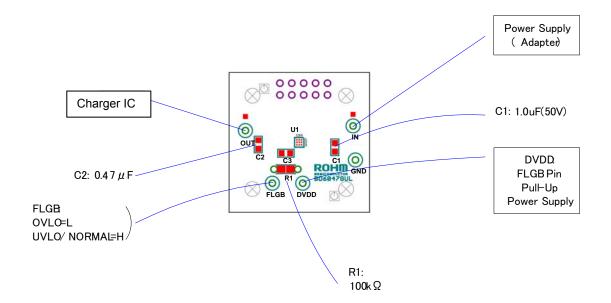
A: In case of FLGB pins are connected.

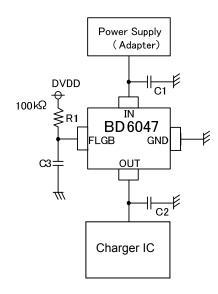


B: In case of FLGB pins are not connected.

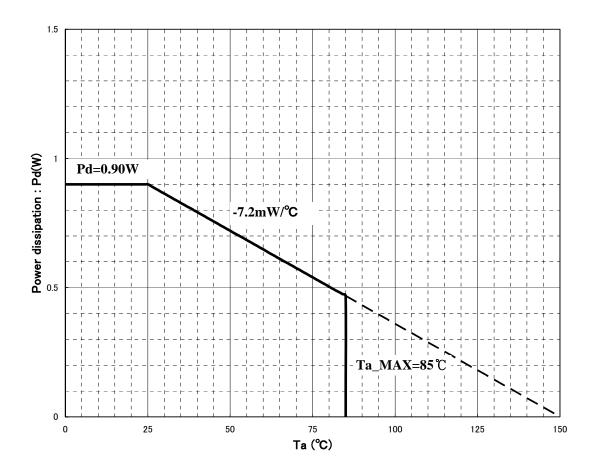


●BD6047 Evaluation Board



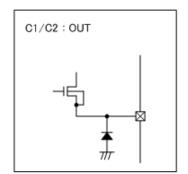


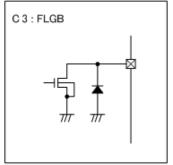
Power dissipation



※ On the ROHM's specification Board

●I/O equivalence circuit





Operational Notes

(1) Absolute maximum ratings

If applied voltage (VDD, VIN), operating temperature range (Topr), or other absolute maximum ratings are exceeded, there is a risk of damage. Since it is not possible to identify short, open, or other damage modes, if special modes in which absolute maximum ratings are exceeded are assumed, consider applying fuses or other physical safety measures.

(2) Recommended operating range

This is the range within which it is possible to obtain roughly the expected characteristics. For electrical characteristics, it is those that are guaranteed under the conditions for each parameter. Even when these are within the recommended operating range, voltage and temperature characteristics are indicated.

(3) Power supply lines

In the design of the board pattern, make power supply and GND line wiring low impedance.

When doing so, although the digital power supply and analog power supply are the same potential, separate the digital power supply pattern and analog power supply pattern to deter digital noise from entering the analog power supply due to the common impedance of the wiring patterns. Similarly take pattern design into account for GND lines as well.

Furthermore, for all power supply pins of the LSI, in conjunction with inserting capacitors between power supply and GND pins, when using electrolytic capacitors, determine constants upon adequately confirming that capacitance loss occurring at low temperatures is not a problem for various characteristics of the capacitors used.

(4) GND voltage

Make the potential of a GND pin such that it will be the lowest potential even if operating below that. In addition, confirm that there are no pins for which the potential becomes less than a GND by actually including transition phenomena.

(5) Shorts between pins and misinstallation

When installing in the set board, pay adequate attention to orientation and placement discrepancies of the LSI. If it is installed erroneously, there is a risk of LSI damage. There also is a risk of damage if it is shorted by a foreign substance getting between pins or between a pin and a power supply or GND.

(6) Operation in strong magnetic fields

Be careful when using the LSI in a strong magnetic field, since it may malfunction.

(7) Inspection in set board

When inspecting the LSI in the set board, since there is a risk of stress to the LSI when capacitors are connected to low impedance LSI pins, be sure to discharge for each process. Moreover, when getting it on and off of a jig in the inspection process, always connect it after turning off the power supply, perform the inspection, and remove it after turning off the power supply. Furthermore, as countermeasures against static electricity, use grounding in the assembly process and take appropriate care in transport and storage.

(8) Input pins

Parasitic elements inevitably are formed on an LSI structure due to potential relationships. Because parasitic elements operate, they give rise to interference with circuit operation and may be the cause of malfunctions as well as damage. Accordingly, take care not to apply a lower voltage than GND to an input pin or use the LSI in other ways such that parasitic elements operate. Moreover, do not apply a voltage to an input pin when the power supply voltage is not being applied to the LSI. Furthermore, when the power supply voltage is being applied, make each input pin a voltage less than the power supply voltage as well as within the guaranteed values of electrical characteristics.

(9) Ground wiring pattern

When there is a small signal GND and a large current GND, it is recommended that you separate the large current GND pattern and small signal GND pattern and provide single point grounding at the reference point of the set so that voltage variation due to resistance components of the pattern wiring and large currents do not cause the small signal GND voltage to change. Take care that the GND wiring pattern of externally attached components also does not change.

(10) Externally attached capacitors

When using ceramic capacitors for externally attached capacitors, determine constants upon taking into account a lowering of the rated capacitance due to DC bias and capacitance change due to factors such as temperature.

(11) Thermal shutdown circuit (TSD)

When the junction temperature reaches the defined value, the thermal shutdown circuit operates and turns a switch OFF. The thermal shutdown circuit, which is aimed at isolating the LSI from thermal runaway as much as possible, is not aimed at the protection or guarantee of the LSI. Therefore, do not continuously use the LSI with this circuit operating or use the LSI assuming its operation.

(12) Thermal design

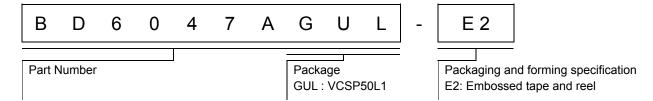
Perform thermal design in which there are adequate margins by taking into account the permissible dissipation (Pd) in actual states of use.

Status of this document

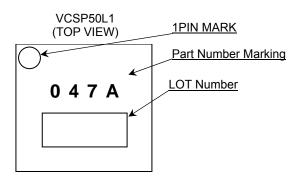
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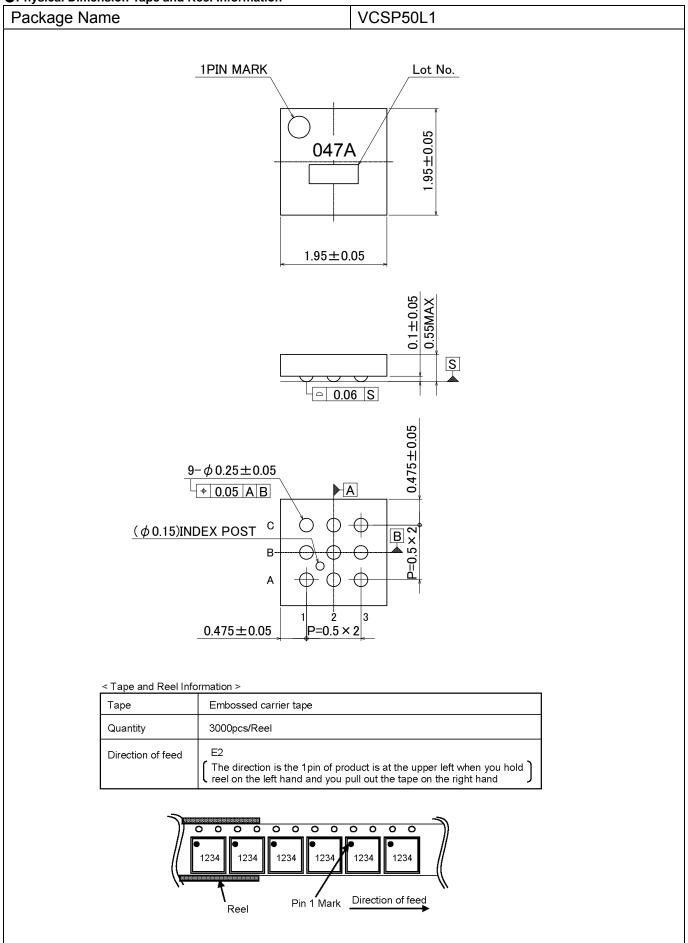
Ordering Information



Marking Diagram



●Physical Dimension Tape and Reel Information



Revision History

Date	Revision	Changes
21.May.2013	001	New Release

Notice

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