

Single-Output LDO Regulators

35V Withstand Voltage

1A LDO Regulators

BDxxFC0 series

●Description

The BDxxFC0 series are low-saturation regulators. The series' output voltages are Variable, 3.0V, 3.3V, 5.0V, 6.0V, 7.0V, 8.0V, 9.0V, 10.0V, 12.0V and 15.0V and packages are HTSOP-J8, TO252-3, and TO252-5. This series has a built-in over-current protection circuit that prevents the destruction of the IC due to output short circuits and a thermal shutdown circuit that protects the IC from thermal damage due to overloading.

●Key Specifications

- 1) Output current capability: 1A
- 2) Output voltage: Variable, 3.0V, 3.3V, 5.0V, 6.0V, 7.0V, 8.0V, 9.0V, 10.0V, 12.0V and 15.0V
- 3) High output voltage accuracy (Ta=25°C): ±1%
- 4) Low saturation with PDMOS output
- 5) Built-in over-current protection circuit that prevents the destruction of the IC due to output short circuits
- 6) Built-in thermal shutdown circuit for protecting the IC from thermal damage due to overloading
- 7) Available Ceramic Capacitor to prevent oscillation
- 8) HTSOP-J8, TO252-3 and TO252-5 packages

●Features

- Output Voltage: 1.0V to 15.0V
- Output Voltage Precision(Ta=25°C): ±1%
- Supply Voltage(Vo≥3.0V): Vo+1.0V to 26.5V
- Supply Voltage(Vo<3.0V): 4.0V to 26.5V
- Output Current: 1A
- Operating Temperature Range: -25°C≤Ta≤+85°C

●Ordering part number

B D x x F C 0 W x x x						-	E 2
Part Number	Output voltage 00: Variable 30: 3.0V 33: 3.3V 50: 5.0V 60: 6.0V 70: 7.0V 80: 8.0V 90: 9.0V J0: 10.0V J2: 12.0V J5: 15.0V	Input Voltage F:35V	Output Current C0:1.0A	Enable "W": Included Enable None: Without Enable	Package EFJ: HTSOP-J8 FP: TO252-3/5	Packaging and forming specification E2: Emboss tape reel	

●Packages

HTSOP-J8

(Typ) (Typ) (Max)
4.90mm x 6.00mm x 1.00mm



TO252-3

6.50mm x 9.50mm x 2.50mm



TO252-5

6.50mm x 9.50mm x 2.50mm



●Lineup

Articles	Variable	3.0	3.3	5.0	6.0	7.0	8.0	9.0	10.0	12.0	15.0	パッケージ	
BDxxFC0WEFJ-E2	○	○	○	○	○	○	○	○	○	○	○	HTSOP-J8	Reel of 2500
BDxxFC0FP-E2	-	-	○	○	-	-	-	-	-	-	-	TO252-3	Reel of 2000
BDxxFC0WFP-E2 ^(Note 1)	○	○	○	○	○	○	○	○	○	○	○	TO252-5	Reel of 2000

(Note 1) under development except for Variable

●Typical Application Circuits

〈Output Voltage Variable Type (With Enable)〉

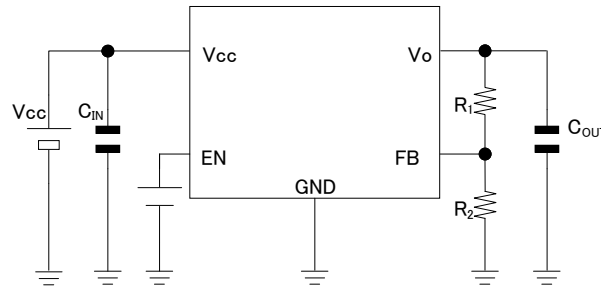


Figure 1. Typical Application Circuit Output Voltage Variable Type (With Enable)

〈Output Voltage Fixed Type (With Enable)〉

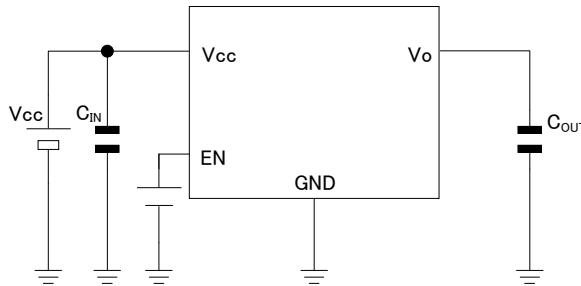


Figure 2. Typical Application Circuit Output Voltage Fixed Type (With Enable)

〈Output Voltage Fixed Type (Without Enable)〉

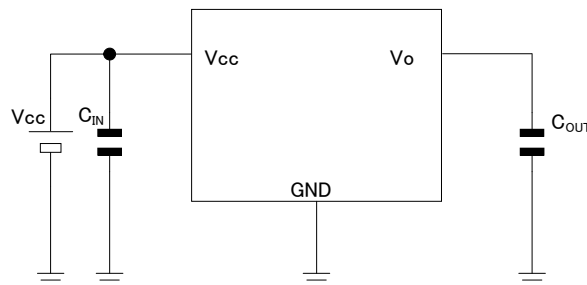


Figure 3. Typical Application Circuit Output Voltage Fixed Type (Without Enable)

●Pin Configuration/Pin Description

<With Enable (HTSOP-J8)>

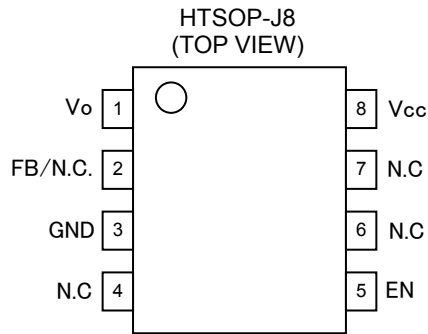


Figure 4. Pin Configuration (With Enable)

Pin No.	Pin name	Pin Function
1	Vo	Output pin
2	FB/N.C. (Note 1)	Feedback pin (Variable Output Type) No Connection (Fixed Output Type)
3	GND	GND pin
4	N.C. (Note 1)	No Connection (Connect to GND or leave OPEN)
5	EN	Enable pin
6	N.C. (Note 1)	No Connection (Connect to GND or leave OPEN)
7	N.C. (Note 1)	No Connection (Connect to GND or leave OPEN)
8	Vcc	Power supply pin
Exposed PAD	GND	Substrate(Connect to GND)

(Note 1) N.C. Pin can be open, because it is not connected to the IC.

<Without Enable (TO252-3)>

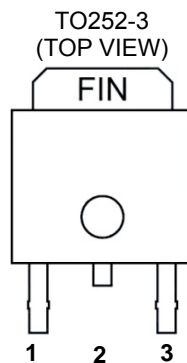


Figure 5. Pin Description (Without Enable)

Pin No.	Pin Name	Pin Function
1	Vcc	Power Supply Pin
2	N.C. (Note 1)	No Connection (leave OPEN)
3	Vo	Output Pin
FIN	GND	GND

(Note 1) N.C.Pin can be open since it is not connected inside of IC.

〈With Enable (TO252-5)〉

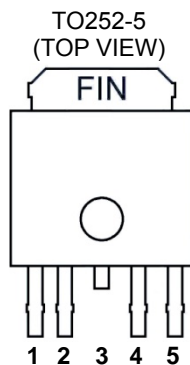


Figure 6. Pin Configuration (With Enable)

Pin No.	Pin Name	Pin Function
1	EN	Enable Pin
2	Vcc	Power Supply Pin
3	N.C. (Note 1)	No Connection (leave OPEN)
4	Vo	Output Pin
5	FB/N.C. (Note 1)	Variable Pin (Variable Output Type) N.C. Pin (Fixed Output Type)
FIN	GND	GND

(Note 1) N.C.Pin can be open since it is not connected inside of IC.

●Block diagrams

■ HTSOP-J8 <BD00FC0WEFJ (Output Voltage Variable Type) with Enable>

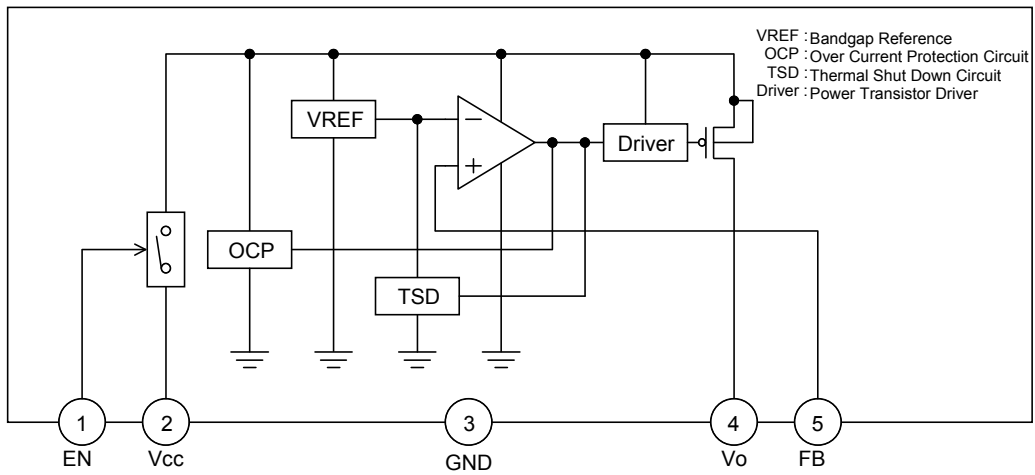


Figure 7. Block diagrams
 BD00FC0WEFJ (Output Voltage Variable Type with Enable)

■ HTSOP-J8 <BDxxFC0WEFJ (Output Voltage Fixed Type) with Enable>

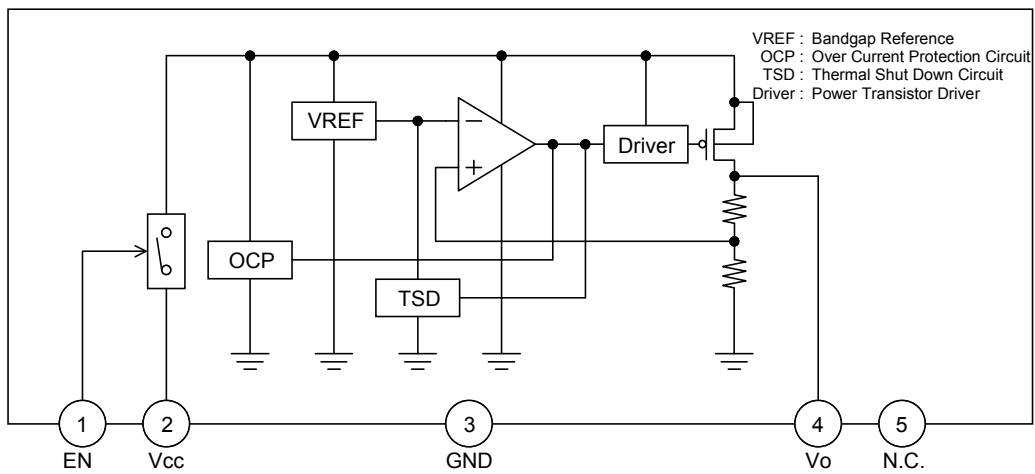


Figure 8. Block diagrams
 BxxFC0WEFJ (Output Voltage Variable Type with Enable)

■ TO252-3 (BDxxFC0FP (Output Voltage Fixed Type) without Enable)

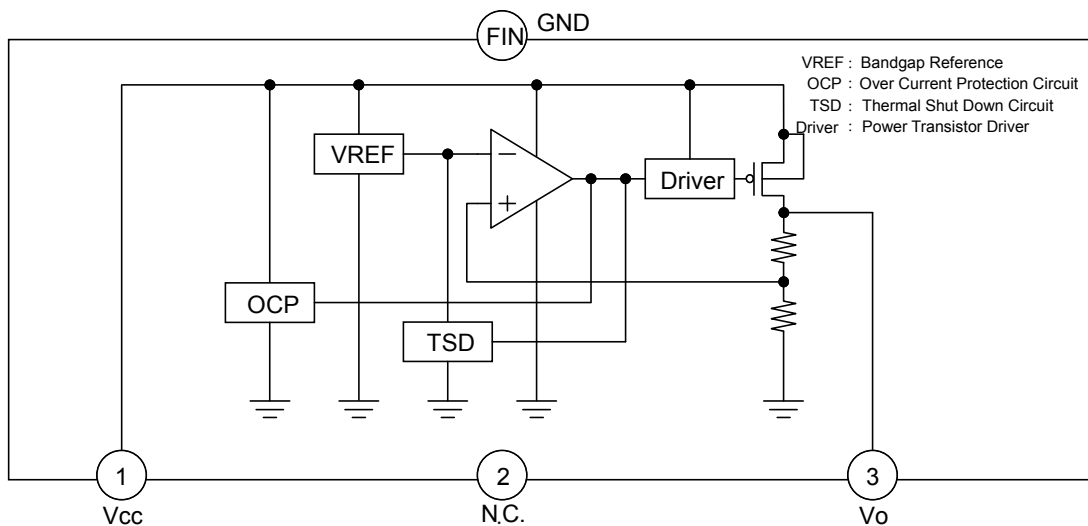


Figure 9. Block diagrams
BDxxFC0FP (Output Voltage Fixed Type, without Enable)

■ TO252-5 〈BD00FC0WFP (Output Voltage Variable Type) With Enable〉

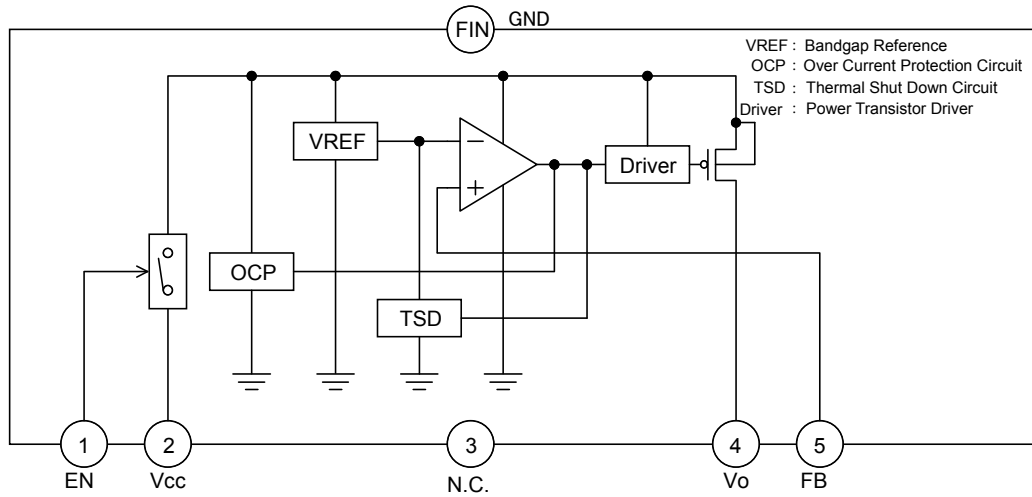


Figure 10. Block diagram
 BD00FC0WFP (Output Voltage Variable Type, with Enable)

■ TO252-5 〈BDxxFC0WFP (Output Voltage Fixed Type) With Enable〉

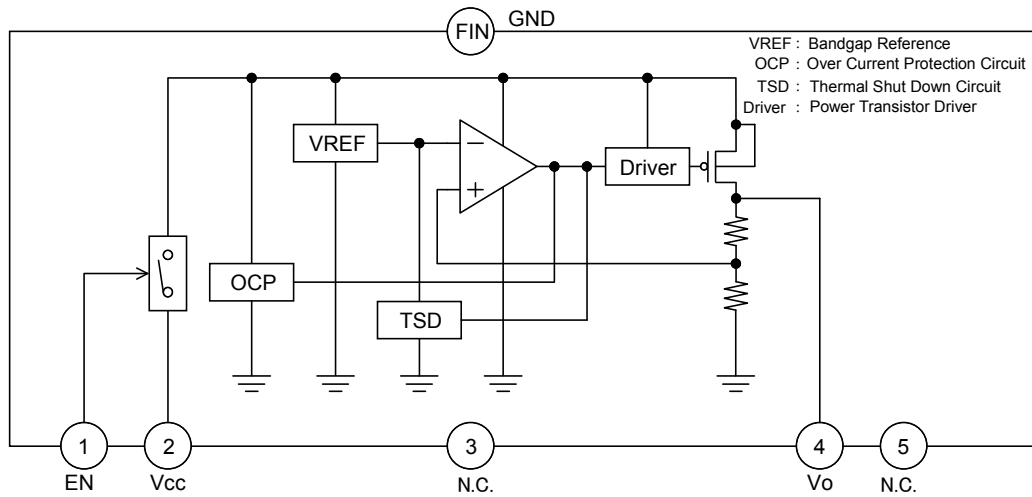


Figure 11. Block diagram
 BDxxFC0WFP (Output Voltage Fixed Type, with Enable)

●Absolute Maximum Ratings (Ta= 25°C)

Parameter	Symbol	Ratings	Unit
Supply Voltage *1	Vcc	-0.3 to +35.0	V
EN Voltage *2	V _{EN}	-0.3 to +35.0	V
Operating Temperature Range	Ta	-25 to +85	°C
Storage Temperature Range	Tstg	-55 to +150	°C
Maximum Junction Temperature	Tjmax	150	°C

*1 Do not exceed Tjmax.

*2 Power Supply (Vcc) and EN pin startup sequence does not matter provided they are operated within the power supply voltage range.

●Operating Conditions (-25°C ≤ Ta ≤ +85°C)

Parameter	Symbol	Min	Max	Unit
Supply Voltage (Vo ≥ 3.0V)	Vcc	Vo+1	26.5	V
Supply Voltage (Vo < 3.0V)	Vcc	4.0	26.5	V
Startup Voltage (Io=0mA)	Vcc	-	3.8	V
EN Voltage (with shutdown ENABLE)	V _{EN}	0	26.5	V
Output Current	Io	0	1.0	A
Output Voltage *3 (BD00FC0)	Vo	1.0	15.0	V

*3 Please refer to Notes when using BD00FC0W at output voltage of 1.0V to 3.0V.

●Electrical Characteristics

Unless otherwise specified, Ta=25°C, Vcc=13.5V, Io=0mA, V_{EN}=5.0V

The resistor between FB and OUT =56.7kΩ, FB and GND =10kΩ (BD00FC0)

Parameter	Symbol	Guaranteed Limit			Unit	Conditions
		Min	Typ	Max		
Circuit Current at shutdown mode	I _{SD}	-	0	5	μA	V _{EN} =0V
Circuit Current	I _{CC}	-	0.5	2.5	mA	
Output Reference Voltage (BD00FC0)	V _{FB}	0.742	0.750	0.758	V	Io =50mA
Output Voltage (BD30/33/50FC0)	Vo	Vo×0.99	Vo	Vo×1.01	V	Io =200mA
Output Voltage (BD60/70/80/90/J0/J2/J5FC0)	Vo	Vo×0.99	Vo	Vo×1.01	V	Io =500mA *4
Minimum dropout voltage	ΔVd	-	0.4	0.7	V	Vcc=4.0V Io =500mA *5
Minimum dropout voltage (BD00/50/60/70/80/90/J0/J2/J5FC0)	ΔVd	-	0.3	0.5	V	Vcc= Vo×0.95, Io =500mA
Line Regulation	Reg.l	-	20	80	mV	Vcc=Vo+1.0V→26.5V
Load Regulation	Reg.Io	-	Vo×0.010	Vo×0.020	V	Io =5mA→1A *4
EN High Voltage (with Enable)	V _{EN(High)}	2.0	-	-	V	ACTIVE MODE
EN Low Voltage (with Enable)	V _{EN(Low)}	-	-	0.8	V	OFF MODE
EN Bias Current (with Enable)	I _{EN}	-	25	50	μA	

*4 In case of J0, J2 and J5, Vcc=Vo+4.5V

*5 In case of Vo ≥ 4.0V

●Thermal Resistance

Parameter	Symbol	Thermal Resistance (Typ)		Unit
		1s ^(Note 3)	2s2p ^(Note 4)	
HTSOP-J8				
Junction to Ambient	θ_{JA}	206.4	45.2	°C/W
Junction to Top Characterization Parameter ^(Note 2)	Ψ_{JT}	21	13	°C/W
TO252-5 / TO252-3				
Junction to Ambient	θ_{JA}	115.3	20.8	°C/W
Junction to Top Characterization Parameter ^(Note 2)	Ψ_{JT}	14	3	°C/W

(Note 1)Based on JESD51-2A(Still-Air)

(Note 2)The thermal characterization parameter to report the difference between junction temperature and the temperature at the top center of the outside surface of the component package.

(Note 3)Using a PCB board based on JESD51-3.

Layer Number of Measurement Board	Material	Board Size
Single	FR-4	114.3mm x 76.2mm x 1.57mmt
Top		
Copper Pattern	Thickness	
Footprints and Traces	70 μ m	

(Note 4)Using a PCB board based on JESD51-5, 7.

Layer Number of Measurement Board	Material	Board Size	Thermal Via ^(Note 5)		
			Pitch	Diameter	
4 Layers	FR-4	114.3mm x 76.2mm x 1.6mmt	1.20mm	Φ 0.30mm	
Top		2 Internal Layers		Bottom	
Copper Pattern	Thickness	Copper Pattern	Thickness	Copper Pattern	Thickness
Footprints and Traces	70 μ m	74.2mm x 74.2mm	35 μ m	74.2mm x 74.2mm	70 μ m

(Note 5) This thermal via connects with the copper pattern of all layers. The placement and dimensions obey a land pattern.

●Reference Data

■BD00FC0 series (5.0V Output Setting)

Unless otherwise specified, $T_a=25^{\circ}\text{C}$, $V_{CC}=13.5\text{V}$, $V_{EN}=5.0\text{V}$, $I_o=0\text{mA}$, $V_o=5.0\text{V}$
 (The resistor between FB and $V_o=56.7\text{k}\Omega$, FB and GND = $10\text{k}\Omega$)

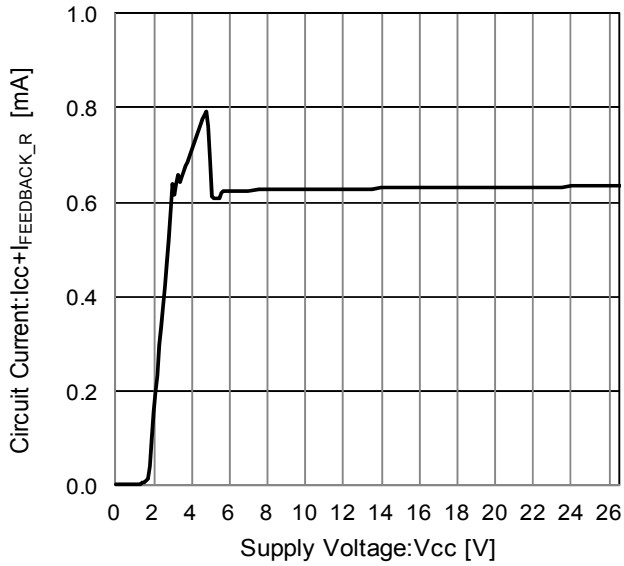


Figure 12. Circuit Current
 ($I_{FEEDBACK_R}(\text{Note 1}) \cong 75\mu\text{A}$)
 (Note 1) $I_{FEEDBACK_R}$ is the current through external Feed Back resistor.

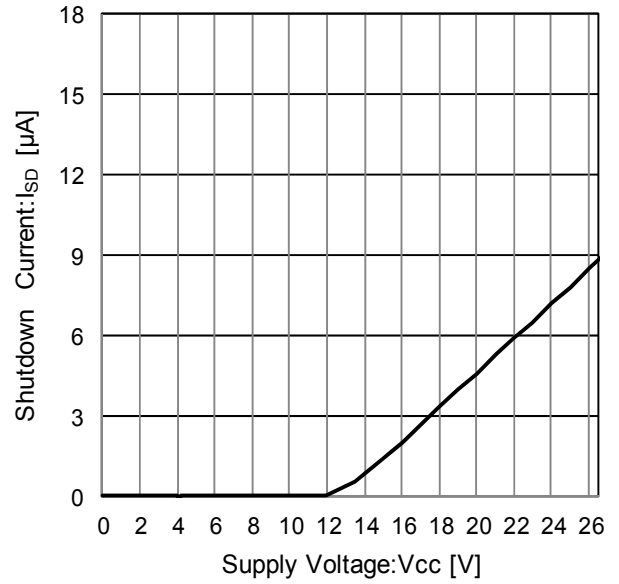


Figure 13. Shutdown Current
 ($V_{EN}=0\text{V}$)

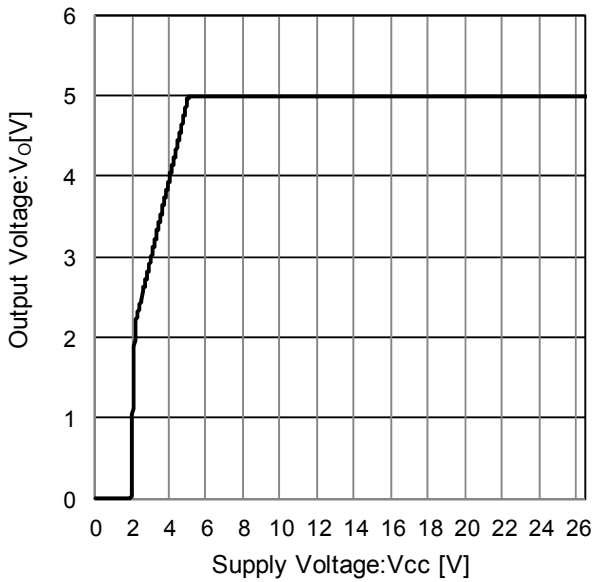


Figure 14. Line Regulation
 ($I_o=0\text{mA}$)

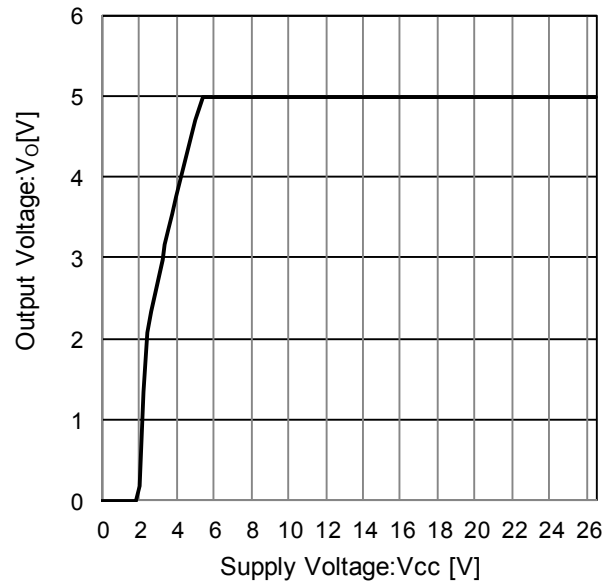


Figure 15. Line Regulation
 ($I_o=500\text{mA}$)

●Reference Data - Continued

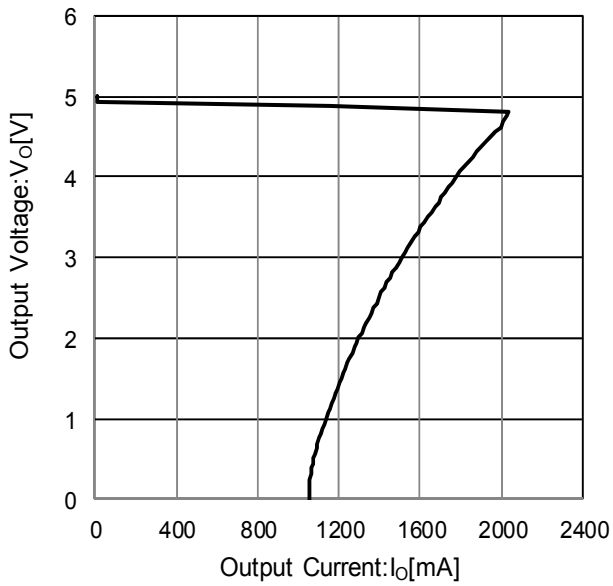


Figure 16. Load Regulation

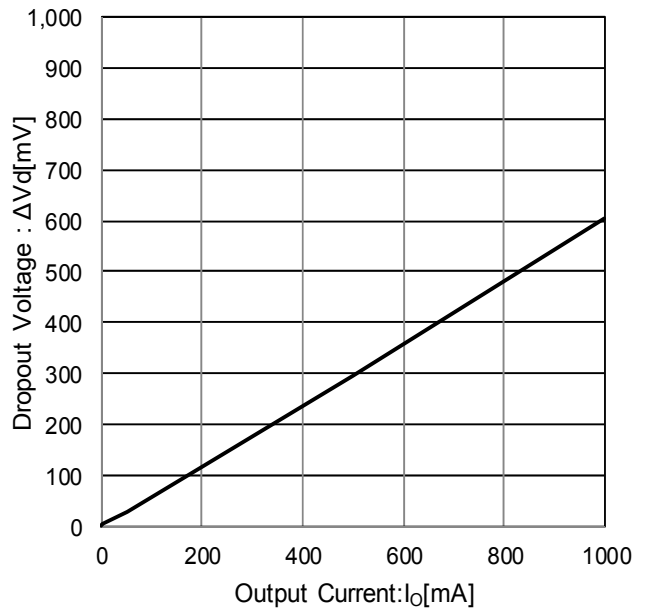


Figure 17. Dropout Voltage
($V_{cc}=4.75V$)
($I_o=0mA \rightarrow 1000mA$)

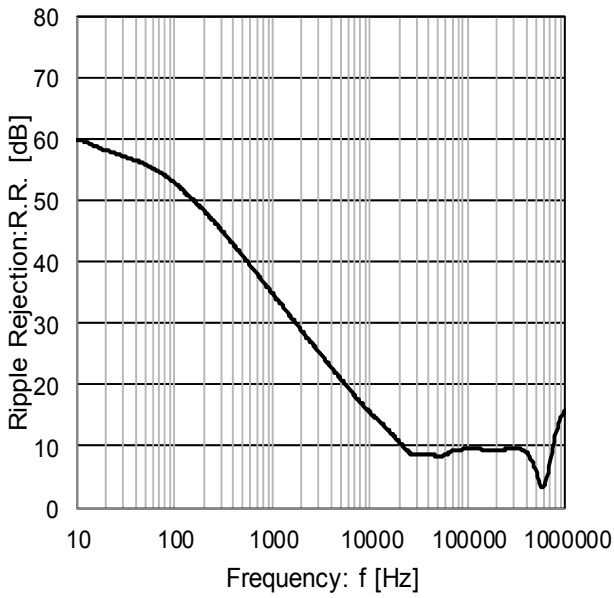


Figure 18. Ripple Rejection
($I_o = 100mA$)

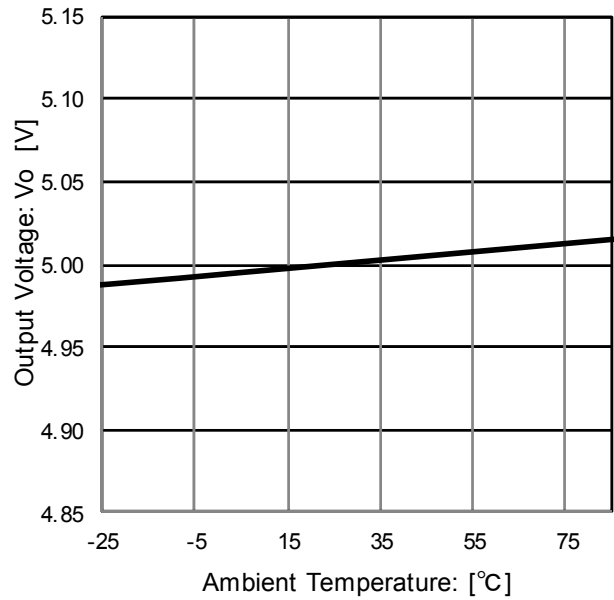


Figure 19. Output Voltage
Temperature Characteristic

●Reference Data - Continued

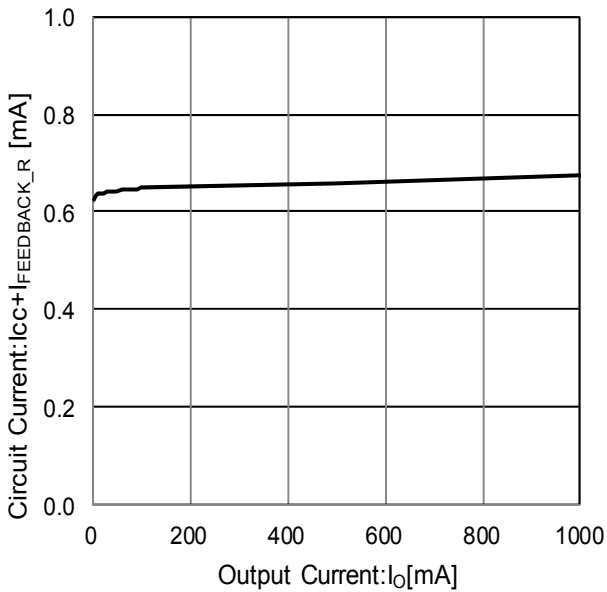


Figure 20. Circuit Current vs Output Current
($I_o = 0\text{mA} \rightarrow 1000\text{ mA}$)
($I_{FEEDBACK_R} \cong 75\mu\text{A}$)

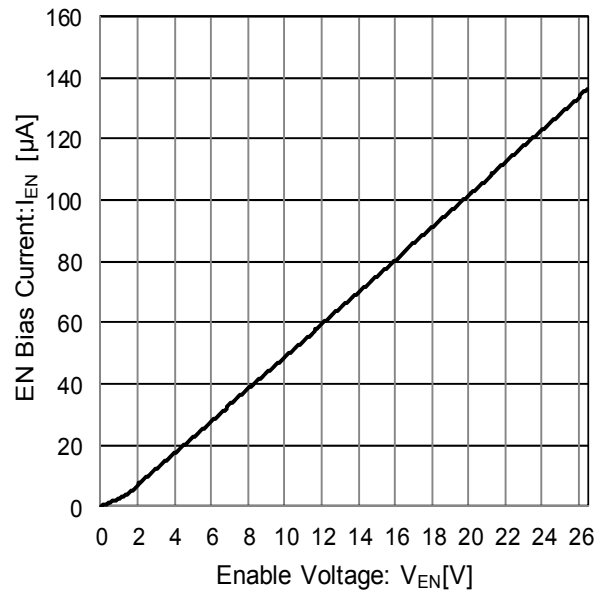


Figure 21. EN Voltage vs EN Current

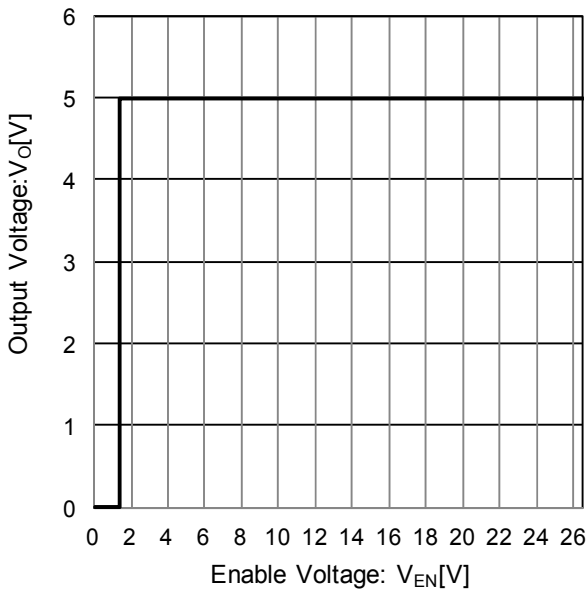


Figure 22. EN Voltage vs Output Voltage

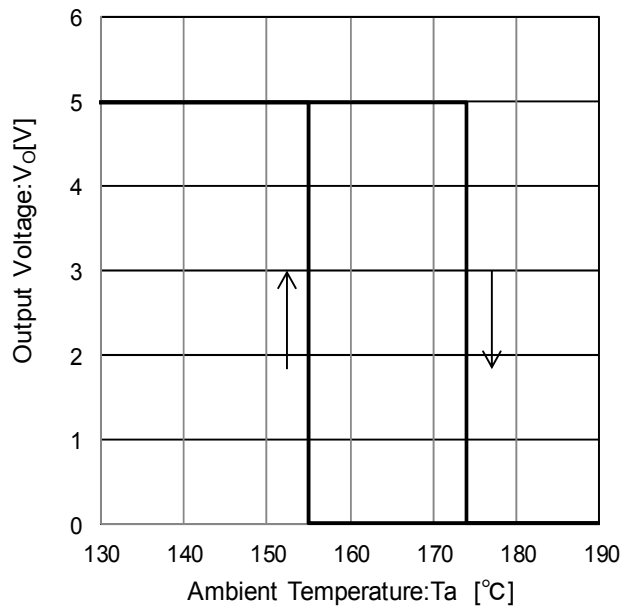
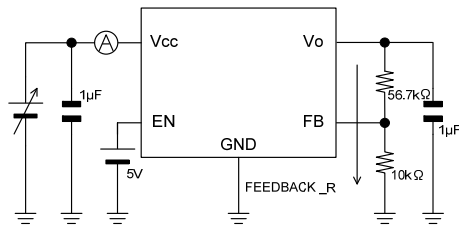


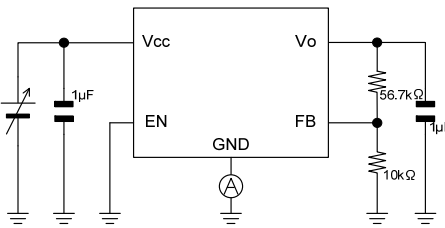
Figure 23. Thermal Shutdown
Circuit Characteristic

● Measurement setup for reference data

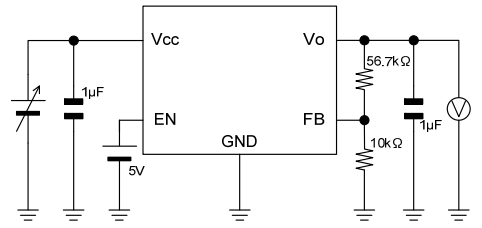
■ BD00FC0 series (5.0V Output Setting)



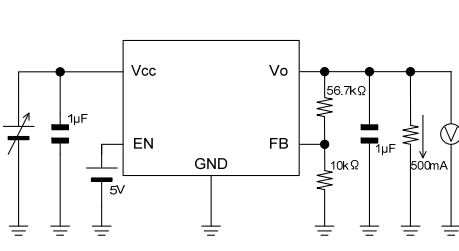
Measurement setup for Figure 12



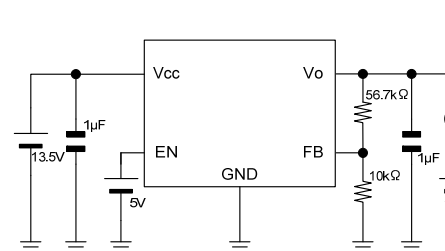
Measurement setup for Figure 13



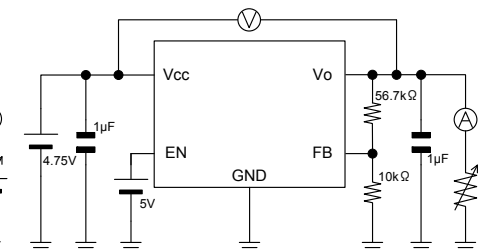
Measurement setup for Figure 14



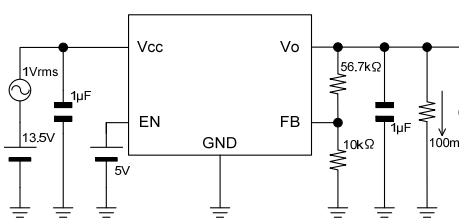
Measurement setup for Figure 15



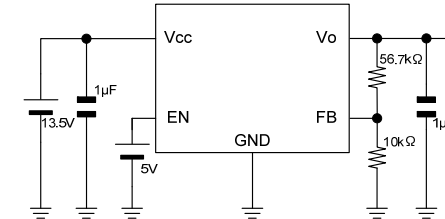
Measurement setup for Figure 16



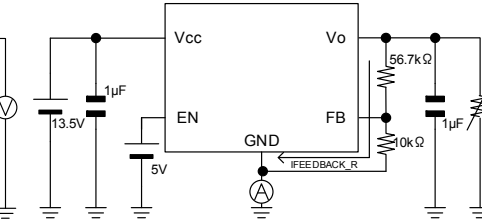
Measurement setup for Figure 17



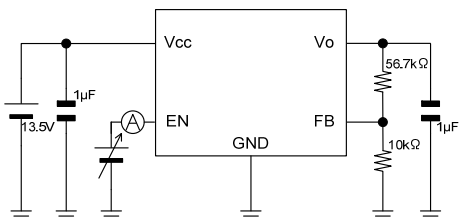
Measurement setup for Figure 18



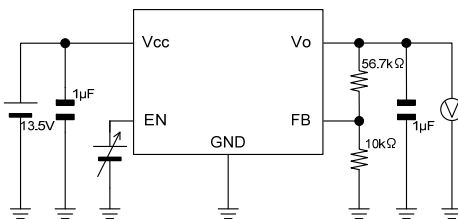
Measurement setup for Figure 19



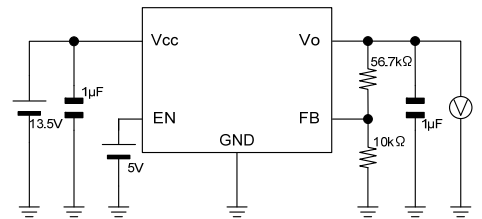
Measurement setup for Figure 20



Measurement setup for Figure 21



Measurement setup for Figure 22



Measurement setup for Figure 23

● Reference Data

■ BD33FC0 series

Unless otherwise specified $T_a = 25^\circ\text{C}$, $V_{CC}=13.5\text{V}$, $V_{EN}=5.0\text{V}$, $I_o=0\text{mA}$

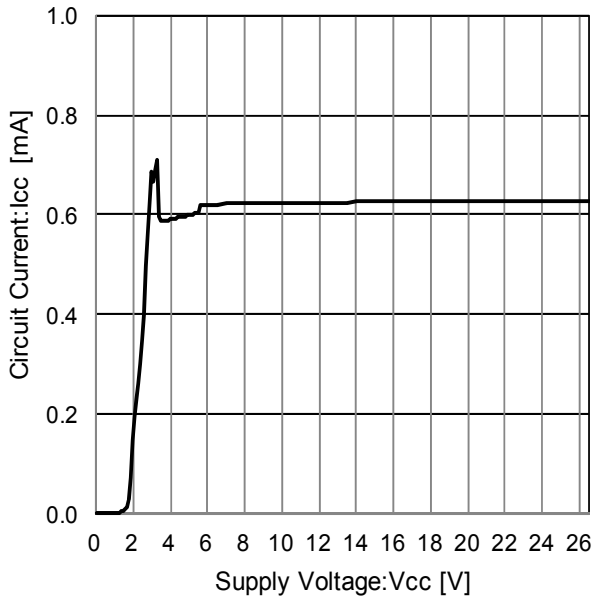


Figure 24. Circuit Current

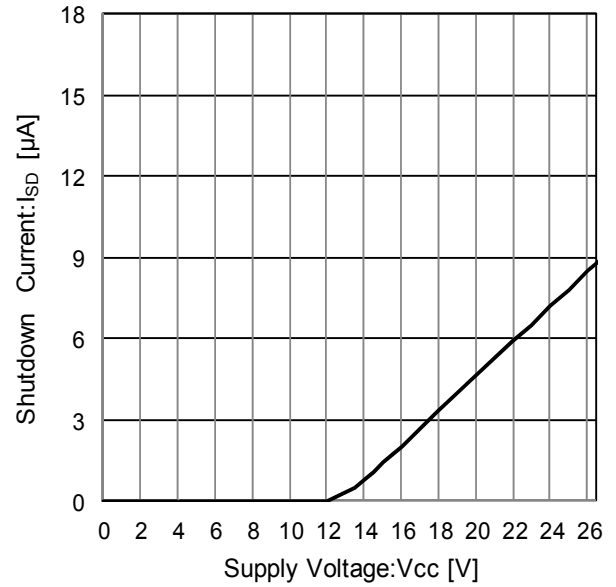


Figure 25. Shutdown Current ($V_{EN}=0\text{V}$)

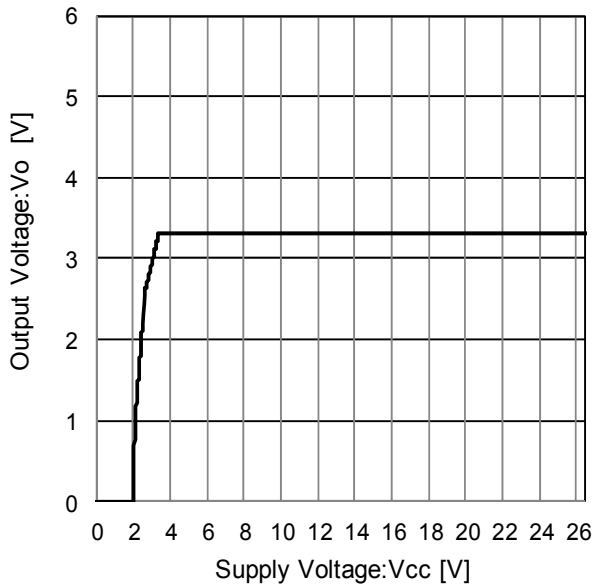


Figure 26. Line Regulation ($I_o=0\text{mA}$)

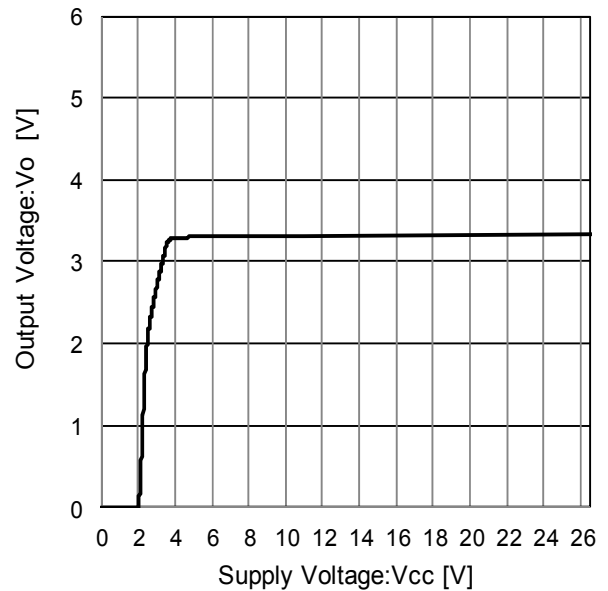


Figure 27. Line Regulation ($I_o=500\text{mA}$)

●Reference Data - Continued

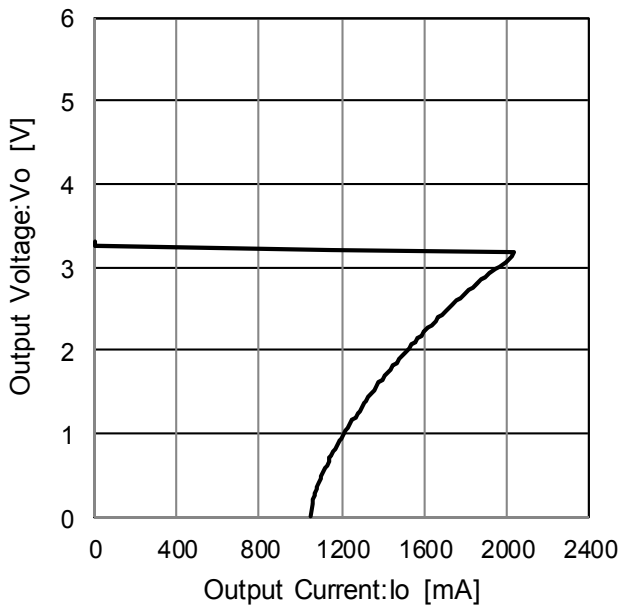


Figure 28. Load Regulation

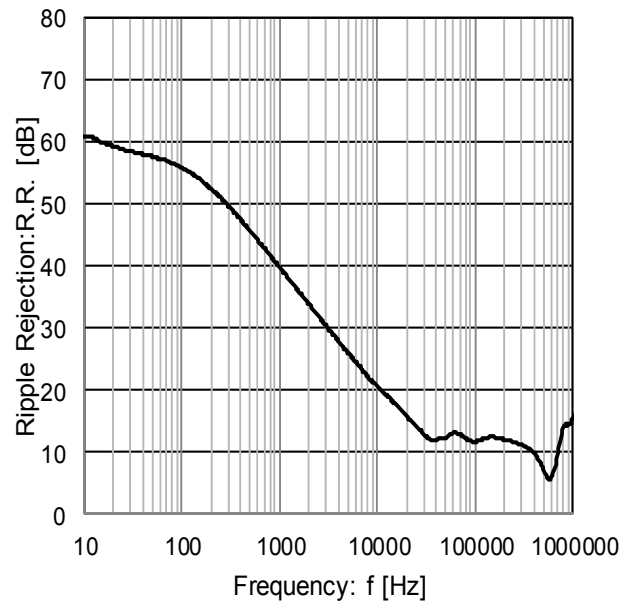


Figure 29. Ripple Rejection ($I_o=100\text{mA}$)

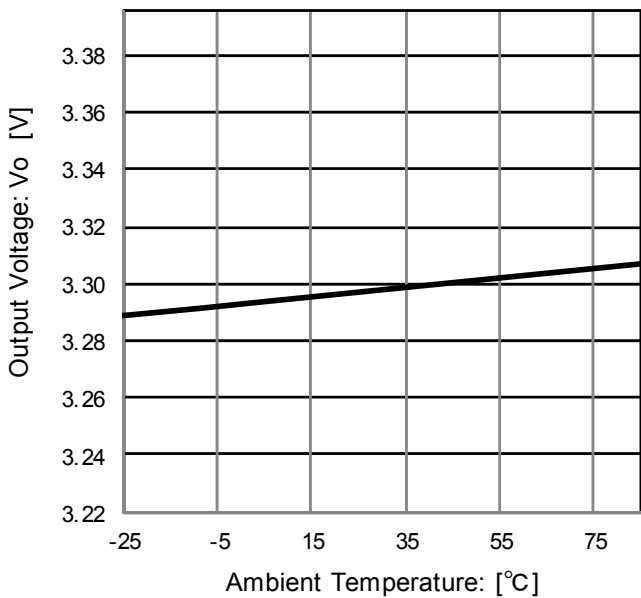


Figure 30. Output Voltage Temperature Characteristic

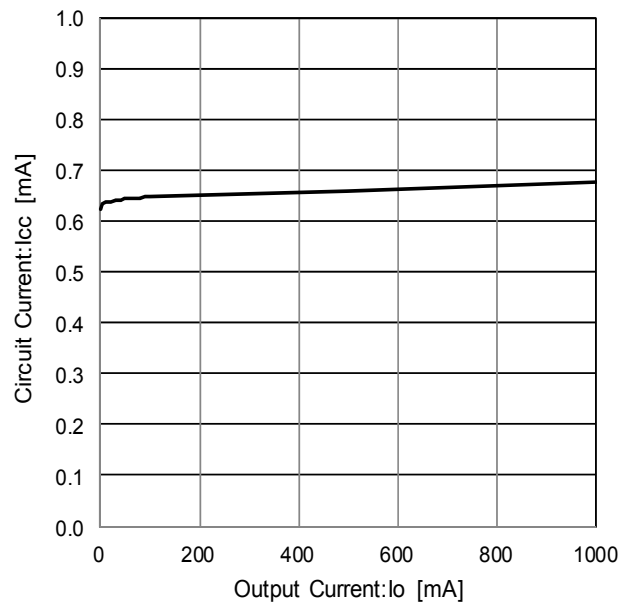


Figure 31. Circuit Current vs Output Current ($I_o = 0\text{mA} \rightarrow 1000\text{mA}$)

●Reference Data - Continued

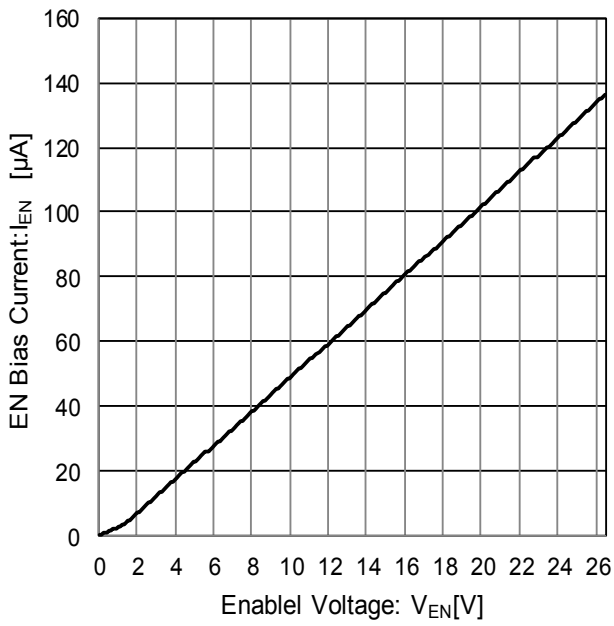


Figure 32. EN Voltage vs EN Current

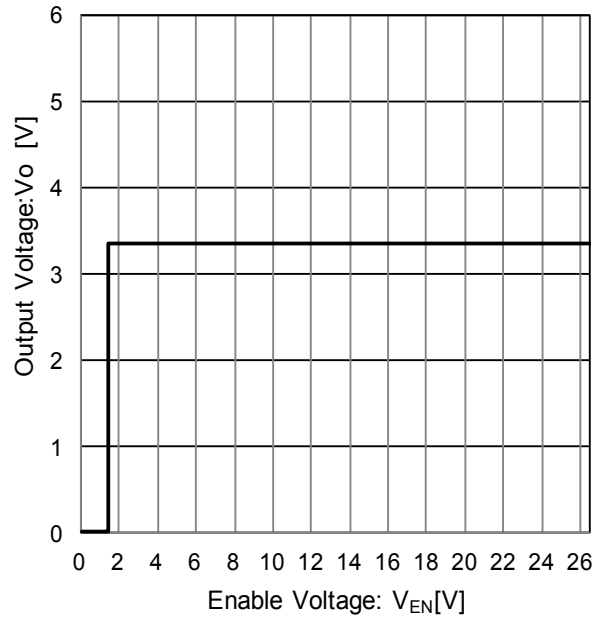


Figure 33. EN Voltage vs Output Voltage

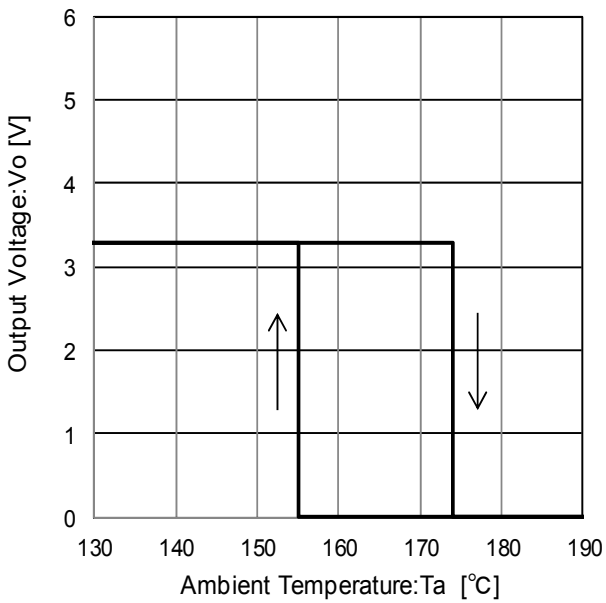


Figure 34. Thermal Shutdown Circuit Characteristic

●Reference Data

■BD50FC0 series

Unless otherwise specified, Ta = 25°C, Vcc=13.5V, VEN=5.0V, Io=0mA

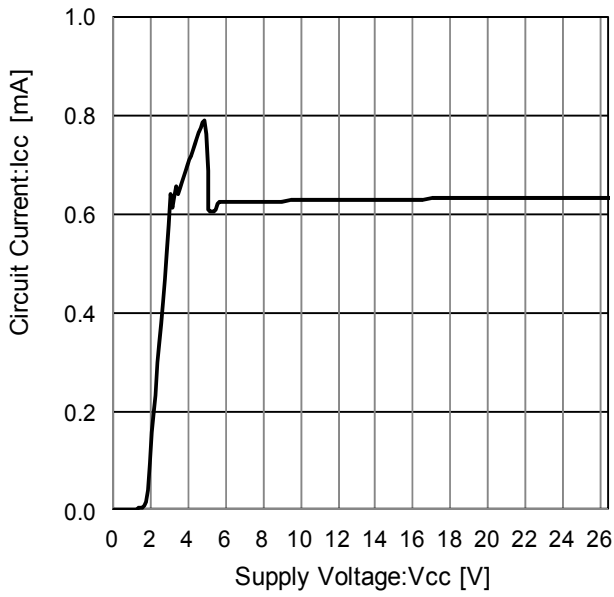


Figure 35. Circuit Current

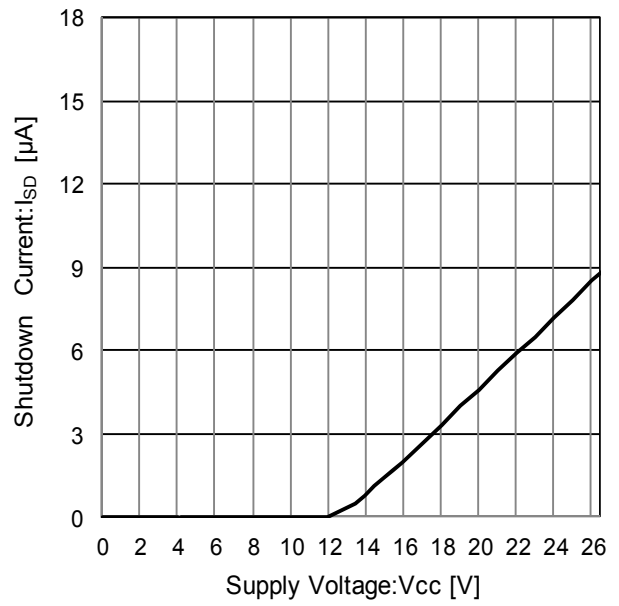


Figure 36. Shutdown Current (VEN=0V)

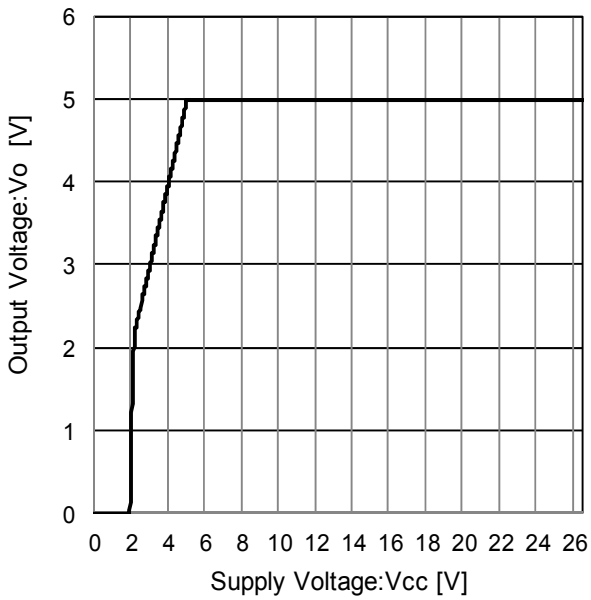


Figure 37. Line Regulation (Io=0mA)

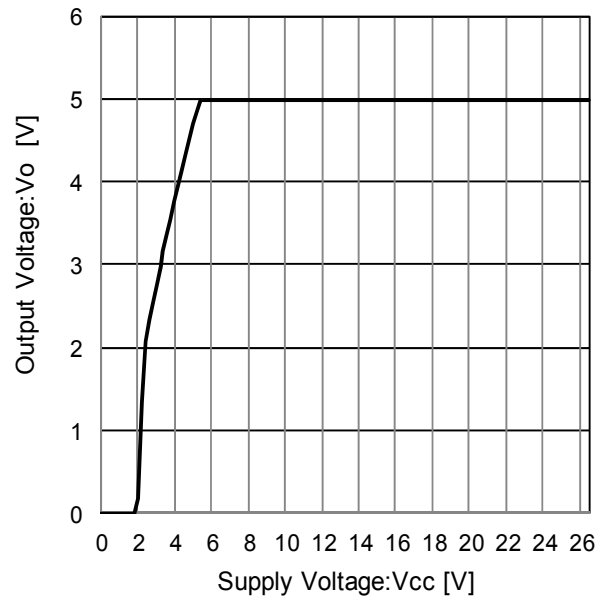


Figure 38. Line Regulation (Io=500mA)

●Reference Data - Continued

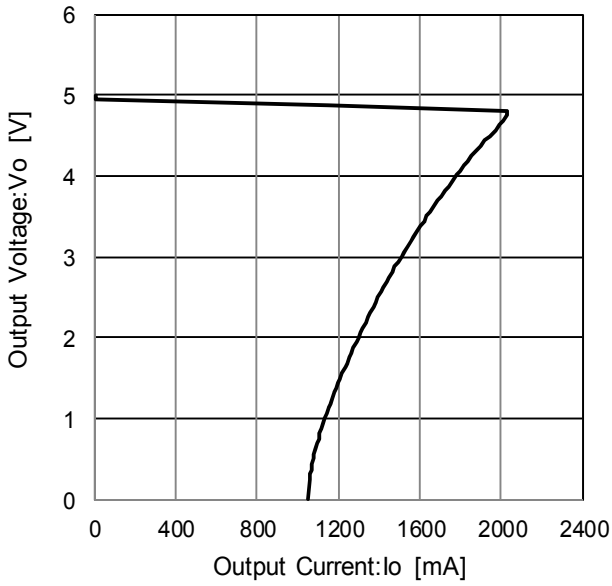


Figure 39. Load Regulation

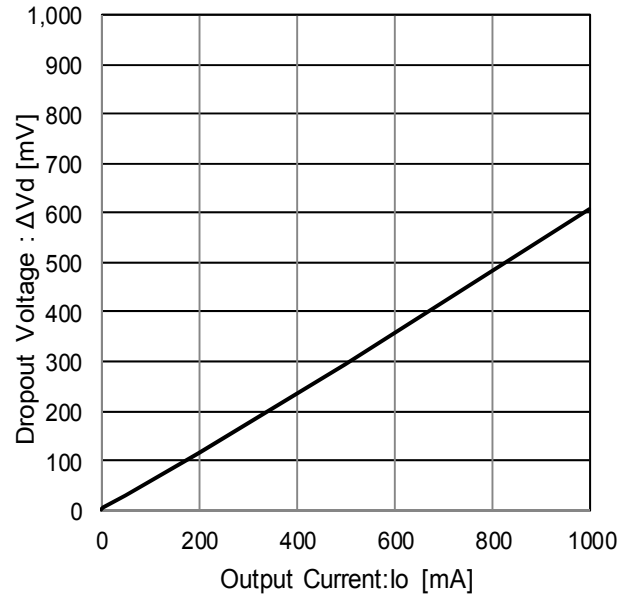


Figure 40. Dropout Voltage
($V_{cc}=V_o \times 0.95=4.75V$)

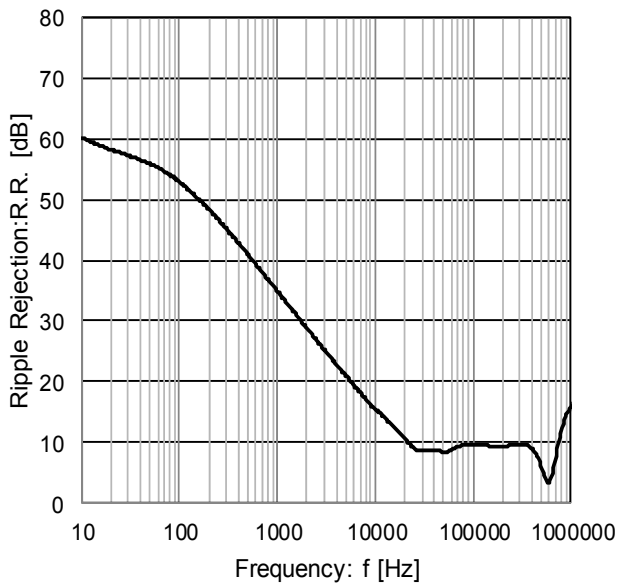


Figure 41. Ripple Rejection
($I_o=100mA$)

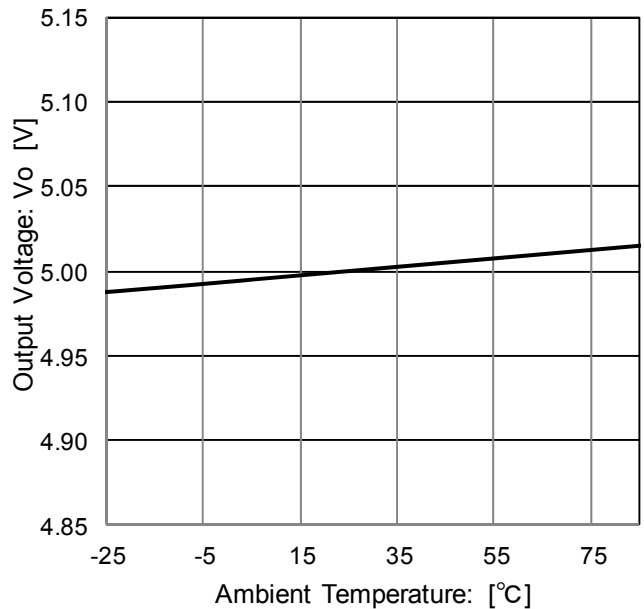


Figure 42. Output Voltage
Temperature Characteristic

●Reference Data - Continued

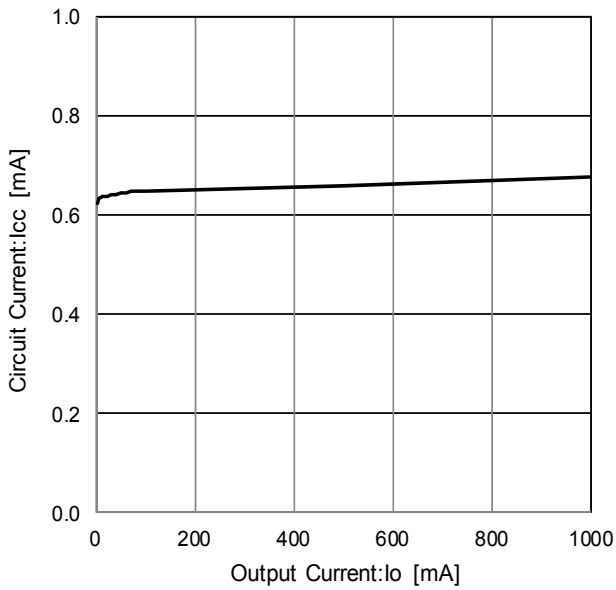


Figure 43. Circuit Current vs Output Current ($I_o = 0\text{mA} \rightarrow 1000\text{ mA}$)

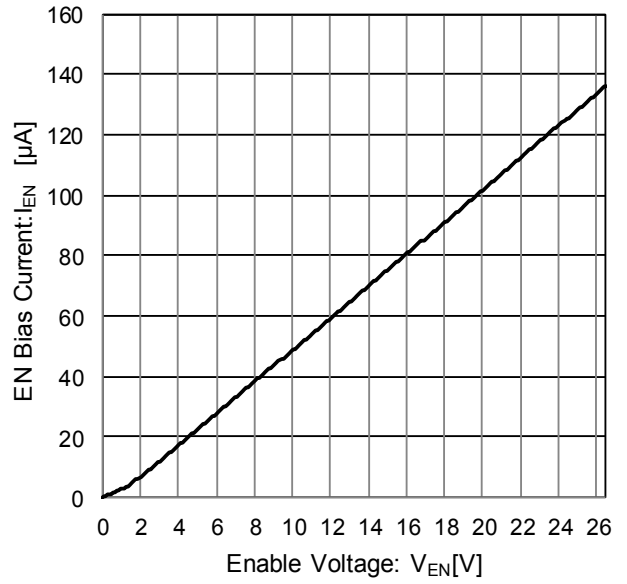


Figure 44. EN Voltage vs EN Current

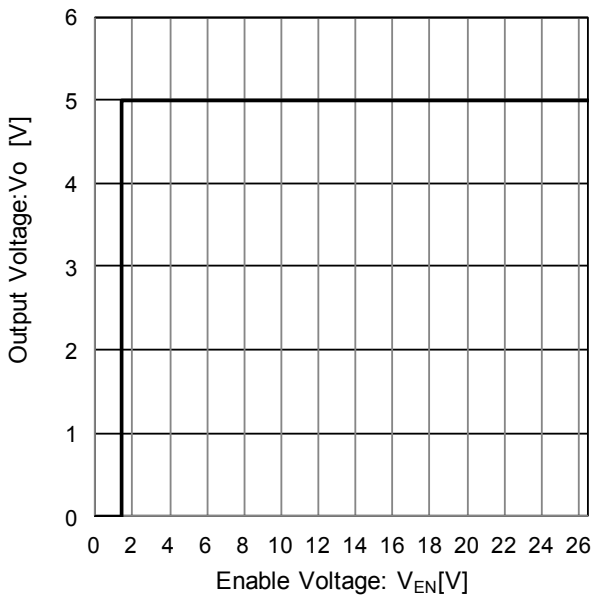


Figure 45. EN Voltage vs Output Voltage

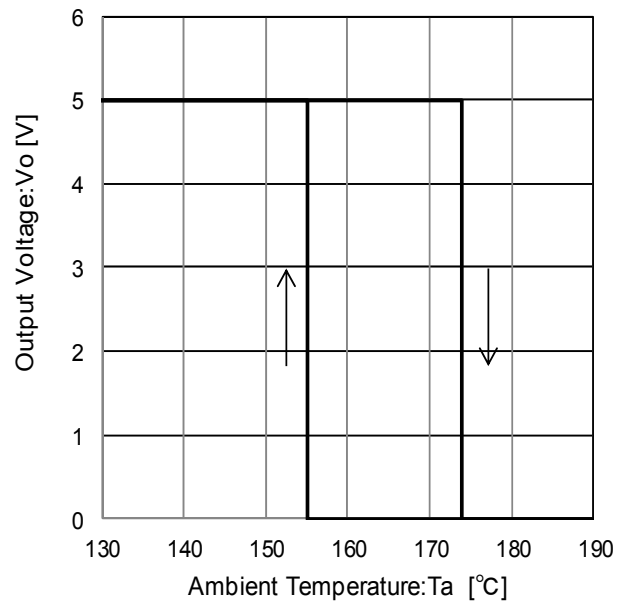


Figure 46. Thermal Shutdown Circuit Characteristic

●Reference Data

■BD80FC0 series

Unless otherwise specified, Ta = 25°C, Vcc=13.5V, VEN=5.0V, Io=0mA

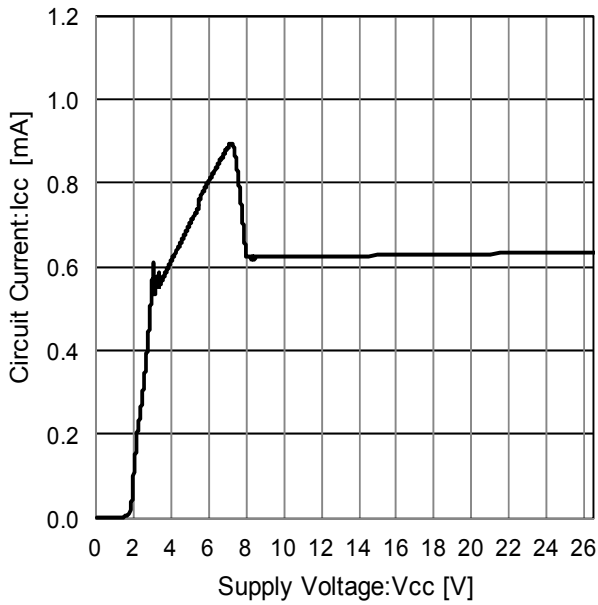


Figure 47. Circuit Current

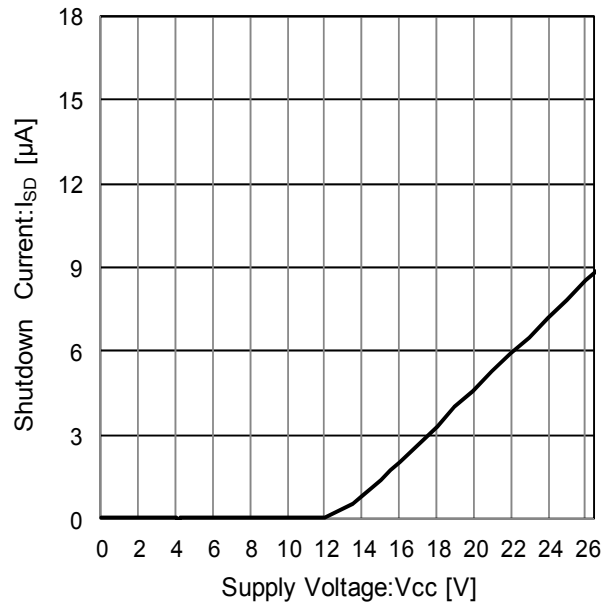


Figure 48. Shutdown Current (VEN=0V)

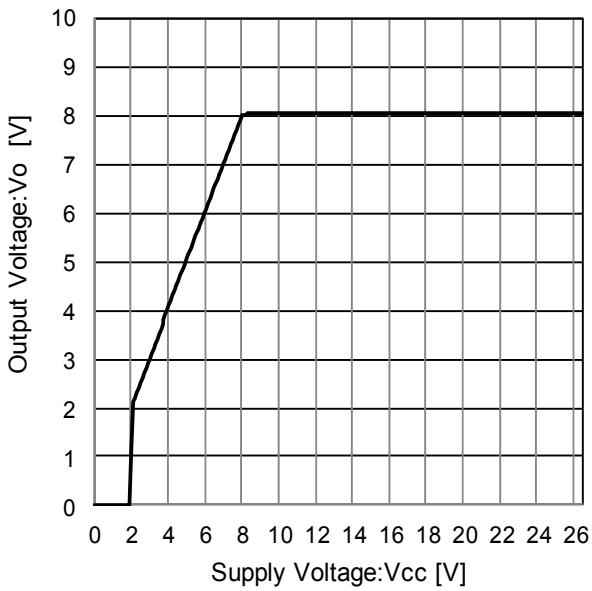


Figure 49. Line Regulation (Io=0mA)

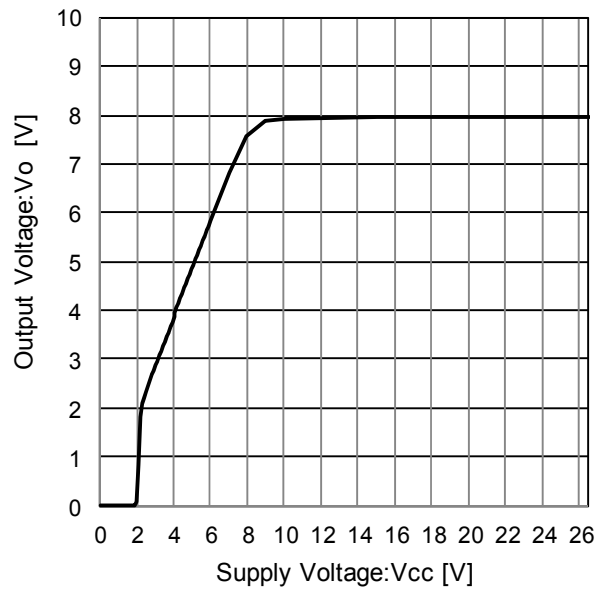


Figure 50. Line Regulation (Io=500mA)

●Reference Data - Continued

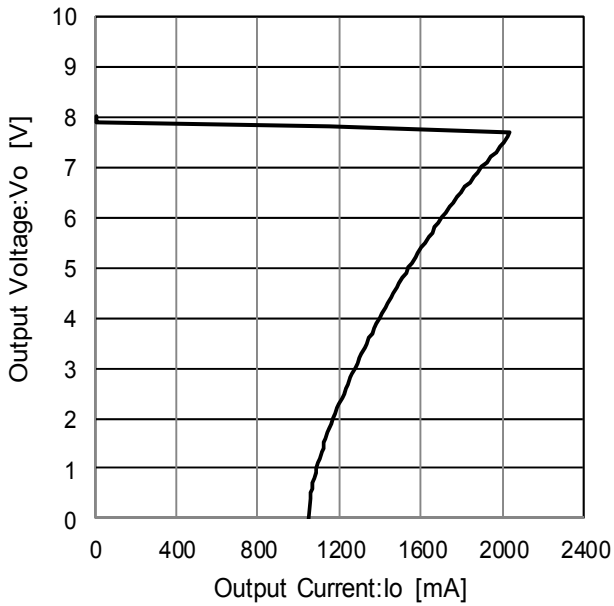


Figure 51. Load Regulation

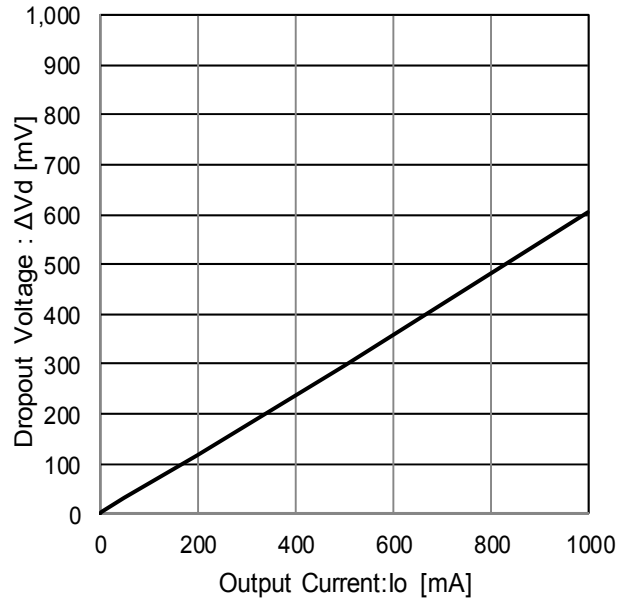


Figure 52. Dropout Voltage
($V_{cc}=V_o \times 0.95=7.6V$)

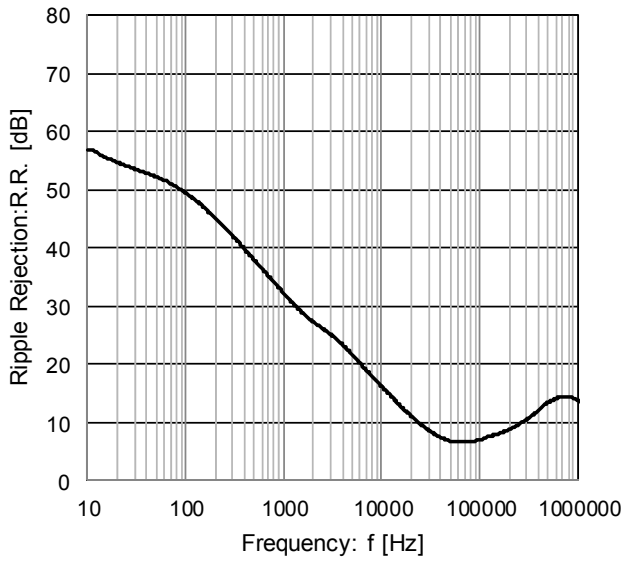


Figure 53. Ripple Rejection
($I_o=100mA$)

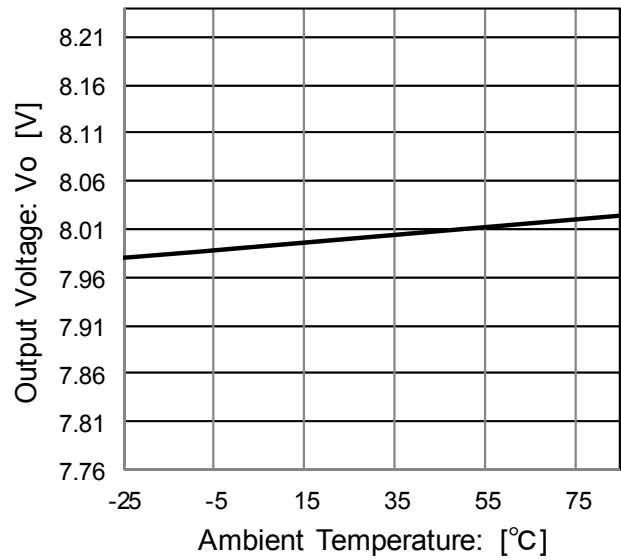


Figure 54. Output Voltage Temperature Characteristic

●Reference Data - Continued

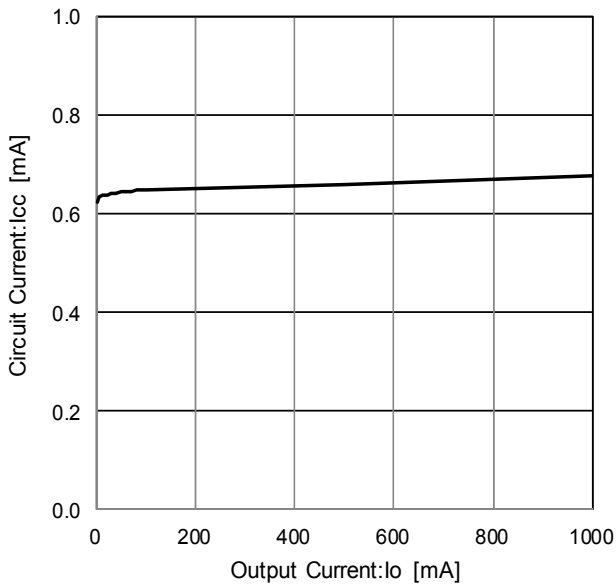


Figure 55. Circuit Current vs Output Current ($I_o = 0\text{mA} \rightarrow 1000\text{ mA}$)

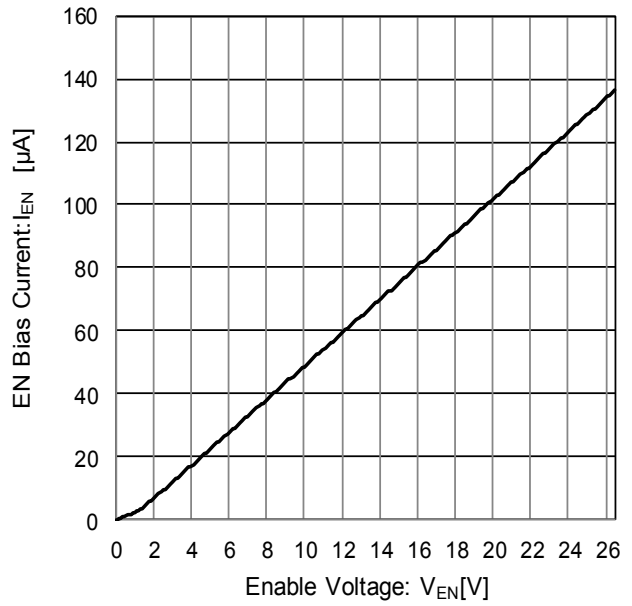


Figure 56. EN Voltage vs EN Current

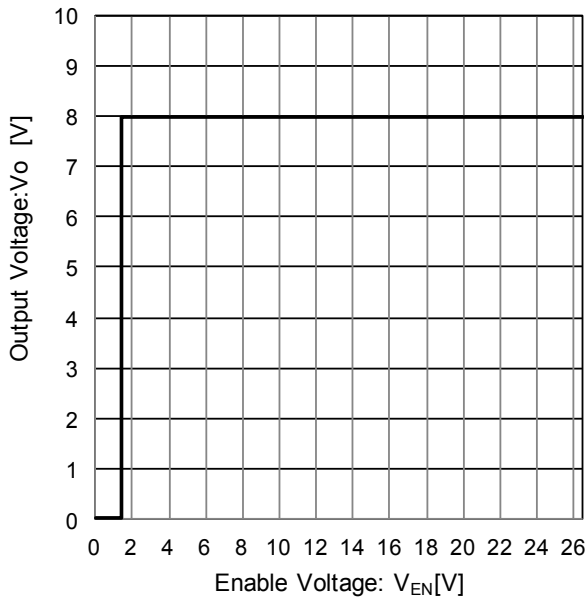


Figure 57. EN Voltage vs Output Voltage

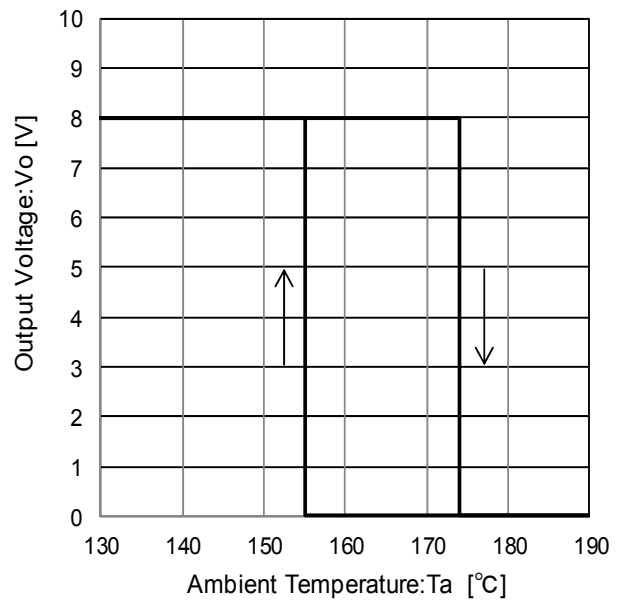


Figure 58. Thermal Shutdown Circuit Characteristic

●Reference Data

■BD90FC0 series

Unless otherwise specified, Ta = 25°C, Vcc=13.5V, VEN=5.0V, Io=0mA

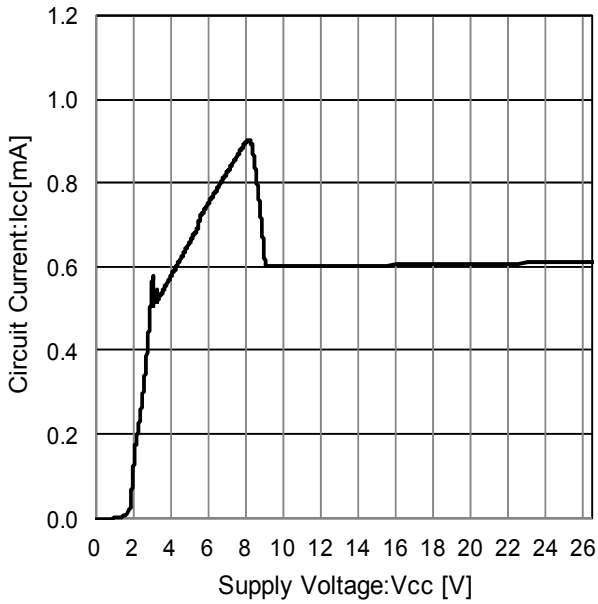


Figure 59. Circuit Current

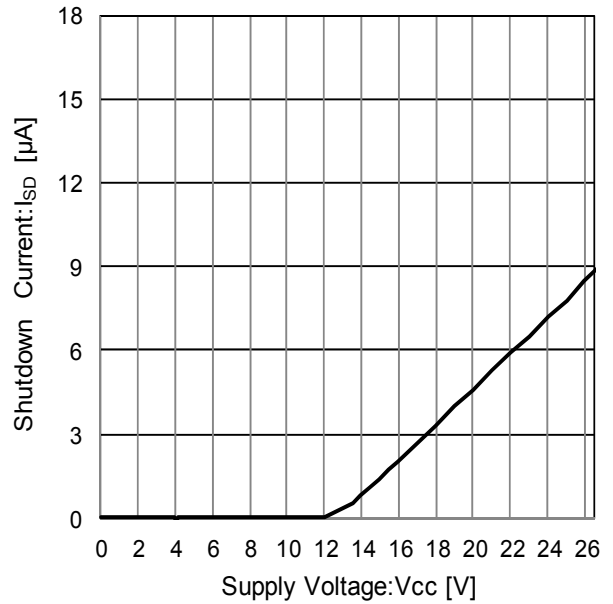


Figure 60. Shutdown Current (V_{EN}=0V)

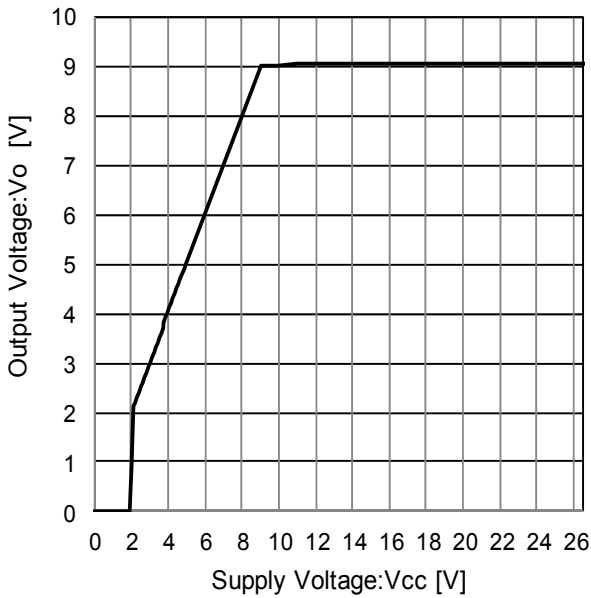


Figure 61. Line Regulation (I_o=0mA)

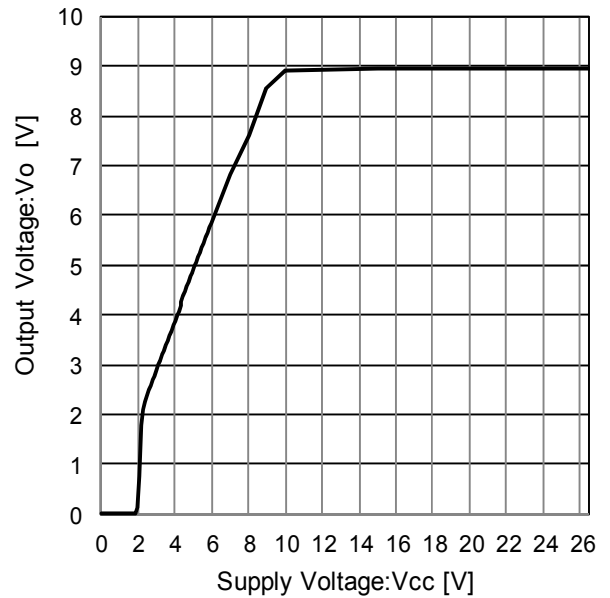


Figure 62. Line Regulation (I_o=500mA)

●Reference Data - Continued

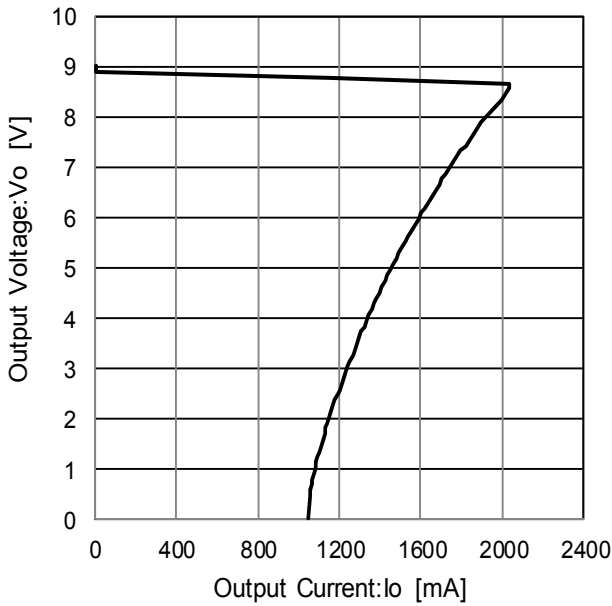


Figure 63. Load Regulation

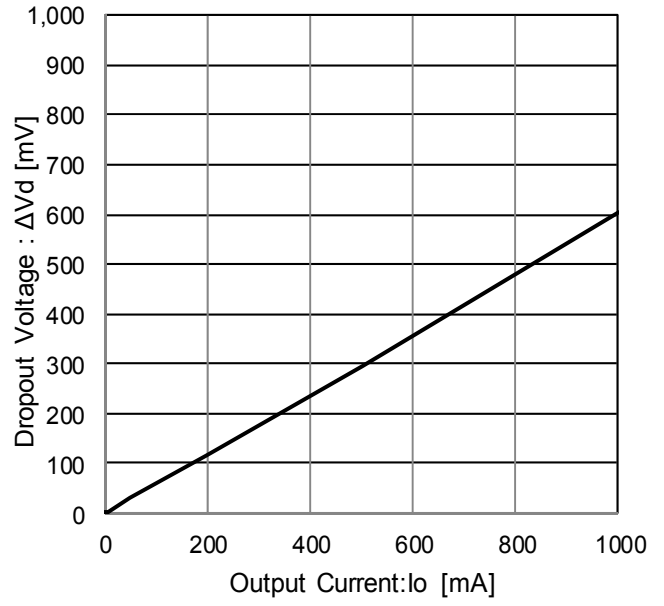


Figure 64. Dropout Voltage
($V_{cc}=V_o \times 0.95=8.55V$)

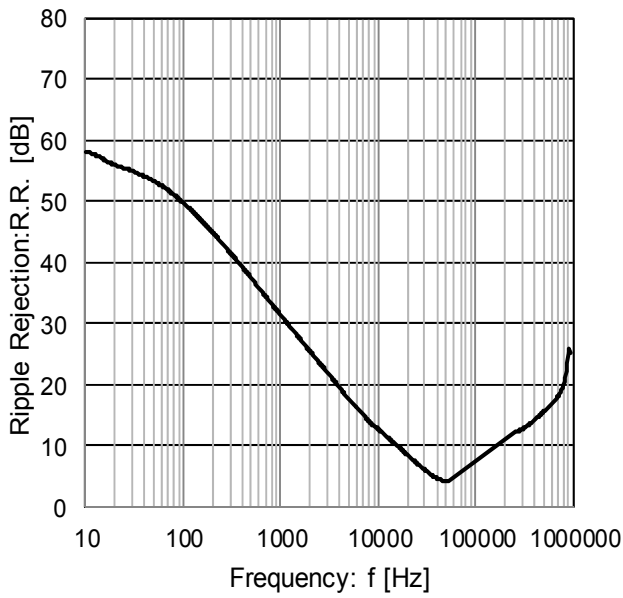


Figure 65. Ripple Rejection
($I_o=100mA$)

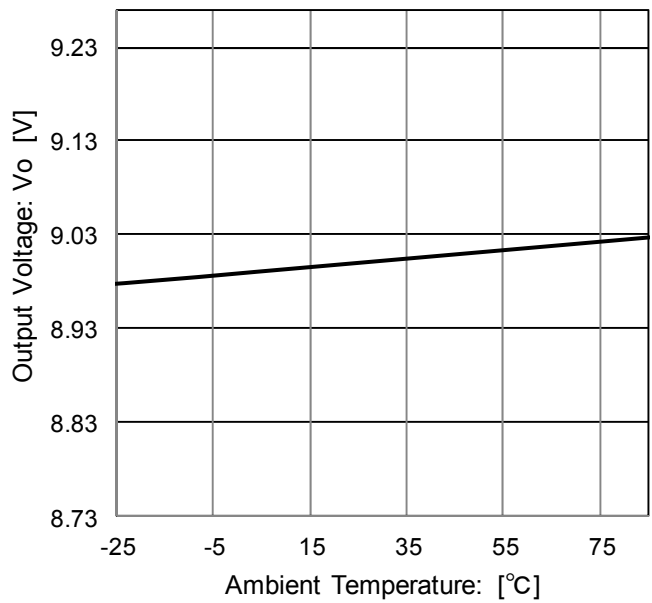


Figure 66. Output Voltage
Temperature Characteristic

●Reference Data - Continued

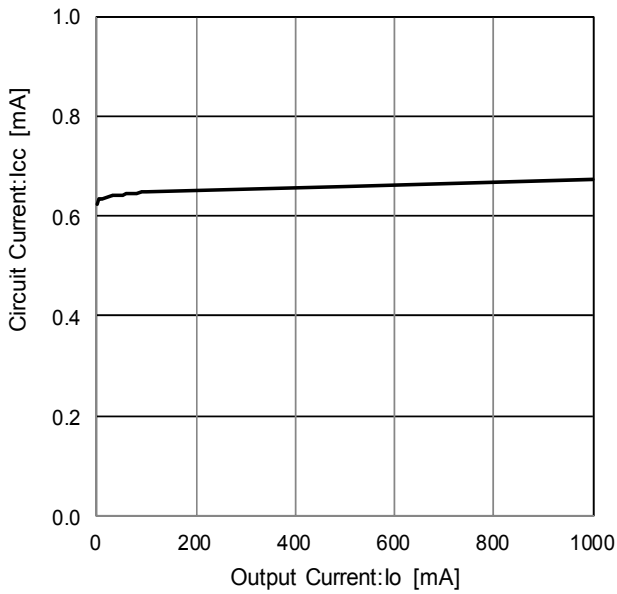


Figure 67. Circuit Current vs Output Current ($I_o = 0\text{mA} \rightarrow 1000\text{ mA}$)

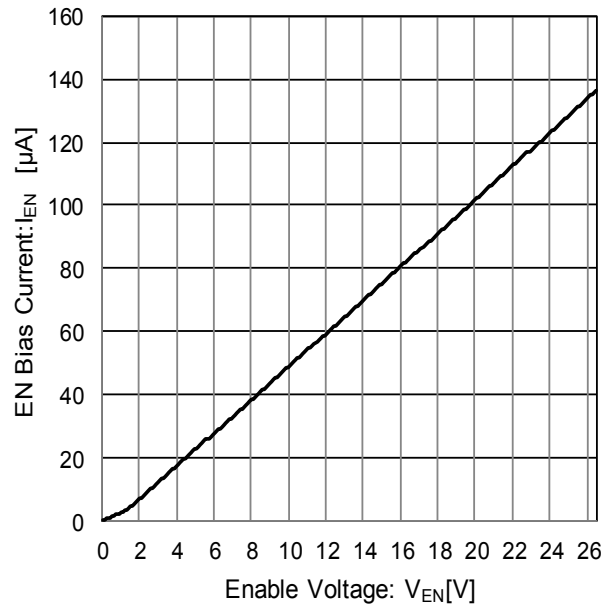


Figure 68. EN Voltage vs EN Current

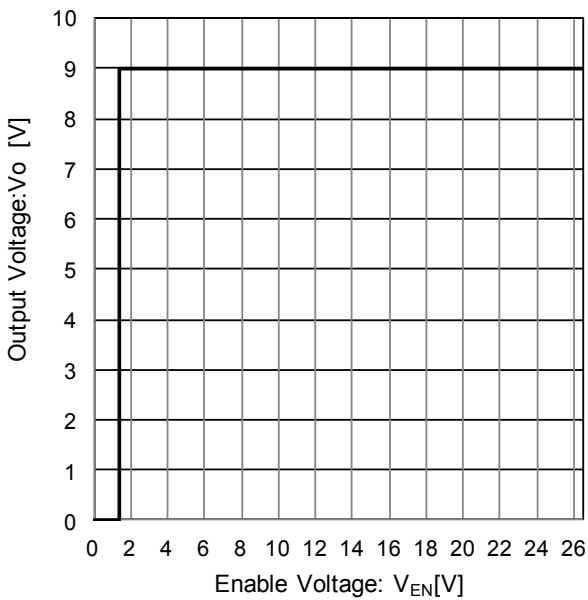


Figure 69. EN Voltage vs Output Voltage

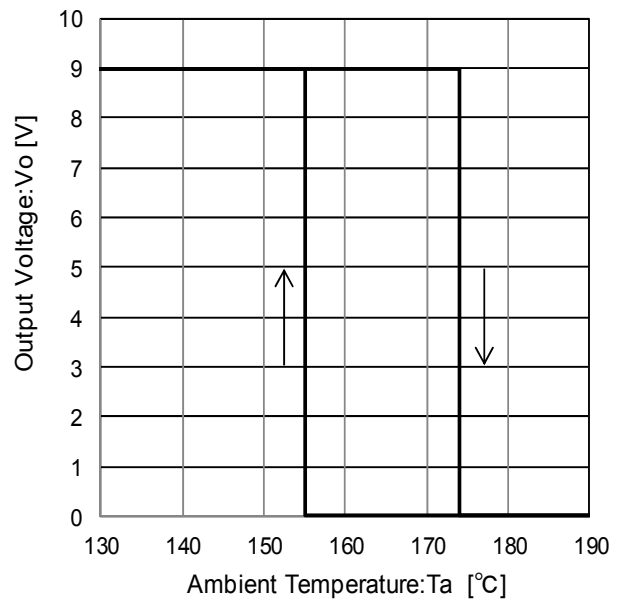
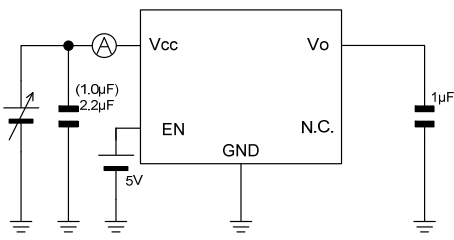


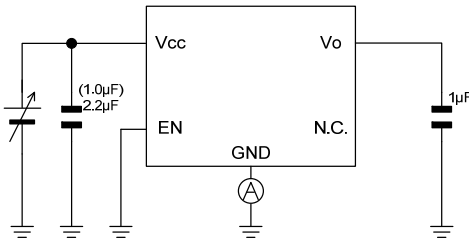
Figure 70. Thermal Shutdown Circuit Characteristic

● Measurement setup for reference data

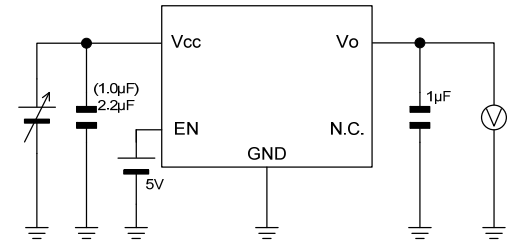
■ BDxxFC0 series(Output Voltage FixedType)



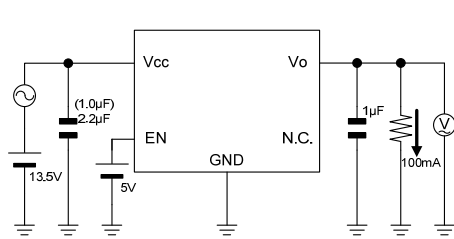
Measurement setup for Figure 24, 35, 47 and 59



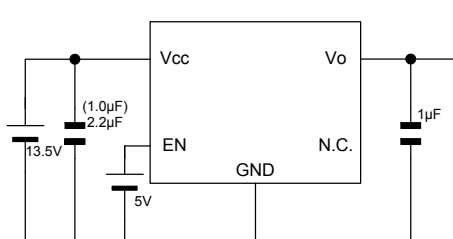
Measurement setup for Figure 25, 36, 48 and 60



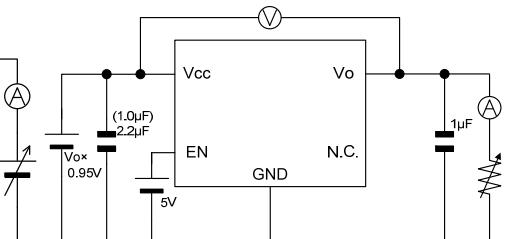
Measurement setup for Figure 26, 37, 49 and 61



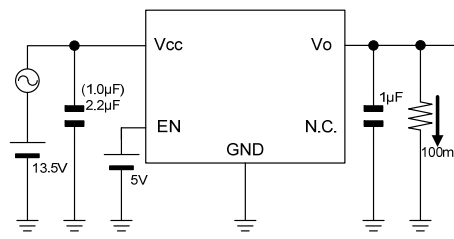
Measurement setup for Figure 27, 38, 50 and 62



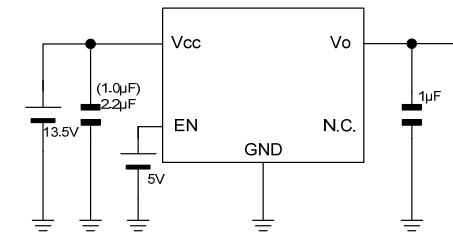
Measurement setup for Figure 28, 39, 51 and 63



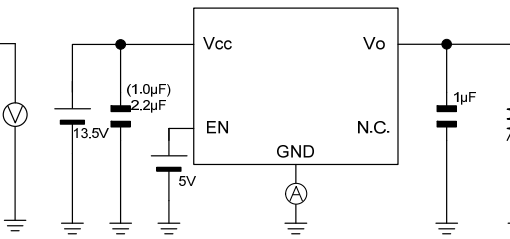
Measurement setup for Figure 40, 52 and 64



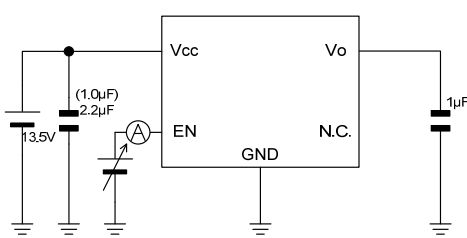
Measurement setup for Figure 29, 41, 53 and 65



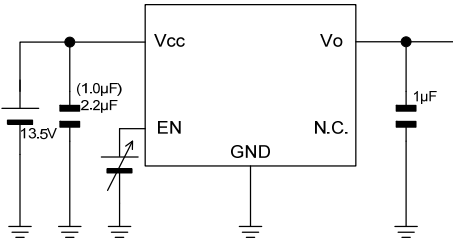
Measurement setup for Figure 30, 42, 54 and 66



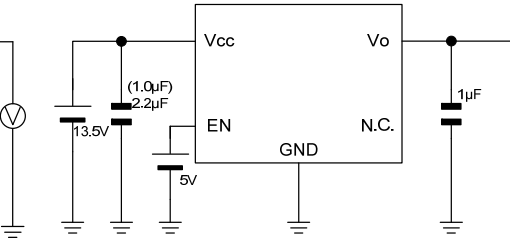
Measurement setup for Figure 31, 43, 55 and 67



Measurement setup for Figure 32, 44, 56 and 68



Measurement setup for Figure 33, 45, 57 and 69



Measurement setup for Figure 34, 46, 58 and 70

● Application Examples

- Applying positive surge to the Vcc pin

If there is a possibility that surges higher than 35.0V will be applied to the Vcc pin, a Zener diode should be placed between the Vcc pin and GND pin, as shown in the Figure below.

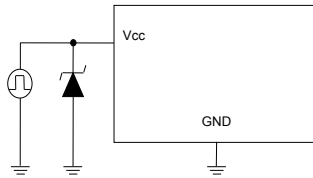


Figure 71.

- Applying negative surge to the Vcc pin

If there is a possibility that negative surges lower than the GND are applied to the Vcc pin, a Schottky diode should be placed between the Vcc pin and GND pin, as shown in the Figure below.

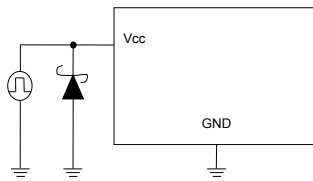


Figure 72.

- Implementing a protection diode

If there is a possibility that a large inductive load is connected to the output pin resulting in back-EMF at time of startup and Shutdown, a protection diode should be placed as shown in the Figure below.

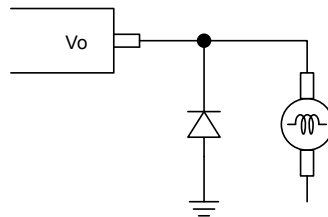


Figure 73.

● Thermal Design

■ HTSOP-J8

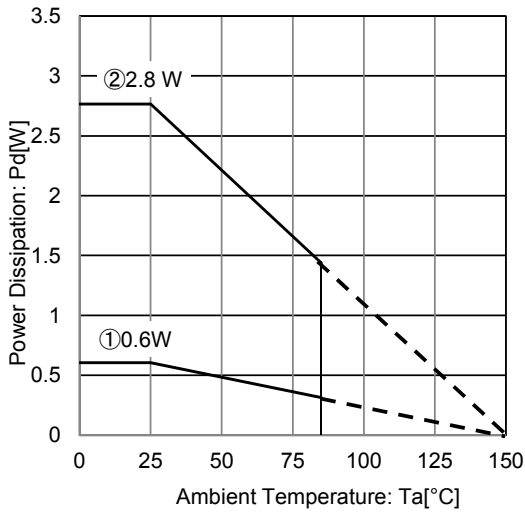


Figure 74.

■ TO252-3/5

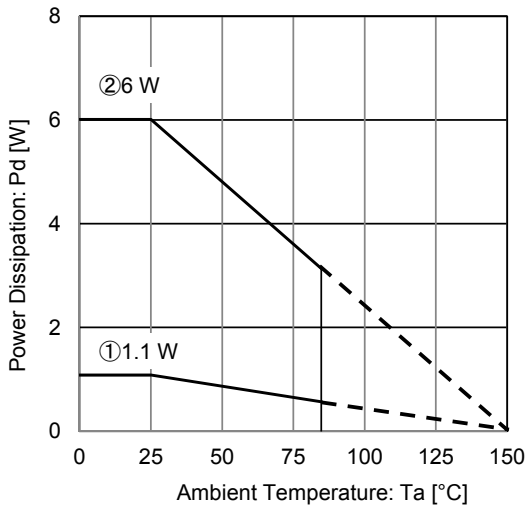


Figure 75.

IC mounted on ROHM standard board based on JEDEC.

Board material: FR4

Board size

1s 114.3 mm x 76.2 mm x 1.57 mmt

2s2p 114.3 mm x 76.2 mm x 1.6 mmt

Mount condition: PCB and exposed pad are soldered.

Top copper foil: The footprint ROHM recommend.

+ wiring to measure.

①: 1-layer PCB (Copper foil area on the reverse side of PCB: 0 mm x 0 mm)

②: 4-layer PCB (2 inner layers and copper foil area on the reverse side of PCB: 74.2mm x 74.2 mm)

Condition①: $\theta_{ja} = 206.4 \text{ }^\circ\text{C/W}$, $\Psi_{JT} = 21 \text{ }^\circ\text{C/W}$

Condition②: $\theta_{ja} = 45.2 \text{ }^\circ\text{C/W}$, $\Psi_{JT} = 13 \text{ }^\circ\text{C/W}$

IC mounted on ROHM standard board based on JEDEC.

Board material: FR4

Board size

1s 114.3 mm x 76.2 mm x 1.57 mmt

2s2p 114.3 mm x 76.2 mm x 1.6 mmt

Mount condition: PCB and exposed pad are soldered.

Top copper foil: The footprint ROHM recommend.

+ wiring to measure.

①: 1-layer PCB (Copper foil area on the reverse side of PCB: 0 mm x 0 mm)

②: 4-layer PCB (2 inner layers and copper foil area on the reverse side of PCB: 74.2mm x 74.2 mm)

Condition①: $\theta_{ja} = 115.3 \text{ }^\circ\text{C/W}$, $\Psi_{JT} = 14 \text{ }^\circ\text{C/W}$

Condition②: $\theta_{ja} = 20.8 \text{ }^\circ\text{C/W}$, $\Psi_{JT} = 3 \text{ }^\circ\text{C/W}$

When operating at temperature more than $T_a=25^\circ\text{C}$, please refer to the power dissipation characteristic curve shown in Figure 74 and 75.

The IC characteristics are closely related to the temperature at which the IC is used, so it is necessary to operate the IC at temperatures less than the maximum junction temperature T_{jmax} .

Figure 74 and 75 show the acceptable power dissipation characteristic curves of the HTSOP-J8 and TO252-3/5 packages. Even when the ambient temperature (T_a) is at normal temperature (25°C), the chip junction temperature (T_j) may be quite high so please operate the IC at temperatures less than the acceptable power dissipation.

The calculation method for power consumption $P_c(\text{W})$ is as follows

$$P_c = (V_{cc} - V_o) \times I_o + V_{cc} \times I_{cc}$$

$$\text{Acceptable loss } P_d \geq P_c$$

Solving this for load current I_o in order to operate within the acceptable loss

$$I_o \leq \frac{P_d - V_{cc} \times I_{cc}}{V_{cc} - V_o}$$

V_{cc} : Input voltage
 V_o : Output voltage
 I_o : Load current
 I_{cc} : Circuit current

It is then possible to find the maximum load current I_{omax} with respect to the applied voltage V_{cc} at the time of thermal design.

Calculation Example) When TO252-3 / TO252-5, $T_a=85^\circ\text{C}$, $V_{cc}=13.5\text{V}$, $V_o=5.0\text{V}$

$$I_o \leq \frac{3.115 - 13.5 \times I_{cc}}{8.5}$$

$$I_o \leq 365.6\text{mA} \quad (I_{cc} : 0.5\text{mA})$$

(Figure 75 $\theta_{ja}=20.8 \text{ }^\circ\text{C/W} \rightarrow -48.1\text{W}/^\circ\text{C}$
 $25^\circ\text{C} = 6\text{W} \rightarrow 85^\circ\text{C} = 3.115\text{W}$)

● I/O equivalent circuit

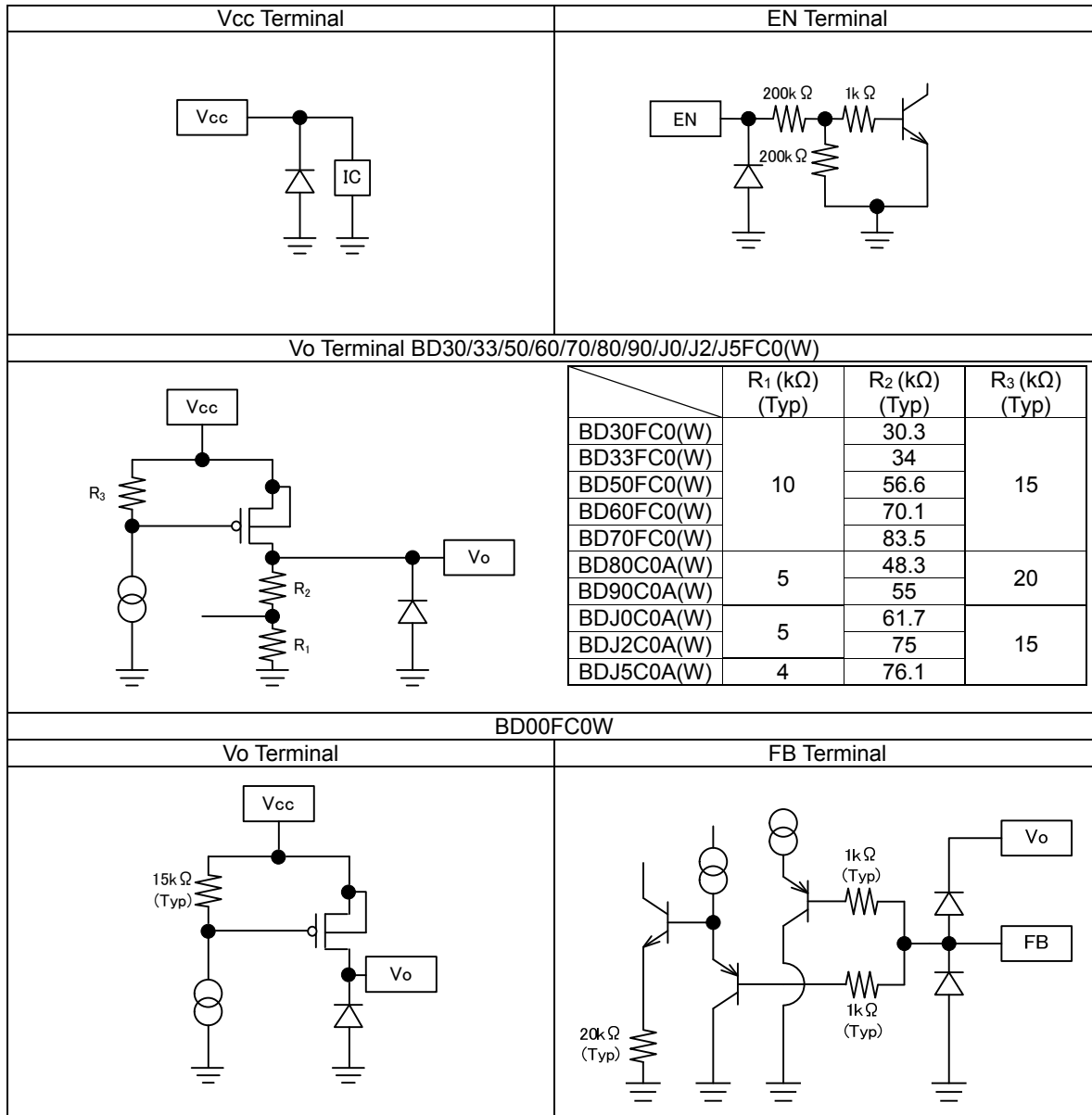


Figure 76.

● Output Voltage Configuration Method (BD00FC0)

Please connect resistors R₁ and R₂ (which determines the output voltage) as shown in Figure 77.

Please be aware that the offset, due to the current that flows from the FB terminal, becomes large when resistors with large values are used. Resistance values ranging from R₂=5kΩ to 10kΩ is recommended. Determine R₁ by adjusting with R₂

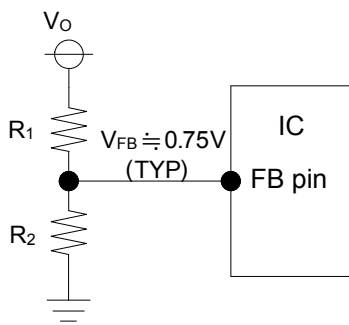


Figure 77.

V_{OUT} setting equation is,

$$V_{OUT} \cong V_{FB} \times (R_1 + R_2) / R_2$$

Thoroughly check the constant settings on the application because circuit current increases depending on connected resistor.

●Operational Notes

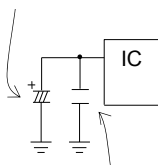
1. Absolute maximum ratings
Use of the IC in excess of absolute maximum ratings (such as the input voltage or operating temperature range) may result in damage to the IC. Assumptions should not be made regarding the state of the IC (e.g., short mode or open mode) when such damage is suffered. If operational values are expected to exceed the maximum ratings for the device, consider adding protective circuitry (such as fuses) to eliminate the risk of damaging the IC.
2. Electrical characteristics described in these specifications may vary, depending on temperature, supply voltage, external circuits, and other conditions. Therefore, be sure to check all relevant factors, including transient characteristics.
3. GND potential
The potential of the GND pin must be the minimum potential in the system in all operating conditions. Ensure that no pins are at a voltage below the GND at any time, regardless of transient characteristics.
4. Ground wiring pattern
When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground potential within the application in order to avoid variations in the small-signal ground caused by large currents. Also, ensure that the GND traces of external components do not cause variations on GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.
5. Inter-pin shorts and mounting errors
Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply or GND pins (caused by poor soldering or foreign objects) may result in damage to the IC.
6. Operation in strong electromagnetic fields
Using this product in strong electromagnetic fields may cause IC malfunction. Caution should be exercised in applications where strong electromagnetic fields may be present.
7. Testing on application boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from a jig or fixture during the evaluation process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.
8. Power Dissipation Pd
Using the unit in excess of the rated power dissipation may cause deterioration in electrical characteristics including reduced current capability due to the rise of chip temperature. The mentioned power dissipation in the Thermal Design is the value at HTSOP-J8 and TO252-3/5 package when 114.3mm × 76.2mm × 1.6mm glass epoxy board is mounted. And in case this exceeds, take the measures like enlarge the size of board; make copper foil area for heat dissipation big; and do not exceed the power dissipation.
9. Thermal consideration
Use a thermal design that allows for a sufficient margin in light of the Pd in actual operating conditions. Consider Pc that does not exceed Pd in actual operating conditions. ($P_d \geq P_c$)

$\left(\begin{array}{l} T_{jmax} : \text{Maximum junction temperature} = 150(^{\circ}\text{C}) , T_a : \text{Peripheral temperature} (^{\circ}\text{C}) , \\ \theta_{ja} : \text{Thermal resistance of package-ambience} (^{\circ}\text{C}/\text{W}) , P_d : \text{Package Power dissipation} (\text{W}) , \\ P_c : \text{Power consumption} (\text{W}) , V_{cc} : \text{Input Voltage} , V_o : \text{Output Voltage} , I_o : \text{Load} , I_{cc} : \text{Circuit Current} \end{array} \right)$

Package Power dissipation : $P_d (\text{W}) = (T_{jmax} - T_a) / \theta_{ja}$
 Power consumption : $P_c (\text{W}) = (V_{cc} - V_o) \times I_o + V_{cc} \times I_{cc}$

10. Vcc pin
Insert a capacitor ($V_o \geq 5.0\text{V}$:capacitor $\geq 1\mu\text{F}$, $1.0 \leq V_o < 5.0\text{V}$:capacitor $\geq 2.2\mu\text{F}$) between the Vcc and GND pins. Choose the capacitance according to the line between the power smoothing circuit and the Vcc pin. Selection of the capacitance also depends on the application. Verify the application and allow for sufficient margins in the design. It is recommended to use a capacitor with excellent voltage and temperature characteristics.

Electrolytic capacitor

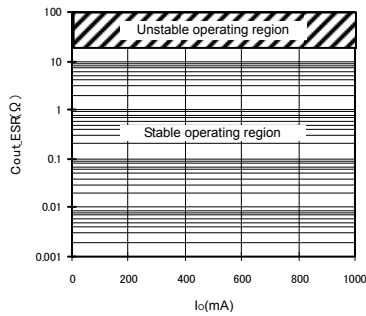


Ceramic capacitor, Low ESR capacitor

11. Capacitor connected to Output pin

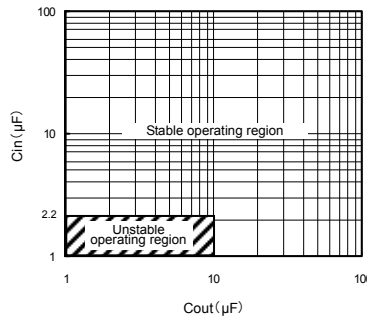
In order to prevent oscillation, a capacitor needs to be placed between the output pin and GND pin. We recommend a capacitor with a capacitance of more than $1\mu\text{F}$ ($3.0\text{V} \leq V_O \leq 15.0\text{V}$). Electrolytic, tantalum and ceramic capacitors can be used. We recommend a capacitor with a capacitance of more than $4.7\mu\text{F}$ ($1.0\text{V} \leq V_O < 3.0\text{V}$). Ceramic capacitors can be used. When selecting the capacitor, ensure that the capacitance of more than $1\mu\text{F}$ ($3.0\text{V} \leq V_O \leq 15.0\text{V}$) or more than $4.7\mu\text{F}$ ($1.0\text{V} \leq V_O < 3.0\text{V}$) is maintained at the intended applied voltage and temperature range. Due to changes in temperature, the capacitance can fluctuate possibly resulting in oscillation. For selection of the capacitor, refer to the C_{out_ESR} vs I_{out} data. The stable operation range given in the reference data is based on the standalone IC and resistive load. For actual applications, the stable operating range is influenced by the PCB impedance, input supply impedance, and load impedance. Therefore, verification of the final operating environment is needed. When selecting a ceramic type capacitor, we recommend using X5R, X7R, or better, with excellent temperature and DC-biasing characteristics and high voltage tolerance. Also, in case of rapidly changing input voltage and load current, select the capacitance in accordance with verifying that the actual application meets the required specification.

$4.0\text{V} \leq V_{CC} \leq 26.5\text{V}$ $3.0\text{V} \leq V_O \leq 15.0\text{V}$
 $-25^\circ\text{C} \leq T_a \leq +85^\circ\text{C}$
 $5\text{k}\Omega \leq R_2 \leq 10\text{k}\Omega$ (BD00FC0W)
 $C_{in} = 2.2\mu\text{F} \leq C_{in} \leq 100\mu\text{F}$
 $1\mu\text{F} \leq C_{out} \leq 100\mu\text{F}$



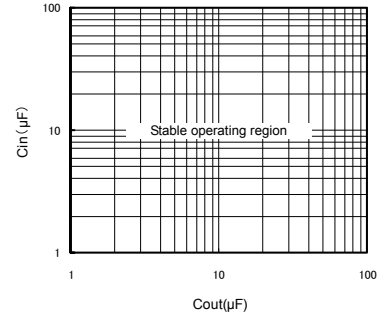
Cout_ESR vs Io
 $3.0\text{V} \leq V_O \leq 15.0\text{V}$
 (Reference data)

$4.0\text{V} \leq V_{CC} \leq 26.5\text{V}$
 $3.0\text{V} \leq V_O \leq 15.0\text{V}$
 $-25^\circ\text{C} \leq T_a \leq +85^\circ\text{C}$
 $0\text{A} \leq I_o \leq 1\text{A}$
 $5\text{k}\Omega \leq R_2 \leq 10\text{k}\Omega$ (BD00FC0W)

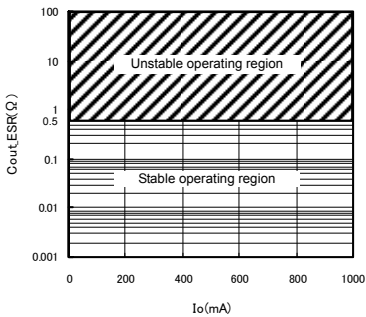


Cin vs Cout
 $3.0\text{V} \leq V_O \leq 15.0\text{V}$
 (Reference data)

$6.0\text{V} \leq V_{CC} \leq 26.5\text{V}$
 $5.0\text{V} \leq V_O \leq 15.0\text{V}$
 $-25^\circ\text{C} \leq T_a \leq +85^\circ\text{C}$
 $0\text{A} \leq I_o \leq 1\text{A}$
 $5\text{k}\Omega \leq R_2 \leq 10\text{k}\Omega$ (BD00FC0W)

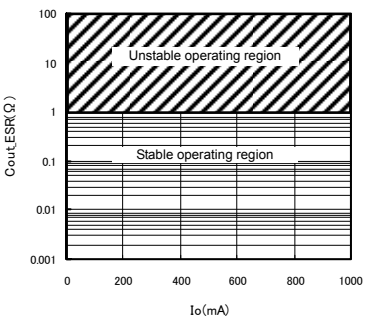


$4.0\text{V} \leq V_{CC} \leq 26.5\text{V}$
 $1.0\text{V} \leq V_O < 1.5\text{V}$
 $-25^\circ\text{C} \leq T_a \leq +85^\circ\text{C}$
 $5\text{k}\Omega \leq R_1 \leq 10\text{k}\Omega$ (BD00FC0W)
 $2.2\mu\text{F} \leq C_{in} \leq 100\mu\text{F}$
 $4.7\mu\text{F} \leq C_{out} \leq 100\mu\text{F}$

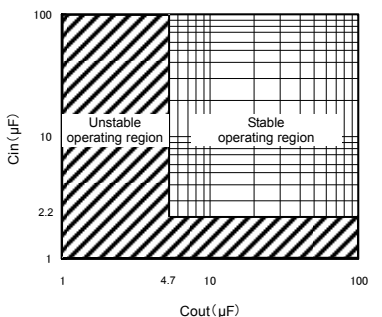


Cout_ESR vs Io
 $1.0\text{V} \leq V_O < 3.0\text{V}$
 (Reference data)

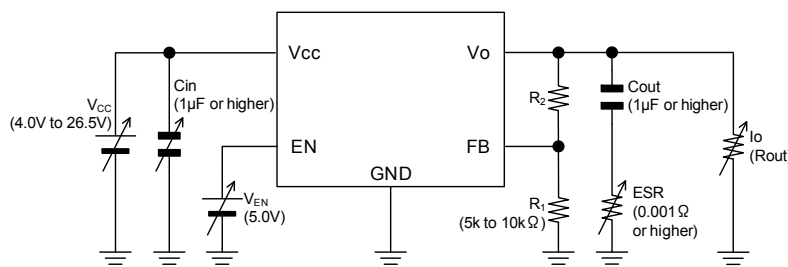
$4.0\text{V} \leq V_{CC} \leq 26.5\text{V}$
 $1.5\text{V} \leq V_O < 3.0\text{V}$
 $-25^\circ\text{C} \leq T_a \leq +85^\circ\text{C}$
 $5\text{k}\Omega \leq R_1 \leq 10\text{k}\Omega$ (BD00FC0W)
 $2.2\mu\text{F} \leq C_{in} \leq 100\mu\text{F}$
 $4.7\mu\text{F} \leq C_{out} \leq 100\mu\text{F}$



$4.0\text{V} \leq V_{CC} \leq 26.5\text{V}$
 $1.0\text{V} \leq V_O < 3.0\text{V}$
 $-25^\circ\text{C} \leq T_a \leq +85^\circ\text{C}$
 $0\text{A} \leq I_o \leq 1\text{A}$
 $5\text{k}\Omega \leq R_1 \leq 10\text{k}\Omega$ (BD00FC0W)

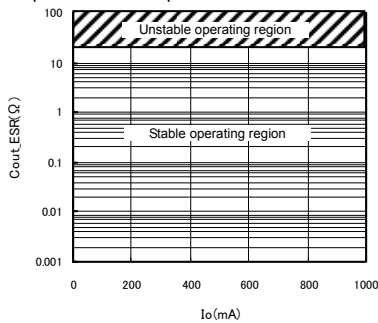


Cin vs Cout
 $1.0\text{V} \leq V_O < 3.0\text{V}$
 (Reference data)



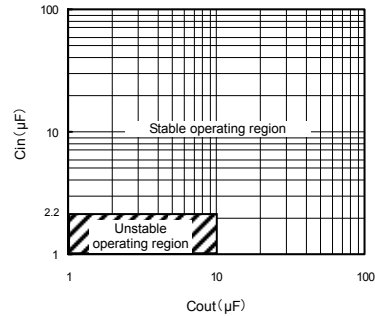
Operation Note 11 Measurement circuit (BD00FC0W)

$4.0V \leq V_{CC} \leq 26.5V$
 $1.0V \leq V_O < 3.0V$
 (Cout and Ceramic capacitor 10 μ F is connected in parallel.)
 $-25^\circ C \leq T_a \leq +85^\circ C$
 $5k\Omega \leq R_1 \leq 10k\Omega$ (BD00FC0W)
 $2.2\mu F \leq C_{in} \leq 100\mu F$
 $1\mu F \leq C_{out} \leq 100\mu F$

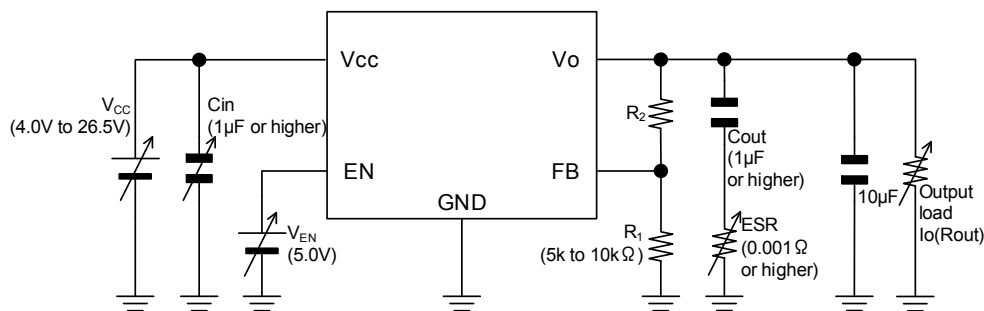


Cout_ESR vs Io
 $1.0V \leq V_O < 3.0V$
 Cout and Ceramic capacitor 10 μ F is connected in parallel.
 (Reference data)

$4.0V \leq V_{CC} \leq 26.5V$
 $1.0V \leq V_O < 3.0V$
 (Cout and Ceramic capacitor 10 μ F is connected in parallel.)
 $-25^\circ C \leq T_a \leq +85^\circ C$
 $0A \leq I_o \leq 1A$
 $5k\Omega \leq R_1 \leq 10k\Omega$ (BD00FC0W)



Cin vs Cout
 $1.0V \leq V_O < 3.0V$
 Cout and Ceramic capacitor 10 μ F is connected in parallel.
 (Reference data)



Operation Note 11 Measurement circuit (BD00FC0W)

12. EN pin
Do not make the voltage level of the chip's enable pin at floating level or in between $V_{EN(High)}$ and $V_{EN(Low)}$. Otherwise, the output voltage would be unstable or indefinite.
13. For a steep change of the Vcc voltage
Because MOSFET for output Transistor is used when an input voltage change is very steep, it may evoke large current. When selecting the value of external circuit constants, please make sure that the operation on the actual application takes these conditions into account.
14. For infinitesimal fluctuations of output voltage.
For applications that have infinitesimal fluctuations of the output voltage caused by some factors (e.g. disturbance noise, input voltage fluctuations, load fluctuations, etc.), please take enough measures to avoid some influence (e.g. insert a filter, etc.).
15. Over current protection circuit (OCP)
The IC incorporates an integrated over-current protection circuit that operates in accordance with the rated output capacity. This circuit serves to protect the IC from damage when the load becomes shorted. It is also designed to limit output current (without latching) in the event of a large and instantaneous current flow from a large capacitor or other component. These protection circuits are effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous or transitive operation of the protection circuits.
16. Thermal Shutdown circuit (TSD)
The IC incorporates a built-in thermal shutdown circuit, which is designed to turn the IC off, completely, in the event of thermal overload. It is not designed to protect the IC from damage or guarantee its operation. IC's should not be used after this function has activated, or in applications where the operation of this circuit is assumed.

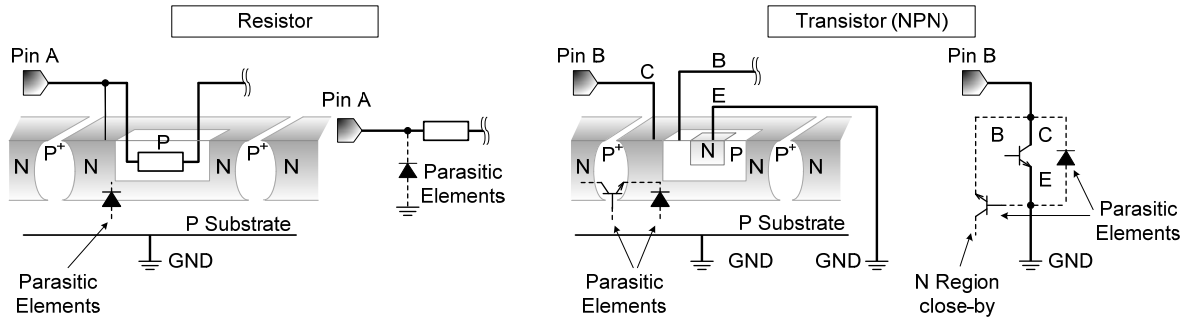
17. In some applications, the Vcc and the Vo potential might be reversed, possibly resulting in circuit internal damage or damage to the elements. For example, the accumulated charge in the output pin capacitor flow backward from the Vo to the Vcc when the Vcc shorts to the GND. Use a capacitor with a capacitance with less than 1000µF for reducing the damage. We also recommend using reverse polarity diodes in series between the Vcc and the GND or a bypass diode between the Vo and the Vcc.

18. Regarding input pins of the IC

This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. PN junctions are formed at the intersection of these P layers with the N layers of other elements, creating parasitic diodes and/or transistors. For example (refer to the Figure below):

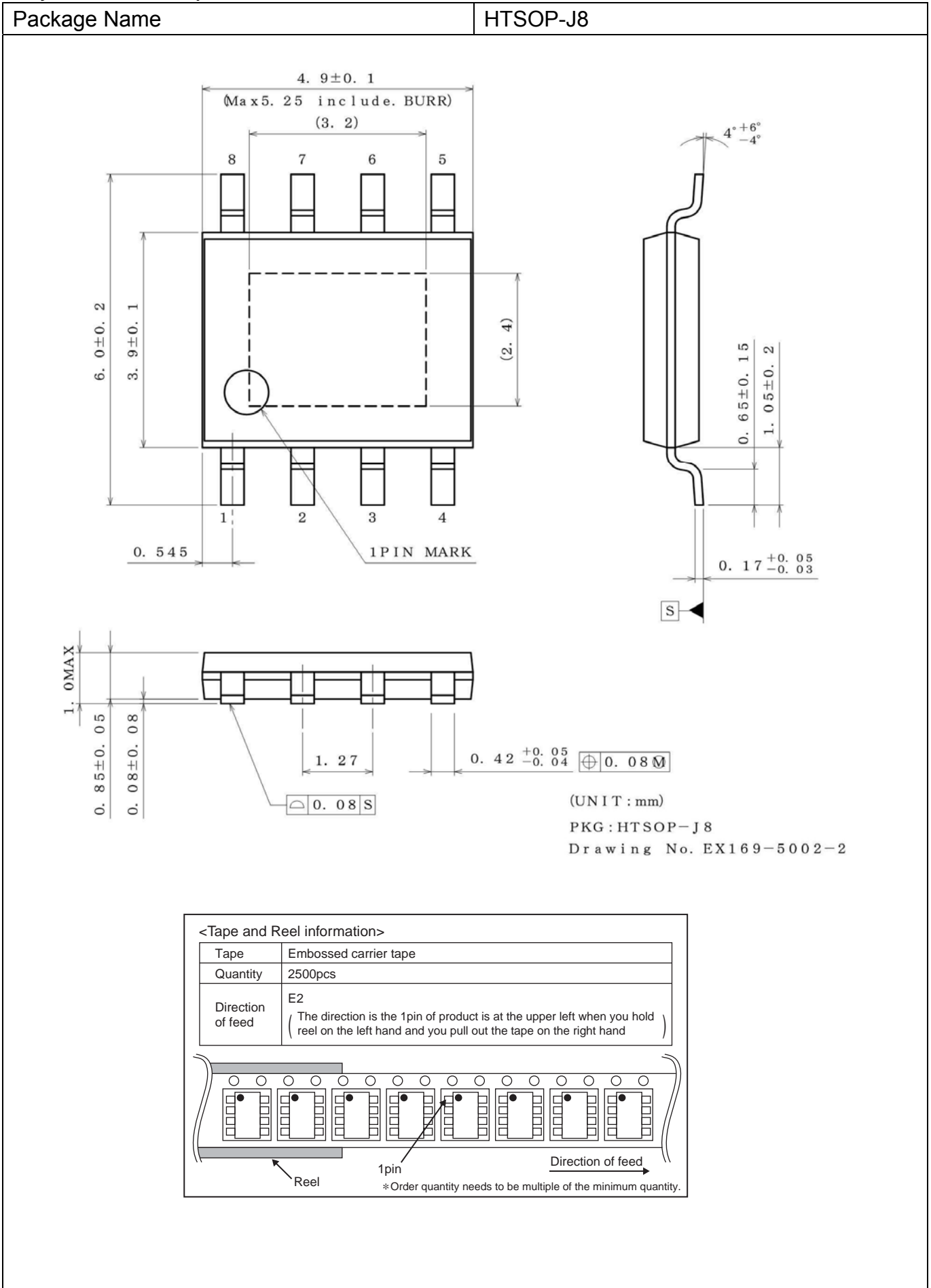
- When GND > Pin A and GND > Pin B, the PN junction operates as a parasitic diode
- When GND > Pin B, the PN junction operates as a parasitic transistor

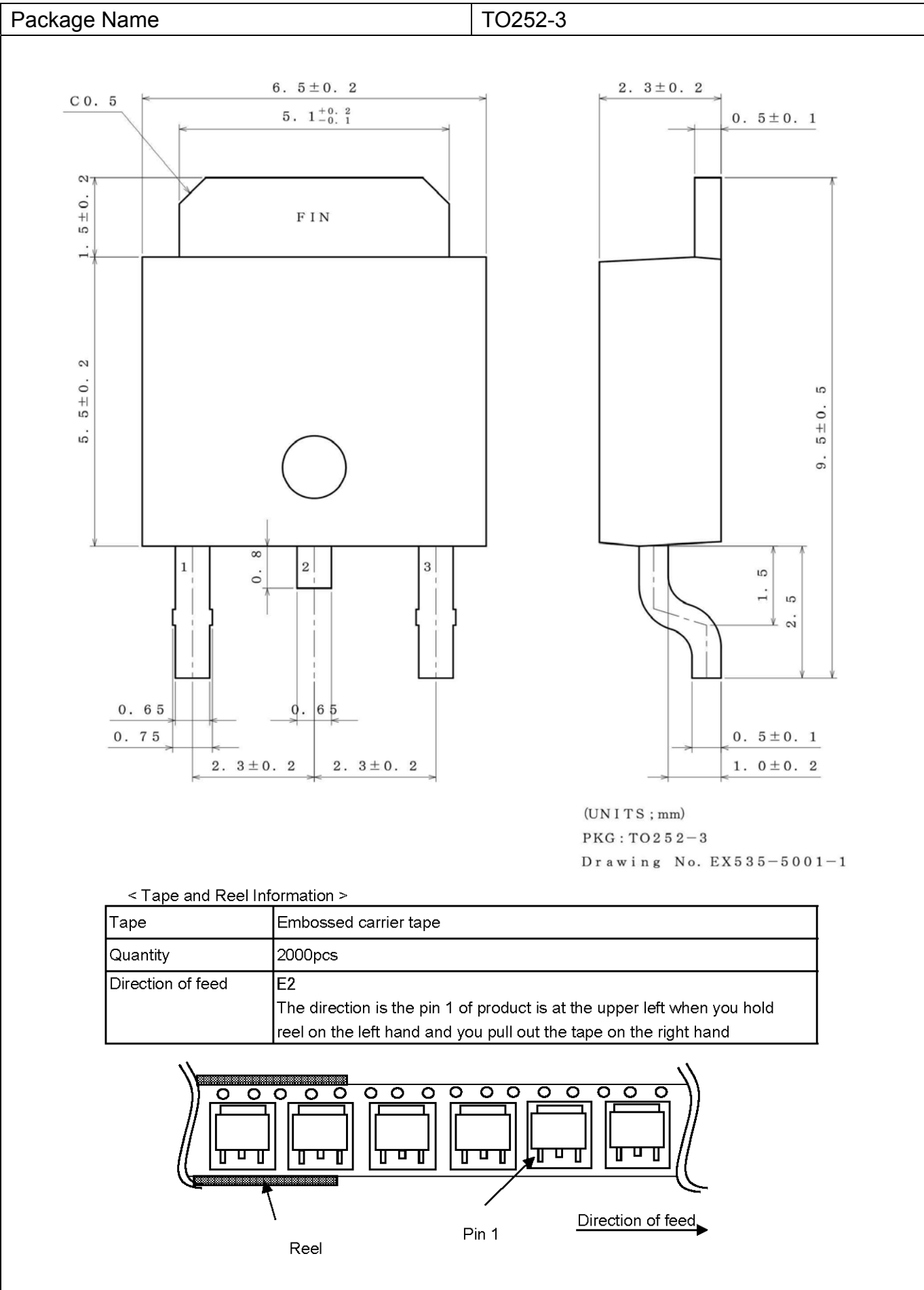
Parasitic diodes occur inevitably in the structure of the IC, and the operation of these parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.

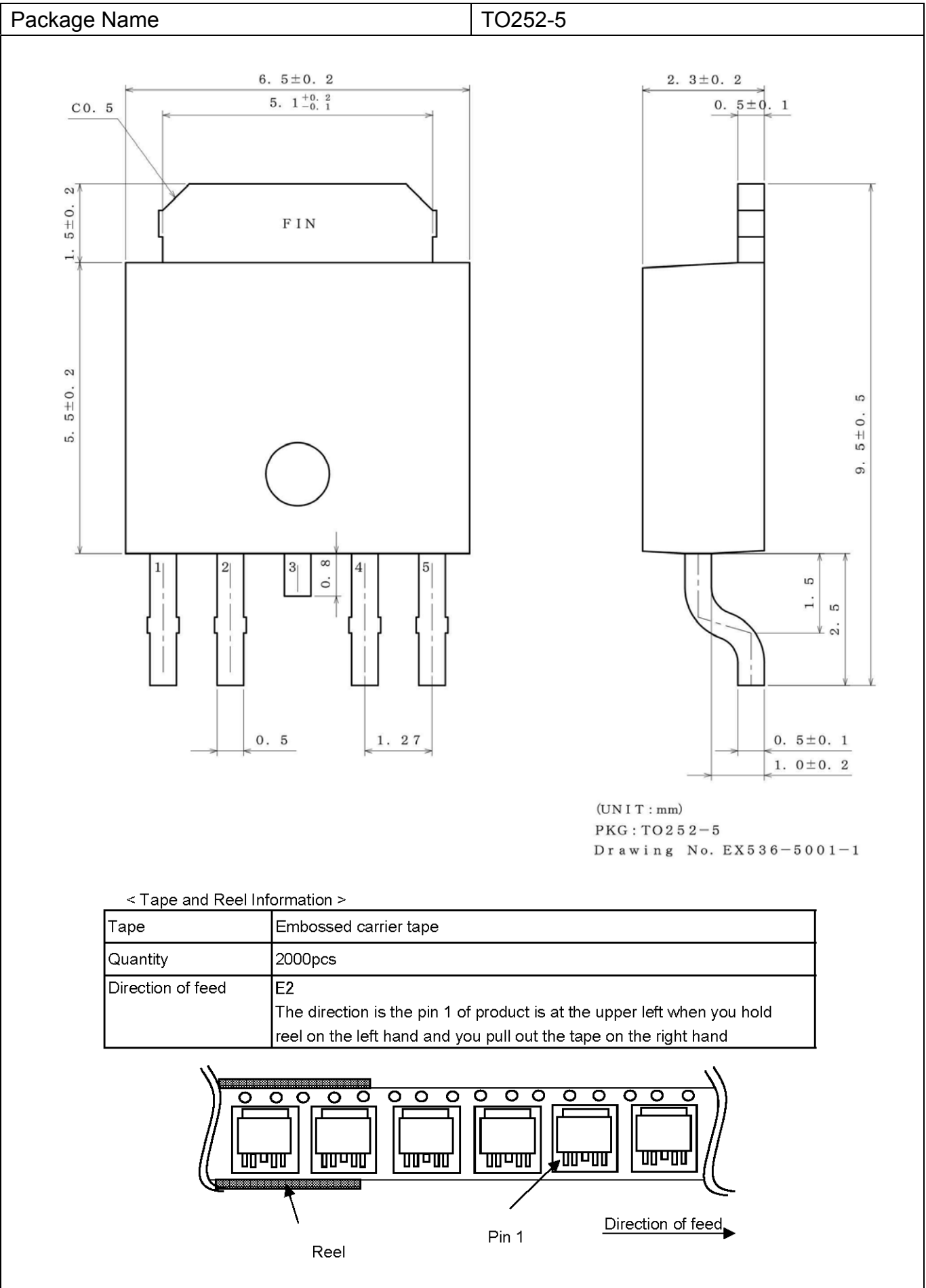


Example of monolithic IC structure

●Physical Dimension Tape and Reel Information

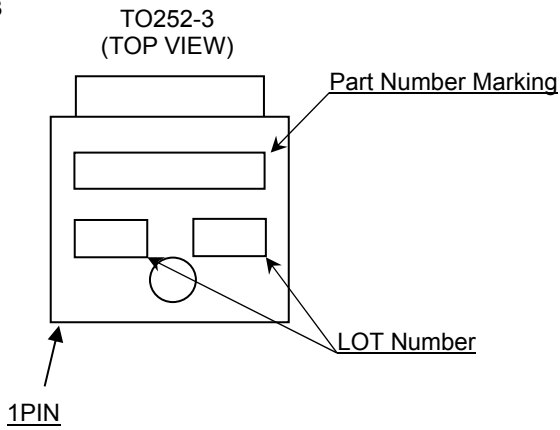






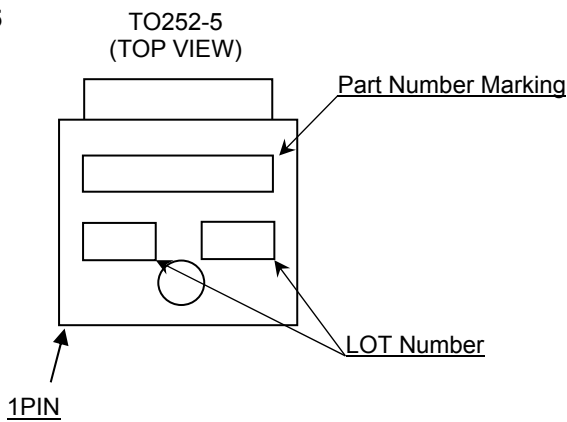
●Marking Diagram

TO252-3



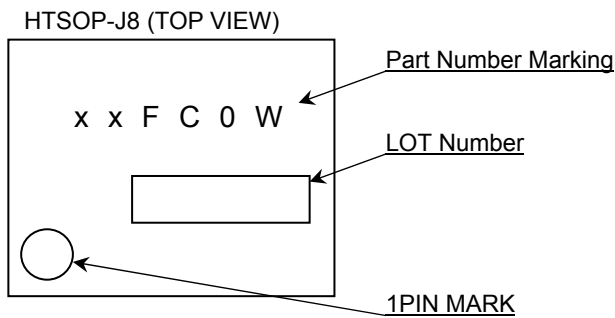
Output Voltage[V]	Part Number Marking
3.3	33FC0
5.0	50FC0

TO252-5



Output Voltage[V]	Part Number Marking
Variable	00FC0W
3.0	30FC0W
3.3	33FC0W
5.0	50FC0W
6.0	60FC0W
7.0	70FC0W
8.0	80FC0W
9.0	90FC0W
10.0	J0FC0W
12.0	J2FC0W
15.0	J5FC0W

HTSOP-J8



Output Voltage[V]	Part Number Marking
Variable	00FC0W
3.0	30FC0W
3.3	33FC0W
5.0	50FC0W
6.0	60FC0W
7.0	70FC0W
8.0	80FC0W
9.0	90FC0W
10.0	J0FC0W
12.0	J2FC0W
15.0	J5FC0W

●Revision History

Date	Revision	Changes
27.Aug.2013	001	New Release
20.Oct. 2015	002	Add BDxxFC0FP and BDxxFC0WFP Change pin name OUT -> Vo
02.Dec. 2015	003	P2 Lineup modified
16.May. 2016	004	The document control number:TSZ02201-0GAG0A600040-1-2 -> TSZ02201-0G2G0A600040-1-2 P8 Power dissipation deleted P8 notes added in electrical characteristics P9 Copper Pattern area modified Misentry modified in Whole page
10.Jan. 2017	005	P3,4 Pin name modified in Pin Configuration/Pin Description P8 Product name modified in Operating Conditions *3 P8 Enable condition added in Circuit Current at shutdown mode for preventing mistake P10-12 Comment and Condition added for preventing mistake Figure title changed due to expression difference between Japanese and English datasheet P14-25 Comment and Condition added for preventing mistake Figure title changed due to expression difference between Japanese and English datasheet P13, P26 Measurement setup for reference data modified P29 Figure 76. I/O equivalent modified P29 Duplicated contents deleted in Output Voltage Configuration Method P30 Misentry modified in Operational notes Expression of shutdown mode and shutdown SW changed to Enable

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JAPAN	USA	EU	CHINA
CLASS III	CLASS III	CLASS II b	CLASS III
CLASS IV		CLASS III	

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- Confirm that operation temperature is within the specified range described in the product specification.
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