Configuration	Silicon Monolithic Integrated Circuit
Product Name	TFT Liquid Crystal Power Management IC for Car Navigation System
Model Name	**BD6171KV**
Outline Drawing	Figure - 1 (Molded Plastic)
Block Diagram	Figure - 2
Functions	1. 2 ch PWM controller with variable stepdown converter. 2. Variable output voltage series regulator. 3. Variable output voltage positive / negative charge pump inverter. 4. Oscillator is enabled by an external pulse synchronization. 5. Overcurrent protection (OCP) circuitry. 6. Undervoltage Lockout protection (UVLO). 7. Thermal Shutdown Protection (TSD). 8. Each channel can be individually turned ON/OFF. 9. VQUFP48 package

○ Absolute Maximum Ratings (Ta=25℃)

Specifications	Symbol	Rating	Unit
Voltage between VCC, DVCC-GND	Vcc, DVcc	36	V
Voltage between PVCC1,2-GND	PVcc1,2	36	V
Voltage between VCC-PVCC1,2	Vcc-PVcc1,2	0.3	V
Voltage between VREF-GND	VREF	7	V
Voltage between VREGA-GND	VREGA	7	V
Voltage between VCC-VREGB	VREGB	7	V
Voltage between VCC-OUT1,2	VOUT1,2	7	V
Voltage between PVCC3-GND	PVcc3	36	V
Voltage between PVCC4,5—GND	PVcc4,5	12	V
Voltage between OUT4,5—GND	VOUT4,5	PVcc4,5	V
Voltage between CL1,2—GND	VCL1,2	PVcc1,2	V
Voltage between VS1,2—GND	VVS1,2	PVcc1,2	V
Voltage between VODET1,2,3,4,5-GND	VODET1,2,3,4,5	VREGA	V
Voltage between SYNC—GND	VSYNC	7	V
Power Dissipation	Pd	900(*1)	mW
Operating Temperature Range	Topr	-40～+85	℃
Ambient Storage Temperature Range	Tstg	-55～+125	℃

(*1) When mounted on a 70 × 70 × 1.6 mm^3 glass epoxy substrate, for every temperature increase of 1℃, power dissipation decreases by 9 mW (at temperatures of 25℃ or greater).

Application example
The application circuit is recommended for use. Make sure to confirm the adequacy of the characteristics.
When using the circuit with changes to the external circuit constants, make sure to leave an adequate margin for external components including static and transitional characteristics as well as dispersion of the IC.
Note that ROHM cannot provide adequate confirmation of patents.

The product described in this specification is designed to be used with ordinary electronic equipment or devices (such as audio-visual equipment, office-automation equipment, communications devices, electrical appliances, and electronic toys).
Should you intend to use this product with equipment or devices which require an extremely high level of reliability and the malfunction of which would directly endanger human life (such as medical instruments, transportation equipment, aerospace machinery, nuclear-reactor controllers, fuel controllers and other safety devices), please be sure to consult with our sales representative in advance.

ROHM assumes no responsibility for use of any circuits described herein, conveys no license under any patent or other right, and makes no representations that the circuits are free from patent infringement.

○ Recommended Operating Conditions

Specifications	Symbol	Standard Value			Unit	Conditions
		Min.	Standard	Max.		
Supply Voltage	Vcc,DVcc	6.0	—	24.0	V	
PWM Controller Input Voltage	PVcc1,2	6.0	—	24.0	V	
Series REG Input Voltage	PVcc3	5.0	—	24.0	V	
Charge Pump Input Voltage	PVcc4,5	3.0	—	12.0	V	
Oscillator Frequency	Fosc	50	—	500	kHz	
External Synchronization Frequency	FSYNC	60	—	600	kHz	
Oscillator Timing Resistor Value	RT	30	—	680	kΩ	
Overcurrent Protection Cancellation Timing Capacitor Value	Cocp1,2	—	—	1000	pF	

○ Electrical Properties (Ta=25℃, Vcc,DVcc,PVcc1,2,3=13.2V, PVcc4,5=8V, Fosc=500kHz, EN1～5=5V unless otherwise specified.)

Specification	Symbol	Standard Value			Unit	Conditions	Measurement Circuit
		Min.	Standard	Max.			
【Entire Device】							
Standby Current	Iccst	—	—	10	μA	EN1～5=0V	1
Operating Current	Icc	—	5	10	mA	FB1,FB2=0V	1
【Reference Voltages】							
Output Voltage	VREF	2.97	3.00	3.03	V	IREF=-0.1mA	1
Line Regulation	ΔVLIREF	—	—	10	mV	Vcc=7～18V, IREF=-0.1mA	1
Load Regulation	Δ	—	—	10	mV	IREF=-0.1mA～-1mA	1
【Internal Regulator】							
VREGA Output Voltage	VREGA	4.5	5.0	5.5	V		1
VREGB Output Voltage	VREGB	VCC -5.5	VCC -5.0	VCC -4.5	V	When switching between PVcc1,2-OUT1,2 with a 1000 pF connection	1

VREGB Dropout Voltage	ΔVREGB	—	1.8	2.2	V	Voltage between VREGB-GND When switching between Vcc=5.6V,PVcc1,2-OUT1, 2with a 1000 pF connection	1
【Enable Unit】EN1～5							
Threshold Voltage	VEN	1.2	1.8	2.4	V		1
Inflow Current	IEN	—	17	35	μA	EN1～5=5V	1

◎ The design of this device does not incorporate measures used to harden against radiation.

○ Electrical Properties (Ta=25℃, Vcc,DVcc,PVcc1,2,3=13.2V, PVcc4,5=8V, Fosc=500kHz, EN1～5=5V unless otherwise specified.)

Specification	Symbol	Standard Value			Unit	Conditions	Measurement Circuit
		Min.	Standard	Max.			
Series REG Unit							
【Output】 (Measured at a 5V output setting, unless otherwise specified.)							
Feedback Voltage	VFB3	0.97	1.00	1.03	V	Io3=-80mA	2
Load Regulation	ΔVLO3	—	80	160	mV	Io3=0～-80mA	2
Line Regulation	ΔVLI3	—	20	40	mV	Vcc=10～16V, Io3=-80mA	2
Output Current Ability	Io3	100	—	—	mA	VO3=4.75V	2
Dropout Voltage	ΔVo3	—	0.4	0.7	V	PVCC3=4.75V,Io3=-80mA	2
Ripple Rejection	RR3	45	60	—	dB	f=100Hz, Io3=-80mA	2
Output Voltage	Vo3	—	5.0	—	V	Io3=-80mA	2
Output Short Current	Io3S	—	25	—	mA	Vo3=0V	2
FB3 Outflow Current	IFB3	—	—	1	μA	VFB3=0.97V	2
【Output Voltage Detection】							
Output Detection Voltage	VDET3	0.55	0.6	0.65	V	FB3 Voltage	2
Hysteresis	VHYS3	0.1	0.2	0.3	V		2
Output High Voltage	VDETH3	VREGA-0.4	—	—	V	IDET3=-1μA	2
Output Low Voltage	VDETL3	—	—	0.4	V	IDET3=25μA	2
PWM Controller Unit							
【Oscillator】							
Oscillator	Fosc	270	300	330	kHz	RT=91kΩ	3
Oscillator Frequency Ratio	ΔFosc	—	—	2	%	Vcc=7～18V	3
【Frequency Synchronization】							
Synchronization Frequency	FSYNC	—	375	—	kHz	FSYNC=375kHz	3
SYNC Threshold Voltage	VSYNC	1.2	1.4	1.6	V		3
SYNC Outflow Current	ISYNC	-1	—	—	μA	VSYNC=1.4V	3

【Error Amp】							
Feedback Voltage	VINV1,2	0.98	1.00	1.02	V		3
Input Bias Current	IINV1,2	-1	—	—	μA	VINV1,2=0.97V	3
Maximum Output Voltage	VFBH1,2	2.8	—	—	V	VINV1,2=0.5V	3
Minimum Output Voltage	VFBL1,2	—	—	0.1	V	VINV1,2=1.5V	3
Output Sink Current	IFBSINK 1,2	-6.0	-2.0	-0.5	mA	VFB1,2=1.5V	3
Output Source Current	IFBSOURCE1,2	60	100	160	μA	VFB1,2=1.5V	3
Soft Start Charging Current	ISS1,2	-4.0	-2.5	-1.0	μA	VSS1,2=1.0V	3
Soft Start Threshold Voltage	VSS1,2	—	1.0	—	V	VINV1,2=1.0V,SS Voltage	3
Soft Start Standby Voltage	VSSSTD 1,2	—	10	100	mV	SS Voltage	3

◎ The design of this device does not incorporate measures used to harden against radiation.

○ Electrical Properties (Ta=25℃, Vcc,DVcc,PVcc1,2,3=13.2V, PVcc4,5=8V, Fosc=500kHz, EN1～5=5V unless otherwise specified.)

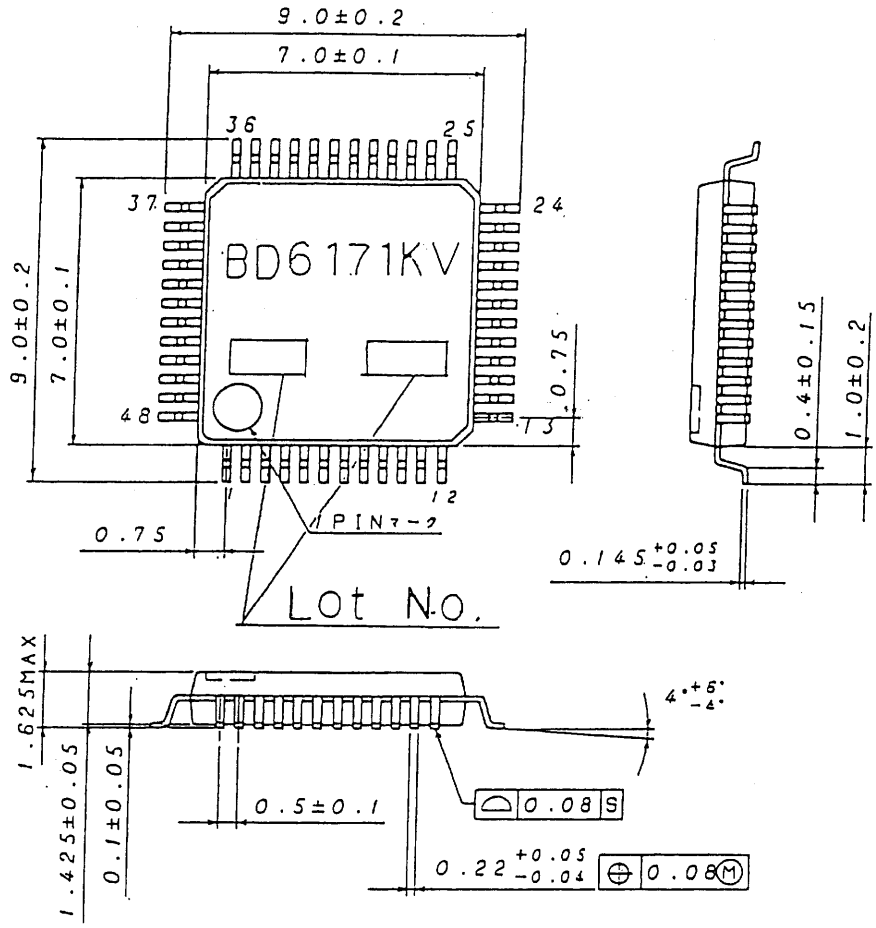
Specification	Symbol	Standard Value			Unit	Conditions	Measurement Circuit
		Min.	Standard	Max.			
【FET Driver】							
Output Source Current	IoSOURCE1,2	—	-100	—	mA	PVcc1,2-OUT1,2=0.4V	3
Output Sink Current	IoSINK1,2	—	100	—	mA	OUT1,2-VREGB=1.3V	3
PchON Resistance	RONP1,2	—	3.0	6.0	Ω	IOUT1,2=-100mA	3
NchON Resistance	RONN1,2	—	13.0	20.0	Ω	IOUT1,2=100mA	3
Rise Time	Tr1,2	—	20	—	nsec	When switching between PVcc1,2-OUT1,2 with a 1000 pF connection ※Design Assurance	3
Fall Time	Tf1,2	—	20	—	nsec	When switching between PVcc1,2-OUT1,2 with a 1000 pF connection ※Design Assurance	3
【Overcurrent Protection】							
VS Threshold Voltage	VVS1,2	VCC -0.22	VCC -0.20	VCC -0.18	V	RCL1,2=20KΩ	4
VS Inflow Current	IVS1,2	—	—	1	μA	VS1,2=PVCC1,2	4
CL Inflow Current	ICL1,2	9	10	11	μA	VCL1,2=13.2V	4
【Overcurrent Protection Cancellation】							
Charging Current	IOCPC1,2	-4.0	-2.5	-1.0	μA	VOCPC1,2=1.0V	4
Threshold Voltage	VOCPC1,2	1.9	2.0	2.1	V		4
Standby Voltage	VOCPCSTB1,2	—	0.6	1.0	V		4
【Input Undervoltage Malfunction Prevention】							
Threshold Voltage	VUVLO	5.6	5.7	5.8	V	Vcc sweep down	4
Hysteresis Voltage	VHYSUVLO	0.05	0.1	0.15	V		4
【Output Voltage Detection】							
Output Detection Voltage	VDET1,2	0.55	0.6	0.65	V	VINV1,2 Voltage	3
Hysteresis Voltage	VHYS1,2	0.1	0.2	0.3	V		3
Output High Voltage	VDETH1,2	VREGA -0.4	—	—	V	IDET1,2=-1μA	3
Output Low Voltage	VDETL1,2	—	—	0.4	V	IDET1,2=25μA	3

◎ The design of this device does not incorporate measures used to harden against radiation.

○ Electrical Properties (Ta=25℃, Vcc,DVcc,PVcc1,2,3=13.2V, PVcc4,5=8V, Fosc=500kHz, EN1～5=5V unless otherwise specified.)

Specification	Symbol	Standard Value			Unit	Conditions	Measurement Circuit
		Min.	Standard	Max.			
Charge Pump Unit							
【Output】							5
Output Source Current	IoSOURCE4,5	—	—	-10	mA	OUT4,5=PVCC4,5-150mV	5
Output Sink Current	IoSINK4,5	10	—	—	mA	OUT4,5=150mV	5
【Error Amp】							
Feedback Voltage (Positive Voltage)	VFB4	0.97	1.00	1.03	V		5
Input Bias Current (Positive Voltage)	IFB4	-1	—	—	μA	FB4=0.97V	5
Feedback Voltage (Negative Voltage)	VFB5	-0.03	0.0	0.03	V		5
Input Bias Current (Negative Voltage)	IFB5	-1	—	—	μA	FB5=-0.03V	5
【Output Voltage Detection】							
Output Detection Voltage (Positive Voltage)	VDET4	0.55	0.6	0.65	V	FB4	5
Hysteresis Voltage (Positive Voltage)	VHYS4	0.1	0.2	0.3	V		5
Output Detection Voltage (Negative Voltage)	VDET5	0.55	0.6	0.65	V	FB5	5
Hysteresis Voltage (Negative Voltage)	VHYS5	0.1	0.2	0.3	V		5
Output High Voltage	VDETH4,5	VREGA-0.4	—	—	V	IDET4,5=-1μA	5
Output Low Voltage	VDETL4,5	—	—	0.4	V	IDET4,5=25μA	5

◎ The design of this device does not incorporate measures used to harden against radiation.



(UNIT: mm)

Figure - 1 Outline Drawing

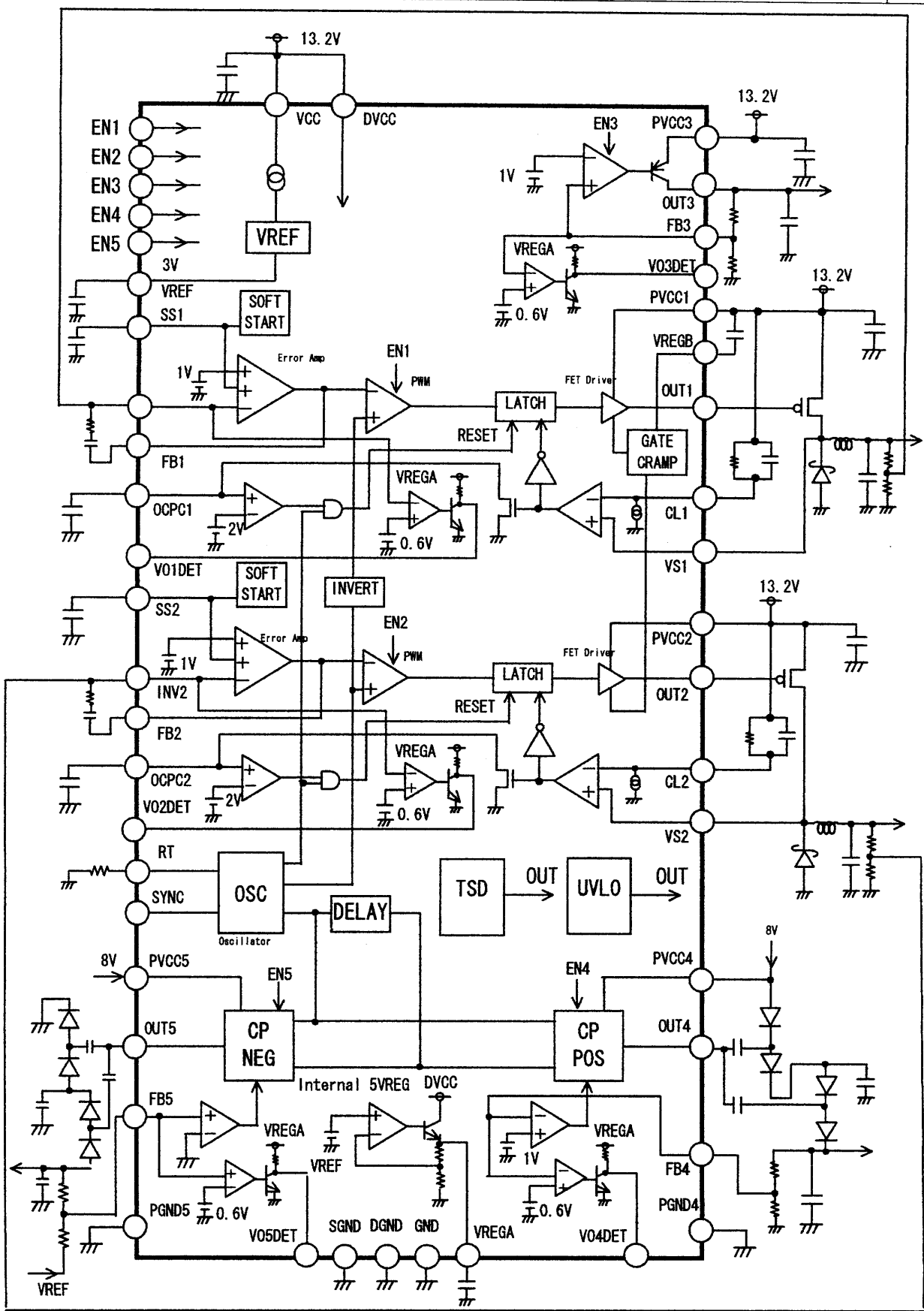
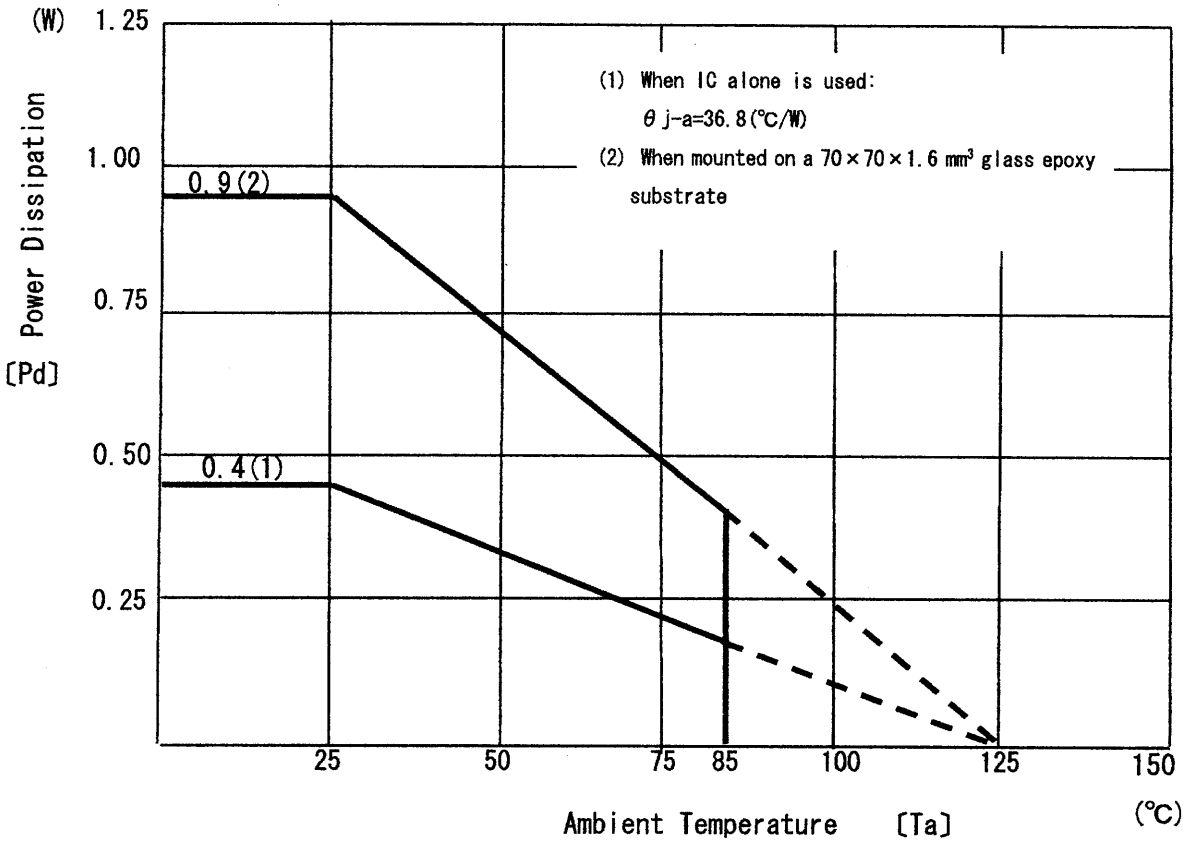


Figure - 2 Block Diagram

○ Heat Dissipation Graph



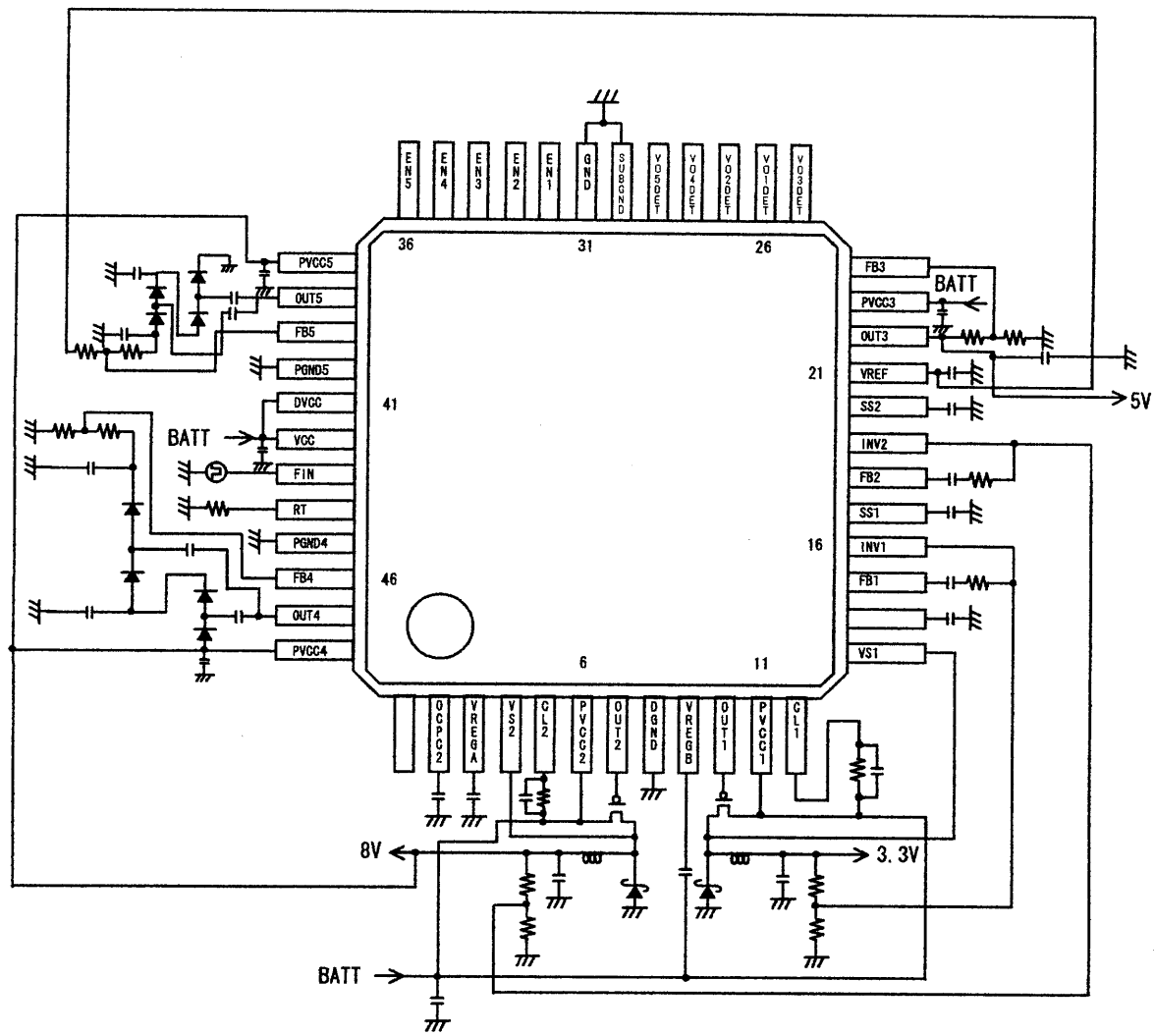


Figure - 3 Pin Plot Diagram (Example of Recommended Circuit)

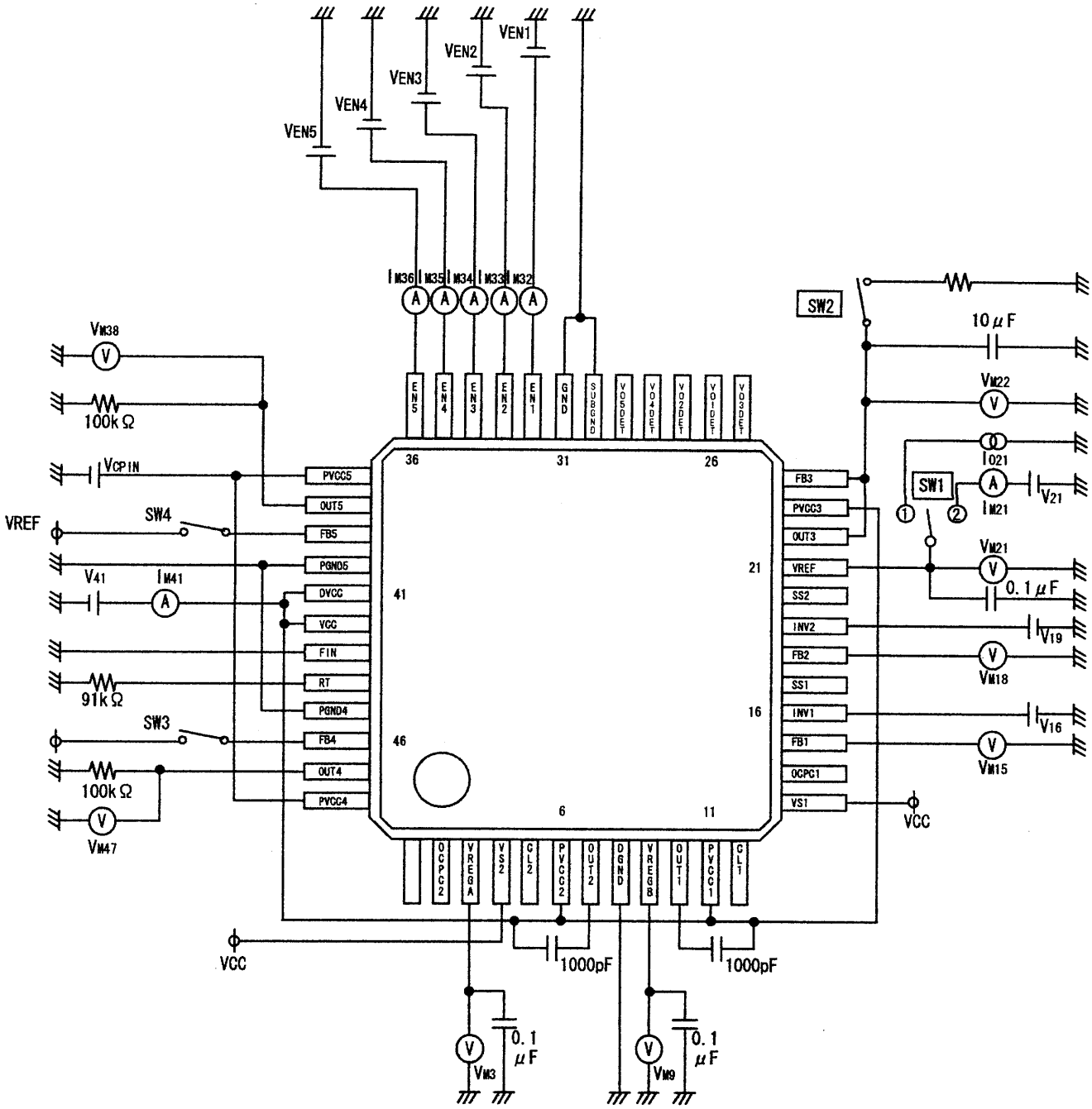


Figure - 4 Measurement Circuit Diagram - 1

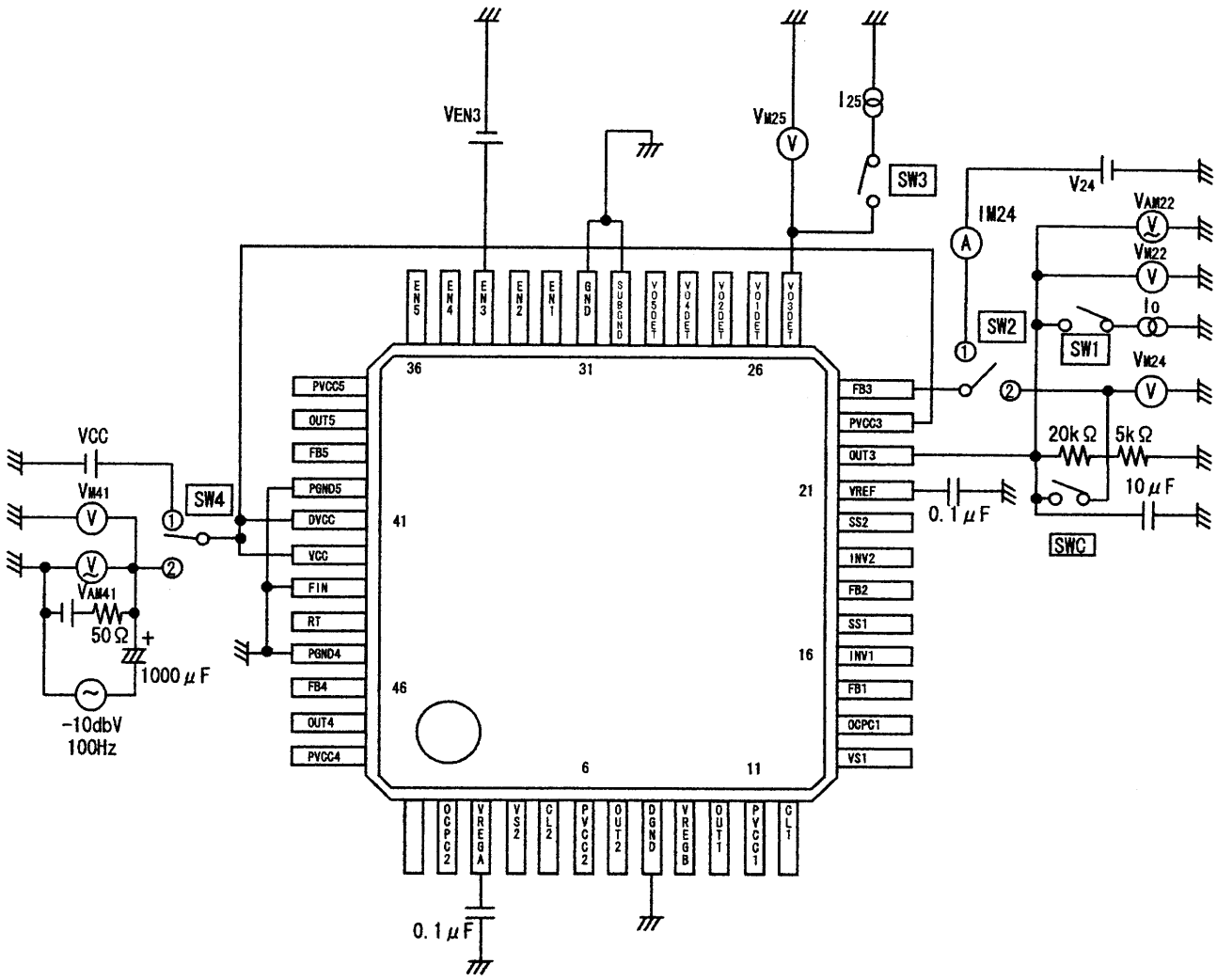


Figure - 5 Measurement Circuit Diagram - 2

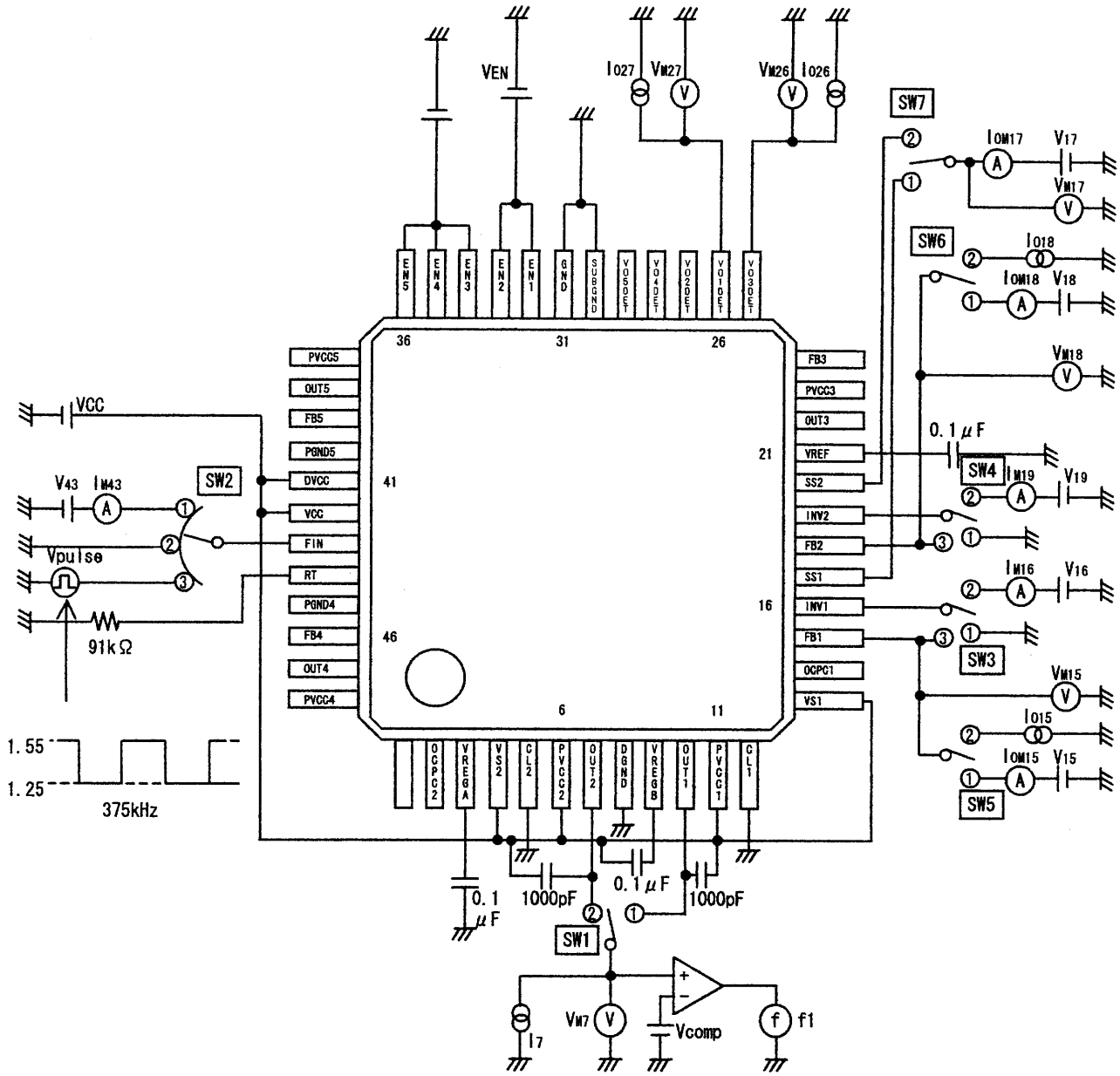


Figure - 6 Measurement Circuit Diagram - 3

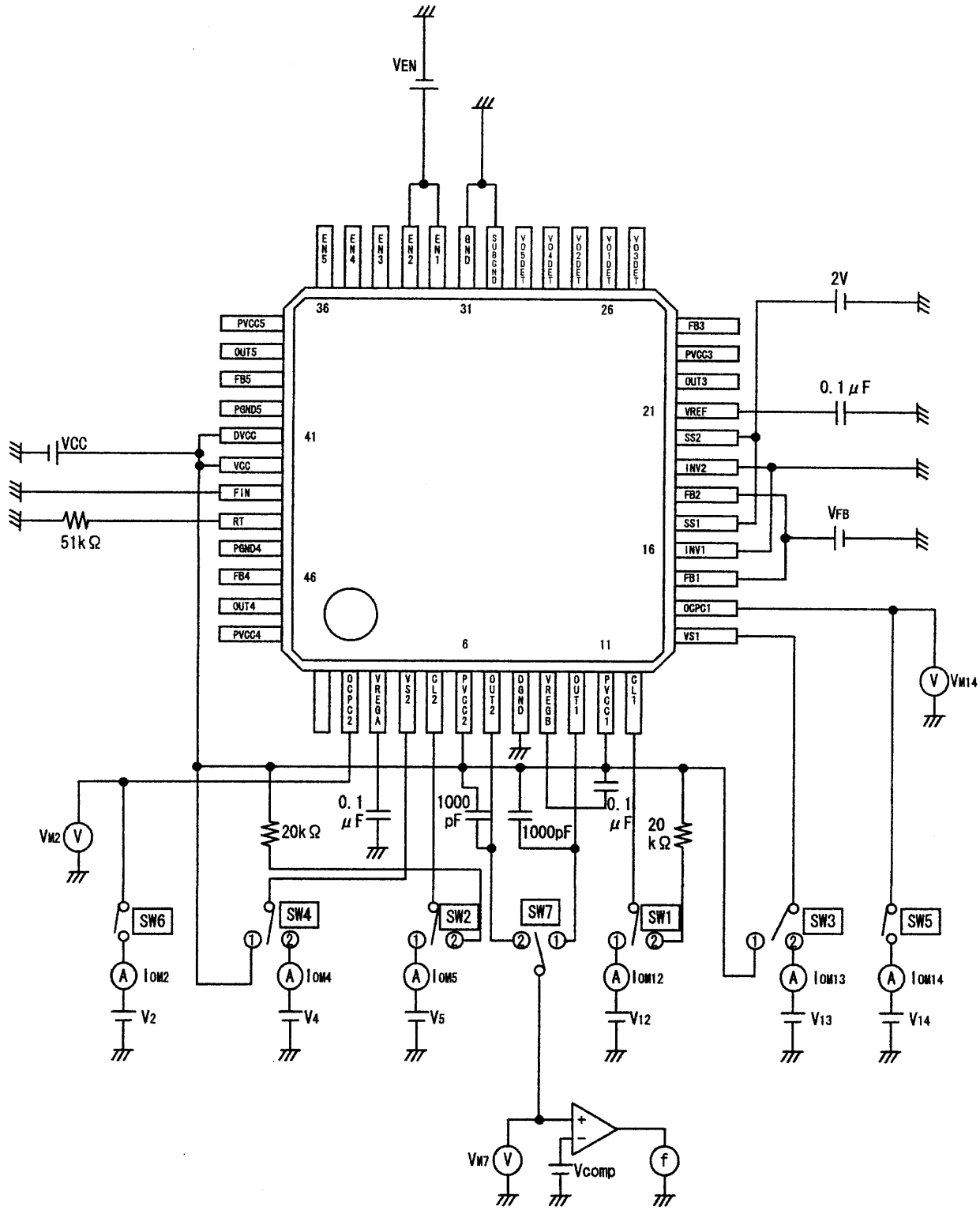


Figure - 7 Measurement Circuit Diagram - 4

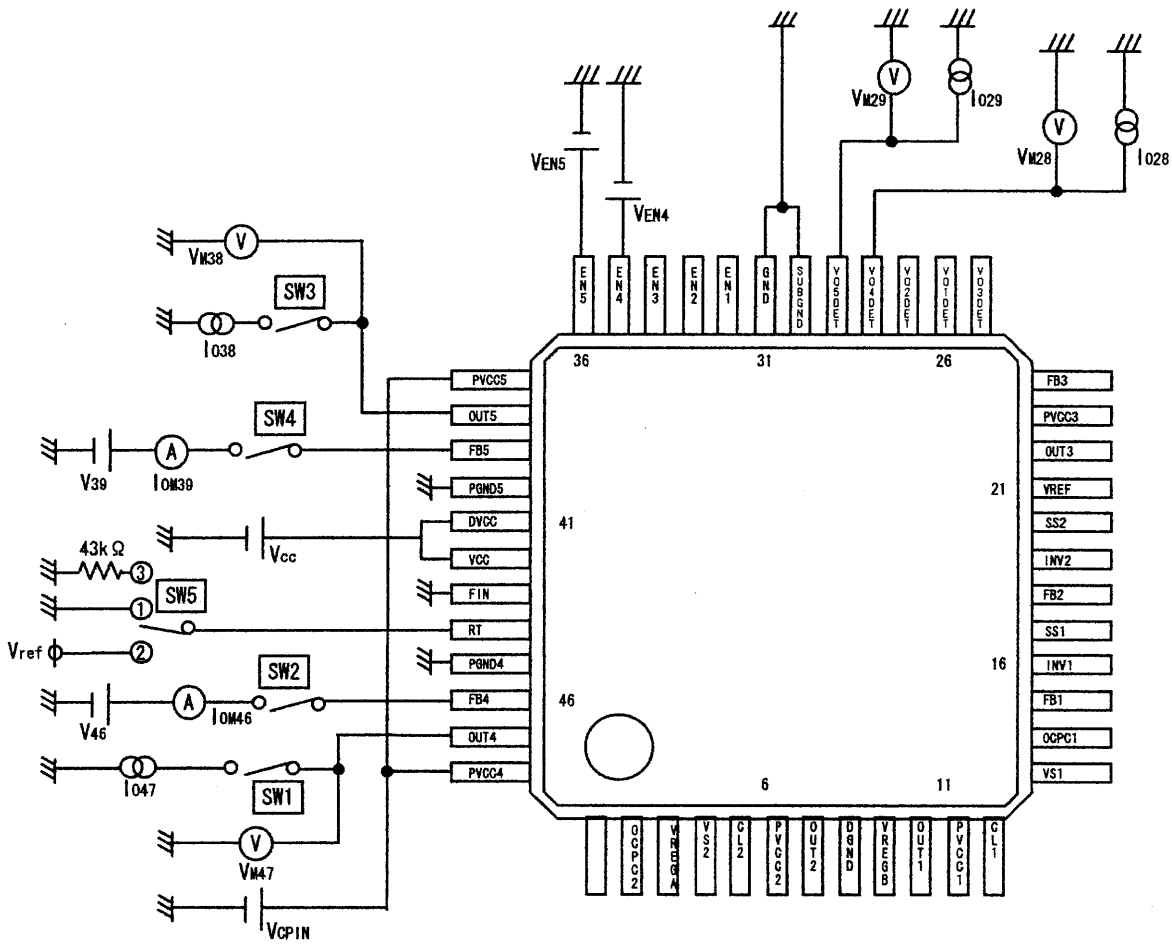
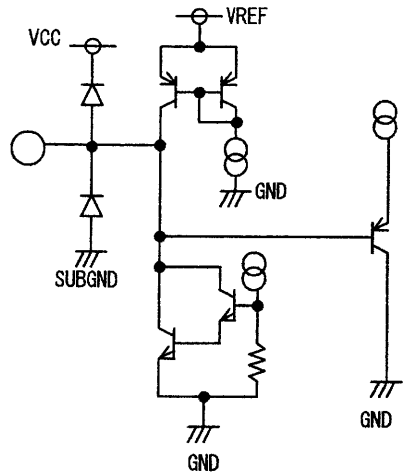


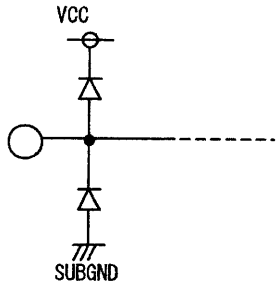
Figure - 8 Measurement Circuit Diagram – 5

○ Terminal Internal Equivalence Circuits

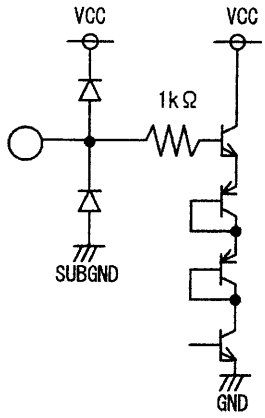
・OUTC2(2pin), OUTC1(14pin)



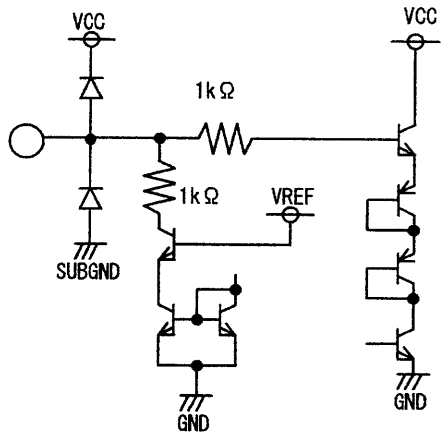
・VREGA(3pin)



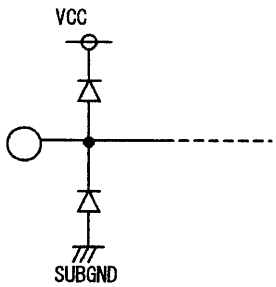
・VS2(4pin), VS1(13pin)



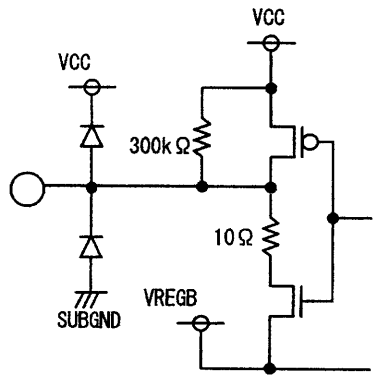
・CL2(5pin), CL1(12pin)



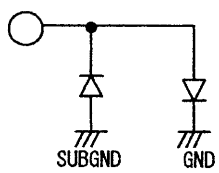
・PVCC2(6pin), PVCC1(11pin)



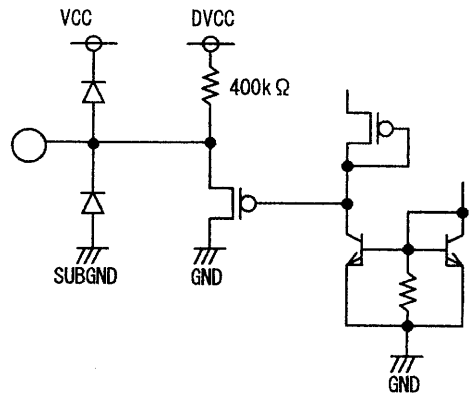
・OUTH2(7pin), OUTH1(10pin)



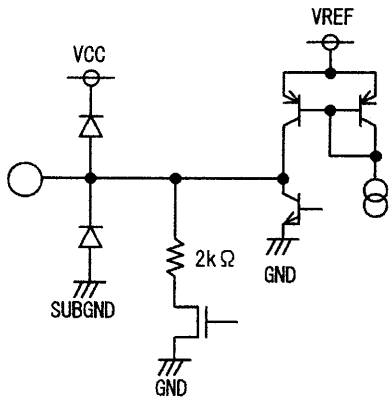
・DGND(8pin)



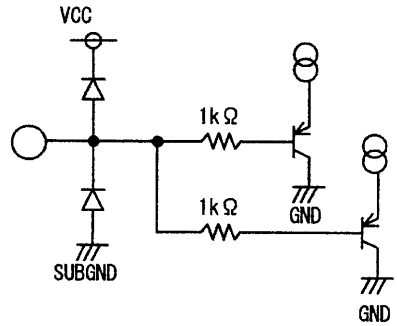
・VREGB(9pin)



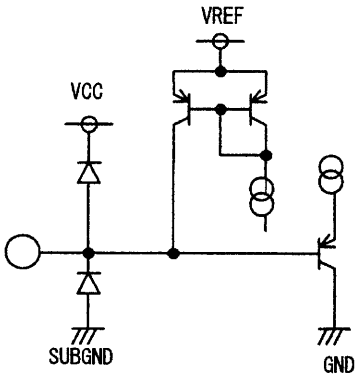
・FBI(15pin), FB2(18pin)



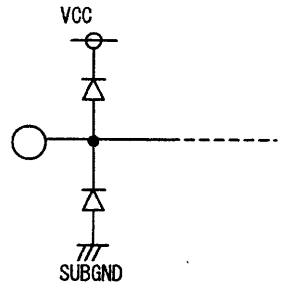
・INV1(16pin), INV2(19pin)



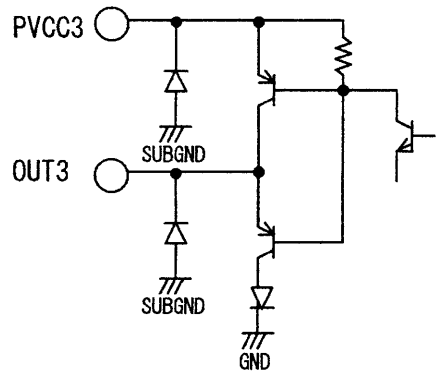
・SS1(17pin), SS2(20pin)



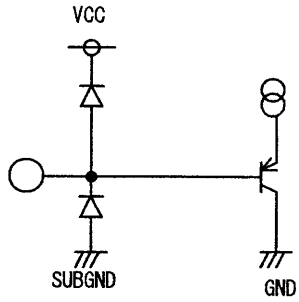
・VREF(21pin)



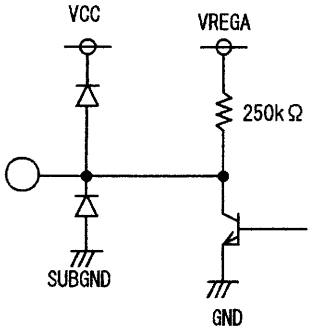
・OUT3(22pin), PVCC3(23pin)



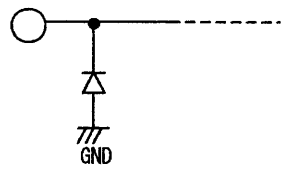
・FB3(24pin)



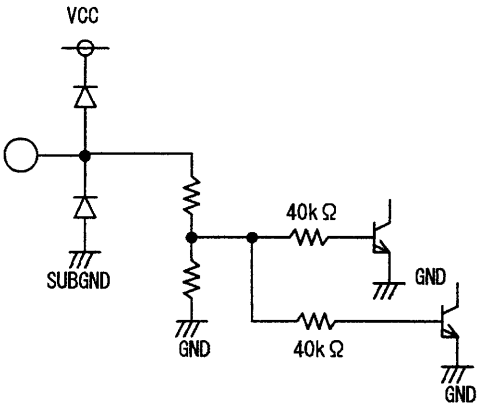
・VoDET(25～29pin)



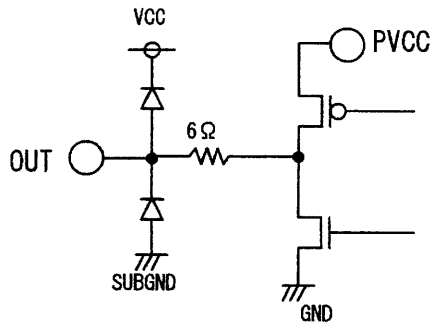
・SUBGND(30pin)



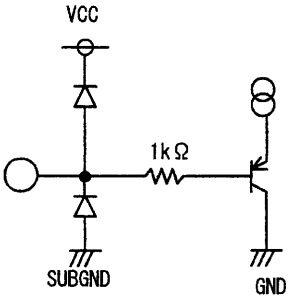
・EN1～5(31～36pin)



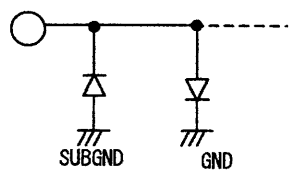
・PVCC5(37pin), PVCC4(48pin), OUT5(38pin), OUT4(47pin)



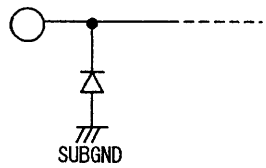
・FB5(39pin),FB4(46pin)



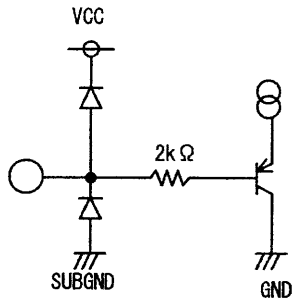
・PGND5(40pin), PGND(45pin)



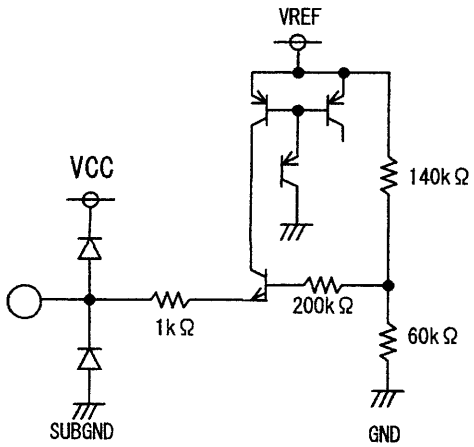
・VCC(42pin)



・FIN(43pin)



・RT(44pin)



O Explanation of Each Function (Typical values are used for all numeric values below.)

1. PWM Controller Functions

(1) Reference Voltage Block
This circuit generates a constant, temperature-compensated voltage from the power input supplied to the VCC terminal. The voltage is 3V.

(2) Internal Regulator Block (VREGA)
This circuit generates a 5V voltage from the power input supplied to the VCC terminal. A low ESR capacitor must be connected between VREGA−GND.

(3) Internal Regulator Block (VREGB)
This circuit generates a voltage (Vcc-5V) from the voltage supplied to the VCC terminal. This voltage serves as the voltage supply for the main FET driver unit. A low ESR capacitor must be connected between VREGB−VCC.

(4) Oscillator Block
This circuit generates a triangular waveform via the connection of a resistance, which is used to set the frequency, to the RT terminal. It allows for external synchronization of the oscillator via the input of a pulsed waveform to the SYNC terminal, at a frequency higher than the specified oscillator frequency, thus enabling the fine adjustment of the oscillator frequency (within 25%).

(5) Error Amp Block
This circuit detects the output voltage at the INV terminal, amplifies the error in relation to the output voltage setting and then outputs the resulting error voltage from the FB terminal.
The comparison voltage used is 1V.
An arbitrary degree of phase compensation can be specified externally by connecting a resistance and a capacitor between the INV terminal and the FB terminal.

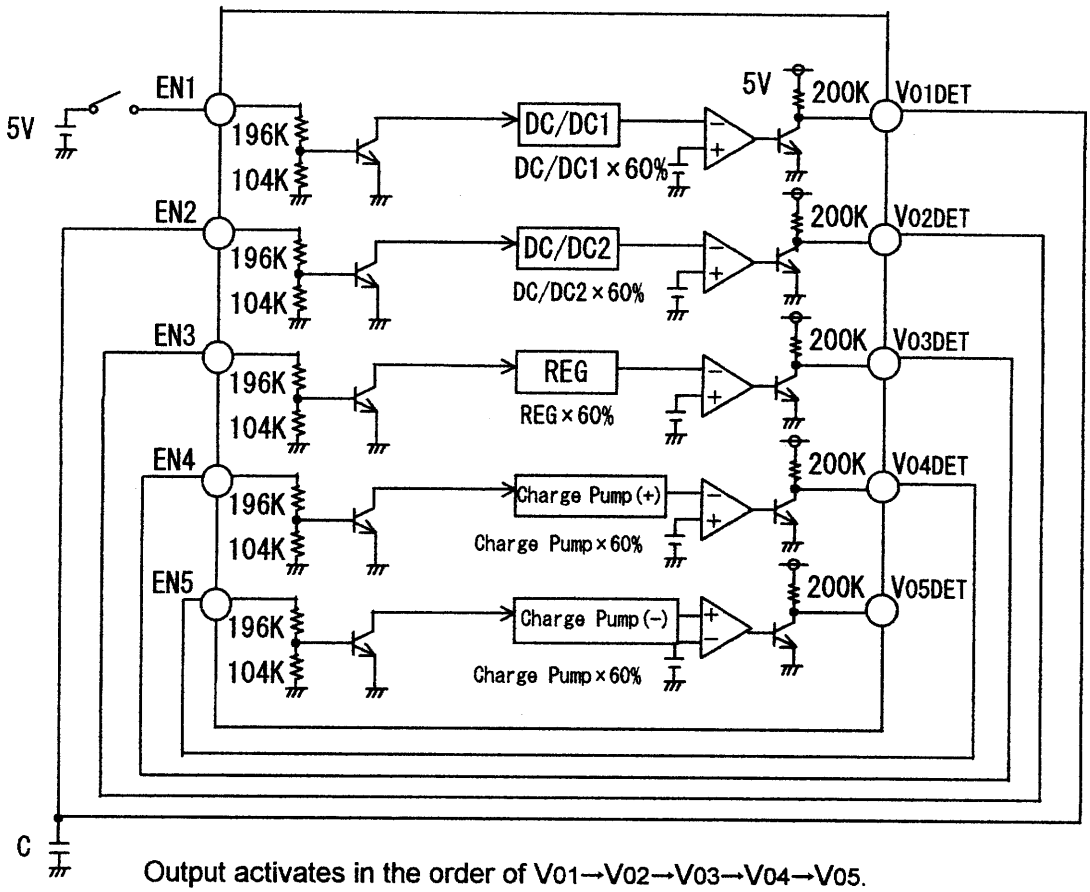
(6) PWM Comparator Unit
This unit converts the voltage output from the error amp into a PWM waveform and then outputs it to the FET driver.

(7) FET Driver Unit
Outputs are driven by Pch FETs, with all outputs being push/pull.
Each output voltage is clamped by the VREGB output voltage.

2. Channel Control Function

Each output can be controlled individually, via terminals EN1 - EN5.
As well, by connecting the DET terminal of each output to terminals EN1 - EN5, the order of activation can be controlled arbitrarily for each output.

(Example)



Output activates in the order of VO1→VO2→VO3→VO4→VO5.

Furthermore, when the activation of each output must be delayed, a specific delay time can be set by connecting a capacitor C to an EN terminal, as shown in the diagram above.

3. Protection Functions

(1) Overcurrent Protection Circuit (OCP)

In the DC/DC unit, if the external Pch MOS drain voltage drops to a lower value than the specified external voltage when the output FET is ON, this circuit will cause the output to latch OFF.
Subsequently, this circuit begins to charge the capacitor connected to the OCPC terminal. Once the capacitor reaches 2.0V, the latch OFF operation will cancel and the circuit will reactivate. At that time, if the unit is still in the overcurrent condition, the output will turn OFF. If the unit has returned to normal load conditions, then normal operation will resume.

(2) Input Undervoltage Malfunction Prevention Circuit (UVLO)

In order to prevent the IC from malfunctioning during power-up or during a power interruption, whenever the supply voltage decreases to approximately 5.7V or less, this circuit turns all of the outputs off. There is approximately 0.1V of hysteresis width between the detection voltage and the UVLO cancellation voltage, thus preventing malfunctions due to input voltage fluctuations at the threshold online.

(3) Overheating Protection Circuit (TSD)

This circuit detects any excess chip heat and turns all of the outputs off, in order to prevent IC damage.
A hysteresis width is present between the overheat detection temperature and the cancellation temperature, thus preventing malfunctions caused by temperature fluctuations at the threshold online.

4. Oscillator External Pulse Synchronization Function

Permits external pulse synchronization of the oscillator through the connection of a resistance to the RT terminal and the input of a synchronizing signal to the SYNC terminal.
The input must be a pulse waveform having a higher frequency than that determined by RT.
However, the frequency differential must be specified to within 25%.
In addition, the duty cycle of the pulse signal must be set within the range of 10% - 90%.

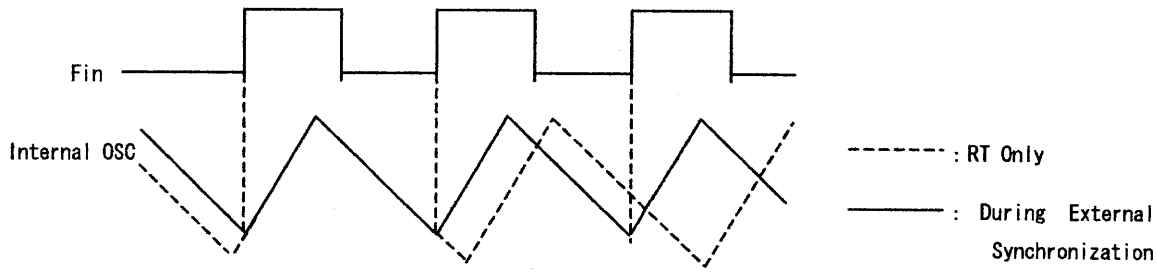


Figure - 9 CT Waveform During External Pulse Synchronization

If the external synchronization function is not utilized, the SYNC terminal must be shorted to GND.

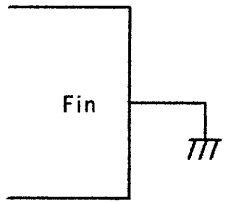
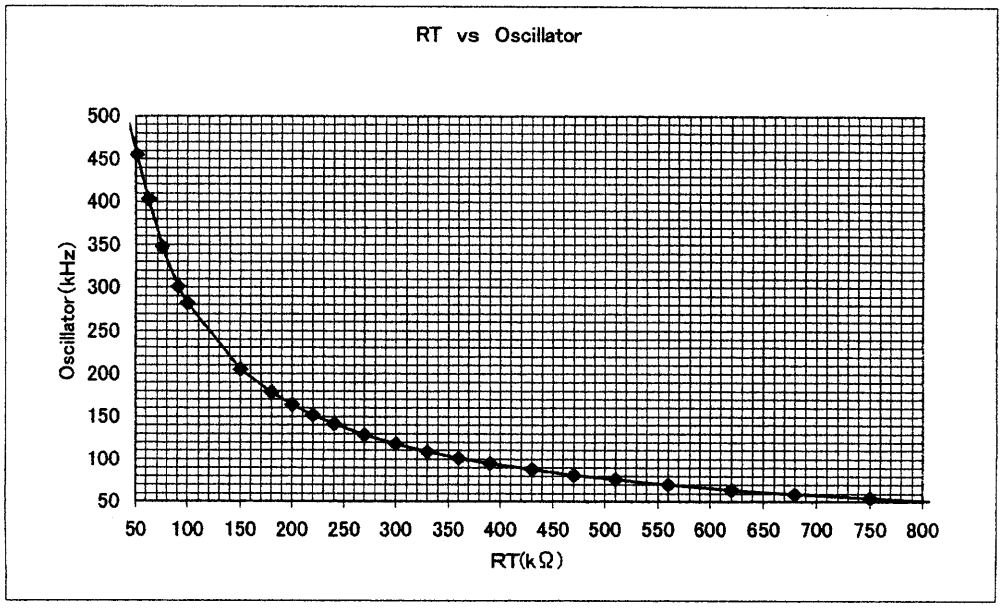


Figure - 10 If External Synchronization Function is Not Utilized

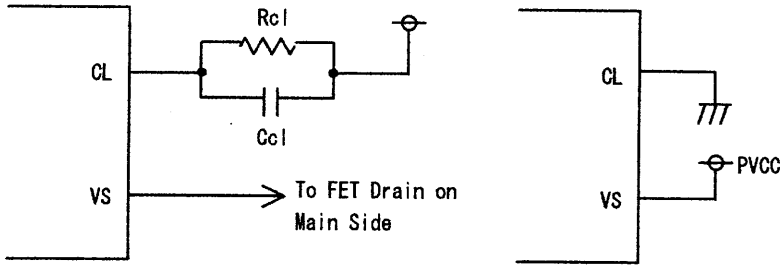


5. Setting the Overcurrent Detection Level

The level of overcurrent detection for the overcurrent protection circuit (Iocp) is determined by the resistance connected to the ON-resistor (RON) of the external main FET and the resistance connected between CL-VCC (Rcl).

$$Iocp = \frac{RCL}{RON} \times 10^{-5} \quad [A] \quad (typ.)$$

In addition, a capacitor (Ccl) must be connected in parallel to Rcl, in order to prevent incorrect detection due to noise.
If the overcurrent protection circuit is not utilized, the VS terminal must be short-circuited to PVCC and the CL terminal must be short-circuited to GND. (Refer to Figure 11)



If Overcurrent Protection Circuit is Used If Overcurrent Protection Circuit is Not Used

Figure - 11 CL and VS Terminal Connections

6. Setting the Timer to Reset Overcurrent Protection

The time required for the unit to reset from the overcurrent protection state (Tocprst) is determined by the size of the capacitor (Cocp) connected to the OCPC terminals.

$$Tocprst \fallingdotseq 8 \times 10^{5} \times Cocp \quad [sec] \quad (typ.)$$

7. Setting the soft start timer

The soft start time is determined by the size of the capacitor (Css) connected between SS1, SS2 to GND.

$$Tss = \frac{Vss \times Css}{Iss}$$

The soft start is from VIN standup to Output voltage 100%.

8. Connecting Channel Terminals If DC/DC Is Not Used

If DC/DC is not utilized, connect the terminals as shown below.

FB ⟶ Short-circuit to GND
INV ⟶ Short-circuit to VREF
EN ⟶ Short-circuit to GND

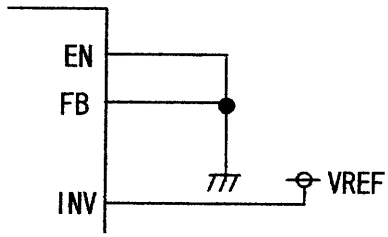


Figure - 12 Connecting Channel Terminals If DC/DC Is Not Used

9. Setting Output Voltage For OUT3

The output voltage for OUT3 can be determined by using the formula shown below.

$$V_{OUT3}=\frac{R_1+R_2}{R_1}$$

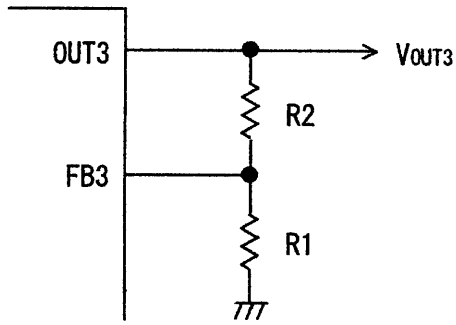


Figure - 13 Setting Output Voltage For OUT3

The output voltage for OUT3 must be set to 10V or less using R1 + R2 values that are equal to or less than 3kΩ.

10. Setting Output Voltage For OUT1,2

The output voltage for OUT1,2 can be determined from the formula below.

$$V_{OUT1,2} = \frac{R1+R2}{R1}$$

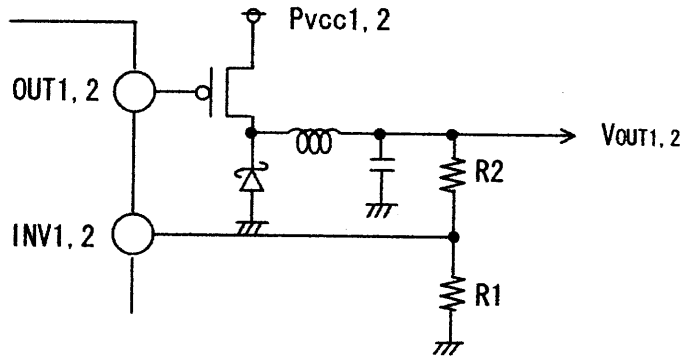


Figure - 14 Setting Output Voltage For OUT1,2

11. Setting Output Voltage For OUT4,5

The output voltage for OUT4,5 can be determined from the formula below.

$$V_{OUT4} = \frac{R1+R2}{R1} \qquad V_{OUT4} = -Vref \times \frac{R2}{R1}$$

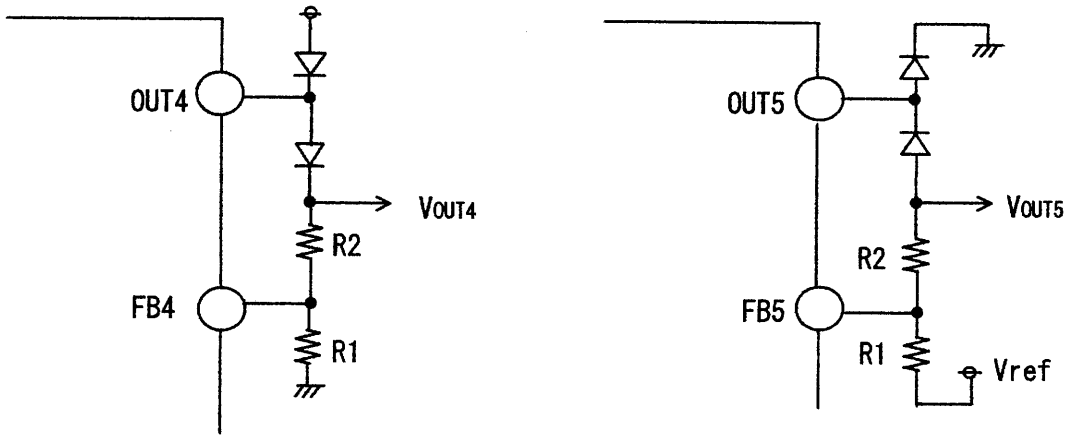
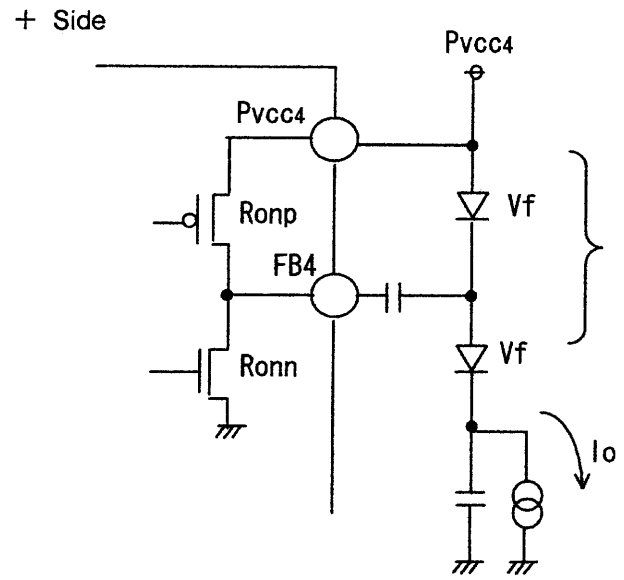


Figure - 15 Setting Output Voltage For OUT4,5

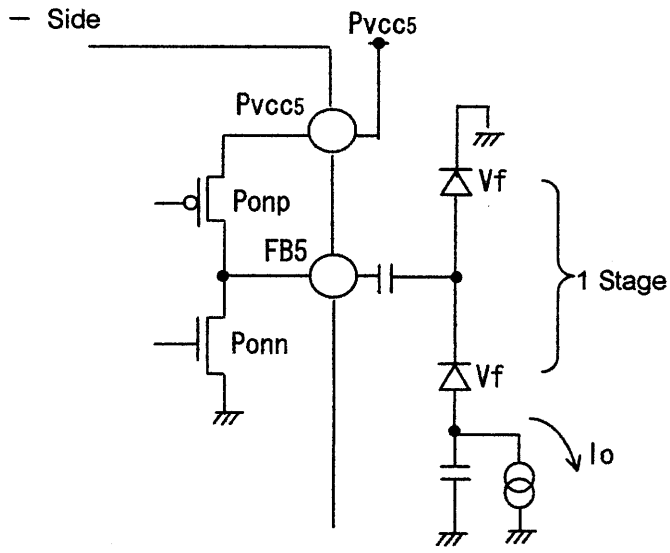
In addition, the charge pump must be configured in a manner such that its voltage is sufficiently greater than Vo, which is determined as shown below.



$$Vo=(n+1)\times PVcc4-n\times 2\times Vf$$
$$-2\times(Ronn+Ronp)\times Io\times n^2$$

n: Number of Diode Stages (1 stage for every 2 diodes)
Vf: Correct Diode Polarity Voltage
Io: Negative Current

Figure - 16 Setting the (+) Side Charge Pump



$$Vo=-n\times PVcc5+n\times 2\times Vf$$
$$+2\times(Ronn+Ronp)\times Io\times n^2$$

n: Number of Diode Stages (1 stage for every 2 diodes)
Vf: Correct Diode Polarity Voltage
Io: Negative Current

Figure - 17 Setting the (−) Side Charge Pump

Precautions For Usage

1. Although these devices have been manufactured under strict quality control conditions, if any of the absolute maximum ratings are exceeded, such as for the applied voltage or operating temperature range, the devices may malfunction or be damaged. If a malfunction occurs, no assumptions can be made for any special modes of operation, such as short mode or open mode. In the event that a special mode of operation is required, in which the absolute maximum ratings may be exceeded, it is recommended that physical safety measures be implemented.

2. Information About The Operating Supply Voltage Range
   As long as the circuit is supplied with power within the operating supply voltage range, all circuit functions are guaranteed for operation within the ambient operating temperature range. With respect to the values for electrical properties, although particular standardized values cannot be guaranteed, abrupt fluctuations in electrical property values will not occur within these ranges.

3. Information About Grounding
   The configuration of each ground circuit shown in the circuit application examples must be kept as short as possible, for connection to the ground pin (GND). Furthermore, the configuration must not be susceptible to electrical interference.

4. Information About Input Power
   The configuration of the input power circuit shown in the circuit application examples must be kept as short as possible, for connection to the input pin VCC. Furthermore, the configuration must not be susceptible to electrical interference.

5. Information About The Bypass Capacitor Between VCC−GND
   It is recommended that a bypass capacitor be connected between each VCC terminal and GND, located as close to the pins as possible.

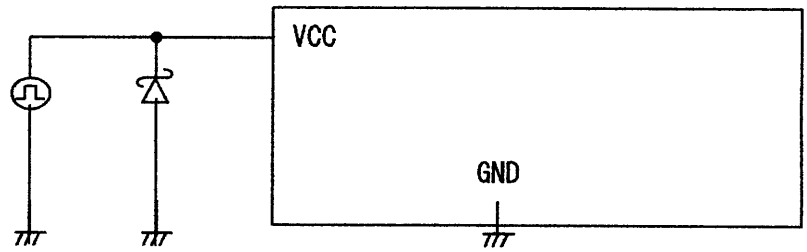
6. Information About The FB Terminal
   The FB terminal determines the phase margin of the DC/DC system. Connect either a capacitor or a capacitor and resistor combination between the INV terminal and the FB terminal. As each set value changes depending upon the output coil, the capacitance, the input/output voltages and the load, adjust each value to its optimum, in accordance with these conditions.

7. Information About Operation Within Electromagnetic Fields
   Please note that the device may not function correctly if used in the presence of strong electromagnetic fields.

8. Information About Applications
   When the device is used with external circuitry, ensure that sufficient spacing and margin for adjustment is available for performing external circuit settings.

9. Information About Power Dissipation (Pd)
   Please refer to the heat dissipation characteristics described within these specifications (8/29) and ensure that your application design does not exceed the specified maximum power ratings, for the appropriate operating temperature range.

10. Information About Negative Surges Applied To The VCC Terminal
In the event that the voltage at the VCC terminal may fall to a value lower than that at the GND terminal, a protection diode (D1) must be connected between the VCC and GND terminals, as shown in the figure below.



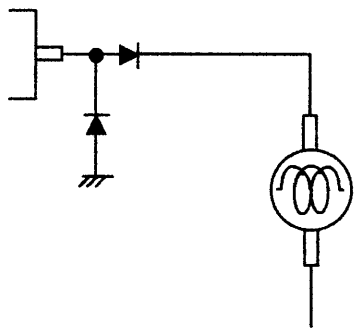
11. Information About The Overcurrent Protection Circuit
The REG3 output terminal incorporates an overcurrent protection circuit that prevents against IC malfunction in the event of an overcurrent condition. The OCPC has a "hanging J shape" and limits the flow of electrical current. The IC has been designed with sufficient margin such that it will not latch up, even in the event of a high transient current flow released from a large-value capacitor. In addition, when the output voltage is 1V or less, the output is considered to be in short mode, thus further limiting the output current. Please ensure that the output voltage is carefully verified for the design of each application.

12. Information About The Built-in Thermal Protection Circuit
The device incorporates a thermal protection circuit that prevent against IC malfunction due to excess heat. If the temperature rises excessively, all outputs will enter the OFF state. Once the temperature returns to normal, the device will return to normal operation.

13. If the device is used in a mode where a reverse electrical potential is applied to the input (VCC), to GND and to individual outputs, or if a special operation is performed causing electrical current to flow into the output terminals, then the IC may malfunction. It is recommended that bypass channels and diodes be utilized to prevent reverse current flow. Under normal usage conditions no such problems will occur.

14. If the possibility exists that back electromotive force may be produced during either start-up or when outputs are OFF, and if loads containing large inductive components are present at the output terminals, then ensure that diodes are utilized for protection.

(Example)



15. This device is a monolithic IC, thus has a P substrate and possesses P+ isolation between each element. The P-N junctions are formed from both the P layers and the N layers of each element, thus comprising a variety of parasitic elements.

For example, when a resistor and transistor are connected to the terminal, as shown in Figure – 9;

- The P-N junction functions as a parasitic diode when: GND > (Terminal A) for the resistor and GND > (Terminal B) for the transistor (NPN).
- Also for the transistor (NPN), when GND > (Terminal B), parasitic NPN transistor function will occur within the "N" layer of other elements that are adjacent to the abovementioned parasitic diode.

Due to the configuration of the IC, the effects of parasitic elements will inevitably occur, derived from the relationship between the potentials. The effects of parasitic elements interferes with circuit operation, thus may cause malfunctions or even permanent circuit damage. Please ensure that the device is not utilized in a manner that promotes parasitic element function, such as by applying voltages of less than the GND potential (P substrate) to the input/output terminals.

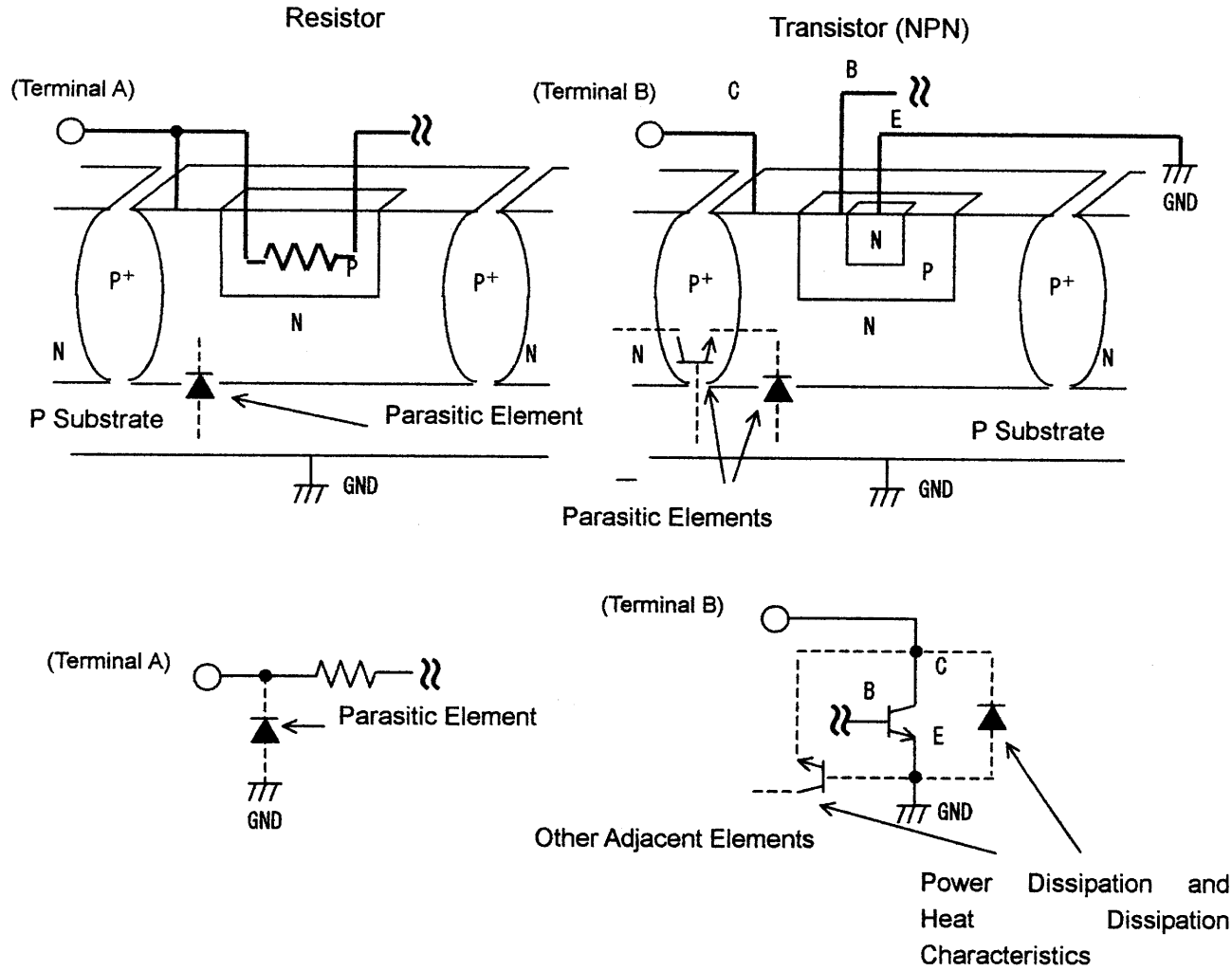


Figure - 9

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